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# Profile

Hardware/Firmware Engineer, Leader and Manager, pragmatic and responsible. Passionate about FPGA, Electronics and Cutting Edge Technology. Responsible for designs and leadership through the complete lifecycle. Offering FPGA and Electronic design Engineering, technical leadership and coaching.

# Key Skills

**Chief Engineering:** Responsibility for and management of Systems, Software, Firmware, Electrical and Mechanical Engineering. Process improvement. Quality conformance.

**Leadership:** Line Management,Large Teams, Resource Management, Recruitment, Appraisals, Performance Development, Project Management.

**Rugged Electronics:** Military and Aerospace: DO160, MIL-STD 704, DEF-STAN 61-5, DEF-STAN 00-35, DEF-STAN-59-411, MIL-STD 810, MIL-STD-461, EN60950.

**Hardware design**: Requirements, specifications and design verification (DOORs). Manufacturing test. Schematic-capture (Cadence, DxDesigner, PADS, OrCAD), supervision of layout. Analog, low noise audio frequency. Signal integrity techniques and simulation (ICX, Hyperlynx). Power supply and distribution design. PSPICE, LTSpice. Component Engineering and de-rating. Processing architecture design (OEM components, Nvidia Tegra, Intel Skylake, Intel Broadwell, FPGA, DSP, Processors). Interfaces: 10GBase-T, 1GBase-T, MGT, Serdes,SDR, DDR and DDR2 SDRAM, QDRII SRAM, FLASH; GTP, PCI, PCI-X Firewire, LVDS, CML, EMIF, McBSP, I2C, OneWire.

**HDL design:** Design: Audio processing, UMTS Baseband data, Test engine design. Interfaces: AMBA, PCI, DDR, DDR2, QDRII, FLASH, TI EMIF and McBSP), Test benches. Languages: VHDL, Verilog. Tools: Modelsim / Questa, Libero, ISE, Vivado, QuartusII, NIOSII SOPC Builder. FPGA: MicroSemi Smartfusion2, Altera Cyclone V, Cyclone IV NIOSII SOPC builder, Xilinx Kintex-7, Virtex-5, Virtex-4 and VirtexII. CPLD: Lattice Mach4000, Altera MAXII.

**Software / Scripting:** Linux, Embedded C and assembler. TCL scripting, Python, Perl, proprietary scripting tools, Excel Macros. Batch and Bash scripts.

**EMC / RF Test:** Solving EMC problems. Designing and carrying out tests for UMTS and CDMA base stations. Channel configurations, protocol testers, spectrum analysers, test mobiles together with RF cables.

**Subcontract Manufacture:** DFM, liaising right through supply chain, Managed and supported multiple CEMs overseas and locally to meet production and rework needs.

# Positions / Contracts

**Cambridge Quantum Computing Ltd 25/02/2019 – present**

**Electronic Design Consultant**

BMC. Analog switching, power supply and Digital/FPGA design. Hardware design using KiCad, Altium, PSPICE, LTSpice. Firmware design using Xilinx Zynq.

**Drumgrange Ltd 19/06/2017 – present**

**Electronic Design Consultant**

Low noise analog signal, power supply and Digital/FPGA design. Engineered a variety of assemblies and PCBs for a low-noise high precision audio monitoring system. Hardware design using OrCAD, PSPICE, LTSpice. Firmware design using OrCAD, Modelsim, Xilinx Spartan 6.

**Abaco Systems Ltd** (formerly GE Intelligent Platform Systems Ltd) **17/09/2015 – 14/06/2017**

**Electronic Design Consultant**

NVIDIA Linux for Tegra, 10GBase-T, EMC problem solving, Electronic and FPGA design, Embedded C with Microsemi SmartFusion2 SOC (FPGA Fabric + ARM Cortex-M3) on single board computer (SBC) products, Intel Skylake and Intel Broadwell. Design entry, design review and requirements capture (DOORS).

**Britannia2000 Ltd 02/02/2015 – 31/07/2015**

## Chief Engineer / Manager

Led a multi-disciplinary team designing rugged optical and video systems plus Windows applications. Recruited to fill skills gaps. Managed customer funded projects and ensured successful design reviews. Customer facing. Ensured successful delivery from Engineering through to Production. Championed process improvement and encouraged a culture of efficiency savings.

## Projects

Rugged soldier mounted digital video receiver (MIL-810G, MIL-461)

Airborne DVR system (DO160)

Rugged computer (DO160)

**Ultra Electronics Ltd Communication and Integrated Systems 25/03/2013 – 22/01/2015**

### Hardware Lead

Responsible for three teams, electronic, mechanical and technician. Led a team of electronic design engineers developing high grade crypto. Responsible for hardware and maintaining correct resource levels to match business need. Responsible for engineering sign-off and providing skilled engineers into project teams within a matrix management structure. Training and development of high potential staff.

Responsible for ensuring reviews of requirements, design, schematics and layout, are carried out accurately and according to process.

## Projects

* End Cryptographic Unit Replacement Program (ECR-RP) (MAA, MIL-STD-704, DEF-STAN-00-35, 59-411, 61-5, SDIP-25)

## Training

Product design for EMC 9th to 11th Dec 2013. Held at Ultra Electronics. With Tim Williams

MAD1 Influencing, Negotiation and Feedback Skills. 26th to 27th Feb 2014. OPDC

MAD2 Leading and working in teams. 25th to 26th March 2014. OPDC

MAD3 Coaching and Developing Others. 12th to 13th November 2014. OPDC

## Curtiss-Wright Controls (formerly VMETRO UK Ltd) 06/01/2006 – 23/03/2013

### Electronic Design Engineer

Designed and developed rugged DSP COTS products. Responsible for hardware design, management of layout and manufacturing, design verification testing, manufacturing test development, HDL design and coding, manual writing and support. Took ownership of complex products developed at other sites. Worked with teams in other disciplines to solve thermal, mechanical, component, and production issues.

#### Major Projects

* Audio ADC, DAC PMC. Altera Cyclone IV NIOS II.
* Lead Design Engineer on 6U VPX multiple Virtex-5 SXT based card.
* Expert Engineer on 6U VPX dual PPC, Virtex-5 based card.
* Lead Design Engineer on ‘Early Access’ Virtex-5 LX based PMC card.

## Lucent Technologies (Now Alcatel – Lucent 18/9/2000 to 31/12/2005

### Senior Hardware Engineer (4/2002 – 12/2005)

**FPGA Design:** Virtex4 test images: EMIF, McBSP, DDR controller, PCI, LVDS. Collaboration with Xilinx Virtex4 early access program. Supported Baseband Combiner FPGA (VirtexII).

**Hardware Design:** Virtex4 FPGA, TMS320C64x/TMS320TCI100, SDRAM DDR / SDR, Dual PPC, MPX, PCI, PPMC, McBSP, Ethernet, Firewire and Device bus. Hardware design developed from requirements to specifications and block diagrams, schematics. Timing analysis, signal integrity simulations, aiding layout and routing. DVT.

**Hardware Architecture:** Proposals and evaluations of hardware architectures. Evaluated integrated silicon solutions. Wrote requirements. Represented hardware issues in cross-functional teams.

**System Analysis:** E-DCH, HSDPA, Voice traffic and other 3GPP traffic. Quantitative analysis of maximum/realistic call/code scenarios identifying system bottlenecks. Latency analysis in DSP architecture proposals. Firewire, PCI and local bus load testing.

**UMTS Conformance Tests:** UMTS RACH TS 3GPP 25.141

### CDMA UDT Integration Engineer (10/2001 – 4/2002)

**Integrating** CDMA platform with UDT. Contributed to software specifications and provided reference scripts. Bringing up CDMA channels to verify performance.

**UMTS** test support. Test environment for RACH conformance testing and support of end users.

RACH layer 1 baseband performance testing.

### DSP Software Engineer (18/9/2000 – 10/2001)

Integration of NodeB platform.

Test development, and the automation of regression testing.

Involved in introduction of internally developed test tool. Influencing, demonstrating and training a multinational DSP team in the use of the tool.

### External Courses Attended

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| **Course** | **Duration** | **Description** |
| **TI TMS320C54x** | 4 days | Architecture and semantics of coding TMS320 C54x DSP. |
| **Lucent 16400** | 3 days | Architecture and semantics of coding Lucent 16400 DSP. |
| **OSE workshop** | 1 day | Using the OSE real time operating system. |
| **GSM Air Interface** | 3 days | Wray Castle training on the GSM Air interface. |
| **UMTS Air Interface** | 3 days | Wray Castle training on the UMTS Air interface. |
| **Xilinx Extreme DSP** | 3 days | DSP techniques and their implementation on an FPGA. |
| **Xilinx PCI Basics** | 3 days | PCI and implementing PCI on a Xilinx FPGA. |
| **Xilinx Rocket IO** | 2 days | Rocket IO and Xilinx VirtexIIPro |

## Tandberg Television / NDS 30/10/1998 to 15/9/2000

## Post Development Design Engineer

Fixed interoperability problems and design faults. Bug fixing products such as encoders, professional receivers, multiplexers and mobile contribution encoders. Multi-disciplinary role developed software, firmware and hardware skills. Role required strong problem solving abilities.

#### Projects

* **Audio Encoder Card** for Multiplexer: Audio encoding card for multiplexer.
* **AUDITEL**: A requirement of the UK DVB specification that provided a commentary service to visually impaired television users.

#### Training

Mentor Graphics Design Architect Doulos Comprehensive VHDL.

IEE PLL Colloquium TV Technology for Engineers

Introduction to Satellite Transmission MPEG-2/DVB

MCC Configuration Introduction to MCE

# Higher Education

University of Brighton (1993-1998)

Broadcast and Electronic Engineering BEng (hons)

# Education and Qualifications

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| Autumn 2009 | Microelectronic Technologies and Applications (University of Bolton) |
| Summer 2009 | Systems Design Using FPGAs (University of Bolton) |
| February 2003 | Understanding Law (W200) (Open University) |
| Summer 1998 | Elementary Spanish Course (Escuela International de Lenguas) |
| 1993 – 1998 | BEng (hons) Electronic and Broadcast Engineering 2ii  (University of Brighton. Lewes Rd, Brighton) |
| 1991 – 1993 | ‘A’ levels and GCSEs  Fullbrook Sixth Form, Selsdon Road, New Haw, Surrey. |
| 1987 – 1991 | GCSEs  Fullbrook School, Selsdon Road, New Haw, Surrey. |

# Foreign Languages

German: Conversational Spoken. French: Basic. Spanish: Basic