Anita Sharma

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OBJECTIVE

To utilize my acquired skills, abilities and knowledge with a company offering career & knowledge growth with whole aim of

seeing the progress of the company.

TECHINICAL EXPOSURE

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| --- | --- |
| Languages/Technologies | C, C++, Assembly, VHDL, shell scripting ,SQL, FIX protocol |
| Operating Systems / Platform | Linux, Unix, Windows, Tizen . |
| Domain | Embedded, Consumer Electronics (CODEC/Camera), multimedia, Networking, Infotainment ,Investment Banking |
| Development Tools | Enterprise Architect, Visual Studio, Rational Purify, Rational Quantify, Rational RTC, Multi, Vectorcast ,Xilinx, Cygwin , SVN ,GIT, Gerrit , Astah, Perforce, Rhapsody, Squirrel SQL,cmake, CANoe (Automotive) |

WORK DETAILS

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| Nippon Seiki, Redditch ,United Kingdom | Jan 2017-Till Date |
| Cognizant Technology solutions | Oct 2015- 25th Nov 2016 |
| Persistent Systems, Pune | June 2015– Sept 2015 |
| KPIT Technologies, Pune | June 2014 –June 2015 |
| Samsung Research, Noida | Aug 2013- May 2014 |
| HCL Technologies, Noida | Oct 2012- Aug 2013 |
| Society for Applied Microwave Electronics Engineering & Research  (SAMEER), Department of Electronics & Information Technology, Ministry of Communications & Information Technology, Govt. Of India, I.I.T Mumbai Campus, Powai, Mumbai | Embedded Research  Project as mentioned below for MTech Electronics. |
| Watumull Institute of Electronics Engineering and Information Technology, Mumbai | July 2008 –Jan 2009 |
| D.J.Sanghvi College of Engineering, Vile Parle, Mumbai | July 2008 - July 2008 |
| Smt. Indira Gandhi College of Engineering, Koparkhairane | Mar 2008 –June 2008 |
| Radio Electric Institute, Mumbai | Nov 2007- Mar 2008 |
| Maharashtra Academy of Engineering, Pune | July 2005- May 2006 |
| K.C.E.S’ COEIT, Jalgaon | Mar 2003–June 2005 |

PROJECT DETAILS

Company : Nippon Seiki, Redditch ,United Kingdom.

Duration in company : Jan 2017-Till Date

Designation : Software Engineer

PROJECT : Driver Information System (DIS)

Team Size : 26

Platform : Linux, Green hills OS,CANoe

Tools used : Rational RTC, Multi, Vectorcast

Skills used : C, Green Hills OS, Data Structure, Design patterns, Unit testing

Domain : Embedded – Automotive

The project is development and Enhancement of the existing software of a global automotive tier 1 supplier who design and manufacture driver information displays/instrument clusters to some of the leading automotive OEMs across the world.

Driver Information systems are integral unit of a car providing vital information like fuel status, speed etc.

The work involved working according to strict technical standards including MISRA in an AGILE environment.

The roles & responsibilities included the full lifecycle ranging from understanding new customer requirements, design, development & unit testing.

Actual testing on packs was done using CANoe.

Company : Cognizant Technology solutions, Pune, India.

Duration in company : Oct 2015- 25th Nov 2016

Designation : Senior Associate

PROJECT : Investment banking project

Team Size : 26

Platform : Linux, Solaris

Tools used : Tortoise SVN, Squirrel SQL

Skills used : C++, UNIX, Data Structure, Design patterns, SQL, Shell scripting, Databases, FIX protocol

Domain : Investment Banking –Exchange connectivity

The project is in Investment banking domain & provides connectivity between clients & the various exchanges based on FIX and Native protocols like Athex, SAFEX,Milan SDX etc for Equities and Derivative markets.

It also involves critical responsibilities for migration of exchanges from a previous version to a new version in a fast moving AGILE cycle whilst attending to the regular responsibilities of the exchanges meanwhile.

The role & responsibilities include design, coding, unit testing, release to PROD alongside mentoring of the team members.

Have handled successfully many projects in this umbrella project like developing tools for PROD stability to reduce frequently happening issues, continuous monitoring of environment, including an ongoing project of migration to newer platform. Apart from the regular work, I have also owned the responsibility of automating a various frequently needed functionalities which were prone to human error like updating or adding in a critical DB table along with creating a backup automatically.

Have experience of working on multiple exchanges both FIX and non-FIX/Native protocol.

Company : KPIT Technologies, Pune, India.

Duration in company : June 2014 –June 2015

Designation : Senior Technical Leader

PROJECT : Device Projection

Team Size : 5

Platform : Linux

Tools used : Enterprise Architect 11, Redmine, Tortoise SVN, Tortoise GIT

Skills used : C++, UNIX, Data Structure, Design patterns, STL, Scripting

The module deals with device projection which allows screen replication of the projection device onto the infotainment screen through MirrorLink protocol.

The role and responsibilities included technical ownership of the module, architecture & design of the module, mentoring the team members and code reviews as well.

Since the project started from scratch it involved all phases including requirement gathering & analysis, Design and Architecture & POC .

It also involved technical interactions with the client, vendor whose software components were to be integrated in MirrorLink as well as other module Design Leads like Device Manager, HMI etc. to finalize the APIs, dependencies etc.

Enterprise Architect was the tool standardized for Design and Architecture.

Company : Samsung Research, Noida, India

Duration in company : Aug 2013- May 2014

Designation : Lead Engineer II

PROJECT : TV Middleware & Application

Team Size : 14

Platform : Tizen, Linux

Tools used : Visual Studio, GIT, Gerrit, GBS, Virtual Box, Ubuntu, Rhapsody, other client specific

Coding, design, review and testing tools

Domain : DTV-Connectivity

Skills used : C++, UNIX, Data Structure, Design patterns, STL

The project was in TV connectivity Domain (middleware + Application).

The project catered to three main sub-modules –Network, Bluetooth, Wi-Fi & Screen mirroring.

The project scope involved development of features related to above for a target of commercialization.

The responsibilities involved high & low –level design, Development, Unit testing, mentoring team members on technical issues along with close interactions with client.

Company : Samsung Research, Noida ,India

Duration in company : Aug 2013- May 2014

Designation : Lead Engineer II

PROJECT : TV Middleware (Camera/player)

Role & Responsibility : Technical Lead

Team Size : 20

Platform : Tizen, Linux

Tools used : Visual Studio, GIT, Gerrit, GBS, Virtual Box, Ubuntu, Perforce, Rhapsody, other client

Specific coding, design, review and testing tools

Domain : DTV

Skills used : C++, UNIX, Data Structure, Design patterns, STL,GStreamer

The project was in TV/multimedia Domain (middleware) .I was involved in a module related to camera middleware.

The module scope was to capture the picture using DTV camera and save the same in the form of video in DTV .Support for thumbnail was also there. GStreamer was used as the Multimedia framework.

The responsibilities involved high & low –level design, Development, Unit testing, leading team members on technical issues.

Company : Samsung Research, Noida ,India

Duration in company : Aug 2013- May 2014

Designation : Lead Engineer II

PROJECT : DTV Flash player Plug-in development

Role & Responsibility : Technical Lead

Team Size : 07

Platform : Tizen, Linux

Tools used : Visual Studio, GIT, Gerrit, GBS, Virtual Box, Ubuntu, Perforce, Rhapsody, other client

Specific coding, design, review and testing tools

Domain : DTV

Skills used : C++, UNIX, Data Structure, Design patterns, STL

The project was in TV/multimedia Domain (middleware).

The responsibilities range right from setting up a new team , grooming team members to leading team members on technical issues.

Apart from the technical responsibilities, the responsibilities also involved direct communication with the client and also taking care of entire project lifecycle technically.

The Project scope ranged from RA to high & low –level design.

Company : HCL Technologies, Noida ,India

Duration in company : Oct 2012- Aug 2013

Designation : Lead Engineer

PROJECT : AV CODEC

Team Size : 30

Tools used : Visual Studio, Perl, GIT, SVN ,Cygwin & other client specific coding, design, review & testing tools

Domain : Audio Video CODEC/Camera

Skills used : C++, UNIX, Data Structure, Design patterns, STL,Astah

The project was in Camera Domain and I was involved in the middleware development with AV CODEC in AGILE methodology

with TDD .

Apart from the development responsibilities, the responsibilities also involved direct communication with the client and leading development requirements. The module responsibilities include interaction with the business layer and also controlling the hardware layer for achieving the purpose of encoding of file formats. The role &responsibilities include low –level design, Development, Unit testing, leading team members on technical issues.

MTech PROJECT : FPGA based Direct Digital Synthesizer (DDS) for RADAR application

Sponsor : Society for Applied Microwave Electronics & Research (SAMEER), Mumbai, Department

of Information Technology, Ministry of communications and Information Technology, India

Team Size : 1

Tools used : Xilinx (VHDL), MATLAB, C++

Domain : Embedded

Skills used : VHDL

The project was made accommodating the technical requirements and specifications of Radar Division I, Society for Applied Microwave Electronics & Research (SAMEER), Mumbai. While the aim of the project was to develop the FPGA implementation of DDS, it involved a three phase process as

1. FPGA implementation of circuit diagram of the pre-requisite signals required for DDS –Phase I Card for Radar system at SAMEER and ensuing testing (Simulation and hardware).
2. FPGA implementation of the DDS core functionality with IC AD9851 taken as a reference and ensuing testing (Simulation and hardware).
3. Integration of the code of Phase I & II and ensuing testing (Simulation and hardware).

The DDS card - Phase I was an assembly of discrete components. The DDS card works as the heart of the radar for generating the proper timing signal to various sub-units of the radar system. DDS –Phase II had to be made using FPGA with the hardware design language VHDL to develop the FPGA implementation of DDS –Phase I Card for Radar system at SAMEER. This had to be reduced to a single chip whilst generating the same signals required for DDS & also the core functionality of phase to sine amplitude conversion.

CORDIC Algorithm was used for the phase to sine amplitude conversion.

The major achievement was to successfully implement and test the approach for representing numbers and doing calculations using floating point arithmetic, to the level of accuracy required as per the SAMEER standards since by default, floating point numbers are not synthesizable (VHDL).This work led to 3 international papers out of which 2 are IEEE papers.

BE PROJECT : Microcontroller Based On-Off Water Pressure Controller (B.E. EXTC)

Sponsor : Jain irrigation, Jalgaon .Jain group of industries

Team Size : 2

This project was developed as per the requirement of Jain irrigation, to maintain the water pressure within the predefined, safe limits set by the user , using the 8 bit microcontroller AT 89c51 .The controller was designed to get the pressure from the water pressure sensor (P) & check if it is in the predefined limits (PL - PH) .In case P > PH or P<PL a logic high signal is given to 2 distinct port pins to which as a part of future development, devices used to bring this pressure P back within the limit (PL - PH) can be connected . Also, Audible alert & visual message alert were provided in order to make the system user friendly.

EDUCATION QUALIFICATIONS

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| Degree | University/College | Percentage | Duration |
| MTech Electronics | VJTI, Matunga | CPI : 9.4 | 2009 - 2011 |
| BE EXTC | GCOE, Jalgaon, Maharashtra. North Maharashtra University | 69.00% | 1998 -2002 |
| Higher Secondary (HSC) | Mooljee Jaitha College, Jalgaon Maharashtra, Nasik Board | 75.50% | 1997-1998 |
| Senior Secondary (SSC) | New English Medium School, Jalgaon Maharashtra, Nasik Board | 70.00% | 1995-1996 |

SEMINAR & INDUSTRIAL TRAINING

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| --- | --- |
| Seminar | Internet protocol version 6 (IPv6) in BE |
| Industrial Training | Signal & Telecommunication branch, central railway (Bhusawal junction) |
| Industrial Training | Hitech controls limited, Jalgaon Maharashtra |

ACHIEVEMENTS

1. Published a paper in 2011 IEEE International Conference on Information and Education Technology (ICIET 2011), 26-28 January 2011, in Guiyang, China titled ‘Digital Frequency(sinusoidal) Synthesizer using CORDIC algorithm’. ICIET 2011 is an IEEE organized conference.

IEEE Catalog Number: CFP1156M-PRTISBN: 978-1-4244-9586-3

1. Published a paper in 2011 3rd International Conference on Computer modeling and simulation (ICCMS 2011), January 7-9, 2011, Mumbai, India. ICCMS 2011 is sponsored by International Association of Computer Science and Information Technology (IACSIT) and technical co-sponsored by IEEE titled ‘Amplitude quantization effect in FPGA implementation of CORDIC algorithm for Direct Digital Synthesizer (DDS)’.

IEEE Catalog Number: CFP1197F-ART ISBN: 978-1-4244-9243-5

1. Published a paper in International Conference on Computer Applications, 2010, December 24-27, 2010, Pondicherry, India titled ‘CORDIC algorithm for the phase to sine amplitude conversion for digital sinusoidal generators’.

I hope my resume will be as per your requirement and you will give me a chance to prove my capabilities in your organization.

Date: (Anita Sharma)