**ERIC BASILIO** [ericbasilio@yahoo.com](mailto:ericbasilio@yahoo.com) (+44)-7849-055207 Stroud, Gloucestershire GL5 4EH

**WORK HISTORY:**

**X.** 8/2018 – 12/2019: GE Renewable Energy (Stafford) FPGA Firmware Design Engineer for High Voltage DC Valve Based Electronics

Transfer Passive Optic Network (PON) packets via Aurora 8b10b interface from Modular Multi-level Converter (MMC) to Optical Line to Network Terminals (OLT to ONT), to USB Data logger.

Ramped-up verification from scratch with Mentor’s UVM Framework to create and connect environment and multiple agents.

Customised test-harness, configurations, drivers, monitors, predictors, sequences and tests.

Consolidated FPGA build/versions supported from multiple repositories into one.

**IX.** 10/2016 – 4/2018: [Toshiba OCZ](https://www.ocz.com/eu/) (Didcot) **UVM** Verification Engineer for block and chip-level SSD Controller

Extended environment to add/connect register adapter and model.  
Created portable VBA macro to convert existing differently-formatted spreadsheet register definitions to IEEE 1685-2014 **IP-XACT** xml format, up to RAL SV classes.

Bound open-source ARM AMBA interface **ABV** checkers, capturing/debugging protocol violations early in the design phase

System interconnectivity matrix and access restriction verification. Created access traffic from multiple CPU masters to sub-block slaves.

Created base sequences for every team-member to extend. Improved previous block-level base sequences to be reusable “as-is” from block to chip-level.

Used exhaustive UVM built-in test sequences: hard reset and bit-bash

**VIII.** 7/2016 – 10/2016: [AMS AG](http://ams.com/eng/) (Graz Austria) Verification Engineer responsible for class-based constrained randomization and functional coverage in **SystemVerilog** for mobile applications chip used for USB power cable. Redefined configuration space to meet 100% functional coverage

**VII.** 1/2015 – 7/2016: [Alstom Grid](http://www.alstom.com/microsites/grid) (Stafford) Power Electronics Control Systems Firmware Engineer

Reviewed **VHDL/Verilog** RTL against specification for sign-off. Removed meta-stability and race condition issues using DRC. Introduced repository access methodology using externals property. Emulated lab environment by Integrating 4 FPGA RTL designs, some of which having multiple instantiations, for System-level verification. Met timing constraints in SDC. Introduced **SystemVerilog** with class-based constrained randomisation. Shortened overnight simulation to 1hr, making debug process less lab-centric. Created makefile to run tests, merge coverage reports. SerDes 10b8b simulation. Revived obsolete test-bench. SerDes, UART, DAC IF RTLs in **VHDL**. Optimised area, speed and performance of previous design. FreeScale FlexBus Interface.

**VI.** 5/2014 – 12/2014: [Intel](http://www.intel.co.uk/content/www/uk/en/company-overview/company-overview.html) (Swindon) IoT SoC Interconnectivity Design and Verification Engineer

MSI-X application logic verification using **UVM**. Met 99.9% code and functional block coverage. OVM environment reuse. RDL generation of Synopsys DesignWare PCI Express endpoint registers. Created OVC register model (RAL) for Pin Multiplexer, Power Management and PCIe blocks. Test, sequence creation and extension. Created register map. Reused GPIO.

**V.** 10/2007 – 2/2014: [Wolfson Microelectronics](http://www.wolfsonmicro.com) (Newbury) Audio mixed signal IC maker for mobile applications

**FPGA** Design Engineer for Ambient Noise Cancellation Group (2 years **Verilog**)

Verification Engineer for 65nm Audio Hubs Group (4 years **System Verilog**, with 1 year **UVM**)

2013 – 2014: Developed **UVM** environments for ALU, Router, and AHB arbiter blocks. Integrated multiple environment classes in one environment. Connected and built **UVM** scoreboards.

2011 – 2013: Audio Codec chip-level mixed-signal verification which involved:

Verification plan. Time and resource estimation. Test creation from specification, verifying complex functions and features which require integration between digital and analogue top-level blocks, leading to bug detection in both RTL and analogue behavioural blocks.

Parameterisation for portability to future chips, using command arguments and define macros. PWL generation. Power-aware simulation with CPF. Usage of both function/task checkers and assertion-based verification, ABV.

Test and harness creation in **System Verilog**, then converted to classes for **UVM** migration.

2010: Audio interface RTL block design optimisation and parameterisation for IP use. Used synthesizable **Verilog**-generate statements and Ruby text-processing scripts for comprehensibility.

2009 – 2010: **ASIC** verification of ambient noise cancellation as IP block, in co-simulation with MATLAB Simulink HDL Coder. Fill verification holes found in coverage report by constrained input randomisation. Met 99.8% functional coverage. 80% code coverage due to unused saturation logics and excess bits left in the RTL.

2007 – 2009: **ASIC** prototyping of CIC, feed-forward IIR, noise gate and low-frequency soft-limiter algorithms. Made Simulink models configurable.

ADC board evaluation using **FPGA** and Audio Precision audio analyser equipment.

Implemented fixed-point math Simulink models to RTL design, Utilised Xilinx DSP blocks, e.g. FIR, decimator, interpolator, and data-matched with Simulink results.

**ASIC** emulation/prototyping of low-latency ambient noise cancellation technology, working closely with algorithm developers and PCB designer.

**FPGA** implementation via net-list generation of RTL-encrypted memory BIST from Synopsys for increased confidence prior tape-out. Gate-level simulation.

**IV.** 09/2005 – 06/2007: ZDRIVE, Inc. (Laguna, Philippines) Technical Training Consultancy

Role: Digital Design Engineer, training LSI design engineers and managing training centre.

Main training project: NTSC2VGA. Display NTSC camera output to VGA monitor. The module interfaces ITU-R 656 data format from a video decoder to VGA encoder’s RGB data format. The design was implemented in Virtex2-**FPGA** in both **Verilog** and **VHDL**. HDL converts YCbCr to RGB data format. It also converts 720x480 to 640x480 pixel frame size using external ZBT SRAMs. Additional feature displays 800x600 VGA output frame size by applying horizontal and vertical scaling/interpolation. The **FPGA** is in a multi-media evaluation board populated with ZBT SRAMs, video decoder and encoder used in the project. Simulation reads RAW, then DUT output is compared with C-generated RAW image files.

**PROJECT HISTORY : (\***: Project Leader)

Item. Period Member/s Work Detail (HDL: SV = **SystemVerilog**; V=**Verilog**; **VHDL**)

22. 01/2010 – 12/2010 1 Personal project, i.e. solution finder using brute-force array sorting for [Eternity2](http://en.wikipedia.org/wiki/Eternity_II_puzzle) NP-complete puzzle offering $2M reward (SV)

21. 09/2005 – Present: Refer to Work History

20. 01/2005 – 04/2005 4 108 MHz Network Surveillance Memory Controller (V)

19. 08/2004 – 12/2004 3 100 MHz Network Digital Recorder (V)

18. 07/2004 – 08/2004 2**\*** ITU-R 656 digital video I/F (V)

17. 04/2004 – 06/2004 2**\*** Design Engineers' Skill Evaluation Board (**VHDL**/V)

16. 11/2003 – 12/2003 2 125 MHz DIMMnet 2.5Gbps DDR LVDS I/F (**VHDL**)

15. 09/2003 – 11/2003 3 ATM, AAL2, MPFP, and MAC-d WCMDA System Verification (V)

14. 06/2003 – 09/2003 6 MPEG-4 MC/ME Engine system integration, APB and AXI I/F (V)

13. 05/2003 – 06/2003 1 Transmission Equipment (**ASIC** Schematic to Verilog net-list)

12. 02/2003 – 05/2003 1 No. 6's Revision. 108MHz Controlling 2 LCDs at the same time (V)

11. 12/2002 – 02/2003 2 IEEE1394 Interface PCB design

10. 11/2002 – 01/2003 2**\*** 133MHz ZBT-SRAM and SDRAM Controller Evaluation Board (V)

09. 08/2002 – 12/2002 2**\*** 125 MHz Data Encryption Eval Board 1.5 Gbps DDR LVDS I/F (**VHDL**)

08. 06/2002 – 08/2002 3 4-Channel Serial Transmission TDMA for Wireless Comms (**VHDL**)

07. 042002 – 05/2002 2**\*** MPEG2 ITU-R 656 Zoom and Multi-picture Surveillance Features (V)

06. 01 /2001 – 04/2002 3**\*** 80MHz (S)VGA/(S)XGA Controller w/ overlay and CPU-SH3 I/F (V)

05. 09/2001 – 01/2002 5 Frame Rate Converter with I2C, DDS, and EEPROM controllers/IF (V)

04. 04/2001 – 09/2002 2 LSI Testing Equipment (V)

03. 02/2001 – 03/2001 1 UART RS-232 with FIFO (V)

02. 12/2000 – 11/2001 1 Data Rate Converter (**VHDL**)

01. 05/2000 – 11/2000 1 Xilinx Engineer Formal Training (**VHDL**/V)

**SPECIAL SKILLS:**

OS/Environment: Windows, UNIX

Version Control: SVN, Git

HDLs: **SystemVerilog** IEEE 1800 2012, **Verilog** IEEE 1364-2001, **VHDL** IEEE 1076-2008

Verification Methodologies: **UVM 1.1d** as environment developer and test writer, OVM

**FPGAs**: Xilinx ISE, Altera MAX, Quartus II, Aldec/Microsemi Libero

Synthesis: Synplify Pro, Synopsys DC, **FPGA**-Express, XST, Leonardo Spectrum

DRC/lint: ALINT using STARC policy

Digital Simulation: ModelSim, Questa Prime, VCS, IES

Project/Issue/Bug Tracking: Jira

Interface/Bus: I2C, I2S, SPI, APB, AHB(Lite), AXI3, AXI4, AXI4 stream

Text processing: Ruby, Perl, Visual Basic for Applications

Command Scripting: make, tcl, csh

Analogue IC Net-list: Virtuoso

PCB: OrCAD Capture, Circuit Maker Pro (Spice), WinSpice

C Compiler: GCC, Kiel uVision Debugger

Microcontroller: 8061

Lab Equipment: ChipScope Pro, SignalTap, Audio Precision audio analyser, oscilloscopes, logic analysers, spectrum/network analysers, Edirol sound card

Register definition: IP-XACT XML, Synopsys RALF, SystemRDL

Preferred Text Editors: DVT Eclipse, Notepad++

**EDUCATION:** BS Electronics and Communications at [University of Santo Tomas](http://www.ust.edu.ph/academics/overview/faculties-and-colleges/faculty-of-engineering/), Philippines

**OTHERS:** UK Citizen, BPSS clearance, 日本語可