**IAN BANBROOK**

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An experienced, hands on design engineer leading a team working at the leading edge of data communications. Highly skilled designer with a long track record of embedded circuit, PCB, FPGA, mechanical and firmware product development. Working with the full product lifecycle from the initial customer concept, requirement generation, design, test, approvals, new product introduction and technical support. Experienced in working and delivering to tight deadlines while multi tasking over many projects.

**KEY SKILLS**

* Schematic Capture ( Orcad )
* PCB layout (Impedance Control, Trace Matching, DFM/DFT )
* FPGA Design ( Xilinx ISE/Vivado VHDL, Spartan 3/6, Kintex, Zync, IP modules, Testbench)
* Embedded System Design ( PowerQUICC, PIC, AVR, 68k, i960 )
* Hardware test and debug ( ISE/Vivado Chipscope )
* Component Obsolescence
* Firmware (Assembler/C)
* Project Management
* EMC / Safety / Environmental Approvals
* Documentation – Requirements / Test Specifications / User Manuals
* Version Control
* Pre/Post Sales support
* Team Leading
* Consultancy

**CAREER**

**Metrodata Ltd 1995 - Date**

**Engineering Manager**

Metrodata is a small UK manufacturer of data communications equipment. As Engineering Manager I lead the design team in the development of a range of products to very tight timescales and with limited budget. I also work closely with the directors in setting the technological direction, strategy and product roadmap for the company.

I designed and delivered a range of Carrier Ethernet Products for both 1G and 10G Ethernet service delivery which were MEF CE2.0 compliant. This involved leading the projects from initial customer concept, generating functional specifications from which the software team developed the application code through schematic/FPGA and PCB design, hardware and system testing and initial customer trials.

Xilinx FPGA design used both ISE for Spartan-6, and Vivado for Kintex-7 with all design in VHDL making use of system IP blocks such as Memory Controller for DDR3, QDR-2+ and XAUI. All VHDL modules were individually verified using test benches. The PCB layout required tight impedance control for 10G signalling and was designed using ORCAD. The FPGA included high performance, low latency wire speed data path packet processing for 10Gbps operation. After consideration and evaluation of the various vendor chipsets, Marvell Switch and Phy devices were selected for use in these products.

I designed and delivered a range of Ethernet Access Devices, both managed and unmanaged to enable the transport of Ethernet over a range of interfaces, E1/E2/E3/STM-1, HSSI, LVDS, Serial X.21/EIA-530/V.35. These access devices were designed as both standalone units and as modules for the MC12000 rack system. FPGA design used Xilinx ISE VHDL and targeted Spartan 3, and Spartan 6 devices.

Metrodata also offers consultancy and OEM product development. I am currently designing a serial controller for an aircraft telemetry channel transceiver with a US company. This will be provided as an IP module for use within their Xilinx Zync-7 node controller module. I have also designed a delivered a comms controller for special forces for backhaul of Ethernet and Serial EIA-530 over Fibre and provided Red/Black side interface conversion for latest generation high speed Military Encryption devices for the Dutch Army.

I was also lead product architect and designer for the development of the APX product family of ATM access devices which provided all the standard ATM interface support, however through development of proprietary interfaces we secured a market in Satellite backhaul way beyond the end of the general ATM market opportunity.

**Cray Communications** 1987 - 1995

(Formerly Case Communications/ Dowty Communications )

I joined Case as a graduate engineer and initially worked on designs using Xilinx X2000 series using Future Net schematic capture for use in the X.25 product range. I progressed to Principal Engineer and was project manager for the DCX SM2 development with a team of 10 engineers, where my main responsibility was hardware design including the schematics, documentation and system testing.

**QUALIFICATIONS**

1984-1987 Electrical and Electronic Engineering 1st class BSc (Hons)

University of Nottingham