*Andrew Hudson*

**Consultant FPGA Engineer, Ephemeral Logic, Ltd.**

*A multi-skilled FPGA, electronic and software engineer, specialised in imaging systems development, equally at home in highly agile commercial development or structured defence/aerospace environments. Able to develop complete products and subsystems or to troubleshoot complex cross-discipline problems under pressure.* ***Current Security Clearance.***

**Skills**

**FPGA Development**. Areas of expertise:

* **Xilinx**, **Zynq**, **Virtex**, **Kintex**, **Spartan**, **7-series**, **Vivado**, **ISE**, **SDK**, **System Generator**;
* **System-on-Chip** (SoC); **Zynq**, **Microblaze**, custom bespoke processors;
* **Multi-Gigabit Transceivers** (**SerDes**): the enabling technology behind **PCI-Express**, **XAUI** (**10Gb Ethernet**), **SATA**, **Infiniband** & **Fiberchannel**;
* **High speed memory** **DDR2**, **3**, **4**; NAND/NOR **Flash**;
* **Image Compression**: **JPEG**, **JPEG-LS**, **JPEG2000**, **HVC/H264**;
* **Ethernet** & IP routing and **encryption** **IPSec**, **DES**, **AES**; **TCP**, **UDP**;
* **Software Defined Radio**;
* **VHDL** & schematic capture;
* **DSP**: Video, Audio, Communications;
* **Motor control**: brushless DC, commutation, speed/current control, control loops;
* **Microsemi**/**Actel**: **Smartfusion**, **ProASIC**, **RTAX**, **Libero**;
* **Simulation**/**verification**: **Modelsim**, **TCL**, **Matlab**;
* **Safety critical applications**: defence, space, aviation;
* **Radiation environments:** SEU mitigation, SEL protection;
* Peripheral control: AXI, I2C, I2S, SPI, UART etc.

Example Developments:

* **real-time image compression** for space-borne earth observation and defence applications, Xilinx Virtex/Kintex:
  + **JPEG-LS**, a multi-channel 4Gb/s adaptive predictor;
  + **JPEG**, a custom 2-D Discrete Cosine Transform Engine 2Gb/s;
  + **JPEG2000** low-latency video solution using 3rd party core;
* **software-defined radio**, digital down-converting receiver, geolocating L-band sources, Xilinx Virtex;
* **sample-rate conversion,** multi-rate, multi-channel, for ultra-high precision audio, Xilinx Spartan;
* **IPsec routing** for satellite-groundstation communications including **AES & DES** encryption/decryption 400Mb/s, Xilinx Virtex;
* **brushless DC motor control** for spacecraft reaction wheels, Microsemi RTAX;
* **custom soft-core microprocessor**, optimised for client’s proprietary buses.

**Embedded Software development**

Complete lifecycle; C/C++, assembler; multi-context real-time event/interrupt driven systems; task-scheduling; memory management (MMUs, DMA, paging, cache configuration etc.); hardware abstraction layers; device drivers; board support packages; user interfaces; peripheral control e.g. CAN, UART, SPI, I2C, ADC/DAC etc.; PowerPC, PIC, Zynq/ARM, Freescale 56k, SHARC, 68HC11, 8051 and derivatives, Z80, custom soft processors.

**Board design** - **high-speed digital, analogue** and **mixed signal** with DACs/ADCs, analogue front-end design, high performance imaging and audio, design for EMC and signal integrity. Flexi-rigid, multi-layer PCB layout and design. Analogue simulation with p-Spice. Familiar with manufacturing for mass production and prototyping. Thermal/mechanical design. Design and component selection for high-radiation environments. CADStar, ORCAD, Mentor Graphics.

# Previous Contracts

**FPGA Consultancy for a global Defence Contractor** 03/14-present.

* Independent verification of a pair of safety critical FPGAs; developed multi-scenario test-benches in VHDL run on Modelsim controlled by TCL script and test-vectors to verify against derived requirements. Achieved an order of magnitude simplification over the baseline while delivering a more comprehensive and credible result. Elucidated and re-stated the requirements, introducing a new style of requirement setting to the client which they adopted as their new standard, since used on many other developments;
* developed a JPEG2000 video compression system to use optionally a 3rd party compression core or an off-the-shelf ASIC; logic implemented in Xilinx Virtex-5 and Kintex-7 using multiple DDR2/3 interfaces; resource efficiency enabled re-use of existing hardware conferring significant cost and schedule saving over expected new board development;
* developed a custom FPGA-based soft-core microprocessor, optimised for client’s proprietary bus.
* developed a series of radar DSP subsystems for complex guided weapons, including requirements capture, algorithm development and implementation/optimisation, Xilinx 7-series SoC.

# Training

**Xilinx - Designing with Multi-Gigabit Serial IO**, Core|Vision (07/15)

**Xilinx - Embedded Systems Hardware and Software Design**, Zynq, Vivado and SDK, Doulos (08/14)

**DSP for FPGAs**, by Steepest Ascent; comprehensive DSP course, Xilinx System Generator (2012).

**Expert VHDL, Design & Verification,** by Doulos (2010).

**VHDL for FPGAs/ASICS**, Doulos (10/97).

## EMC and High-Speed Board Design, a comprehensive three-day course on design techniques to minimise EMC and signal integrity problems (03/07).

**PowerPC microprocessor**, comprehensive course on all HW/SW aspects of PowerPC processors, (5/98).

# Employment History

**Principal Engineer, On-board Data Handling** for **Surrey Satellite Technology Ltd**. 31/01/05 – 01/01/14.

A responsive, world leading spacecraft manufacturer specialising in the use of commercial-off-the-shelf electronic components for space applications; using agile techniques for industry-leading development speed.

Performed clean-sheet subsystem development and provided internal troubleshooting consultancy:

* Developed a new class of performance-critical electronic imaging systems for earth observation satellites, involving requirements capture, system design, FPGA and software development, board design (analogue front-end, mixed signal and high-speed digital), testing, calibration, integration;
* numerous FPGA, embedded software, analogue and digital hardware solutions for satellite and groundstation data-handling applications.

**Design Engineer** for **Prism Sound**. Cambridge. 30/11/98 – 15/11/04.

A small Pro-Audio engineering company developing very sophisticated products for the top end of the recording and test/measurement market. Typically employing engineers on a one-person-per-product basis in an agile development culture.

Primarily responsible for the Prism Sound, Dream ADA-8: the world-leading, multi-channel AD/DA converter and audio processor with modular I/O and processing. Complete product life-cycle experience:

* hardware design (10 boards, high-speed digital logic, mixed signal design, ultra-low noise/distortion analogue design, phase-locked loops, power system design;
* FPGA design (signal processing and glue logic), simulation;
* embedded software on micro-controller and DSPs in assembler and high-level;
* DSP (in FPGAs and DSPs), algorithm development and modelling.

**Digital Design Engineer** for GEC Marconi Radar and Defence Systems, Dynamics Division, Stanmore. 10/97 – 11/98. Designed and integrated PowerPC computing engines for the Brimstone missile project. High-speed digital design, FPGA development and hardware/software integration.

# Qualifications

**BEng (Hons.) in Electrical and Electronic Engineering** (1997)

**Imperial College of Science, Technology and Medicine**