AMACv2 Functional Verification Test Plan

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Abstract

This document enumerates features to be tested, and defines test procedures for single-chip verification of AMACv2. This document will be augmented to act as a test record. System-level and production test procedures are outside the scope of this document.

Revision History

Revision	Date	Author(s)	Description
0.0	19 July 2018	P: A.N.	Initial outline
0.1	23 July 2018	P: V.R.	Update AM Channel Tests

Contents

1 Related Documents

The main SVN repository for code and documentation is located at: https://svnweb.cern.ch/cern/wsvn/itkstrasic/AMACv2/. Please refer to doc/README.txt for the latest version of the specification, as well as schematics, register map, Verilog, and verification code for the November 2017 MPW ASIC.

2 AMACv2 Feature Test List

2.1 Current Consumption

Measure before configuration, and after various configurations. Gather statistics from several single-chip test cards.

2.2 Digital Pins

2.2.1 ROPG (ring oscillator power good)

Output. Confirm pin goes logic high approximately 250µs after power is applied.

2.2.2 LAM ("look-at-me")

Output. Confirm that LAM pulse is generated upon interlock if enabled in registers 60-25, bit 16. Confirm multiple LAM pulses are generated upon successive interlocks that are not cleared.

2.2.3 LDx0en, LDy0en, LDx1en, LDy1en, LDx2en, LDy2en

Outputs. Confirm pins go logic high when corresponding bits in registers 40/41 are written. Confirm pins go logic low after enabled if corresponding interlock occurs.

2.2.4 ResetB

Input. Confirm that logic low pulse resets AMACv2 to default condition (all registers to default values, additional SETID required).

2.2.5 SSSHx, SSSHy

Inputs. Confirm that logic high pulse resets Endeavour communications block (register states persist, additional SETID required). Validate deglitching.

2.2.6 HrstBx, HrstBy

Outputs. Confirm pins go logic high when corresponding bits in registers 46/47 are written.

2.2.7 DCDCen

Output. Confirm pin goes logic high when registers 42/43, bit 0 are written.

2.2.8 DCDCadj / GPO

Outputs. Confirm pins go logic high when corresponding bits in register 42/43 are written.

2.2.9 ID[4:0]

Inputs. Confirm bits can read in serial number register 31.

2.2.10 OFin

Input. Confirm that DCDCen is disables when OFin is asserted. Validate deglitching.

2.2.11 OFout

Output. Confirm pin is goes high when registers 46/47, bit 0 are written.

2.2.12 GPI

Input. Confirm pin state can be read in status register 0, bit 12.

2.2.13 PGOOD

Input. Confirm pin state can be read in status register 0, bit 8. Confirm DCDCen cannot be enabled when PGOOD is logic high, if and only if this functionality is enabled by setting registers 50/51, bit 8.

2.3 Analog Pins

2.3.1 ClkOut

Output. Confirm 40MHz nominally.

135 #### 2.3.2 AMBG600

136 #### 2.3.3 AMBG900

137 #### 2.3.4 VDDREG1/2

138 #### 2.3.5 Shuntx, Shunty

139 #### 2.3.6 CALx, CALy

140 #### 2.3.7 NTCxp/n, NTCyp/n, NTCpbp/n

141 #### 2.3.8 Hrefx, Hrefy

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144 #### 2.3.11 Cur1Vp/n

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146 #### 2.3.13 HVret1/2

147 #### 2.3.14 HVref1/2

148 #### 2.3.15 CAL

149 ### 2.4 HVOsc0/1/2/3

150 Output.

151 - Measure HV oscillator drive capability (charge pump to voltage attained)
152 - Measure 4 frequency settings
153 - Confirm enable/disable

154 ### 2.5 Power Pins

155 #### 2.5.1 VDDLR1/2

156 Confirm operational ranges. Confirm PoR threshold.

157 #### 2.5.2 VDCDC1/2

158 Switch AMAC power from linear regulator to DCDC converter power.

2.5.3 VDDHI

2.6 Communications Pins

2.6.1 CMDinP/N

Input. Measure voltage at receive side.

2.6.2 CMDoutP/N

Output.

- Measure current drive
- Measure common mode of driver
- Confirm high impedance when not transmitting (475ns window for switch-on)

2.7 AM Channel Tests

Note: Calibration of Analog Monitor [1] must be done before proceding with the below tests

2.7.1 DCDC converter output (scaled)

Read the DCDC converter output voltage on Channel 0 (See Table 2). The output is scaled by $\frac{1}{2}$. The output voltage can also be measured on VDCDC1 and VDCDC2 pins.

Pad Name	Channel	Sub-channel	MUX select	Value
VDCDC	0	–	–	∼750 mV

Table 2: DCDC converter output

2.7.2 Linear regulator output (scaled)

Read the linear regulator output voltage on Channel 1 (See Table 3). The output is scaled by $\frac{1}{2}$. The output voltage can also be measured on VDDLR1 and VDDLR2 pins.

Pad Name	Channel	Sub-channel	MUX select	Value
VDDLR	1	–	–	∼700 mV

Table 3: Linear regulator output

2.7.3 DCDC converter input (scaled)

Measure the input voltage to the DC/DC converter on Channel 2 (See Table 4). It is scaled by $\frac{1}{15}$.

Pad Name	Channel	Sub-channel	MUX select	Value
DCDCin	2	–	–	~830 mV

Table 4: DCDC converter input

2.7.4 Regulated VDD (scaled)

Modify Bangap reference voltage (See [2]) and measure the corresponding regulated VDD voltage. The regulated VDD is scaled by $\frac{2}{3}$. Table 5 summarizes the output details.

Pad Name	Channel	Sub-channel	MUX select	Value
VDDREG	3	a	Reg53$< 5:4 >$	~800 mV

Table 5: Regulated VDD ouput

The regulated VDD voltage can also be measured on VDD1 and VDD2 pins.

2.7.5 AMBG600/AMBG900

- Read AMBG600 (See Table 6). It should be ~600 mV.
- If not, tune the bangap reference output voltage using the 5 bit AM BG switches provided in Register 52 (BgCnt).
- After tuning AMBG600 to 600 mV, Read AMBG900.

Pad Name	Channel	Sub-channel	MUX select	Value
AM600BG	4	a	Reg53$< 9:8 >$	~600 mV
AM900BG	3	c	Reg53$< 5:4 >$	~900 mV

Table 6: 600 mV and 900 mV AM Bandgap ouput

2.7.6 CAL from EoS

Read End of Stave ground reference voltage (See Table 7).

2.7.7 CALx/y from DAC

Calx/y DAC outputs are available on Channel 5a,b. (See Table 8)

- Choose CALx output on Channel 5.
- Set the 5-bit DACbias on Register $55 < 4:0 >$ as 1111. This is the highest bias current condition for the DAC.
- To test the mid range output value of this DAC, Set the 8 bit DAC input value for CALx on Register $54 < 7:0 >$ to 8h7F.
- Read the output. Output voltage should be ~450 mV.
- Set the 8 bit DAC input value for CALx on Register $54 < 7:0 >$ as 8h00.
- Read the output. Output voltage should be ~zero.
- Set the 8 bit DAC input value for CALx on Register $54 < 7:0 >$ as 8hFF.

Pad Name	Channel	Sub-channel	MUX select	Range
CAL	4	b	Reg53< 9 : 8 >	∼0 to 1 V

Table 7: EoS reference voltage

Pad	Channel	Sub-Channel	MUX select	Description
CALx	5	a	Reg53< 14 : 12 >	Output of Hybrid X Calibration DAC
CALy	5	b	Reg53< 14 : 12 >	Output of Hybrid Y Calibration DAC

Table 8: Calx/y DAC output

- Read the output. Output voltage should be ∼800 mV.
- Test the DAC for different bias setting and input values.
- Repeat the above procedure to test CALy DAC.

The output of this PMOS DAC is expected to deviate from linear near VDD. See [3] page 40 for schematic.

2.7.8 Shuntx/y from DAC

Shuntx/y DAC outputs are available on Channel 5c,d. (See Table 9)

Pad	Channel	Sub-Channel	MUX select	Description
Shuntx	5	c	Reg53< 14 : 12 >	Output of Hybrid X Shunt DAC
Shunty	5	d	Reg53< 14 : 12 >	Output of Hybrid Y Shunt DAC

Table 9: Shuntx/y DAC output

- Choose Shuntx DAC output on Channel 5.
- Set the 5-bit DACbias on Register 55 < 4 : 0 > as 1111. This is the highest bias current condition for the DAC.
- To test the mid range output value of this DAC, Set the 8 bit DAC input value for Shuntx on Register 54 < 23 : 16 > to 8h7F.
- Read the output. Output voltage should be ∼700 mV.
- Set the 8 bit DAC input value for Shuntx on Register 54 < 23 : 16 > as 8h00.
- Read the output. Output voltage should be ∼1.17 V.
- Set the 8 bit DAC input value for Shuntx on Register 54 < 23 : 16 > as 8hFF.
- Read the output. Output voltage should be ∼80 mV.
- Test the DAC for different bias setting and input values.
- Repeat the above procedure to test Shunty DAC.

The output of this NMOS DAC is expected to deviate from linear near zero. See [3] page 40 for schematic.

2.7.9 NTCx/y/pb

NTC Outputs are available on Channel 7,8 and 9 for NTCx, NTCy, NTCpb. See Table 10.

Pad	Channel	Sub-Channel	MUX select	Description
NTCxp,n	7	–	–	Hybrid X NTC Temperature
NTCxp,n	8	–	–	Hybrid Y NTC Temperature
NTCpdp,n	9	–	–	Power board NTC Temperature

Table 10: NTC output

The 3-bit range select for NTC is mapped to register 57 (See Table 11).

NTC name	Register	Bits
Hybrid X	57	2:0
Hybrid Y	57	10:8
Power board	57	18:16

Table 11: NTC range selection

- Calibrate NTCx sensor. See [1].
- Set NTCx range select bits to 3b110.
- Place a 10 K Ohm resistance (equivalent to the NTC resistance at room temperature) between NTCxp and NTCxn pads.
- Read the NTC sensor output, the output should be ∼600 mV.
- Vary the potentiometer resistance and the NTC range switches to test the circuit for differnt temperatures.
- Repeat the steps for NTCy and NTCpb.

2.7.10 Hrefx/y from hybrids

- Apply voltage to Hrefx and Hrefy pins.
- Read the Hrefx and Hrefy voltages (See Table 12). The expected test range is −15 mV to 1 V.

Pad	Channel	Sub-Channel	MUX select	Description
Hrefx	10	–	–	Hybrid X local ground
Hrefy	11	–	–	Hybrid Y local ground

Table 12: Hybrid X/Y local ground value

2.7.11 DCDC input current

Outputs idcdcCMOut, idcdcVlowTP and idcdcVhighTP are multiplexed on Channel 12 (See Table 13).

- Calibrate the 12 V current measurement block. See [1].
- Vary the current through Rsense series resistor from 0 to 1A, the DCDC current monitor output voltage should vary linearly fromm ∼100 mV to 1V.

Output	Channel	Sub-Channel	MUX select	Description
idcdcCMOut	12	a	53< 18 : 17 >	Input DC DC converter output
idcdcVlowTP	12	b	53< 18 : 17 >	Calibration test point low
idcdcVhighTP	12	c	53< 18 : 17 >	Calibration test point high

Table 13: 12 V DCDC input current measurement block outputs.

2.7.12 DCDC output current

Outputs odcdcCMOut, odcdcVlowTP and odcdcVhighTP are multiplexed on Channel 13 (See Table 14).

Output	Channel	Sub-Channel	MUX select	Description
odcdcCMOut	13	a	53< 21 : 20 >	Output DC DC converter output
odcdcVlowTP	13	b	53< 21 : 20 >	Calibration test point low
odcdcVhighTP	13	c	53< 21 : 20 >	Calibration test point high

Table 14: 1.5 V DCDC output current measurement block outputs.

- Calibrate the 1.5 V current measurement block. See [1].
- Vary the current through RSense series resistor from 0 to 4A, the DCDC current monitor output voltage should vary linearly from ∼100 mV to 900 mV.

2.7.13 HV current return monitor

The HV current monitor is available on Channel 14 (See Table 15) and its operating range is selected through 4 bits in Register 56< 19 : 16 > (See Table 16).

Output	Channel	Sub-Channel	MUX select	Description
HVret	14	–	–	Sensor HV bias return current measurent

Table 15: HV current monitor block

- The operation range of the HV current monitor can be selected through register
- Select HVret1.
- Vary the input HVret1 current from 0.01 mA - 5 mA and measure the output voltage.
- Repeat the procedure for HVret2.

2.7.14 die temp (PTAT)

- Voltage output prortional to the AMAC die temperature is provided on Channel 14.
- Vary the temperature between −40 to +50℃and measure the output.
- The output ranges from ∼375 mV to 250 mV. See [4]

Sl no.	**Reg53**$< 19:16 >$	**Current range**
1	4b0000	200 nA − 4.5 μA
2	4b0001	270 nA − 50 μA
3	4b0010	40 μA − 474 μA
4	4b0100	100 μA − 1 mA
5	4b1000	250 μA − 5.7 mA
6	4b1100	250 μA − 7.6 mA

Table 16: HV current monitor range selection

2.7.15 MUX functionality

Channels 3,4,5,12 and 13 are multiplexed. The MUX select bits are mapped to register 53 as shown in Table 17).

Channel no.	**Register**	**MUX Select**
3	53	bits $< 5:4 >$
4	53	bits $< 9:8 >$
5	53	bits $< 14:12 >$
12	53	bits $< 17:16 >$
13	53	bits $< 21:20 >$

Table 17: MUX selection

2.8 AM functionality

2.8.1 Enable/disable

2.8.2 Default value

2.8.3 Overflow value

2.8.4 Full 10-bit range 0-1023

2.8.5 Values below zero

2.8.6 Analog noise injection / flag limit tolerance, dither, ramp latch time

2.9 Digital Functions

2.9.1 Resets

- Commanded hard reset
- Commanded soft reset

2.9.2 WARN

2.9.3 Flags

- Flag limit setting
- Synthetic flags
- Flag latch
- Flag clear
- Flag validation: 2,3,4 ramp cycles
- Edge cases: value below zero, comparator never fires
- Confirm all flags mapped to corresponding limit registers

2.9.4 Interlock

- Enable/disable/clear
- Confirm all states of state machine are exercised
- Confirm all interlocks are mapped to corresponding channels, high and low limit
- More than one LDO interlock programmed
- Synthetc flag interlocks

2.10 Endeavour

- Invalid commands: headers, COMMID, packet size, bitwidth, EoS frequency tolerance
- Pseudorandom data
- Check sequence numbers
- Check CRC validation
- Violate SETID quiescent time
- Send command while busy
- PADID and eFuse matching, wildcard IDs
- Effect of hard/soft/SSSH reset
- R/W all registers
- READNEXT

2.11 Parametric Tests

2.12 Irradiation Tests

Test system infrastructure functionality to be confirmed (long cable tests for TID tests, test board temperature monitoring and control, etc.).

3 AMACv2 Test Plan

3.1 Power-up

This power-up sequence in not intended to be the default use case. Single-chip bringup only.

- Apply VDDLR
- Measure AMACv2 current before configuration
- Measure AMACv2 VDDREG, AMBG600, AMBG900. Gather statistics on multiple MPW chips.
- Measure ROPG pin
- Measure RO frequency on RO pin
- Send SETID
- Read PADID from serial number register 31
- PGODD pin: read status register 0
- Calibrate RO, AMBG600/AMBG900/VDDREG, AM bandgap, record calibration values (histograms)
- Read a AM register and see the default value
- Calibrate AM: zero cal, ramp slope, BG fine tune
- Measure current after config
- Put voltage on CAL and read back
- Test other channels
- DAC calibration, compare with AM measurement

3.2 Digital Functional Tests

All detailed procedures for test items above to be specified here.

3.3 Analog Functional Tests

TBD: CAL, Hrefx/y: input offset variation as a function of voltage, linearity

3.4 Radiation Tolerance

3.4.1 TID

3.4.2 SEU

4 AMACv2 Test Record

Results of above tests to be recorded here.

References

[1] AMACv2 Calibration Procedure

[2] Simulation of Bangap & Regulator Circuit

[3] AMACv2 Schematics

[4] Testing of Diode based Temperature Sensor