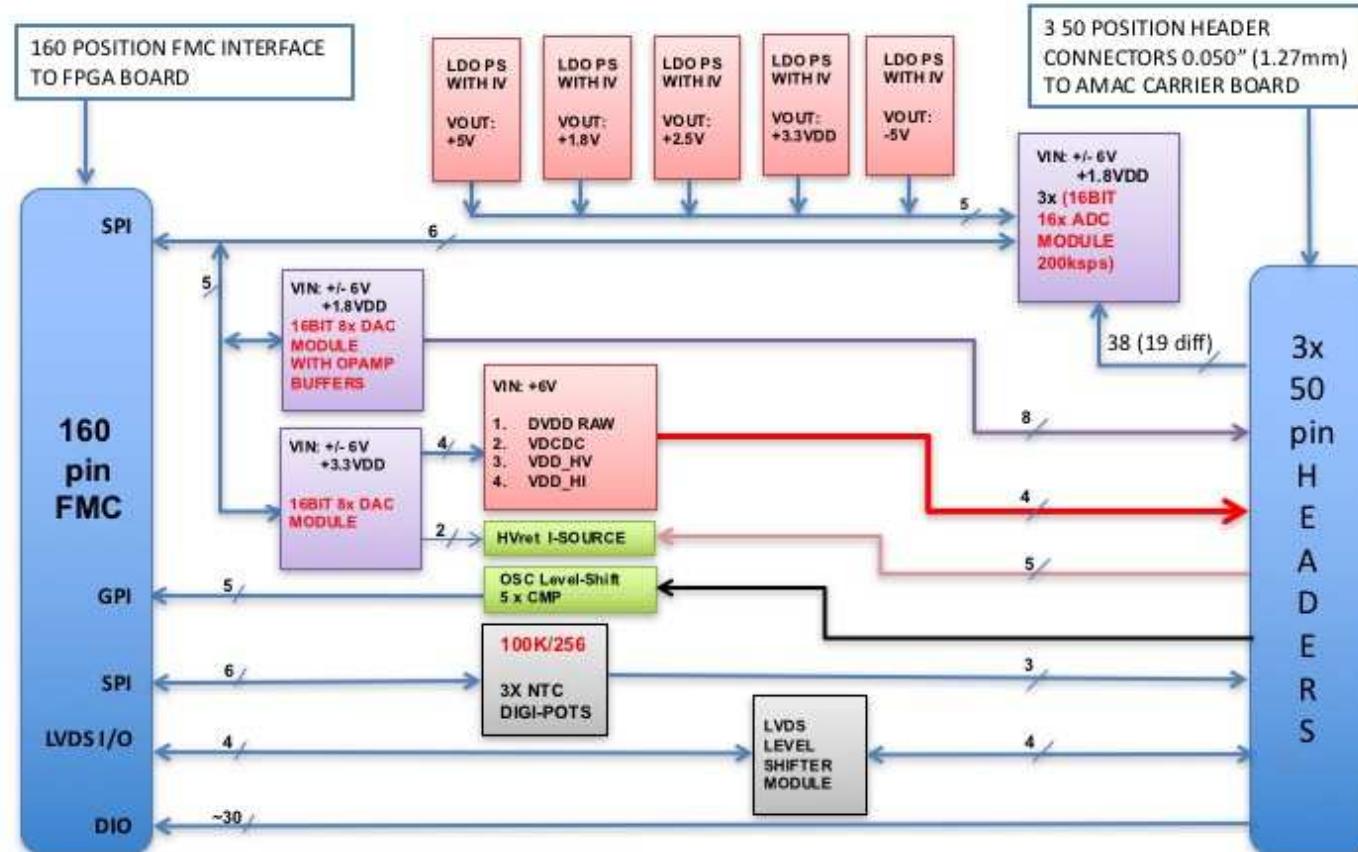
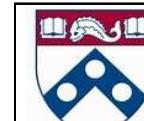


AMAC V2 TEST & CONTROL BLOCK DIAGRAM



3/12/18

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ATCB Block Diagrams

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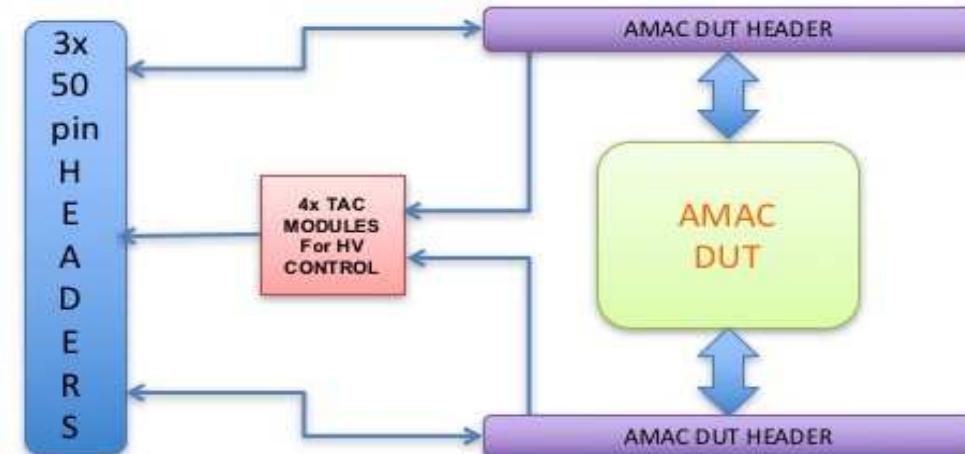
Date: Wednesday, April 04, 2018

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Designer: G.Mayers

AMAC CARRIER AND DUT BOARDS

D
3 50 POSITION HEADER
CONNECTOR 0.050(1.27mm)
TO AMAC TEST & CONTROL
BOARD



3/12/18

Godwin Mayers

2



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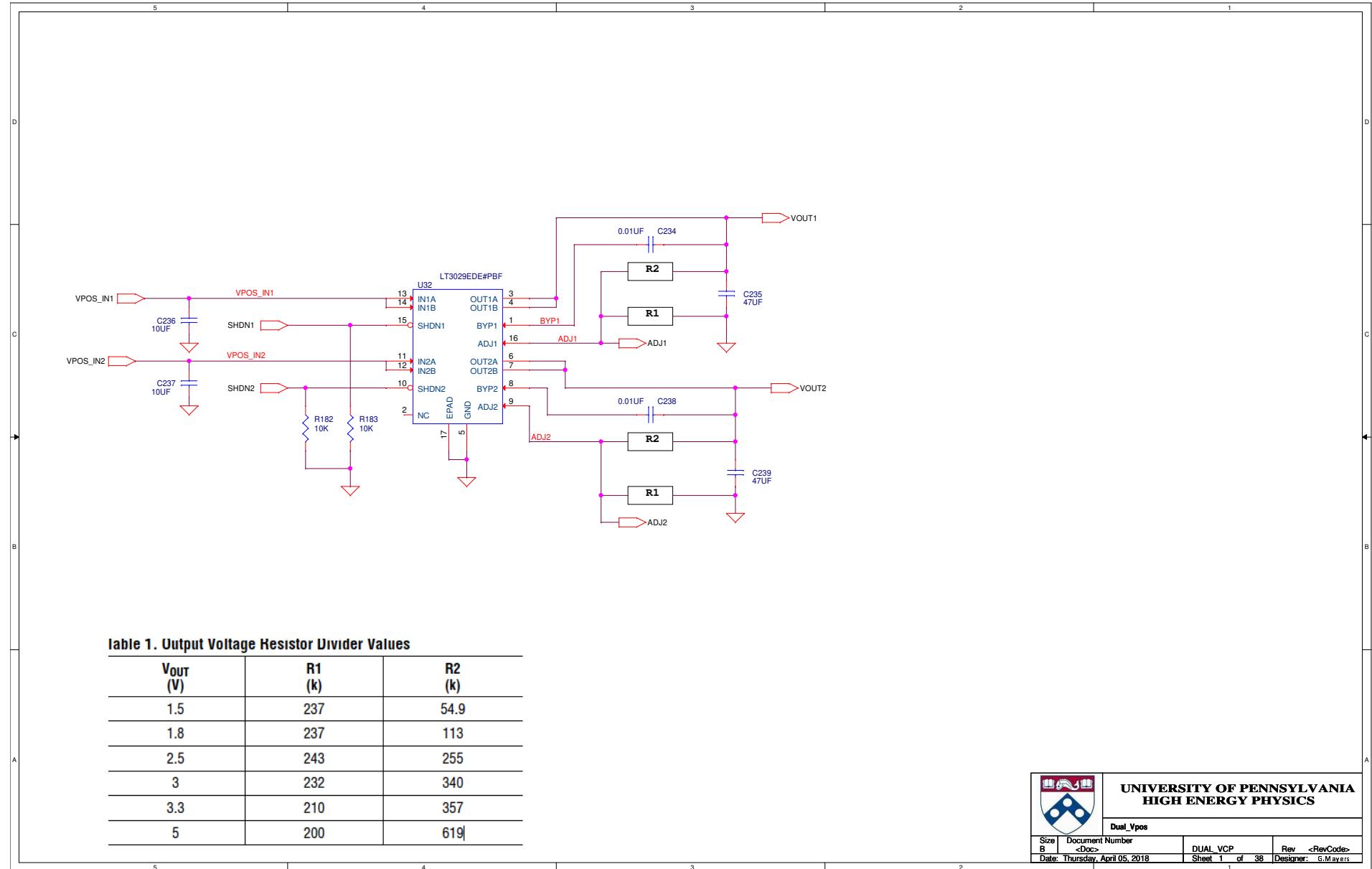
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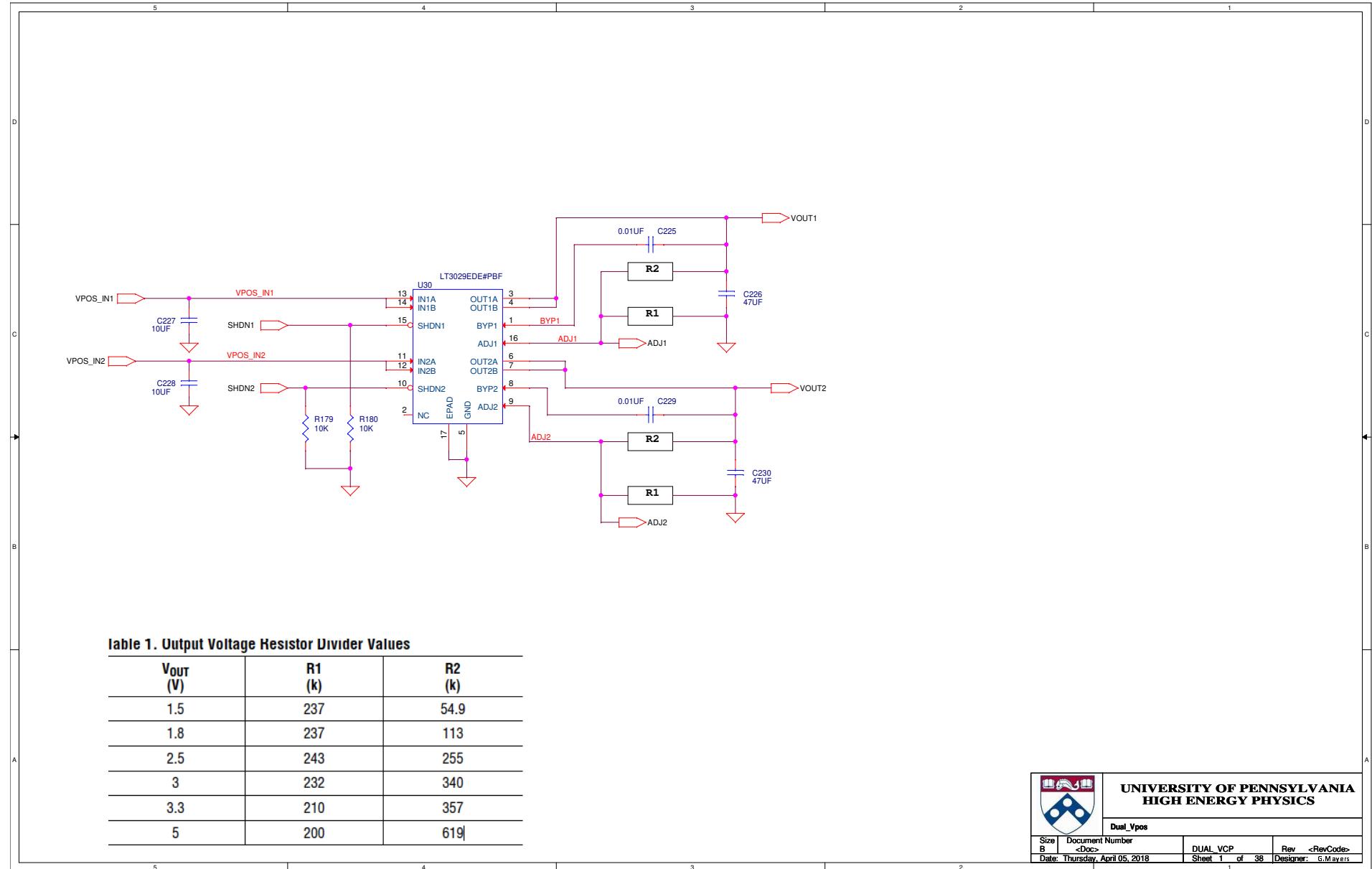
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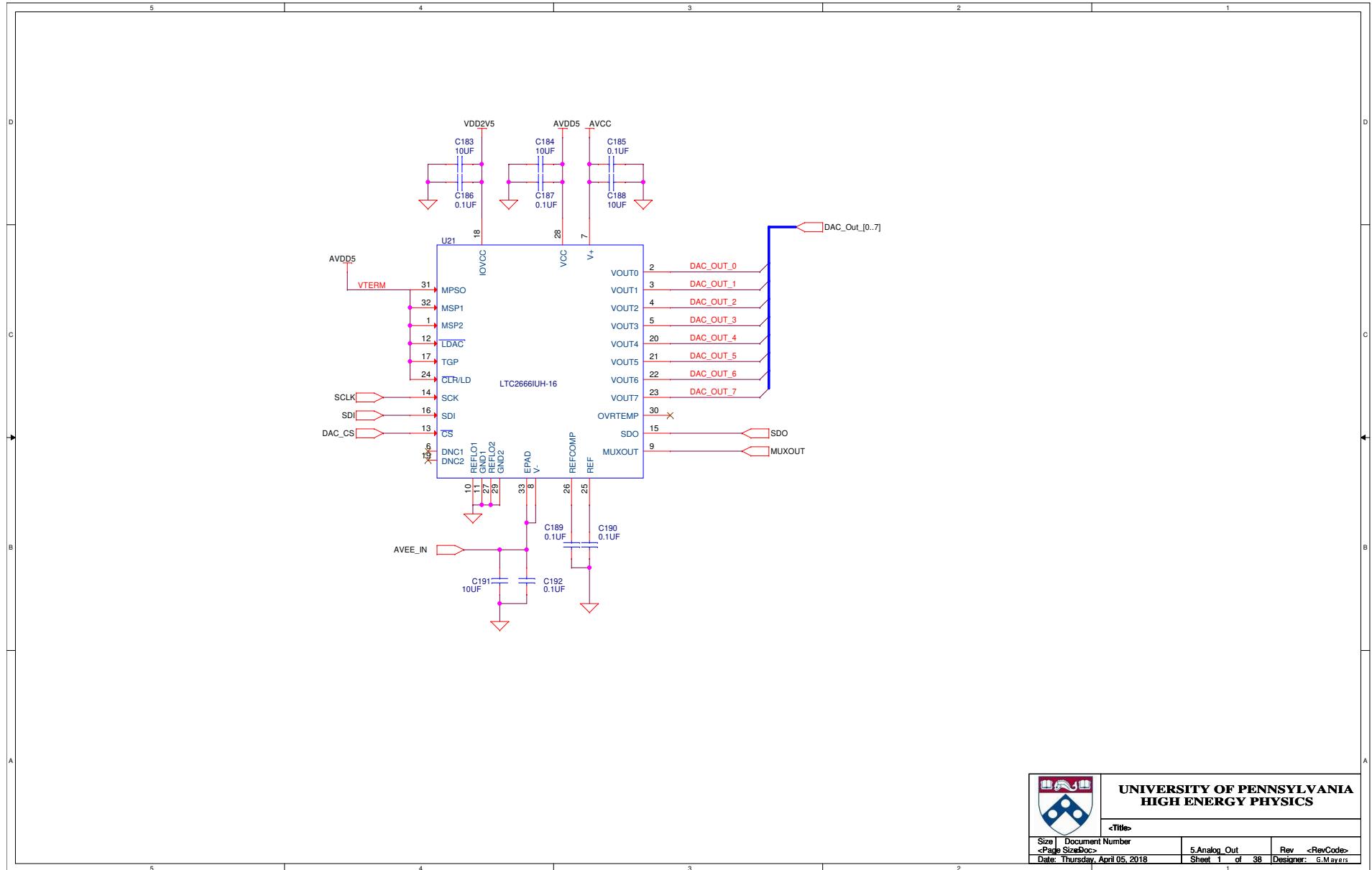
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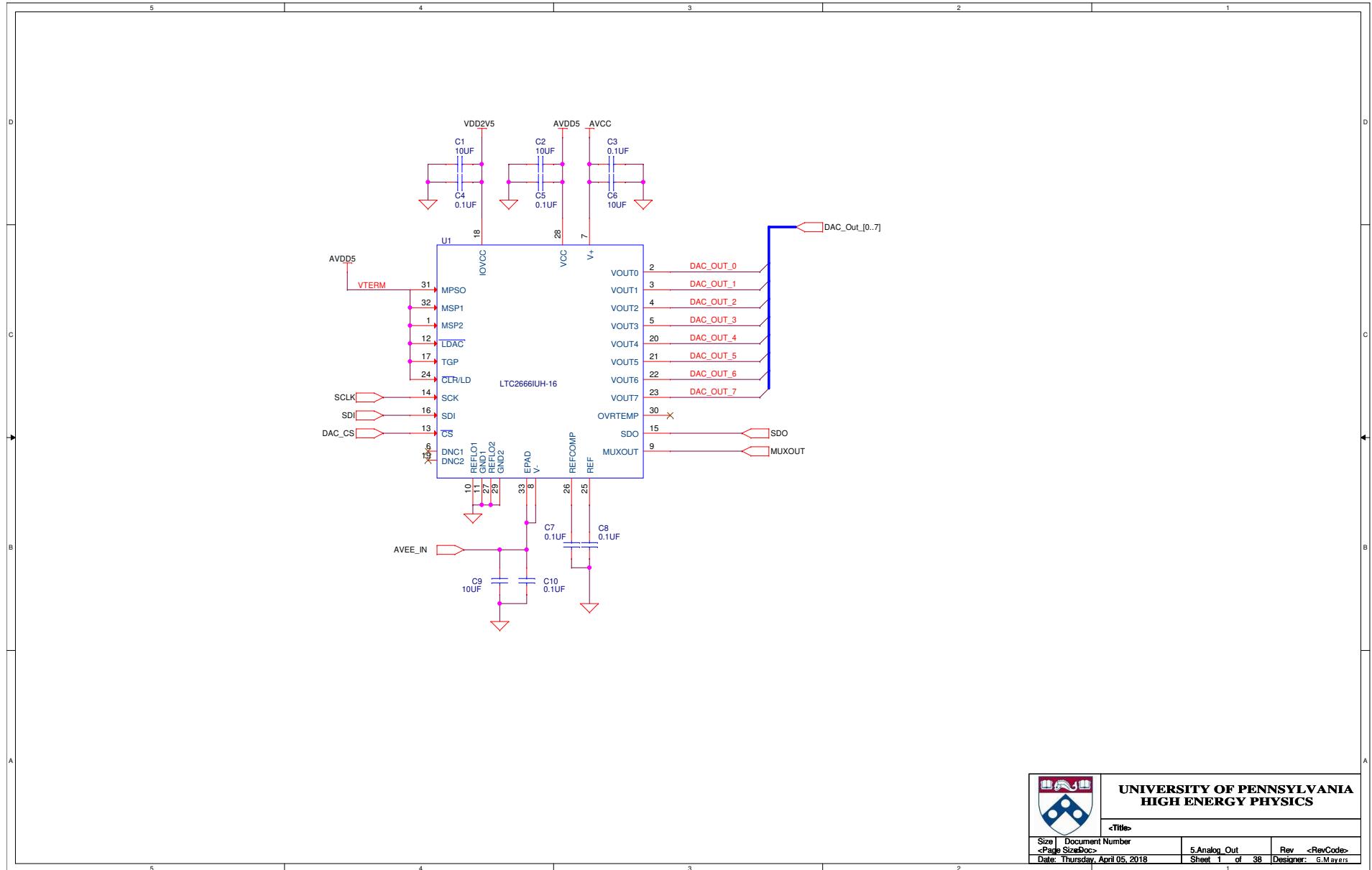
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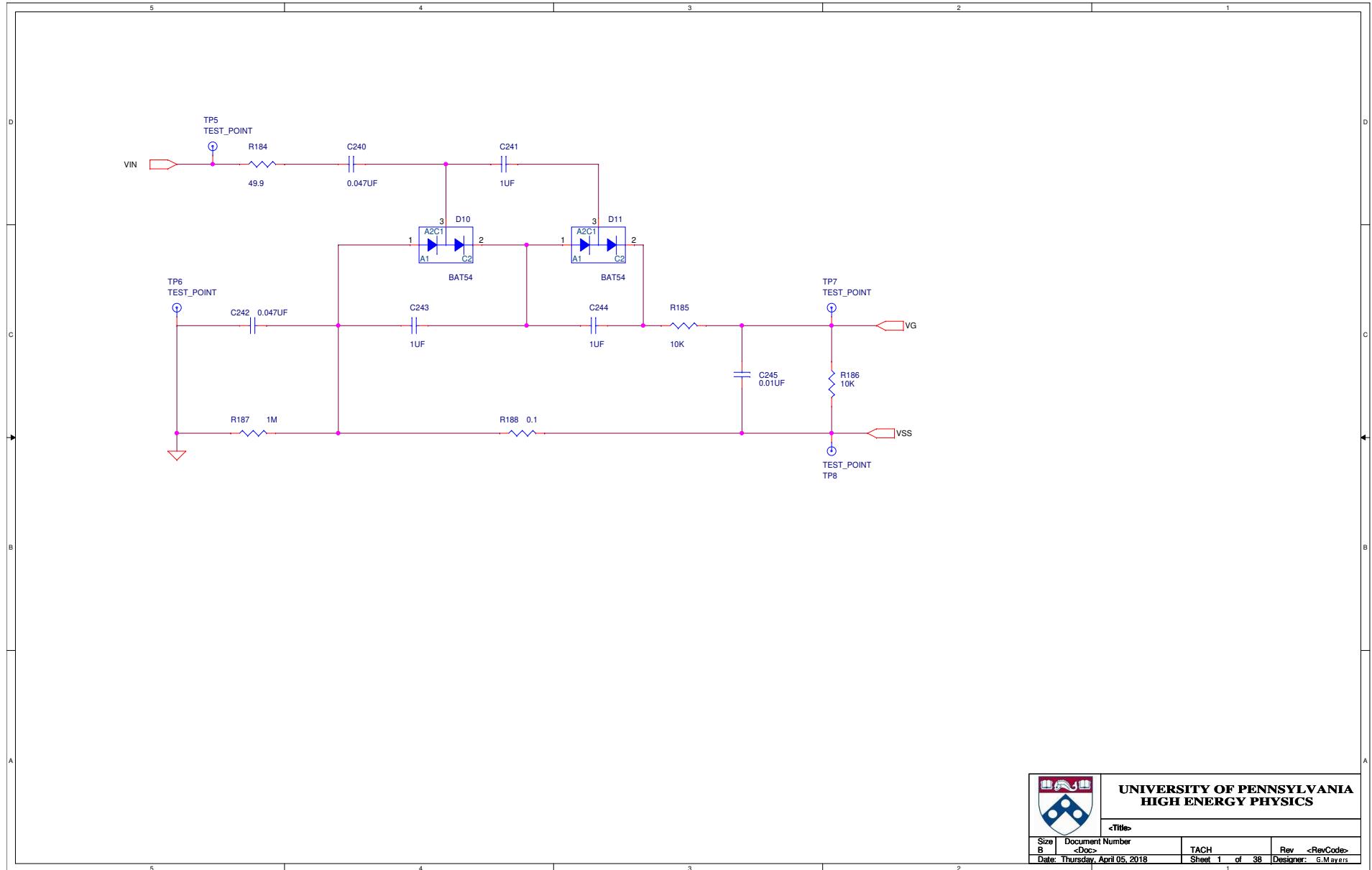
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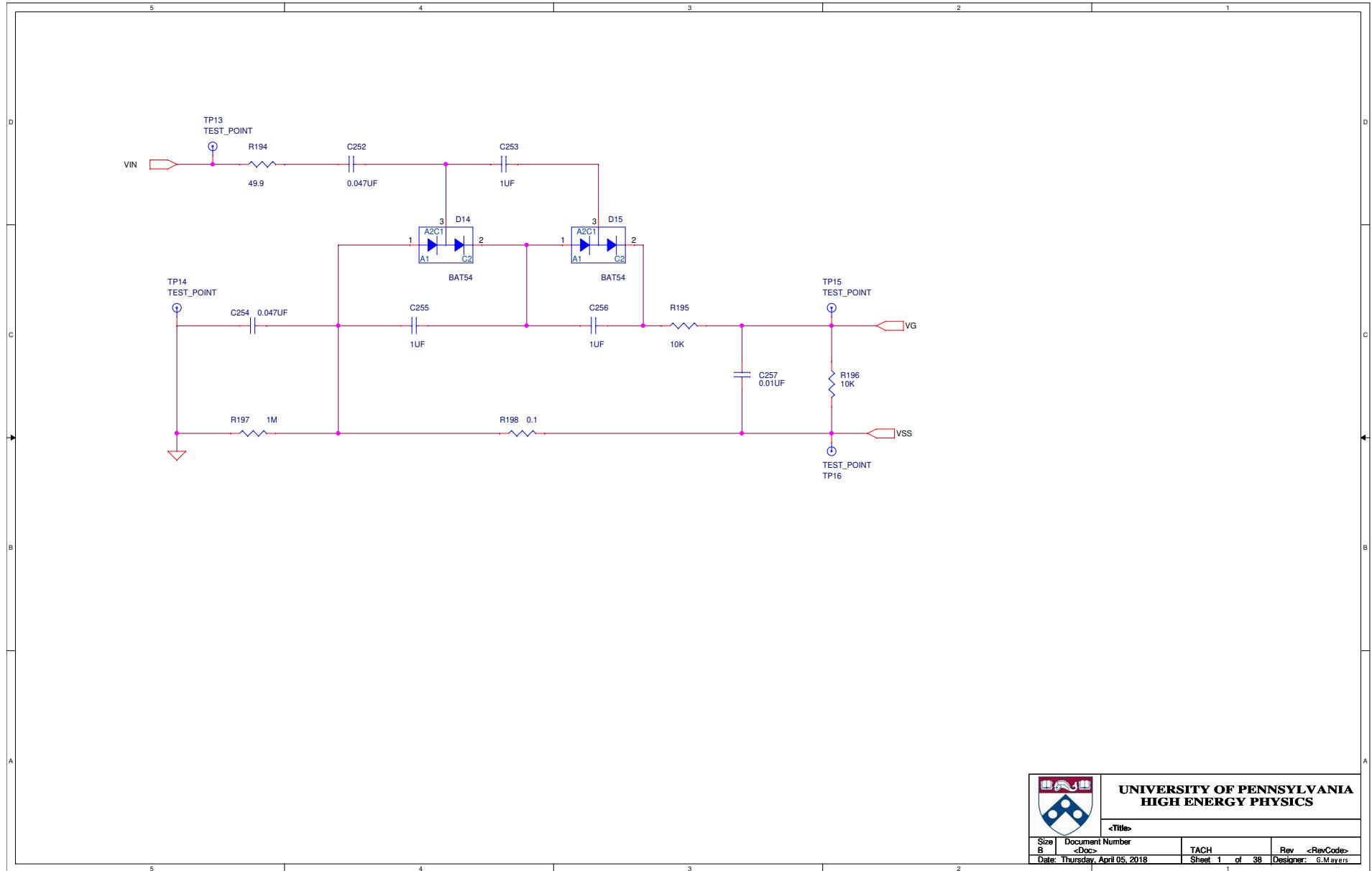
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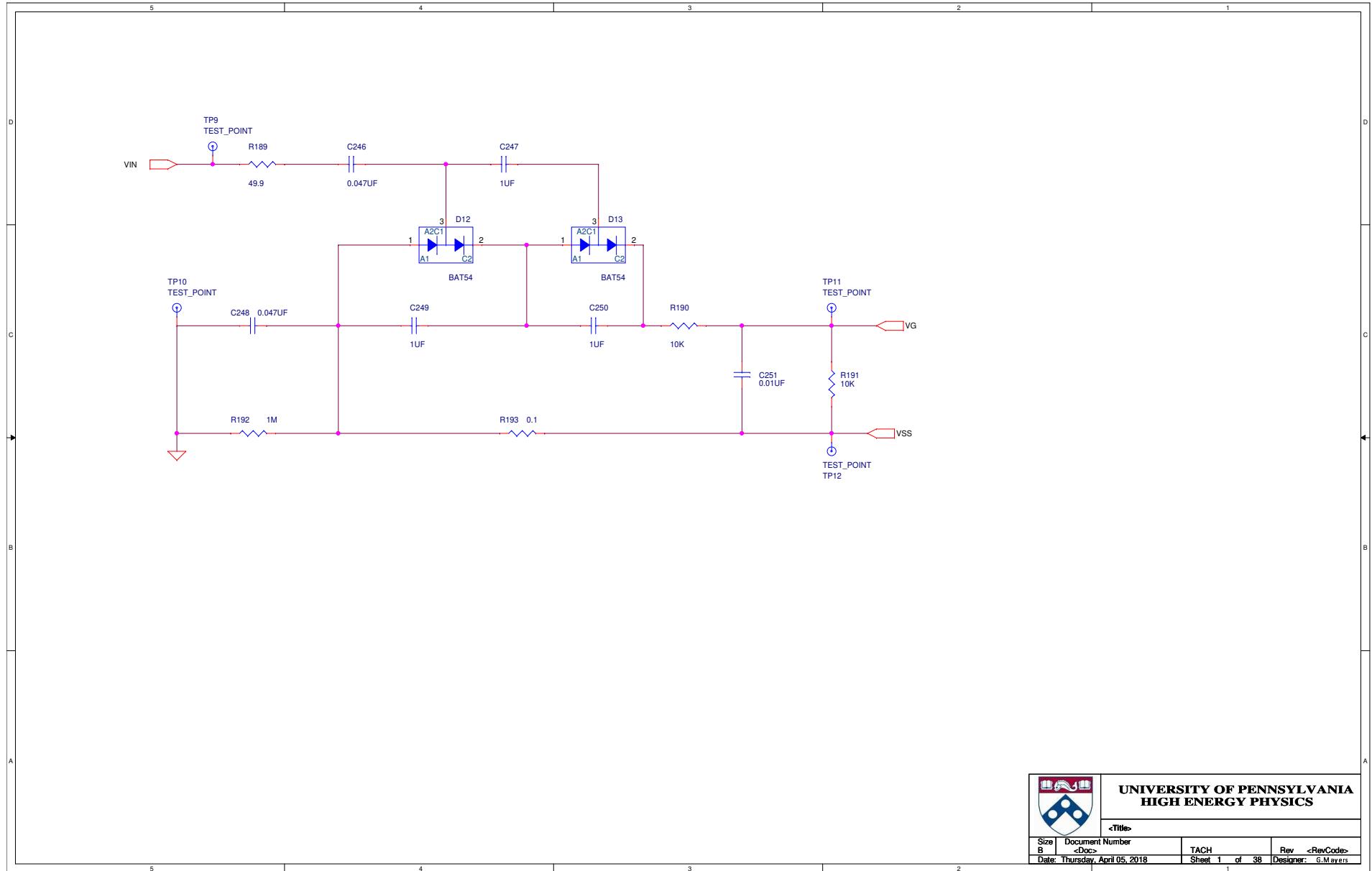
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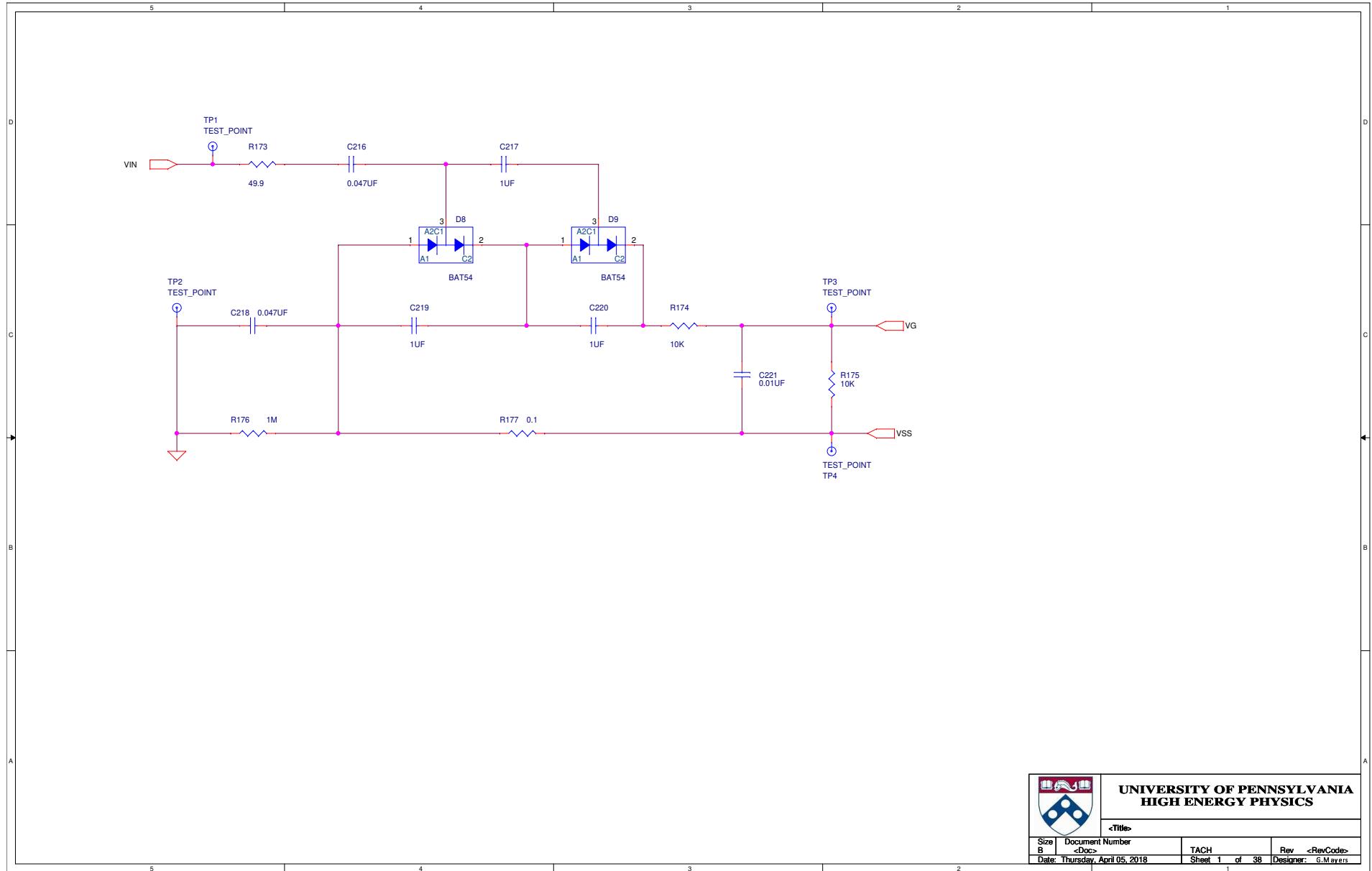


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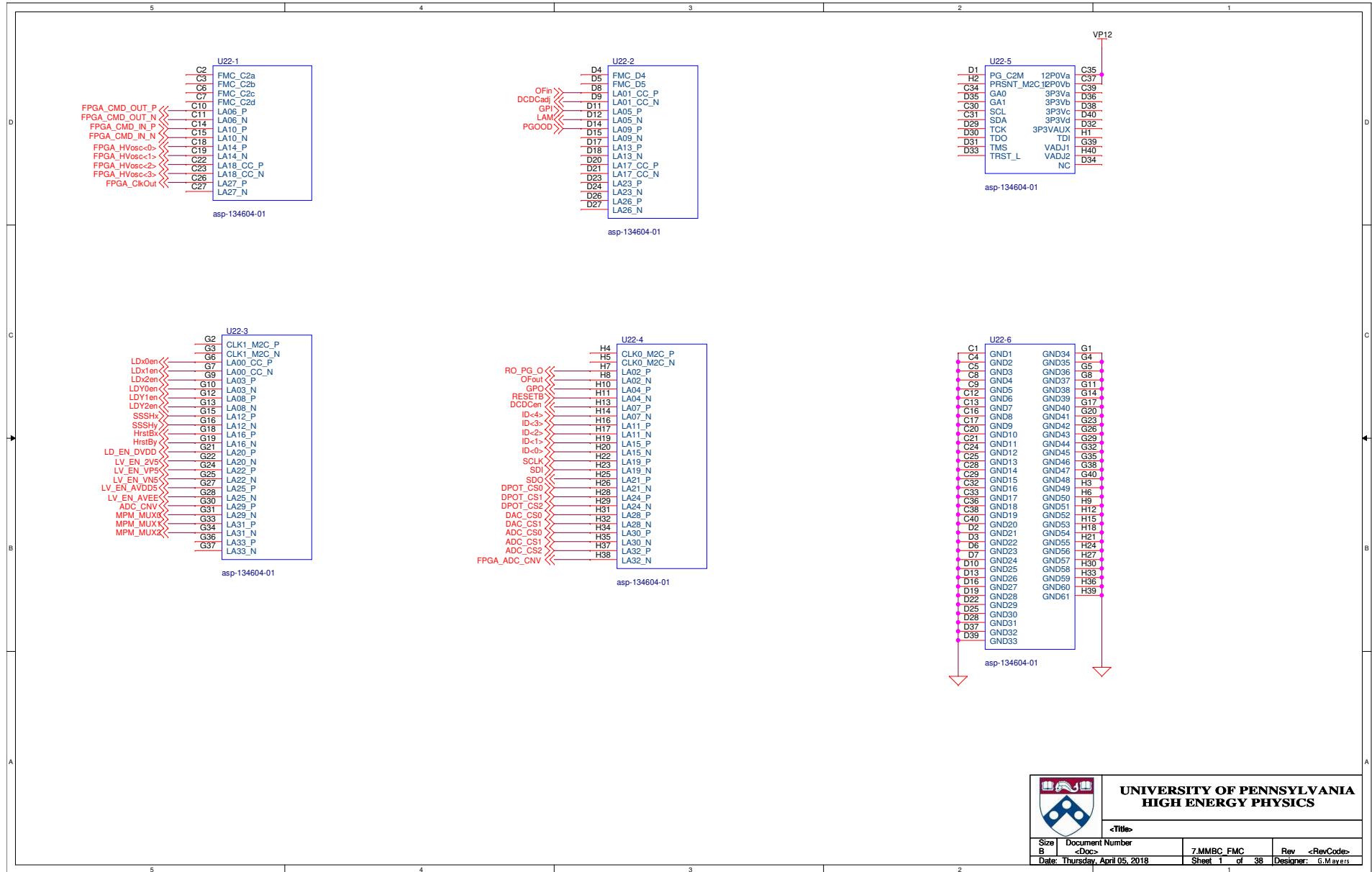
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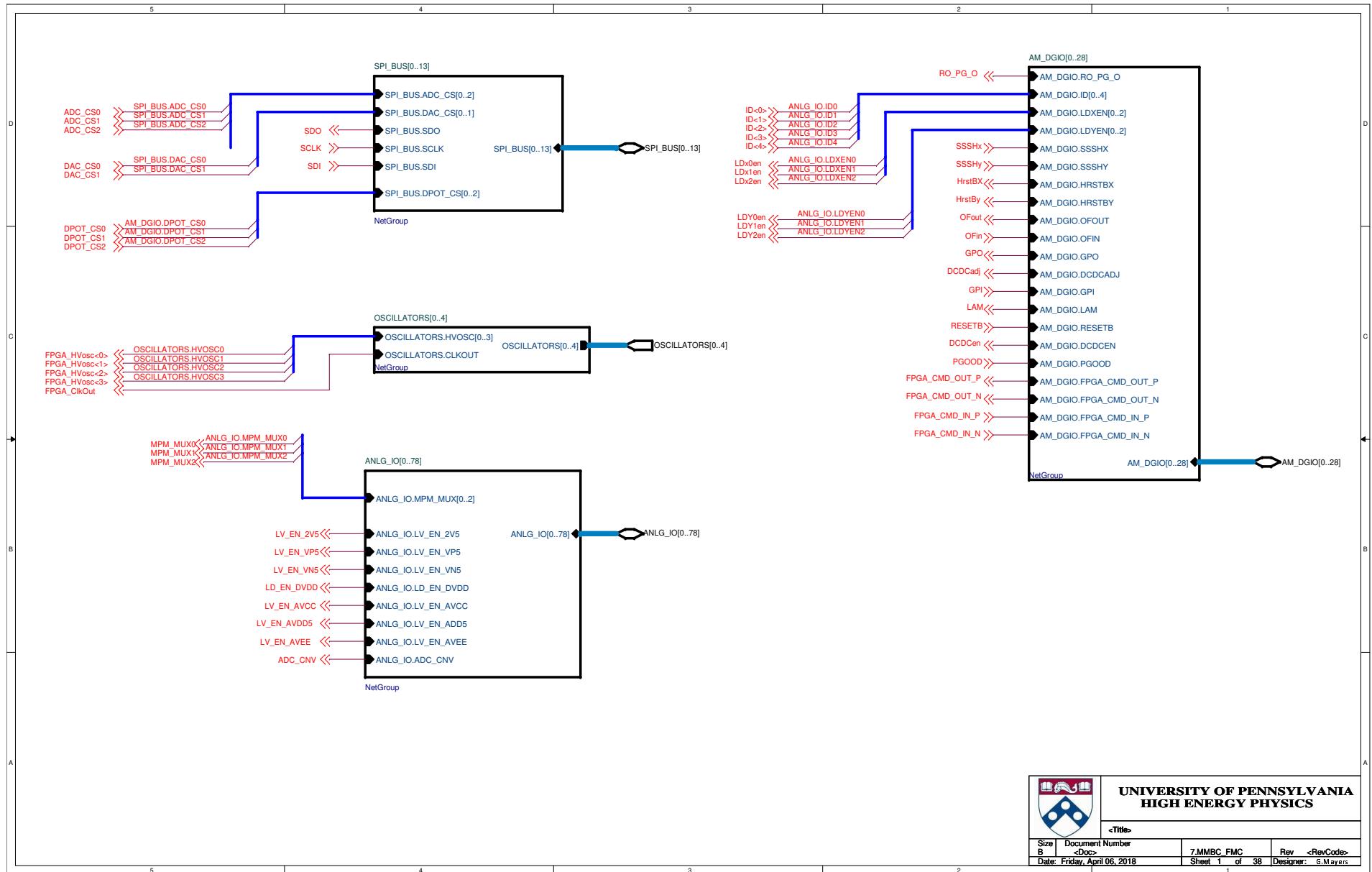


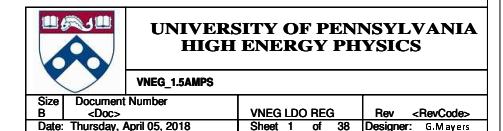
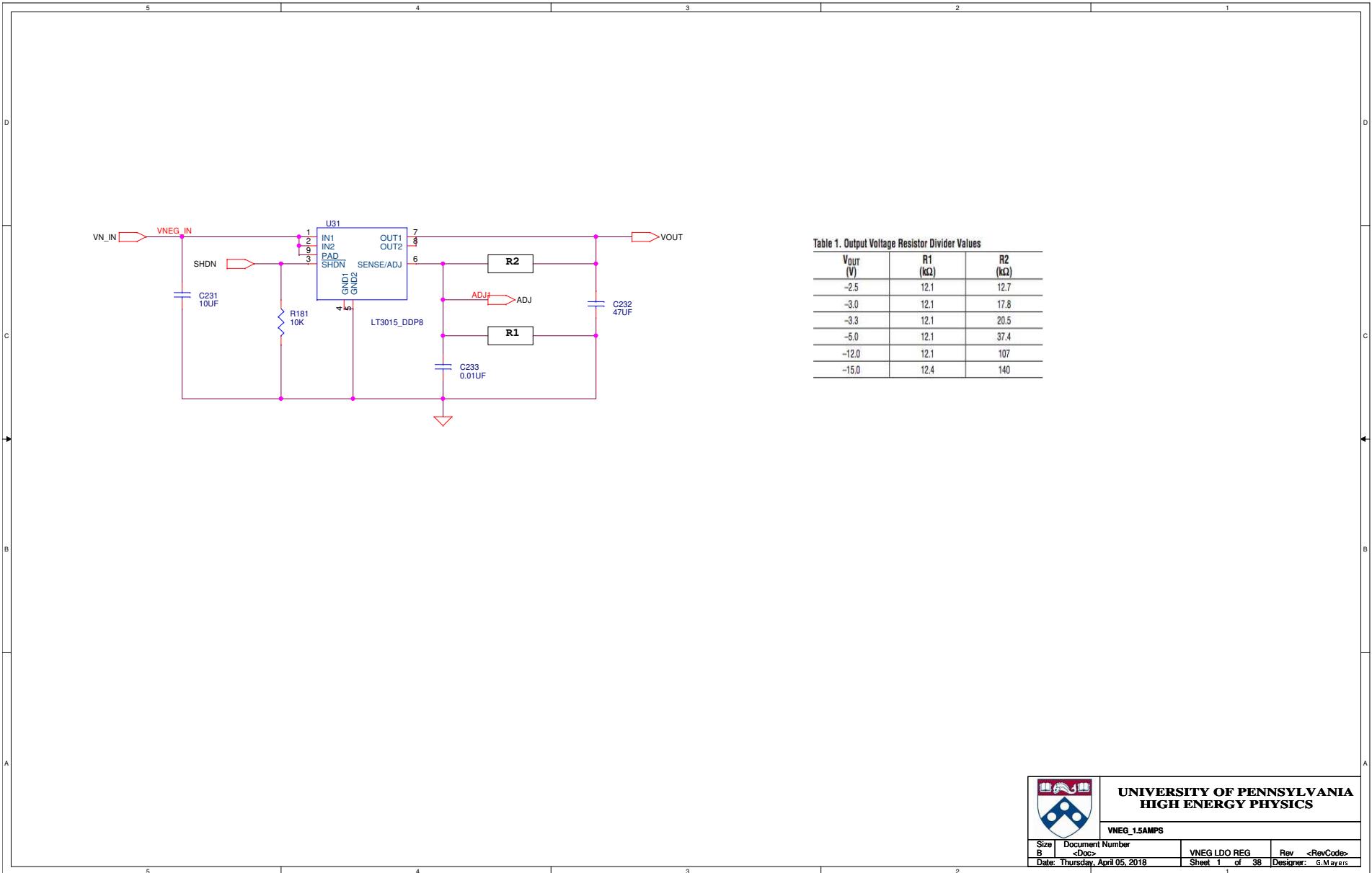


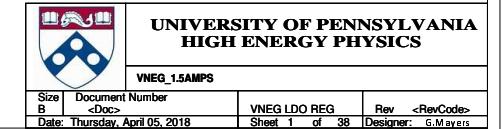
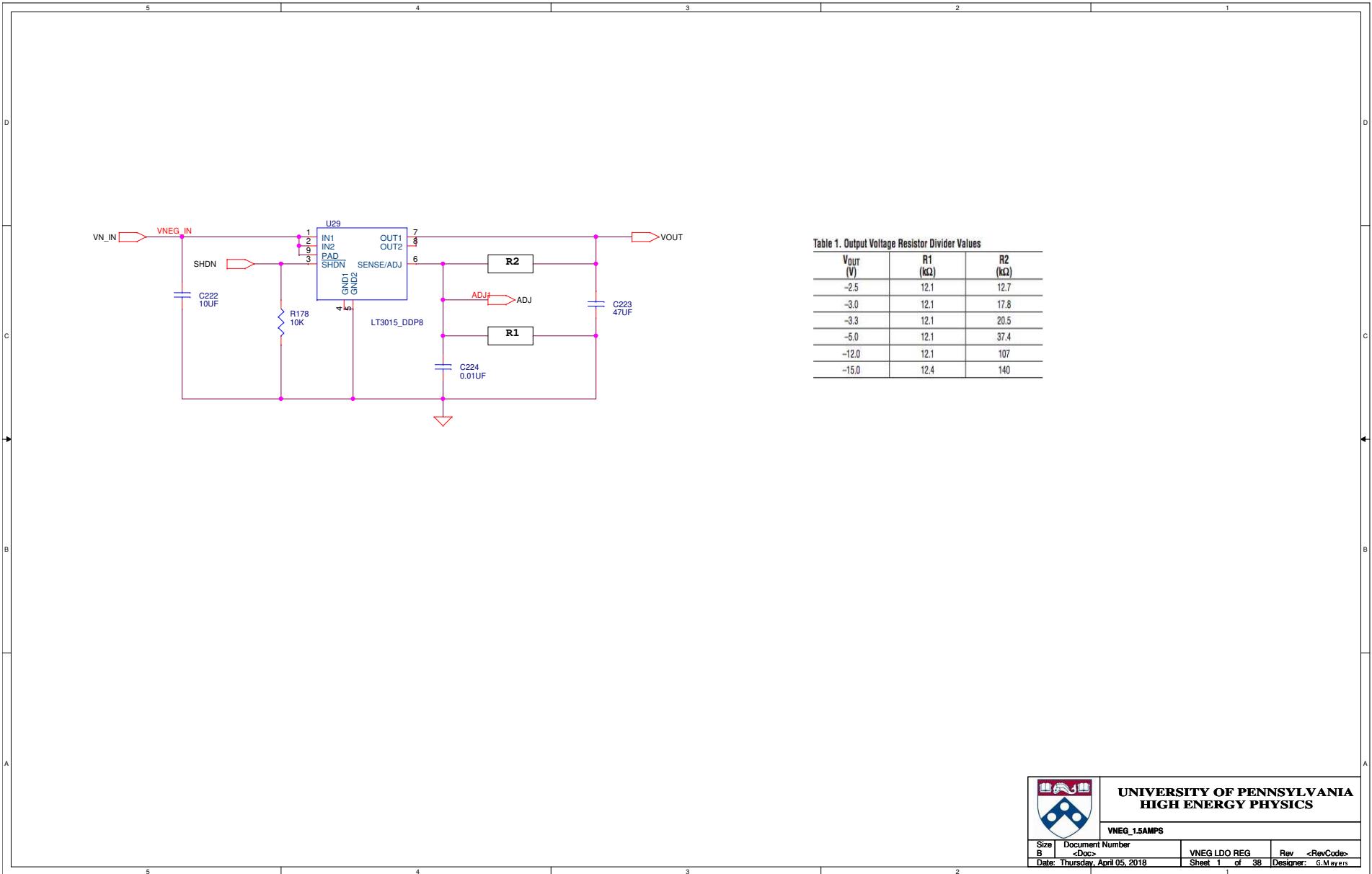
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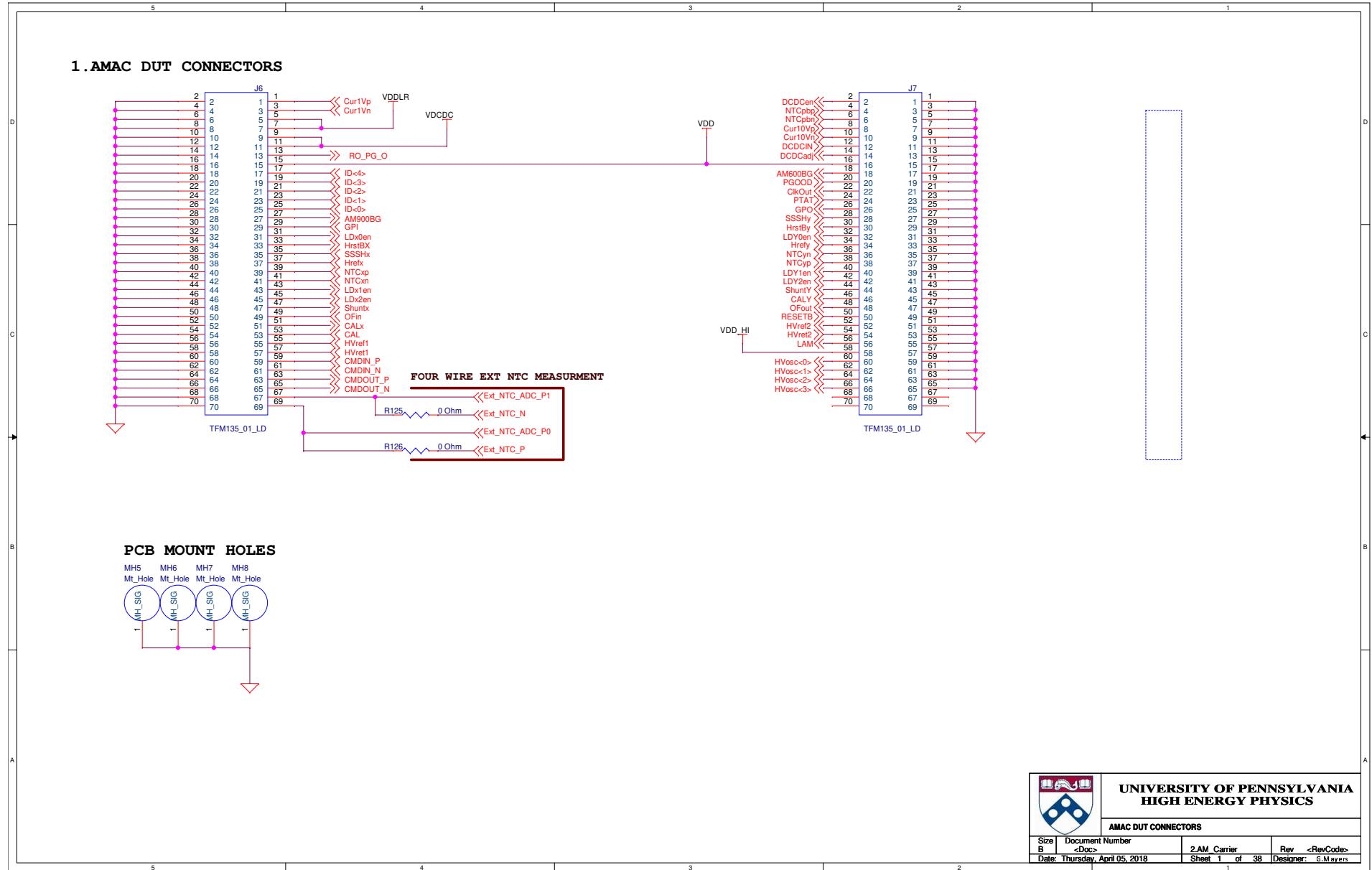
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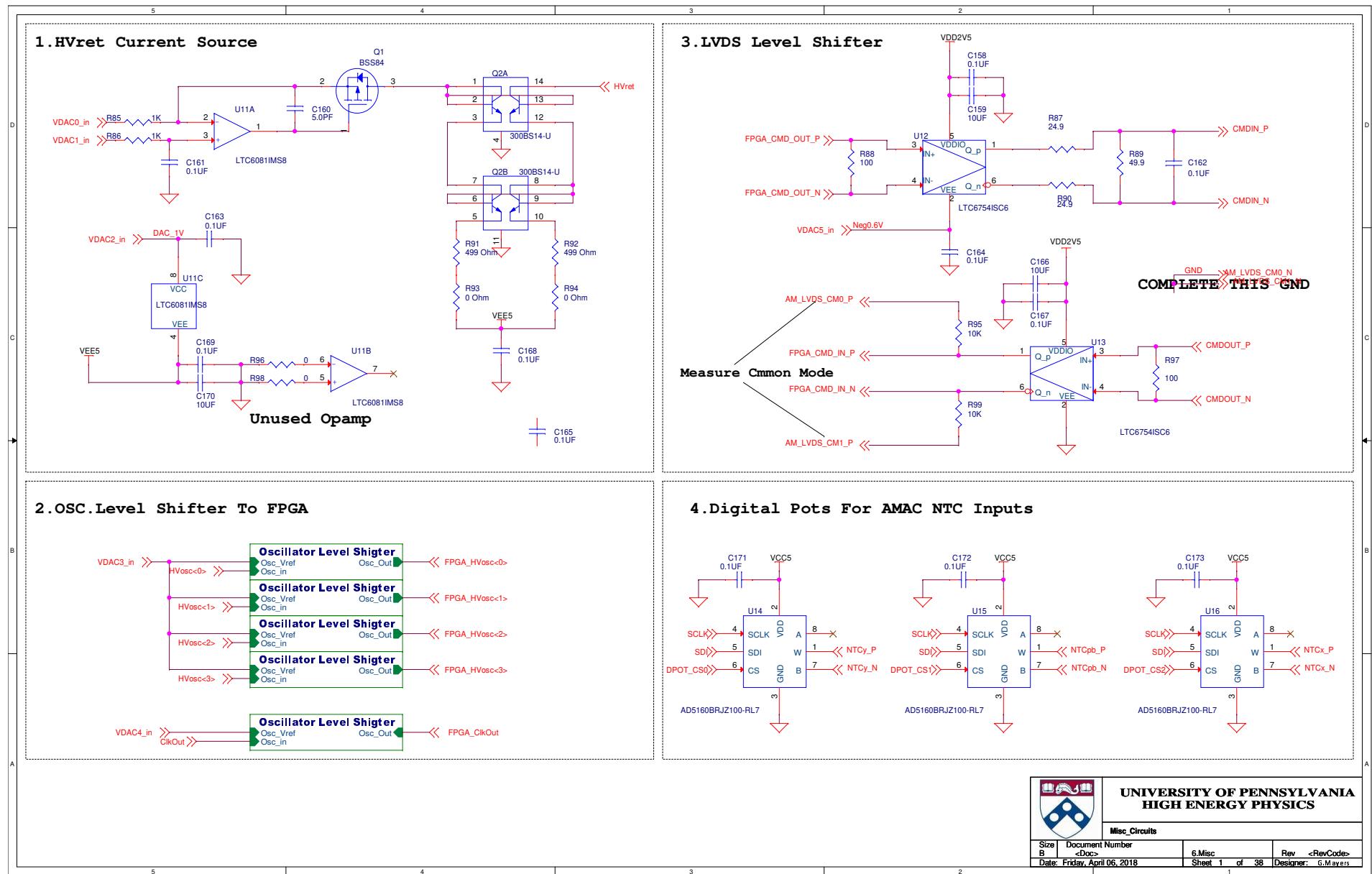


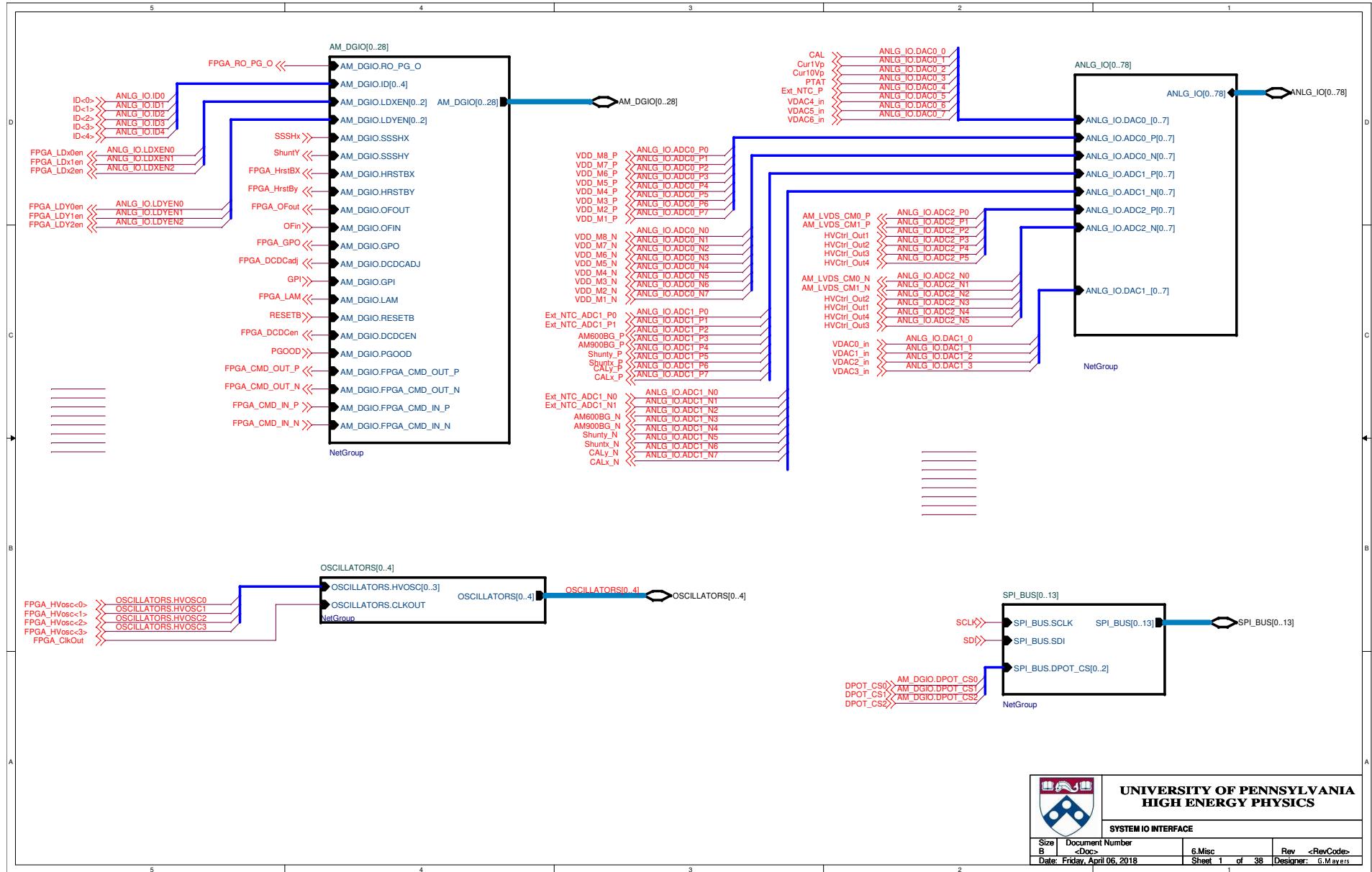




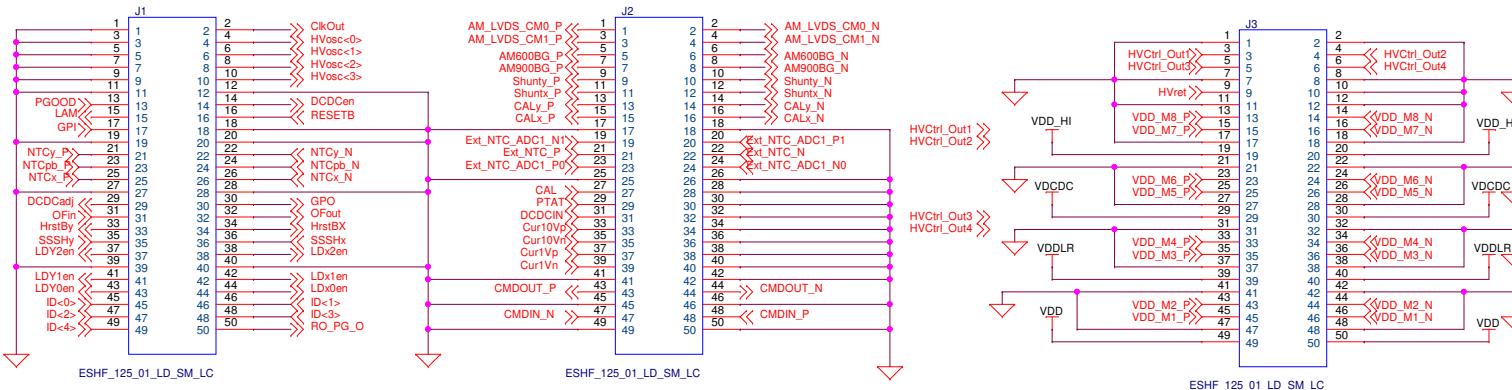




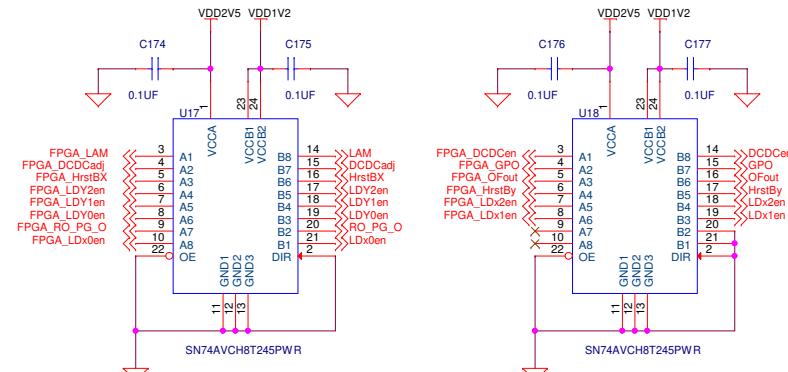




1. ATCB Interface Connectors



2. AMAC To FPGA DIO Level Translators



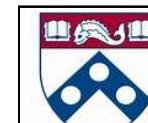
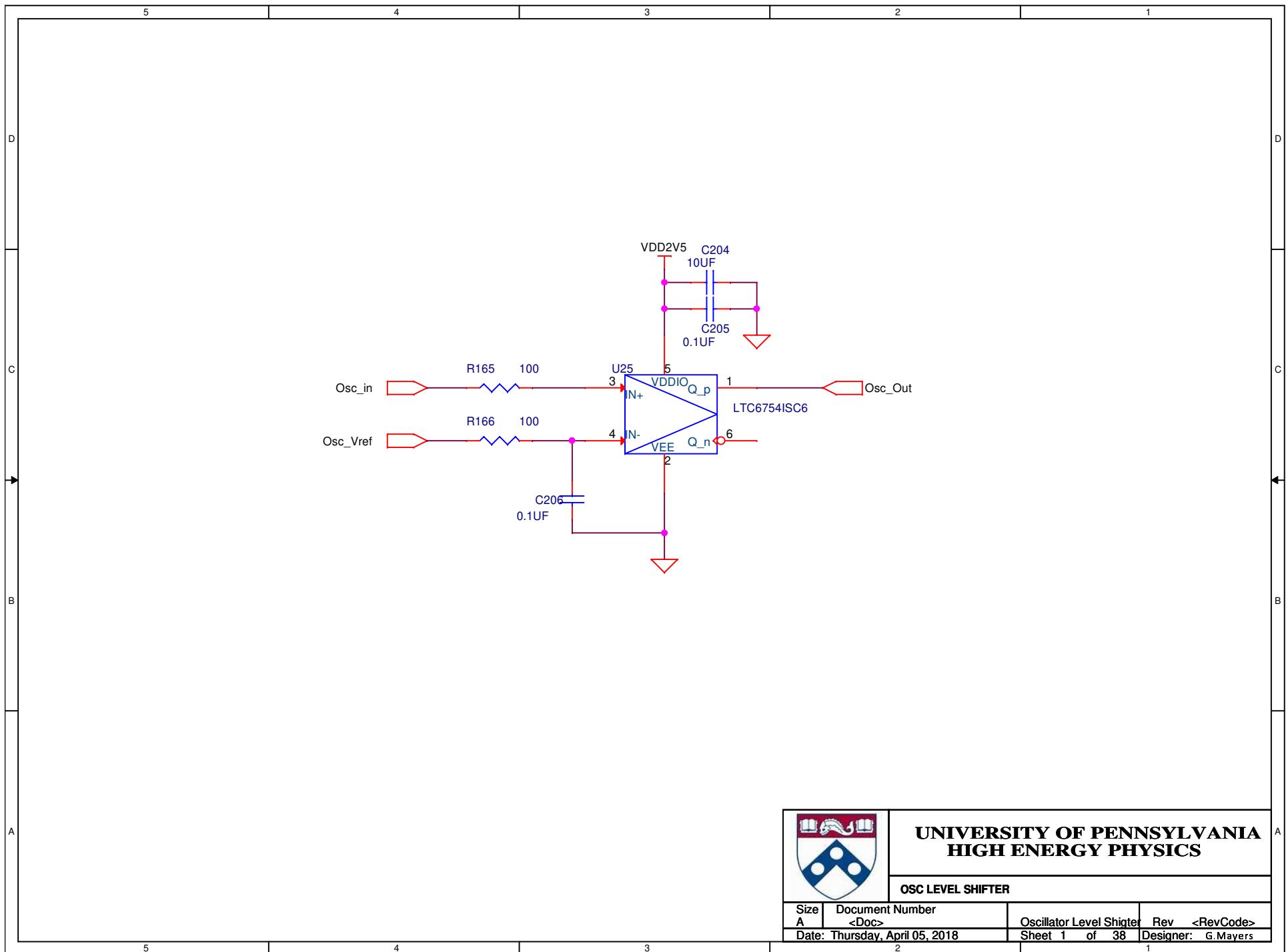
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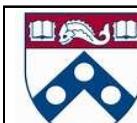
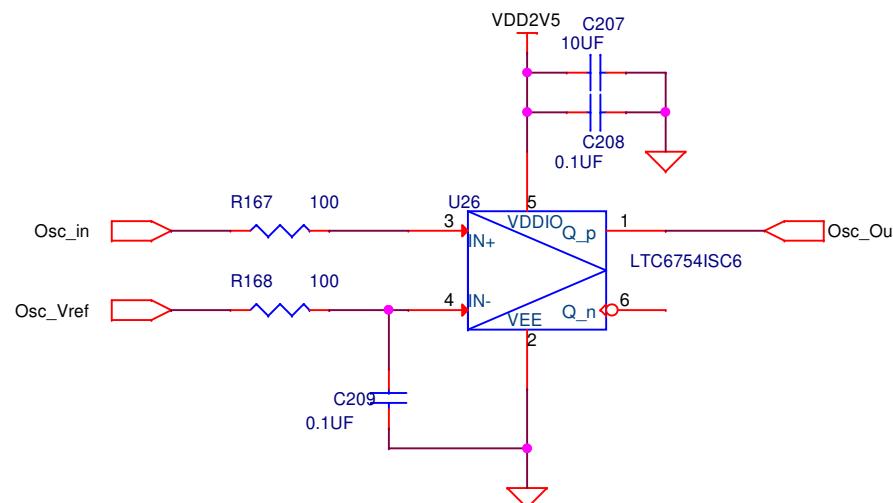
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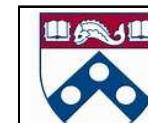
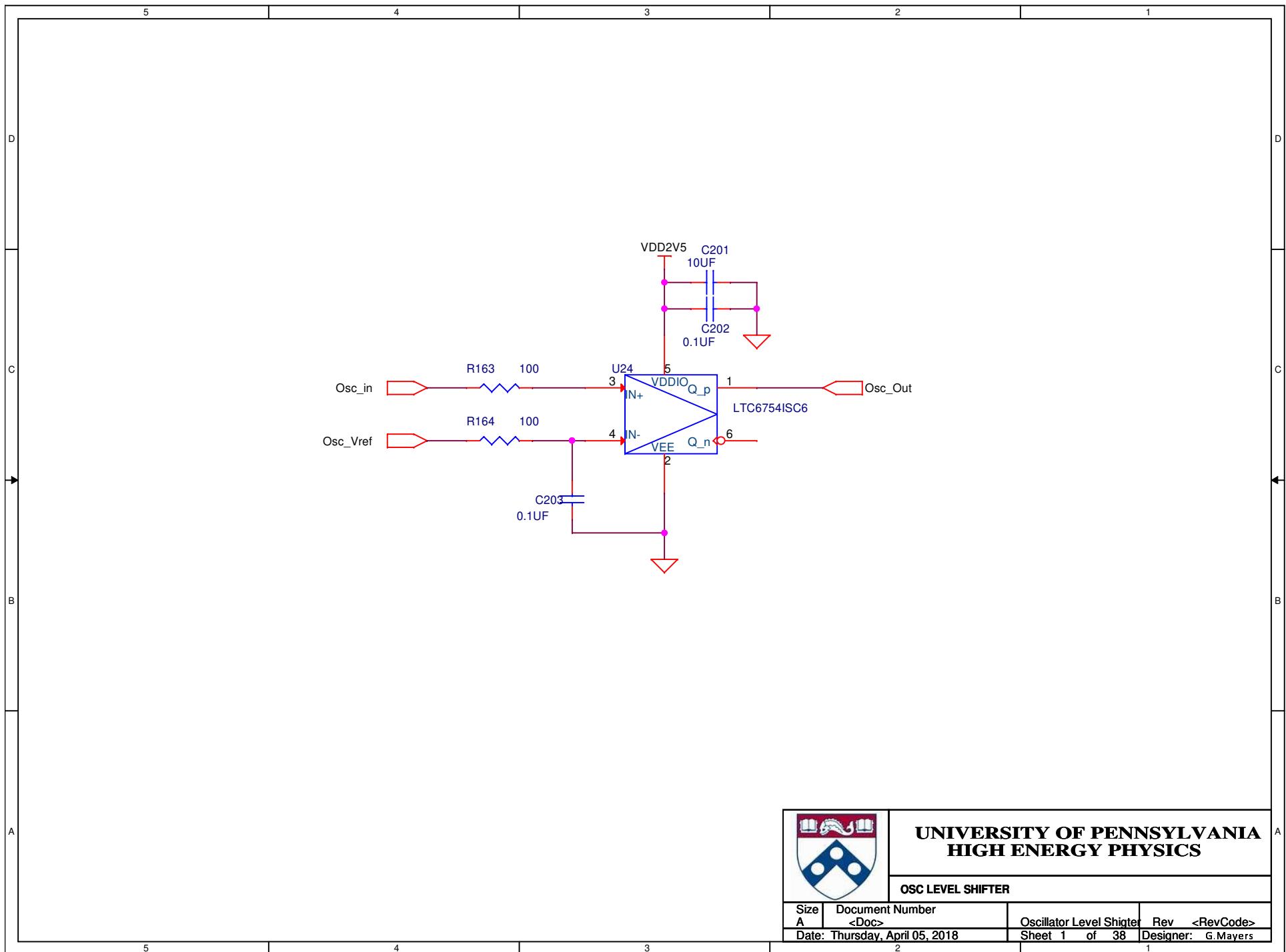
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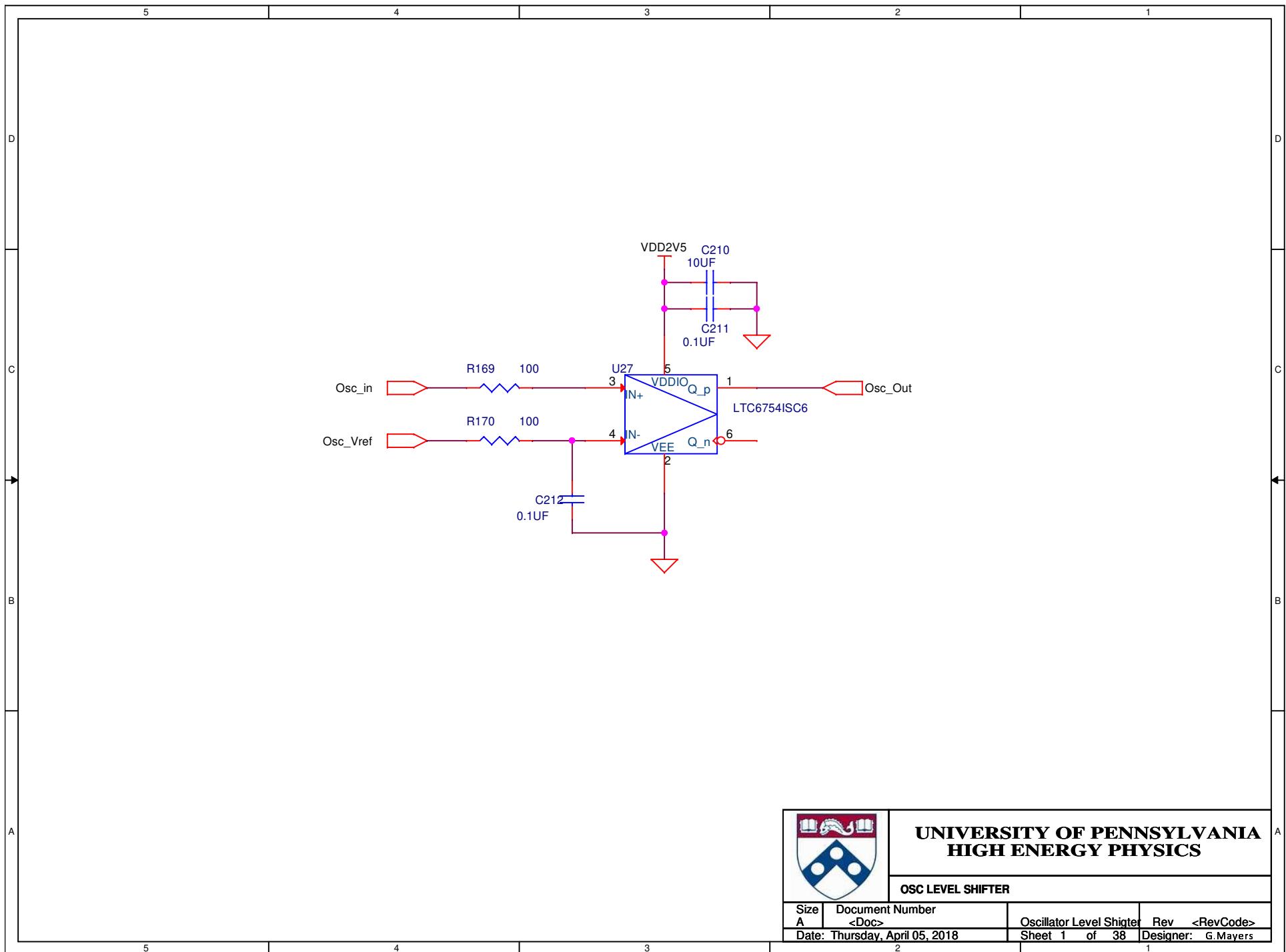


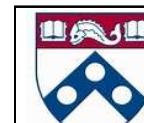
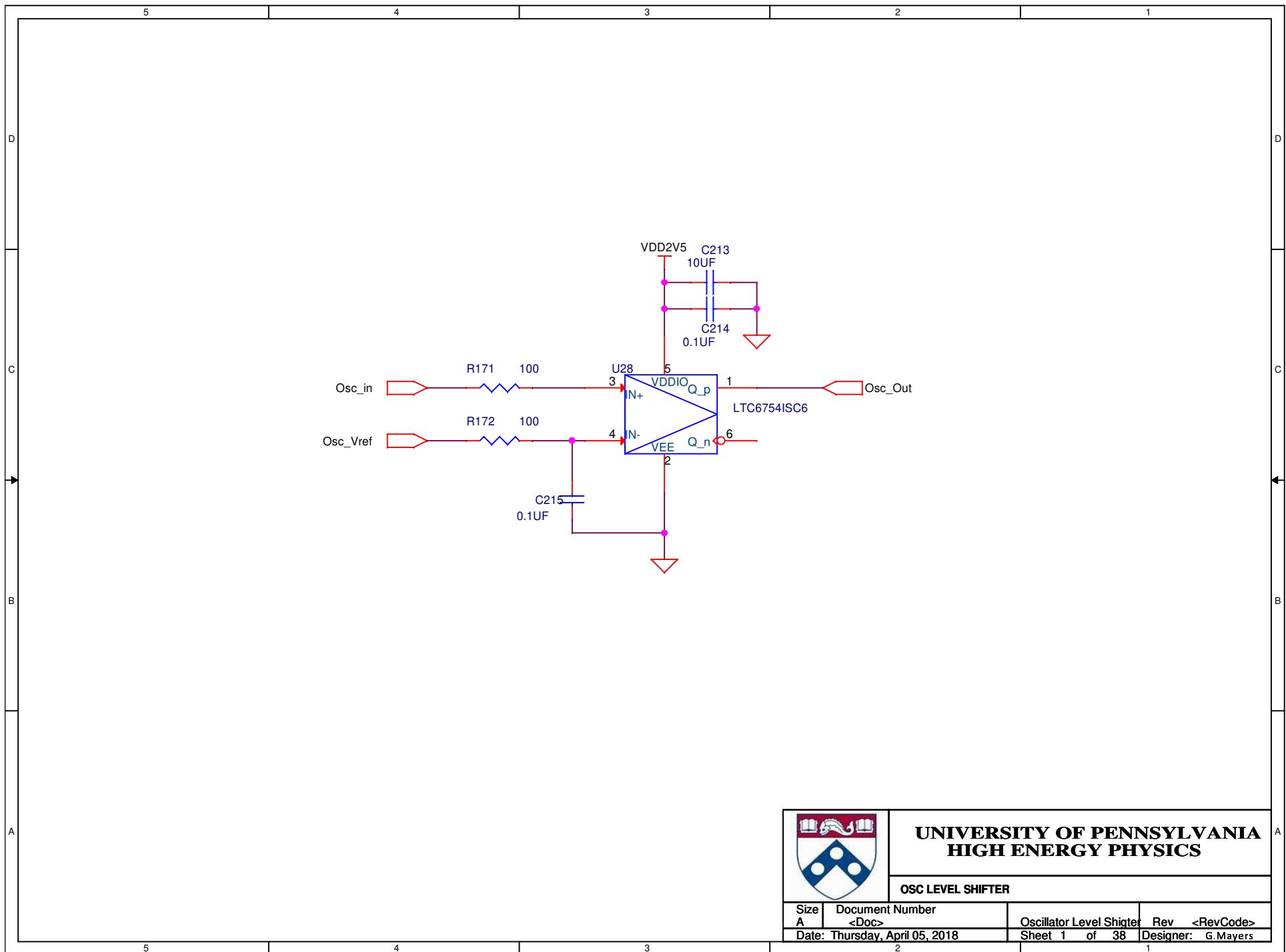
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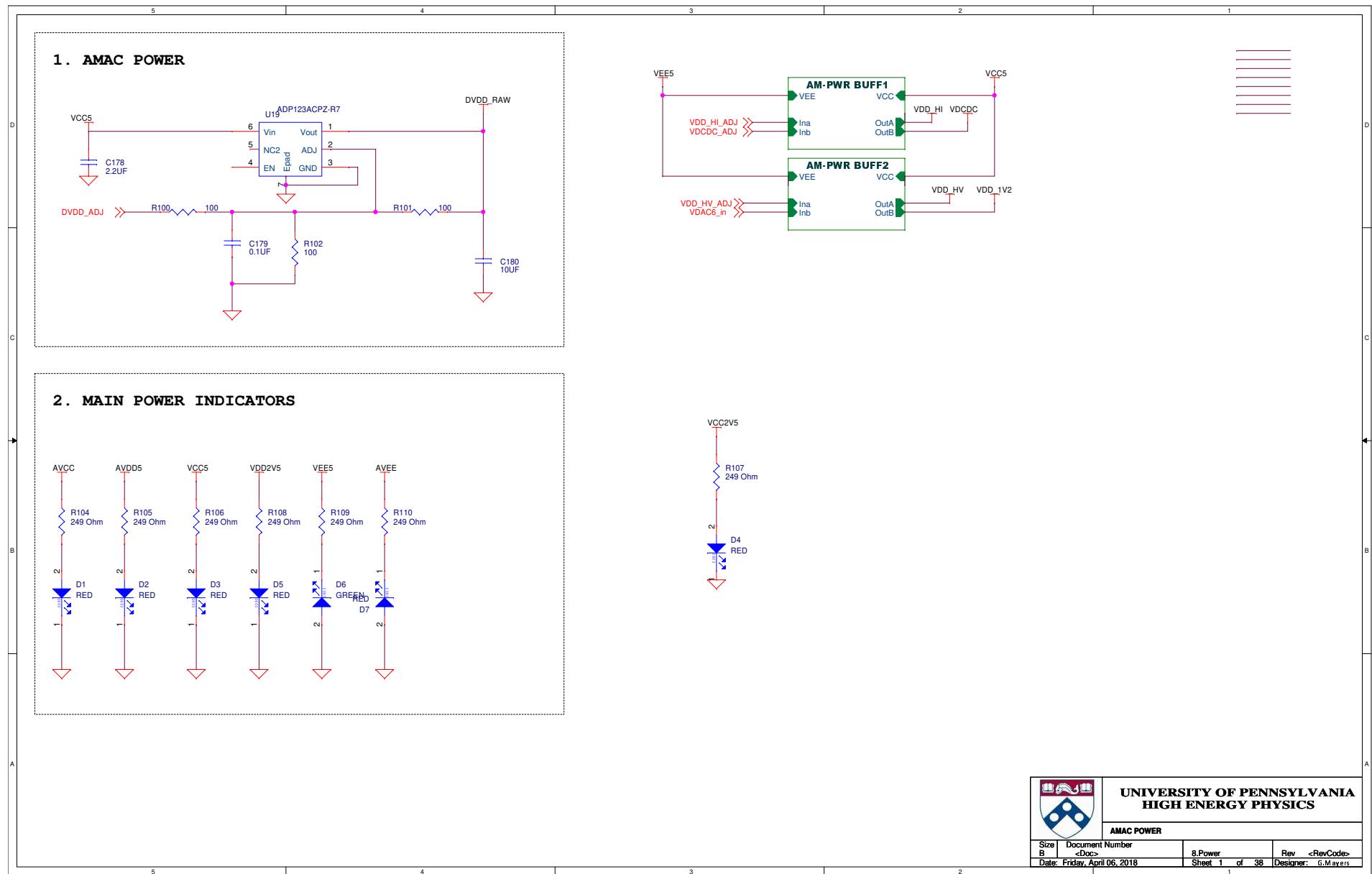
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AMAC POWER

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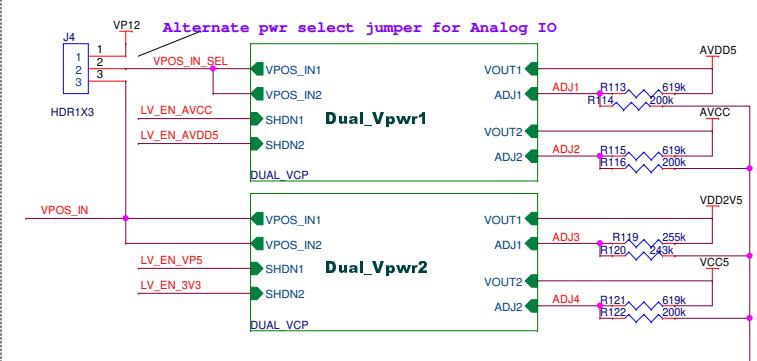
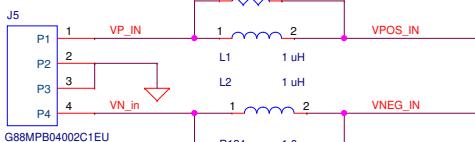


Table 1. Output Voltage Resistor Divider Values

V_{out} (V)	R1 (k)	R2 (k)
1.5	237	54.9
1.8	237	113
2.5	243	255
3	232	340
3.3	210	357
5	200	619

2. MAIN POWER IN



3. VNEG LDO REGULATOR MODULES

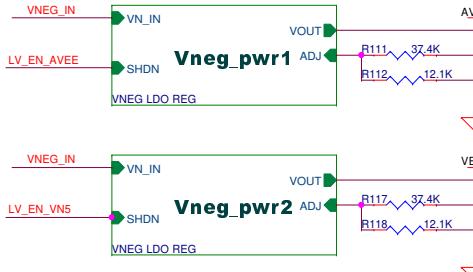
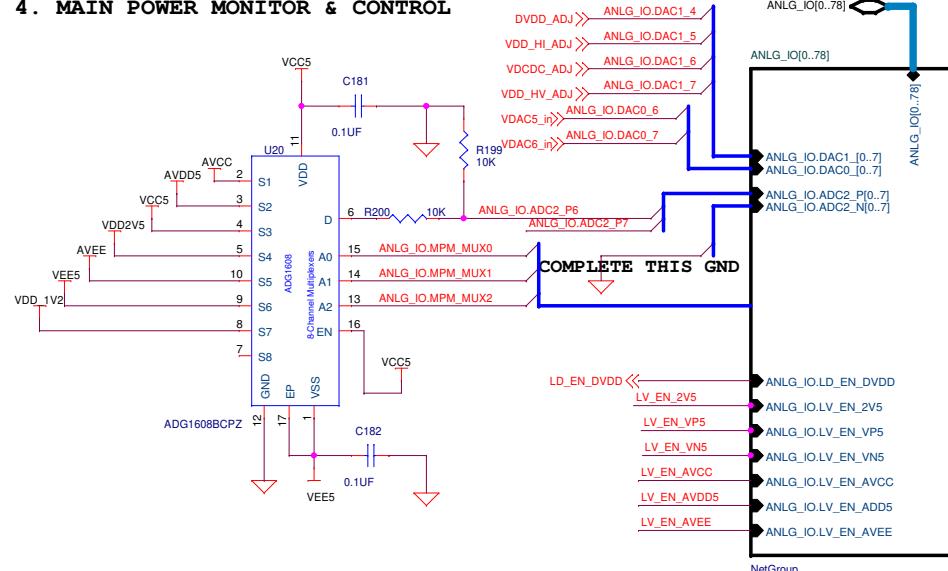


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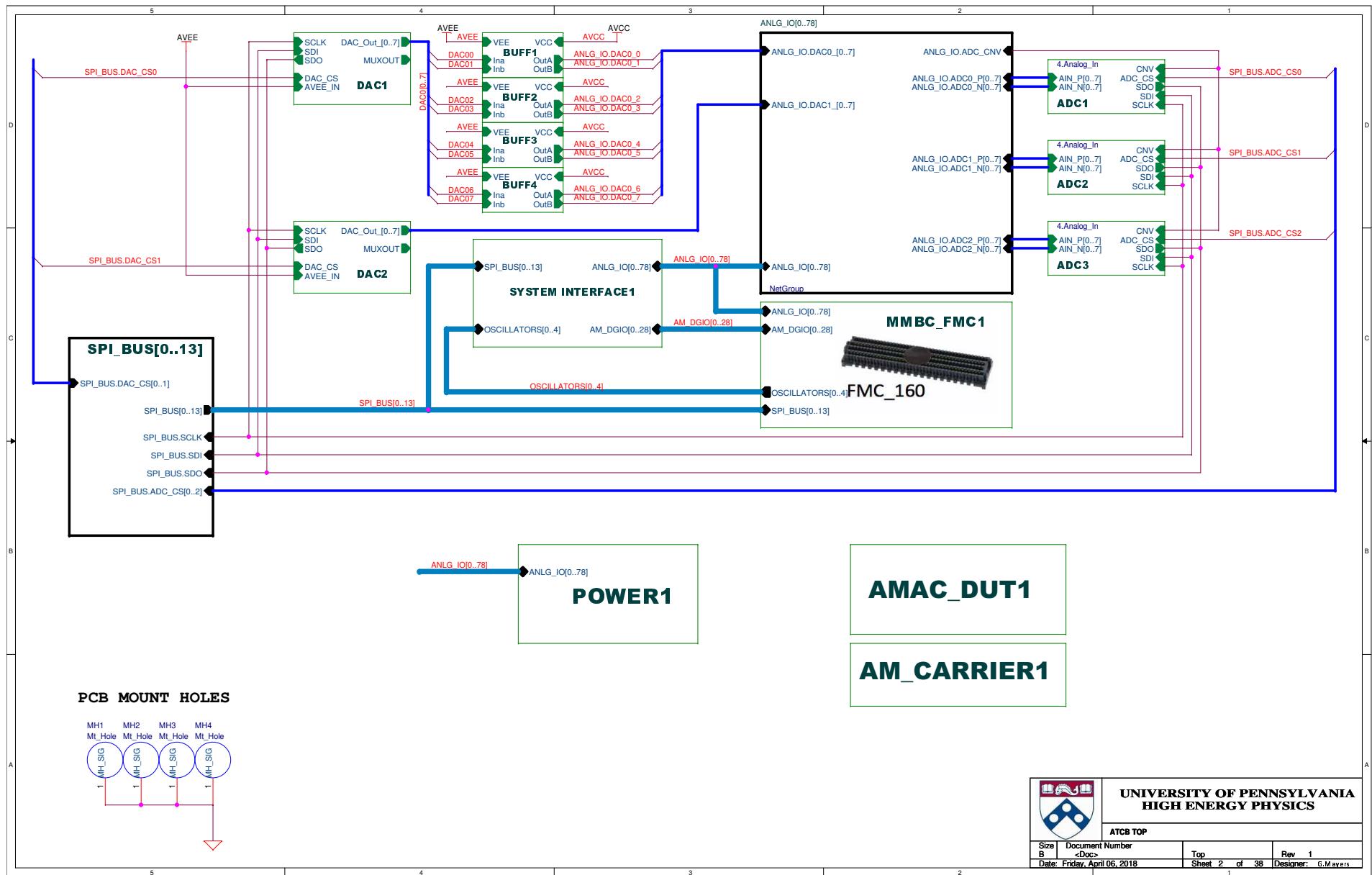
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
-2.5	12.1	12.7
-3.0	12.1	17.8
-3.3	12.1	20.5
-5.0	12.1	37.4
-12.0	12.1	107
-15.0	12.4	140

4. MAIN POWER MONITOR & CONTROL



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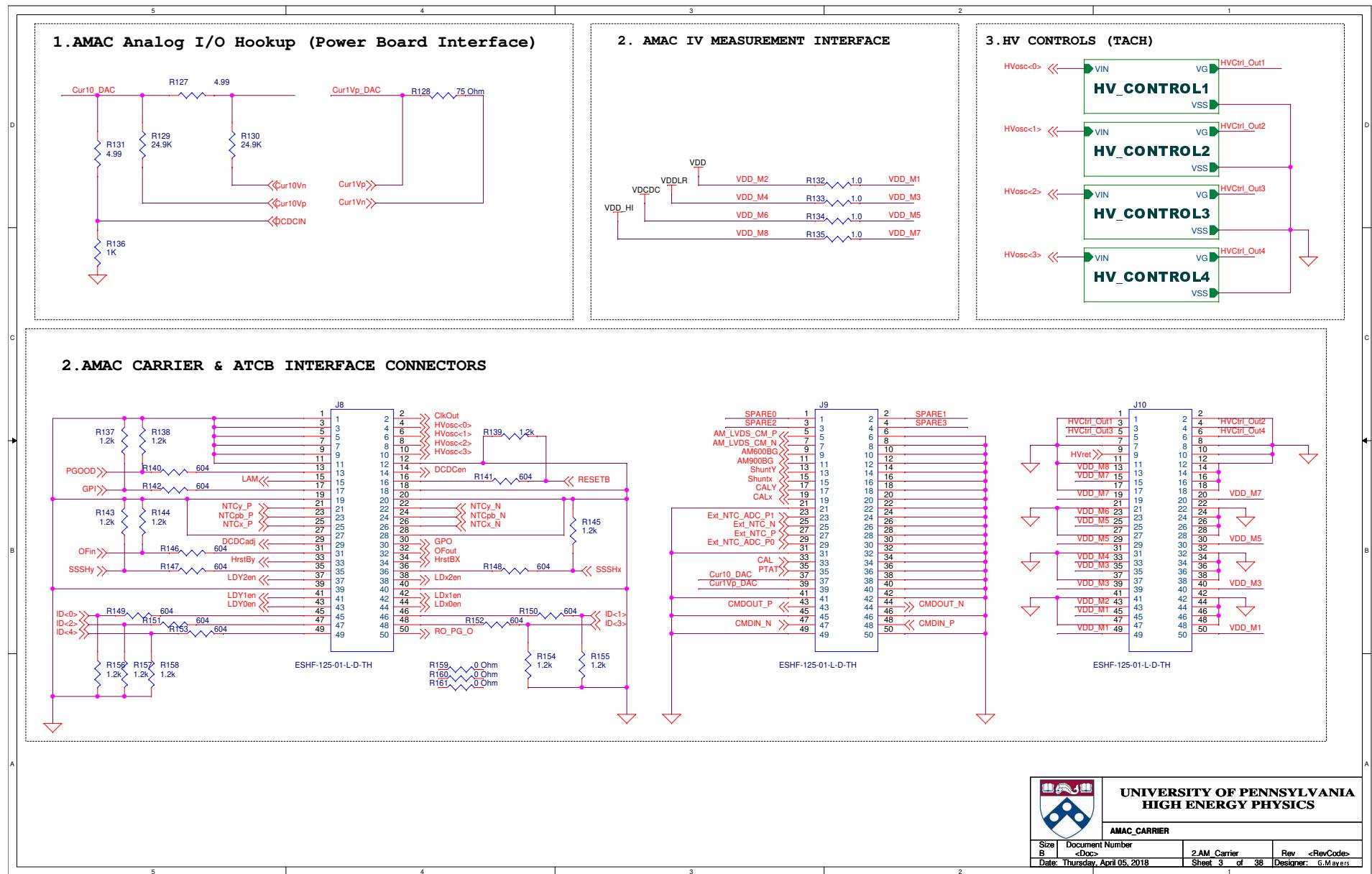
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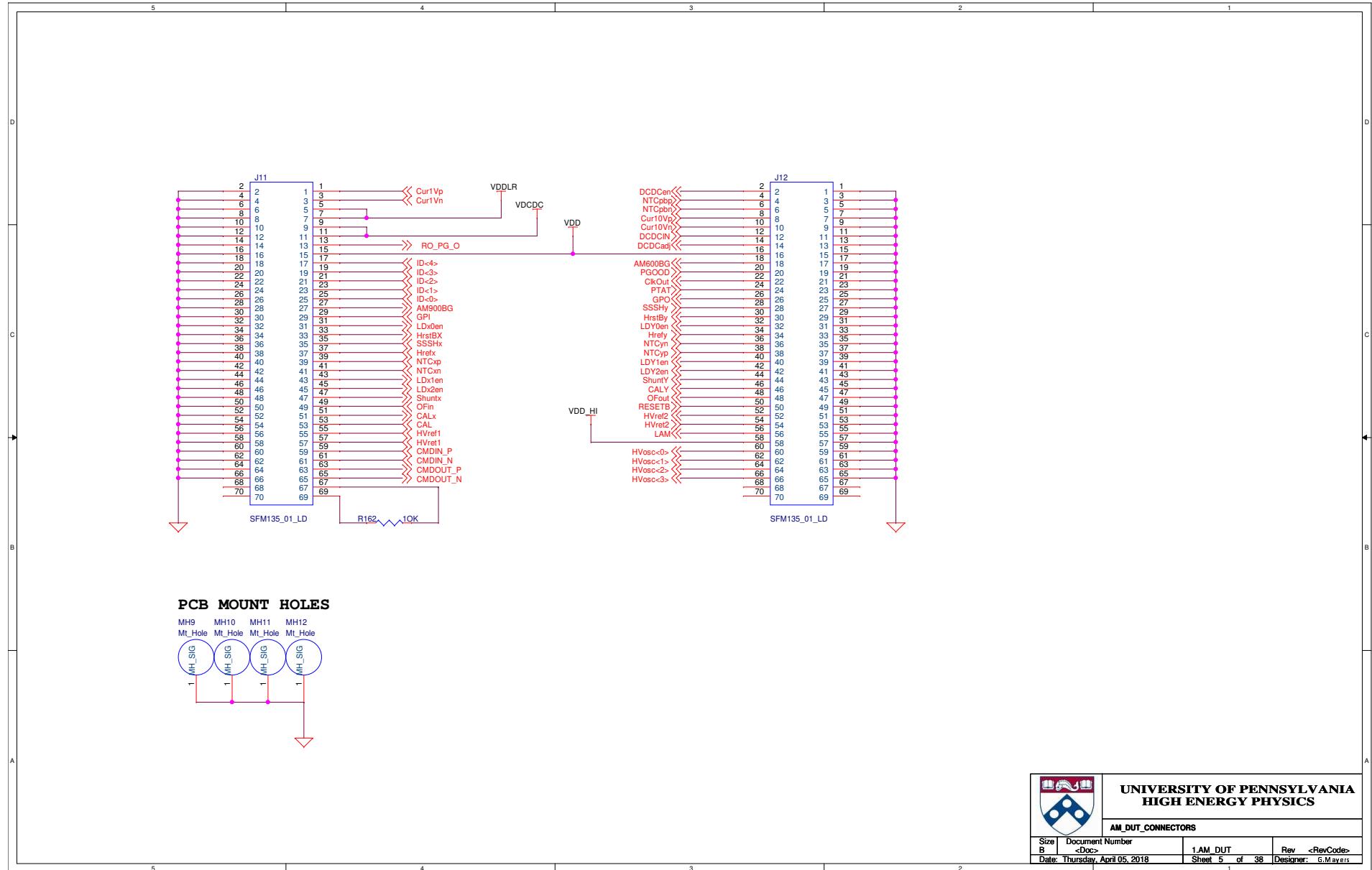
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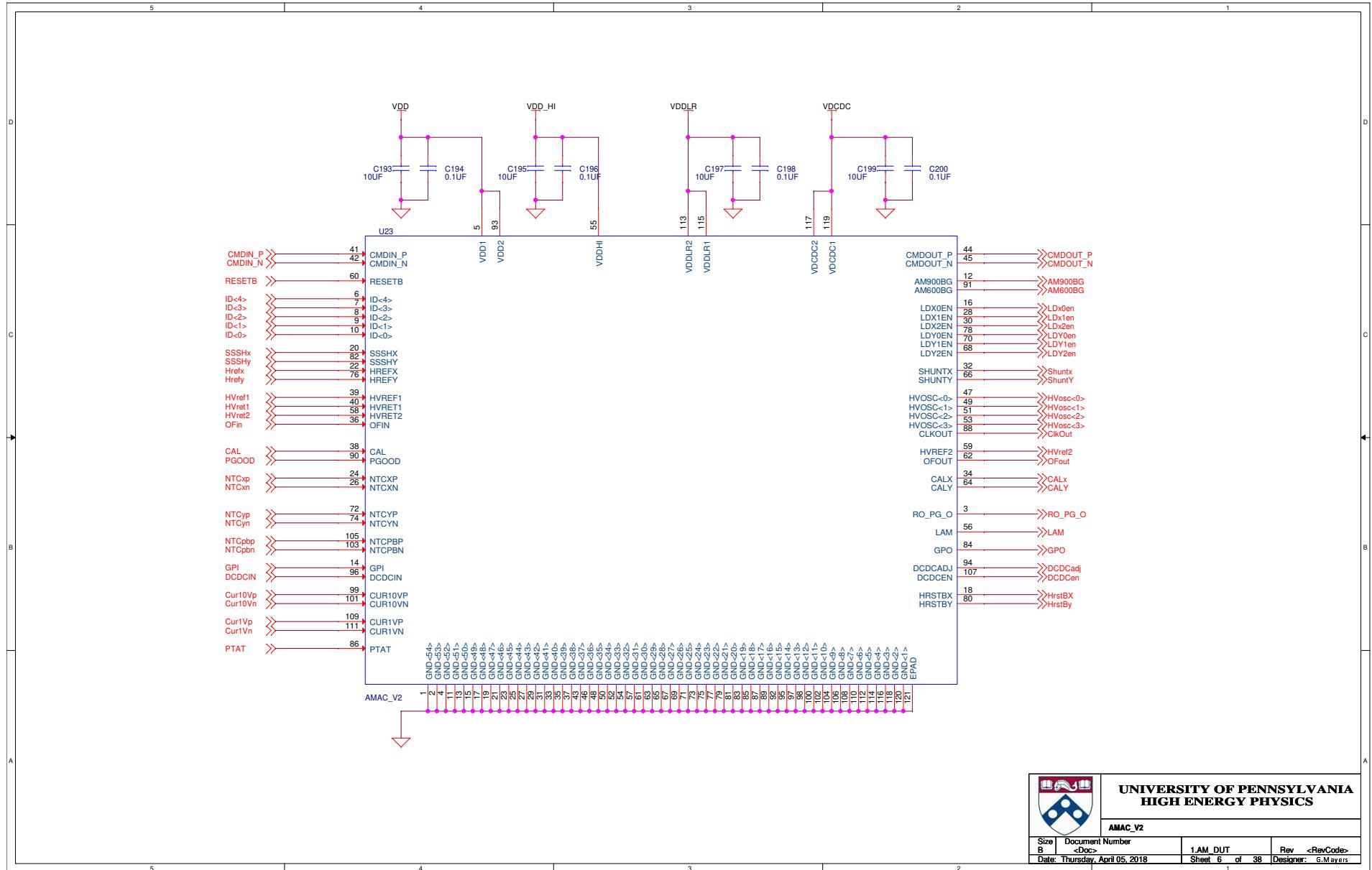
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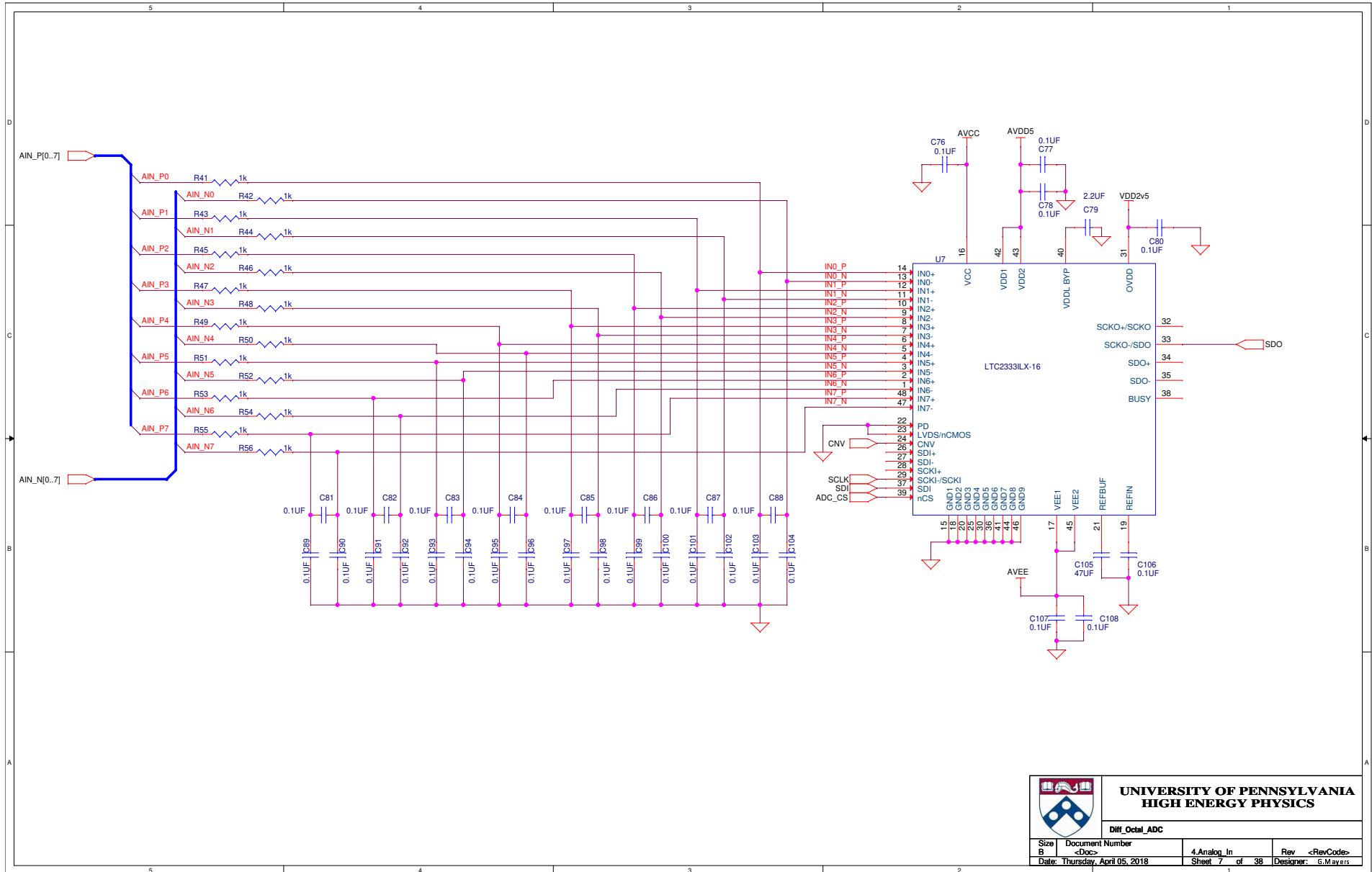






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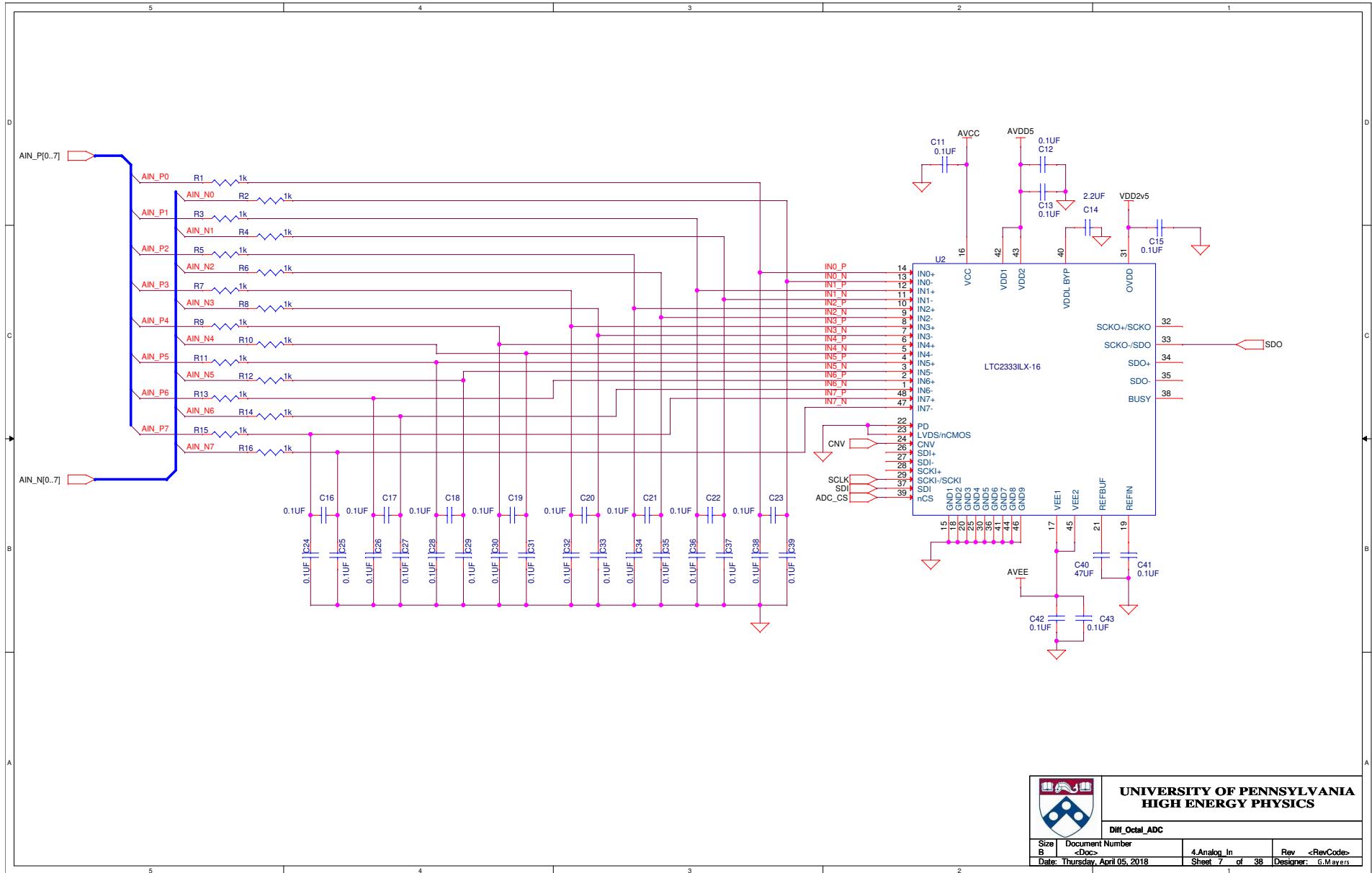
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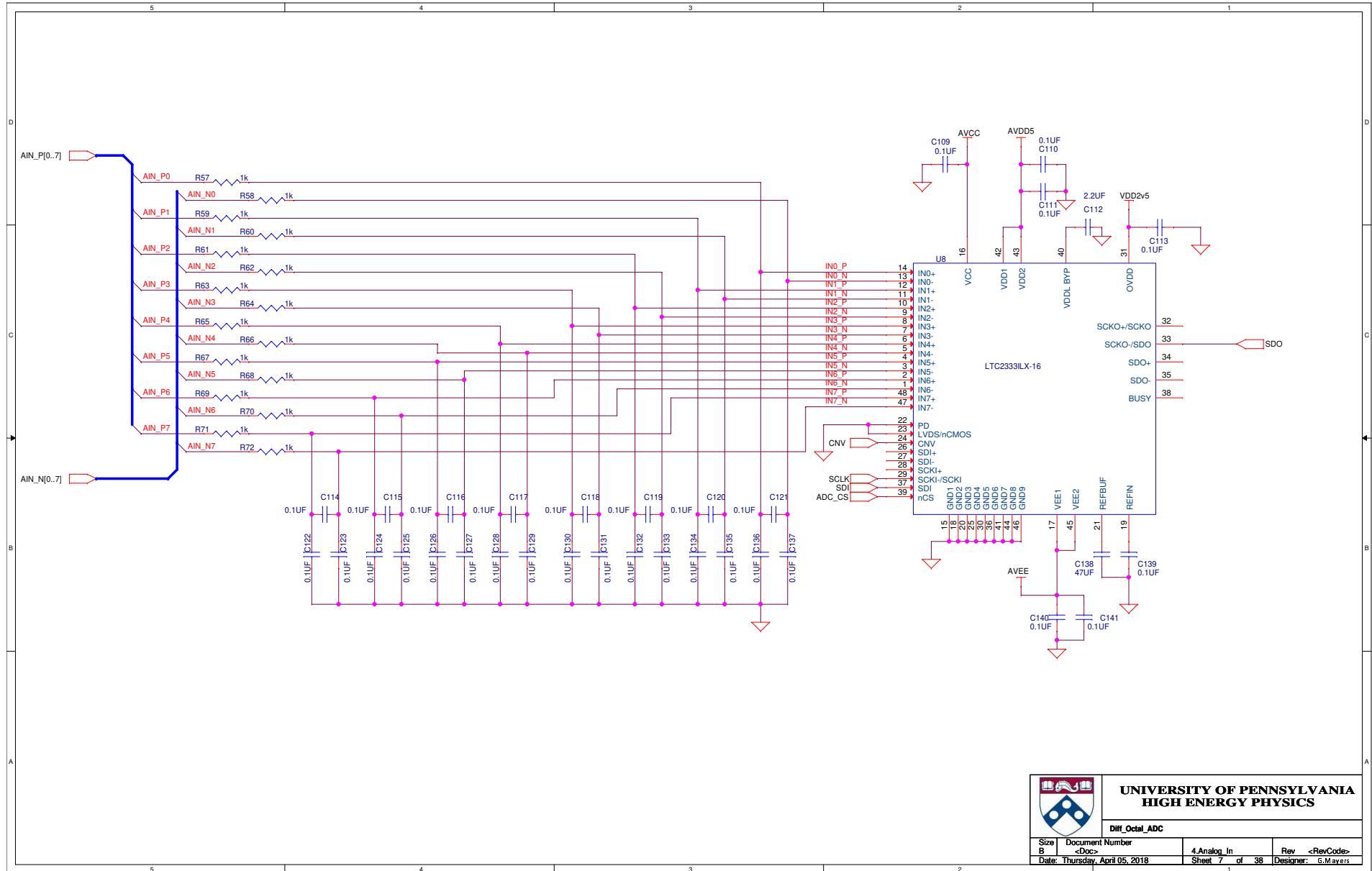


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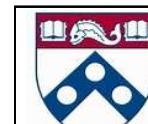
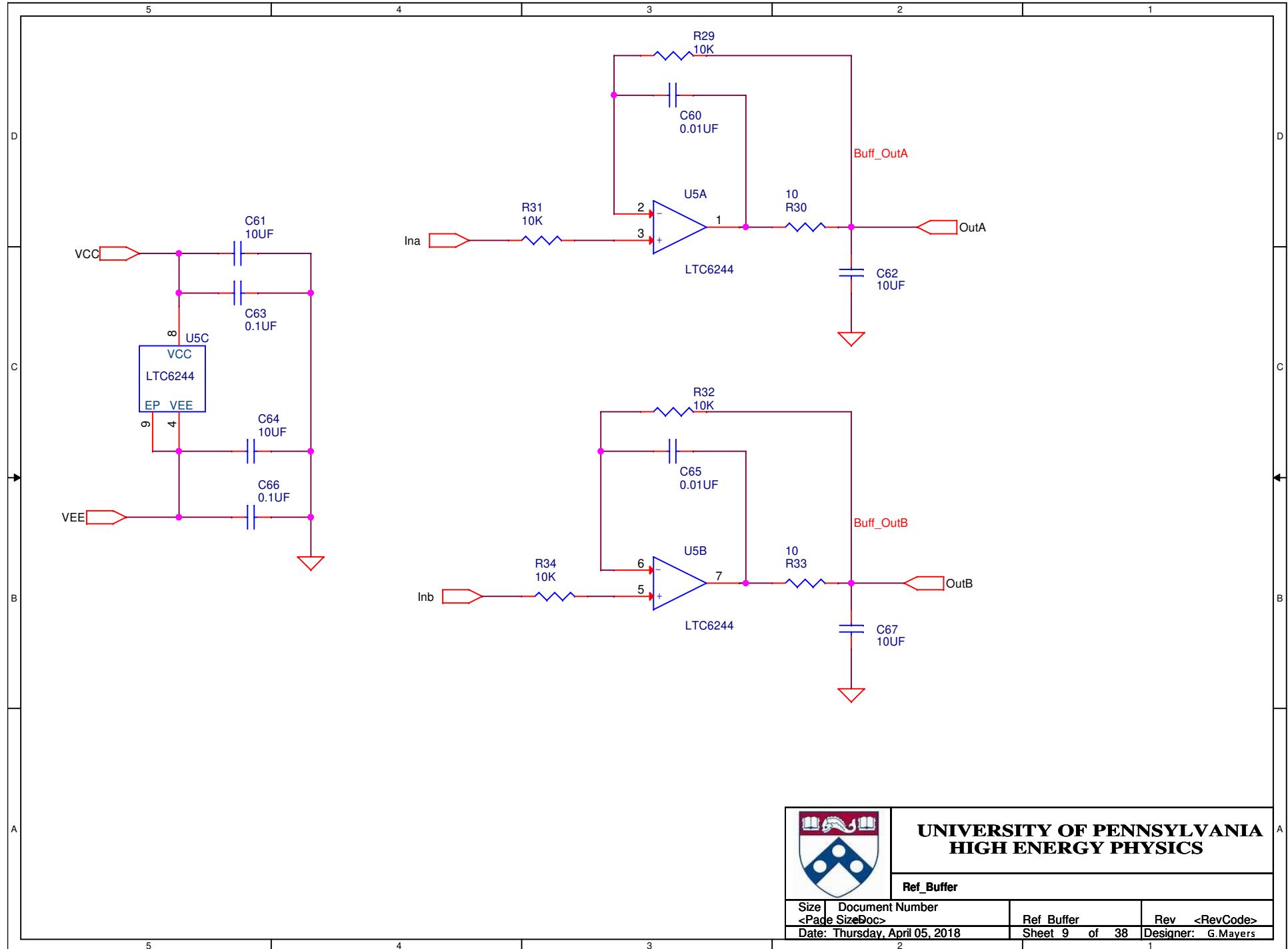


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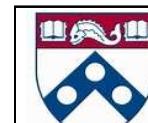
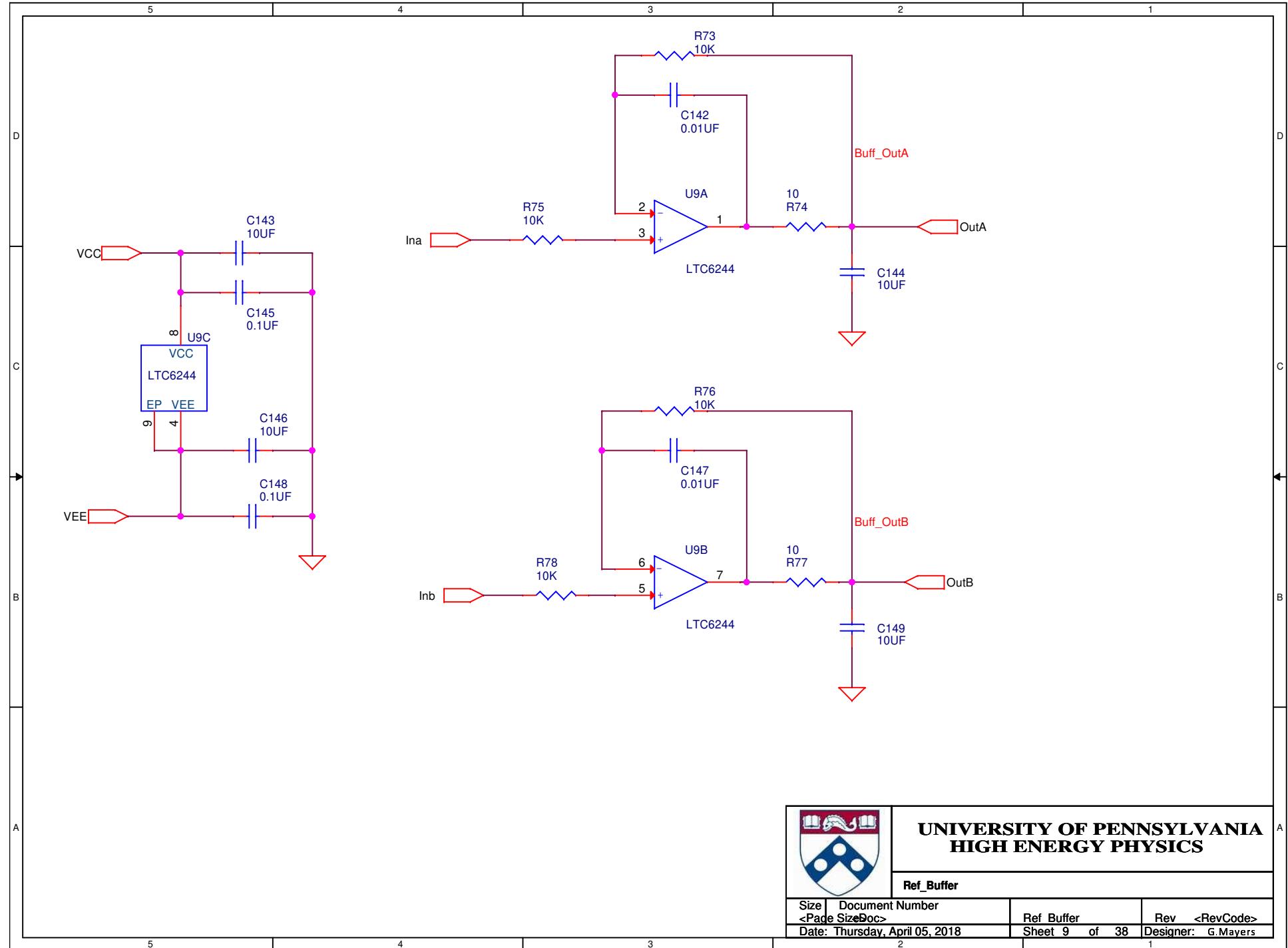
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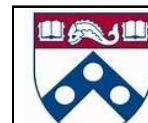
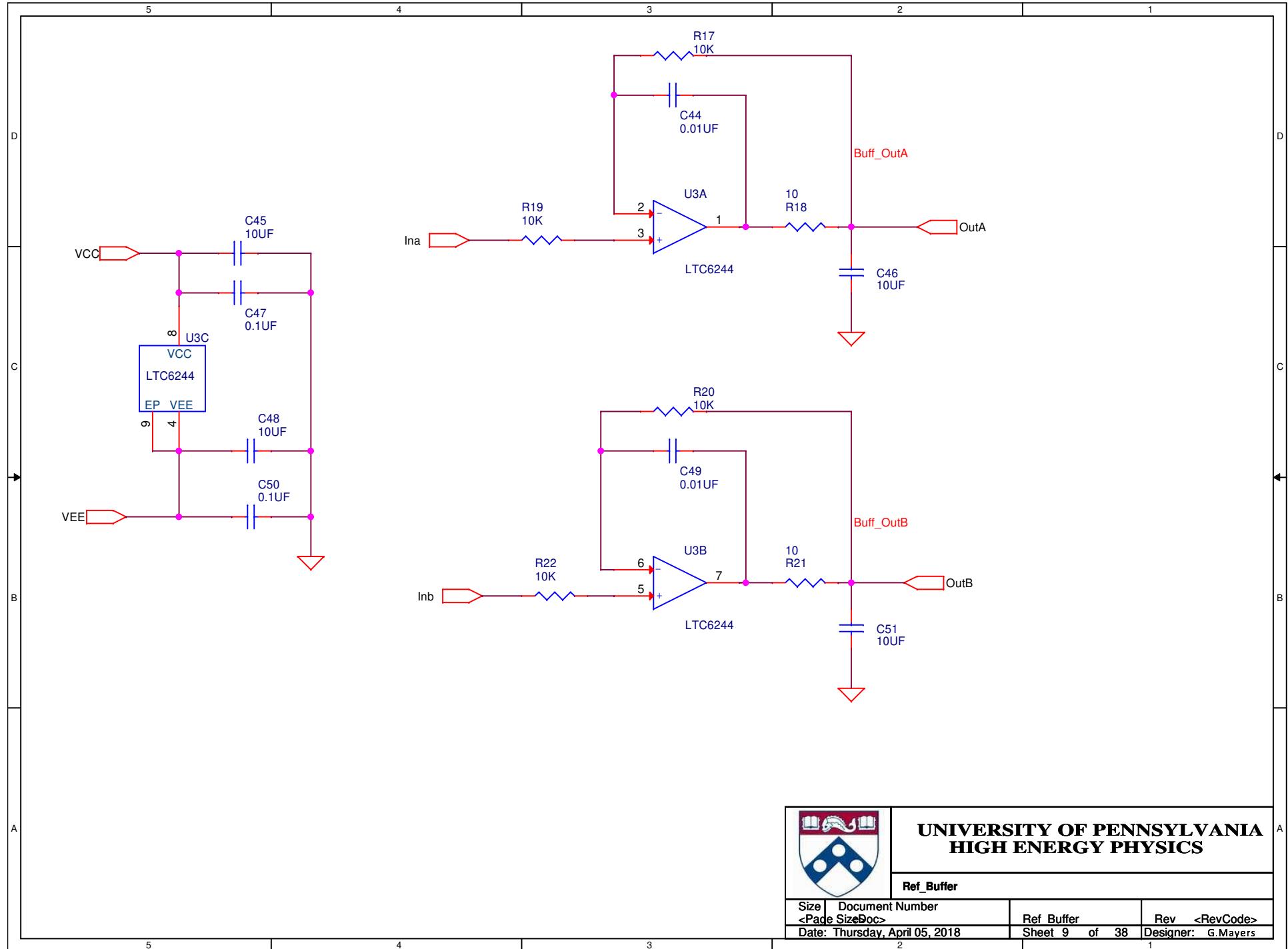
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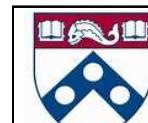
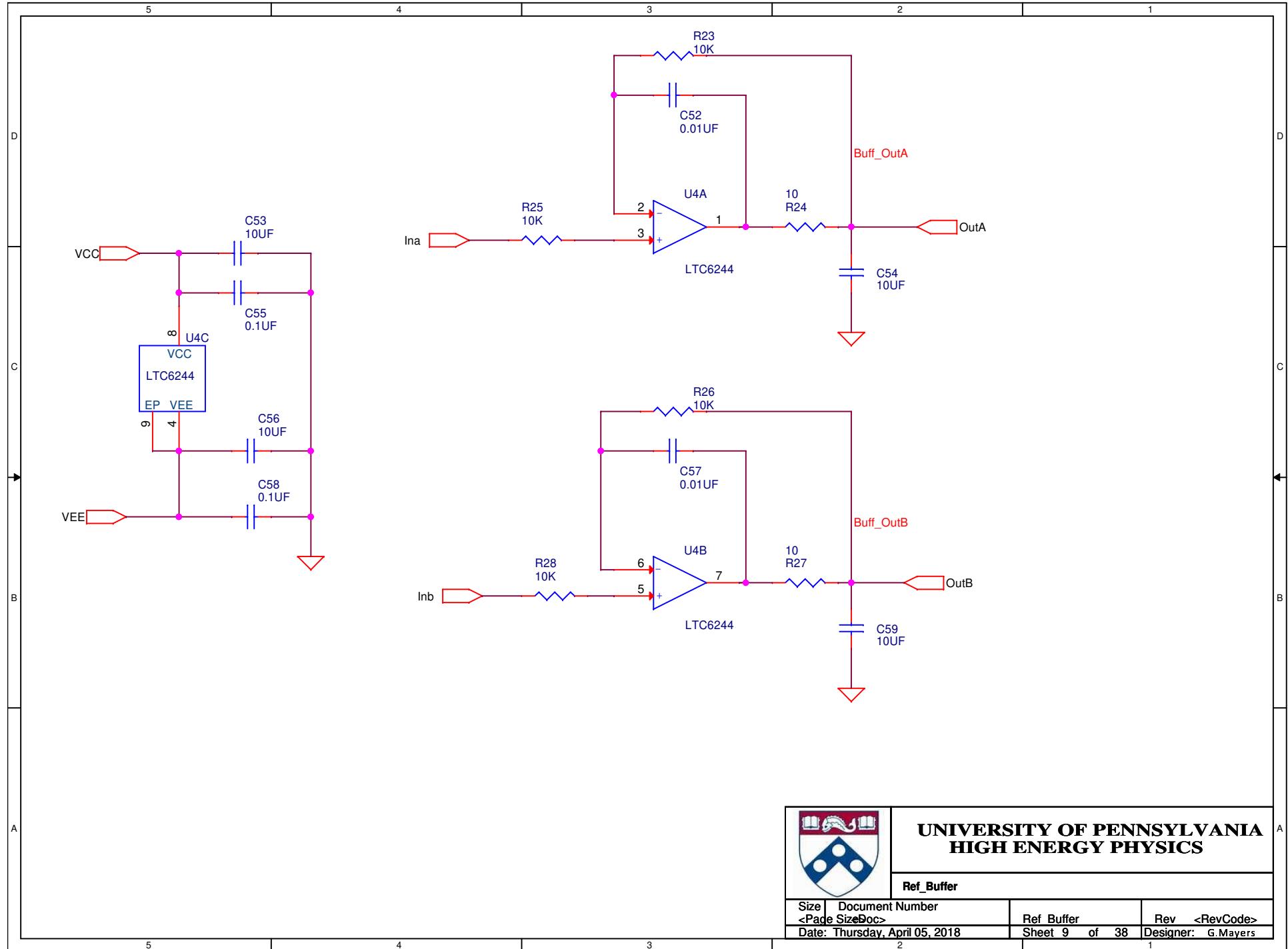
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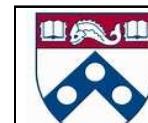
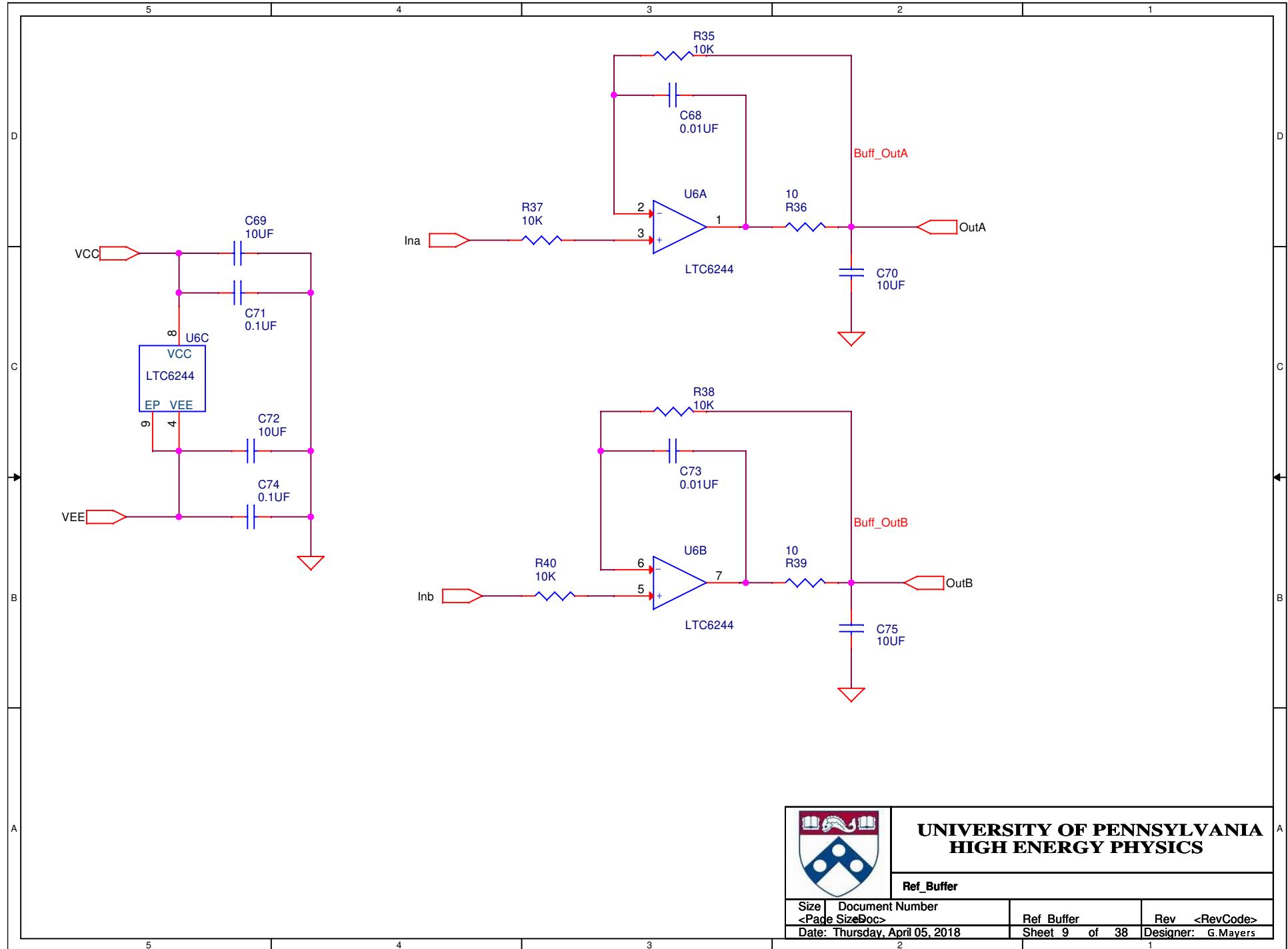


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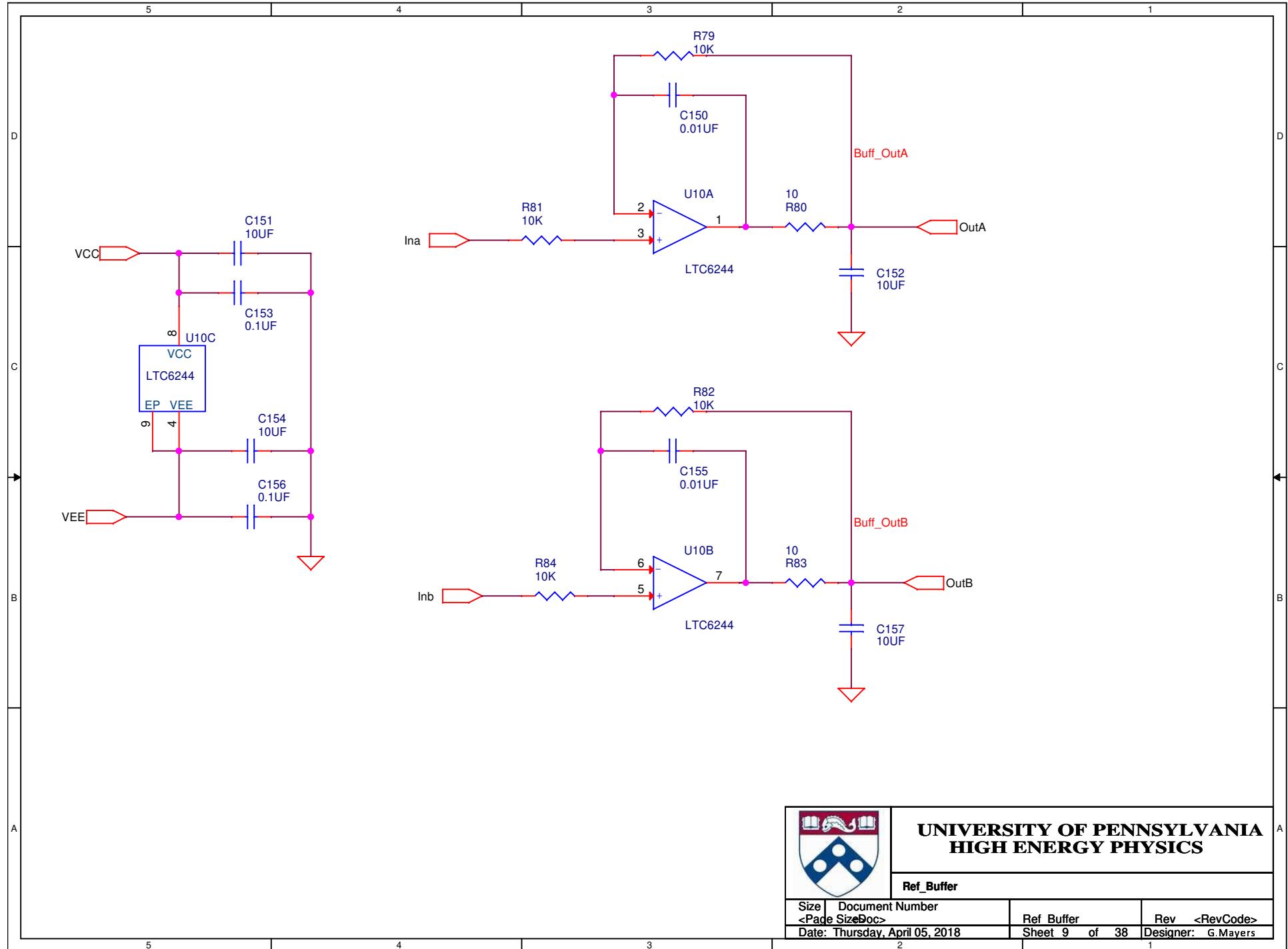
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