AMACv2 Functional Verification Test Plan

July 19, 2018

Abstract

This document enumerates features to be tested, and defines test procedures for single-chip verification of AMACv2. This document will be augmented to act as a test record. System-level and production test procedures are outside the scope of this document.

Revision History

Revision	Date	Author(s)	Description
0.0	19 July 2018	P: A.N.	Initial outline

Contents

1 Related Documents **4**

2 AMACv2 Feature Test List **5**
2.1 Current Consumption . . . 5
2.2 Digital Pins . . . 5
2.2.1 ROPG (ring oscillator power good) . . . 5
2.2.2 LAM ("look-at-me") . . . 5
2.2.3 LDx0en, LDy0en, LDx1en, LDy1en, LDx2en, LDy2en . . . 5
2.2.4 ResetB . . . 5
2.2.5 SSSHx, SSSHy . . . 5
2.2.6 HrstBx, HrstBy . . . 5
2.2.7 DCDCen . . . 5
2.2.8 DCDCadj / GPO . . . 6
2.2.9 ID[4:0] . . . 6
2.2.10 OFin . . . 6
2.2.11 OFout . . . 6
2.2.12 GPI . . . 6
2.2.13 PGOOD . . . 6
2.3 Analog Pins . . . 6
2.3.1 ClkOut . . . 6
2.3.2 AMBG600 . . . 7
2.3.3 AMBG900 . . . 7
2.3.4 VDDREG1/2 . . . 7
2.3.5 Shuntx, Shunty . . . 7
2.3.6 CALx, CALy . . . 7
2.3.7 NTCxp/n, NTCyp/n, NTCpbp/n . . . 7
2.3.8 Hrefx, Hrefy . . . 7
2.3.9 PTAT . . . 7
2.3.10 Cur10Vp/n . . . 7
2.3.11 Cur1Vp/n . . . 7
2.3.12 DCDCin . . . 7
2.3.13 HVret1/2 . . . 7
2.3.14 HVref1/2 . . . 7
2.3.15 CAL . . . 7
2.4 HVOsc0/1/2/3 . . . 7
2.5 Power Pins . . . 7
2.5.1 VDDLR1/2 . . . 7
2.5.2 VDCDC1/2 . . . 7
2.5.3 VDDHI . . . 8
2.6 Communications Pins . . . 8
2.6.1 CMDinP/N . . . 8
2.6.2 CMDoutP/N . . . 8
2.7 AM Channel Tests . . . 9
2.7.1 DCDC converter output (scaled) . . . 9
2.7.2 Linear regulator output (scaled) . . . 9
2.7.3 DCDC converter input (scaled) . . . 9

2.7.4 Regulated VDD . . . 9
2.7.5 AMBG600/AMBG900 . . . 9
2.7.6 CAL from EoS . . . 9
2.7.7 CALx/y from DAC . . . 9
2.7.8 Shuntx/y from DAC . . . 9
2.7.9 NTCx/y/pb . . . 9
2.7.10 Hrefx/y from hybrids . . . 9
2.7.11 DCDC input current . . . 9
2.7.12 DCDC output current . . . 9
2.7.13 HV current return monitor . . . 9
2.7.14 die temp (PTAT) . . . 9
2.7.15 MUX functionality . . . 9
2.8 DAC Functionality . . . 9
2.9 AM functionality . . . 10
2.9.1 Enable/disable . . . 10
2.9.2 Default value . . . 10
2.9.3 Overflow value . . . 10
2.9.4 Full 10-bit range 0-1023 . . . 10
2.9.5 Values below zero . . . 10
2.9.6 Analog noise injection / flag limit tolerance, dither, ramp latch time . . . 10
2.10 Digital Functions . . . 10
2.10.1 Resets . . . 10
2.10.2 WARN . . . 10
2.10.3 Flags . . . 10
2.10.4 Interlock . . . 10
2.11 Endeavour . . . 10
2.12 Parametric Tests . . . 11
2.13 Irradiation Tests . . . 11

3 AMACv2 Test Plan 12
3.1 Power-up . . . 12
3.2 Digital Functional Tests . . . 12
3.3 Analog Functional Tests . . . 12
3.4 Radiation Tolerance . . . 12
3.4.1 TID . . . 12
3.4.2 SEU . . . 12

4 AMACv2 Test Record 13

1 Related Documents

The main SVN repository for code and documentation is located at: https://svnweb.cern.ch/cern/wsvn/itkstrasic/AMACv2/. Please refer to doc/README.txt for the latest version of the specification, as well as schematics, register map, Verilog, and verification code for the November 2017 MPW ASIC.

2 AMACv2 Feature Test List

2.1 Current Consumption

Measure before configuration, and after various configurations. Gather statistics from several single-chip test cards.

2.2 Digital Pins

2.2.1 ROPG (ring oscillator power good)

Output. Confirm pin goes logic high approximately 250µs after power is applied.

2.2.2 LAM ("look-at-me")

Output. Confirm that LAM pulse is generated upon interlock if enabled in registers 60-25, bit 16. Confirm multiple LAM pulses are generated upon successive interlocks that are not cleared.

2.2.3 LDx0en, LDy0en, LDx1en, LDy1en, LDx2en, LDy2en

Outputs. Confirm pins go logic high when corresponding bits in registers 40/41 are written. Confirm pins go logic low after enabled if corresponding interlock occurs.

2.2.4 ResetB

Input. Confirm that logic low pulse resets AMACv2 to default condition (all registers to default values, additional SETID required).

2.2.5 SSSHx, SSSHy

Inputs. Confirm that logic high pulse resets Endeavour communications block (register states persist, additional SETID required). Validate deglitching.

2.2.6 HrstBx, HrstBy

Outputs. Confirm pins go logic high when corresponding bits in registers 46/47 are written.

2.2.7 DCDCen

Output. Confirm pin goes logic high when registers 42/43, bit 0 are written.

2.2.8 DCDCadj / GPO

Outputs. Confirm pins go logic high when corresponding bits in register 42/43 are written.

2.2.9 ID[4:0]

Inputs. Confirm bits can read in serial number register 31.

2.2.10 OFin

Input. Confirm that DCDCen is disables when OFin is asserted. Validate deglitching.

2.2.11 OFout

Output. Confirm pin is goes high when registers 46/47, bit 0 are written.

2.2.12 GPI

Input. Confirm pin state can be read in status register 0, bit 12.

2.2.13 PGOOD

Input. Confirm pin state can be read in status register 0, bit 8. Confirm DCDCen cannot be enabled when PGOOD is logic high, if and only if this functionality is enabled by setting registers 50/51, bit 8.

2.3 Analog Pins

2.3.1 ClkOut

Output. Confirm 40MHz nominally.

136 #### 2.3.2 AMBG600

137 #### 2.3.3 AMBG900

138 #### 2.3.4 VDDREG1/2

139 #### 2.3.5 Shuntx, Shunty

140 #### 2.3.6 CALx, CALy

141 #### 2.3.7 NTCxp/n, NTCyp/n, NTCpbp/n

142 #### 2.3.8 Hrefx, Hrefy

143 #### 2.3.9 PTAT

144 #### 2.3.10 Cur10Vp/n

145 #### 2.3.11 Cur1Vp/n

146 #### 2.3.12 DCDCin

147 #### 2.3.13 HVret1/2

148 #### 2.3.14 HVref1/2

149 #### 2.3.15 CAL

150 ### 2.4 HVOsc0/1/2/3

151 Output.

152 - Measure HV oscillator drive capability (charge pump to voltage attained)
153 - Measure 4 frequency settings
154 - Confirm enable/disable

155 ### 2.5 Power Pins

156 #### 2.5.1 VDDLR1/2

157 Confirm operational ranges. Confirm PoR threshold.

158 #### 2.5.2 VDCDC1/2

159 Switch AMAC power from linear regulator to DCDC converter power.

2.5.3 VDDHI

2.6 Communications Pins

2.6.1 CMDinP/N

Input. Measure voltage at receive side.

2.6.2 CMDoutP/N

Output.

- Measure current drive
- Measure common mode of driver
- Confirm high impedance when not transmitting (475ns window for switch-on)

2.7 AM Channel Tests

2.7.1 DCDC converter output (scaled)

2.7.2 Linear regulator output (scaled)

2.7.3 DCDC converter input (scaled)

2.7.4 Regulated VDD

2.7.5 AMBG600/AMBG900

2.7.6 CAL from EoS

2.7.7 CALx/y from DAC

2.7.8 Shuntx/y from DAC

2.7.9 NTCx/y/pb

2.7.10 Hrefx/y from hybrids

2.7.11 DCDC input current

2.7.12 DCDC output current

2.7.13 HV current return monitor

2.7.14 die temp (PTAT)

2.7.15 MUX functionality

2.8 DAC Functionality

TDB: bais bits, dynamic range.

2.9 AM functionality

2.9.1 Enable/disable

2.9.2 Default value

2.9.3 Overflow value

2.9.4 Full 10-bit range 0-1023

2.9.5 Values below zero

2.9.6 Analog noise injection / flag limit tolerance, dither, ramp latch time

2.10 Digital Functions

2.10.1 Resets

- Commanded hard reset
- Commanded soft reset

2.10.2 WARN

2.10.3 Flags

- Flag limit setting
- Synthetic flags
- Flag latch
- Flag clear
- Flag validation: 2,3,4 ramp cycles
- Edge cases: value below zero, comparator never fires
- Confirm all flags mapped to corresponding limit registers

2.10.4 Interlock

- Enable/disable/clear
- Confirm all states of state machine are exercised
- Confirm all interlocks are mapped to corresponding channels, high and low limit
- More than one LDO interlock programmed
- Synthetc flag interlocks

2.11 Endeavour

- Invalid commands: headers, COMMID, packet size, bitwidth, EoS frequency tolerance
- Pseudorandom data
- Check sequence numbers
- Check CRC validation

- Violate SETID quiescent time
- Send command while busy
- PADID and eFuse matching, wildcard IDs
- Effect of hard/soft/SSSH reset
- R/W all registers
- READNEXT

2.12 Parametric Tests

2.13 Irradiation Tests

Test system infrastructure functionality to be confirmed (long cable tests for TID tests, test board temperature monitoring and control, etc.).

3 AMACv2 Test Plan

3.1 Power-up

This power-up sequence in not intended to be the default use case. Single-chip bringup only.

- Apply VDDLR
- Measure AMACv2 current before configuration
- Measure AMACv2 VDDREG, AMBG600, AMBG900. Gather statistics on multiple MPW chips.
- Measure ROPG pin
- Measure RO frequency on RO pin
- Send SETID
- Read PADID from serial number register 31
- PGODD pin: read status register 0
- Calibrate RO, AMBG600/AMBG900/VDDREG, AM bandgap, record calibration values (histograms)
- Read a AM register and see the default value
- Calibrate AM: zero cal, ramp slope, BG fine tune
- Measure current after config
- Put voltage on CAL and read back
- Test other channels
- DAC calibration, compare with AM measurement

3.2 Digital Functional Tests

All detailed procedures for test items above to be specified here.

3.3 Analog Functional Tests

TBD: CAL, Hrefx/y: input offset variation as a function of voltage, linearity

3.4 Radiation Tolerance

3.4.1 TID

3.4.2 SEU

4 AMACv2 Test Record

Results of above tests to be recorded here.