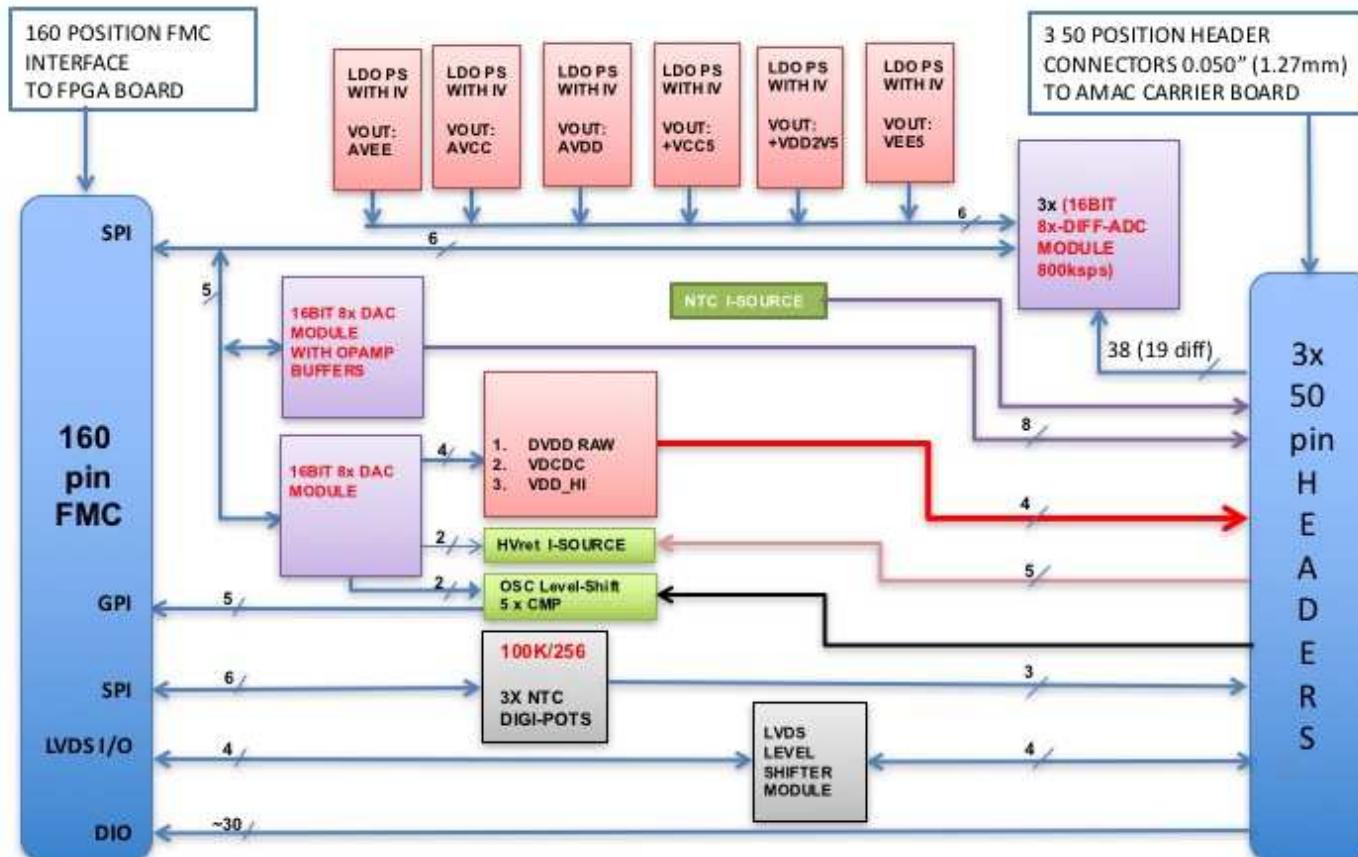


AMAC V2 TEST & CONTROL BLOCK DIAGRAM



4/27/18

Godwin Mayers



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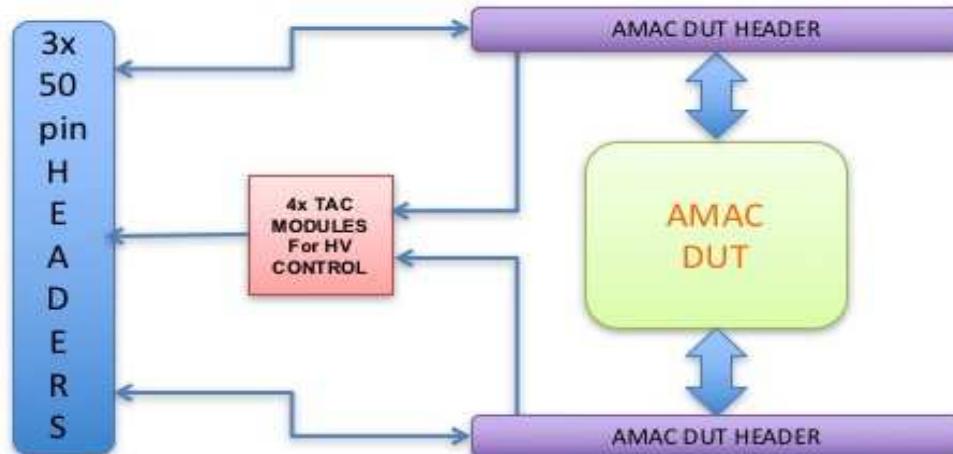
ATCB Block Diagrams

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AMAC CARRIER AND DUT BOARDS

D
3 50 POSITION HEADER
CONNECTOR 0.050(1.27mm)
TO AMAC TEST & CONTROL
BOARD



3/12/18

Godwin Mayers

2



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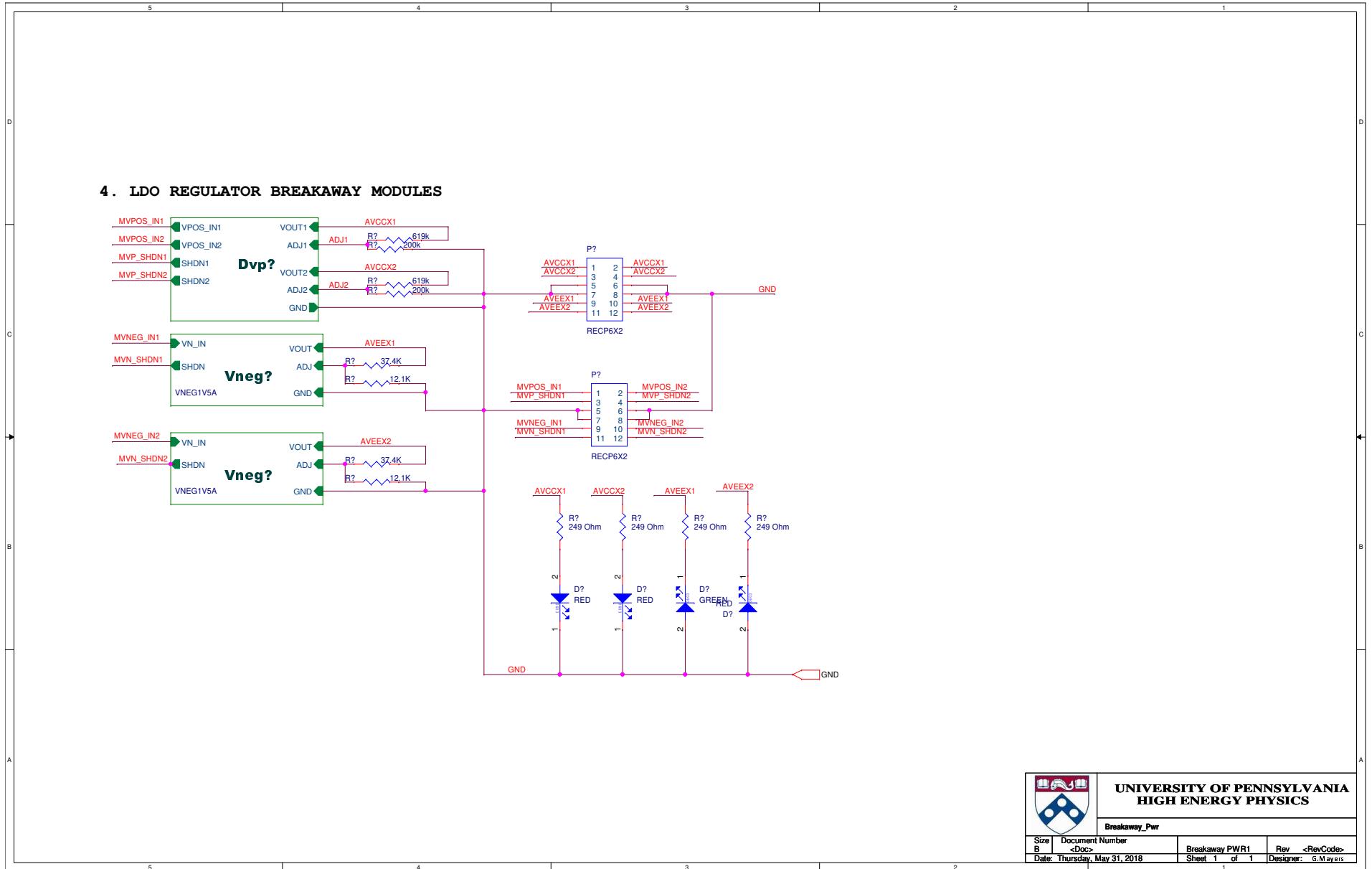
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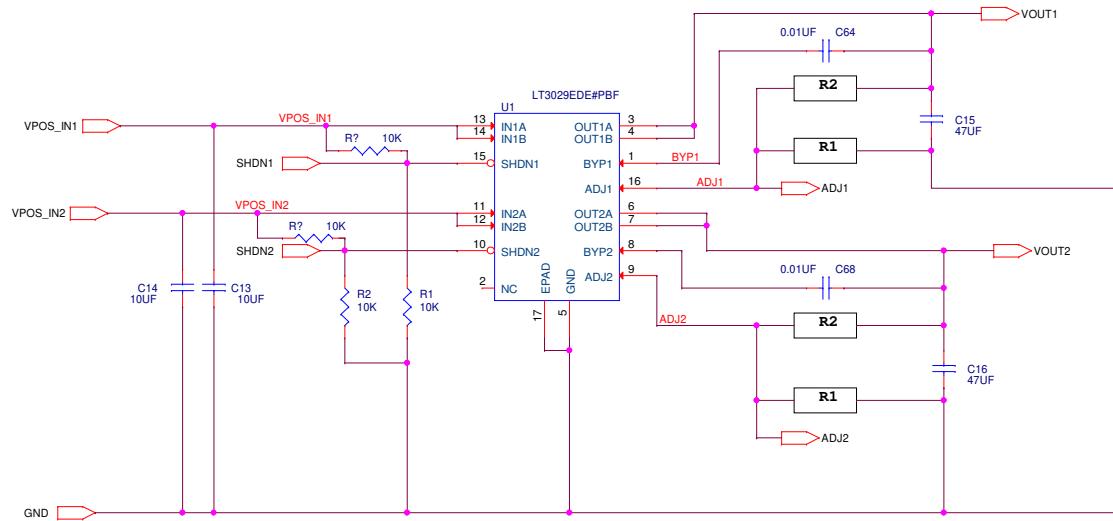
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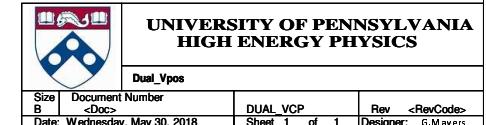


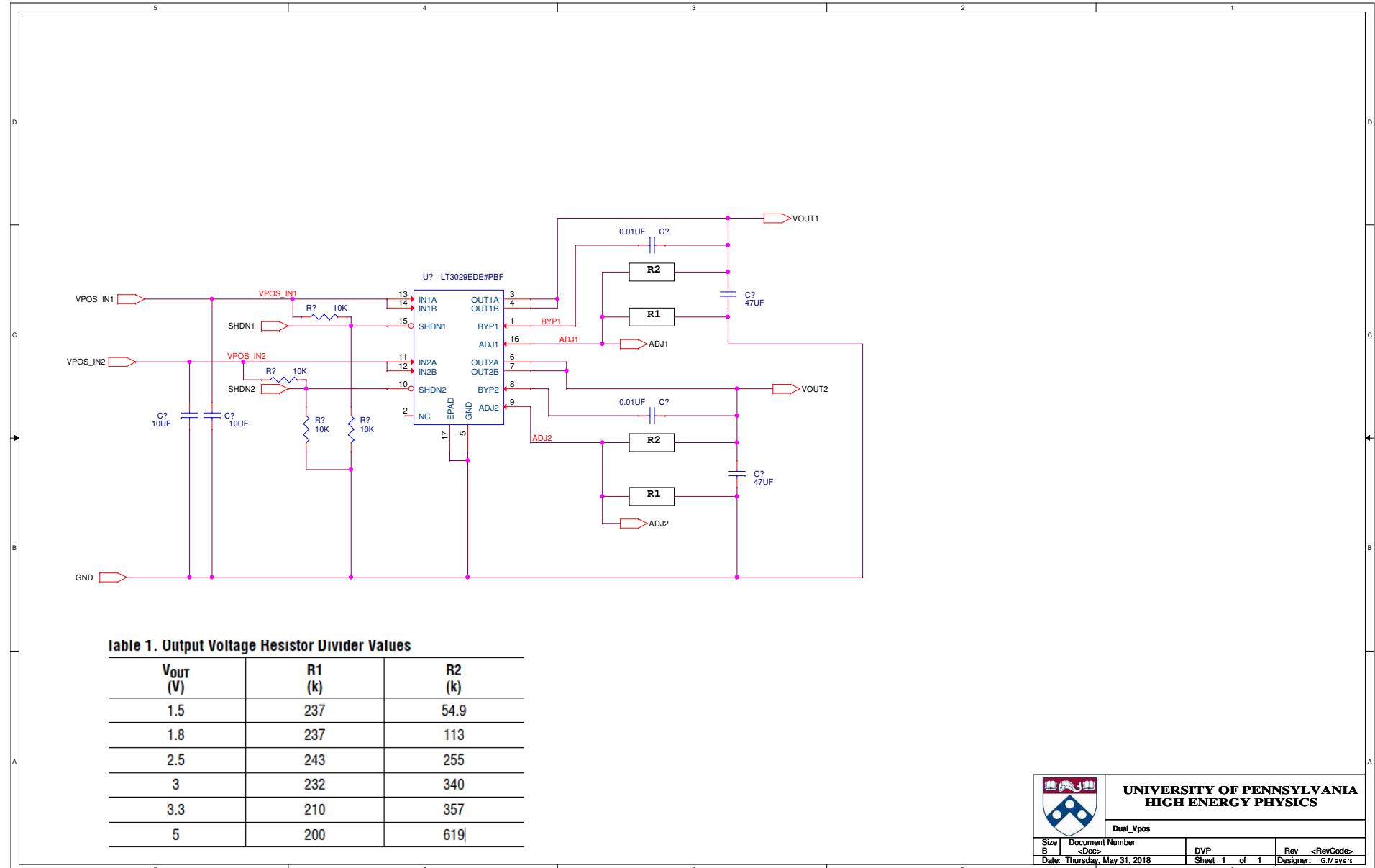


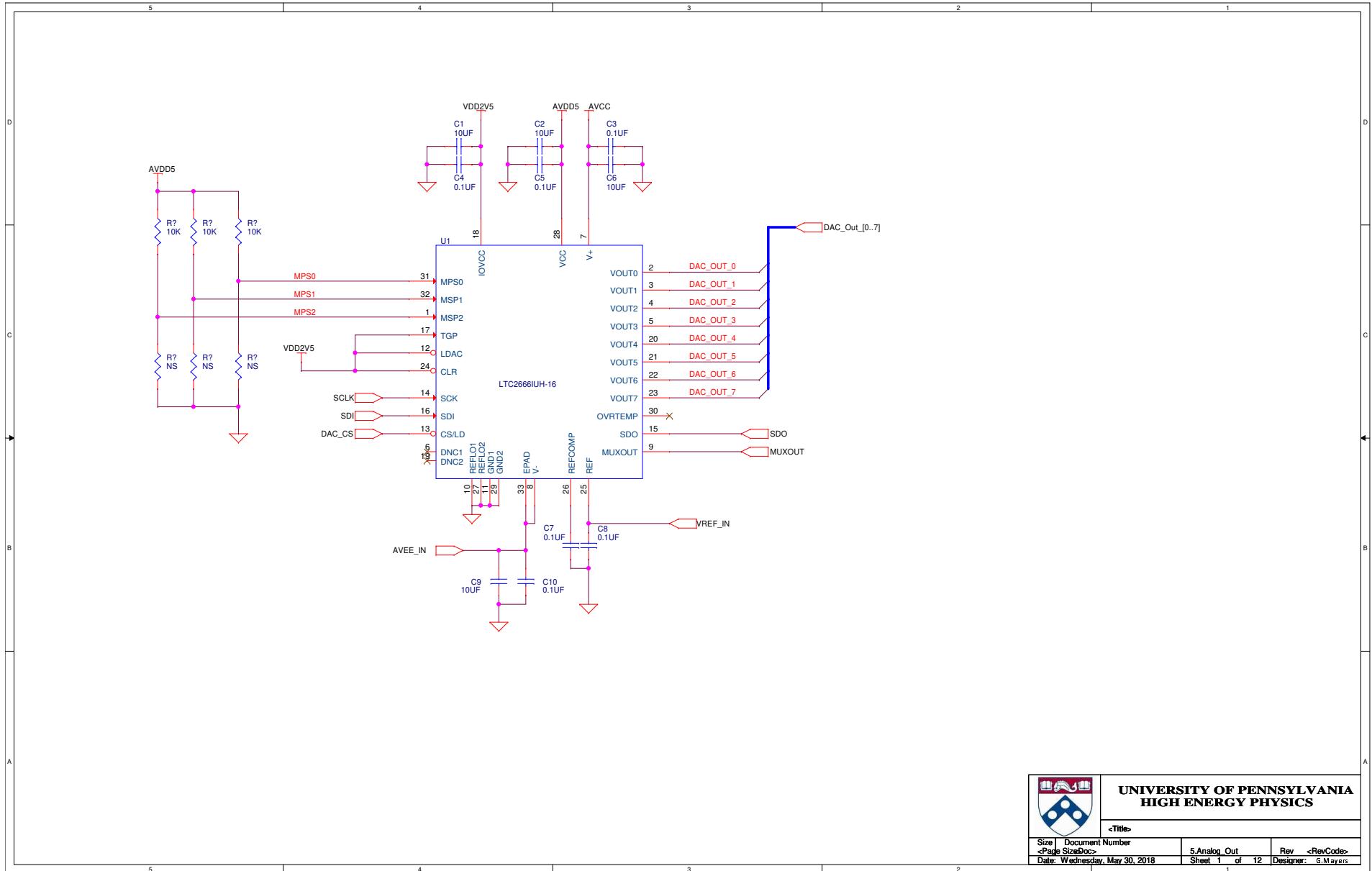
R1 and R2 blocks only serve as place holders when referencing table below
and show where external resistor fit in the circuit.

Table 1. Output Voltage Resistor Divider Values

V _{OUT} (V)	R1 (k)	R2 (k)
1.5	237	54.9
1.8	237	113
2.5	243	255
3	232	340
3.3	210	357
5	200	619







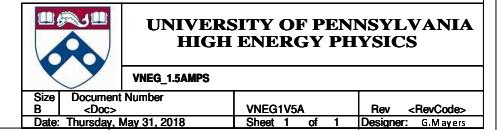
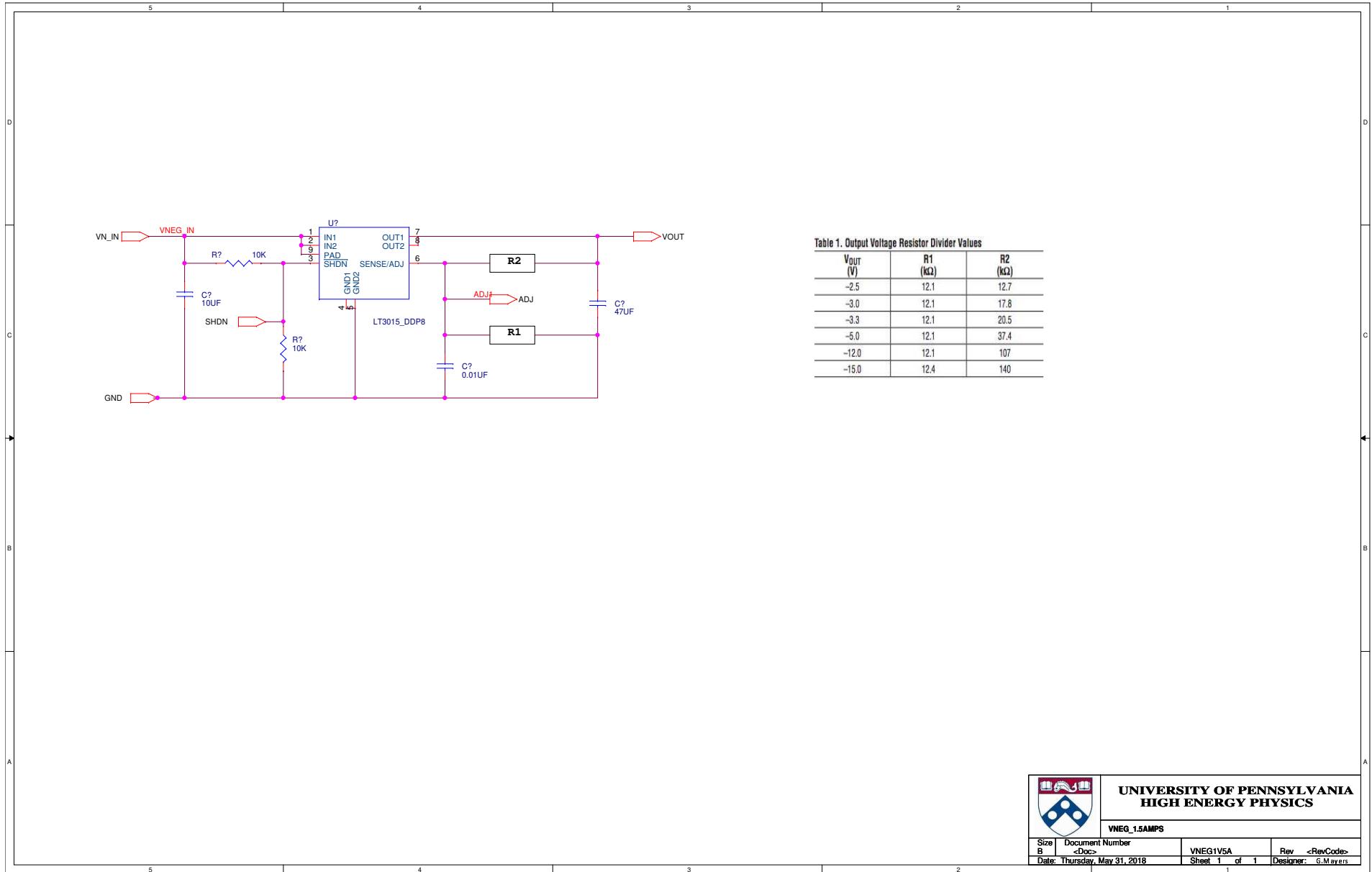
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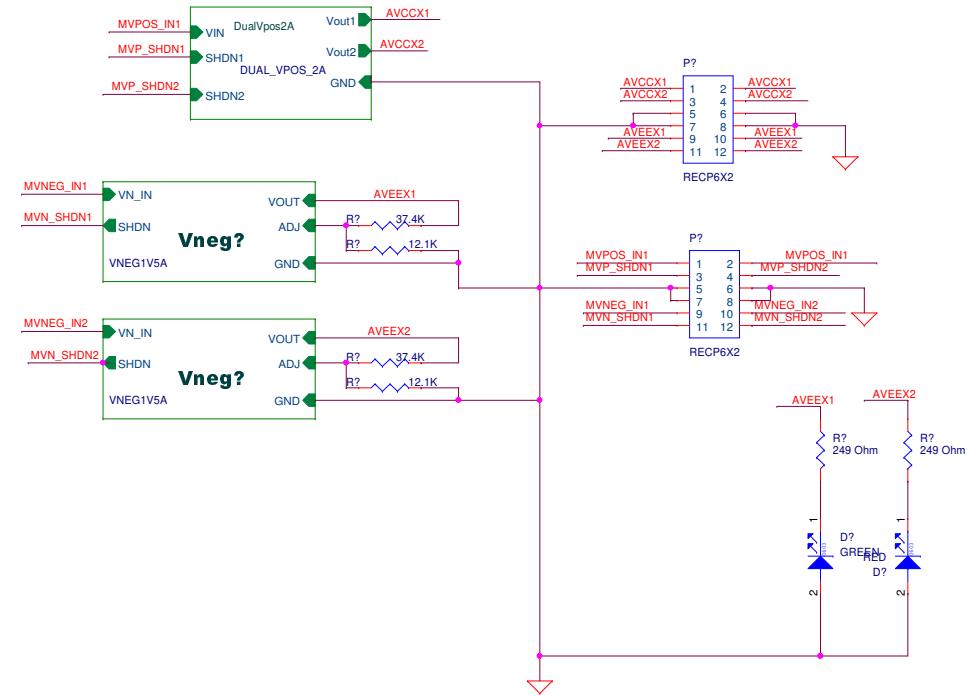
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Designer: G.Mayers



4. LDO REGULATOR BREAKAWAY MODULES



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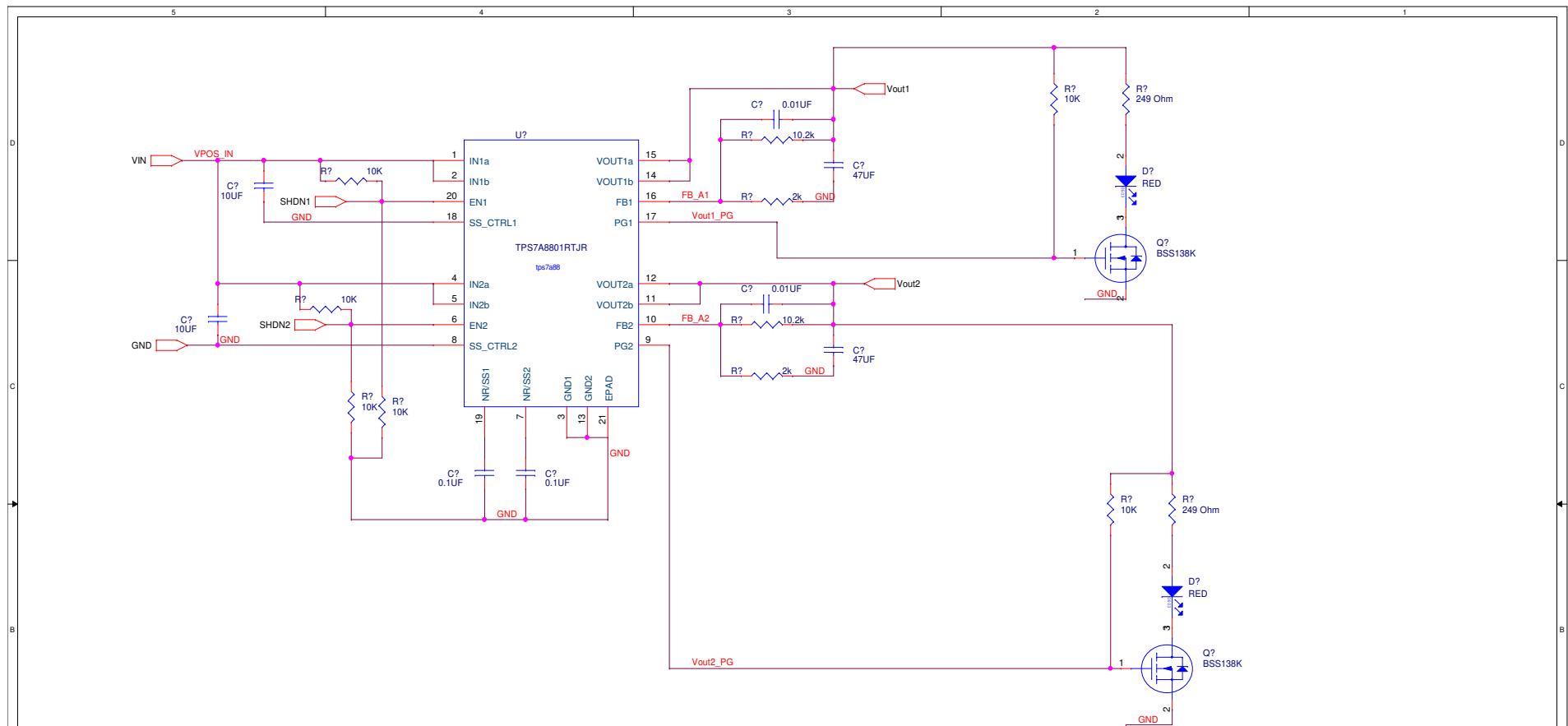
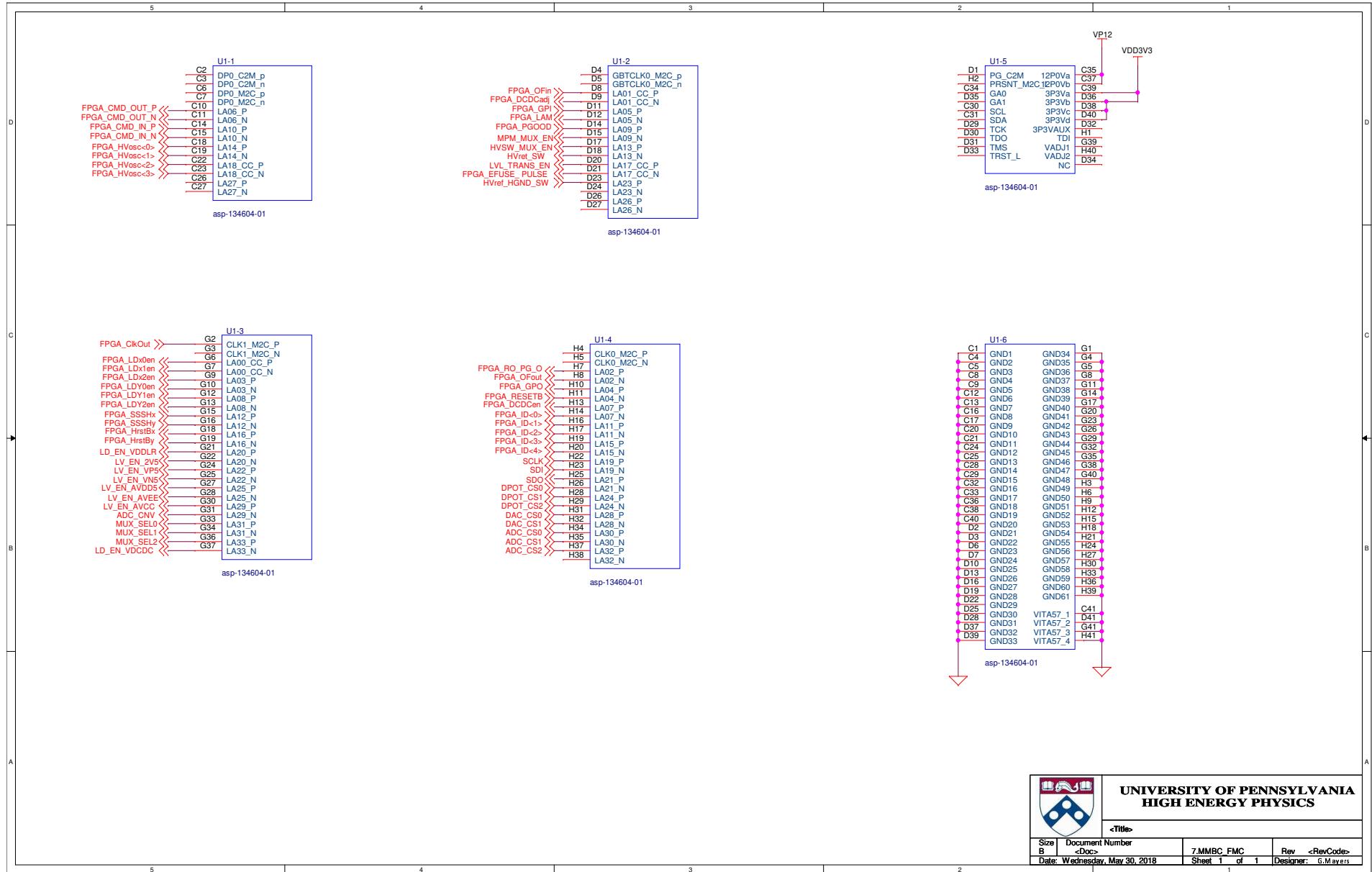
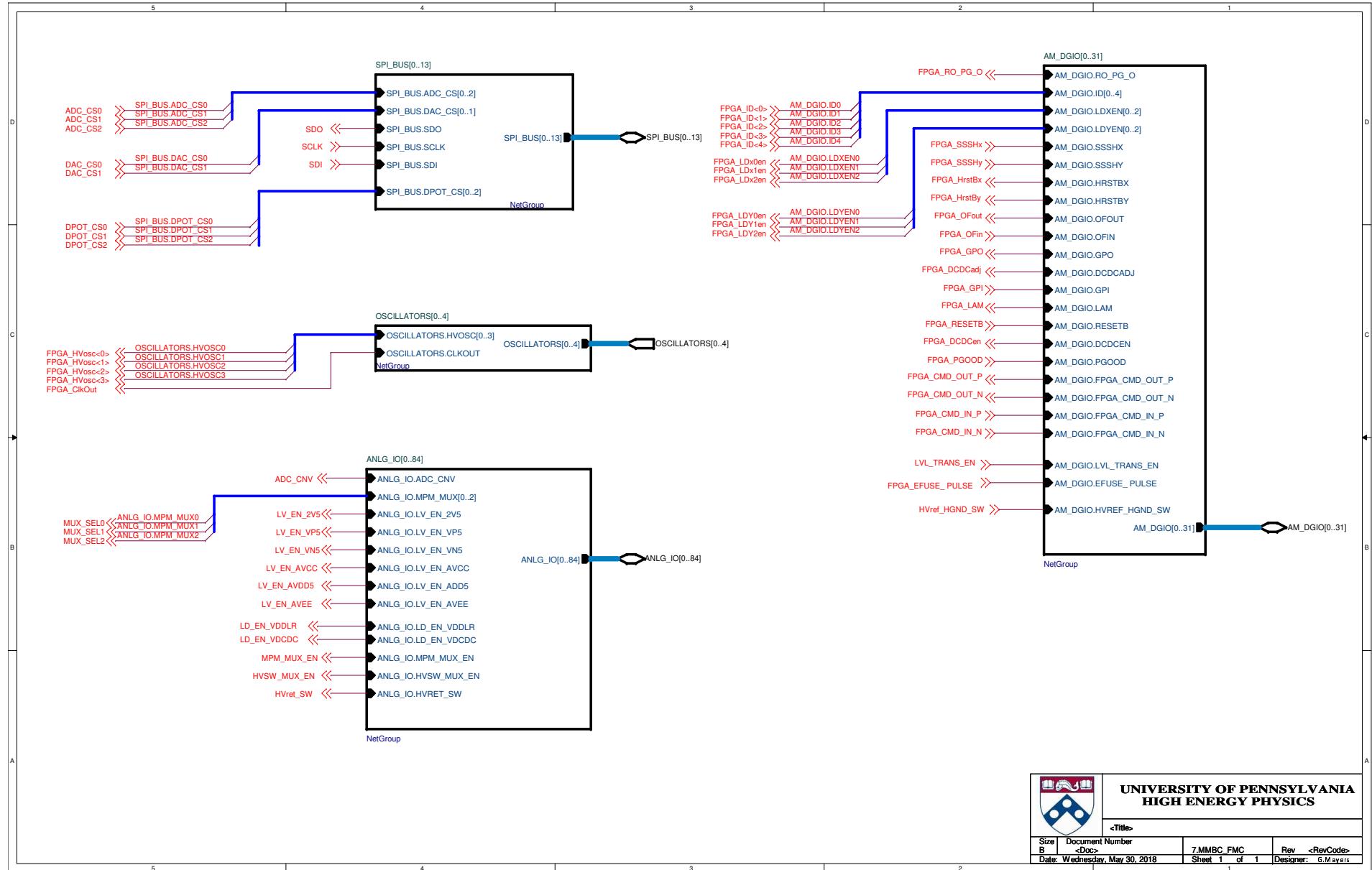
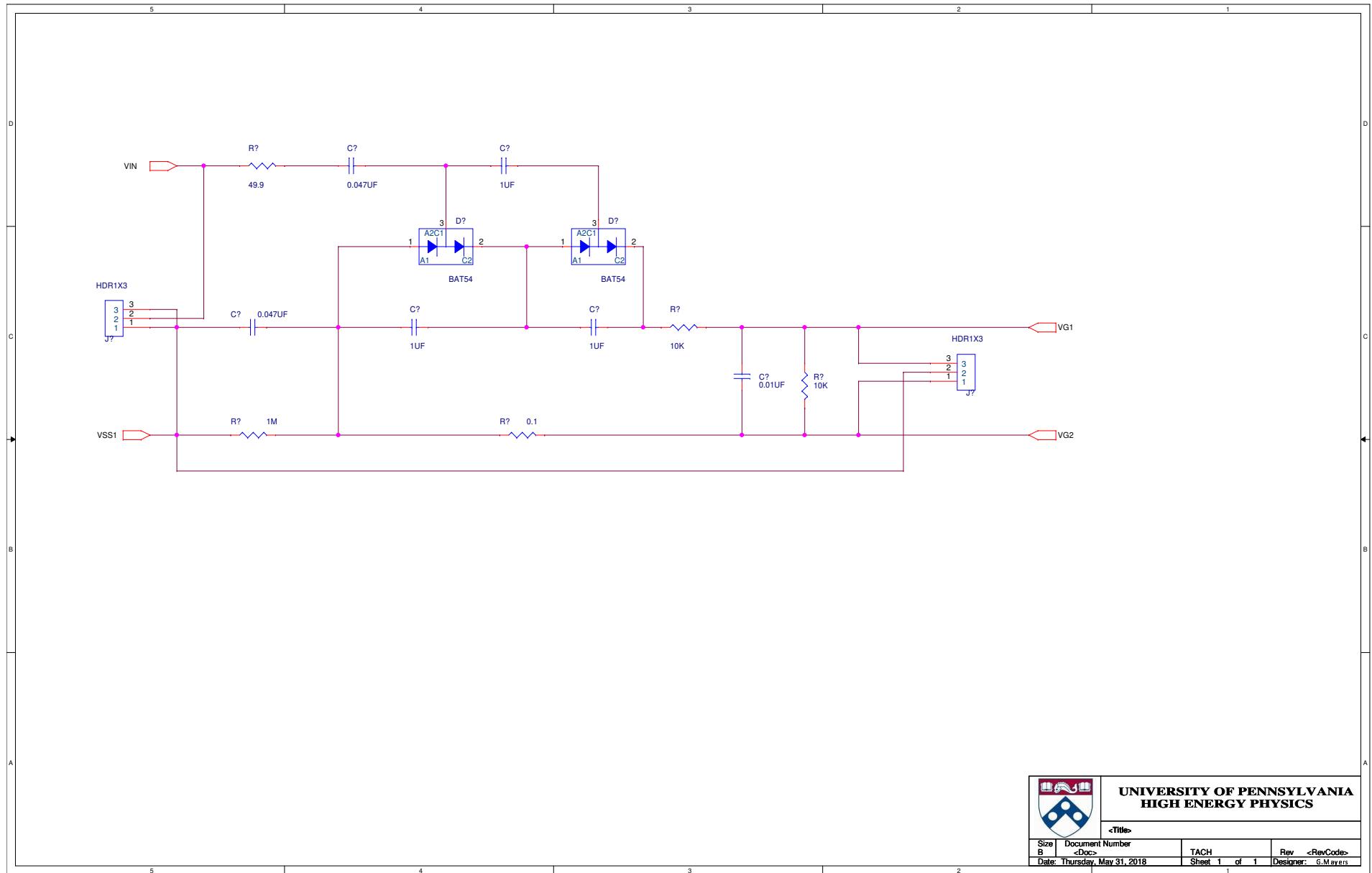


Table 2. Recommended Feedback-Resistor Values

V _{OUT(TARGET)} (V)	FEEDBACK RESISTOR VALUES ⁽¹⁾	
	R ₁ , R ₃ (kΩ)	R ₂ , R ₄ (kΩ)
0.8	Short	Open
1.00	2.55	10.2
1.20	5.9	11.8
1.50	9.31	10.7
1.80	1.87	1.5
1.90	15.8	11.5
2.50	2.43	1.15
3.00	3.16	1.15
3.30	3.57	1.15
5.00	10.5	2

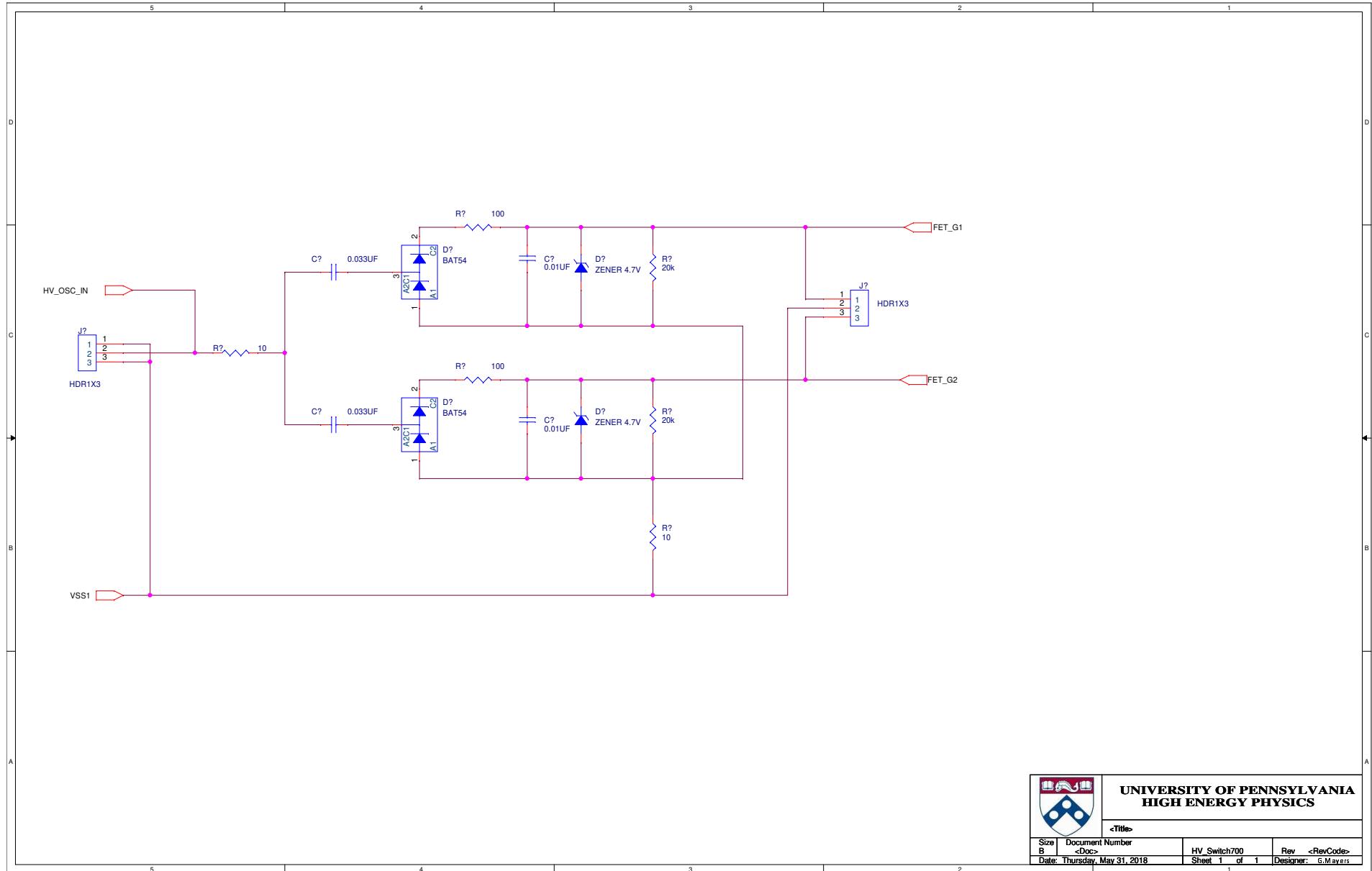






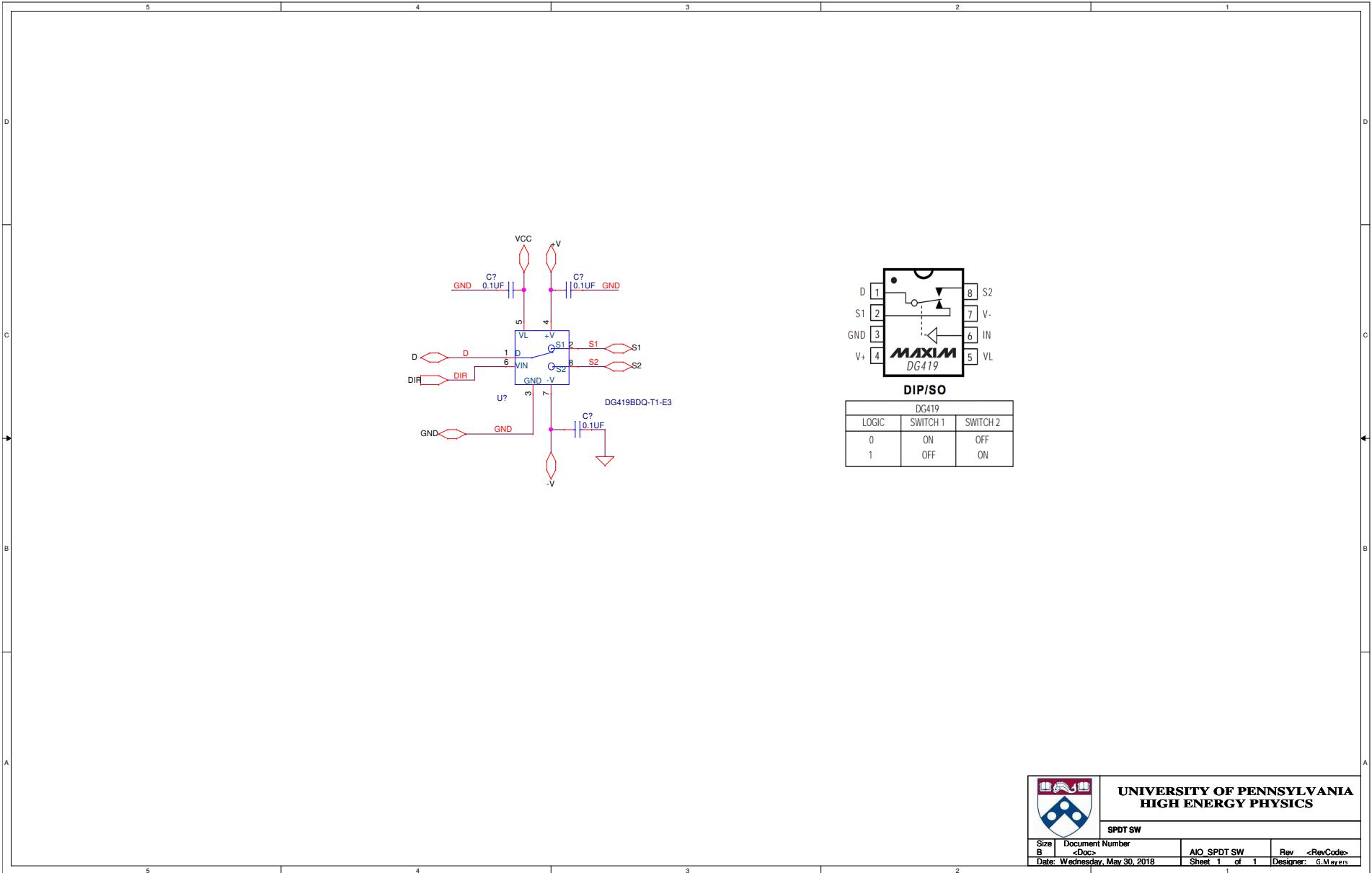
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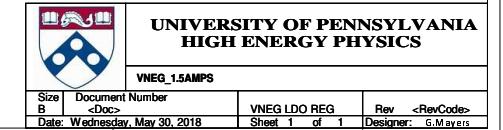
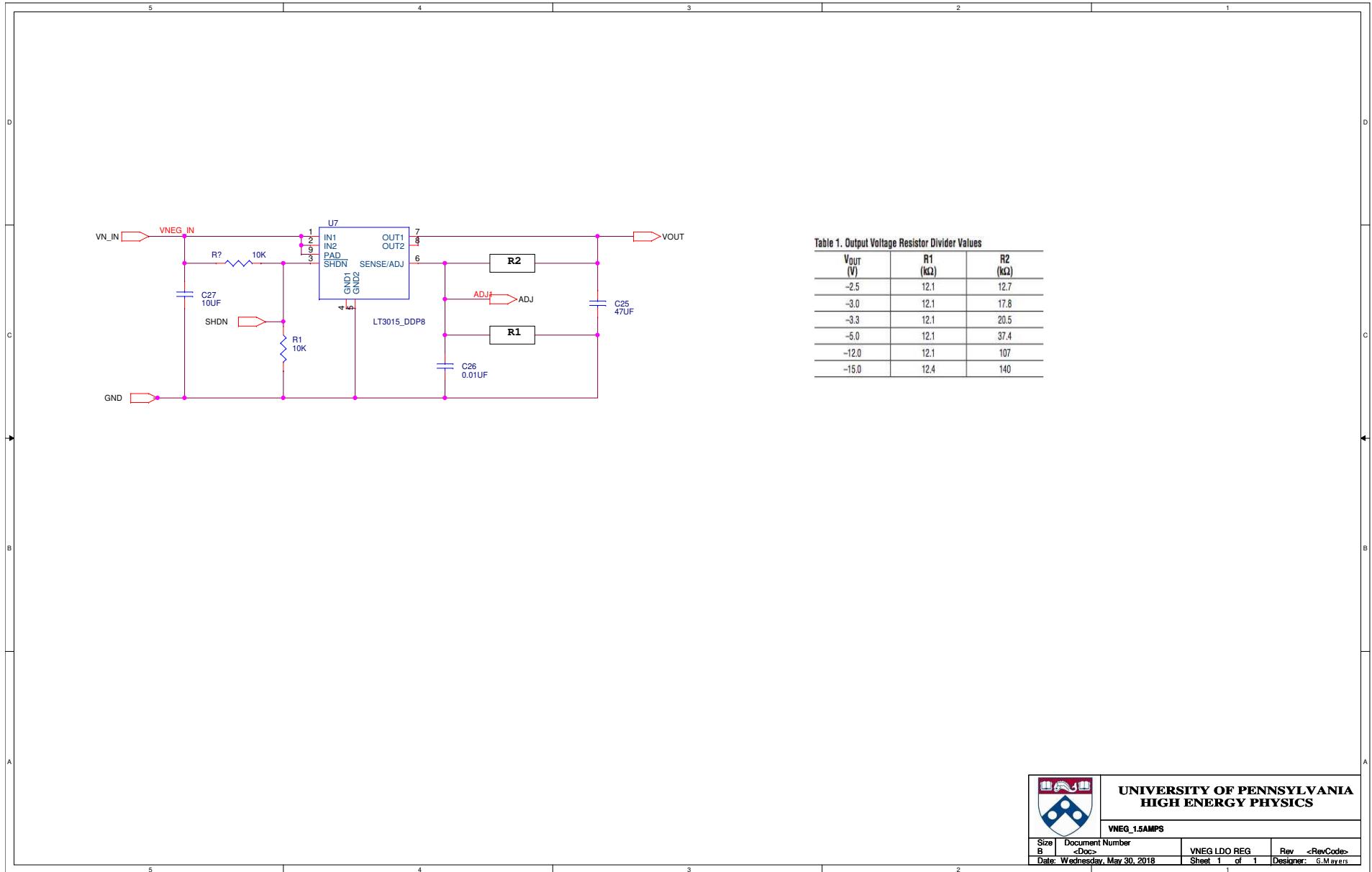
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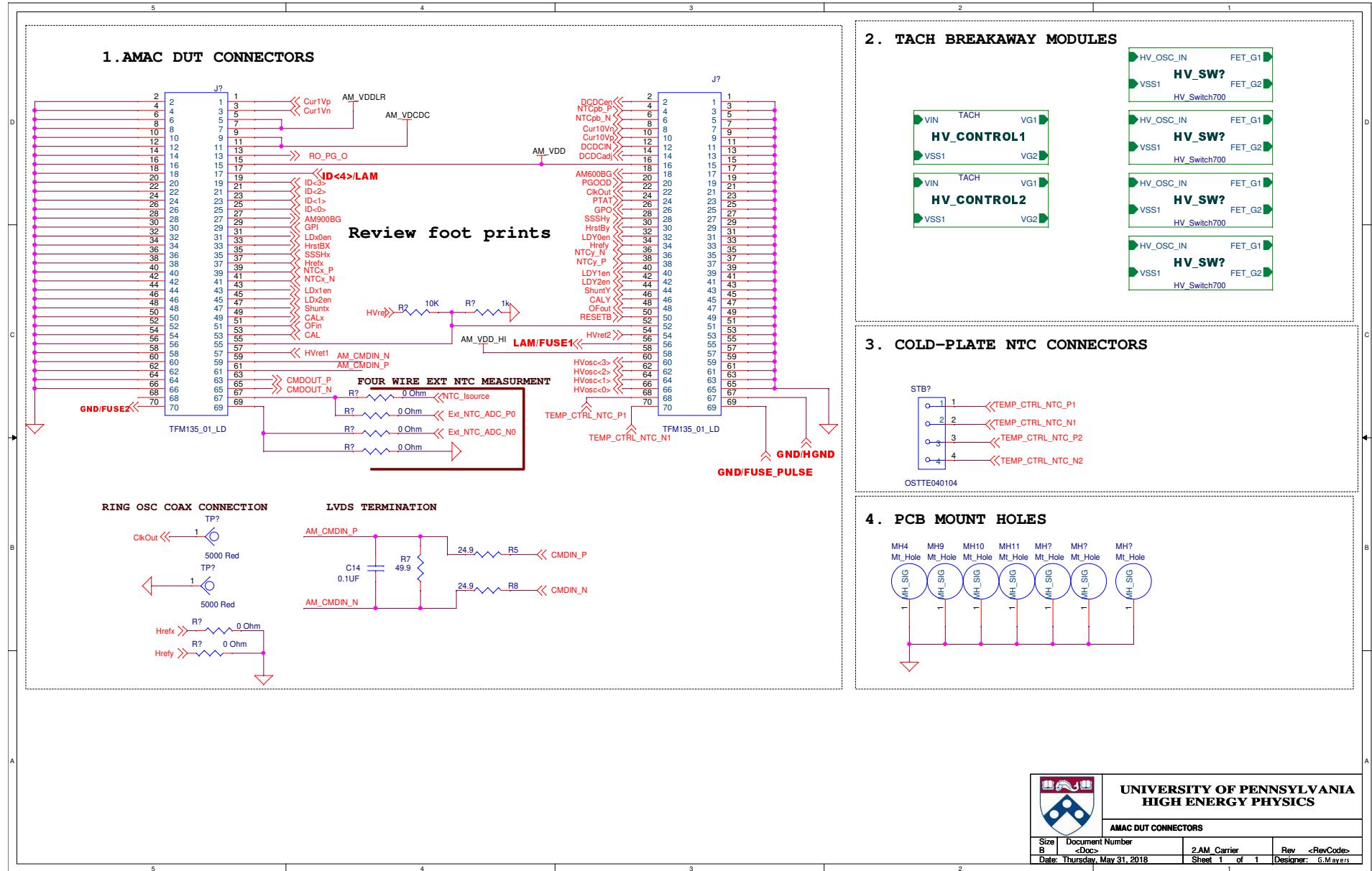


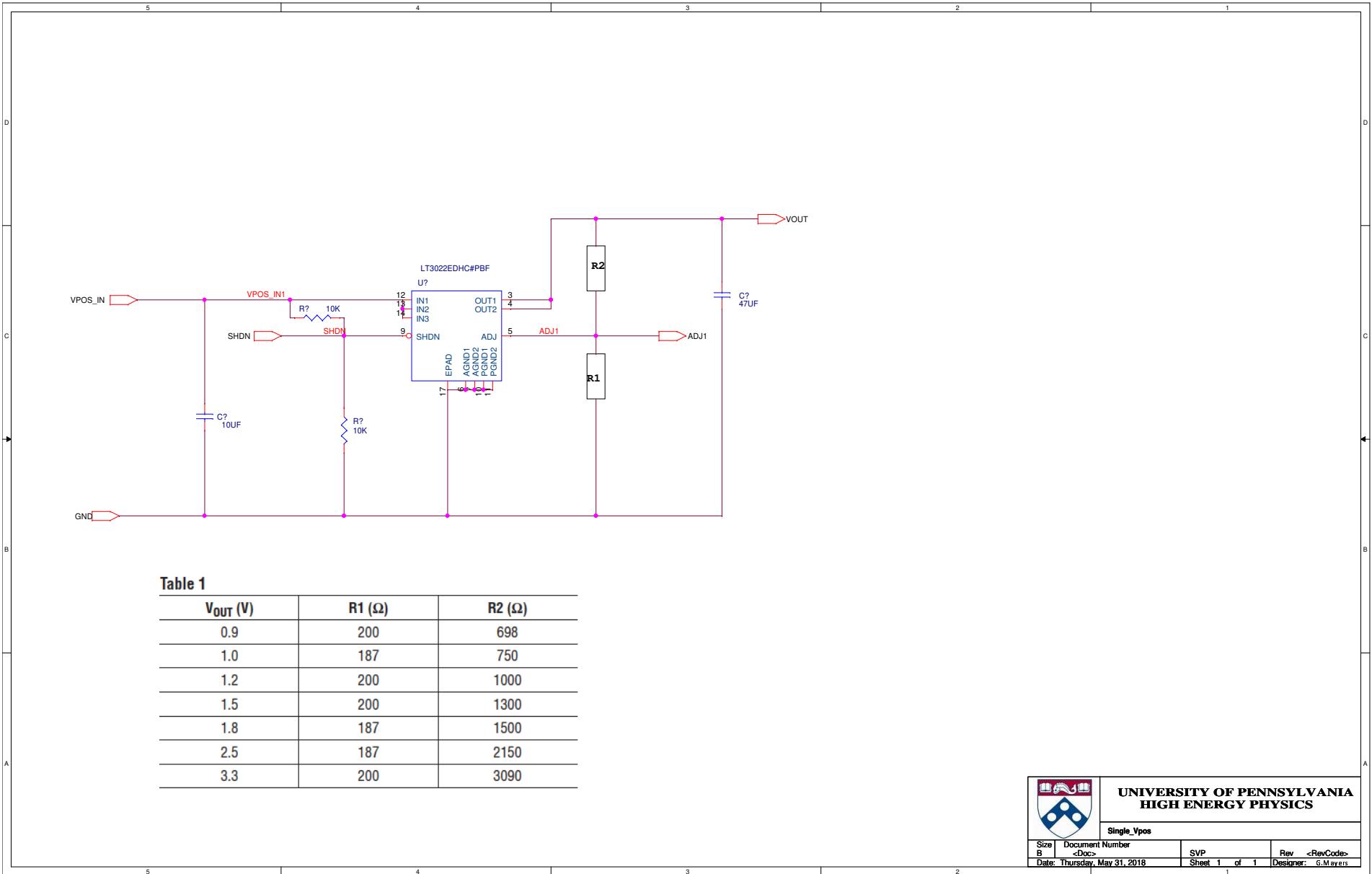
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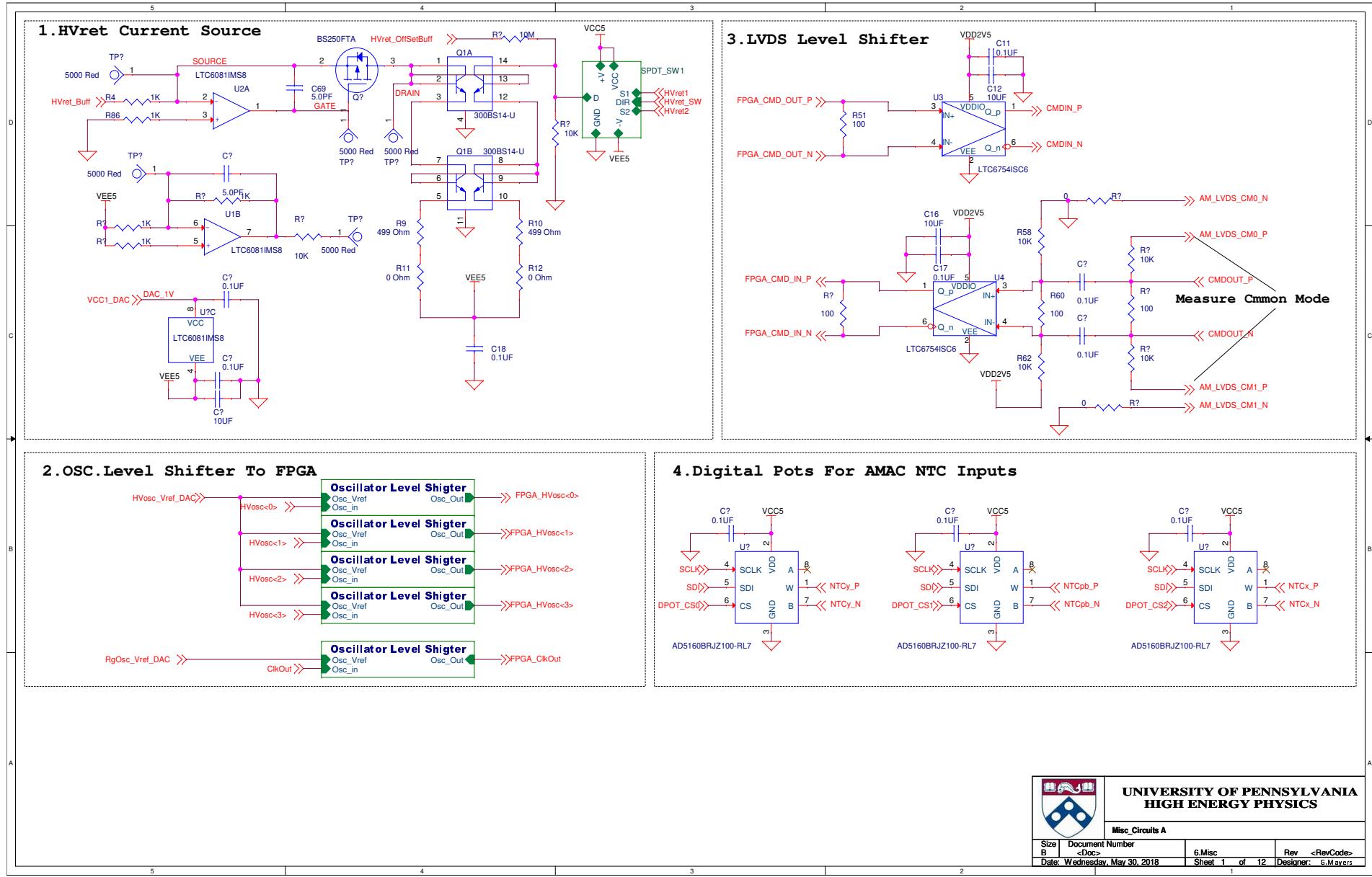
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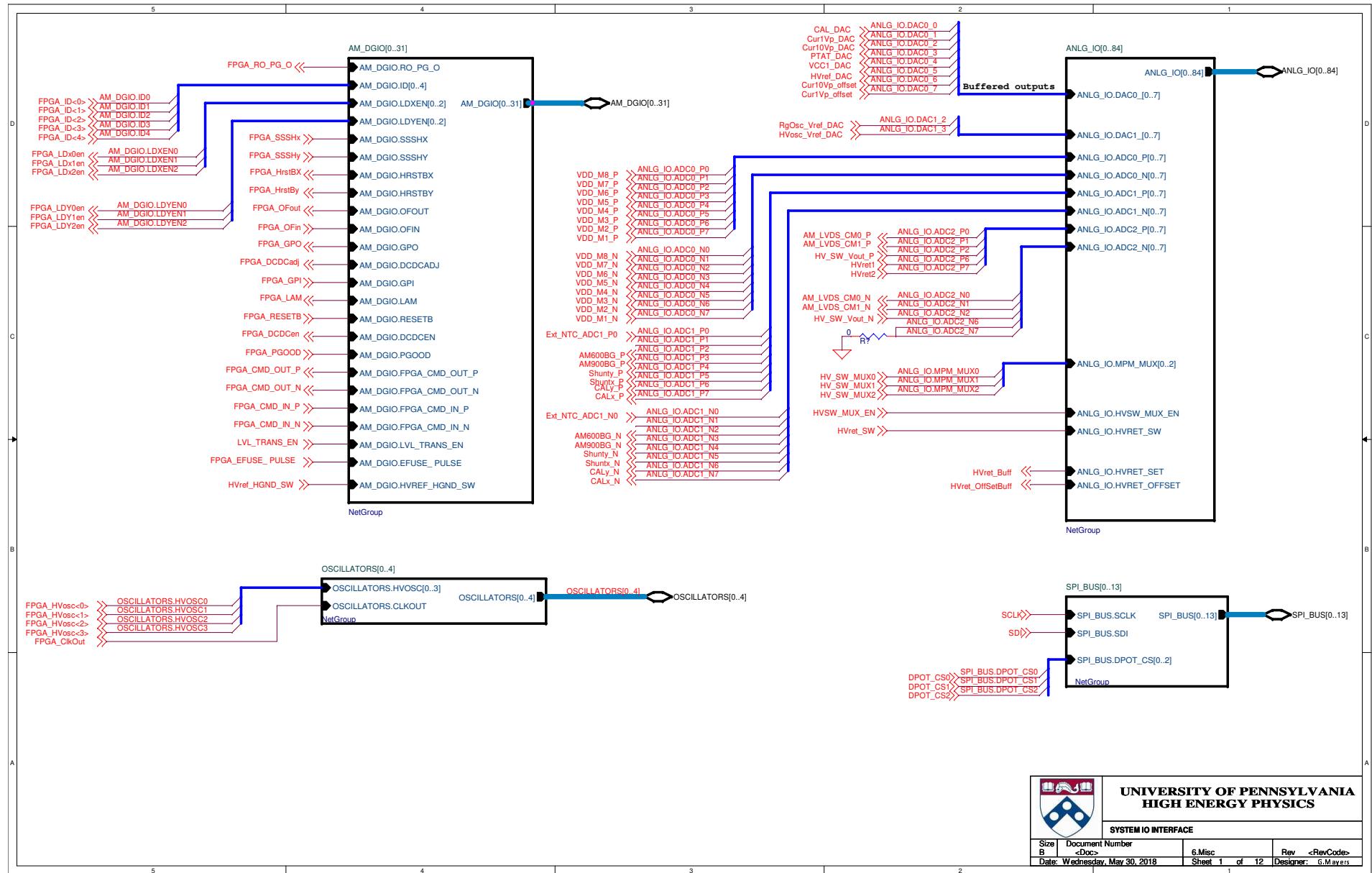




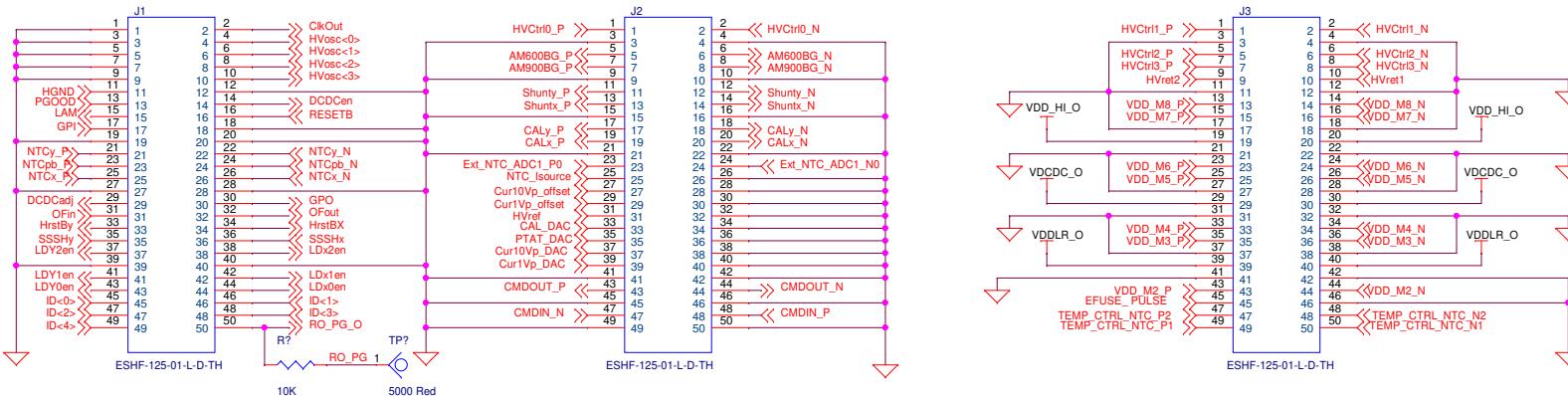


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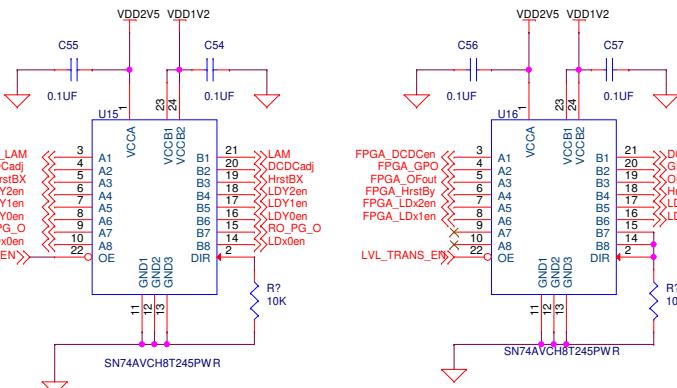
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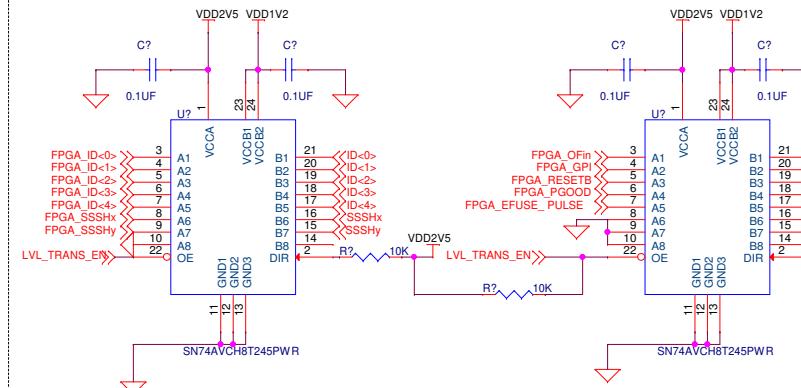
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2. AMAC To FPGA DIO Level Translators



3. FPGA To AMAC DIO Level Translators

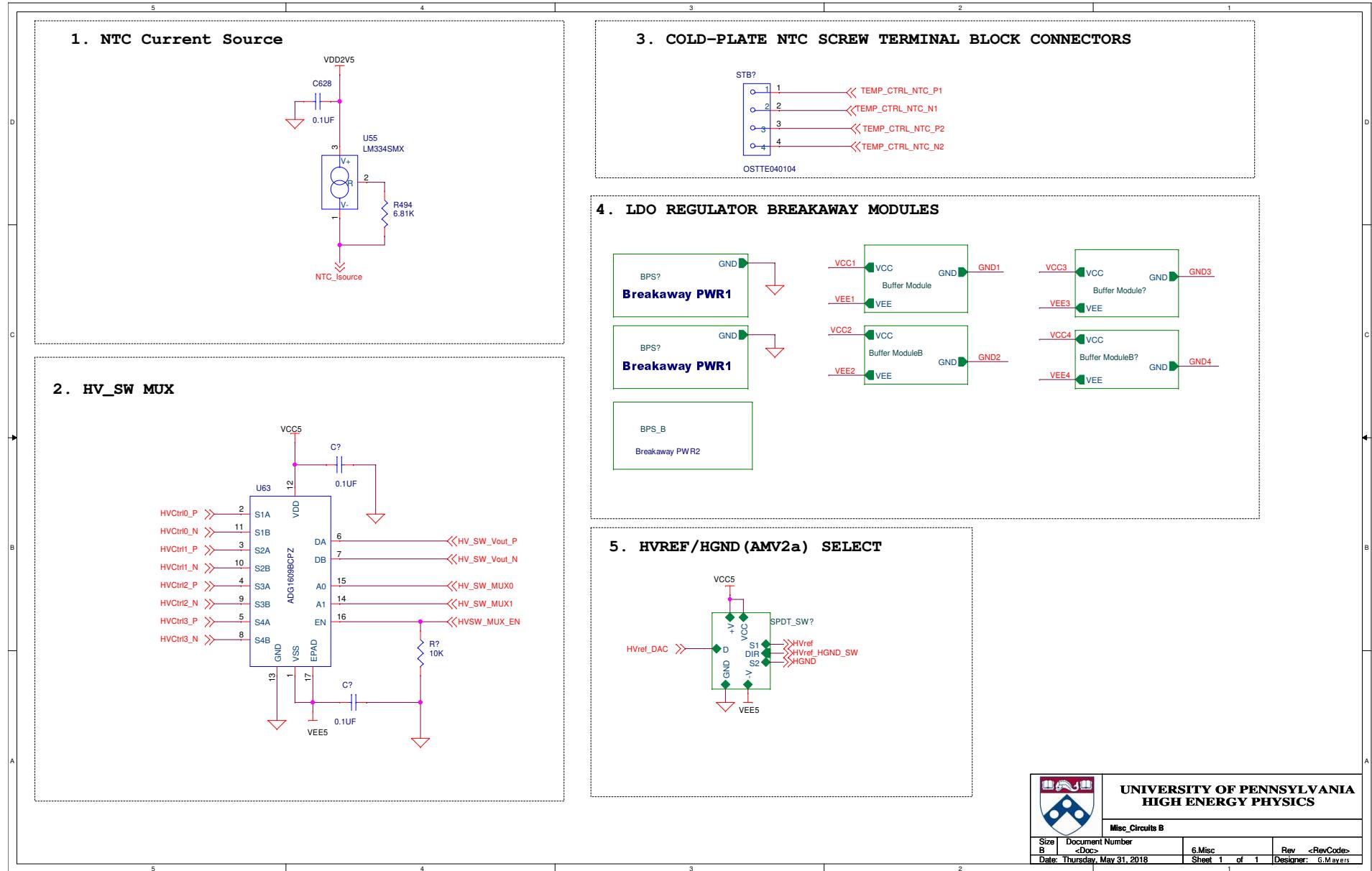


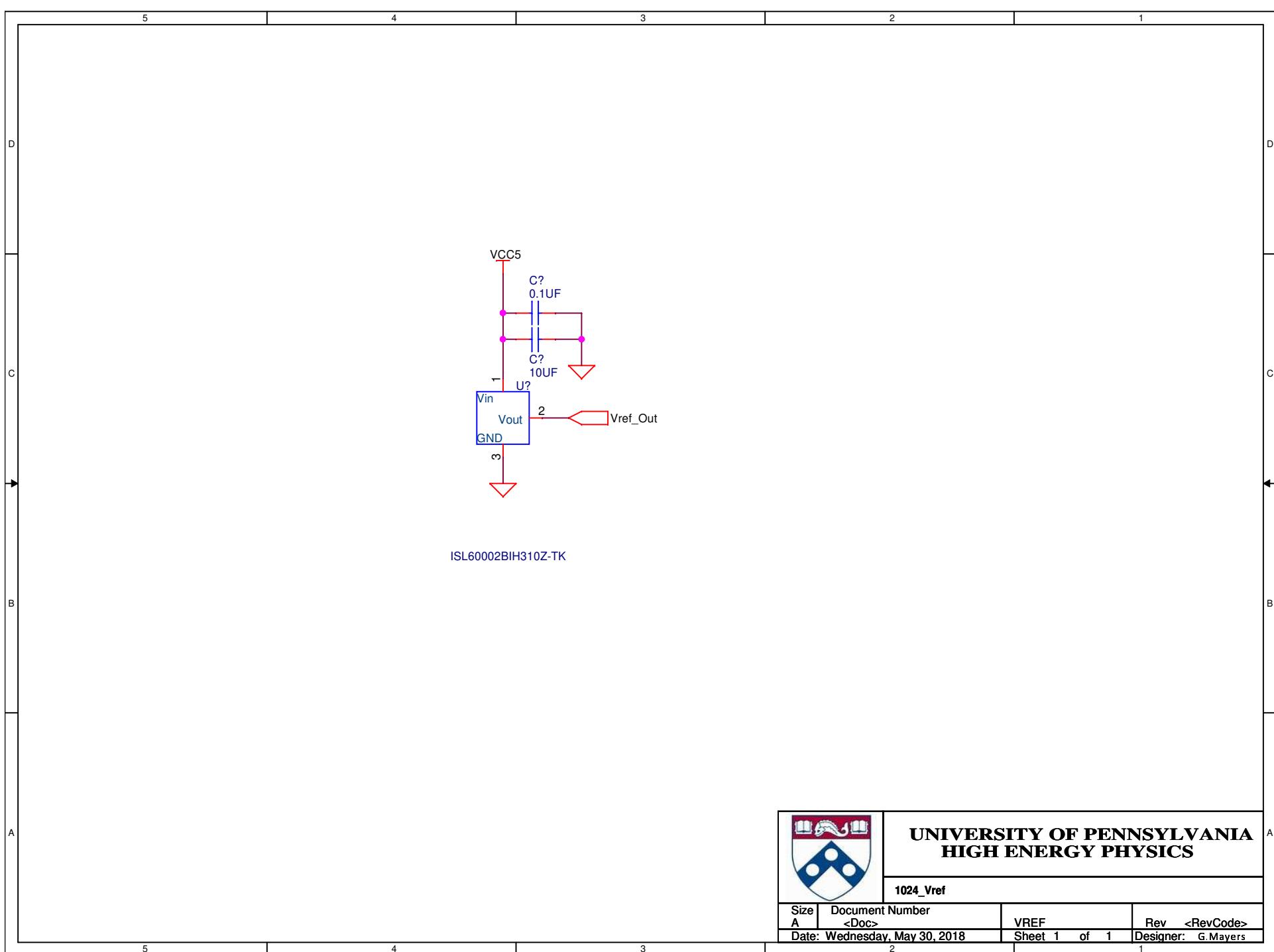
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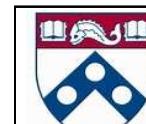
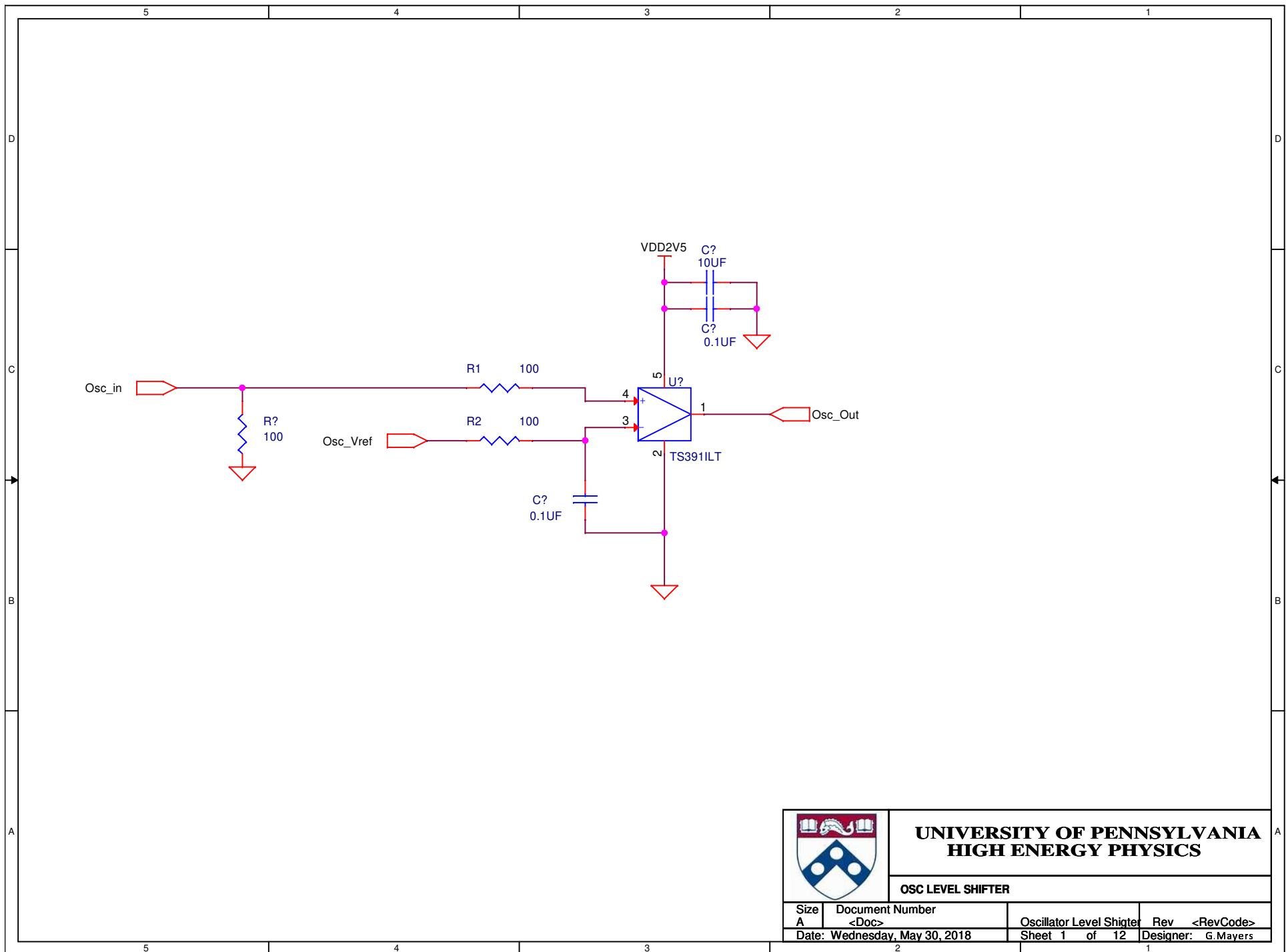
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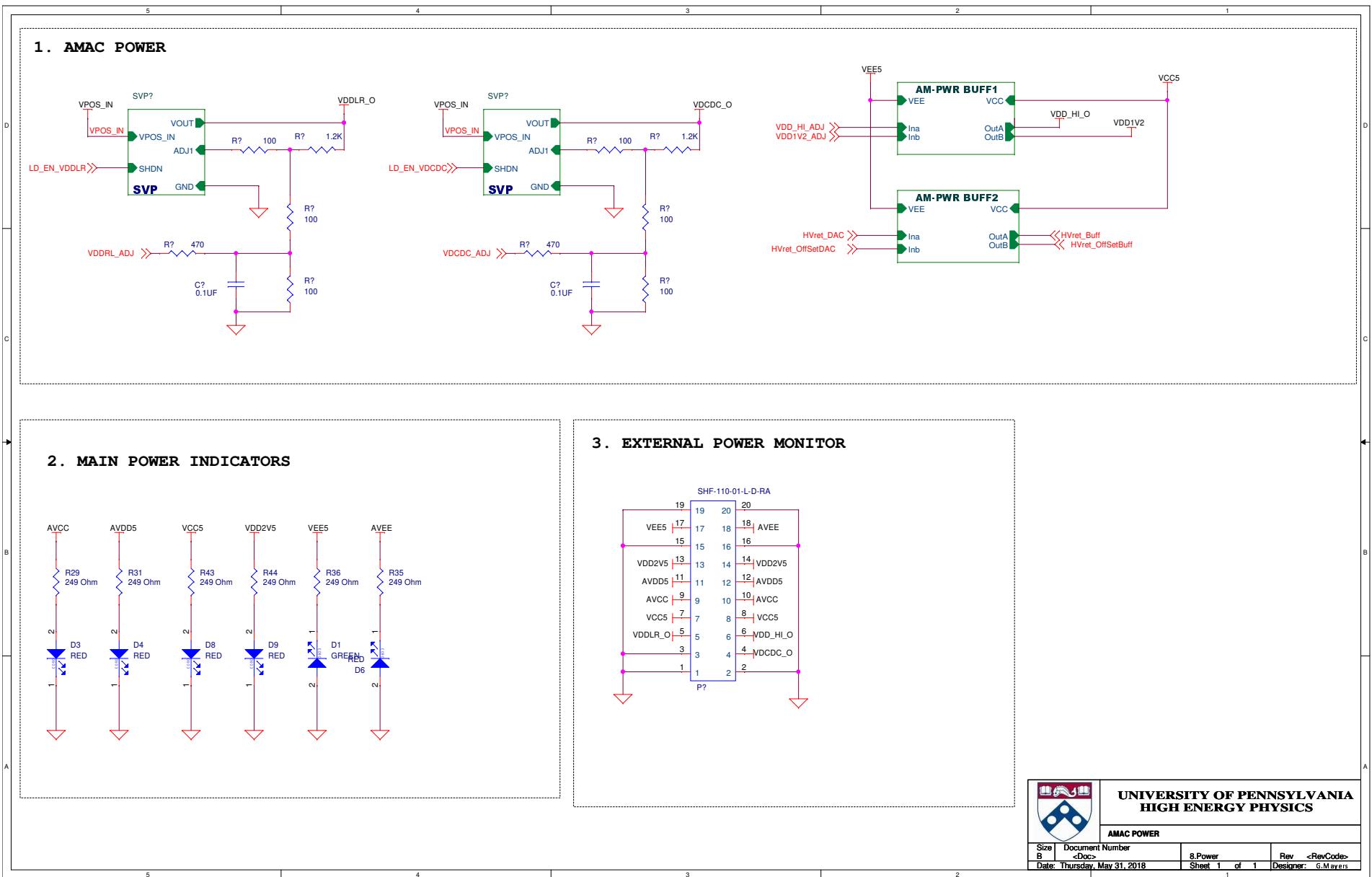


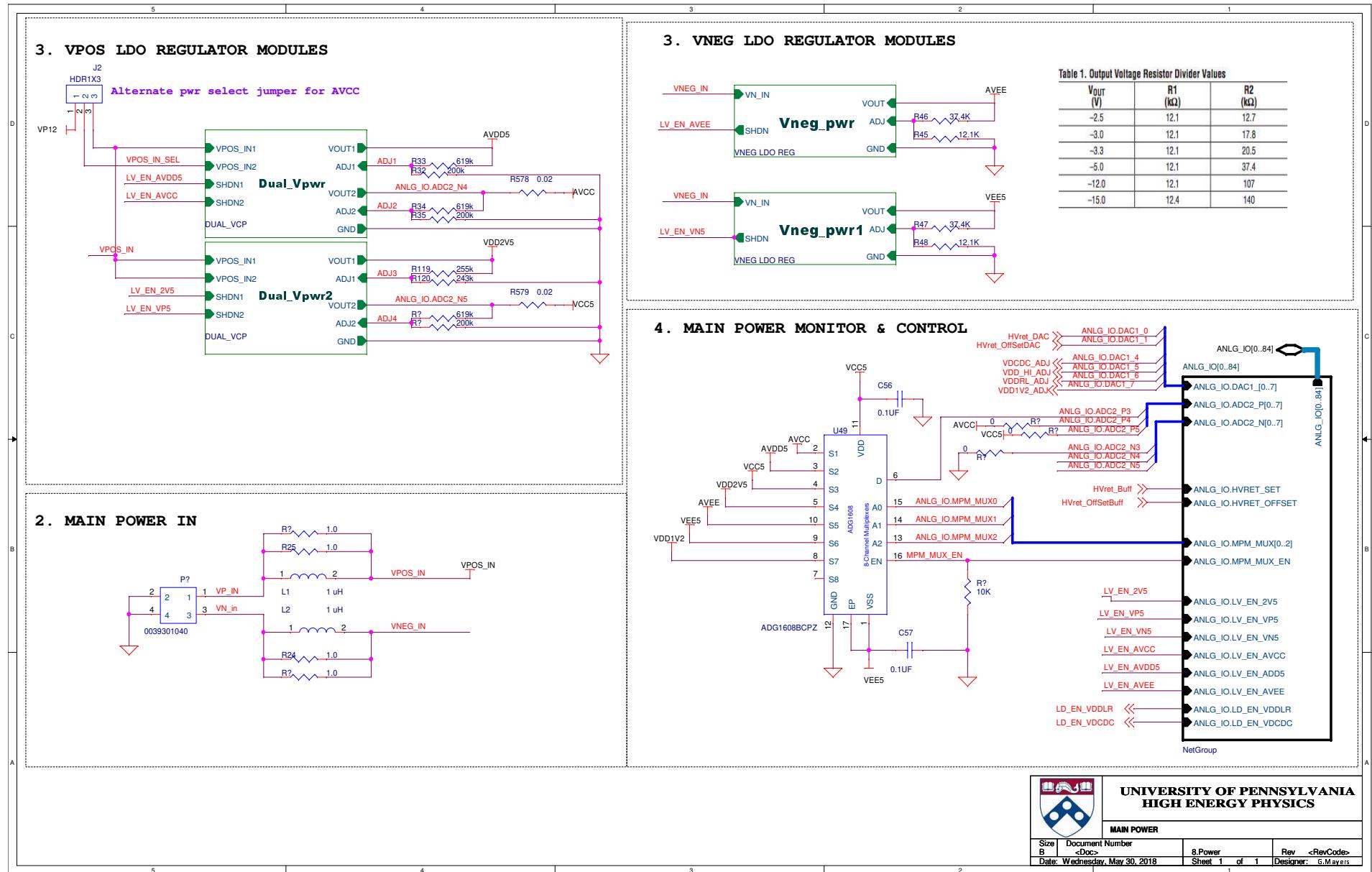




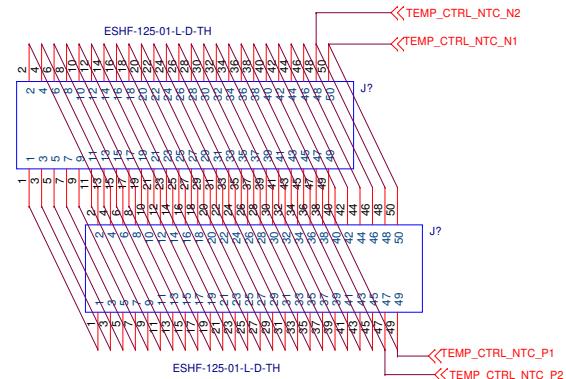
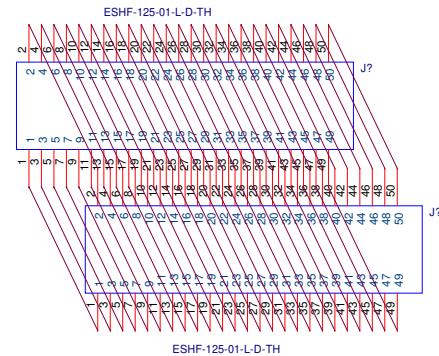
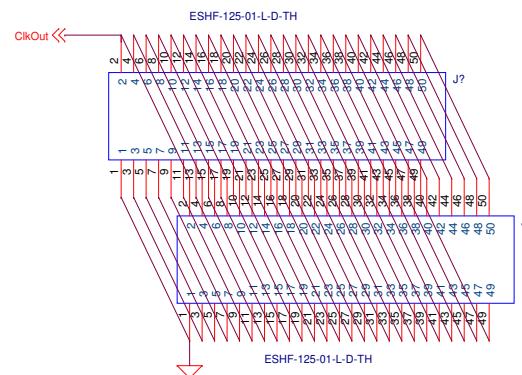
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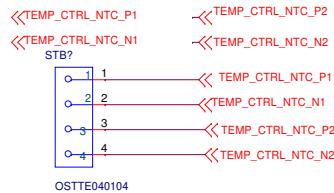




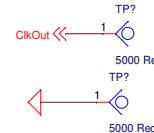
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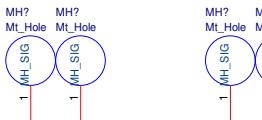
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3. RING OSC COAX CONNECTION

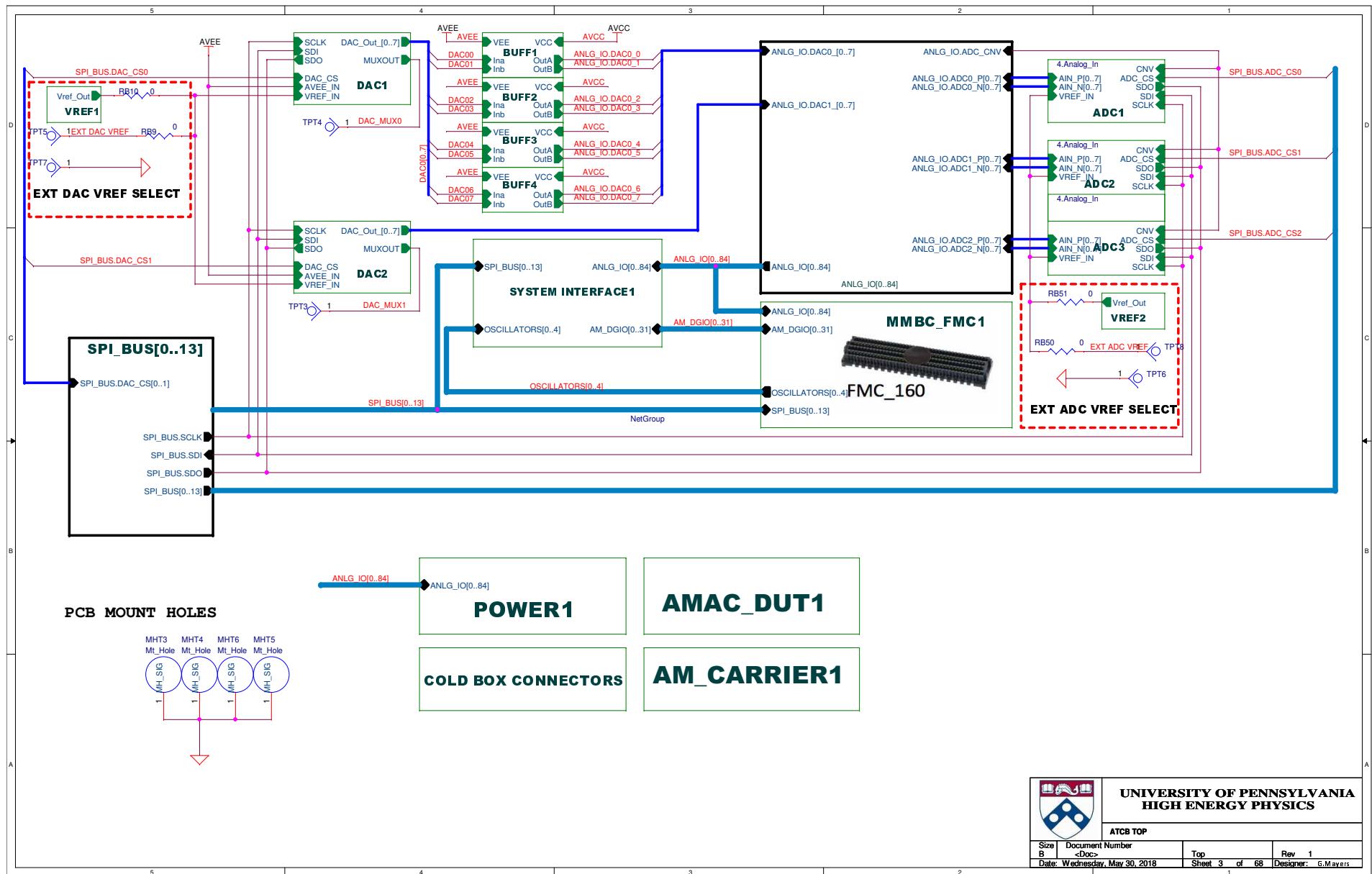


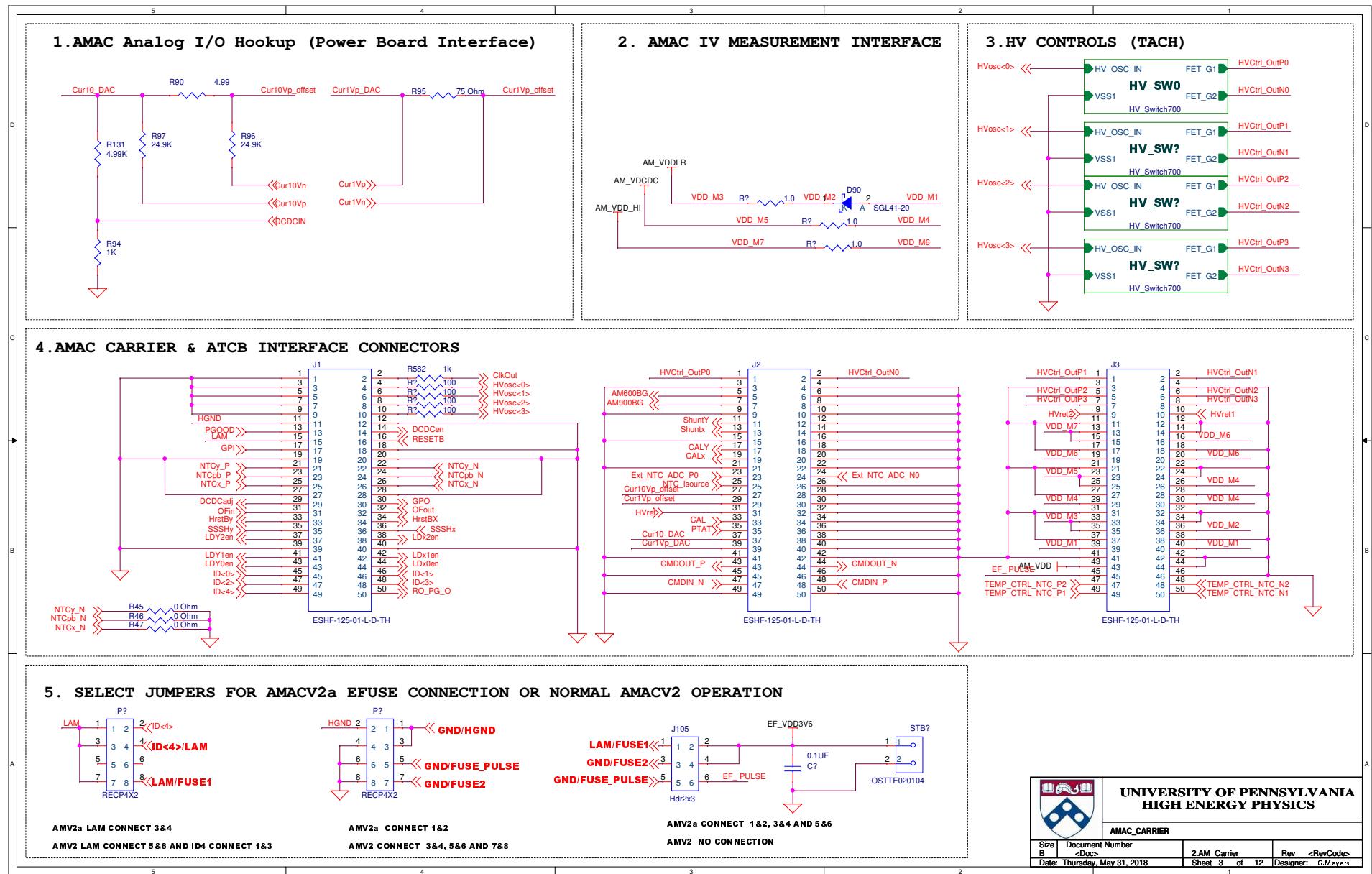
4 . PCB MOUNT HOLES



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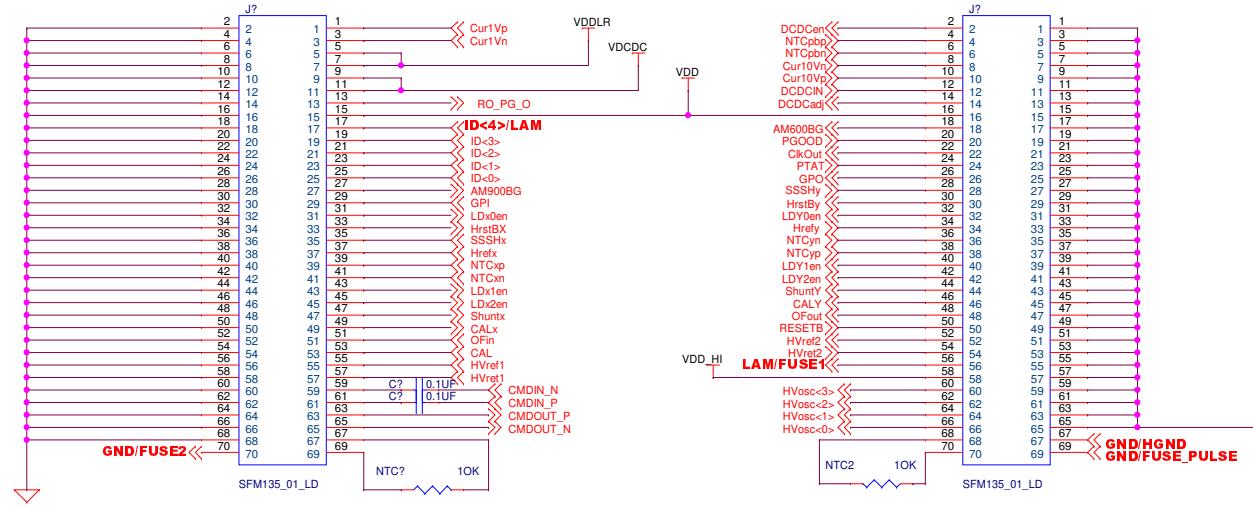
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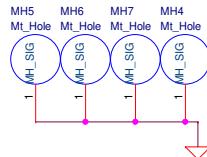
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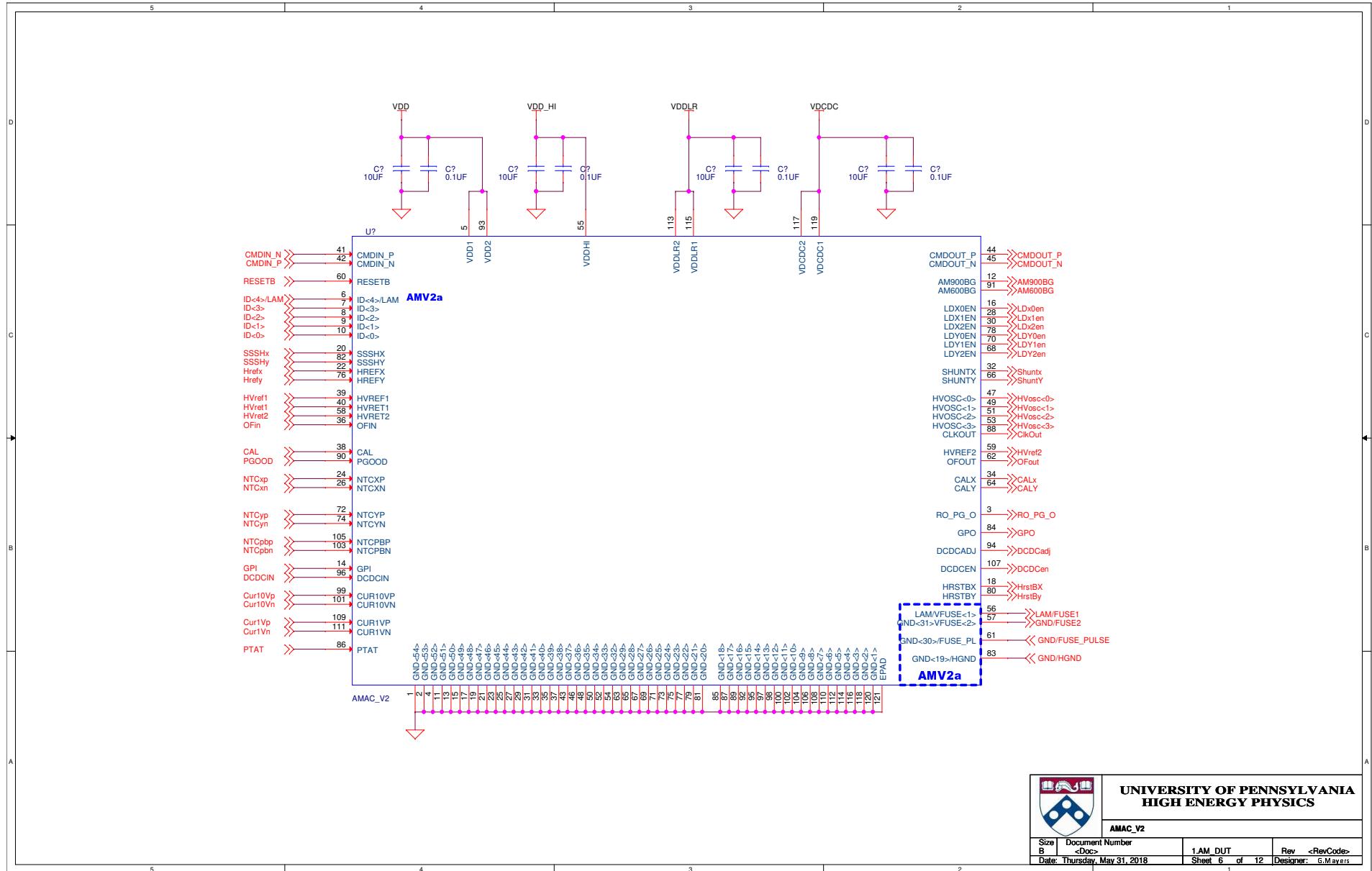


Review foot prints, Vddhv, vdd etc

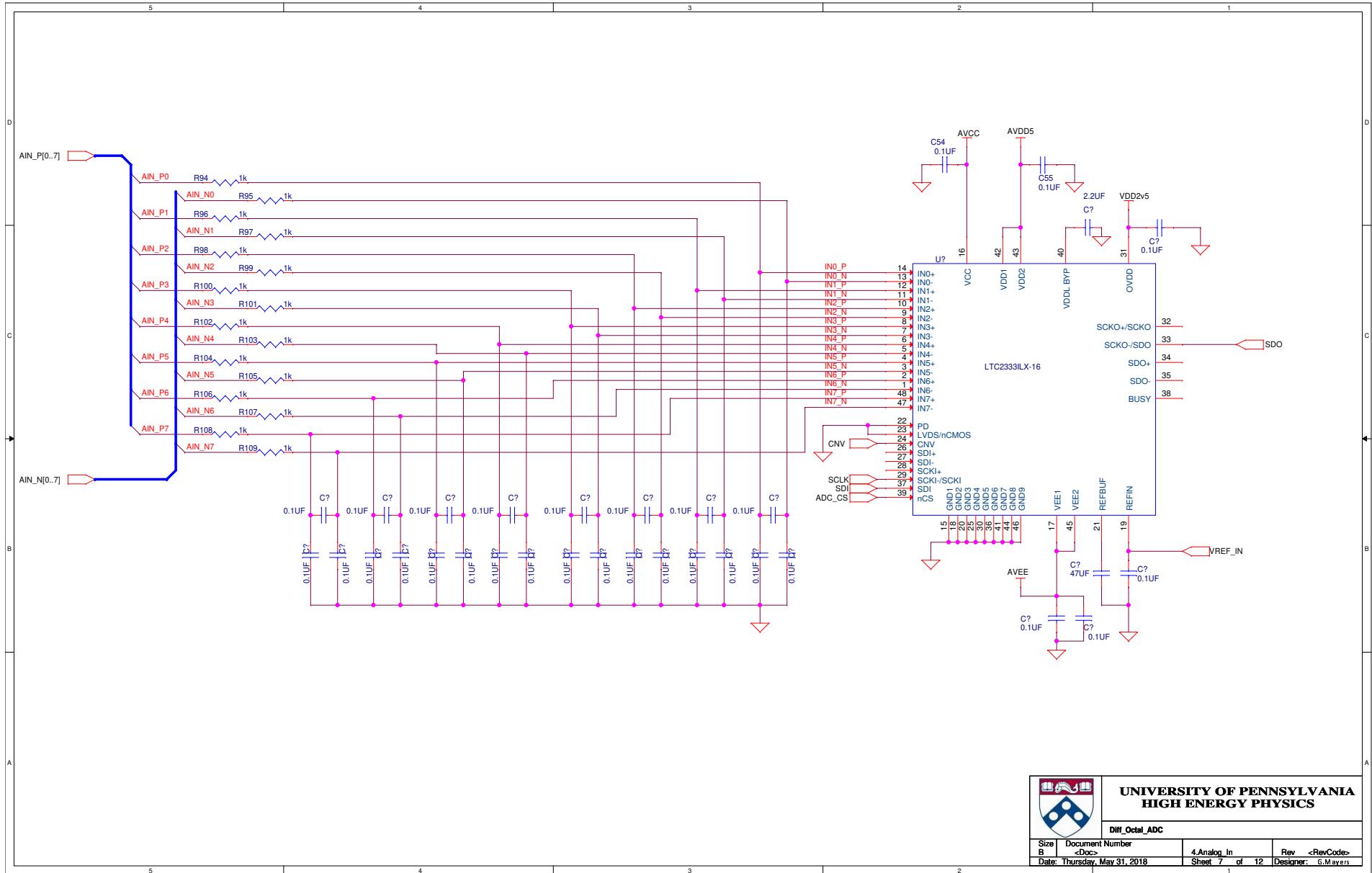
PCB MOUNT HOLES



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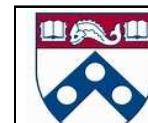
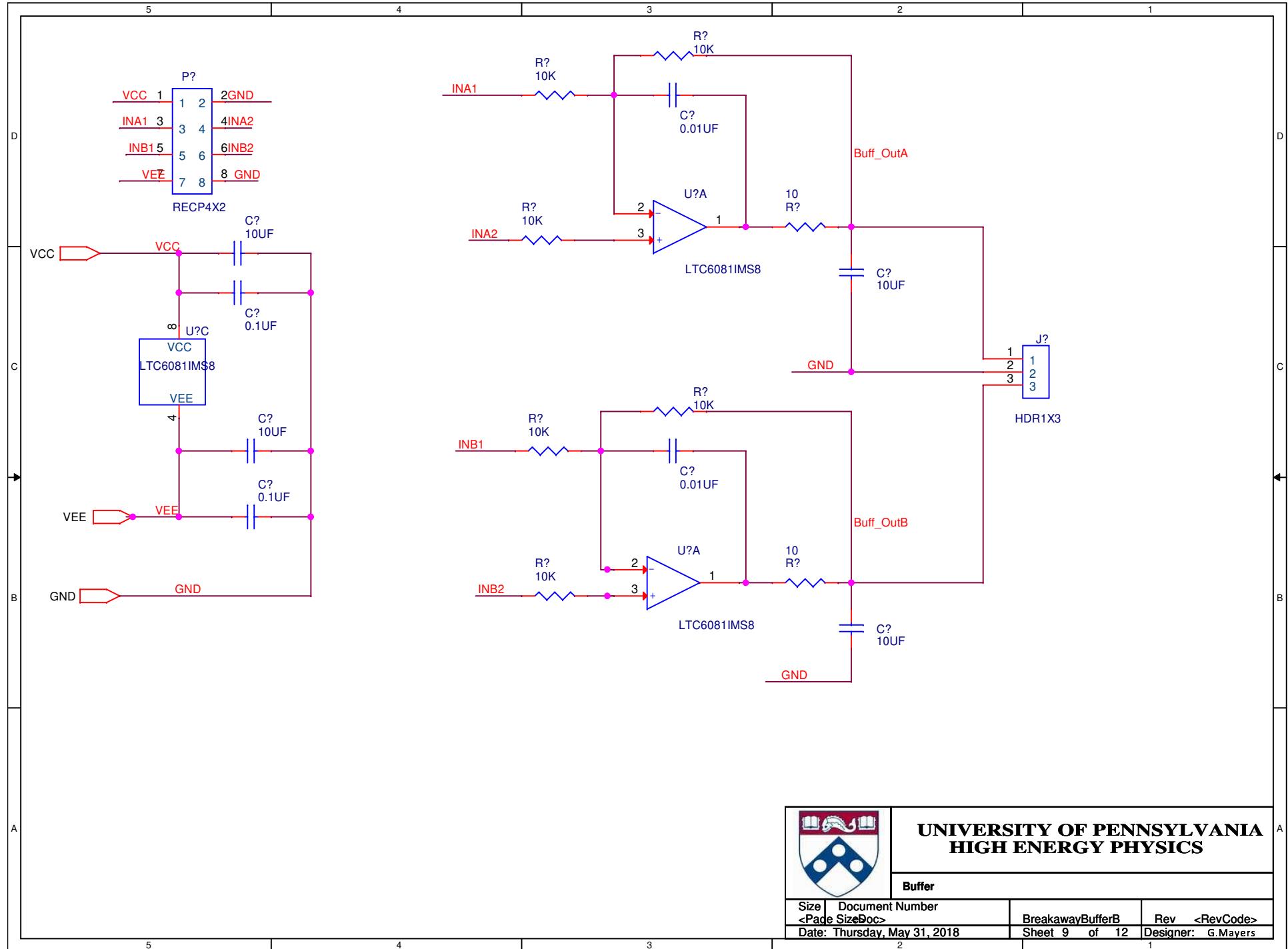


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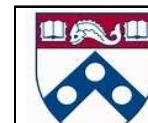
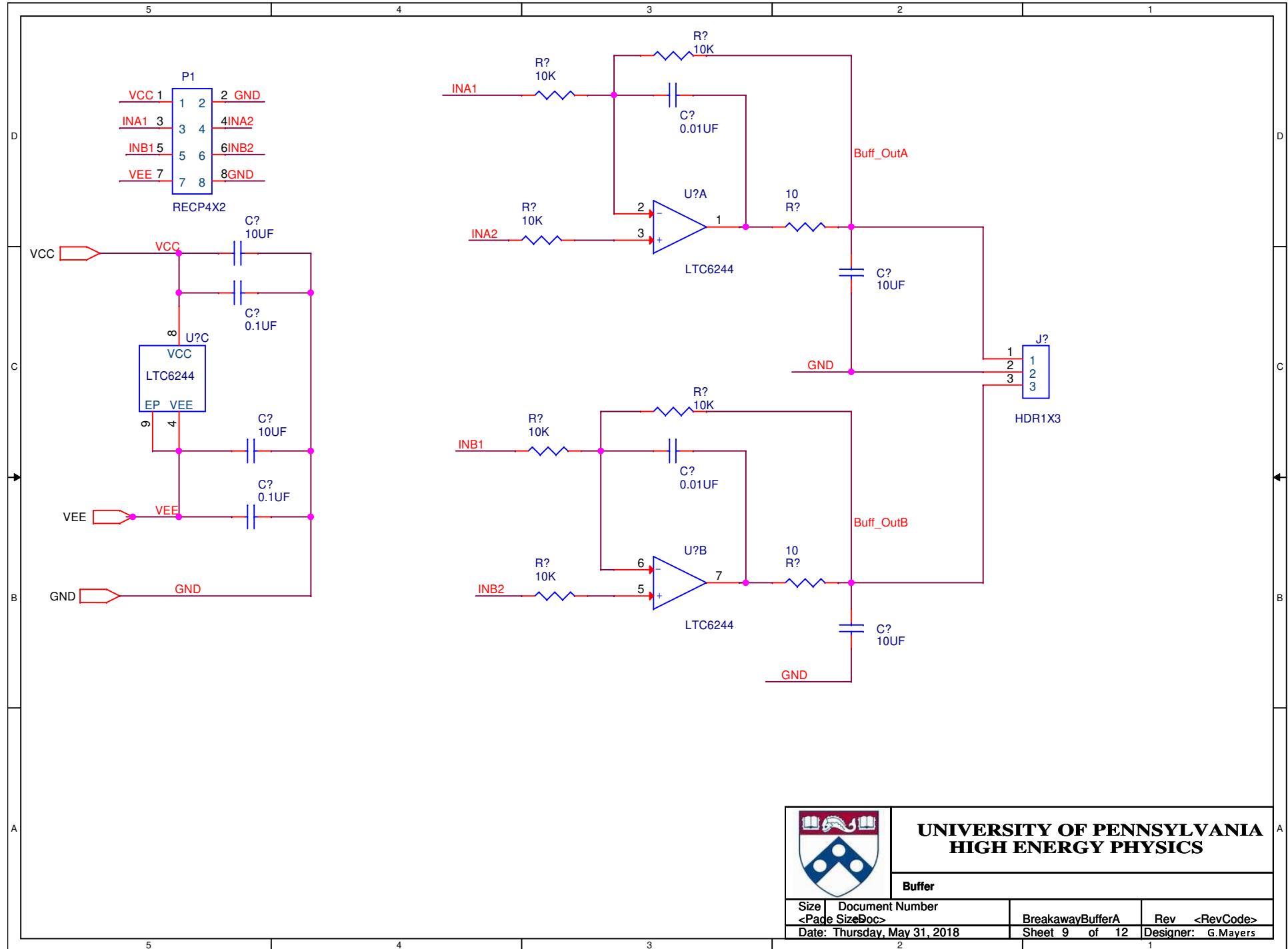
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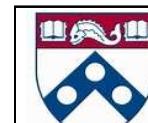
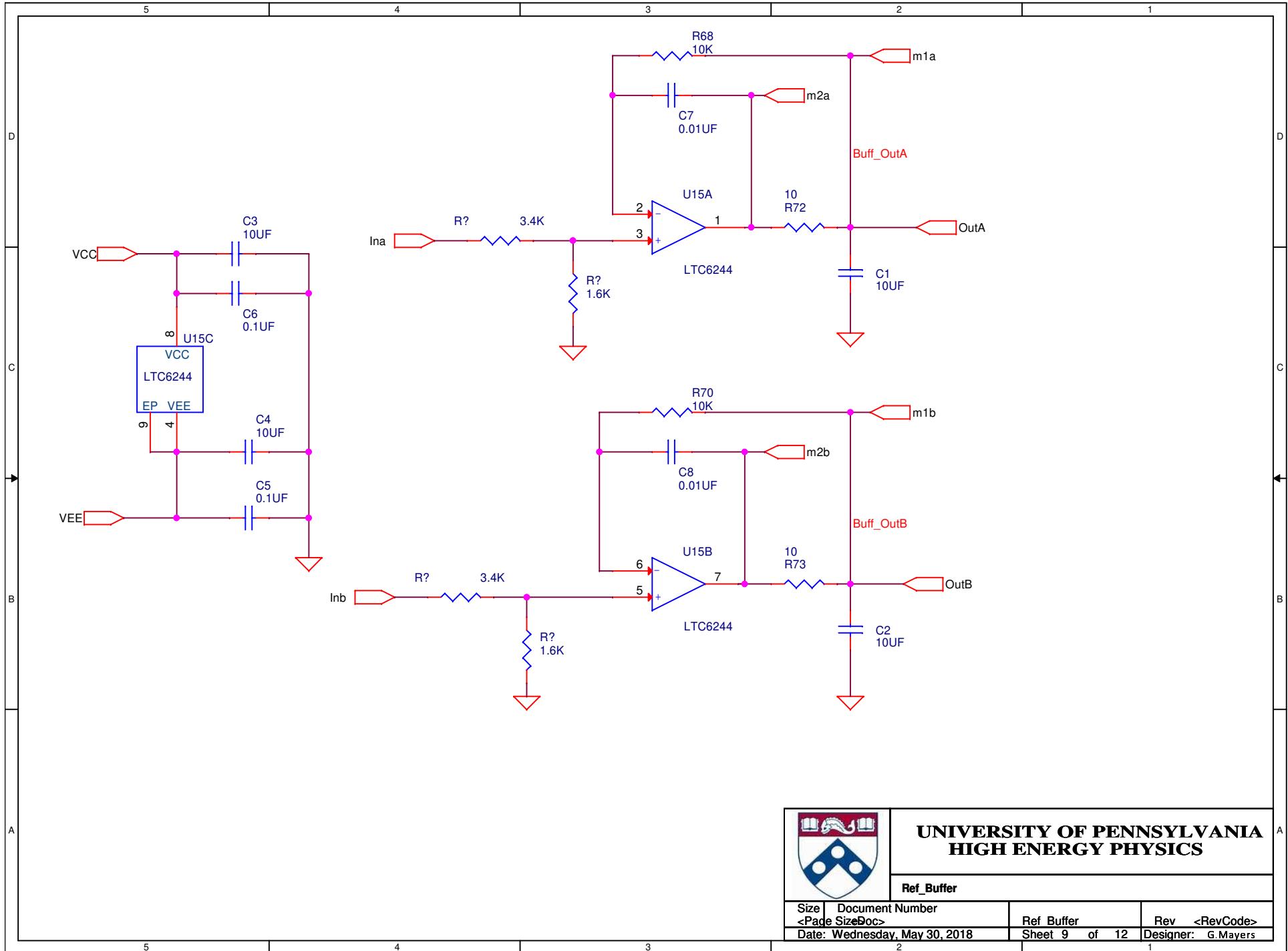
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