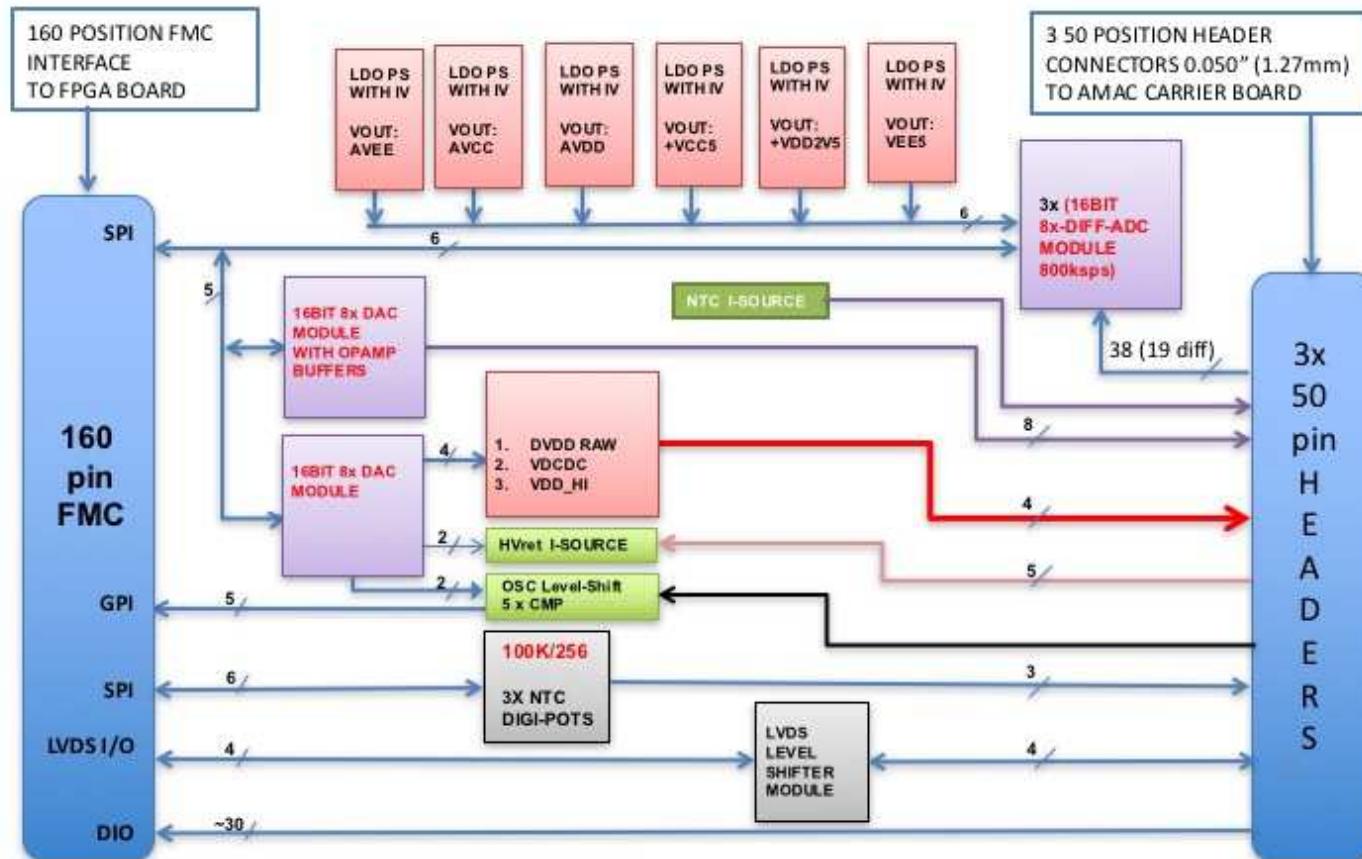


## AMAC V2 TEST & CONTROL BLOCK DIAGRAM



4/27/18

Godwin Mayers

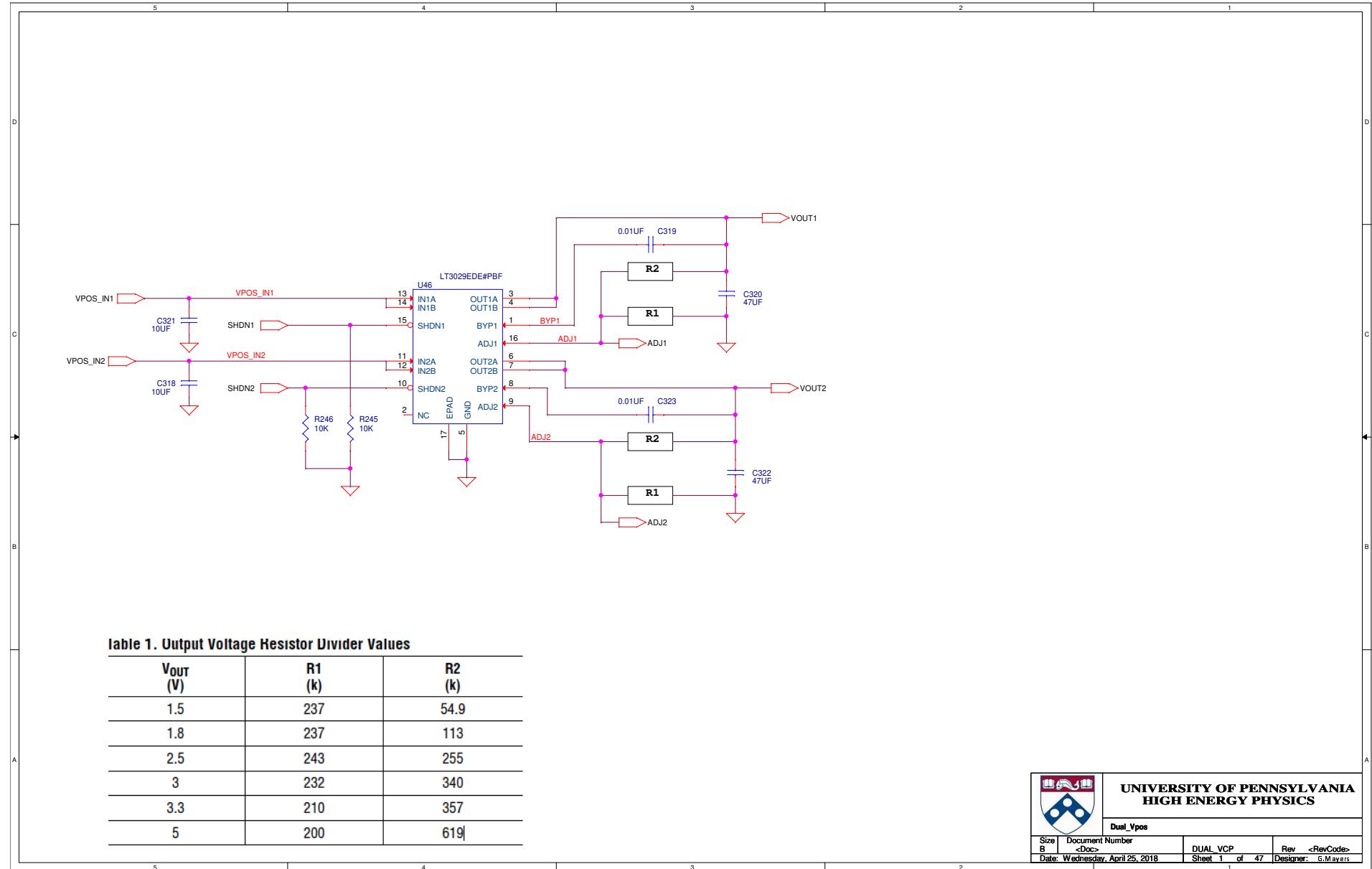


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ATCB Block Diagrams

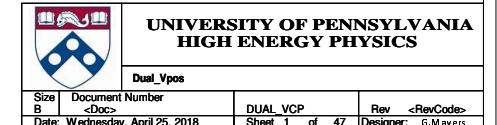
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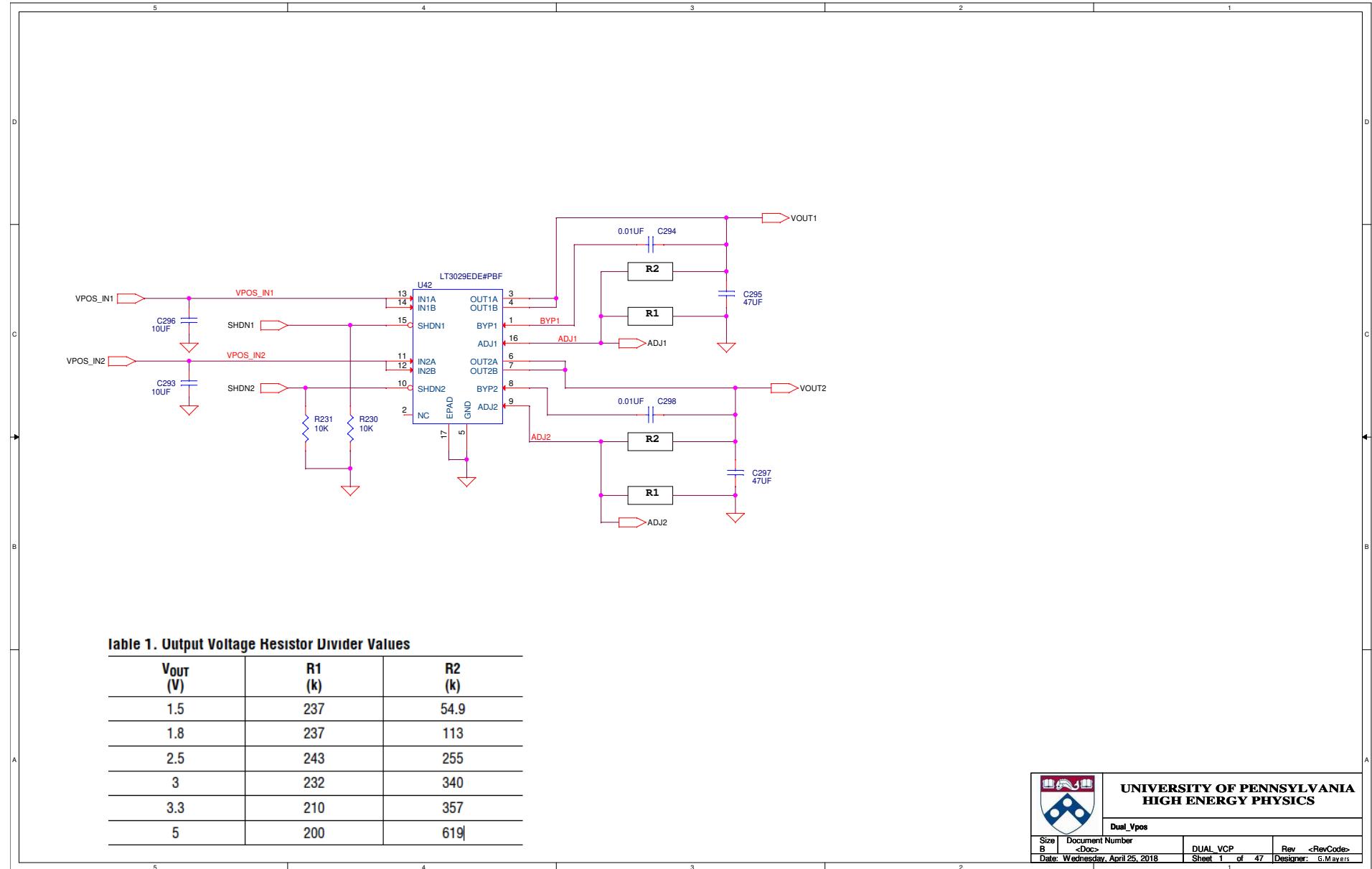
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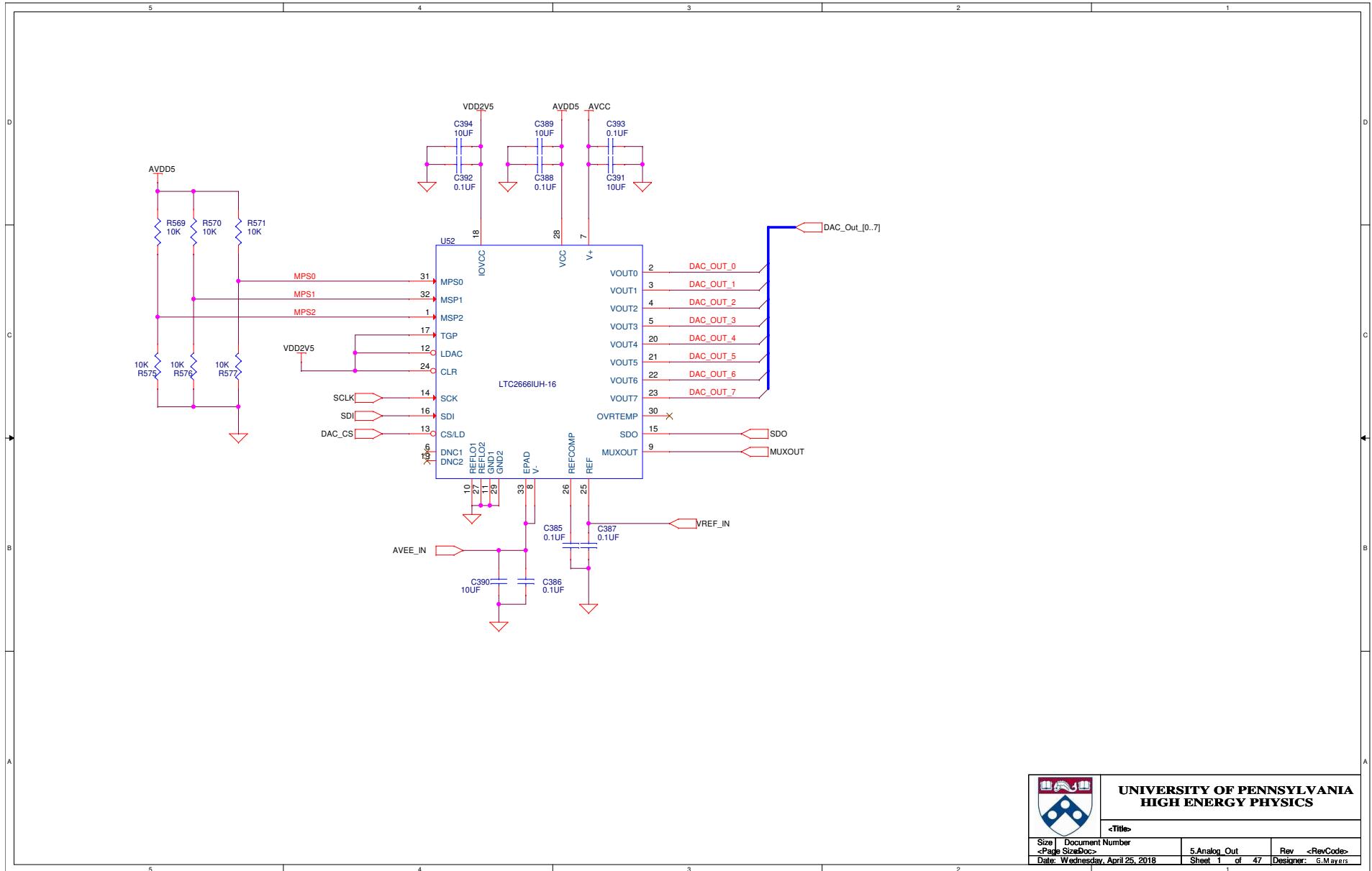


**Table 1. Output Voltage Resistor Divider Values**

V <sub>OUT</sub> (V)	R <sub>1</sub> (k)	R <sub>2</sub> (k)
1.5	237	54.9
1.8	237	113
2.5	243	255
3	232	340
3.3	210	357
5	200	619







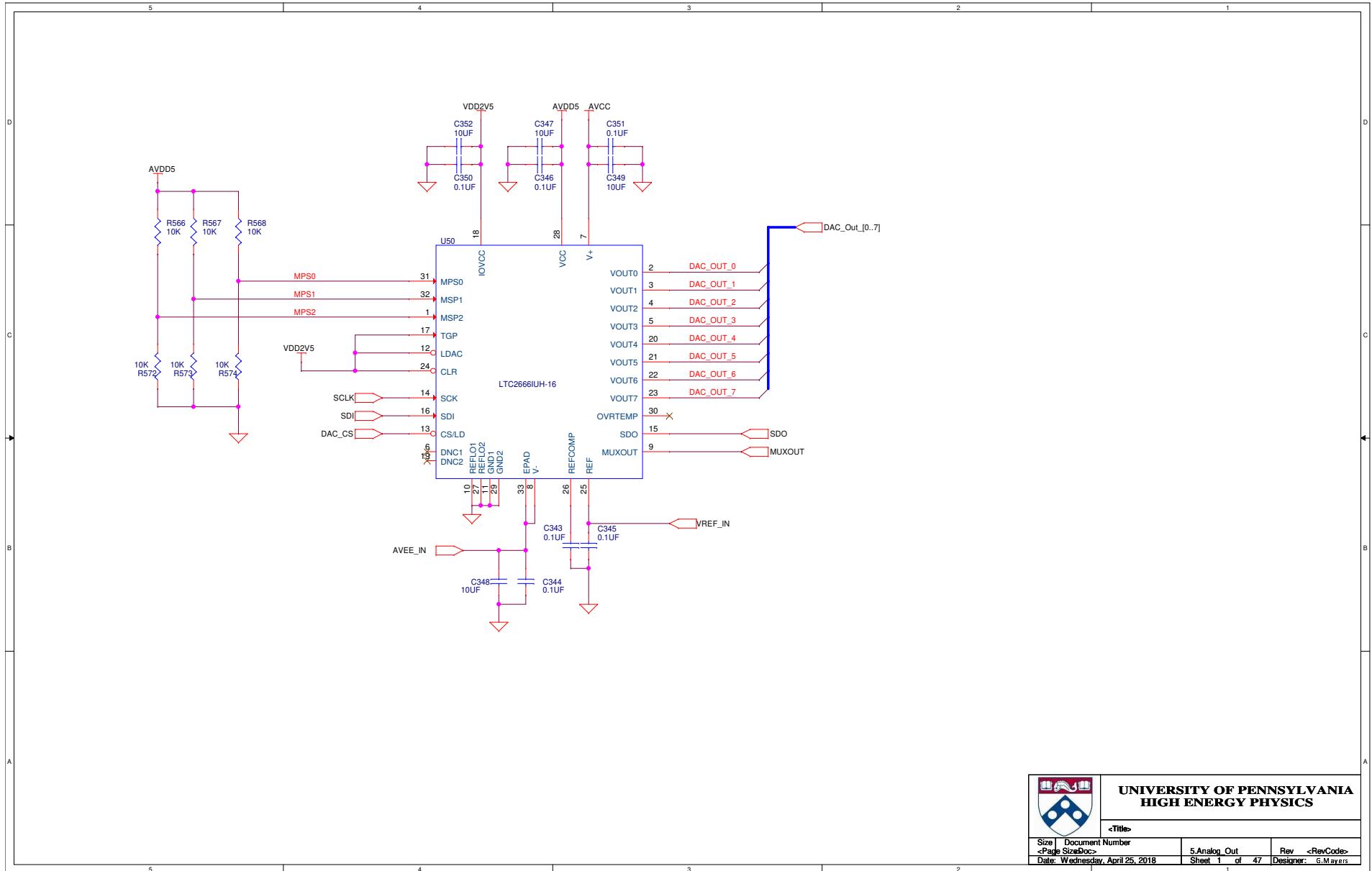
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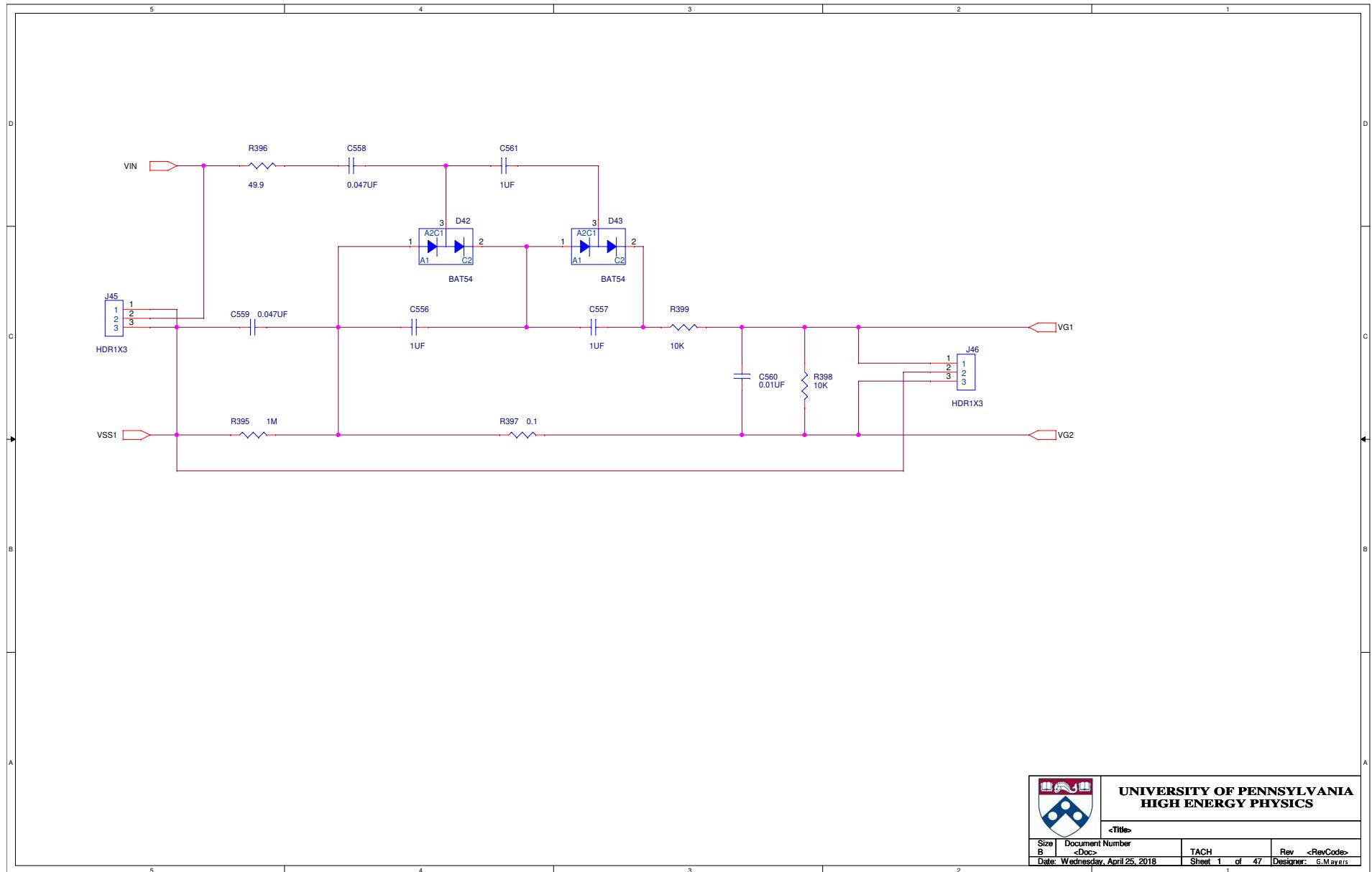
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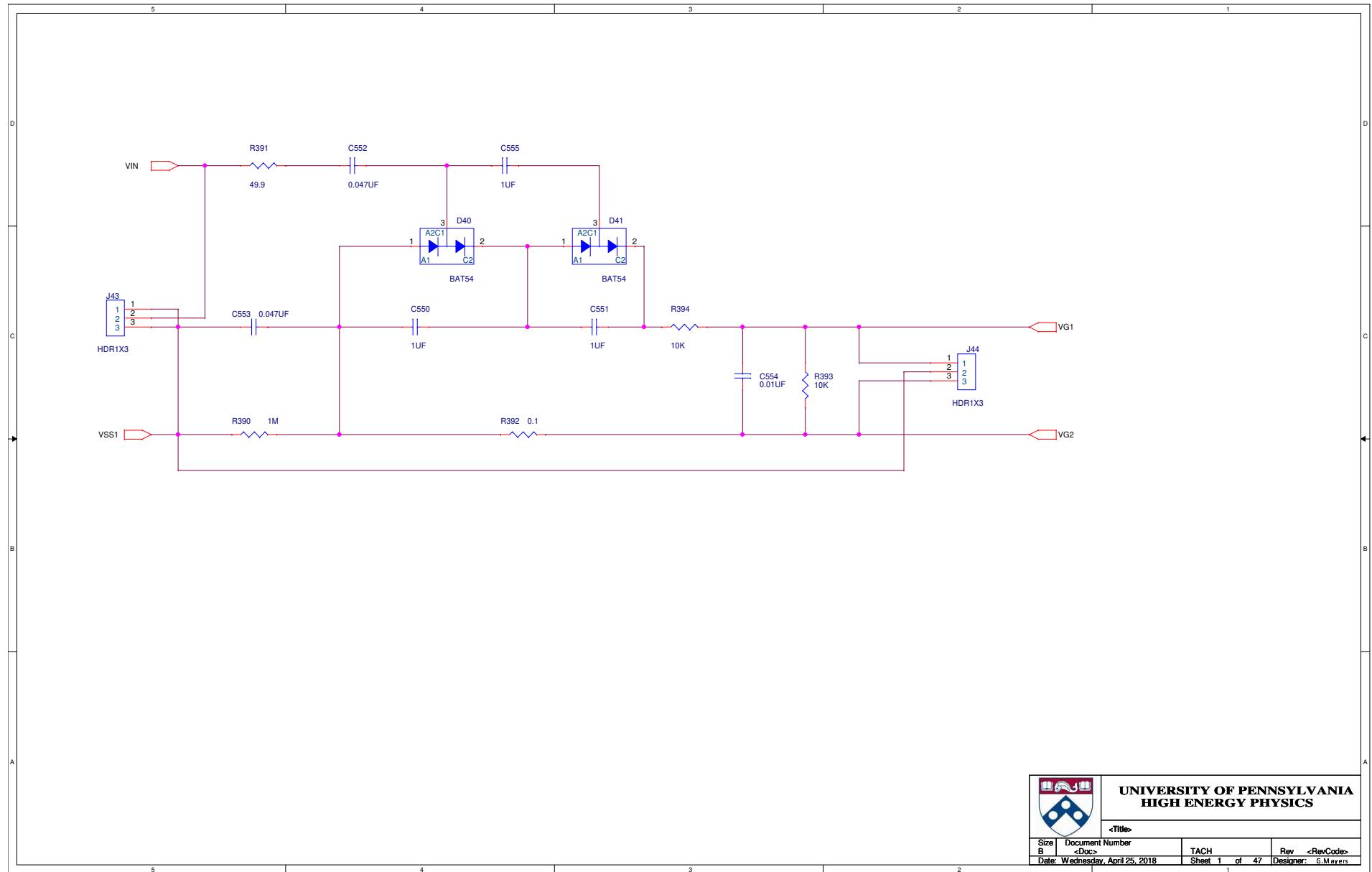
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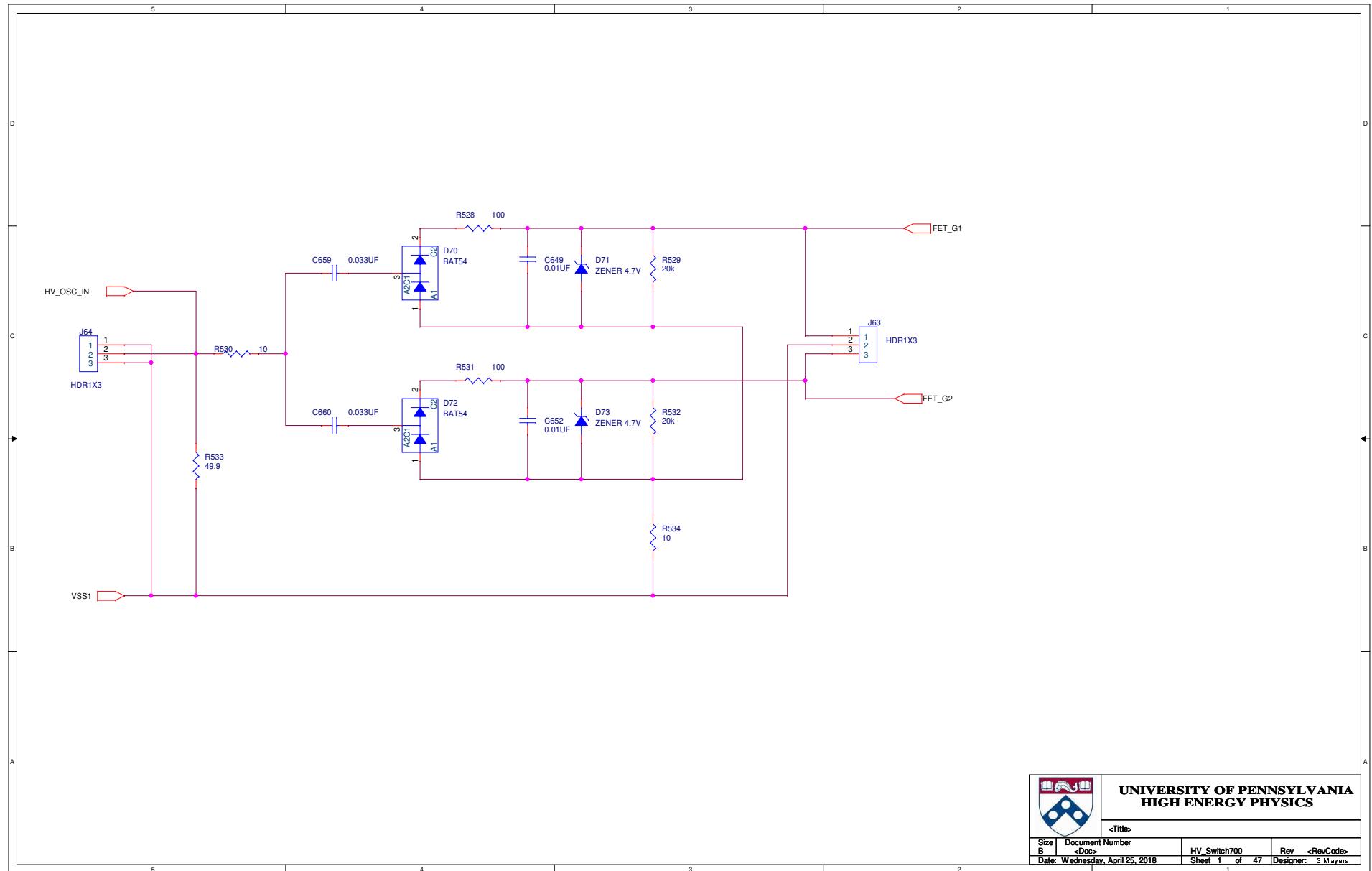
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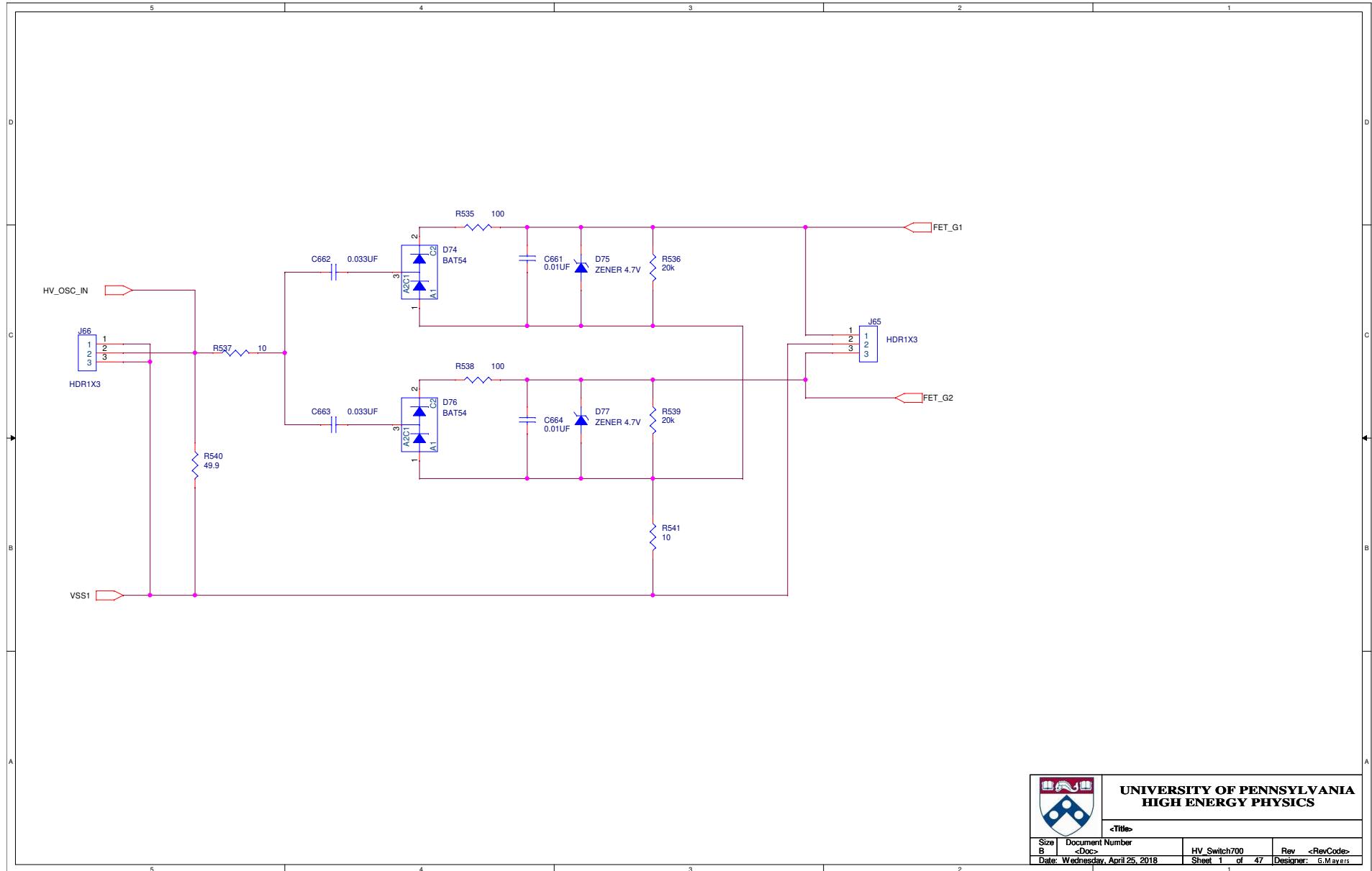
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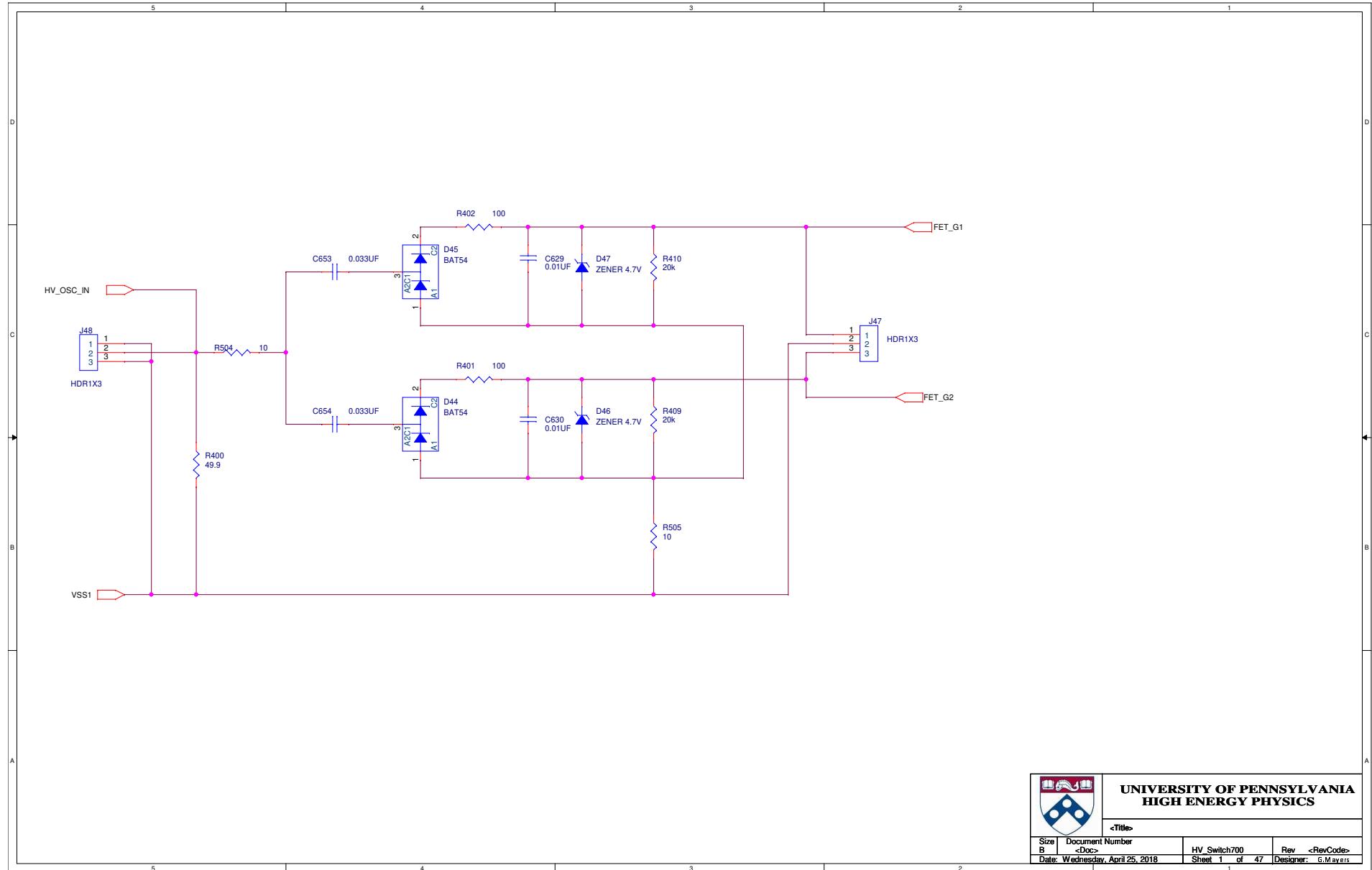
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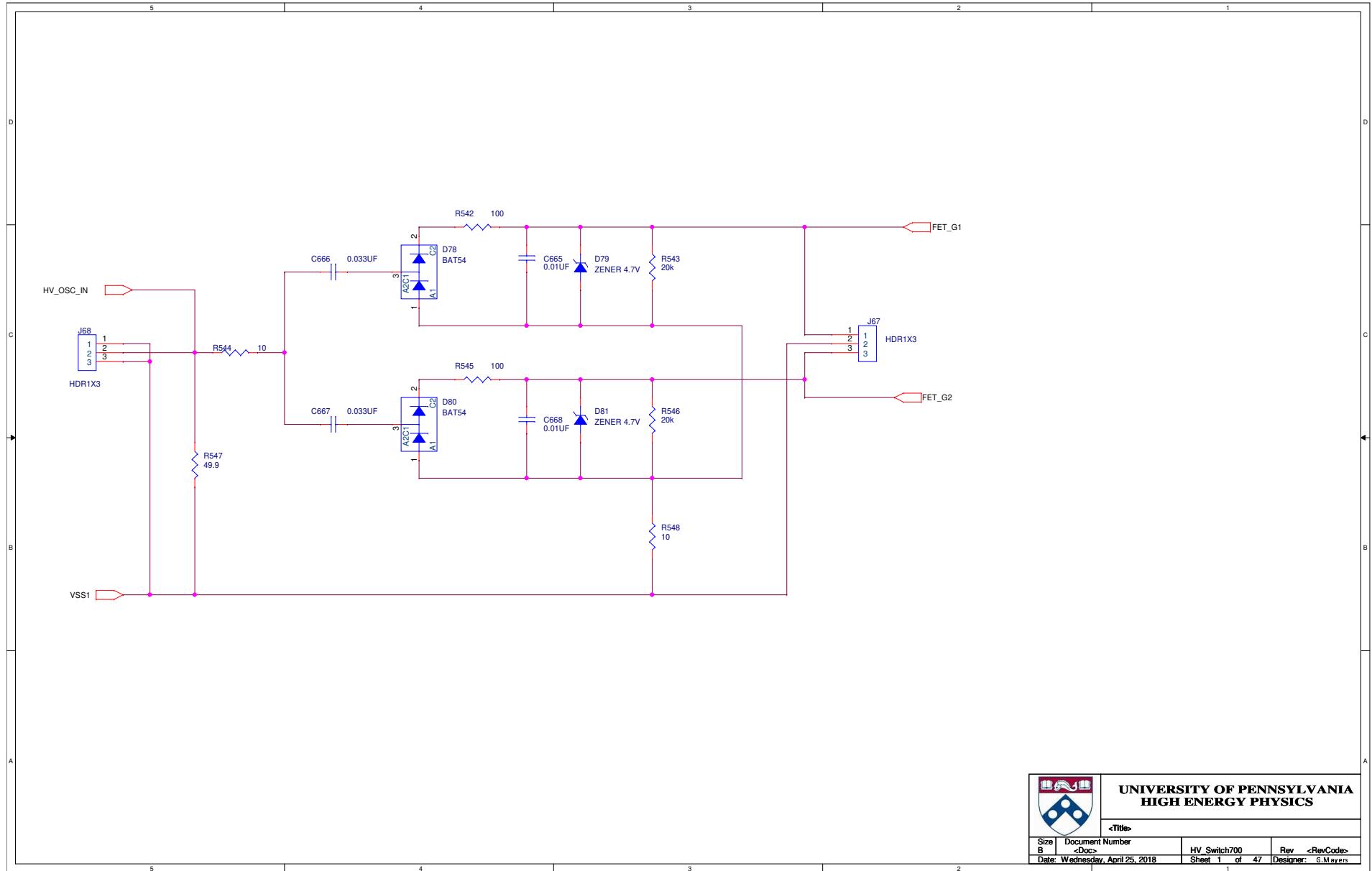
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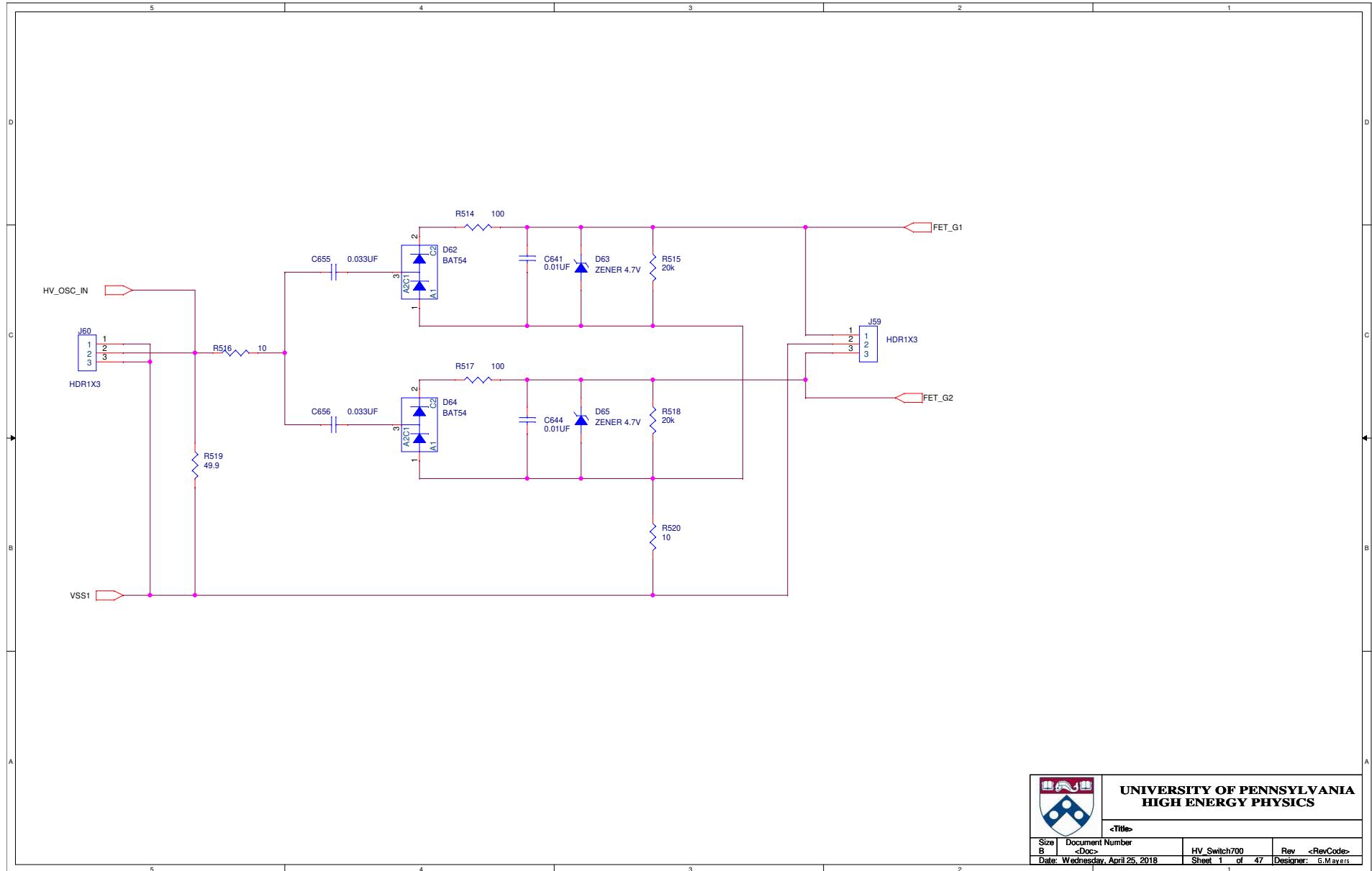
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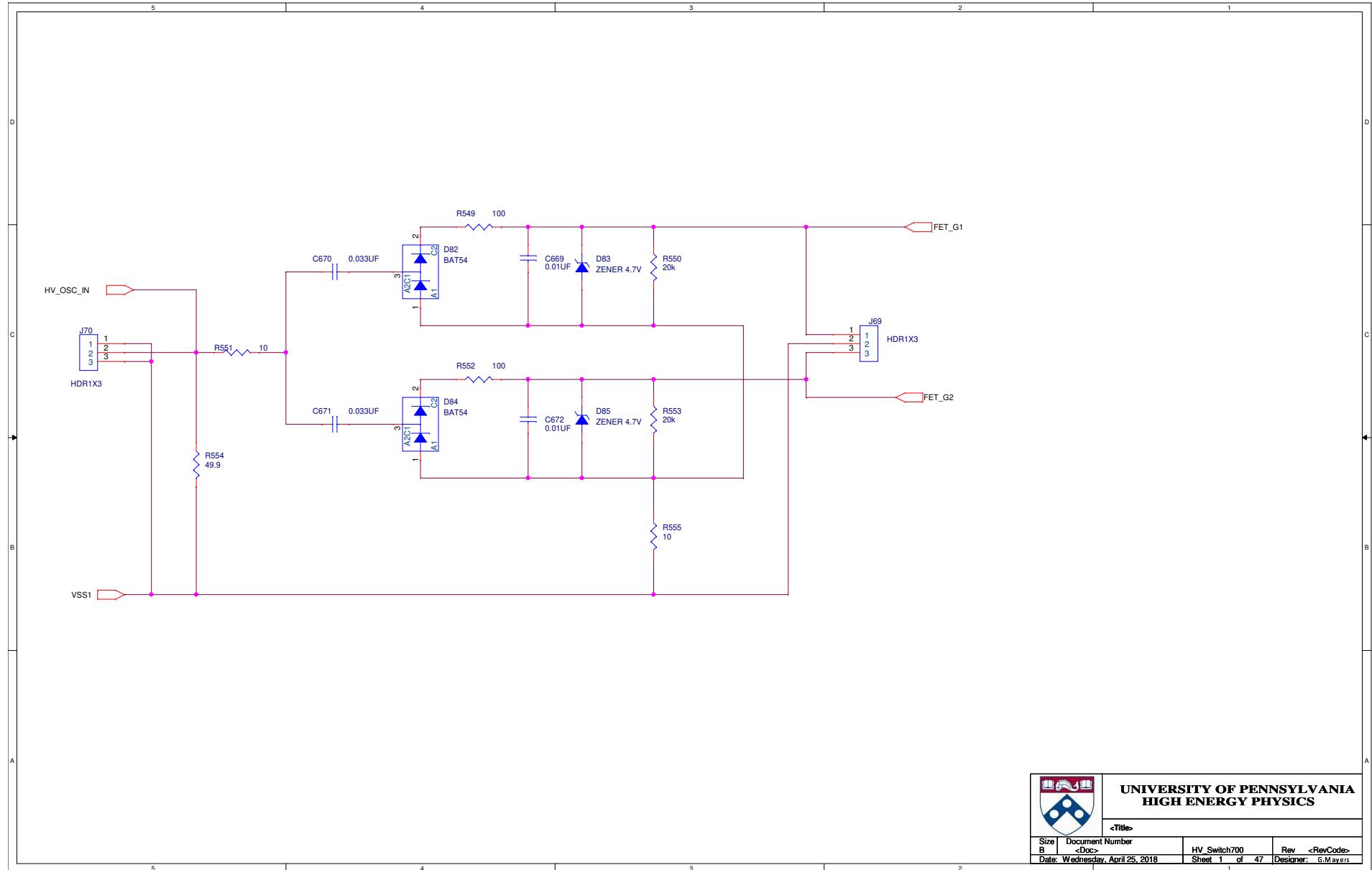
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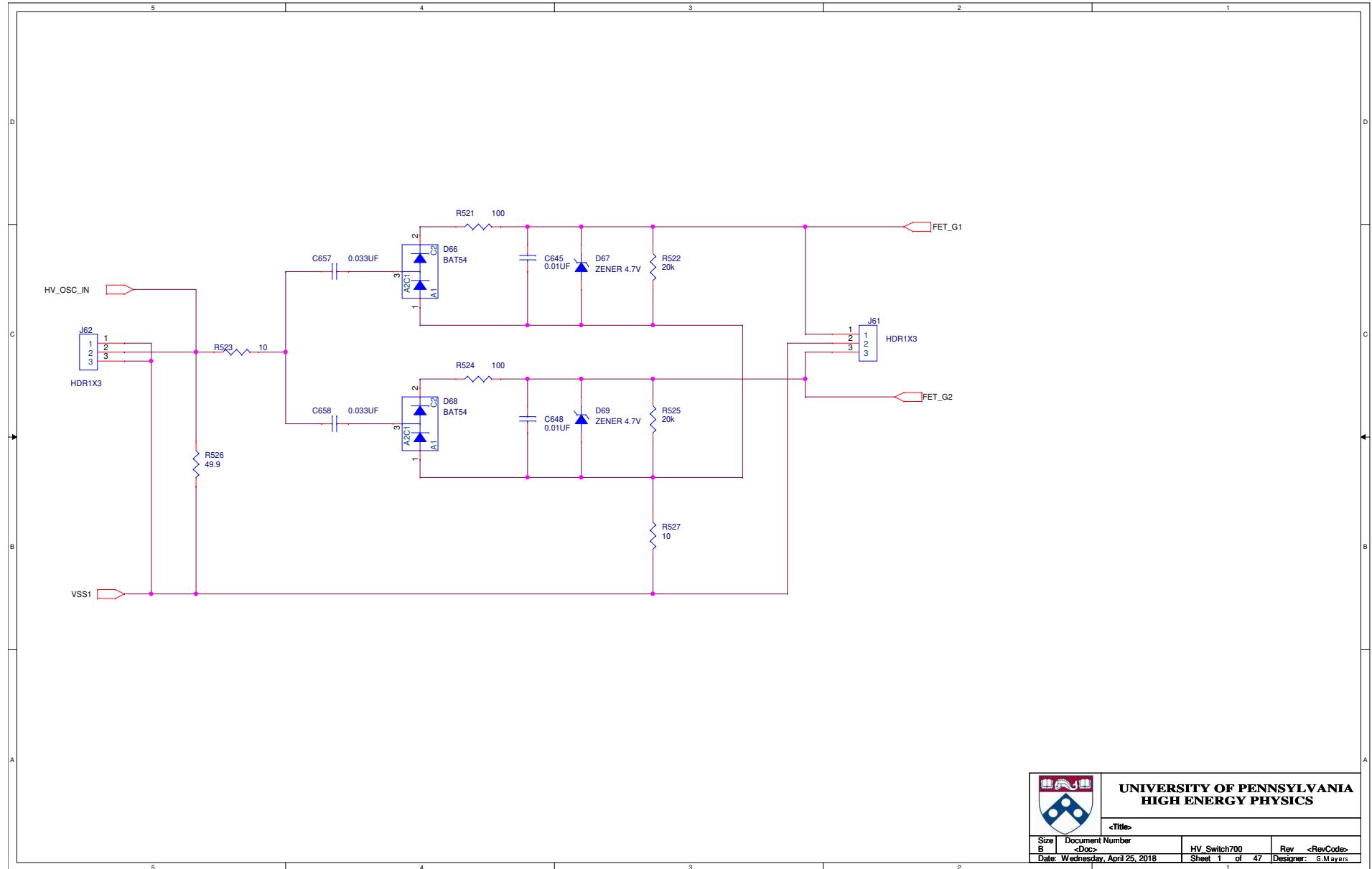


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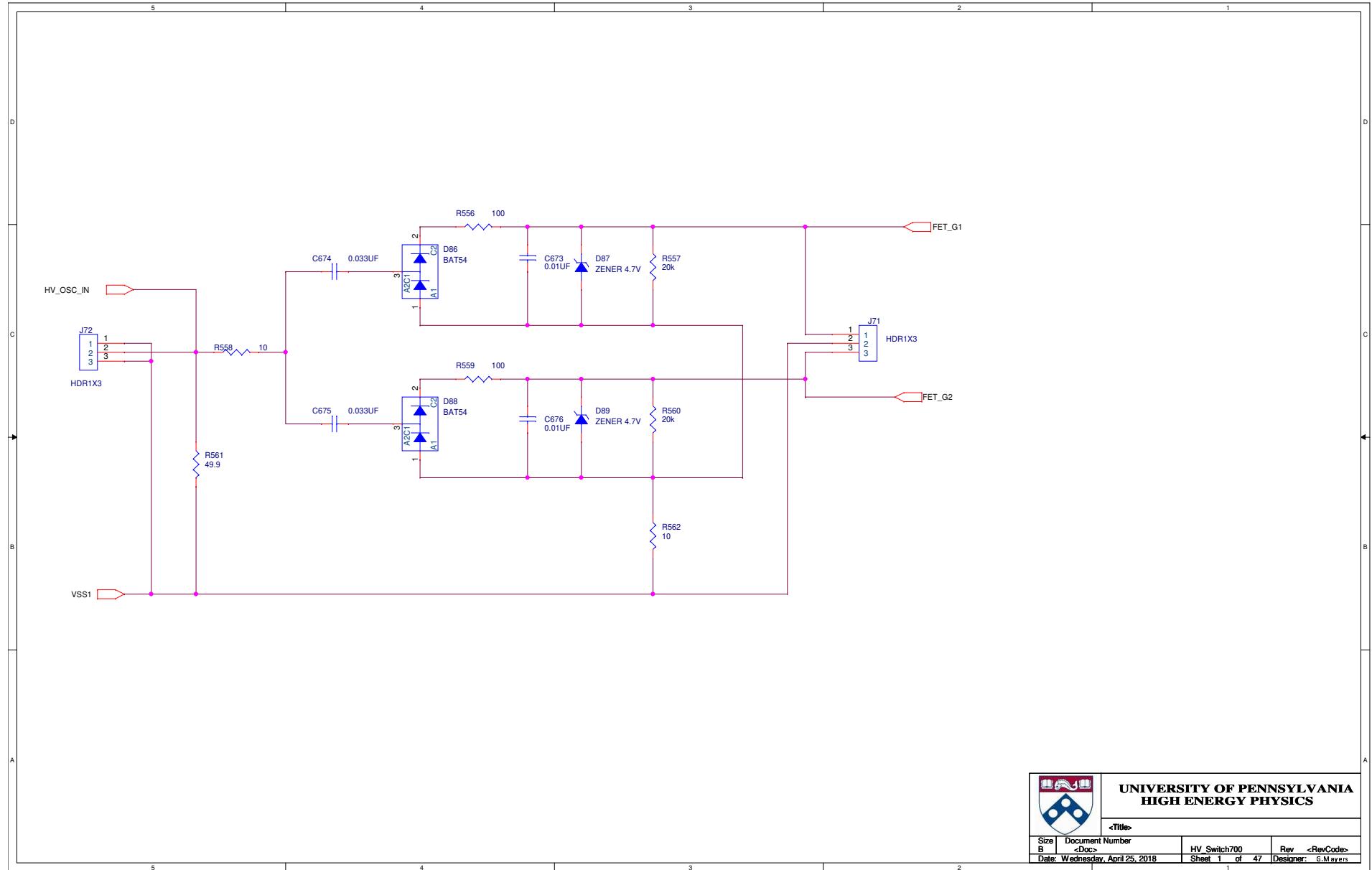






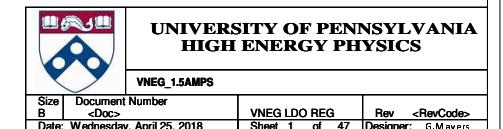
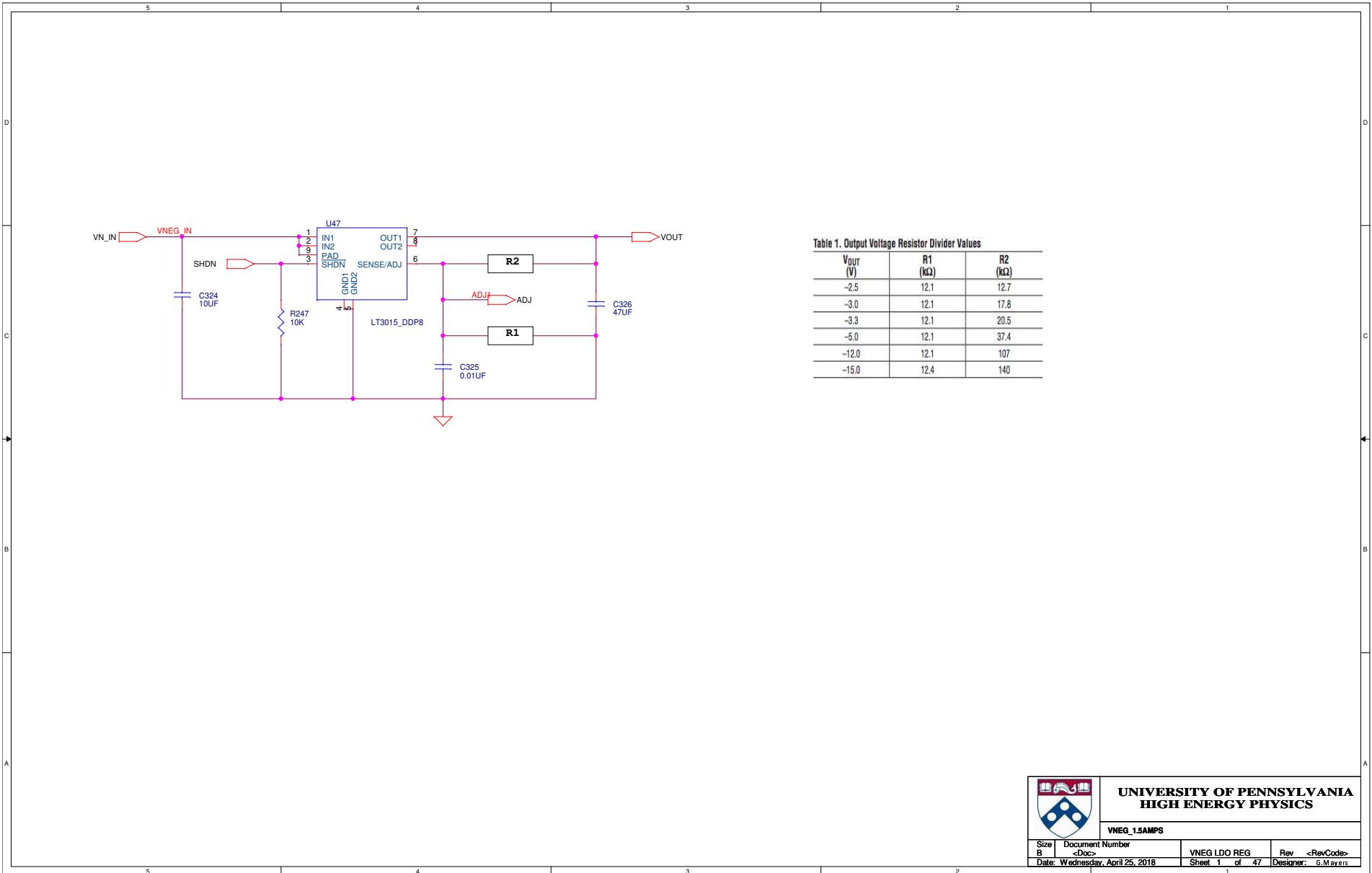
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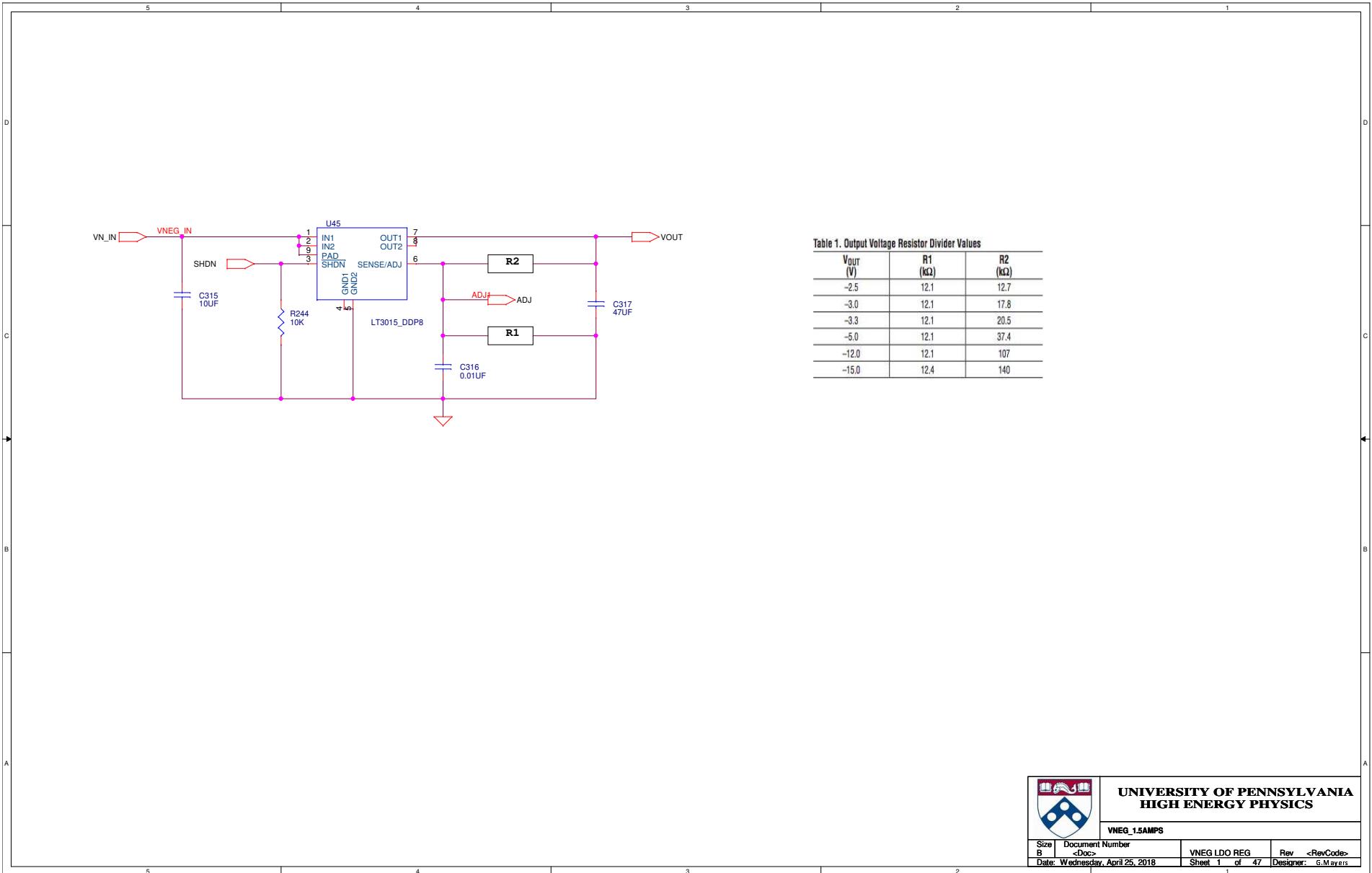
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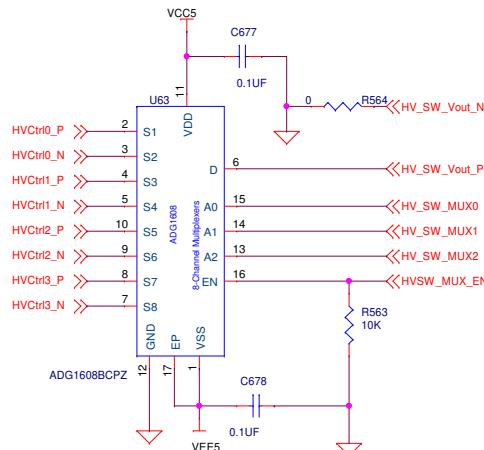
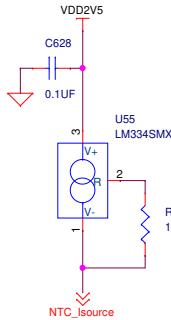
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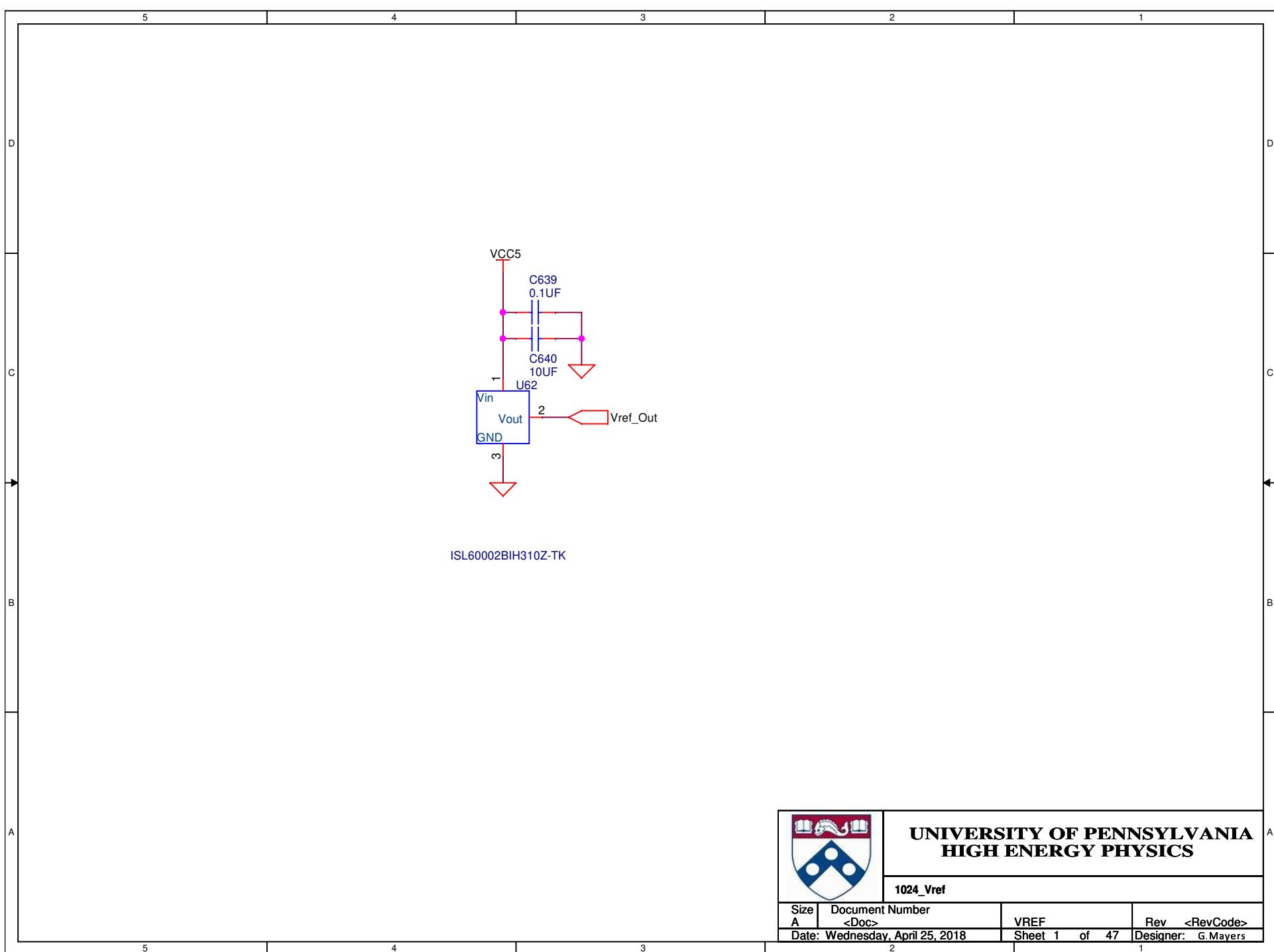


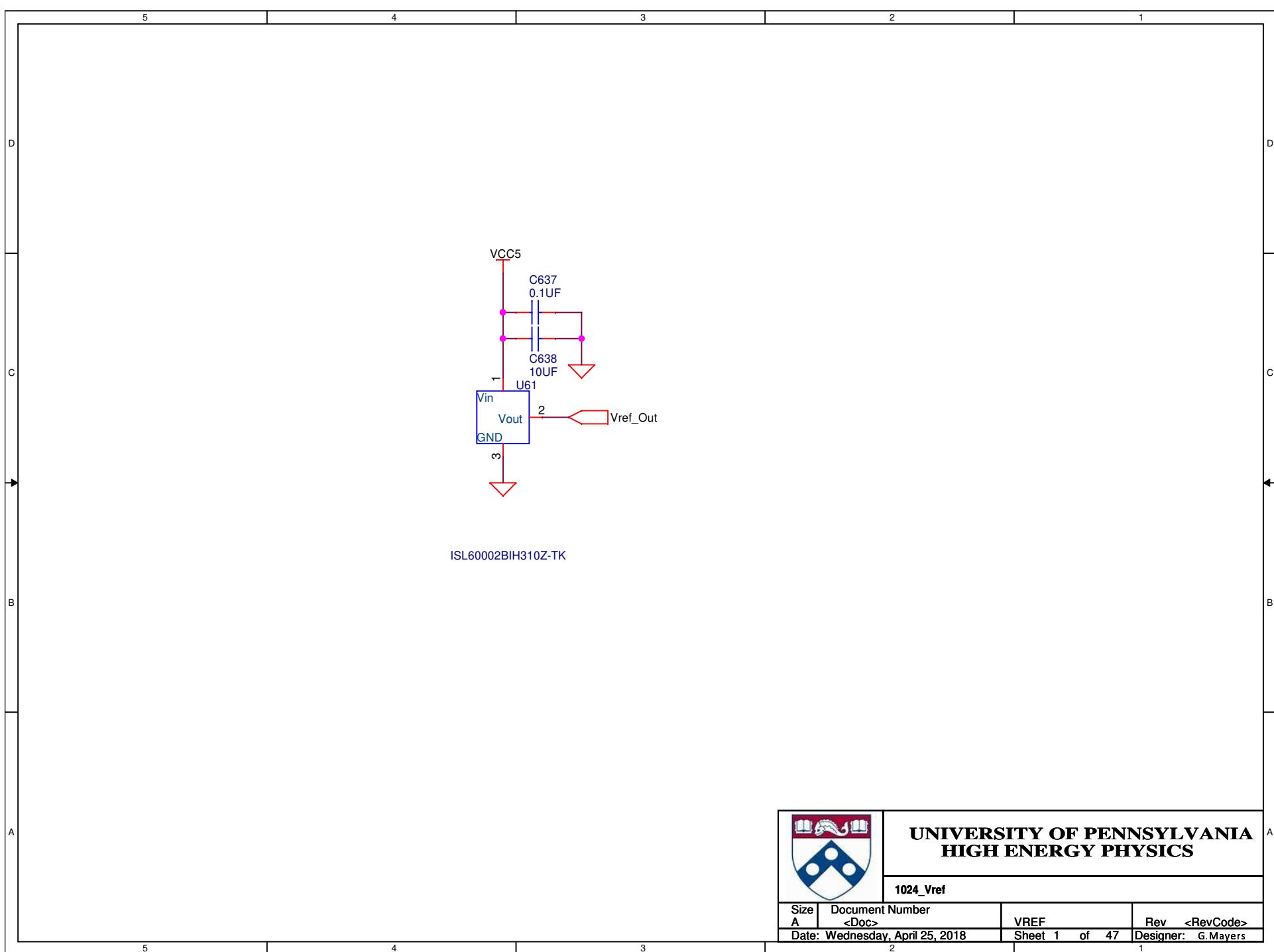
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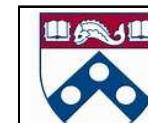
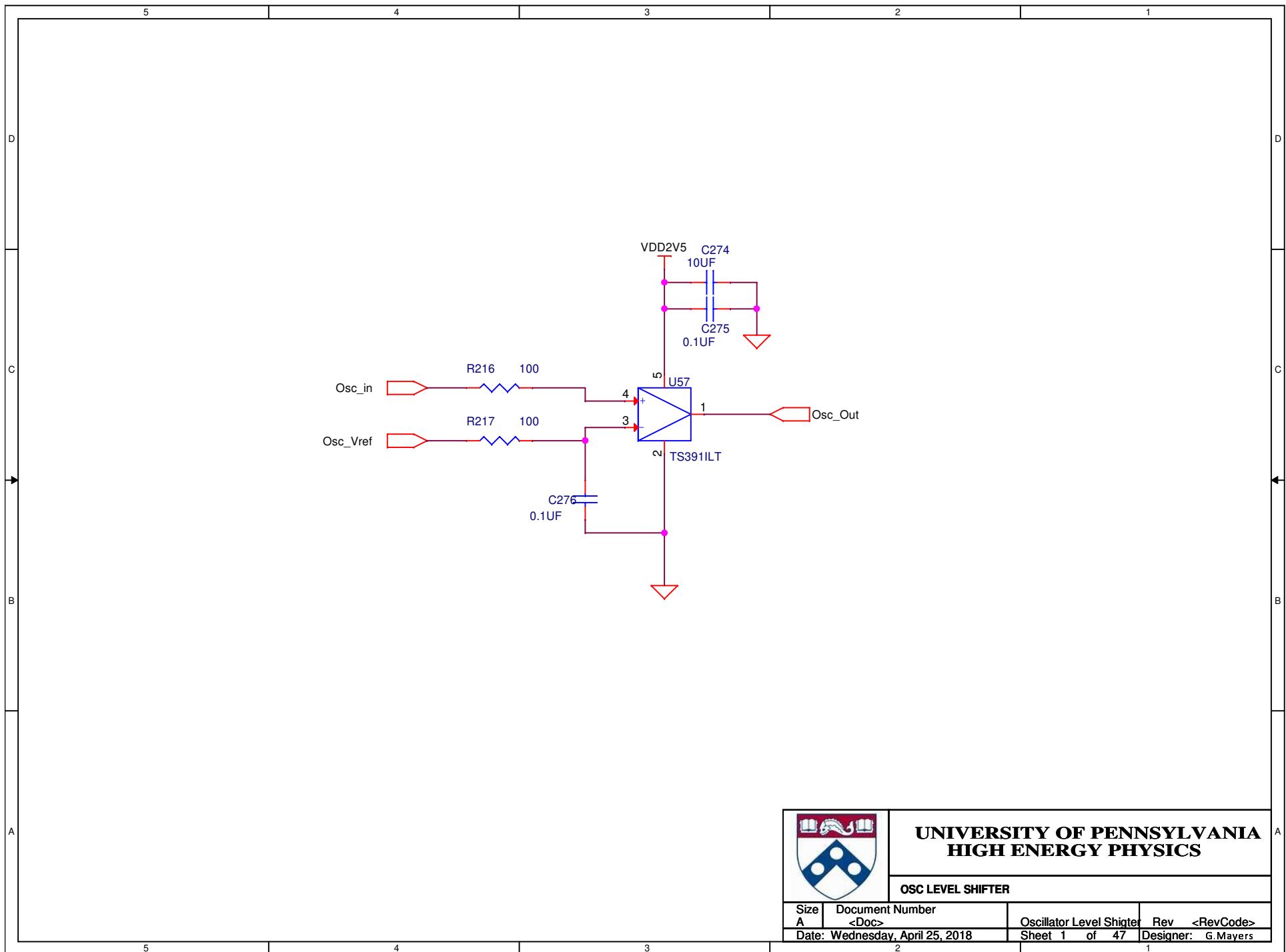


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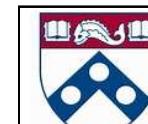
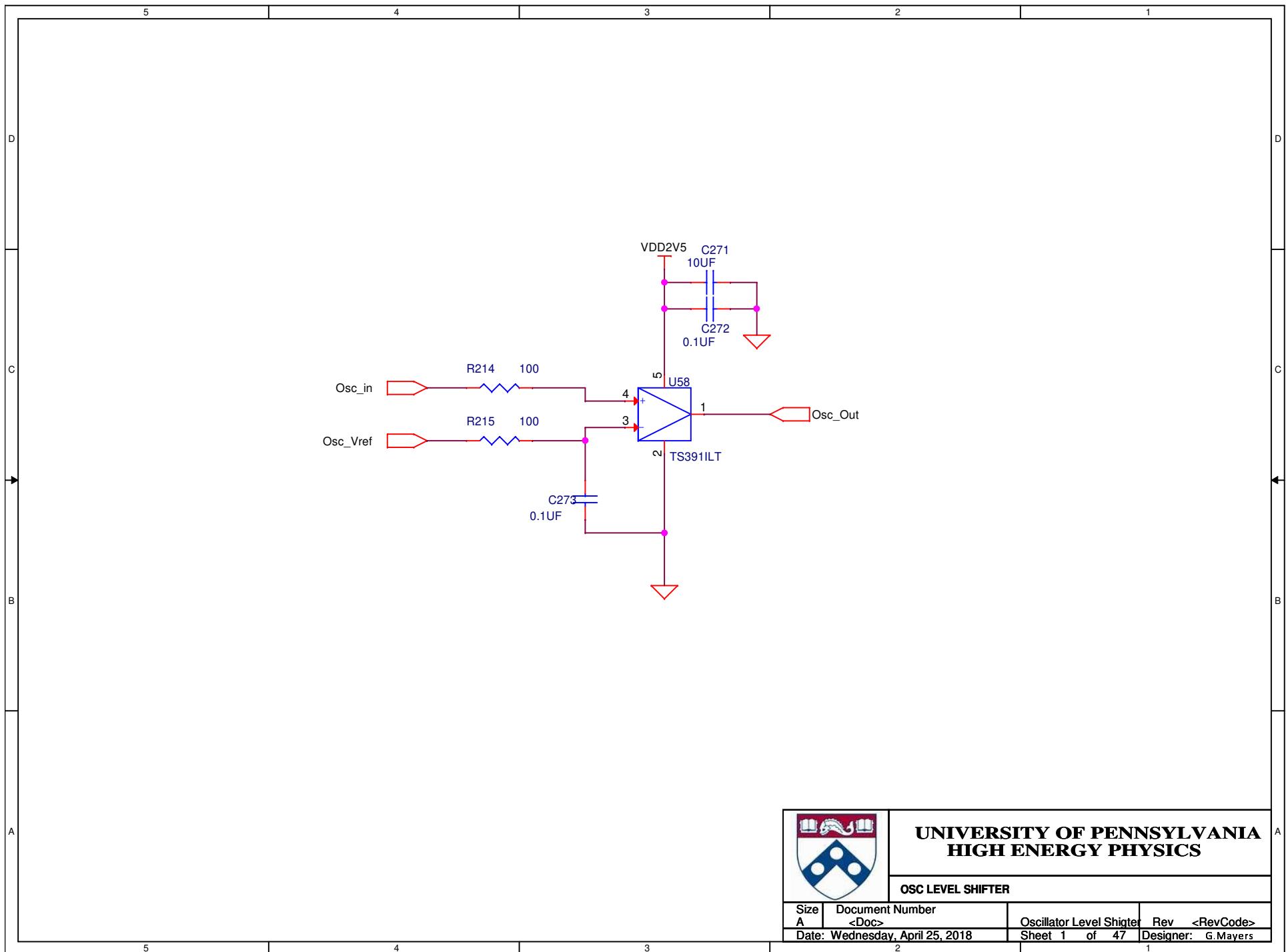
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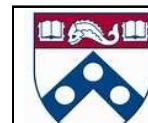
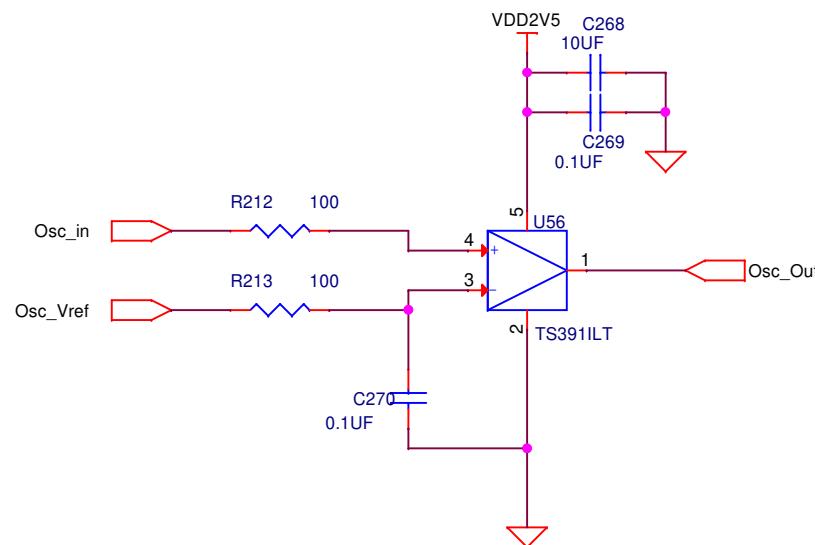
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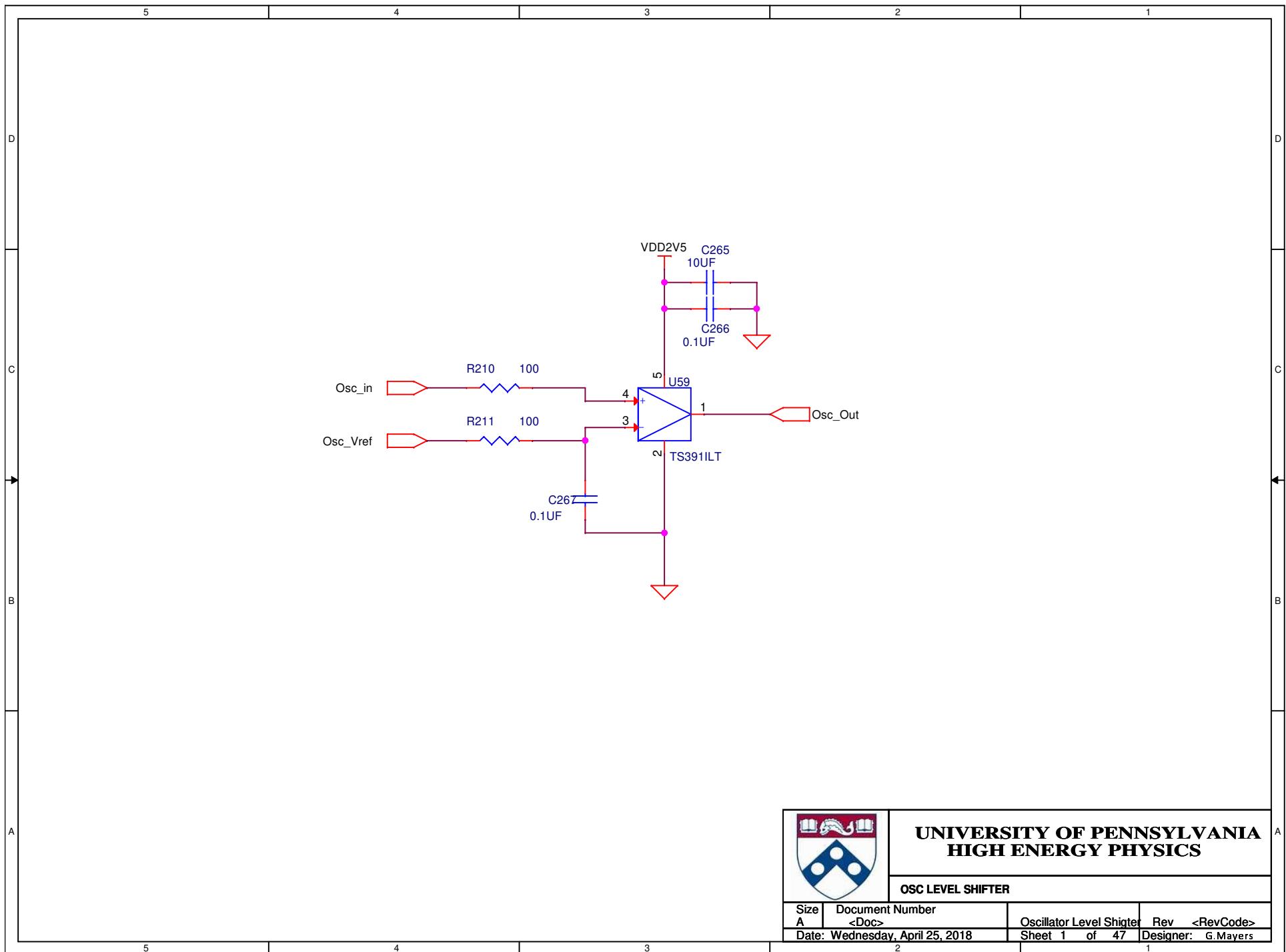
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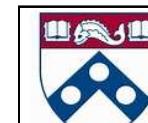
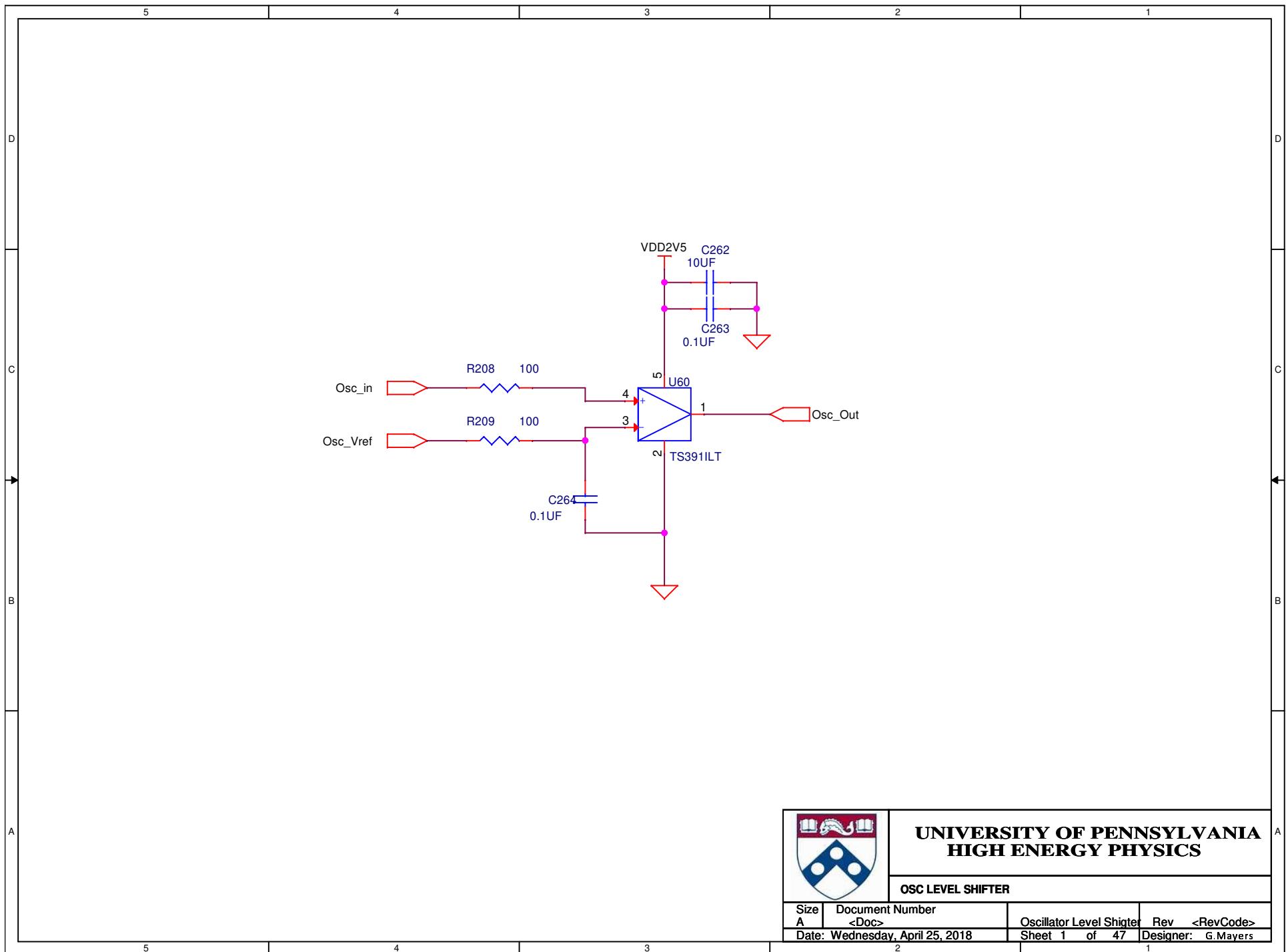
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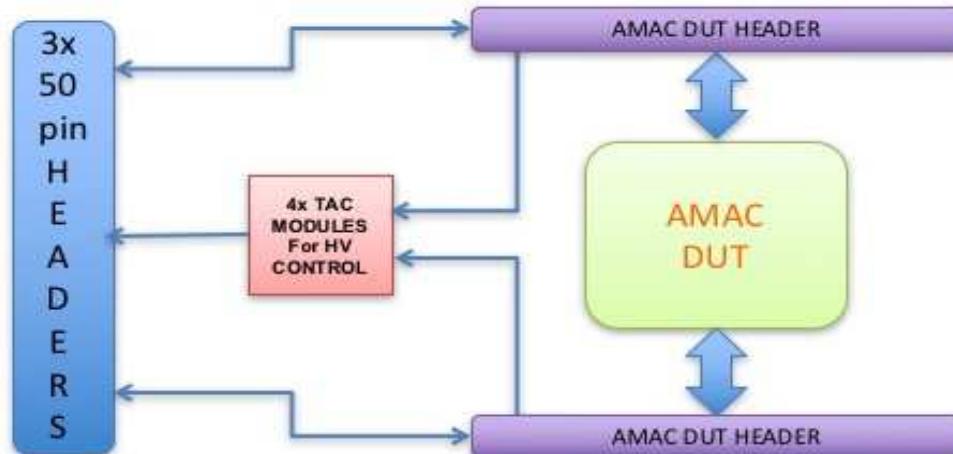


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## AMAC CARRIER AND DUT BOARDS

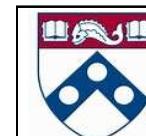
D  
3 50 POSITION HEADER  
CONNECTOR 0.050(1.27mm)  
TO AMAC TEST & CONTROL  
BOARD



3/12/18

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2



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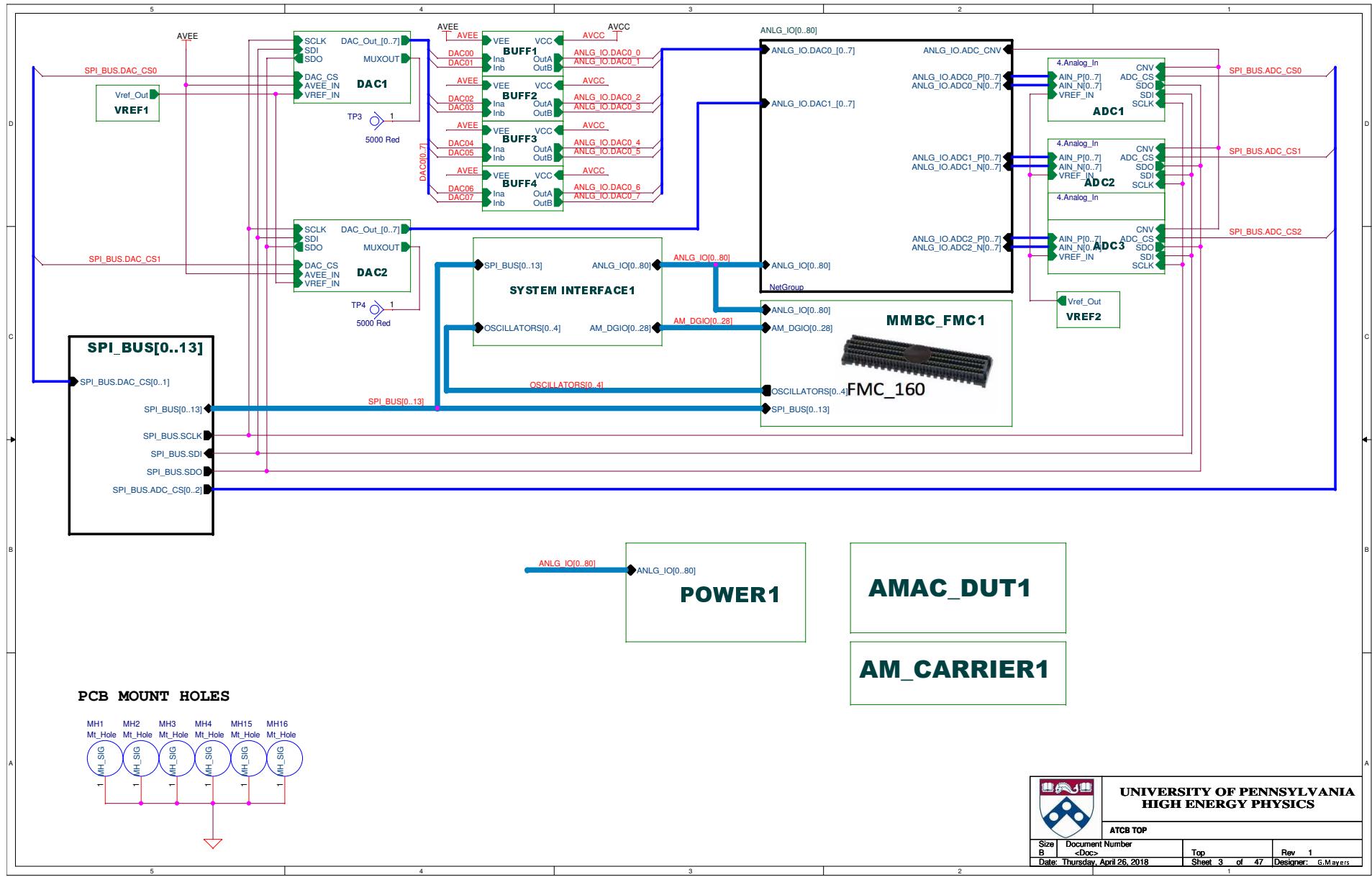
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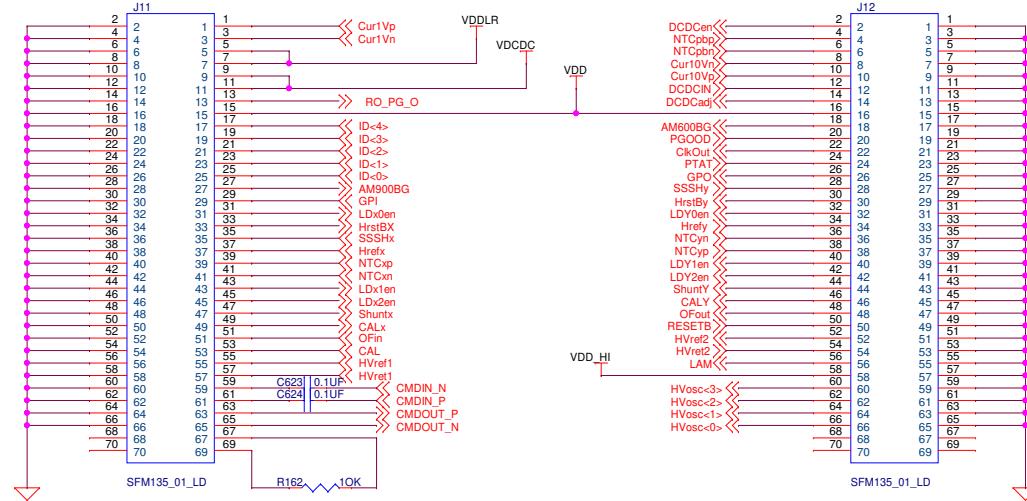
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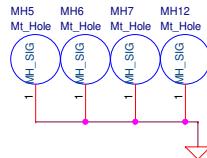
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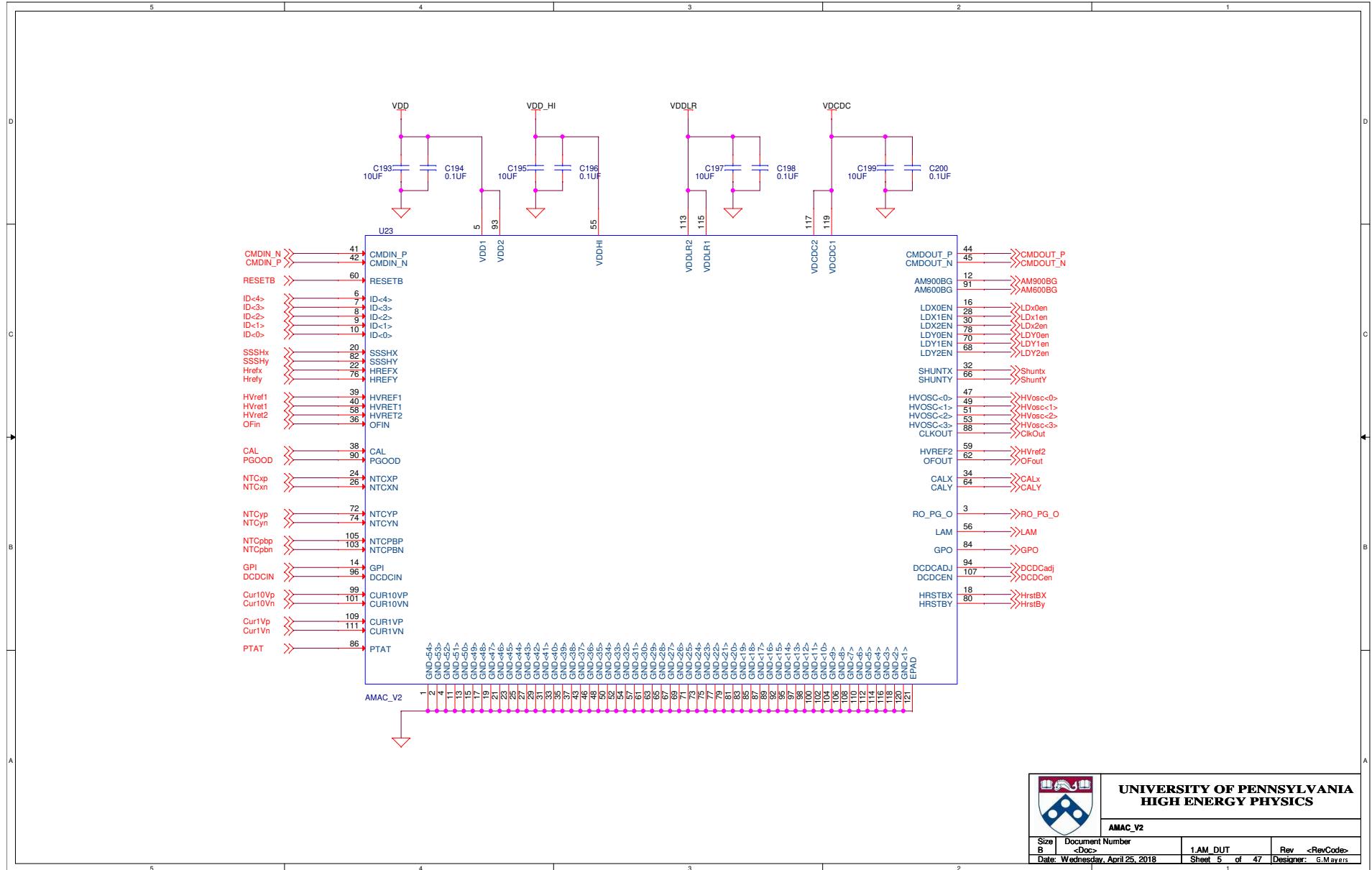


Review foot prints, Vddhv, vdd etc

#### PCB MOUNT HOLES

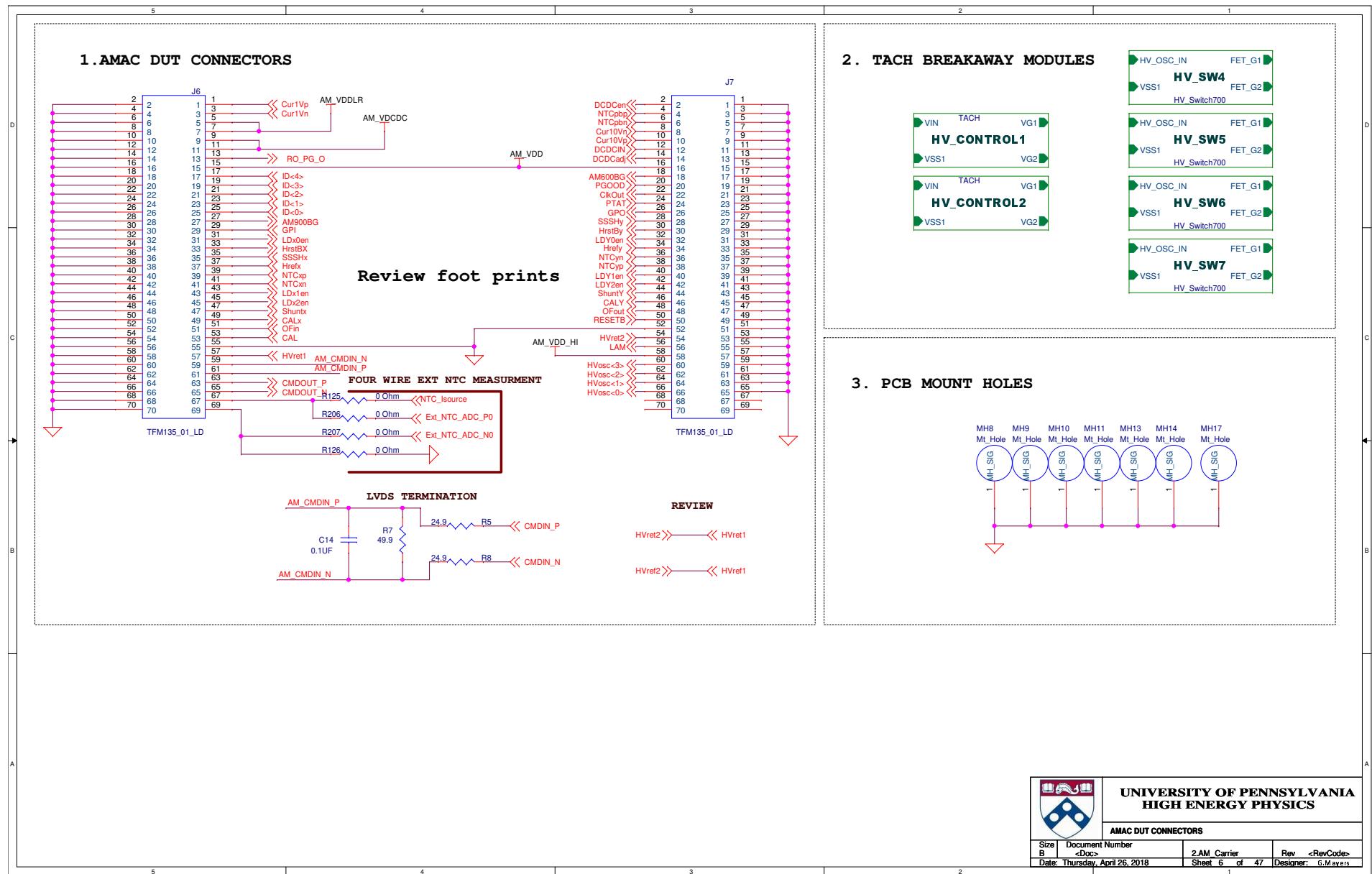


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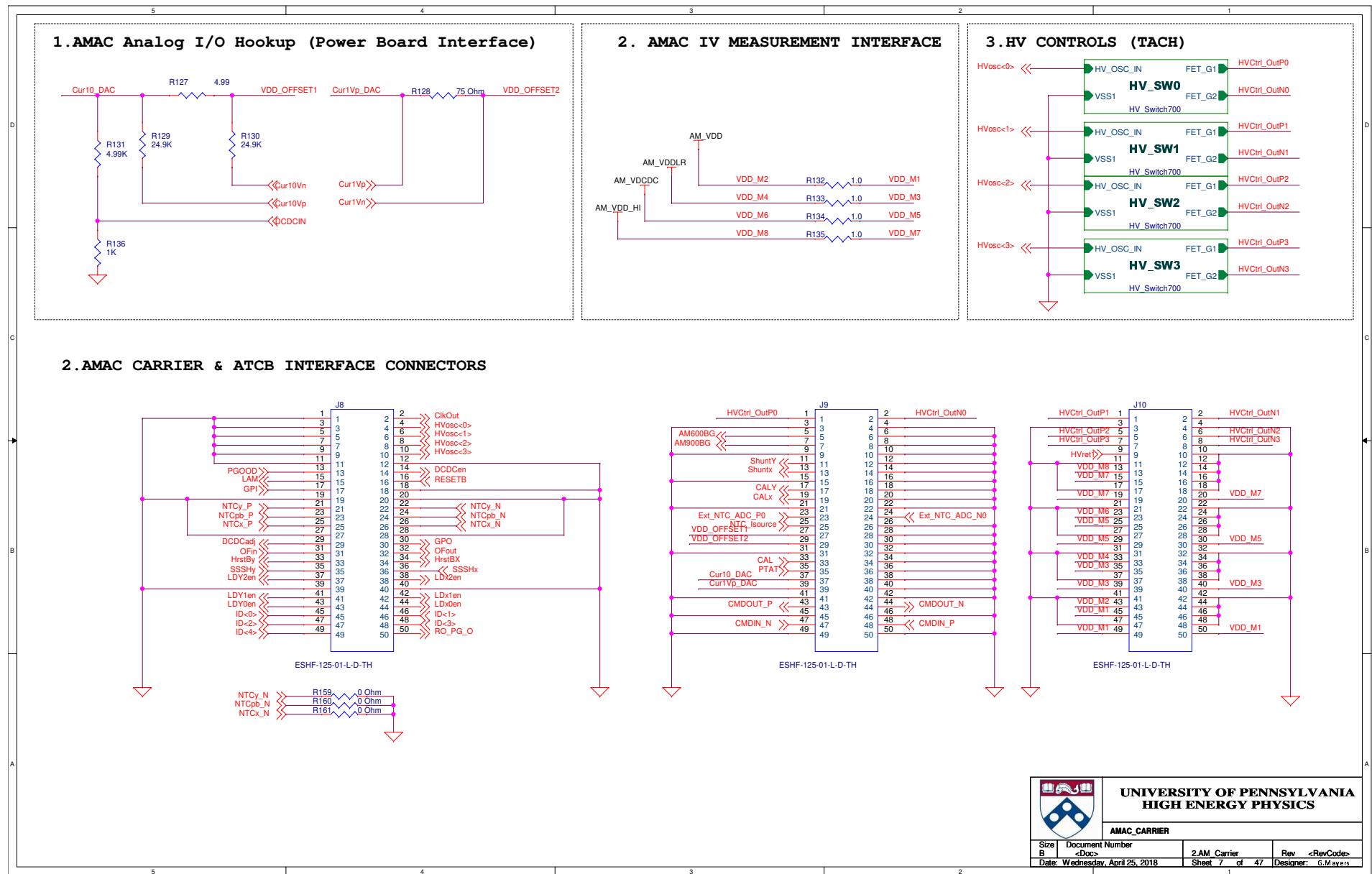


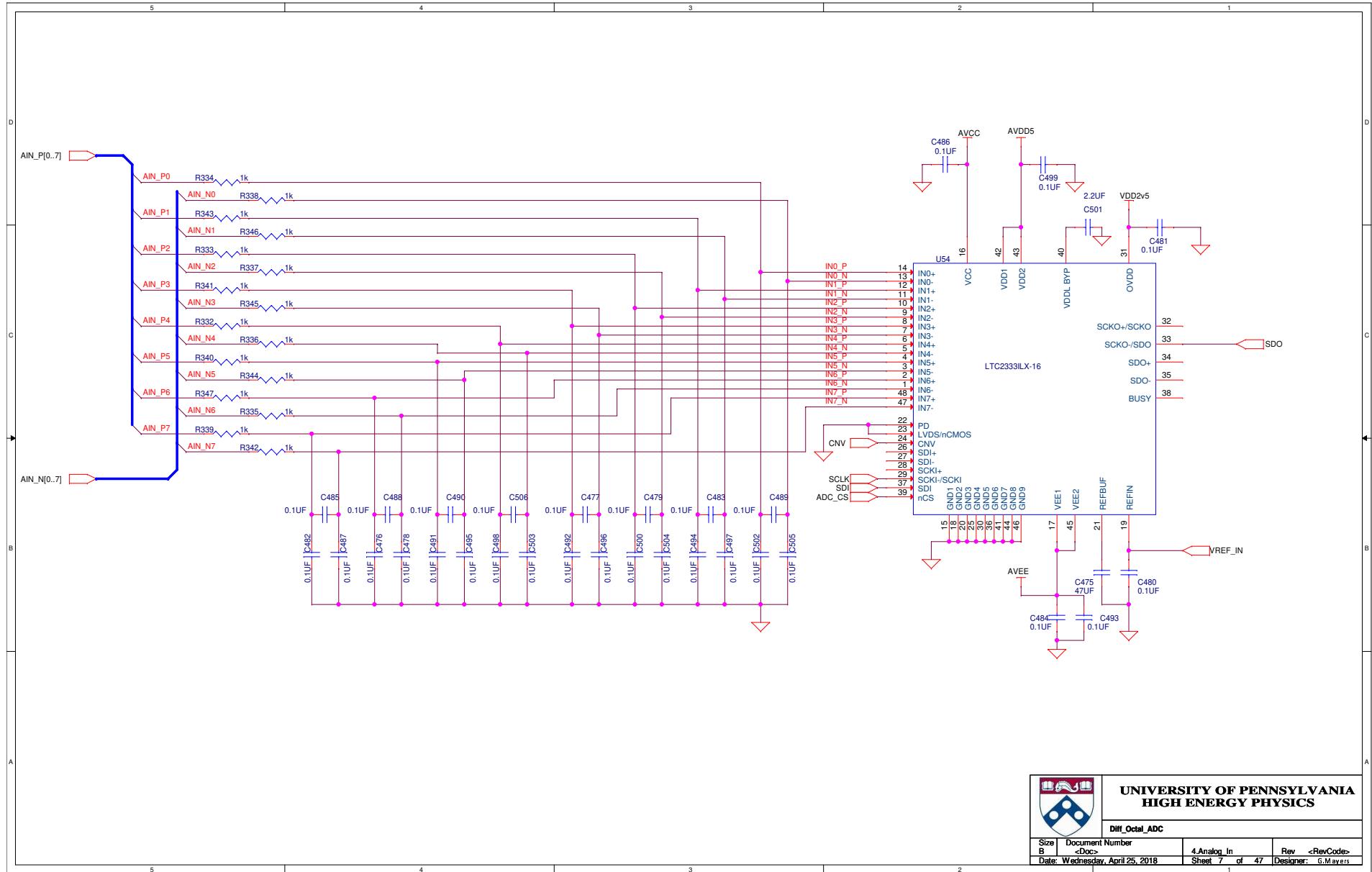
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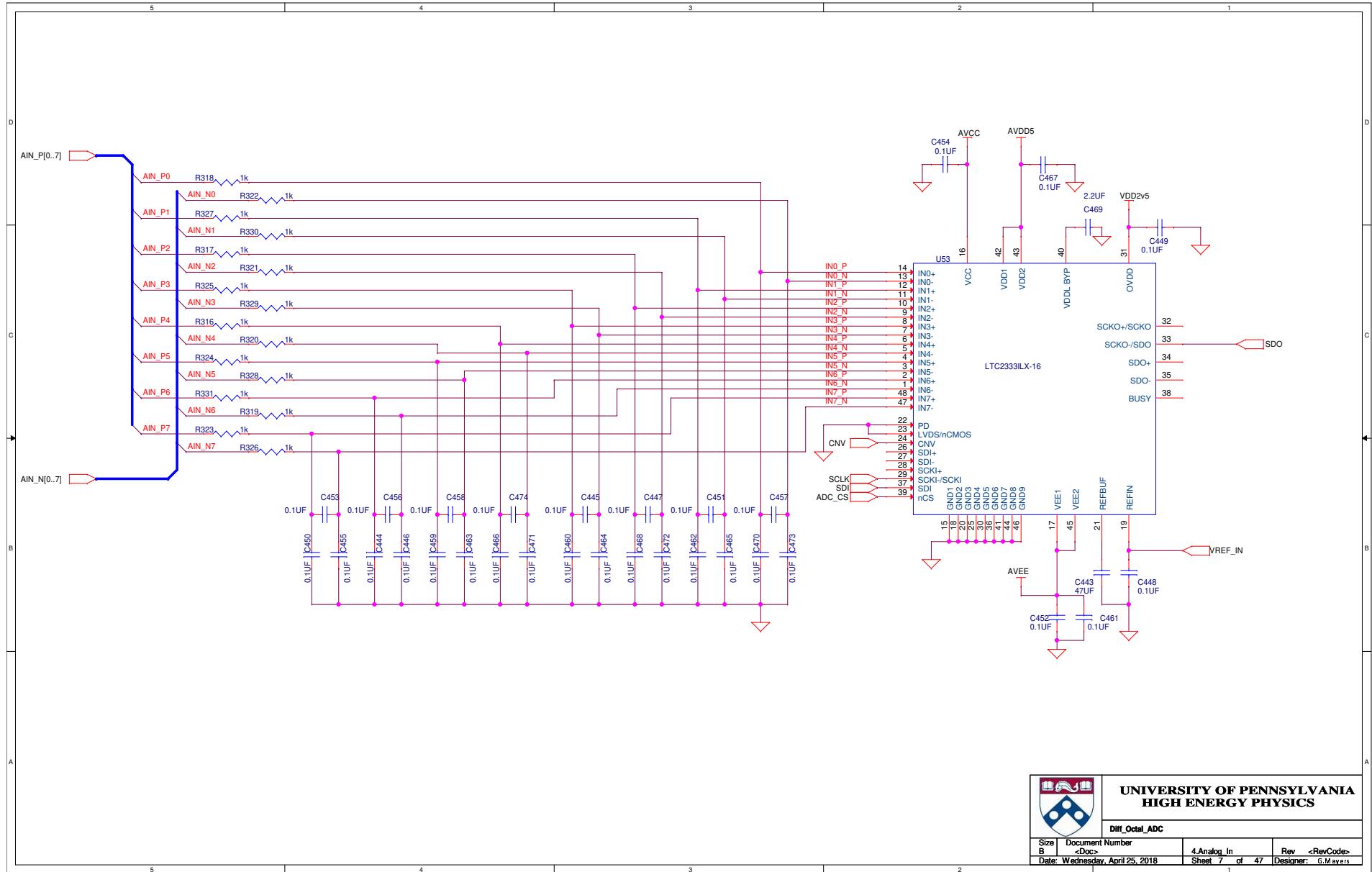
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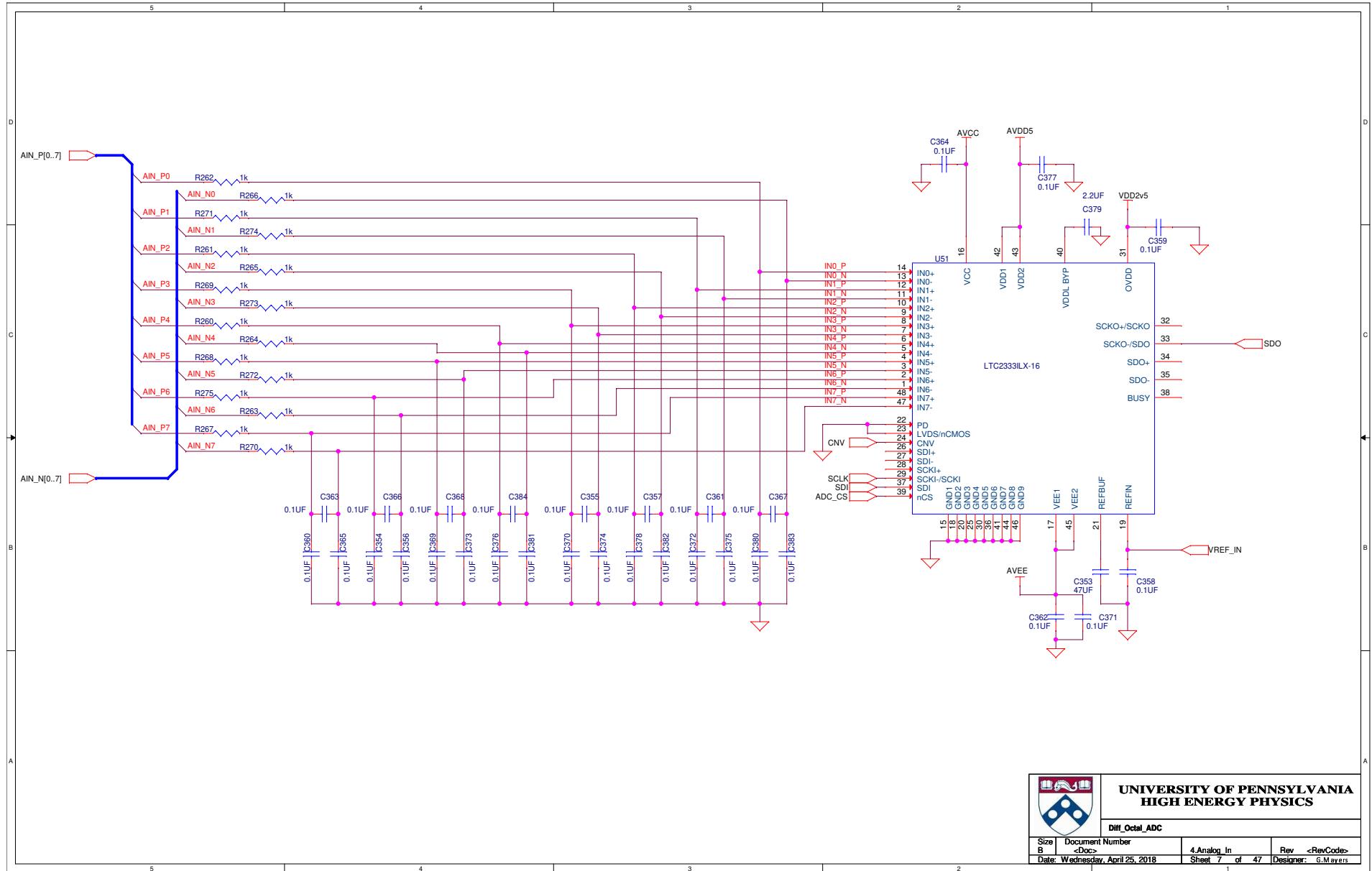


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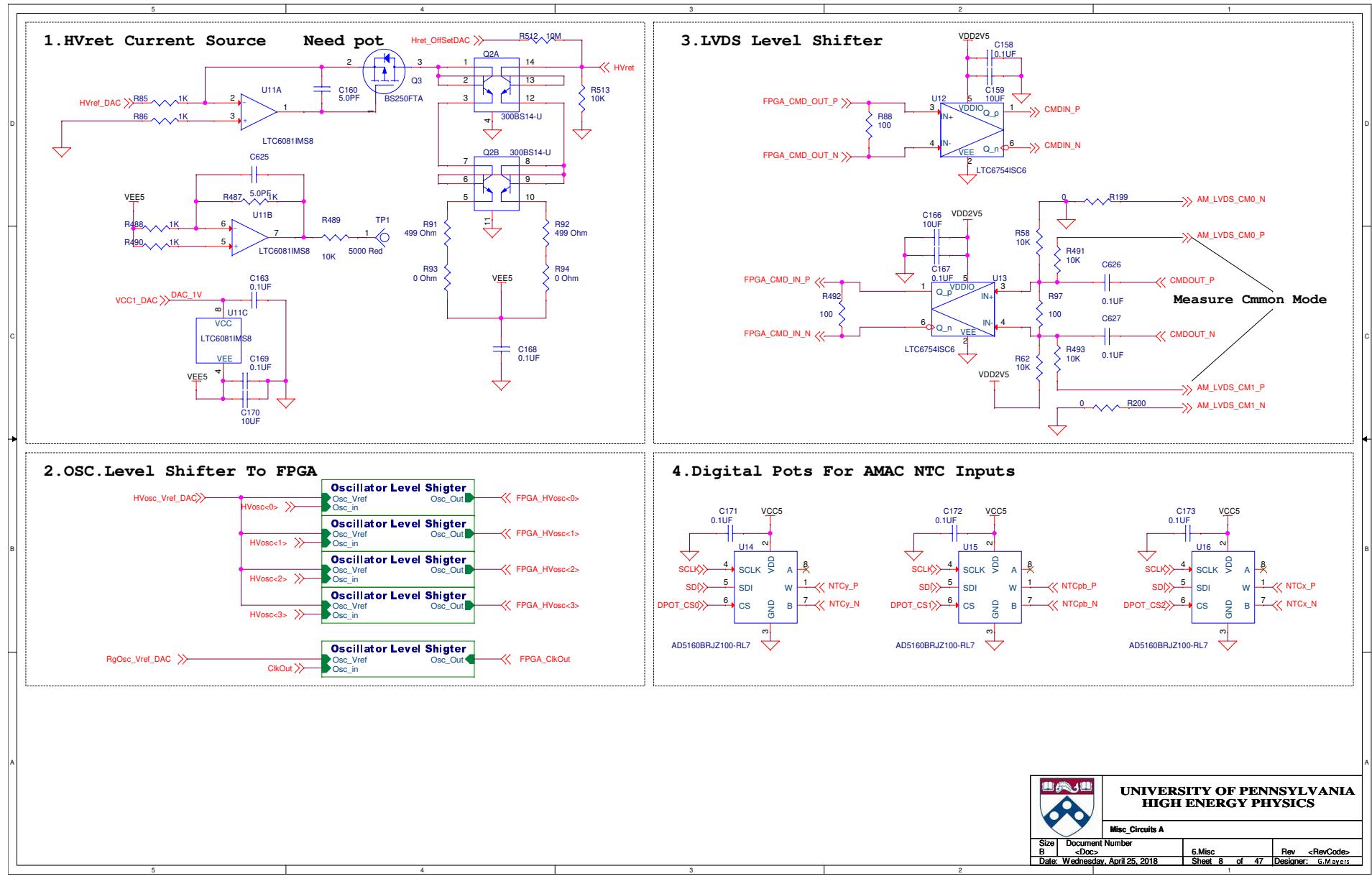




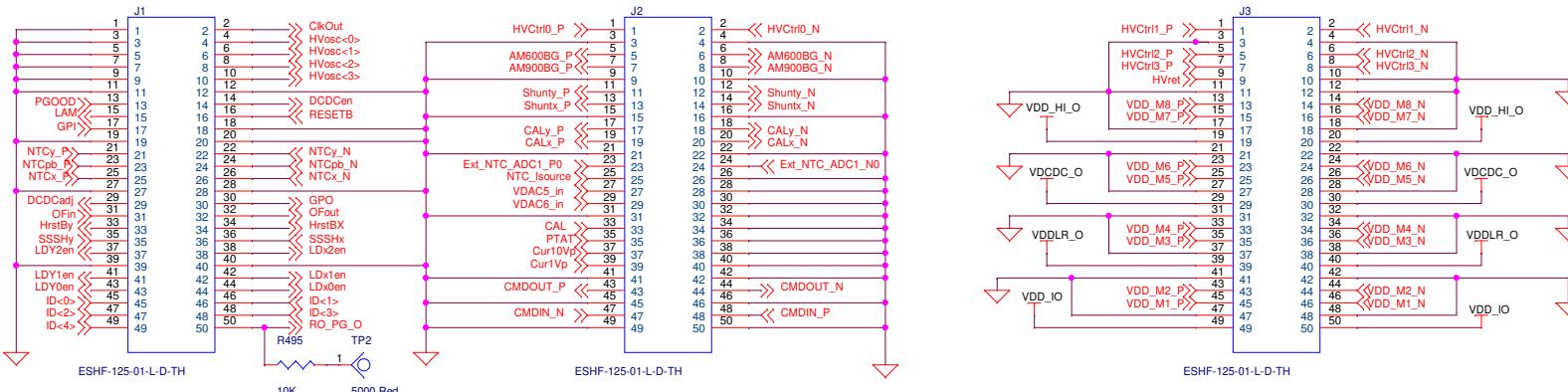
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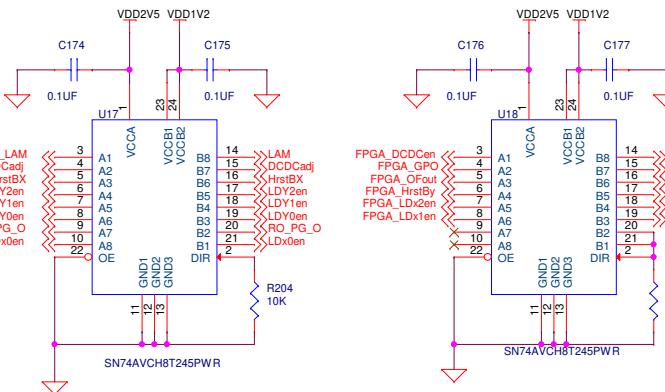
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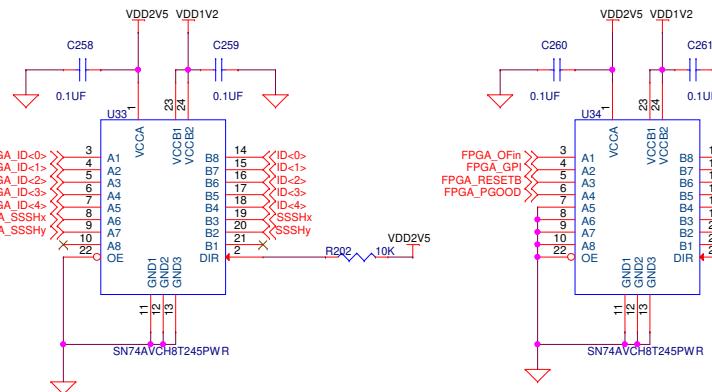
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## 2. AMAC To FPGA DIO Level Translators



## 3. FPGA To AMAC DIO Level Translators



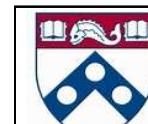
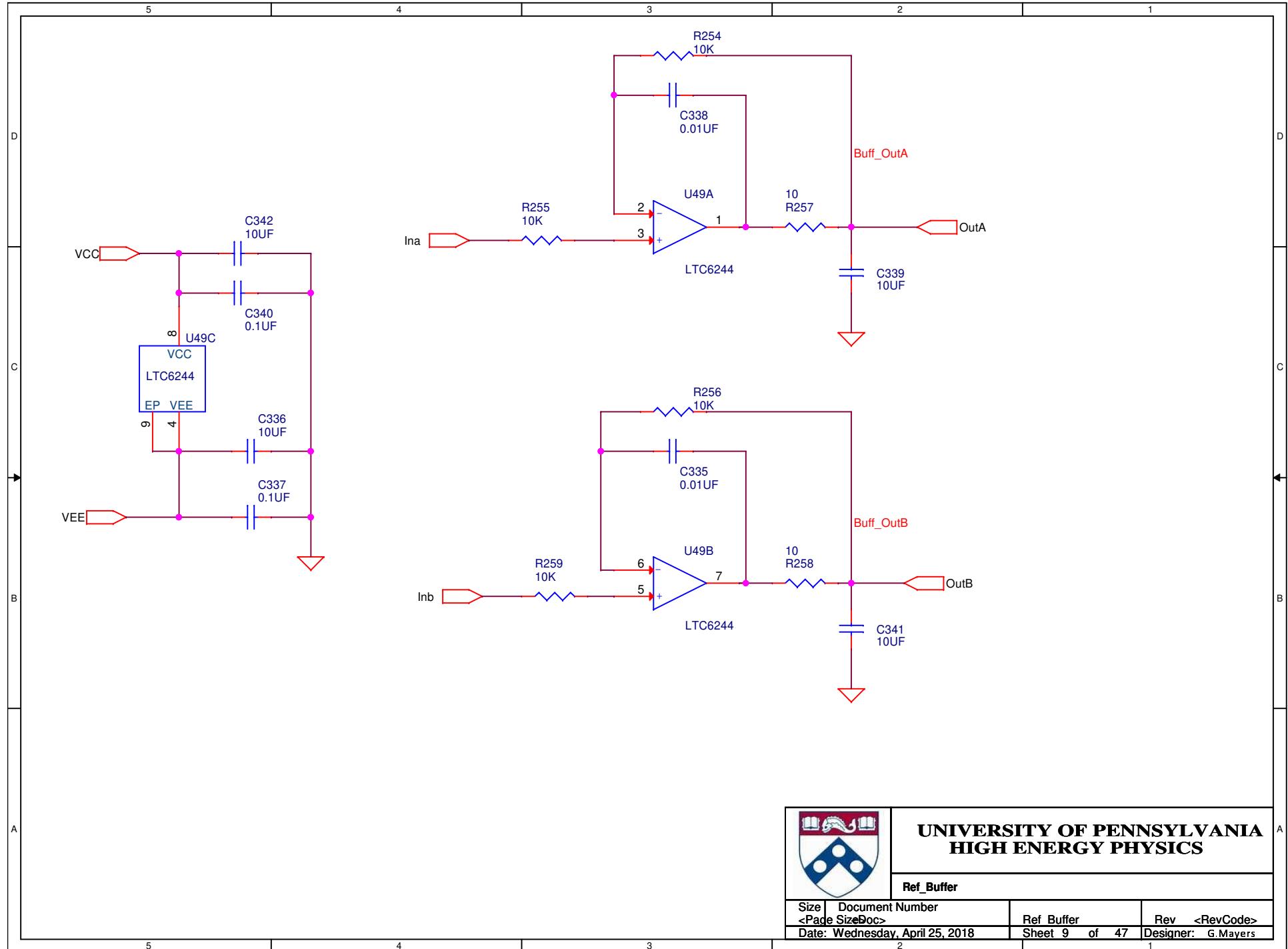
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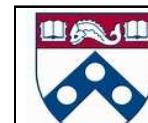
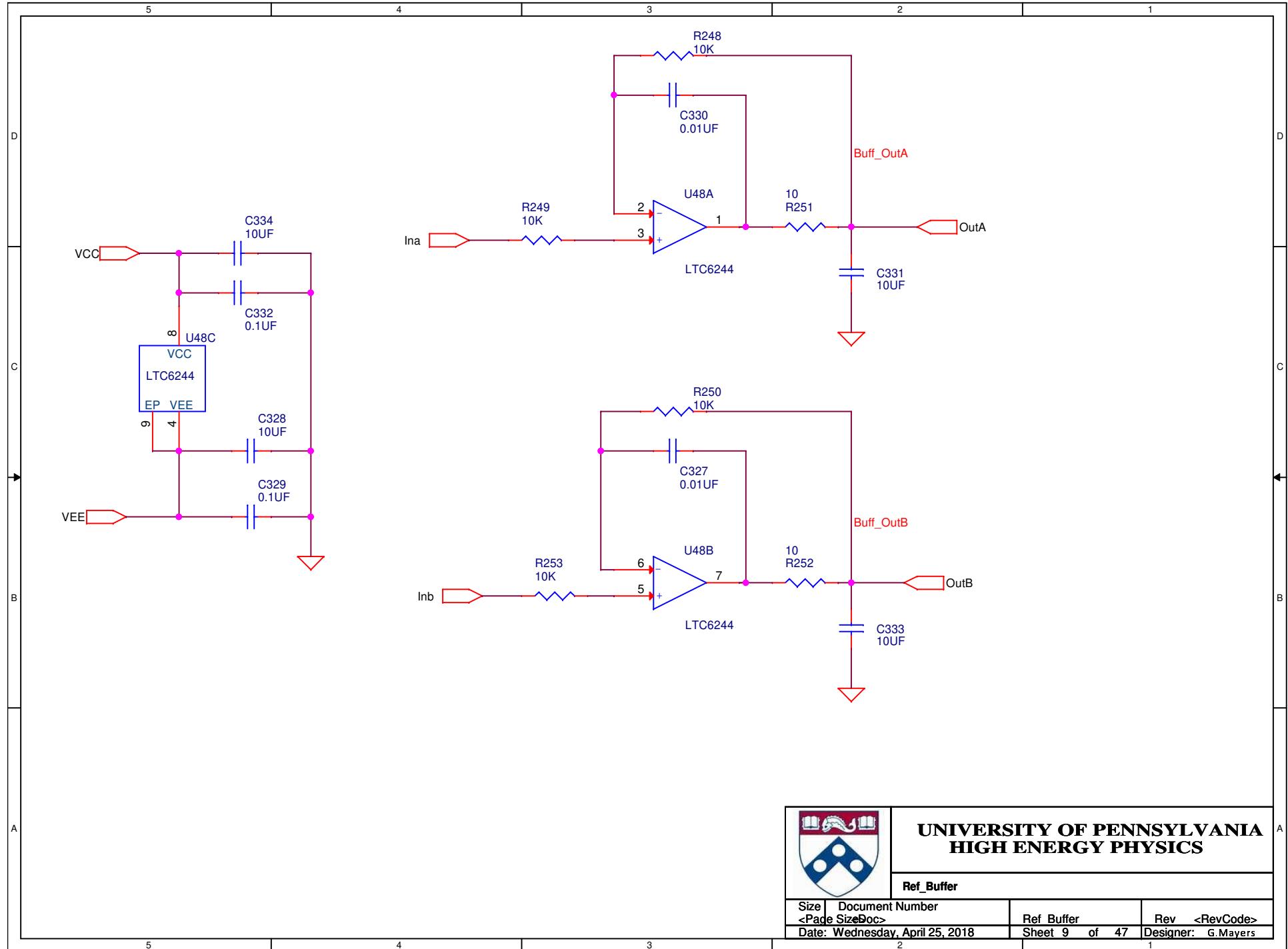
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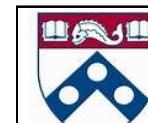
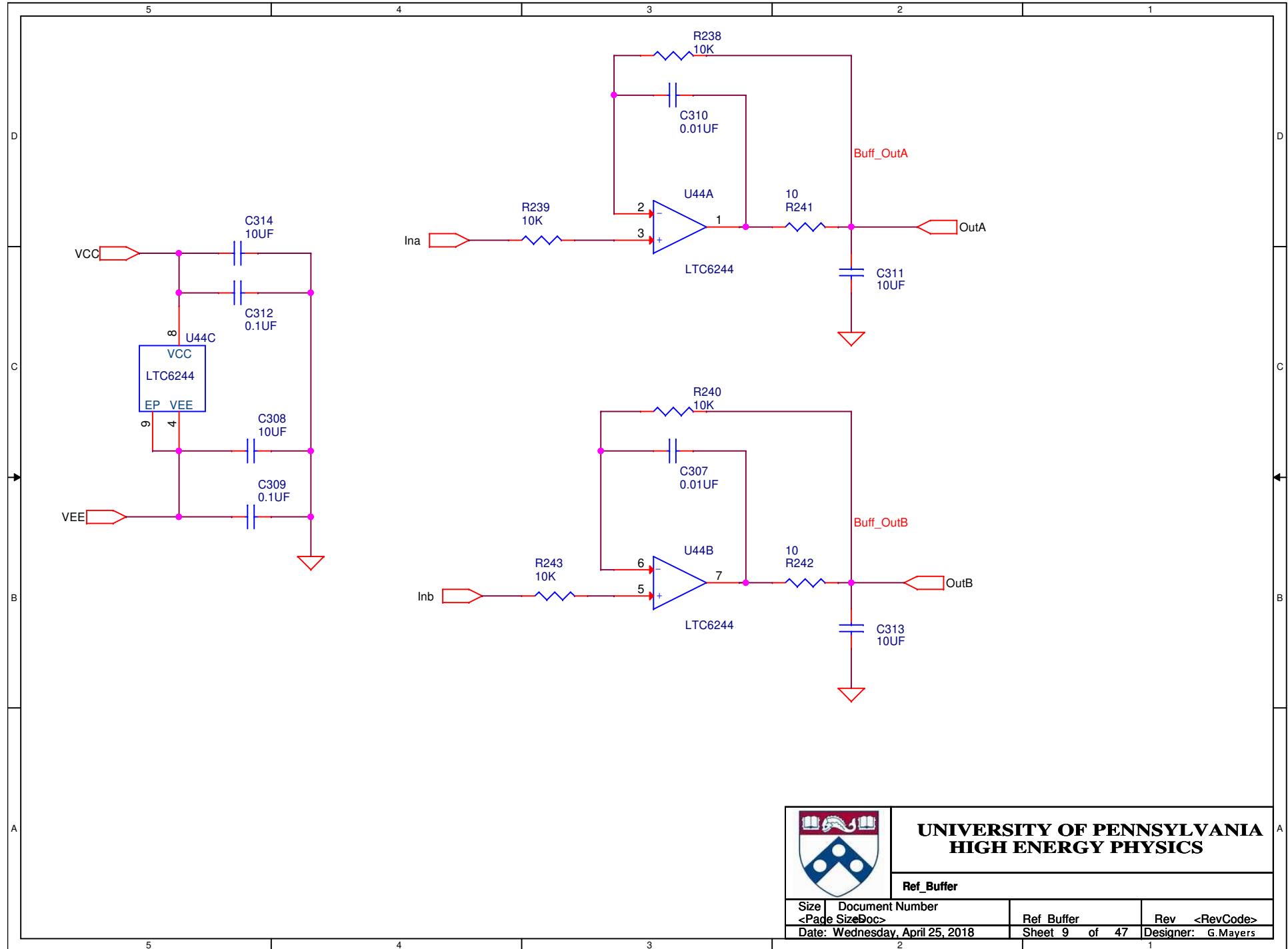
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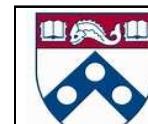
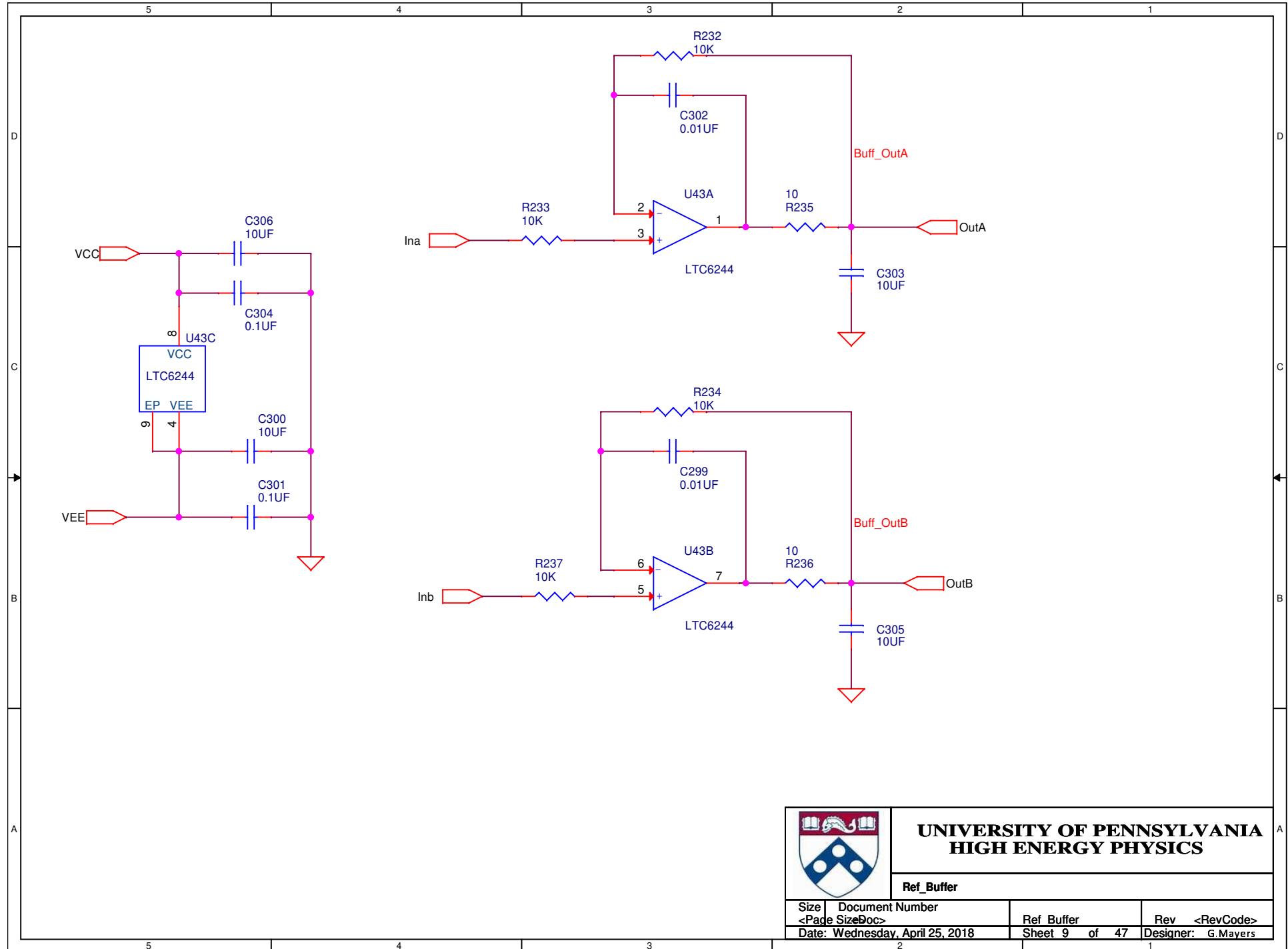
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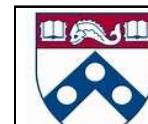
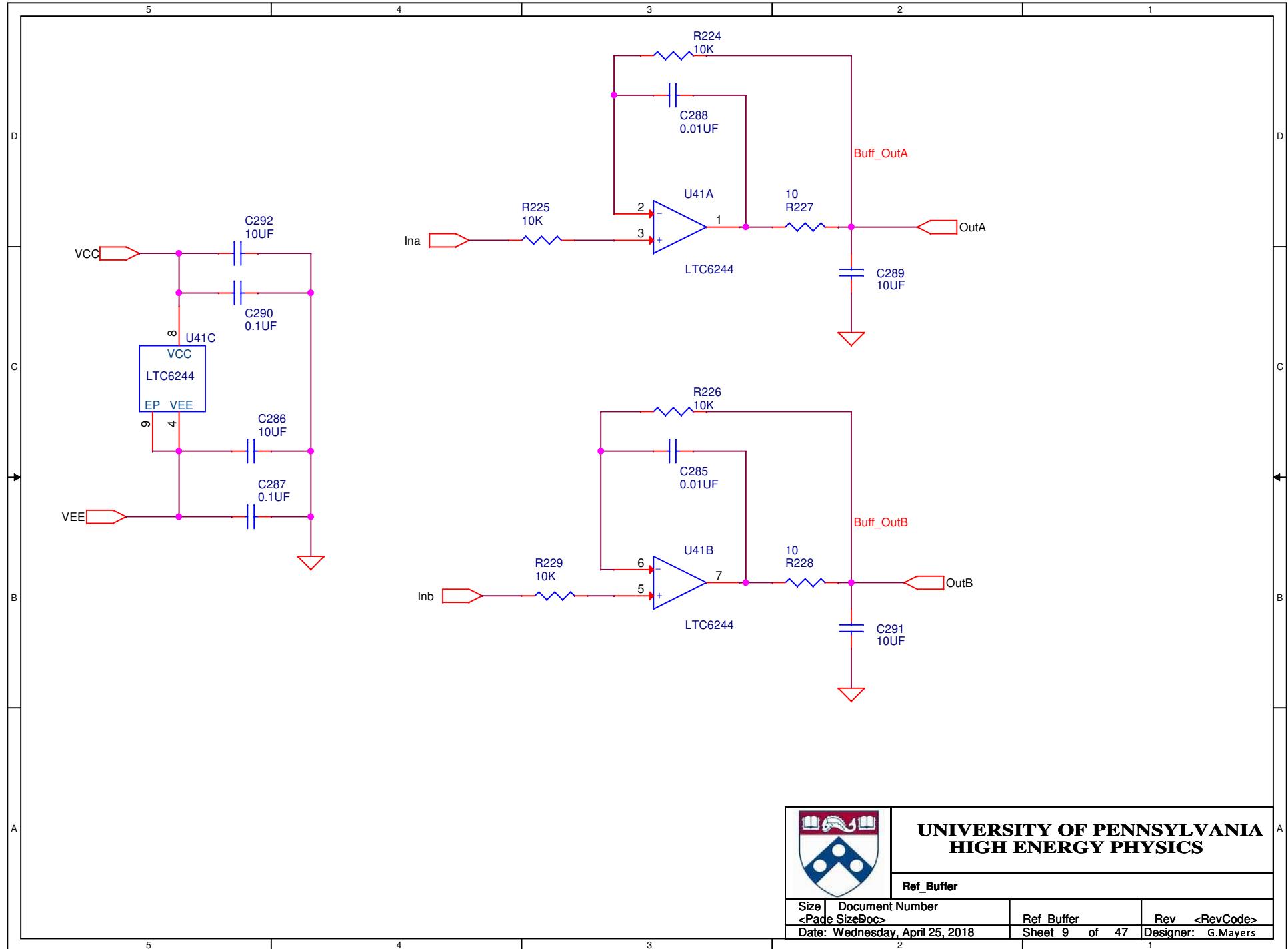
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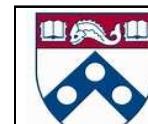
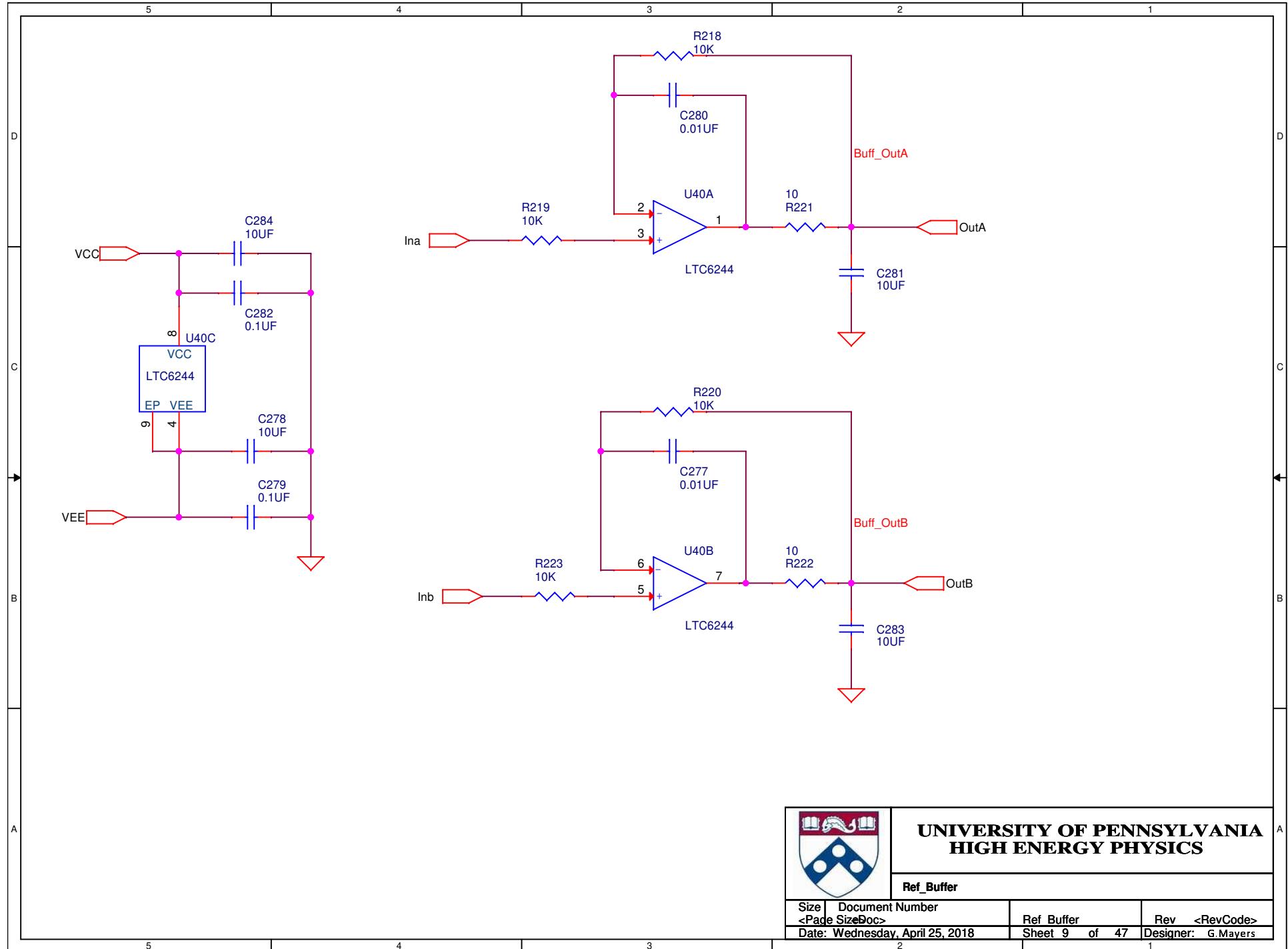
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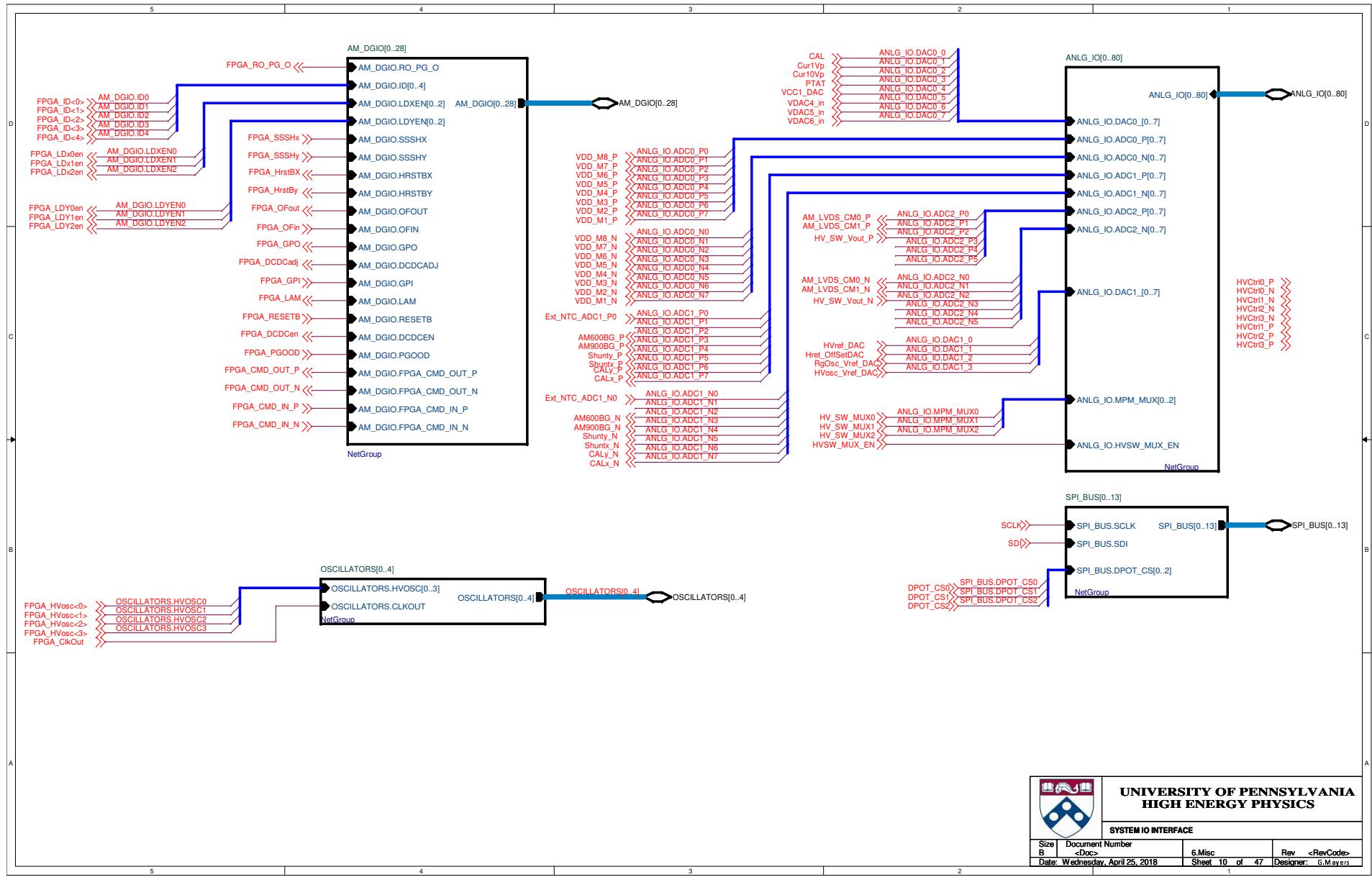
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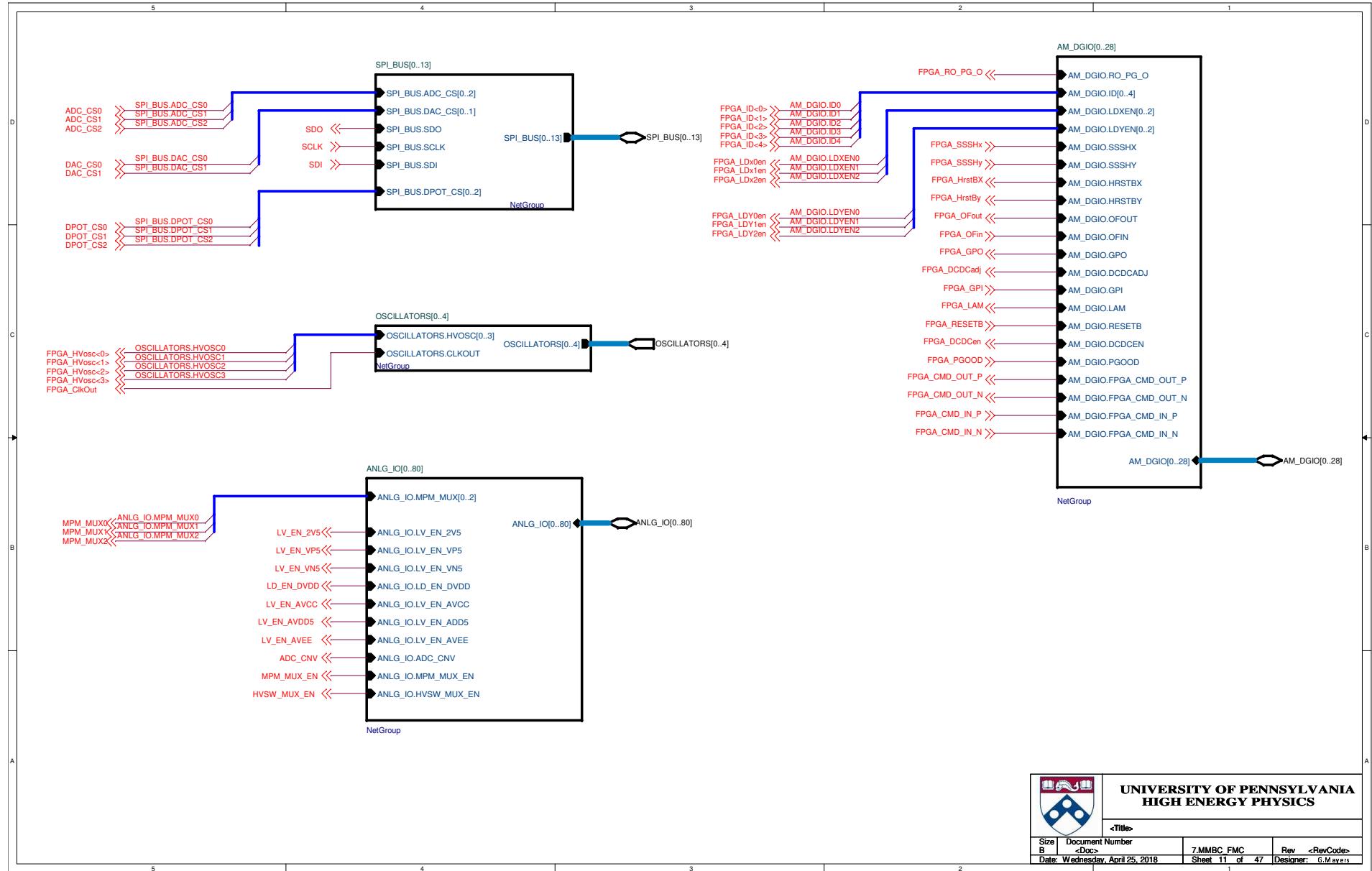


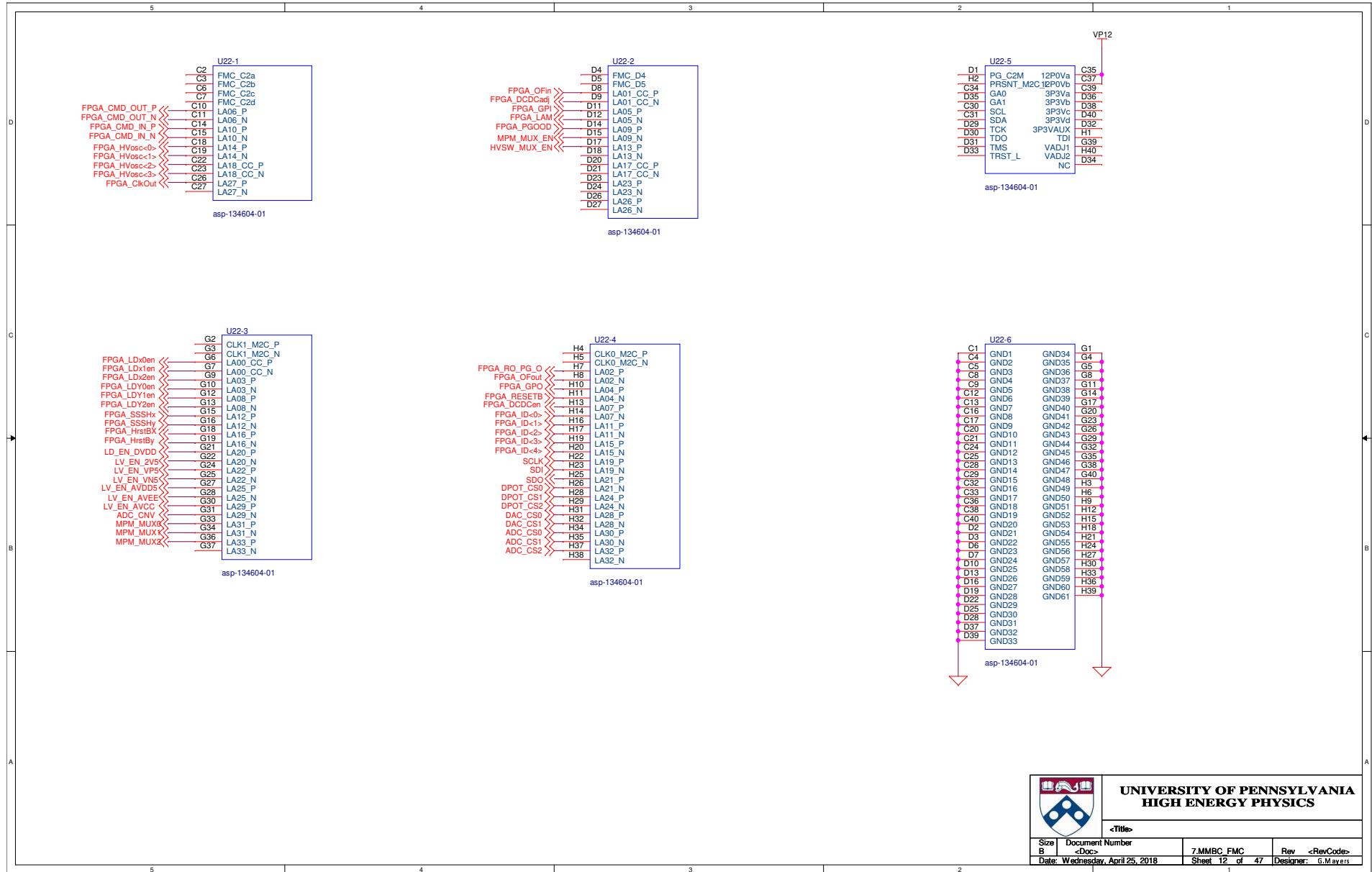
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