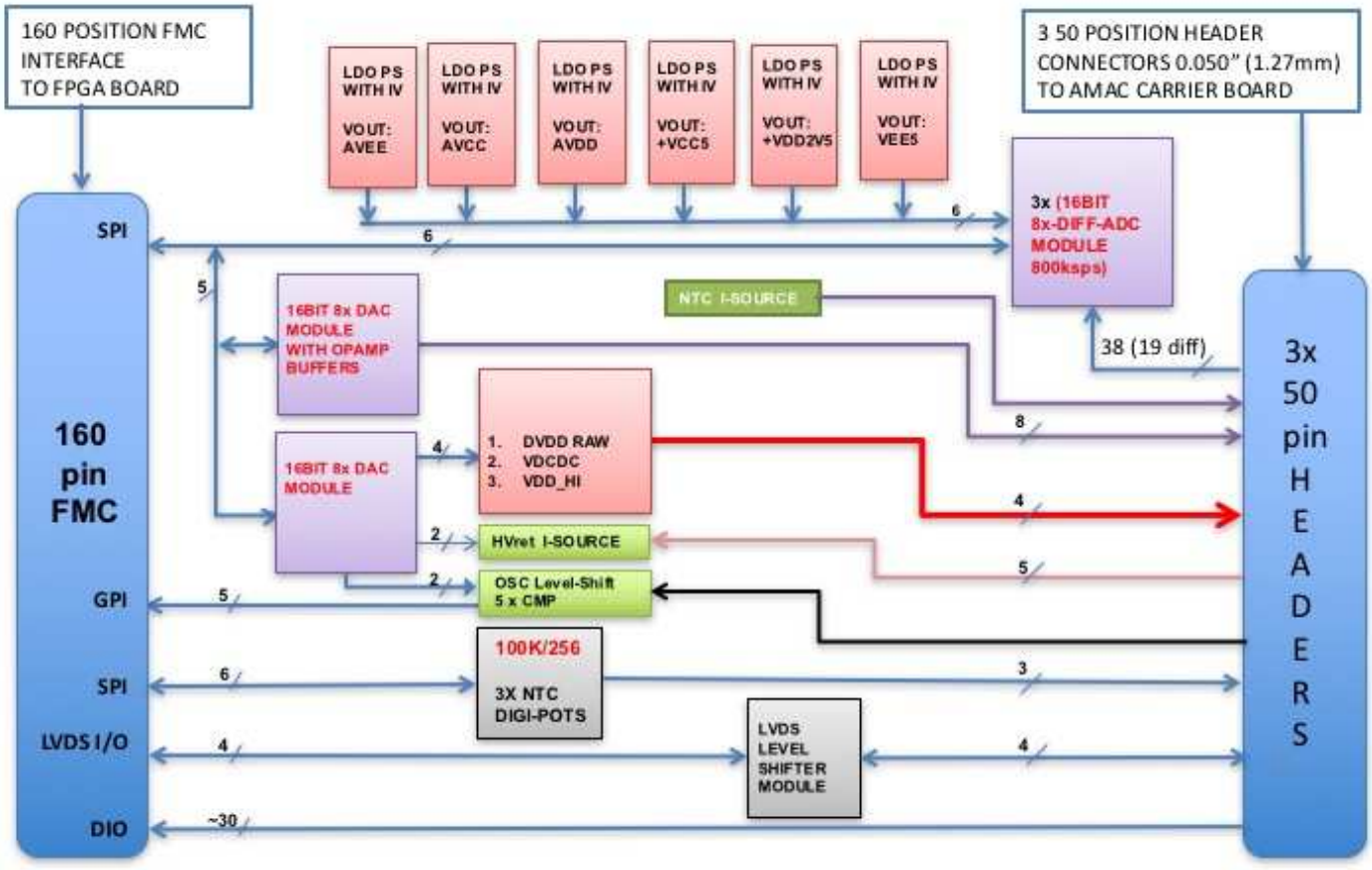
AMAC V2 TEST & CONTROL BLOCK DIAGRAM



4/27/18

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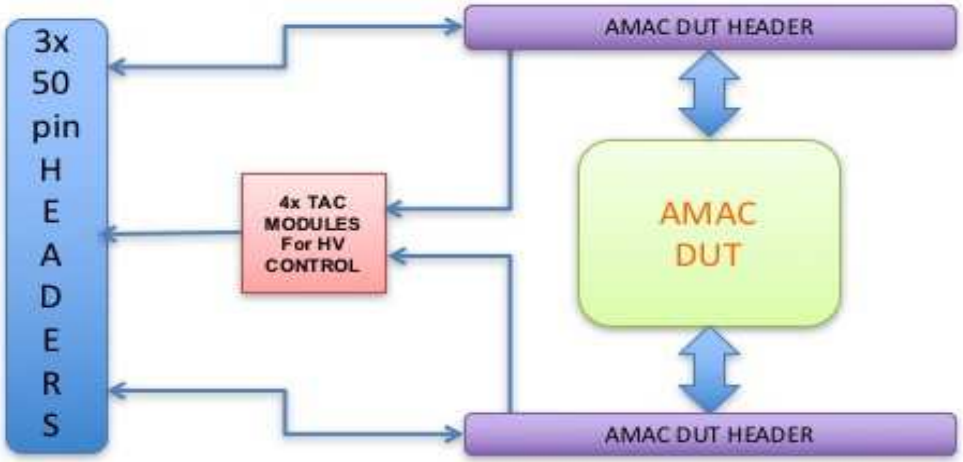
HIGH ENERGY PHYSICS

ATCB Block Diagrams

Size	Document Number		
A	<Doc>	Top	Rev 1
Date: Thursday, May 10, 2018		Sheet 1 of 12	Designer: G.Mayers

AMAC CARRIER AND DUT BOARDS

3 50 POSITION HEADER CONNECTOR 0.050(1.27mm) TO AMAC TEST & CONTROL BOARD



3/12/18 Godwin Mayers 2

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AMAC CARRIER & DUT

Size	Document Number		Rev
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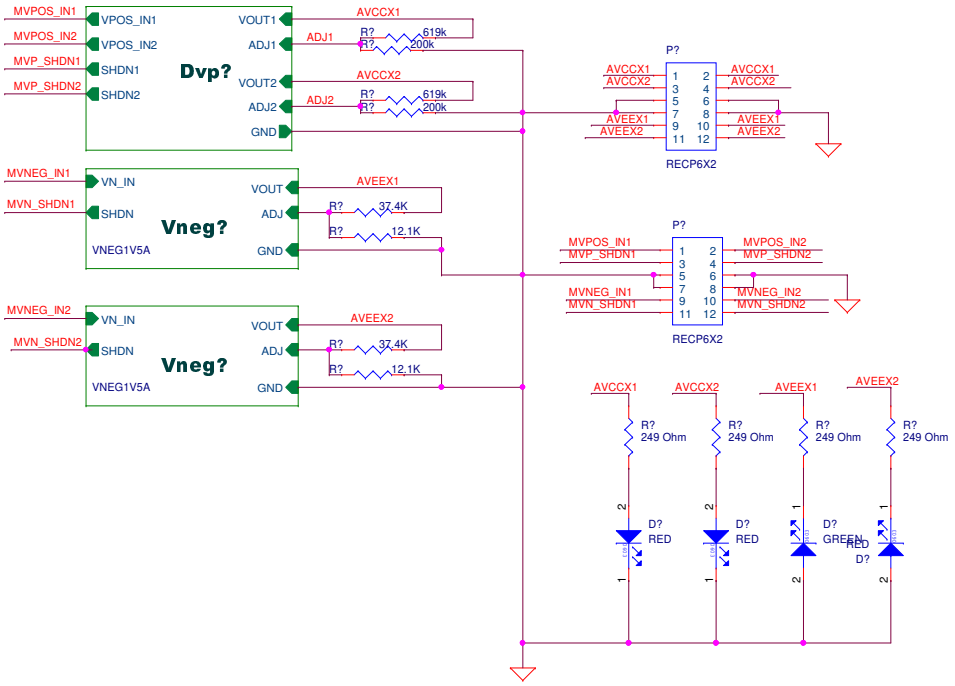
Date: Thursday, May 10, 2018		Sheet 1 of 1	Designer: G.Mayers

4. LDO REGULATOR BREAKAWAY MODULES



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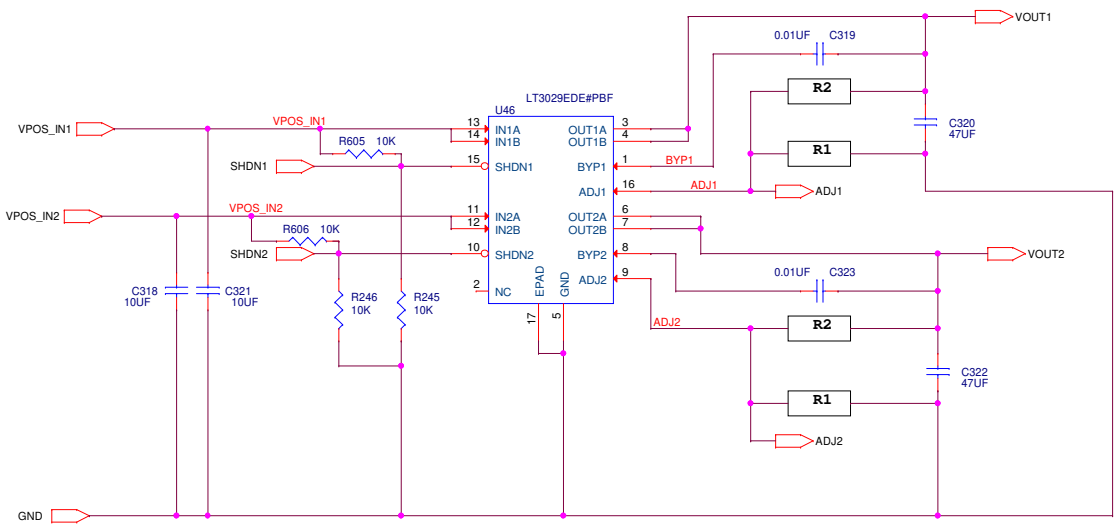

R1 and R2 blocks only serve as place holders when referencing table below and show where external resistor fit in the circuit.

Table 1. Output Voltage Resistor Divider Values

V_{OUT} (V)	R1 (k)	R2 (k)
1.5	237	54.9
1.8	237	113
2.5	243	255
3	232	340
3.3	210	357
5	200	619

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HIGH ENERGY PHYSICS

Dual_Vpos

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Date: Thursday, May 10, 2018		Sheet 1 of 64	Designer: G.Mayers

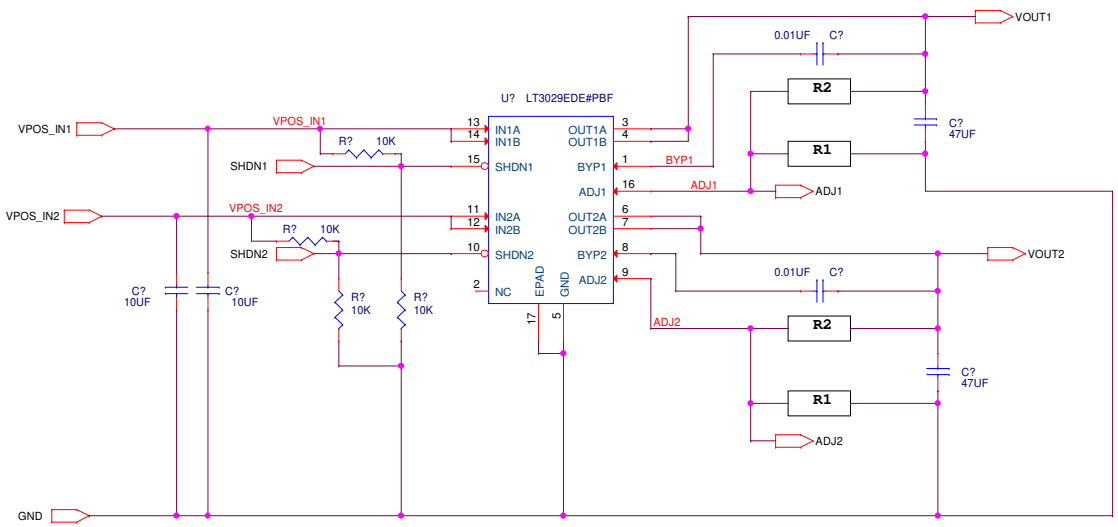

Table 1. Output Voltage Resistor Divider Values

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HIGH ENERGY PHYSICS

Dual_Vpos

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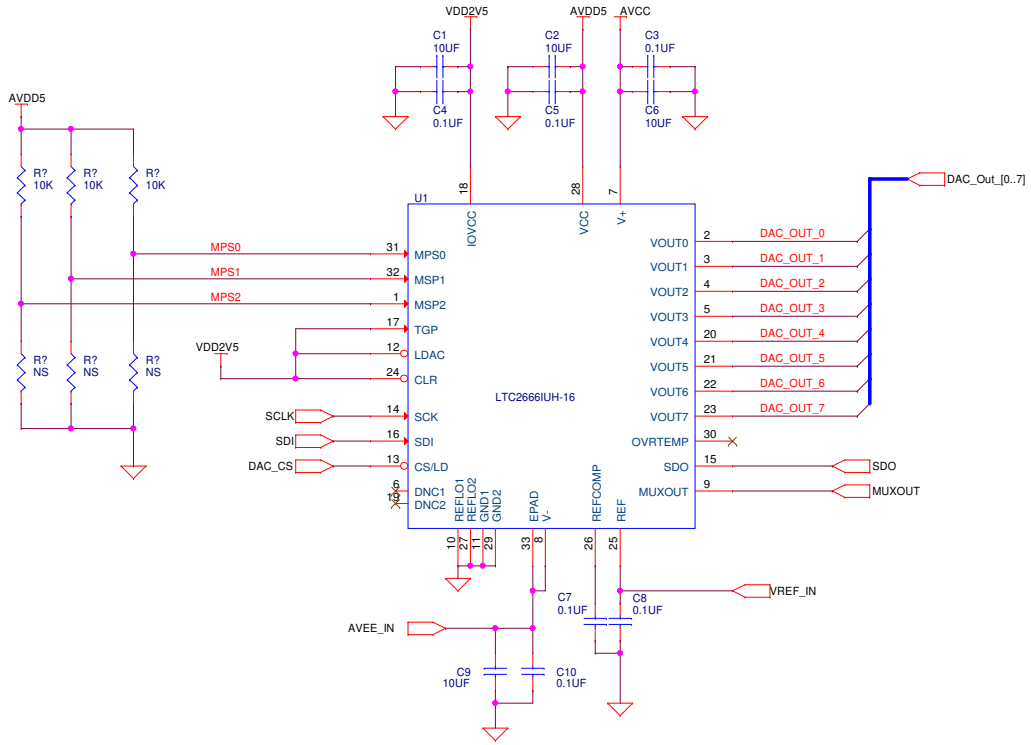

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HIGH ENERGY PHYSICS

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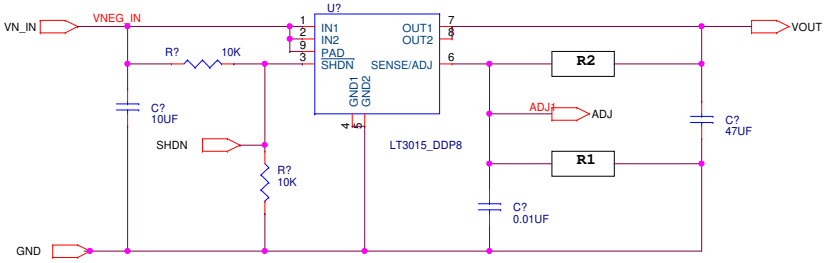

Table 1. Output Voltage Resistor Divider Values

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
−2.5	12.1	12.7
−3.0	12.1	17.8
−3.3	12.1	20.5
−5.0	12.1	37.4
−12.0	12.1	107
−15.0	12.4	140

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HIGH ENERGY PHYSICS

VNEG_1.5AMPS

Size	Document Number		Rev
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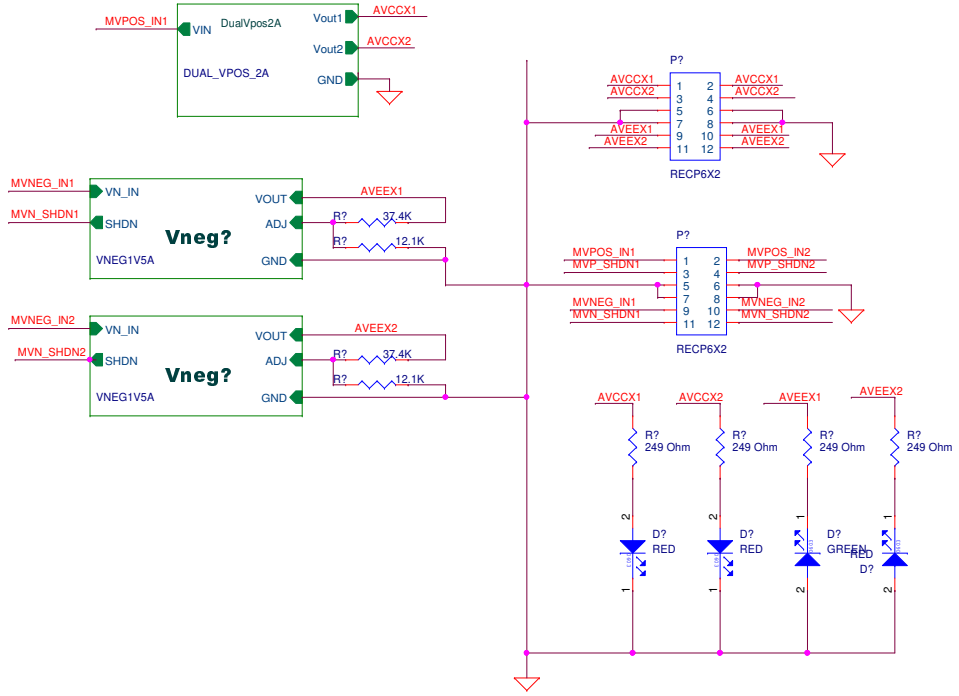
Date: Thursday, May 10, 2018		Sheet 1 of 1	Designer: G.Mayers

4. LDO REGULATOR BREAKAWAY MODULES



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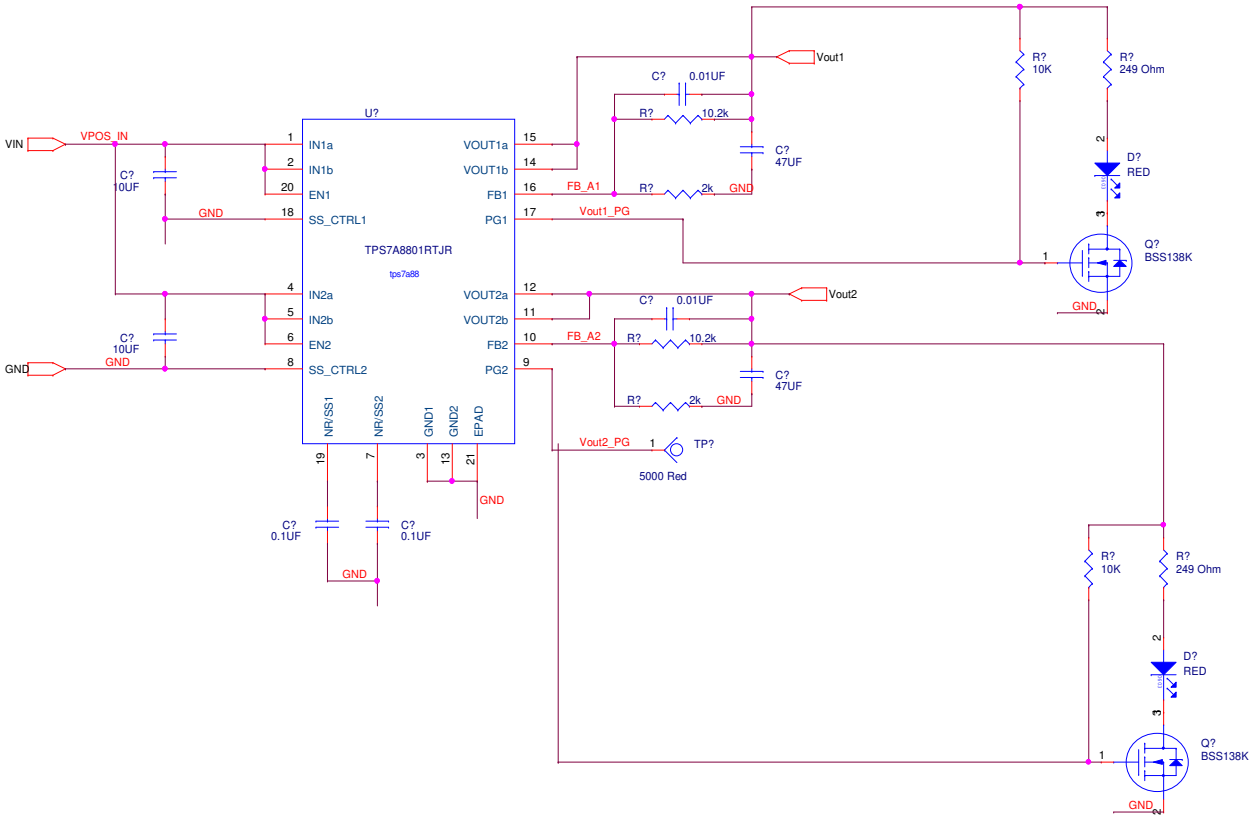

Table 2. Recommended Feedback-Resistor Values

$V_{OUTx(TARGET)}$ (V)	FEEDBACK RESISTOR VALUES(1)	
	R_1, R_3 (kΩ)	R_2, R_4 (kΩ)
0.8	Short	Open
1.00	2.55	10.2
1.20	5.9	11.8
1.50	9.31	10.7
1.80	1.87	1.5
1.90	15.8	11.5
2.50	2.43	1.15
3.00	3.16	1.15
3.30	3.57	1.15
5.00	10.5	2

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HIGH ENERGY PHYSICS

MAIN POWER

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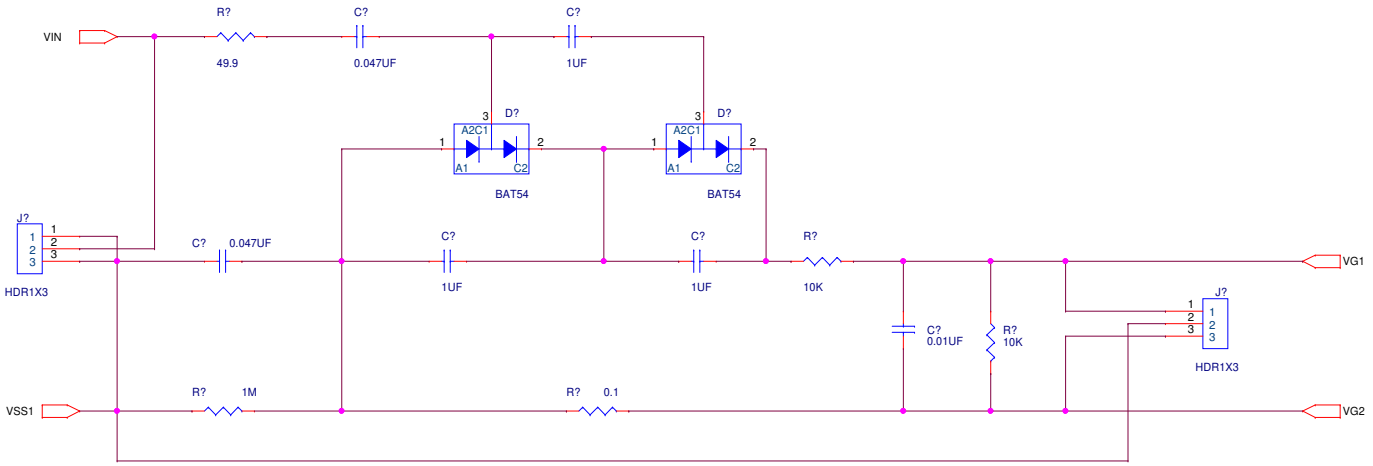
Date: Thursday, May 10, 2018		Sheet 1 of 1	Designer: G.Mayers



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HIGH ENERGY PHYSICS

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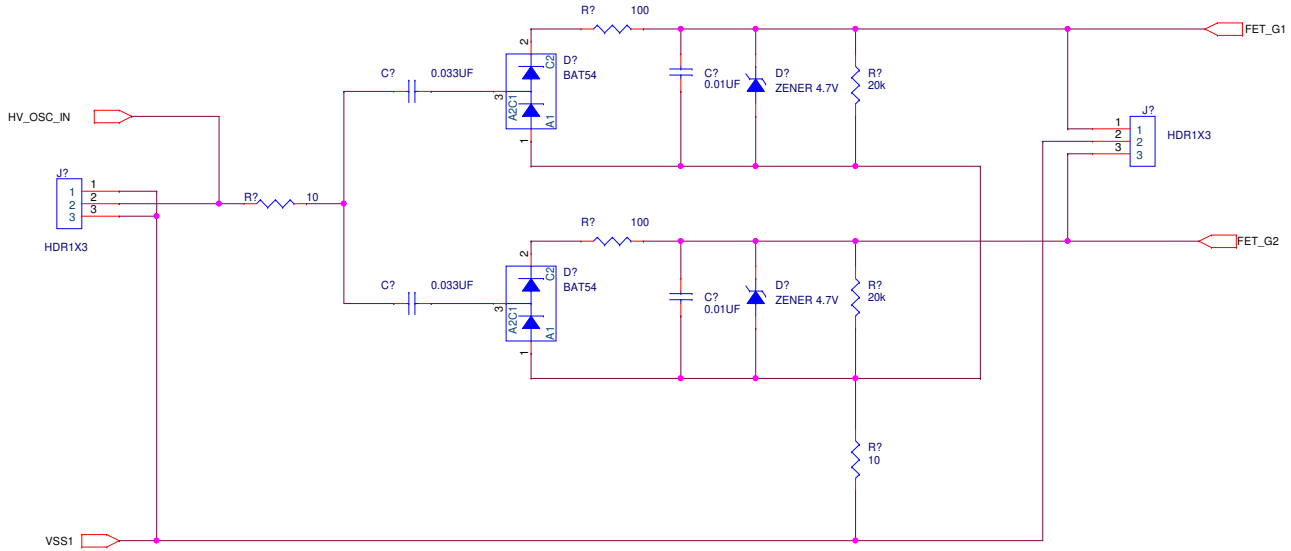

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HIGH ENERGY PHYSICS

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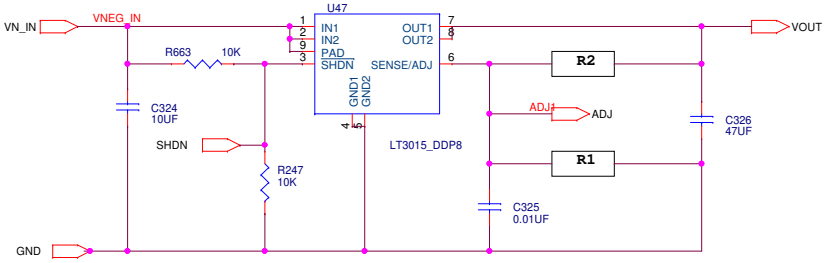

Table 1. Output Voltage Resistor Divider Values

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−3.0	12.1	17.8
−3.3	12.1	20.5
−5.0	12.1	37.4
−12.0	12.1	107
−15.0	12.4	140

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HIGH ENERGY PHYSICS

VNEG_1.5AMPS

Size	Document Number		Rev
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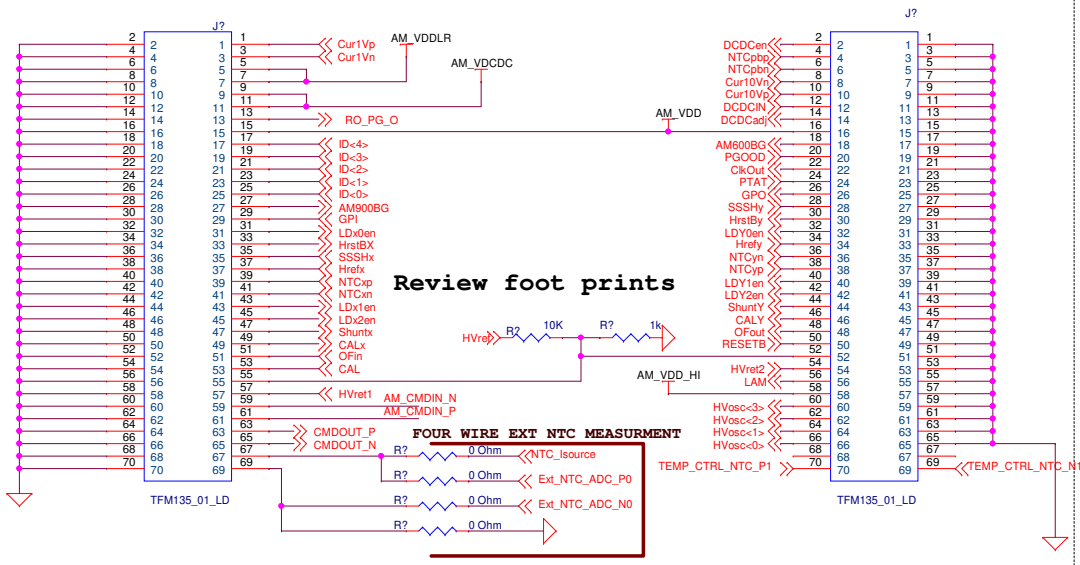
Date: Thursday, May 10, 2018		Sheet 1 of 64	Designer: G.Mayers

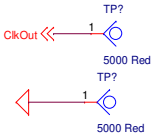
1. AMAC DUT CONNECTORS



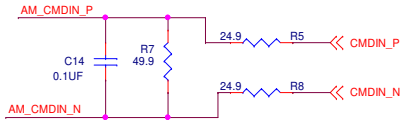
Review foot prints

FOUR WIRE EXT NTC MEASURMENT

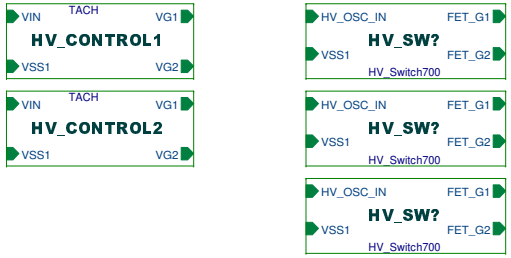
RING OSC COAX CONNECTION



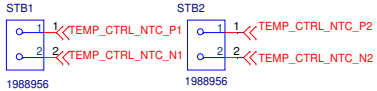
LVDS TERMINATION



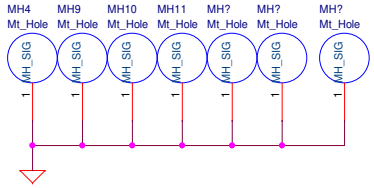
2. TACH BREAKAWAY MODULES



3. COLD-PLATE NTC CONNECTORS



4. PCB MOUNT HOLES



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HIGH ENERGY PHYSICS

AMAC DUT CONNECTORS

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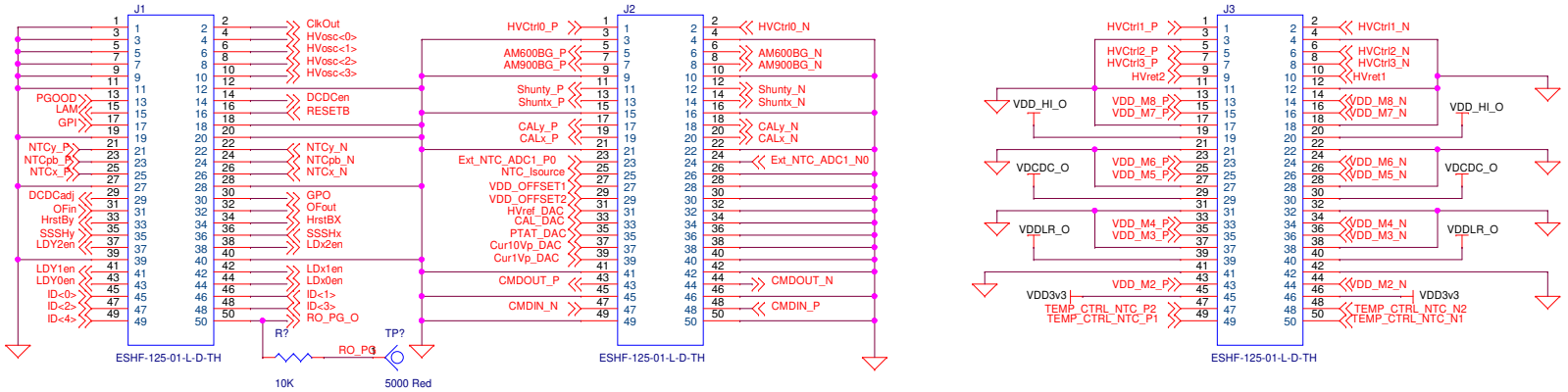
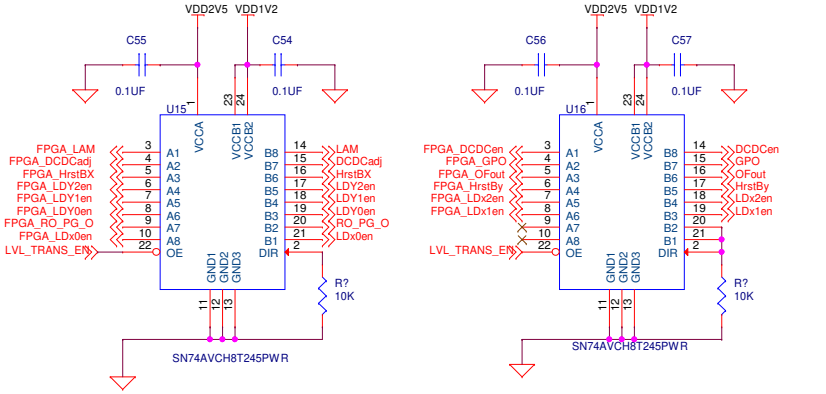
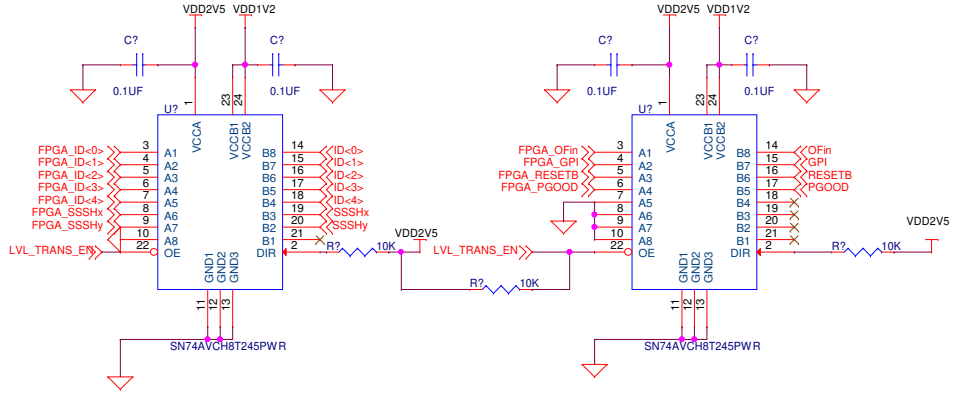
1. ATCB Interface Connectors



2. AMAC To FPGA DIO Level Translators



3. FPGA To AMAC DIO Level Translators



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HIGH ENERGY PHYSICS

ATCB INTERFACE

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Date: Thursday, May 10, 2018		Sheet 1 of 12	Designer: G.Mayers

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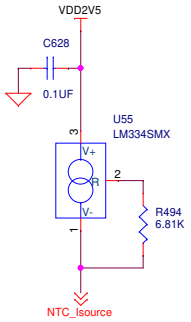
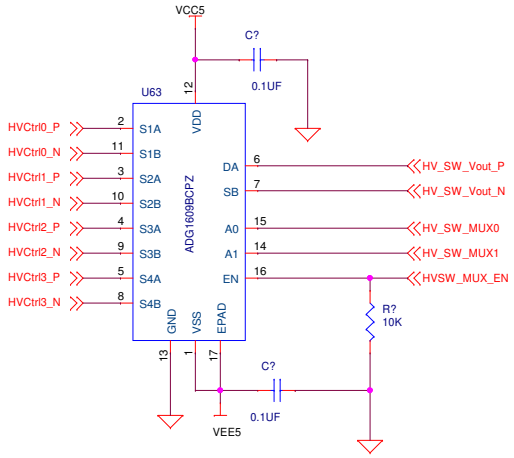
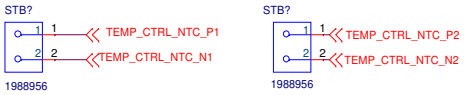


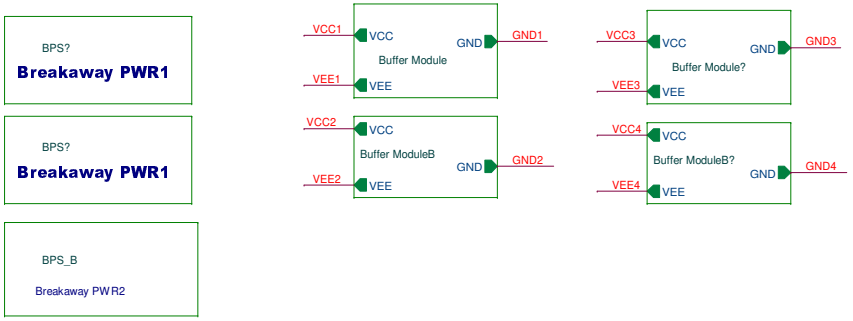
2. HV_SW MUX



3. COLD-PLATE NTC CONNECTORS



4. LDO REGULATOR BREAKAWAY MODULES



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Misc_Circuits B

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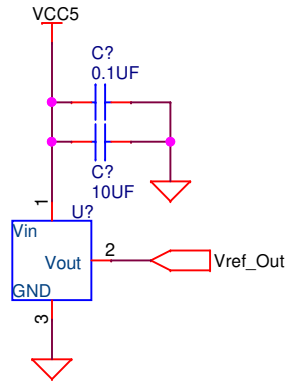

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HIGH ENERGY PHYSICS

1024_Vref

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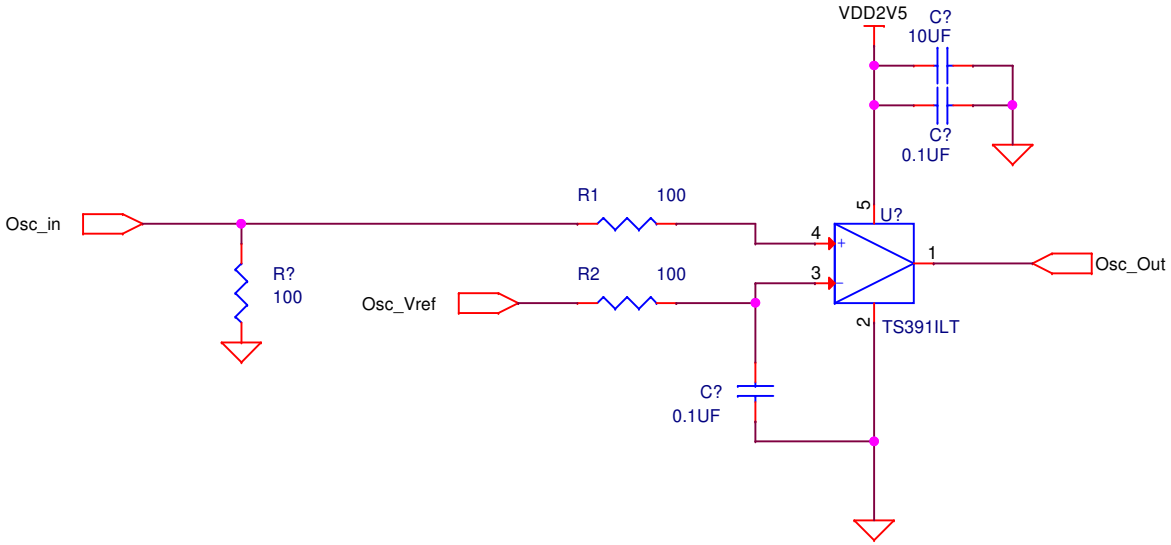

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HIGH ENERGY PHYSICS

OSC LEVEL SHIFTER

Size	Document Number		
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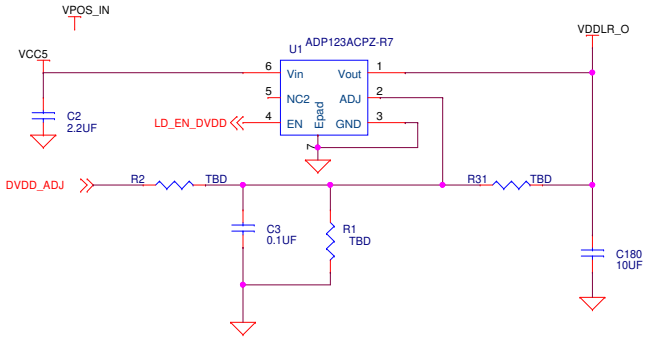
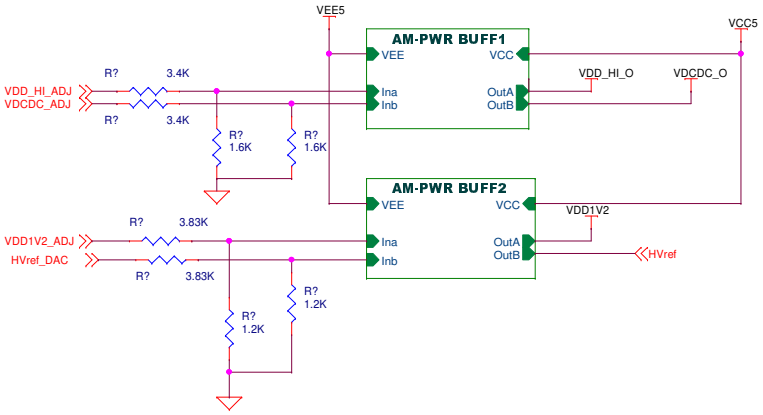
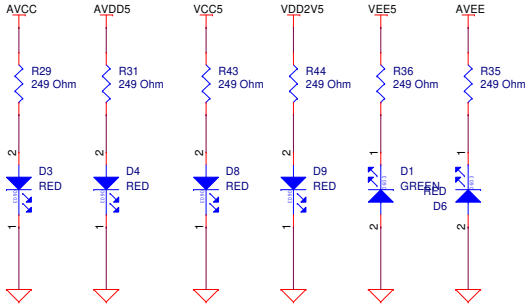
Date: Thursday, May 10, 2018		Sheet 1 of 12	Designer: G.Mayers

1. AMAC POWER

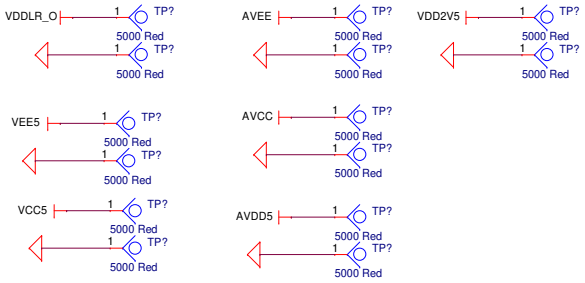




2. MAIN POWER INDICATORS



3. EXTERNAL POWER CONNECTIONS



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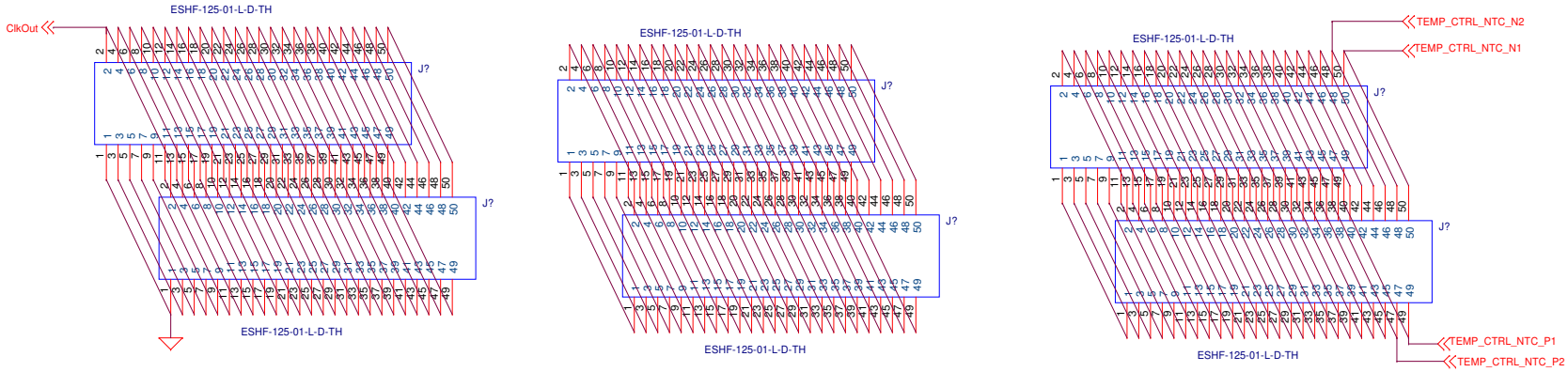
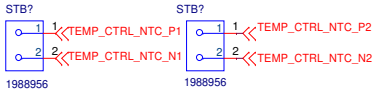
AMAC POWER			
Size B	Document Number <Doc>	8.Power	Rev <RevCode>
Date: Thursday, May 10, 2018		Sheet 1 of 1	Designer: G.Mayers

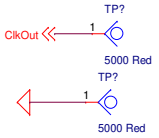
1. COLD-BOX BREAK-OUT CONNECTORS



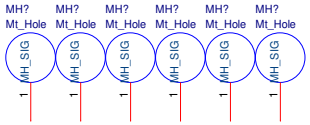
2. COLD-PLATE NTC CONNECTORS



3. RING OSC COAX CONNECTION



4. PCB MOUNT HOLES



UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS			
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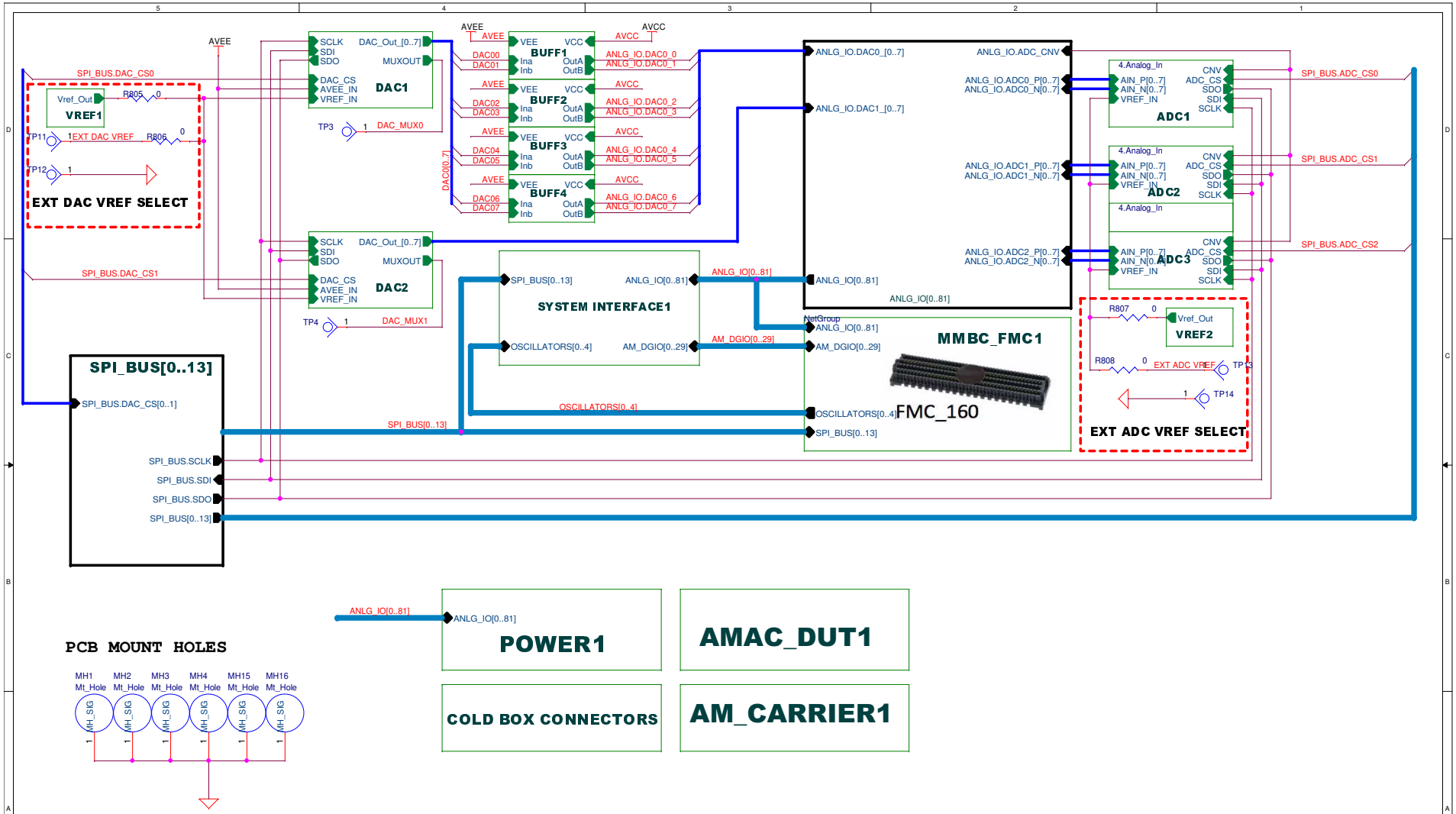
Size B	Document Number <Doc>	Cold Box Interface	Rev <RevCode>
Date: Thursday, May 10, 2018		Sheet 1 of 1	Designer: G.Mayers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EXT DAC VREF SELECT
DAC1
DAC2
BUFF1
BUFF2
BUFF3
BUFF4
SYSTEM INTERFACE1
SPI_BUS[0..13]
MMBC_FMC1
FMC_160
ADC1
ADC2
ADC3
VREF2
EXT ADC VREF SELECT
POWER1
AMAC_DUT1
COLD BOX CONNECTORS
AM_CARRIER1
PCB MOUNT HOLES
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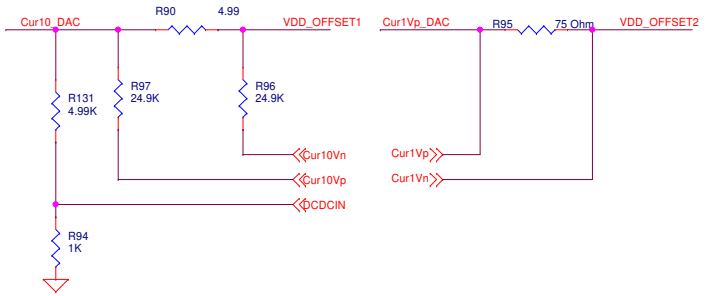
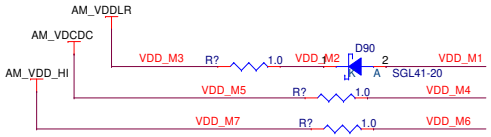
HIGH ENERGY PHYSICS
ATCB TOP
Date: Thursday, May 10, 2018
Designer: G.Mayers

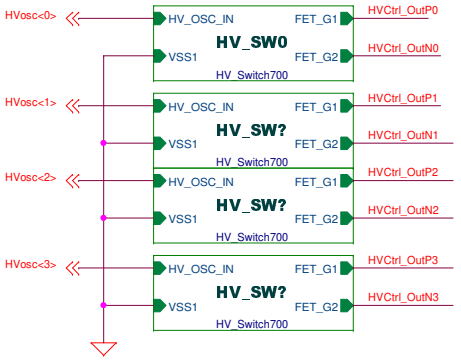
1.AMAC Analog I/O Hookup (Power Board Interface)



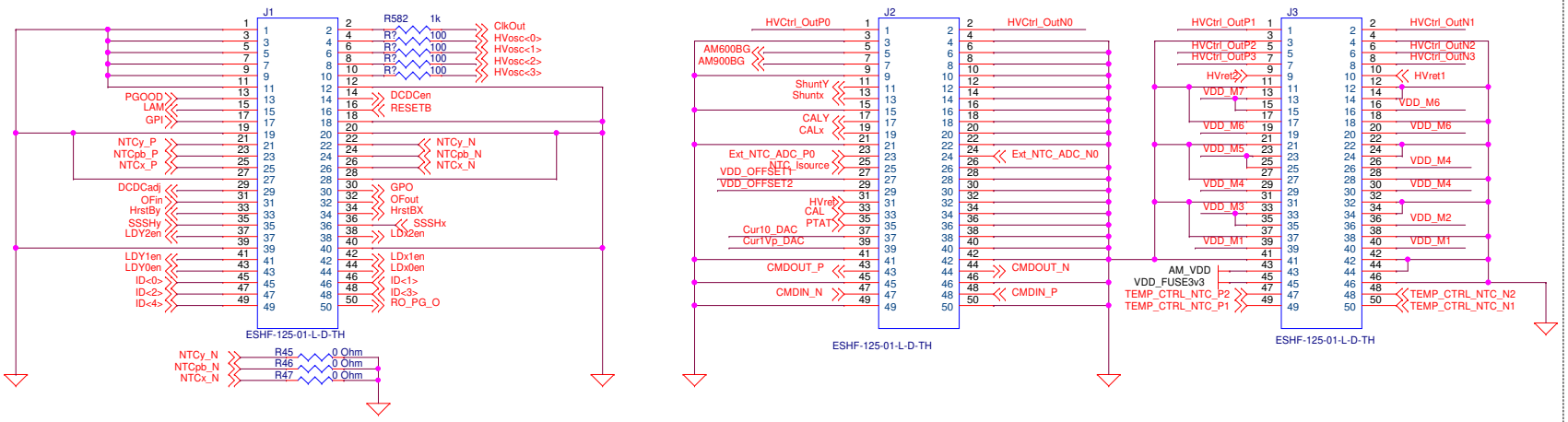
2. AMAC IV MEASUREMENT INTERFACE



3.HV CONTROLS (TACH)



4.AMAC CARRIER & ATCB INTERFACE CONNECTORS



UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS

AMAC_CARRIER

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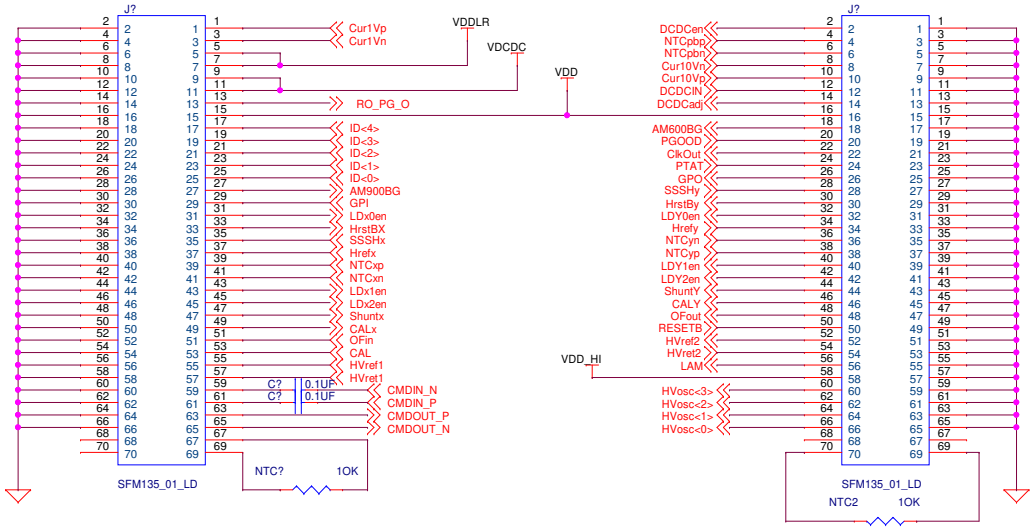
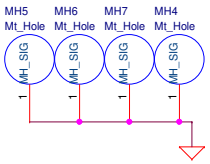
Date: Thursday, May 10, 2018		Sheet 3 of 12	Designer: G.Mayers



Review foot prints, Vddhv,vdd etc

PCB MOUNT HOLES



UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS

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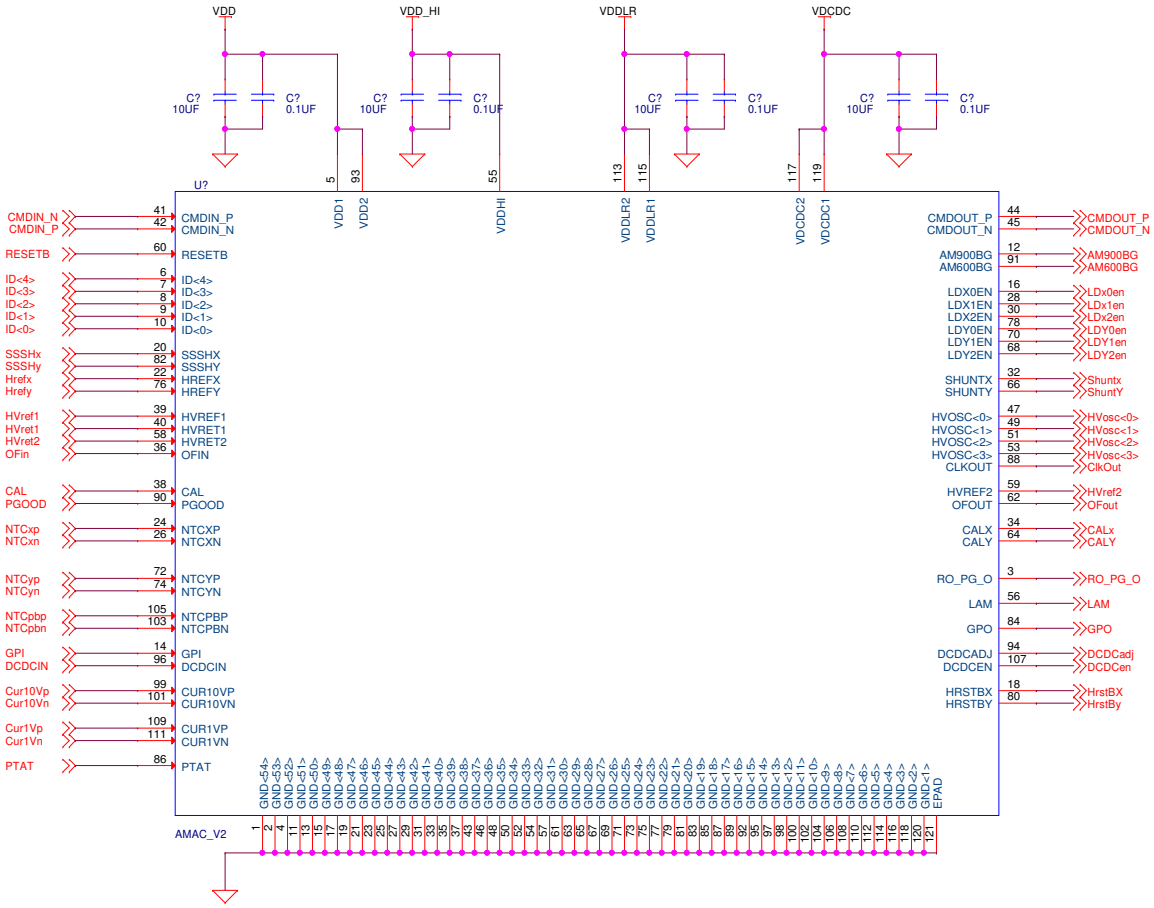

UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS

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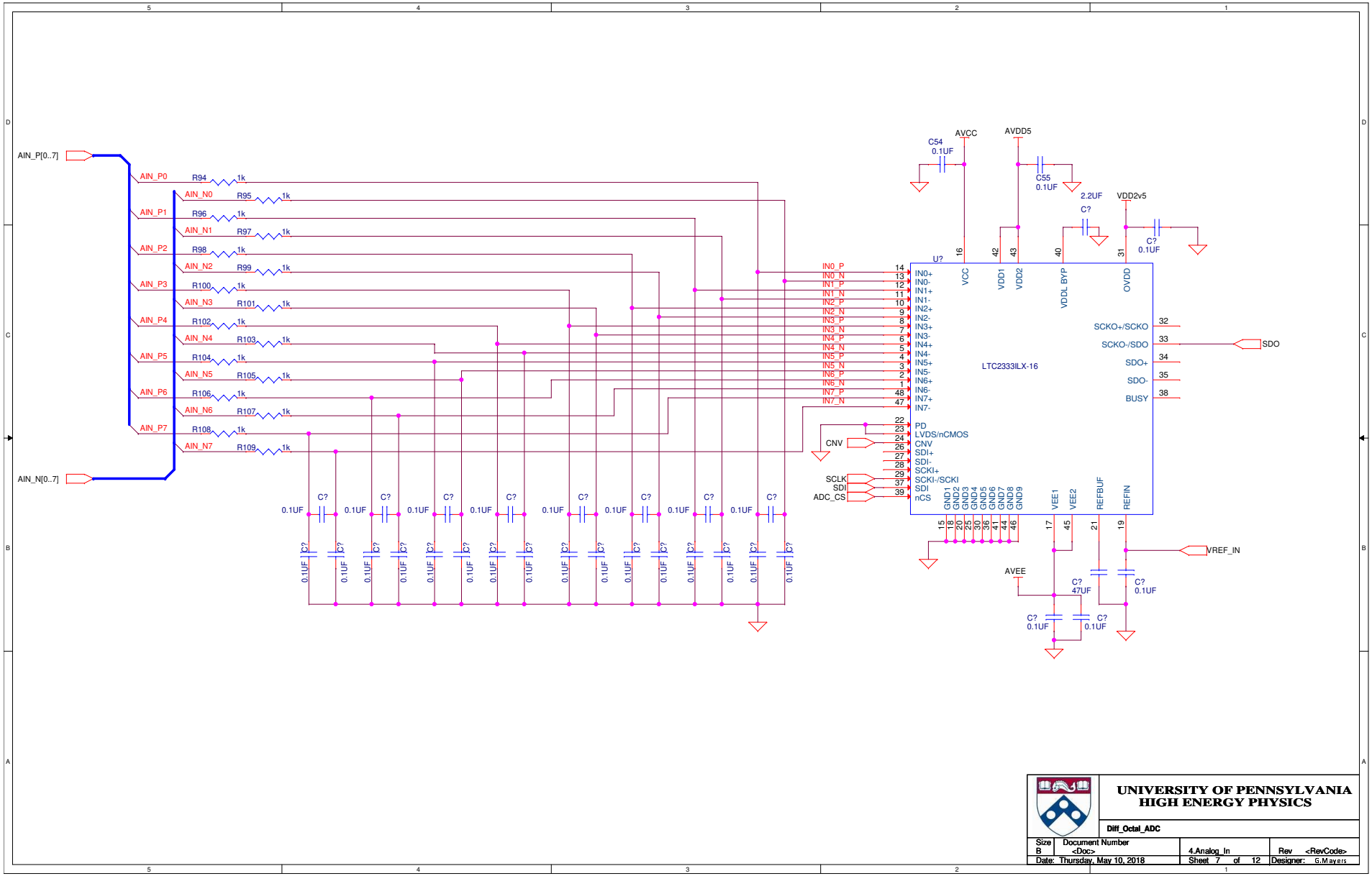

UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS

Diff_Octal_ADC

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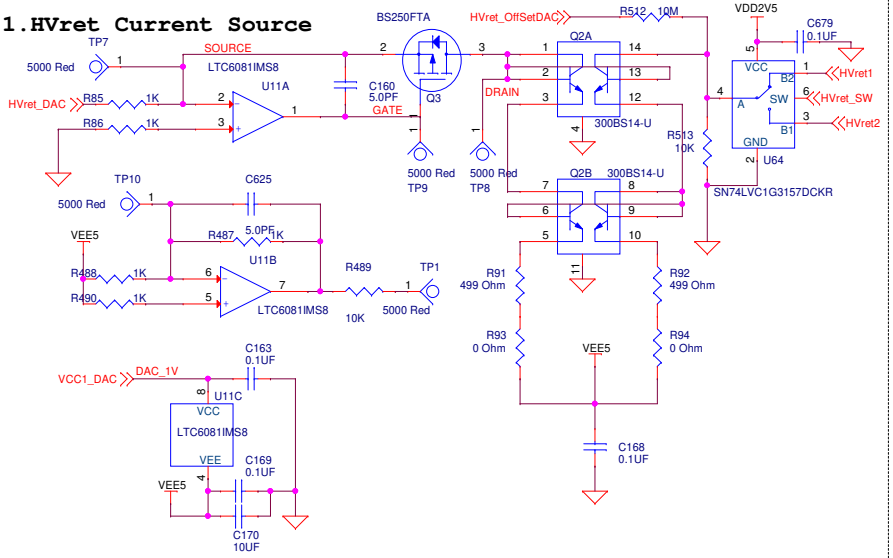
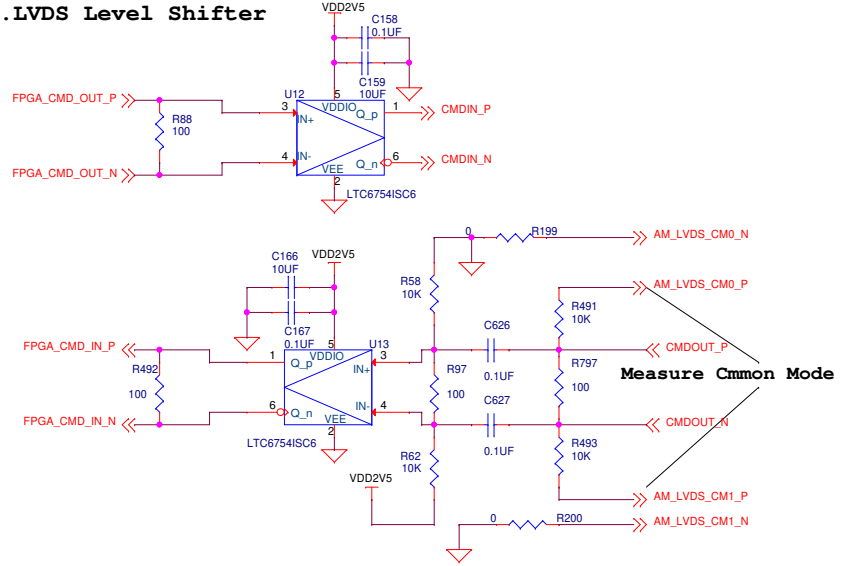
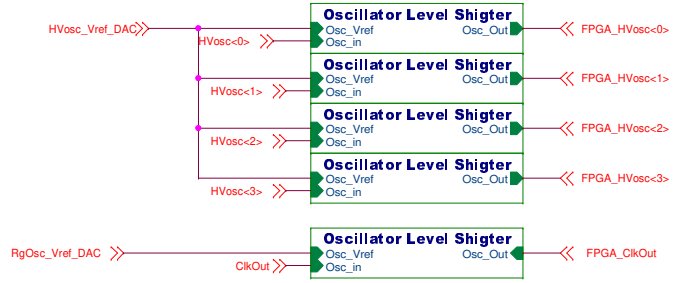


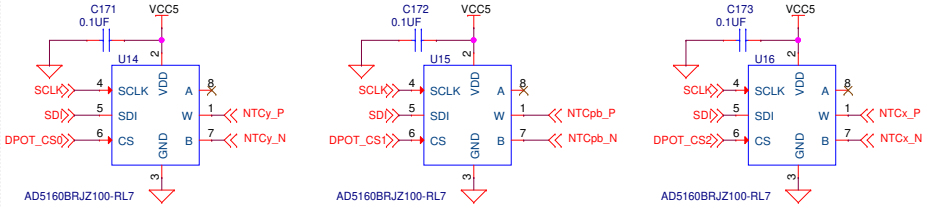
3.LVDS Level Shifter



2.OSC.Level Shifter To FPGA



4.Digital Pots For AMAC NTC Inputs



UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS

Misc_Circuits A

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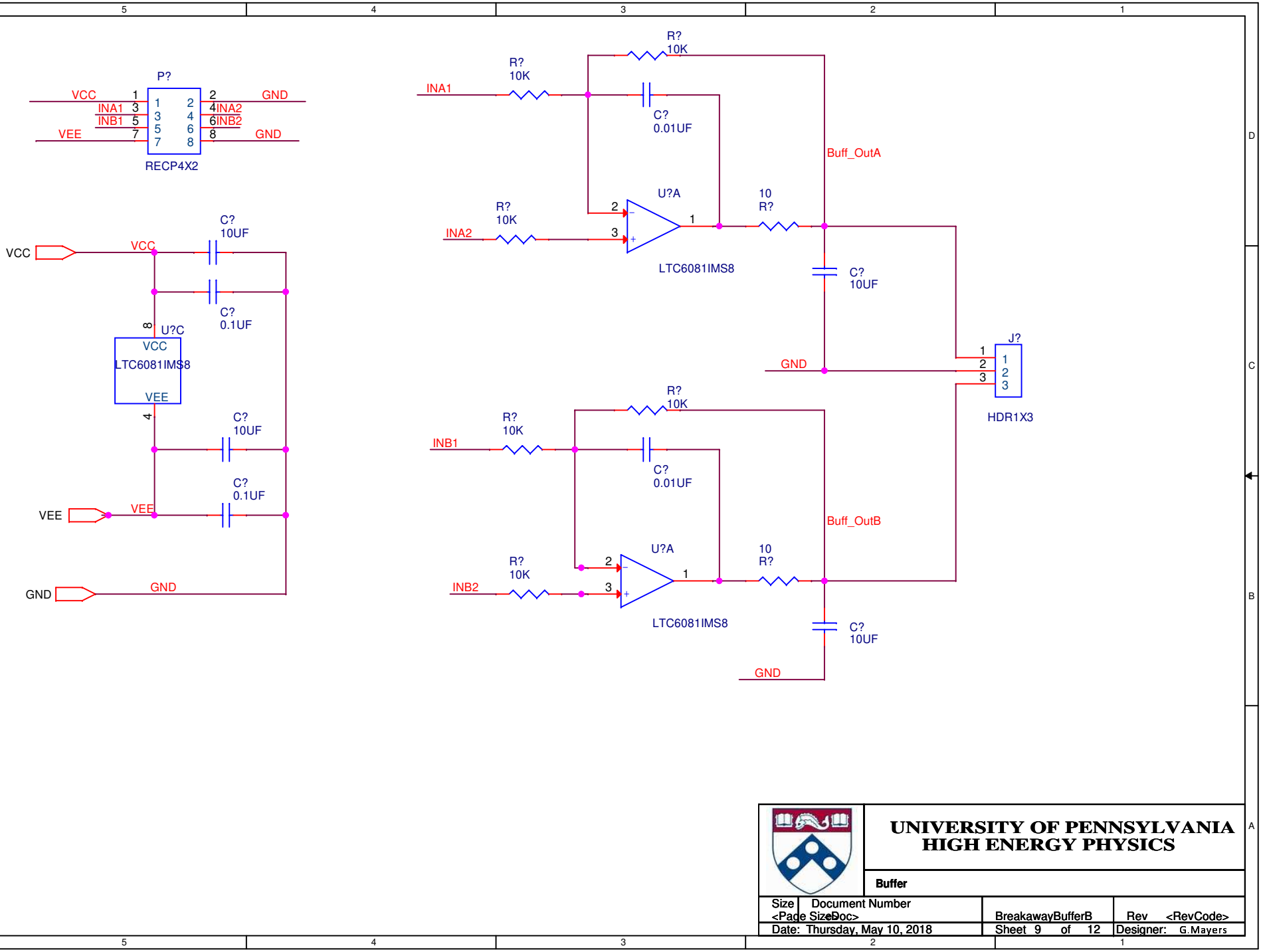
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10K
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Buff_OutA
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UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
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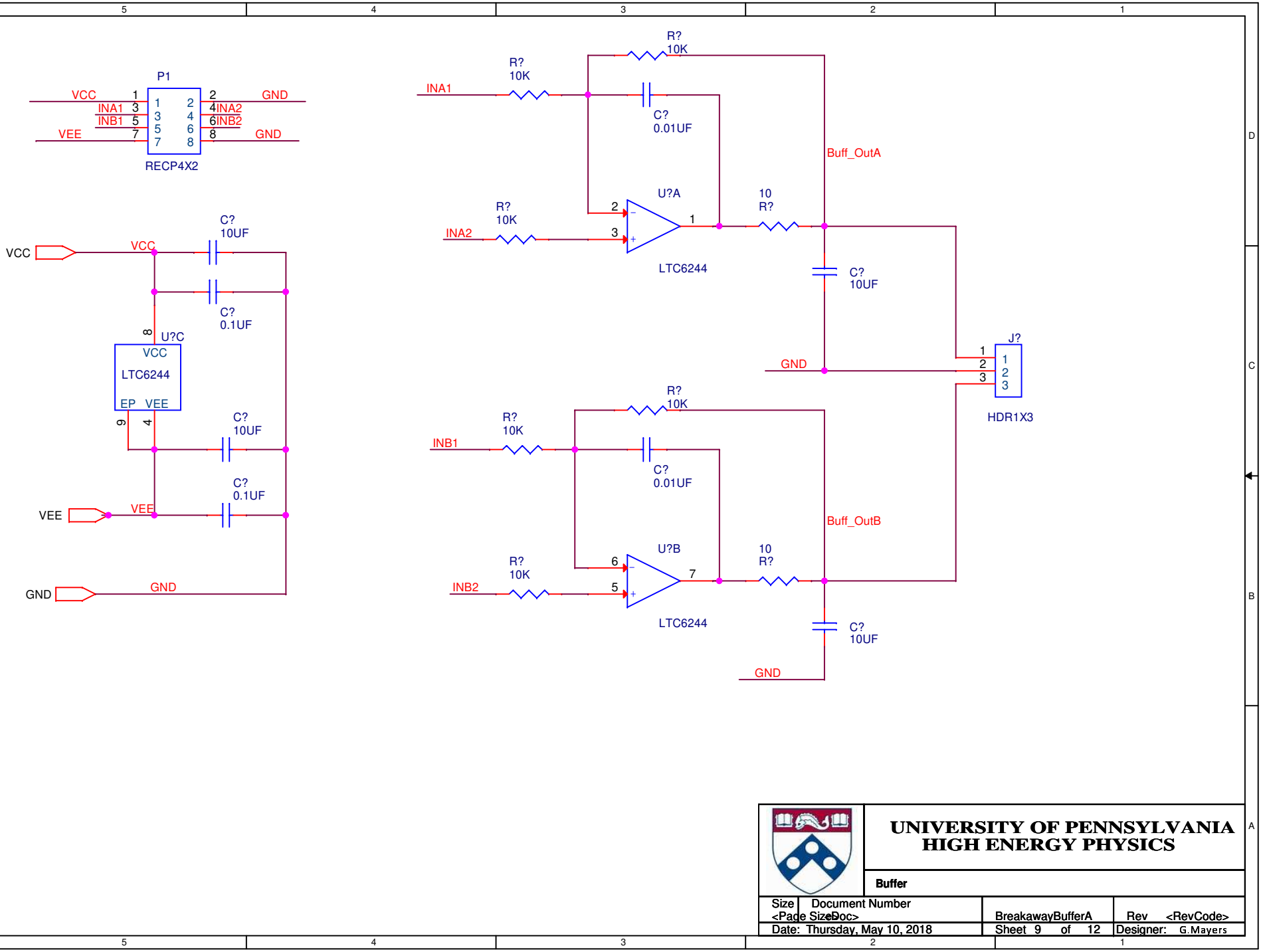
Date: Thursday, May 10, 2018
Sheet 9 of 12
Designer: G.Mayers



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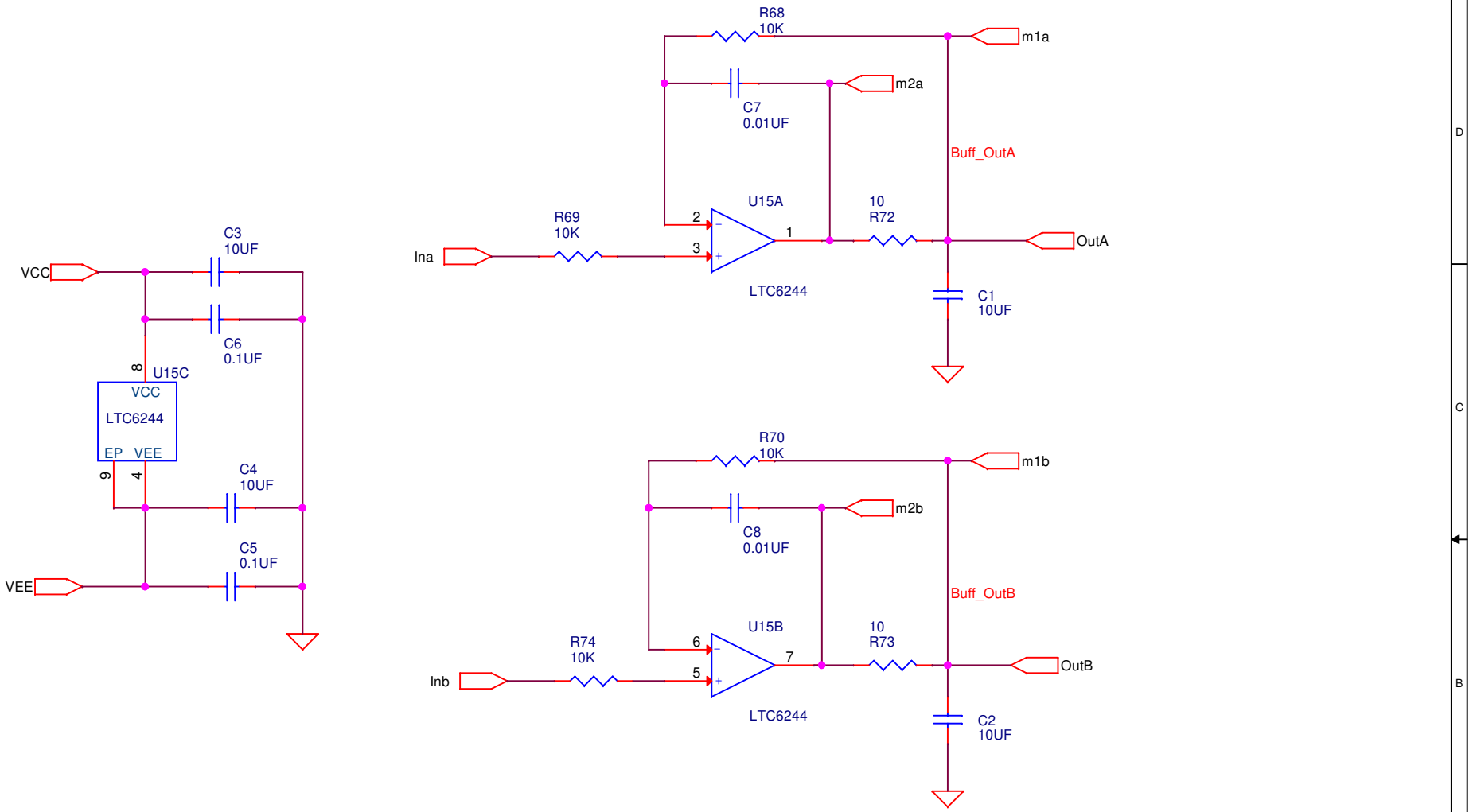

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HIGH ENERGY PHYSICS

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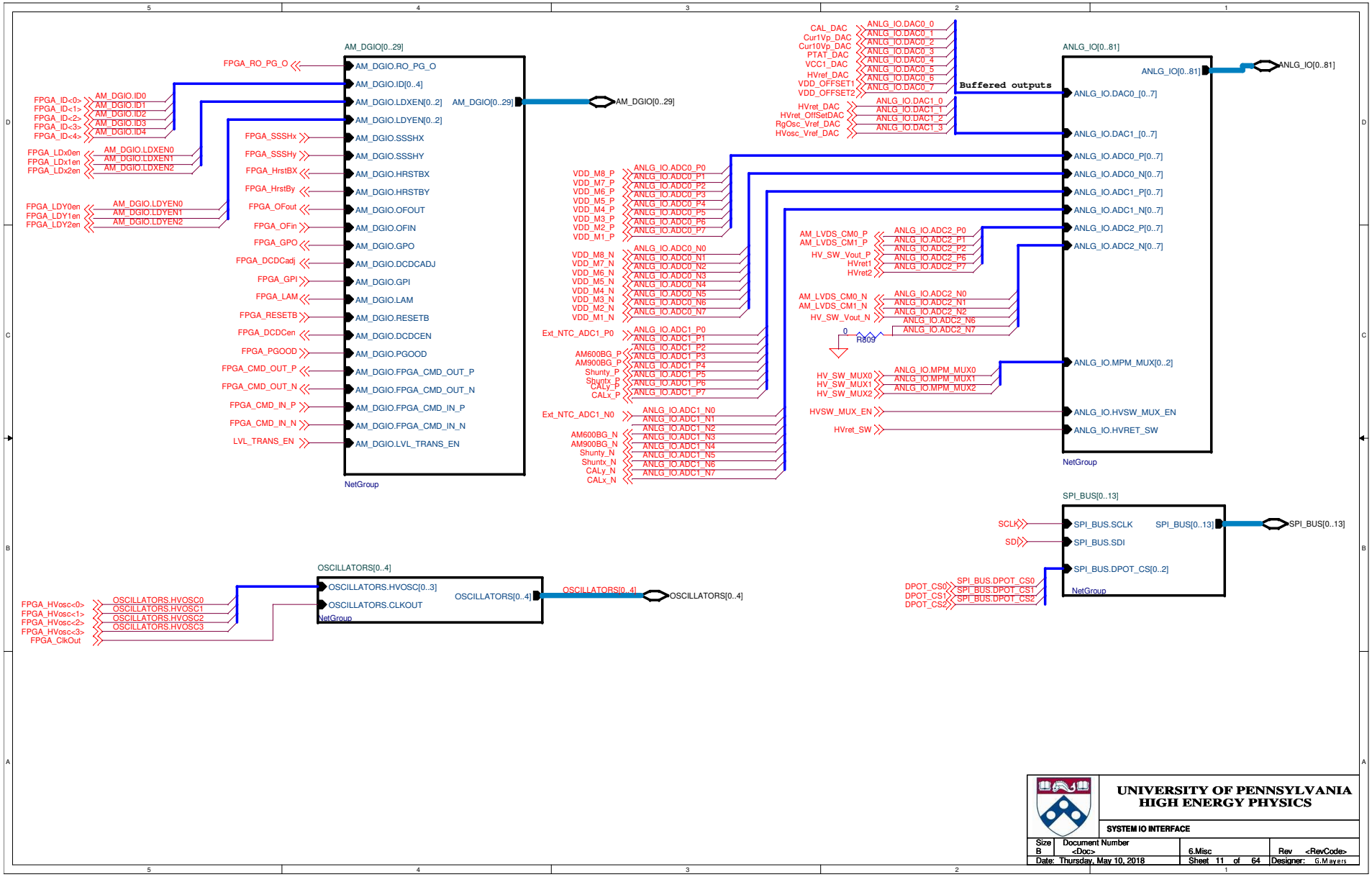
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VDD_OFFSET2
HVret_DAC
HVret_OffSetDAC
RgOsc_Vref_DAC
HVosc_Vref_DAC
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UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
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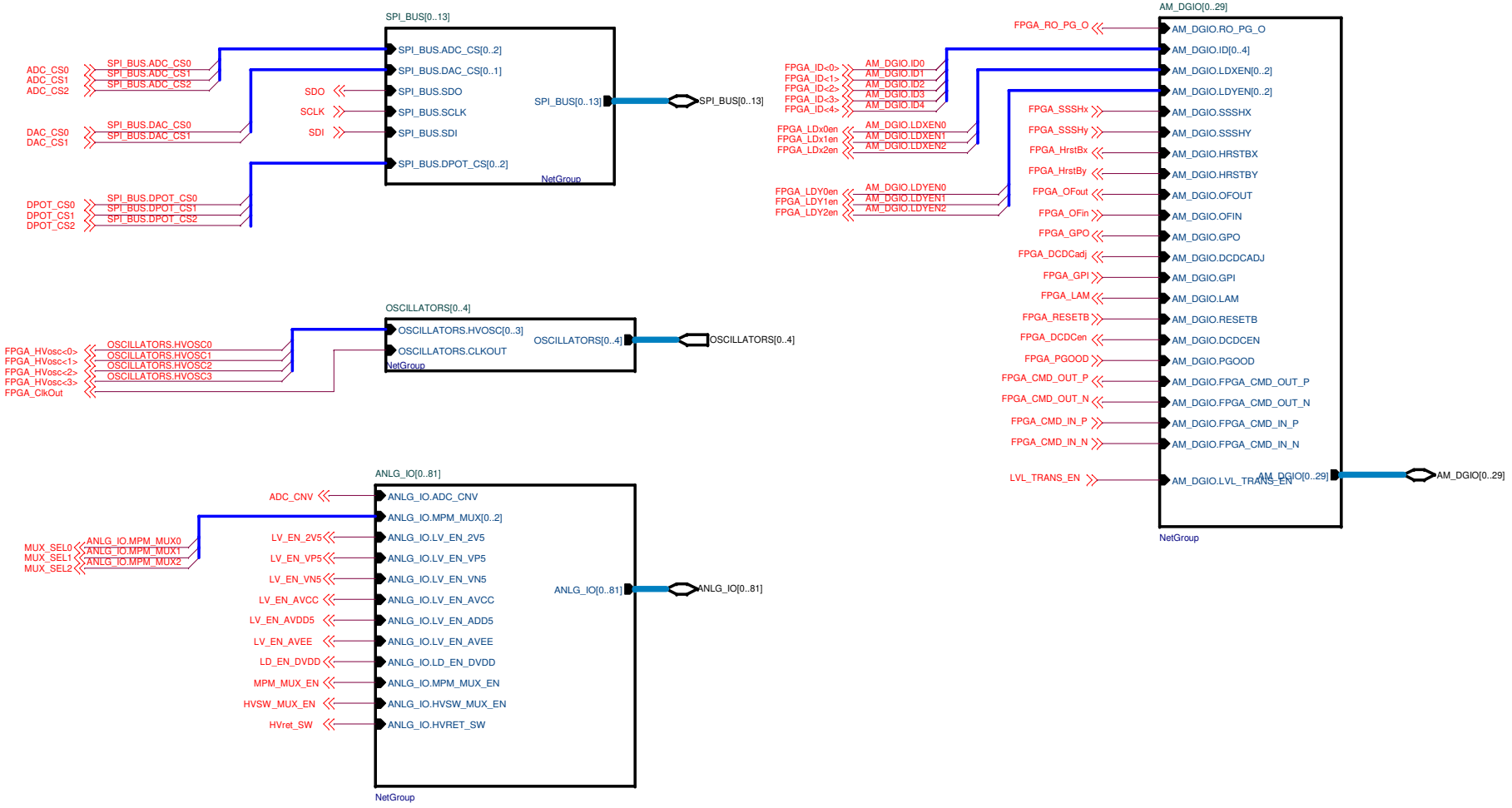
Date: Thursday, May 10, 2018
Sheet 11 of 64
Designer: G.Mayers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UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
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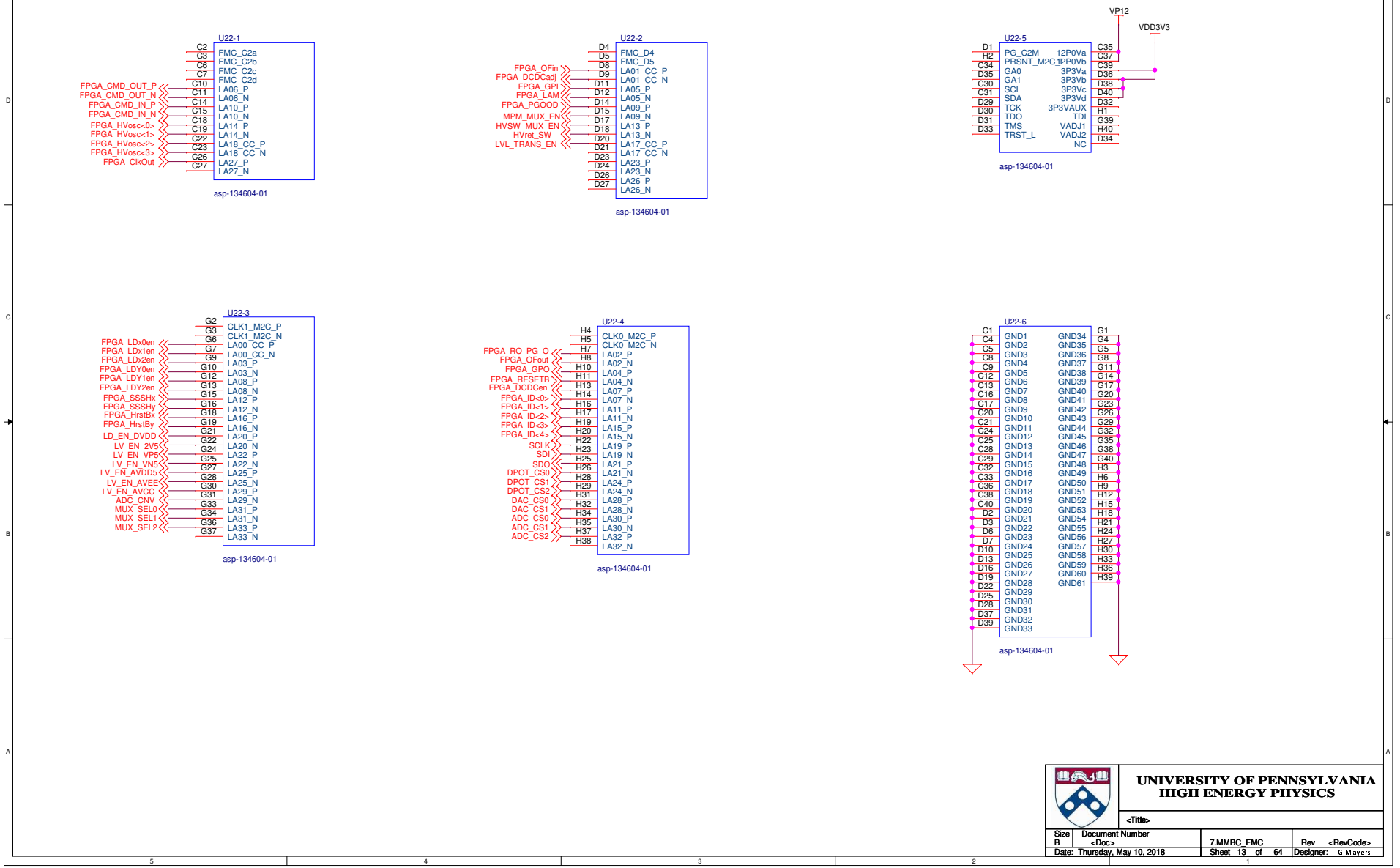
Date: Thursday, May 10, 2018
Sheet 12 of 64
Designer: G.Mayers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SDO H25 LA21_P
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U22-6
C1 GND1 GND34 G1
C4 GND2 GND35 G4
C5 GND3 GND36 G5
C8 GND4 GND37 G8
C9 GND5 GND38 G11
C12 GND6 GND39 G14
C13 GND7 GND40 G17
C16 GND8 GND41 G20
C17 GND9 GND42 G23
C20 GND10 GND43 G26
C21 GND11 GND44 G29
C24 GND12 GND45 G32
C25 GND13 GND46 G35
C28 GND14 GND47 G38
C29 GND15 GND48 G40
C32 GND16 GND49 H3
C33 GND17 GND50 H6
C36 GND18 GND51 H9
C38 GND19 GND52 H12
C40 GND20 GND53 H15
D2 GND21 GND54 H18
D3 GND22 GND55 H21
D6 GND23 GND56 H24
D7 GND24 GND57 H27
D10 GND25 GND58 H30
D13 GND26 GND59 H33
D16 GND27 GND60 H36
D19 GND28 GND61 H39
D22 GND29
D25 GND30
D28 GND31
D37 GND32
D39 GND33
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UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
<Title>
Size B
Document Number <Doc>
7.MMBC_FMC
Rev <RevCode>
Date: Thursday, May 10, 2018
Sheet 13 of 64
Designer: G.Mayers

3. VPOS LDO REGULATOR MODULES

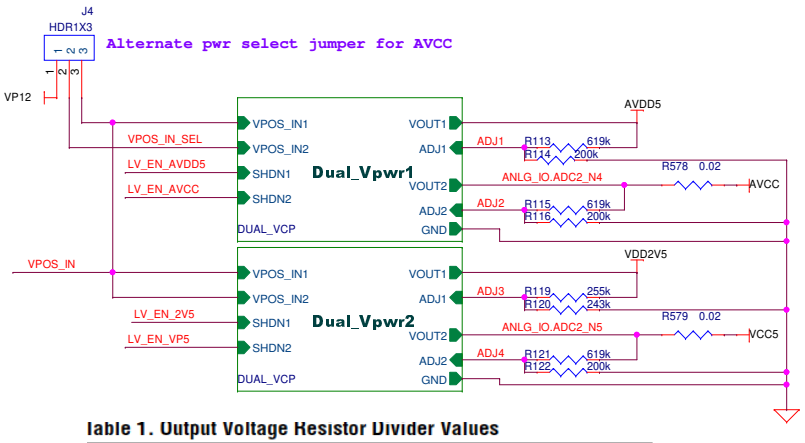
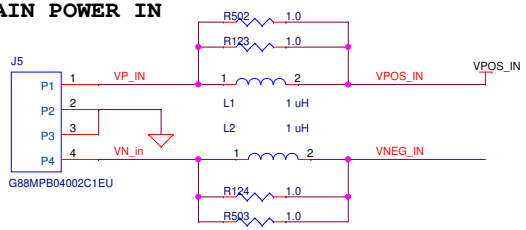


Table 1. Output Voltage Resistor Divider Values

V_{OUT} (V)	R1 (k)	R2 (k)
1.5	237	54.9
1.8	237	113
2.5	243	255
3	232	340
3.3	210	357
5	200	619

2. MAIN POWER IN



3. VNEG LDO REGULATOR MODULES

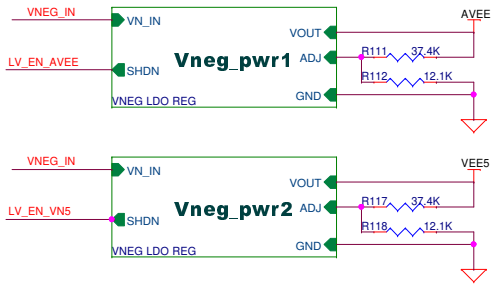
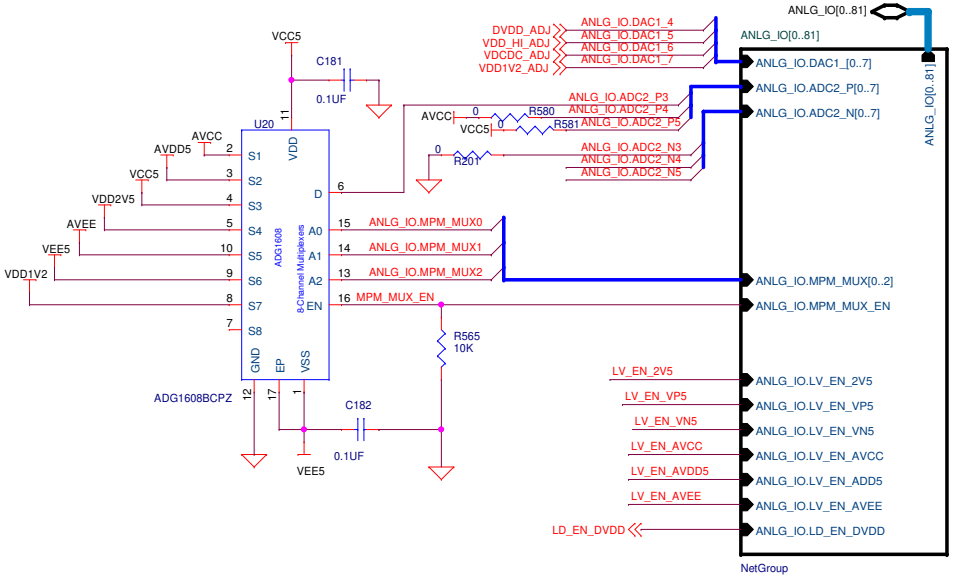


Table 1. Output Voltage Resistor Divider Values

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
-2.5	12.1	12.7
-3.0	12.1	17.8
-3.3	12.1	20.5
-5.0	12.1	37.4
-12.0	12.1	107
-15.0	12.4	140

4. MAIN POWER MONITOR & CONTROL



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HIGH ENERGY PHYSICS

MAIN POWER

Size	Document Number		Rev
B	<Doc>	8.Power	<RevCode>
Date: Thursday, May 10, 2018		Sheet 15 of 64	Designer: G.Mayers