

Jiangxi University of Science and Technology

DIGITAL DESIGN

Digital Integrated Circuits in Proteus





Introduction

- **Proteus software** has a big and vast collection of Digital IC library. This software can be used as an IC selector in digital circuits designing. Circuit designers don't need to waste time searching the availability of various IC's for the application. This library provides information of the IC's along with their commercial nomenclatures and manufacturer details.
- Components can be easily searched within the library using keywords like **AND Gate**, **OR Gate**, flip flops, decoders, counters etc. The description part provides information on the packages of the ICs, like the number of gates present in one IC etc. Preview is provided for ready reference of the component along with the PCB preview, and this makes it easy while converting the schematic model to PCB design.



Objective

- 1. Review students on using proteus software.
- 2. Introduce how to run simulation of designed digital circuit.
- 3. Understand how to applied digital logic equation to real hardware designs



Topics needed to be learnt before

- 1. Boolean algebra
- 2. Basic logic operation (for examples, and, or, not, and, etc.)
- 3. Basic knowledge of circuit design



Short intro to IC

In CMOS logic,

1. The **power dissipation** is usually 10nW per gate depending upon the power supply voltage, output load etc.
2. The CMOS components are usually **costly** but CMOS technology is **cheaper**.
3. **High** input impedance.

In TTL,

1. **Power dissipation** is usually 10nW per gate.
2. **Less** expensive components.
3. They are **less** susceptible to **damage** from electrostatic charge as compared to CMOS.

Short intro to IC



Classification by the Circuit Density

- SSI - several (less than 10) independent gates
- MSI - 10 to 200 gates; Perform elementary digital functions;
Decoder, adder, register, parity checker, etc
- LSI - 200 to few thousand gates; Digital subsystem
Processor, memory, etc
- VLSI - Thousands of gates; Digital system
Microprocessor, memory module

Classification by Technology

- TTL - Transistor-Transistor Logic
Bipolar transistors
NAND
- ECL - Emitter-coupled Logic
Bipolar transistor
NOR
- MOS - Metal-Oxide Semiconductor
Unipolar transistor
High density
- CMOS - Complementary MOS
Low power consumption



Short intro to IC

Logic Family (Silicon Technology)		Introduction	Features	Limitations
Transistor Logic Families (Bipolar Transistor Technology)	Saturated Logic Families (ON – Saturation Mode) (OFF – Cut Off Mode)	1. RTL (Resistor Transistor Logic)	<ul style="list-style-type: none"> - In common use before the development of ICs. Common Emitter Configuration. - Logic 1: 1-3.6 V and Logic 0: 0.2V 	<ul style="list-style-type: none"> - First logic family, require minimum number of transistors.
		2. DCTL (Direct Coupled Transistor Logic)	<ul style="list-style-type: none"> - Direct coupled transistors. - Base resistors of RTL are removed. 	<ul style="list-style-type: none"> - Simpler than RTL, easy to fabricate. - Fewer components hence economical.
		3. DTL (Diode Transistor Logic)	<ul style="list-style-type: none"> - Use diodes and transistors. - Input is fed through diodes followed by transistor at the output side. 	<ul style="list-style-type: none"> - First circuit configuration designed into IC. - Very small in size and high reliability at very low price. - Greater fan out and improved noise margins.
		4. TTL (Transistor-Transistor Logic)	<ul style="list-style-type: none"> - Use all transistors totem pole output. - Function of diodes in DTL is performed by multi-emitter transistor at input 	<ul style="list-style-type: none"> - Fast switching time, larger fan out. - Reduced silicon chip area. - Easy to interface with other logic families.
		5. IIL (Integrated Injection Logic)	<ul style="list-style-type: none"> - Merged Transistor Logic (MTL). - Both PNP and NPN transistors are used. - Designed around multi-collector inverting transistors. 	<ul style="list-style-type: none"> - High component density, less power dissipation. - Low metal interconnection. - Used in MSI and LSI designs.
	Non-Saturated Logic (ON – Active Mode) (OFF – Cut Off Mode)	6.ECL (Emitter Coupled Logic)	<ul style="list-style-type: none"> - Non saturated logic/Current mode logic. - Compliment output/eliminates the need of inverter. - Logic 1: -0.8 and Logic 0: -1.7 	<ul style="list-style-type: none"> - Fastest logic family - Used in very high frequency applications. - No noise spikes, large fan out.
MOS Logic Families (Unipolar Transistor Technology)	7.MOS Logic (Metal Oxide Semiconductor Logic)	<ul style="list-style-type: none"> - Use pMOS, nMOS or both with high packaging density. - Easy to design and fabricate - Less power drawn due to gate dielectric. 	<ul style="list-style-type: none"> - Lower power dissipation. - Shorter rise and fall times. - Large fan-out. 	<ul style="list-style-type: none"> - Larger propagation due to high output impedance. - Noise margin is around 1V.



Short intro to IC

Parameter	RTL	IIL	DTL	HTL	TTL	ECL	MOS	CMOS
Basic Gate	NOR	NOR	NAND	NAND	NAND	OR-NOR	NAND	NOR-NAND
Fan Out	5	Depends on Injector Current	8	10	10-20	25	20	20-50
Power Dissipation	12 mW	6 nW - 70 μW	8-12 mW	55 mW	10 mW	40-55 mW	0.2-10 mW	0.025-1.01 mW
Noise Immunity	Nominal	Poor	Good	Excellent	Very Good	Poor	Good	Very Good
Propagation Delay	12 nSec	25-30 nSec	30 nSec	4 nSec	10 nSec	1-2 nSec	300 nSec	70 nSec
Clock Rate	8 MHz	-	72 MHz	4 MHz	35 MHz	+60 MHz	2 MHz	10 MHz
Speed X Power	144	Less than 1	300	-	100	100	60	70

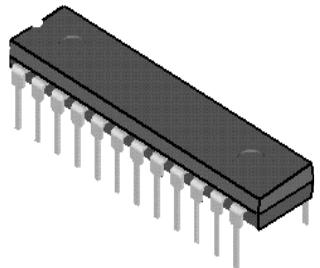
Short intro to IC

Device	Type	Description	Device	Type	Description
7404	TTL	Hex inverter	74LS08	LS TTL	Quad 2-input AND gate
74HC04	CMOS	Hex inverter	74HC08	CMOS	Quad 2-input AND gate
74HCU04	CMOS	Unbuffered Hex inverter	4081B	CMOS	Quad 2-input AND gate
74LS04	LS TTL	Hex inverter	74LS11	LS TTL	Triple 3-input AND gate
74LS05	LS TTL	Hex inverter with o.c. outputs	4073B	CMOS	Triple 3-input AND gate
7406	TTL	Hex inverter with o.c. outputs	74LS21	LS TTL	Dual 4-input AND gate
74LS14	LS TTL	Hex Schmitt inverter	4082B	CMOS	Dual 4-input AND gate
74HC14	CMOS	Hex Schmitt inverter			
4049UB	CMOS	Unbuffered Hex inverter			
74HC4049	CMOS	Hex inverter			
4069UB	CMOS	Unbuffered Hex inverter			
4502B	CMOS	Hex 3-state inverter			
40106B	CMOS	Hex Schmitt inverter			
74LS240	LS TTL	Octal 3-state Schmitt inverter			

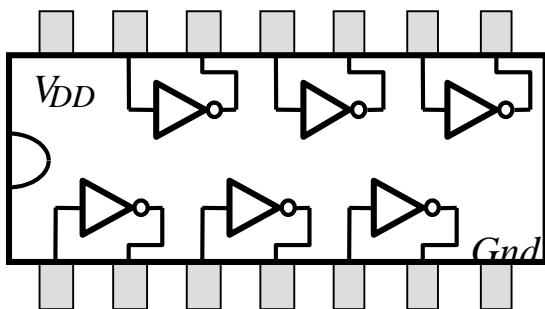
Short intro to IC

IC number	Purpose
4000	Dual 3-input NOR gate + 1 Inverter
4001	Quad 2-input NOR gate
4002	Dual 4-input NOR gate
4025	Triple 3-input NOR gate
4043	Quad NOR R/S latch
4078	8-input NOR gate
4572	Hex gate , quad NOT, single NAND, single NOR
741G02	single 2-input NOR gate
7403	quad 2-input NAND gate with open collector outputs
7423	expandable dual 4-input NOR gate with strobe
7425	dual 4-input NOR gate with strobe
7427	triple 3-input NOR gate
741G27	single 3-input NOR gate
7428	quad 2-input NOR buffer
7433	quad 2-input NOR buffer with open collector outputs
7436	quad 2-input NOR gate (different pin out than 7402)
74128	quad 2-input NOR Line driver
74135	quad exclusive-or/NOR gate
74232	quad NOR Schmitt trigger
74260	dual 5-input NOR gate
74805	hex 2-input NOR drivers
744002	dual 4-input NOR gate
744078	8-input OR/NOR gate

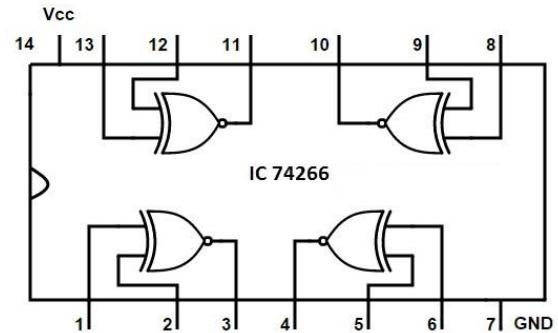
Standard Logic Gate: Pin-out



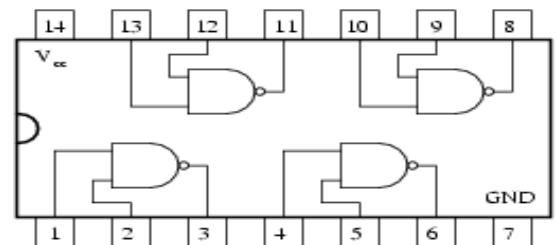
(a) Dual-inline package



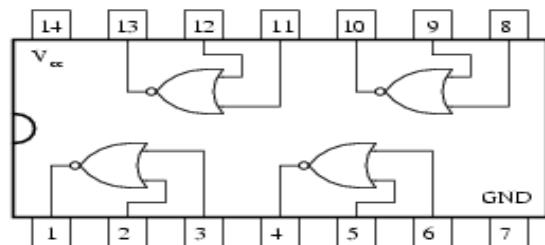
(b) Structure of 7404 chip



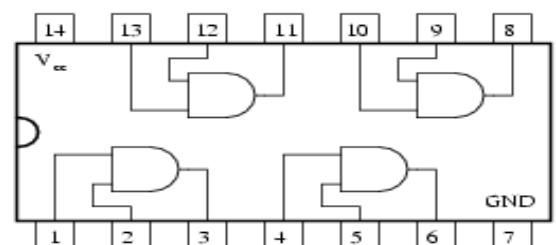
5400/7400
Quad NAND gate



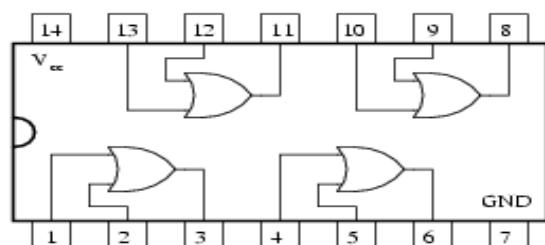
5402/7402
Quad NOR gate



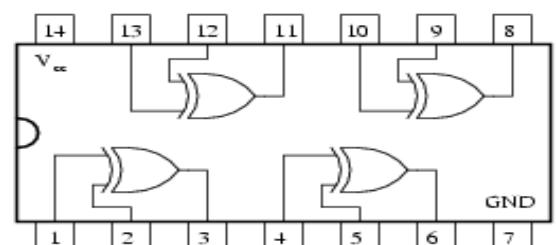
5408/7408
Quad AND gate



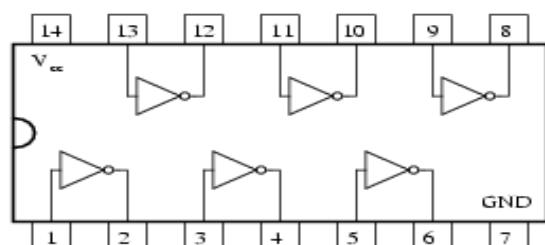
5432/7432
Quad OR gate



5486/7486
Quad XOR gate



5404/7404
Hex inverter



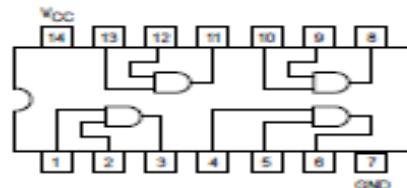
The differences between TTL (transistor-transistor logic) and CMOS (Complementary Metal-oxide semiconductor) are -

1. TTL circuits use bipolar junction transistors (BJTs) while CMOS circuits use field effect transistors (FETs) ie., by connecting NMOS and PMOS (MOSFETs).
2. A single logic gate in a CMOS chip can consist of as little as two FETs while a logic gate in a TTL chip can consist of a substantial number of parts as extra components like resistors are needed.
3. A single gate in a CMOS chip can consume around 10nW while an equivalent gate on a TTL chip can consume around 10mW of power, which is why CMOS is the preferred chip in mobile devices where power is supplied by a limited source like a battery.
4. CMOS are more susceptible to electrostatic discharge. Mere touching the terminals induce enough static electricity to damage the device permanently.
5. The basic gates used in standard TTL are NAND gates while NAND-NOR gates are used in CMOS circuits.
6. Fan-out(number of standard loads that can be connected to the output of the gate under normal operation) for TTL is 10 while it is 50 for CMOS.
7. Propagation delay for TTL is 10 ns and for CMOS, it is 70 ns.
8. Fan-in (Number of inputs that can be connected to a gate) for TTL is around 12–14 and it is greater than 10 for CMOS.
9. For TTL, the noise margin is 0.5 V while for CMOS, it is 1.5V .
10. Noise immunity of CMOS is a lot better than TTL circuits.
11. CMOS circuits are simpler to construct and has a higher packing density than TTL logic family.

Standard Logic Gate: Pin-out



QUAD 2-INPUT AND GATE



SN54/74LS08

QUAD 2-INPUT AND GATE
LOW POWER SCHOTTKY



ORDERING INFORMATION

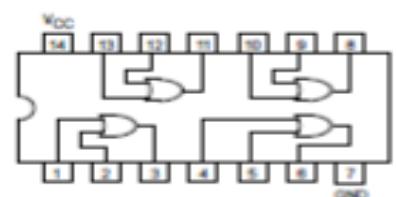
SN54LS08J Ceramic
SN74LS08N Plastic
SN74LS08D SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter	54	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	4.75	5.0	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA



QUAD 2-INPUT OR GATE



SN54/74LS32

QUAD 2-INPUT OR GATE
LOW POWER SCHOTTKY



ORDERING INFORMATION

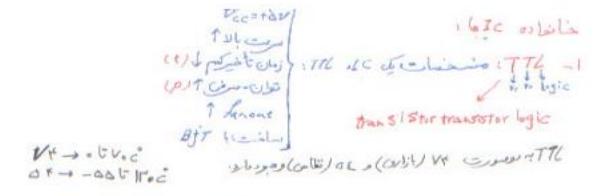
SN54LS32J Ceramic
SN74LS32N Plastic
SN74LS32D SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter	54	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	4.75	5.0	V
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I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA



Standard Logic Gate: Pin-out



T	P
medium	medium
High	Low
L	H
L	m ⁺
L	m
L	L

انواع استادار: TTL
 ۱- لجع کم منی
 ۲- لجع شاکن
 ۳- لجع تکمیلی
 ۴- لجع تکمیلی با شرط های محدود پس از
 ۵- لجع مبتنی بر CMOS

NAND	C ₄ = V _{cc}
NOR	C ₄ = V _{cc}
AND	C ₄ = V _{cc}
OR	C ₄ = V _{cc}
NOT	C ₄ = V _{cc}

متخصصات TTL: C₄ = V_{cc}

MOSFET	متخصصات با تکنولوژی CMOS
V _{cc} = 3.6V _{cc}	متخصصات با تکنولوژی CMOS
مخرج	complementary metal-oxide Semiconductor
Noise	噪聲

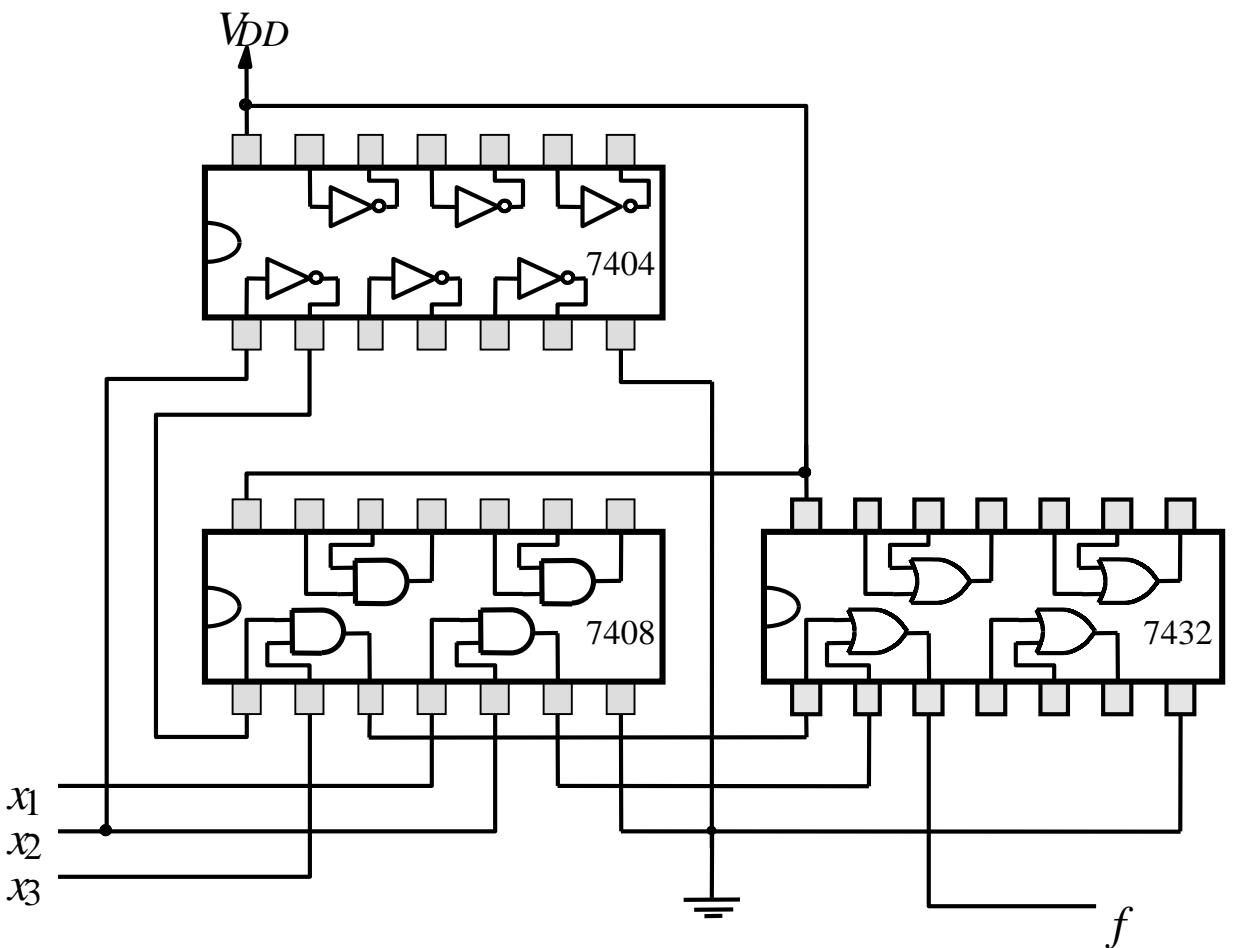
متخصصات CMOS: V_{cc} = 3.6V_{cc}

انواع CMOS: V_{cc} = V_{cc} + V_{cc} = V_{cc} + V_{cc}

Example

Draw the circuit diagram and the wiring diagram for the following Boolean expression:

$$F = x_2' \cdot x_3 + x_1 \cdot x_2$$





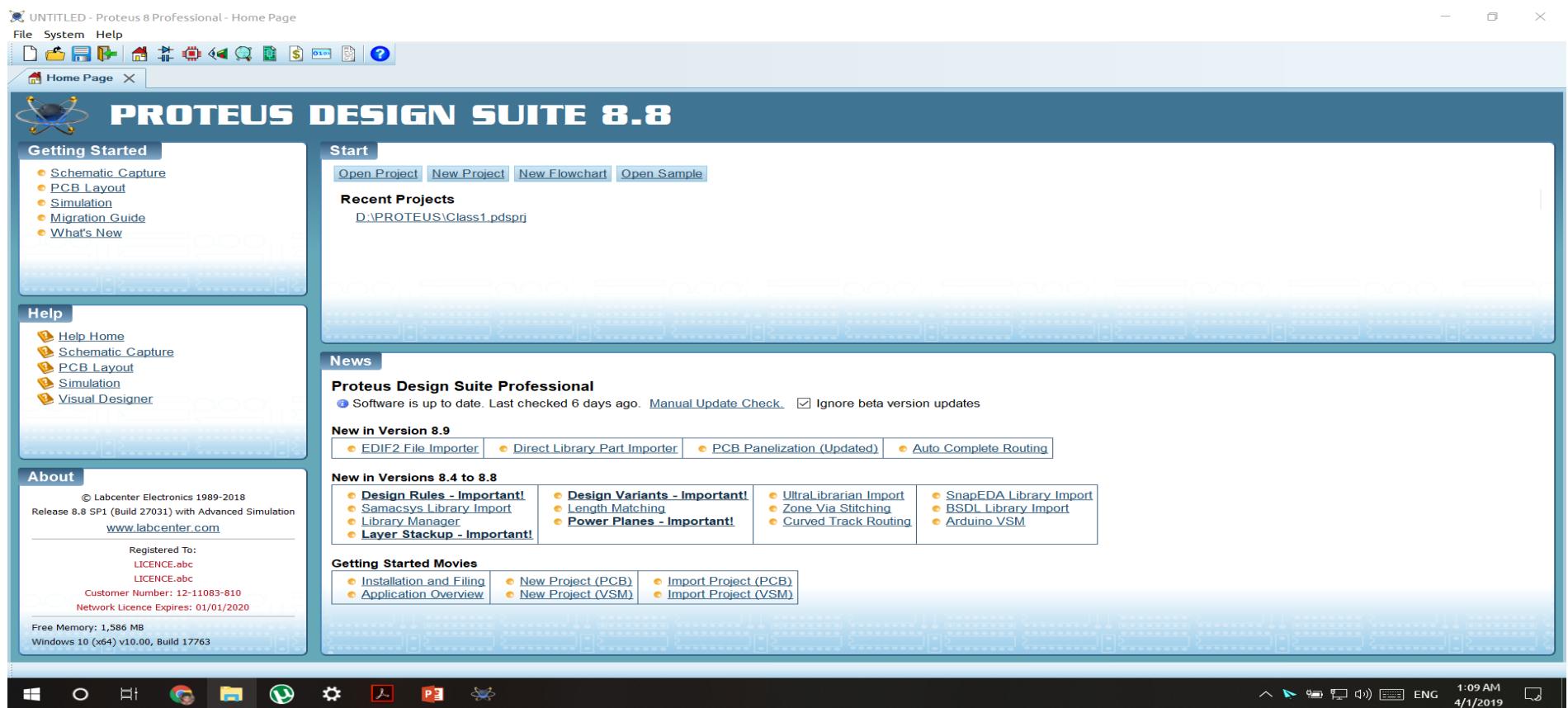
Design techniques to keep in mind

- Do not leave any of the input pins of IC's open, i.e. on the floating state unless it is mentioned in the datasheet about internal pull-up/pull down availability.
- Use resistors of suitable values, mostly 10K for external pull up or pull down.
- Using external pull up or pull down is must, while using manual switches as inputs.
- Use resistors of suitable values for LED loads. Do not connect LEDs directly to the outputs even for simulation purpose, as it may lead to incorrect operation of the circuit due to shifting of voltage levels.
- It is advised to set model type of resistors in the resistor properties to Digital while using them with Digital ICs in the simulation software.
- While analyzing circuits with Oscilloscope, set the channels to DC mode.
- Use Bus mode of wiring for connections if there are too many ICs or if the wiring is untidy.
- All the power pins like Vcc and GND of the ICs are internally connected and those pins are hidden.
- One can view the hidden pins of an IC in its properties tab. Right-click on the component and select edit properties.

Getting started

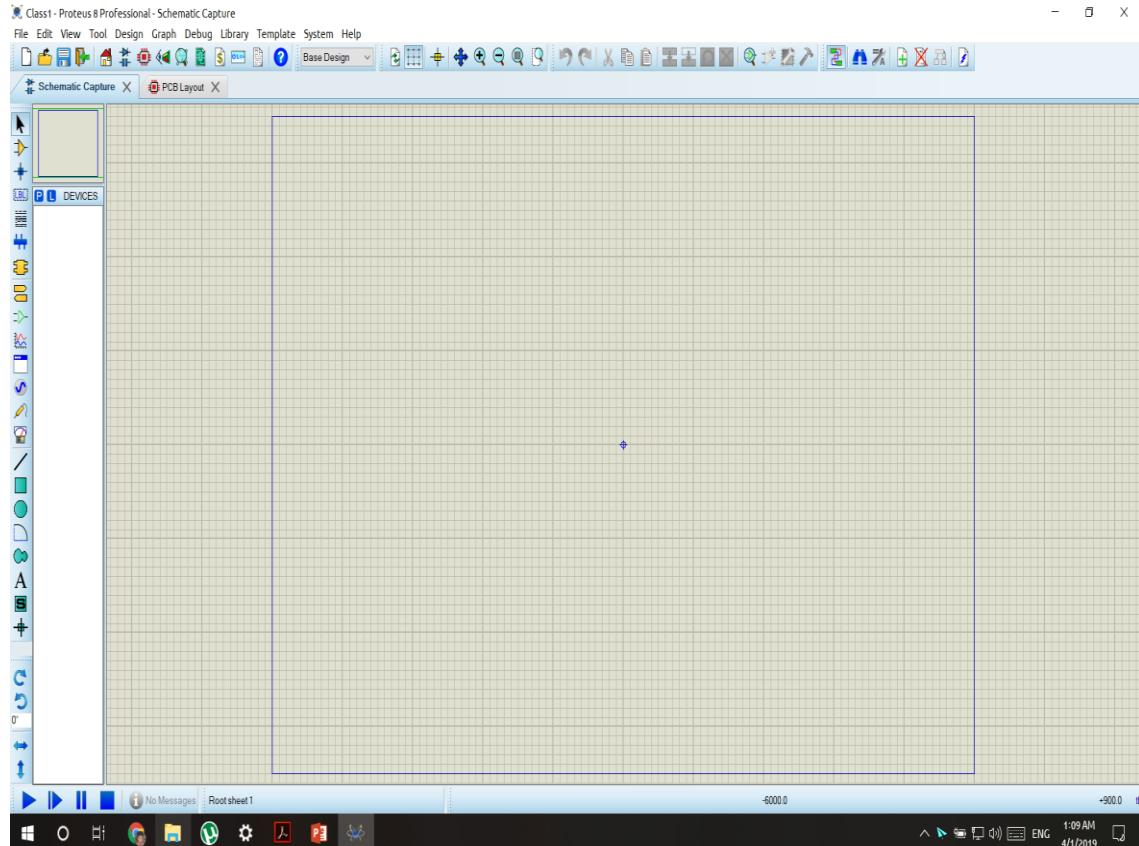


- Open Proteus Design Suite and create a new project





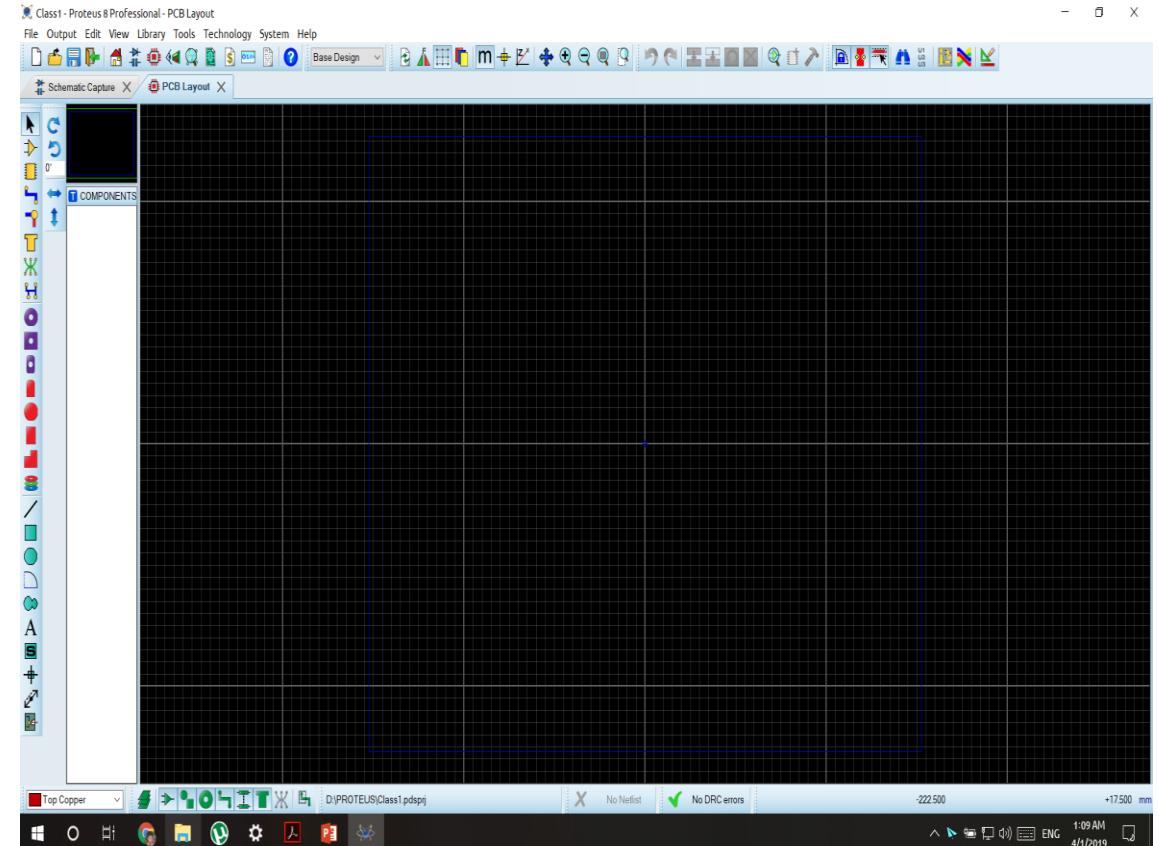
Environment of proteus



Schematic Capture Tab



江西理工大学
JIANGXI UNIVERSITY OF SCIENCE AND TECHNOLOGY



PCB Layout Tab

PROTEUS

©Lab Center Electronics Ltd.



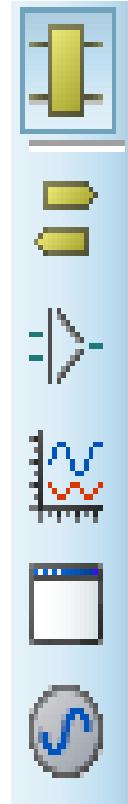
- **ISIS:** Intelligent Schematic Input System - for drawing circuit diagrams etc.
- **LISA:** Lab-center Integrated Simulation Architecture - for simulation of circuit diagram. Separate handout.
- **ARES:** Advanced Routing and Editing Software - for producing pcb layout drawings.



MODES



- Selection Mode
- Component Mode
- Junction Dot Mode
- Wire Level Mode
- Text Script Mode
- Buses Mode



- Subcircuit Mode
- Terminals Mode
- Device Pins Mode
- Graph Mode
- Active Pop-up Mode
- Generator Mode



- Probe Mode
- Virtual Instrumentation Mode

2D Graphics Mode





Component Mode: P=>Pick Device & L=>Library

Subcircuit Mode: Different Ports, like-

Input, Output, Bidir, Power, Ground & Bus.

Terminals Mode: Different Terminals, like-

Input, Output, Bidir, Power, Ground & Bus.

Device Pins Mode: Invert, Posclk, Negclk, Short & Bus.

Graphs Mode: Analogue, Digital, Frequency, Transfer, Noise, Distortion, Fourier, Audio, Interactive, Conformance, DCSweep & AC Sweep.



Generators Mode: DC, Sine, Pulse, Exp, SFFM, PWLIN, File, Audio, Dstate, Dedge, Dpulse, Dclock, Dpattern & Scriptable.

Probes Mode: Voltage, Current & Tape probe.

Instruments Mode: Oscilloscope, Logic Analyser, Counter Timer, Virtual Terminal, SPI Debugger, 12C Debugger, Signal Generator, Pattern Generator, DC-Voltmeter, DC-Ammeter, AC-Voltmeter & AC-Ammeter.



ARES is used for PCB Designing

Another important of ARES is 3D visualization of the circuit

It also has different modes like ISIS



MODES

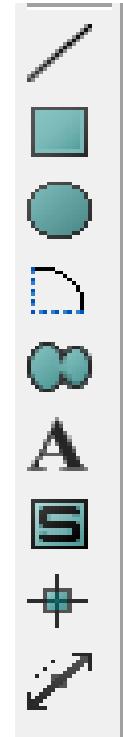


- Selection Mode
- Component Mode
- Package Mode
- Track Mode
- Via Mode
- Zone Mode



- Ratnest Mode
- Connectivity Highlight Mode

Pad Mode



2D Graphics Mode

- Dimension Mode



ROUTING:

- Auto Routing (Not Recommended)
- Manual Routing (More Practical)



Some Important Facts in PCB Designing:



- Layer Selection
- Mirror Bottom Layer
- Output Format Selection





Lets see some Examples in our Workspace



Class1 - Proteus 8 Professional - Schematic Capture

File Edit View Tool Design Graph Debug Library Template System Help

Schematic Capture X PCB Layout X

Pick Devices

Keywords: And Gate

Results (385):

Device	Library	Description
4000	CMOS	Dual 3-Input NOR Gate And Inverter
4000.IEC	CMOS	Dual 3-Input NOR Gate And Inverter
4007	CMOS	Dual Complementary Pair And Inverter
4011	CMOS	Quad 2-Input NAND Gate
4011.DM	CMOS	Quad 2-Input NAND Gate
4011.IEC	CMOS	Quad 2-Input NAND Gate
4012	CMOS	Dual 4-Input NAND Gate
4012.DM	CMOS	Dual 4-Input NAND Gate
4012.IEC	CMOS	Dual 4-Input NAND Gate
4023	CMOS	Triple 3-Input NAND Gate
4023.DM	CMOS	Triple 3-Input NAND Gate
4023.IEC	CMOS	Triple 3-Input NAND Gate
4068	CMOS	8-Input NAND Gate
4068.DM	CMOS	8-Input NAND Gate
4068.IEC	CMOS	8-Input NAND Gate
4073	CMOS	Triple 3-Input AND Gate
4073.DM	CMOS	Triple 3-Input AND Gate
4073.IEC	CMOS	Triple 3-Input AND Gate
4081	CMOS	Quad 2-Input AND Gate
4081.DM	CMOS	Quad 2-Input AND Gate
4081.IEC	CMOS	Quad 2-Input AND Gate
4082	CMOS	Dual 4-Input AND Gate
4082.DM	CMOS	Dual 4-Input AND Gate
4082.IEC	CMOS	Dual 4-Input AND Gate
4085	CMOS	Dual 2-Wide 2-Input AND-OR-Invert Gate
4085.IEC	CMOS	Dual 2-Wide 2-Input AND-OR-Invert Gate
4093	CMOS	Quad 2-Input NAND Schmitt-Trigger
4093.DM	CMOS	Quad 2-Input NAND Schmitt-Trigger
4093.IEC	CMOS	Quad 2-Input NAND Schmitt-Trigger
7400	74STD	Quadruple 2-Input Positive-NAND Gates
7400.DM	74STD	Quadruple 2-Input Positive-NAND Gates
7400.IEC	74STD	Quadruple 2-Input Positive-NAND Gates
7401	74STD	Quad 2-Input Open-Collector NAND Gate
7401.DM	74STD	Quad 2-Input Open-Collector NAND Gate
7401.IEC	74STD	Quad 2-Input Open-Collector NAND Gate
7403	74STD	Quadruple 2-Input Positive-NAND Buffer With Open-Collector Outputs
7403.IEC	74STD	Quadruple 2-Input Positive-NAND Buffer With Open-Collector Outputs

4081 Preview: Schematic Model [40AND2]

PCB Preview:

DIL14

OK Cancel

No Messages Root sheet1

Windows Taskbar: File Explorer, Microsoft Edge, Task View, Settings, People, Power, Taskbar settings, 1:14 AM, ENG, 4/1/2019

Basic Design steps

- Click on the BLUE P Button
- Search your desired gate and it will show all related gates to your searched term
- Click OK to add them to your inventory for later use



Schematic Capture X PCB Layout X

Pick Devices

Keywords: or gate

Match Whole Words?

Show only parts with models?

Category: (All Categories) CMOS 4000 series Modelling Primitives Simulator Primitives TTL 74 series TTL 74ALS series TTL 74AS series TTL 74F series TTL 74HC series TTL 74HCT series TTL 74LS series TTL 74S series

Sub-category:

Manufacturer:

Results (318):

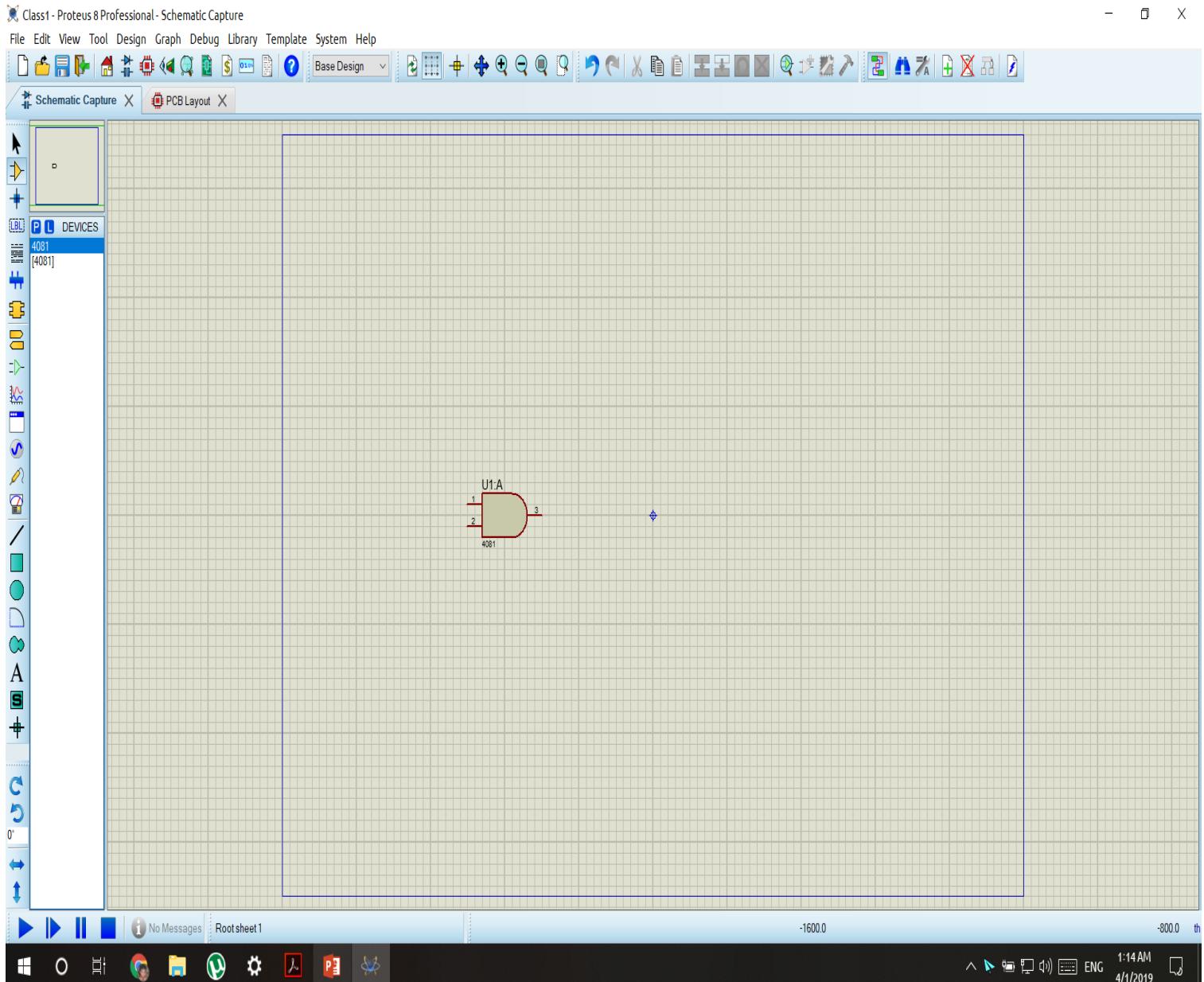
Device	Library	Description
4000	CMOS	Dual 3-Input NOR Gate And Inverter
4000.IEC	CMOS	Dual 3-Input NOR Gate And Inverter
4001	CMOS	Quad 2-Input NOR Gate
4001.DM	CMOS	Quad 2-Input NOR Gate
4001.IEC	CMOS	Quad 2-Input NOR Gate
4002	CMOS	Dual 4-Input NOR Gate
4002.DM	CMOS	Dual 4-Input NOR Gate
4002.IEC	CMOS	Dual 4-Input NOR Gate
4025	CMOS	Triple 3-Input NOR Gate
4025.DM	CMOS	Triple 3-Input NOR Gate
4025.IEC	CMOS	Triple 3-Input NOR Gate
4030	CMOS	Quad XOR Gate
4030.IEC	CMOS	Quad XOR Gate
4070	CMOS	Quad XOR Gate
4070.IEC	CMOS	Quad XOR Gate
4071	CMOS	Quad 2-Input OR Gate
4071.DM	CMOS	Quad 2-Input OR Gate
4071.IEC	CMOS	Quad 2-Input OR Gate
4072	CMOS	Dual 4-Input OR Gate
4072.DM	CMOS	Dual 4-Input OR Gate
4072.IEC	CMOS	Dual 4-Input OR Gate
4075	CMOS	Triple 3-Input OR Gate
4075.DM	CMOS	Triple 3-Input OR Gate
4075.IEC	CMOS	Triple 3-Input OR Gate
4077	CMOS	Quad XNOR Gate
4077.IEC	CMOS	Quad XNOR Gate
4078	CMOS	8-Input NOR Gate
4078.DM	CMOS	8-Input NOR Gate
4078.IEC	CMOS	8-Input NOR Gate
4085	CMOS	Dual 2-Wide 2-Input AND-OR-Invert Gate
4085.IEC	CMOS	Dual 2-Wide 2-Input AND-OR-Invert Gate
4530	CMOS	Dual 5-Input Majority Gate
7401	74STD	Quad 2-Input Open-Collector NAND Gate
7401.DM	74STD	Quad 2-Input Open-Collector NAND Gate
7401.IEC	74STD	Quad 2-Input Open-Collector NAND Gate
7402	74STD	Quadruple 2-Input Positive-NOR Gates
7402.DM	74STD	Quadruple 2-Input Positive-NOR Gates

4071 Preview: Schematic Model [400R2]

PCB Preview: DIL14

OK Cancel





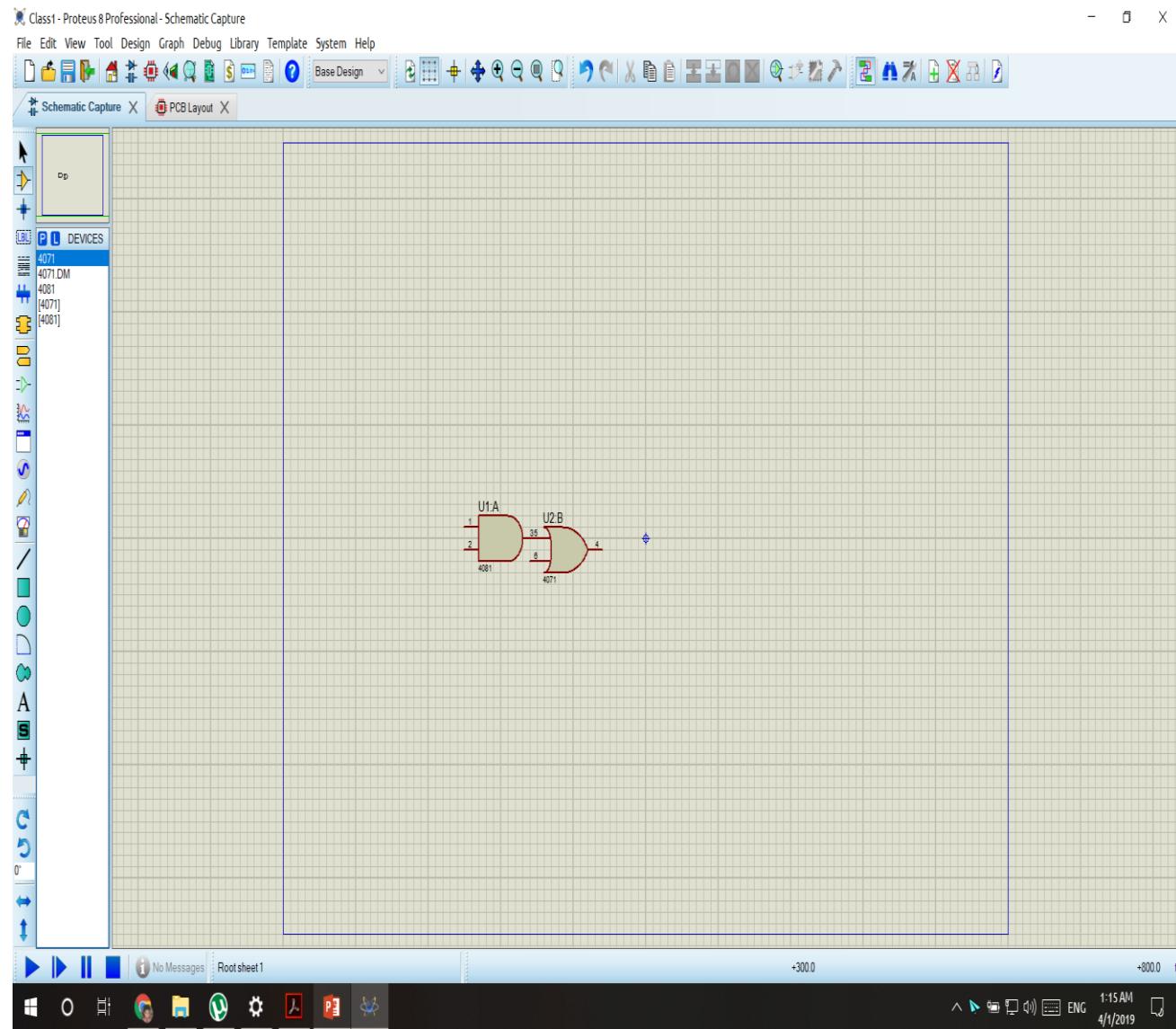
Basic DESIGN STEPS

- Click on your desired gate from your inventory now
- Click on any empty space on your schematic capture tab
- And now drag and position your gate as per your requirement





You can now add more gates and devices and connect them with dragging only





OR GATE

- If any one of the inputs of OR Gate is HIGH, then the output of OR Gate is HIGH. If the inputs are applied manually using switches, the inputs must be pulled down for active high inputs and pulled up for active low inputs.
- OR Gates with inputs up to 12 are available for simulation. However, for hardware implementation, the designer has to confirm their availability in the market from time-to-time

AND GATE

- If all the inputs of AND Gate are HIGH, then the output of AND Gate is HIGH. If the inputs are applied manually using switches, the inputs must be pulled down for active high inputs and pulled up for active low inputs.
- AND Gates with inputs up to 8 are available for simulation. However, for hardware implementation, the designers have to confirm their availability in the market from time-to-time



Proteus Chapter 6 Digital Integrated Circuits - ISIS Professional

File View Edit Tools Design Graph Source Debug Library Template System Help

Pick Devices

Keywords: AND GATE

Match Whole Words?

Show only parts with models?

Category: [All Categories]

Device	Library	Description
4000	CMOS	
4000.IEC	CMOS	
4007	CMOS	
4011	CMOS	
4011.DM	CMOS	
4011.IEC	CMOS	
4012	CMOS	
4012.DM	CMOS	
4012.IEC	CMOS	
4023	CMOS	
4023.DM	CMOS	
4023.IEC	CMOS	
4068	CMOS	
4068.DM	CMOS	
4068.IEC	CMOS	
4073	CMOS	
4073.DM	CMOS	
4073.IEC	CMOS	
4081	CMOS	
4081.DM	CMOS	

Pick Devices

Keywords: OR GATE

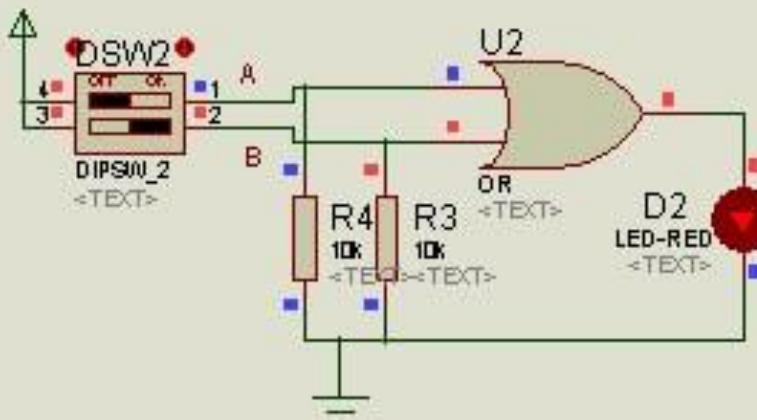
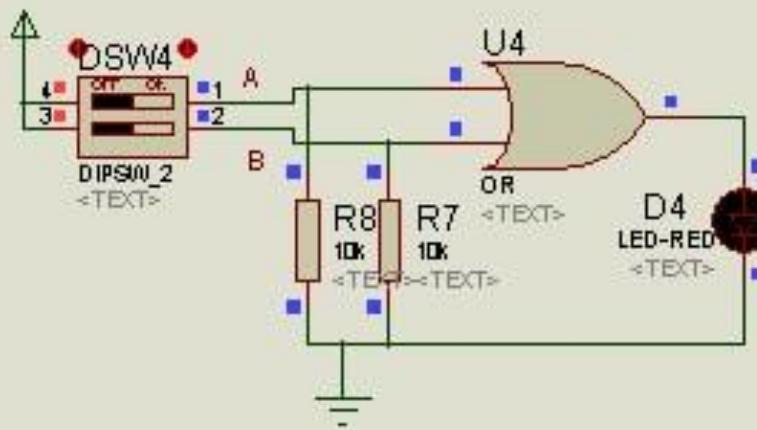
Match Whole Words?

Show only parts with models?

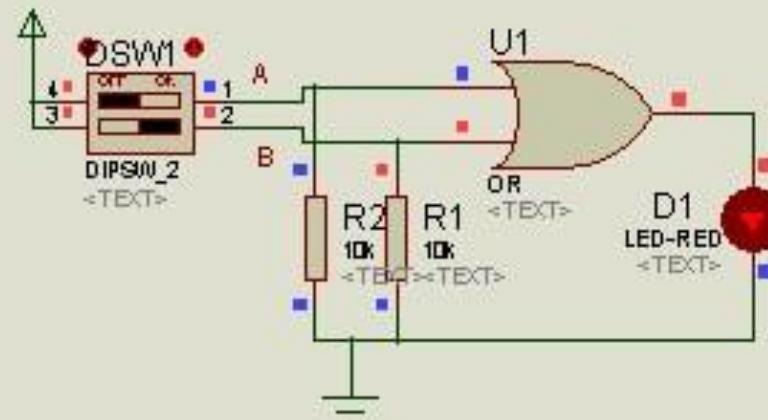
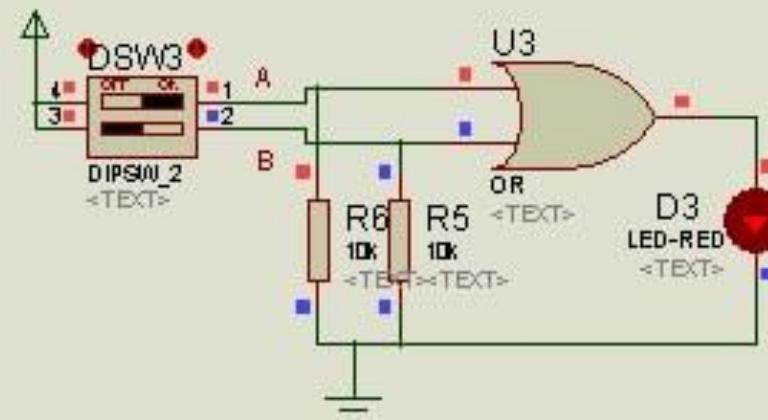
Category: [All Categories]

Device	Library	Description
4071	CMOS	Quad 2-Input OR Gate
4071.DM	CMOS	Quad 2-Input OR Gate
4071.IEC	CMOS	Quad 2-Input OR Gate
4072	CMOS	Dual 4-Input OR Gate
4072.DM	CMOS	Dual 4-Input OR Gate
4072.IEC	CMOS	Dual 4-Input OR Gate
4075	CMOS	Triple 3-Input OR Gate
4075.DM	CMOS	Triple 3-Input OR Gate
4075.IEC	CMOS	Triple 3-Input OR Gate
4085	CMOS	Dual 2-Wide 2-Input AND-OR-Invert Gate
4085.IEC	CMOS	Dual 2-Wide 2-Input AND-OR-Invert Gate
7450	74STD	Dual 2 Wide 2-Input AND-OR Gate
74HC4072	74HC	Dual 4-Input OR Gate
74HC4072.DM	74HC	Dual 4-Input OR Gate
74HC4072.IEC	74HC	Dual 4-Input OR Gate
74S64	74S	4-2-3-2 Input AND-OR-Invert Gate With Totem-Pole Outputs
74S65	74S	4-2-3-2 Input AND-OR-Invert Gate With Open-Collector Outputs
NOR_2	DSIMMDLS	NOR (Negative-OR) Gate Digital Primitive Model
NOR_2.DM	DSIMMDLS	NOR (Negative-OR) Gate Digital Primitive Model
NOR_3	DSIMMDLS	NOR (Negative-OR) Gate Digital Primitive Model

Basic Two Input OR Gate

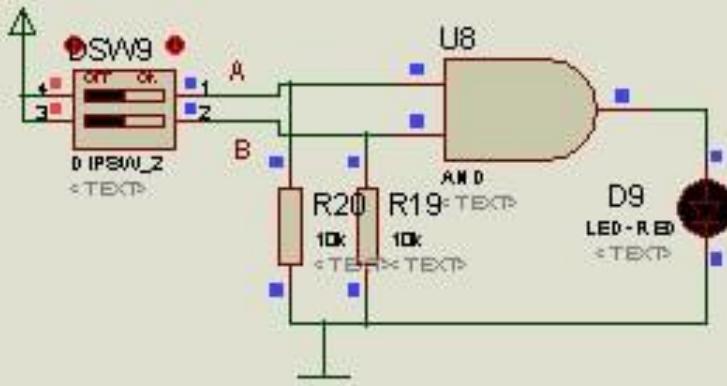


A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

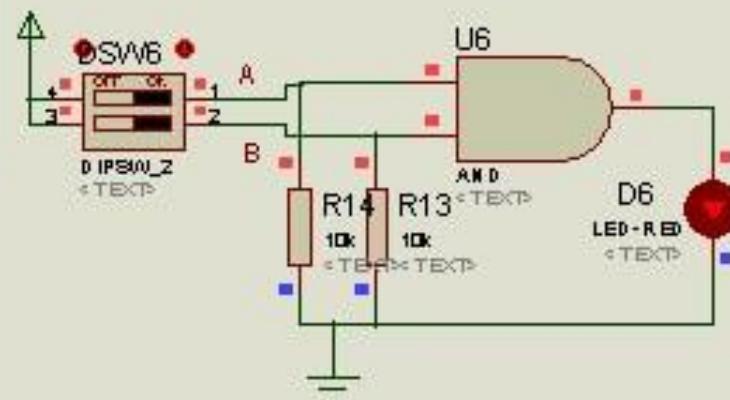
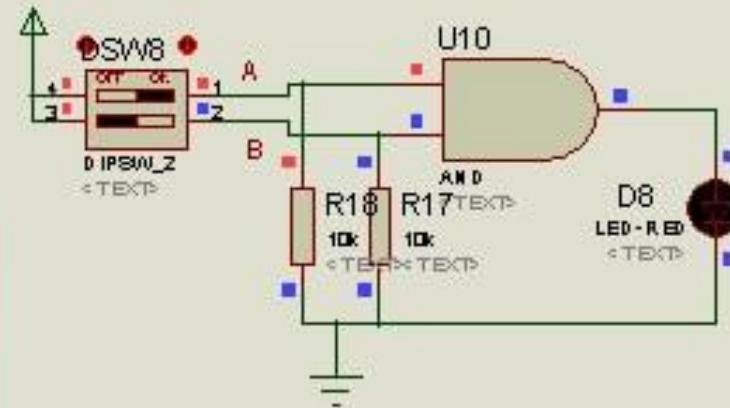




Basic Two Input AND Gate

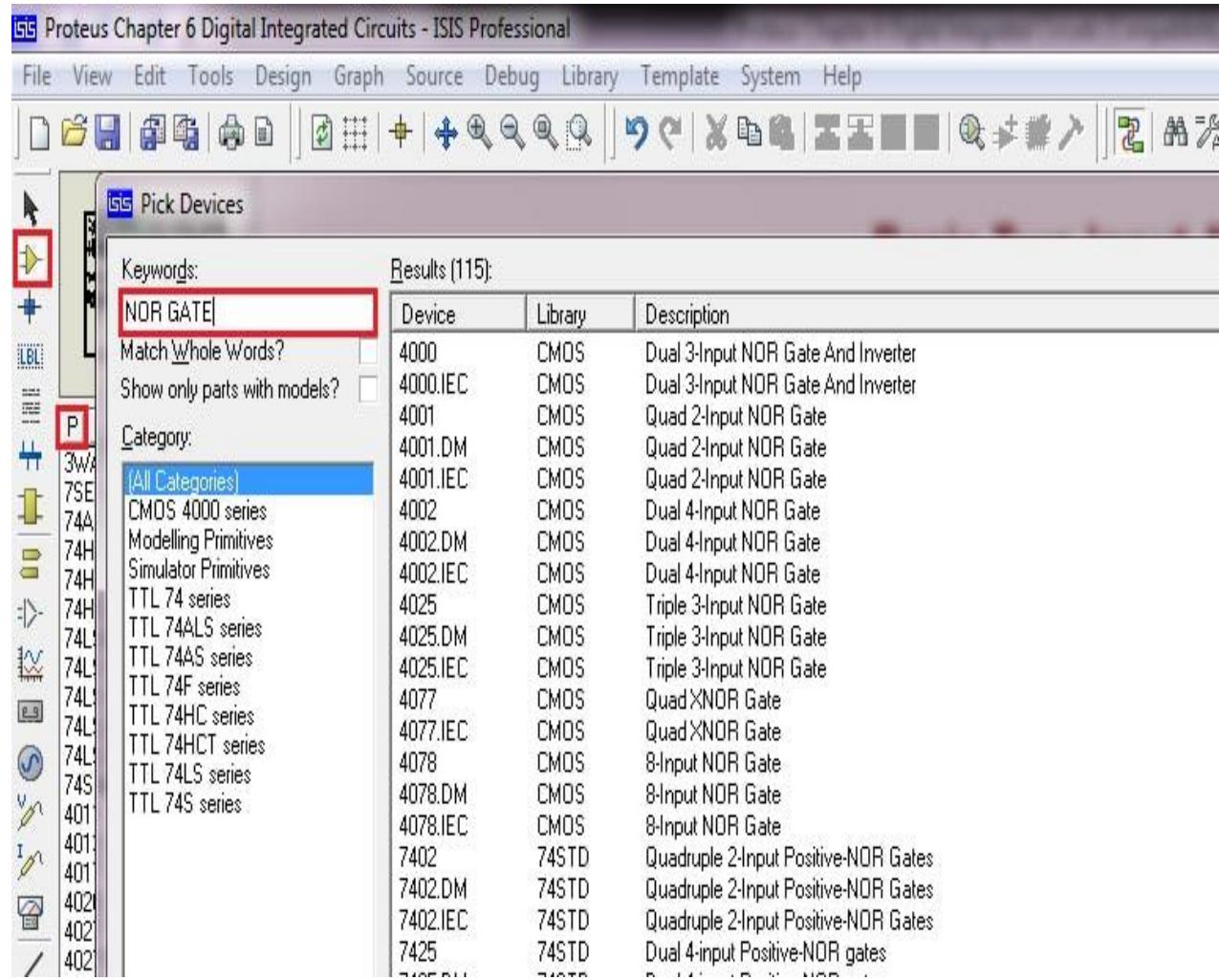


Truth Table		
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

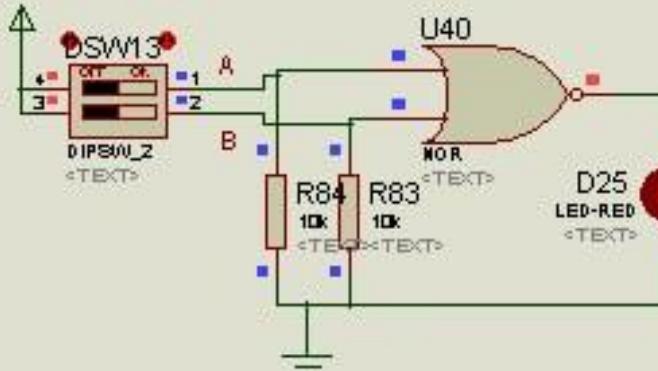


Nor gate

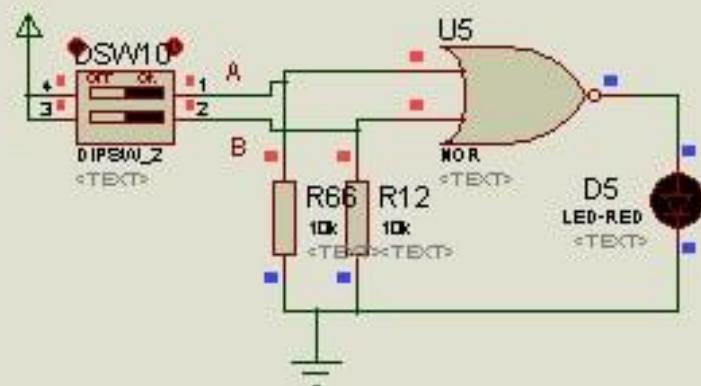
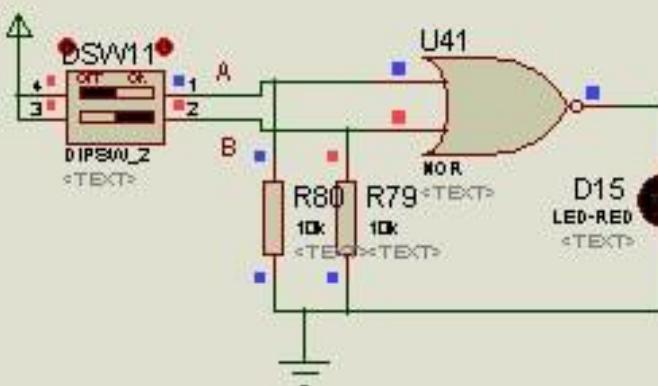
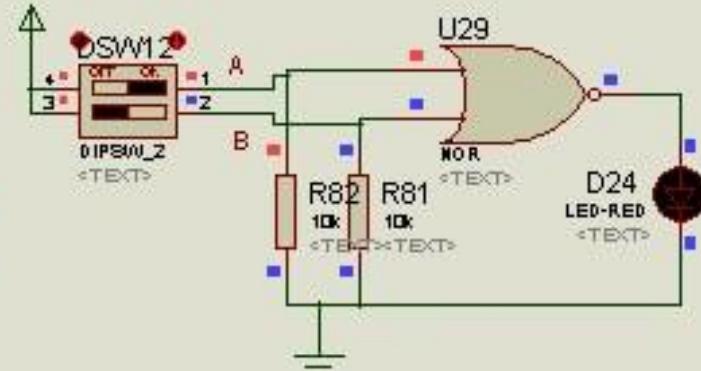
- If any one of the inputs of NOR Gate is HIGH then the output of NOR Gate is LOW. The output is HIGH only when all the inputs are LOW.
- NOR Gate is one of the two universal gates i.e. any logic can be derived using NOR gate. NOR Gates with inputs up to 8 are available for simulation.



Basic Two Input NOR Gate



Truth Table		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0



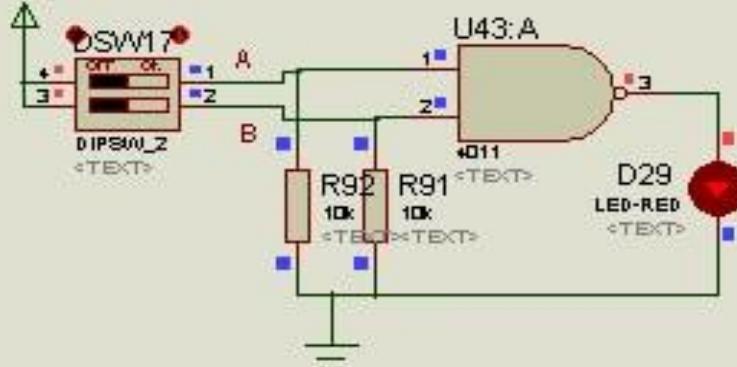


NAND Gate

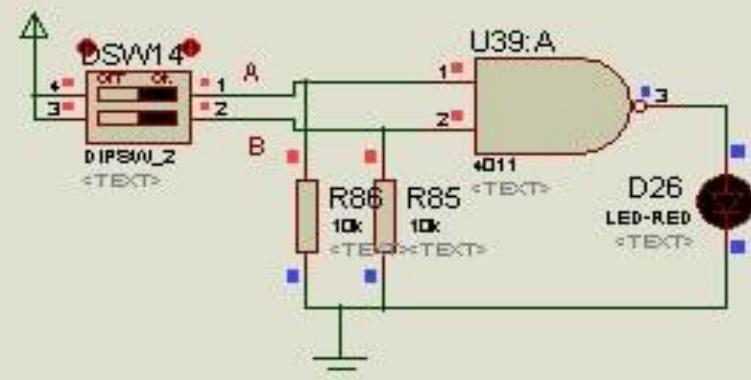
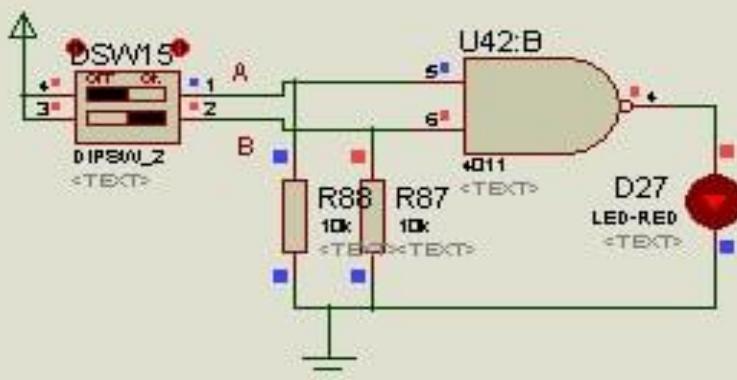
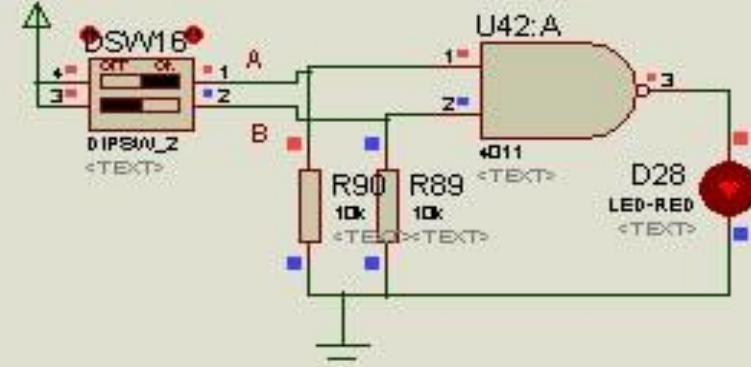
- If any one of the inputs of NAND Gate is LOW then the output of NAND Gate is HIGH. The output is LOW only when all the inputs are HIGH. NAND Gate is one of the two universal gates i.e. any logic can be derived using NAND gates. NAND Gates with inputs up to 13 are available for simulation.

Device	Library	Description
4011	CMOS	Quad 2-Input NAND Gate
4011.DM	CMOS	Quad 2-Input NAND Gate
4011.IEC	CMOS	Quad 2-Input NAND Gate
4012	CMOS	Dual 4-Input NAND Gate
4012.DM	CMOS	Dual 4-Input NAND Gate
4012.IEC	CMOS	Dual 4-Input NAND Gate
4023	CMOS	Triple 3-Input NAND Gate
4023.DM	CMOS	Triple 3-Input NAND Gate
4023.IEC	CMOS	Triple 3-Input NAND Gate
4068	CMOS	8-Input NAND Gate
4068.DM	CMOS	8-Input NAND Gate
4068.IEC	CMOS	8-Input NAND Gate
4093	CMOS	Quad 2-Input NAND Schmitt-Trigger
4093.DM	CMOS	Quad 2-Input NAND Schmitt-Trigger
4093.IEC	CMOS	Quad 2-Input NAND Schmitt-Trigger
7400	74STD	Quadruple 2-Input Positive-NAND Gates
7400.DM	74STD	Quadruple 2-Input Positive-NAND Gates
7400.IEC	74STD	Quadruple 2-Input Positive-NAND Gates
7401	74STD	Quad 2-Input Open-Collector NAND Gate
7401.DM	74STD	Quad 2-Input Open-Collector NAND Gate
7401.IEC	74STD	Quad 2-Input Open-Collector NAND Gate

Basic Two Input NAND Gate

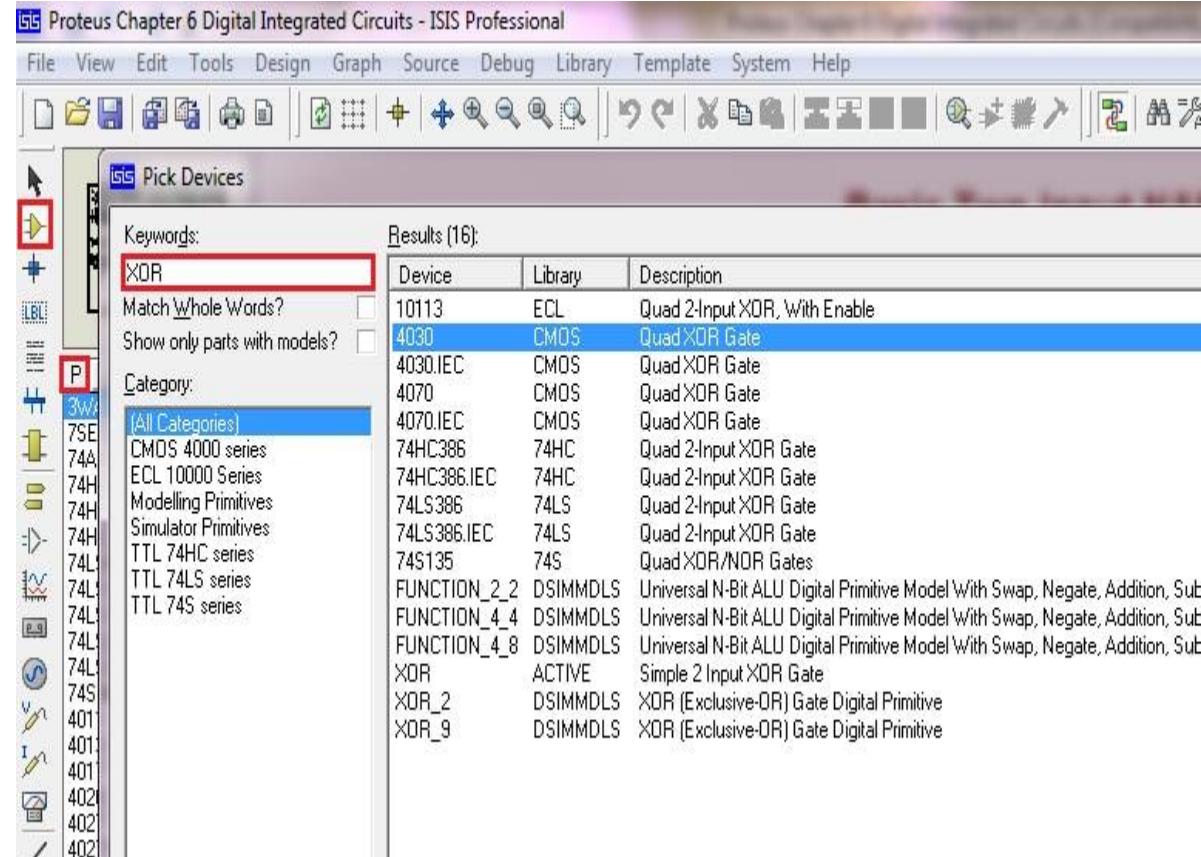


Truth Table		
A	B	$\bar{A} \cdot \bar{B}$
0	0	1
0	1	1
1	0	1
1	1	0

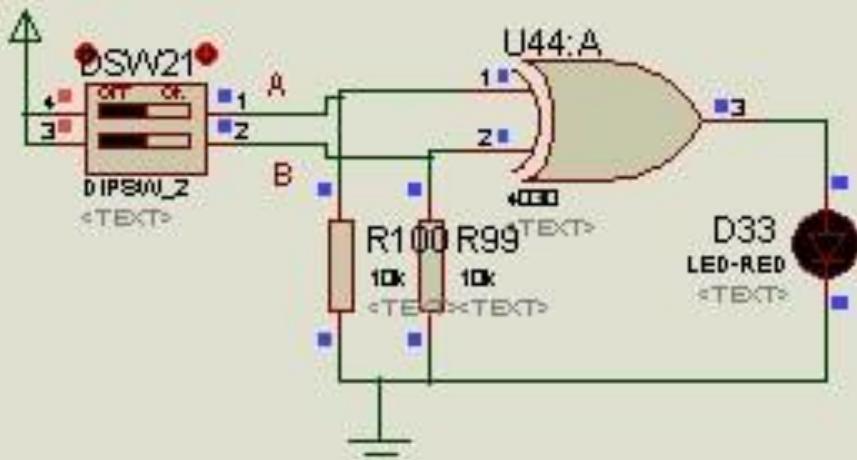


XOR Gate

- If there is an Odd number of HIGH Inputs, then the output is HIGH. Two input X-OR gate function is similar to Two-Way switches in the electrical switchboards. XOR Gate is a two bit Adder. XOR Gates with inputs up to 9 are available for simulation.

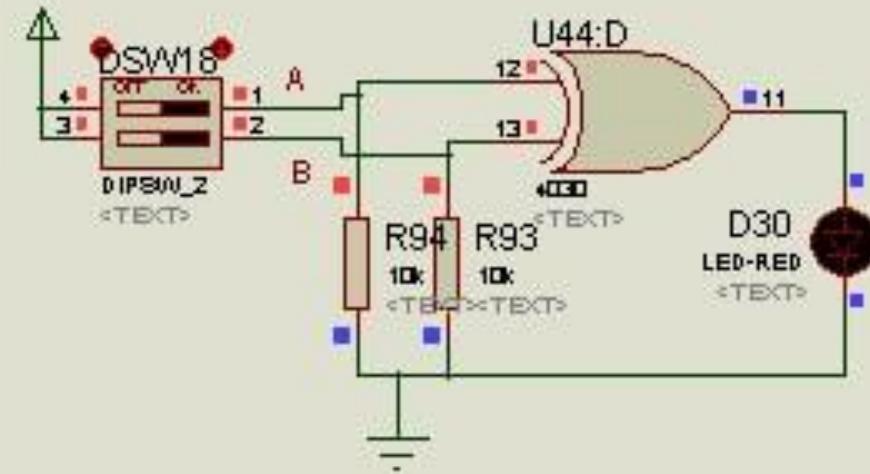
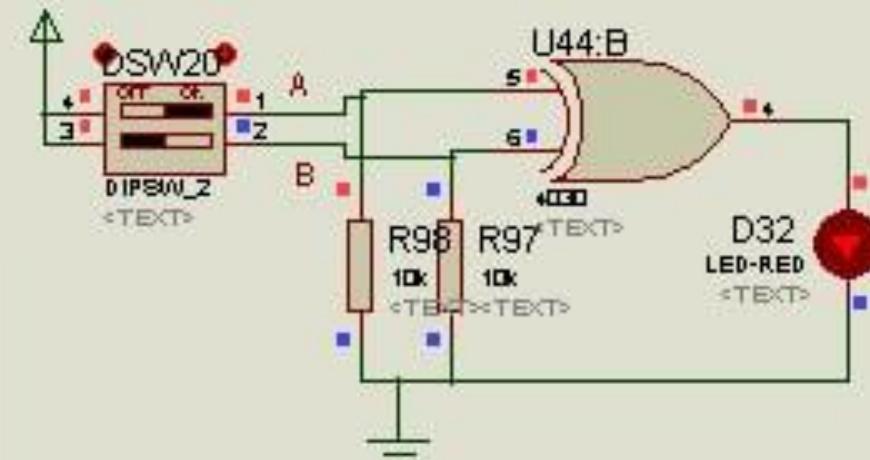
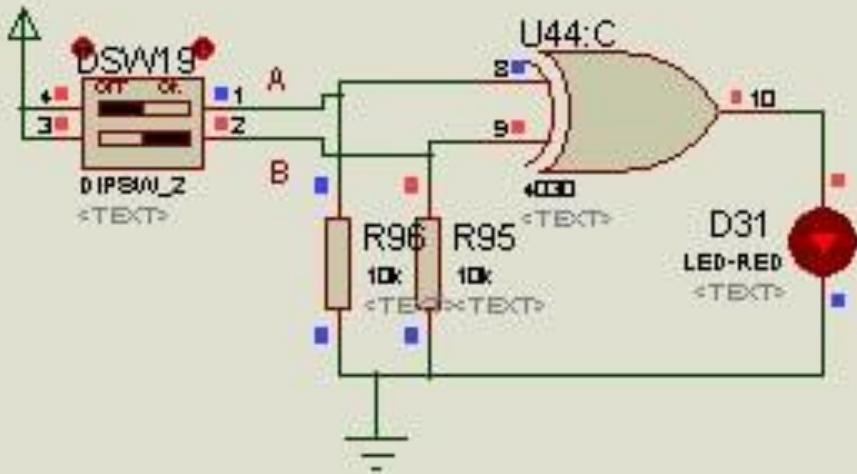


Basic Two Input XOR Gate



Truth Table

A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0





Inverter & Buffer

- The output of this gate is opposite to its input. It is a single input and single output gate.
- The output of this gate is same as that of its input. It is a single input and single output gate. This is generally used to strengthen weak signal in any part of the circuit. Also, this is used to increase the propagation delay.

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Pick Devices

Keywords: **BUFFERS**

Match Whole Words?

Show only parts with models?

Category: **(All Categories)**

Device	Library	Description
4009	CMOS	Hex Inverter With Level Shifted Outputs
4009.DM	CMOS	Hex Inverter With Level Shifted Outputs
4010	CMOS	Hex Non-Inverting Buffer With Level Shifted Outputs
4010.DM	CMOS	Hex Non-Inverting Buffer With Level Shifted Outputs
4041	CMOS	Quadruple True/Complement Buffer
4041.DM	CMOS	Quadruple True/Complement Buffer
4041.IEC	CMOS	Quadruple True/Complement Buffer
4049	CMOS	Buffer Inverting
4049.DM	CMOS	Buffer Inverting
4049.IEC	CMOS	Buffer Inverting
4050	CMOS	Buffer Non-Inverting
4050.DM	CMOS	Buffer Non-Inverting
4050.IEC	CMOS	Buffer Non-Inverting
4054	CMOS	Quad Level Shifters/LCD Drivers With Input Latches
4502	CMOS	Strobed Hex Inverter/Buffer
4502.IEC	CMOS	Strobed Hex Inverter/Buffer
4503	CMOS	Hex Buffer
7406	74STD	Hex inverter buffers / drivers with high-voltage outputs
7406.DM	74STD	Hex inverter buffers / drivers with high-voltage outputs
7406.IEC	74STD	Hex inverter buffers / drivers with high-voltage outputs

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Pick Devices

Keywords: **INVERTER**

Match Whole Words?

Show only parts with models?

Category: **(All Categories)**

Device	Library	Description
4000	CMOS	Dual 3-Input NOR Gate And Inverter
4000.IEC	CMOS	Dual 3-Input NOR Gate And Inverter
4007	CMOS	Dual Complementary Pair And Inverter
4009	CMOS	Hex Inverter With Level Shifted Outputs
4009.DM	CMOS	Hex Inverter With Level Shifted Outputs
4069	CMOS	Hex Inverter (Unbuffered)
4069.IEC	CMOS	Hex Inverter (Unbuffered)
4502	CMOS	Strobed Hex Inverter/Buffer
4502.IEC	CMOS	Strobed Hex Inverter/Buffer
7406	74STD	Hex inverter buffers / drivers with high-voltage outputs
7406.DM	74STD	Hex inverter buffers / drivers with high-voltage outputs
7406.IEC	74STD	Hex inverter buffers / drivers with high-voltage outputs
7416	74STD	Hex inverter buffers / drivers with high-voltage outputs
7416.DM	74STD	Hex inverter buffers / drivers with high-voltage outputs
7416.IEC	74STD	Hex inverter buffers / drivers with high-voltage outputs
74F06	74F	Hex inverter buffers / drivers with high-voltage outputs
74F06.DM	74F	Hex inverter buffers / drivers with high-voltage outputs
74F06.IEC	74F	Hex inverter buffers / drivers with high-voltage outputs
INVERTER	DSIMMDLS	Inverting Buffer Digital Primitive Model
NOT	ACTIVE	Simple Digital Inverter

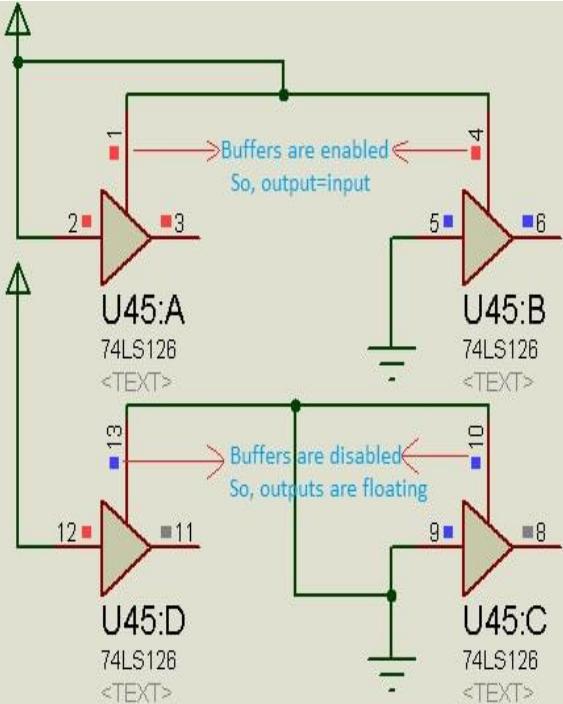
Truth Table of Inverter

A	Y=
0	1
1	0

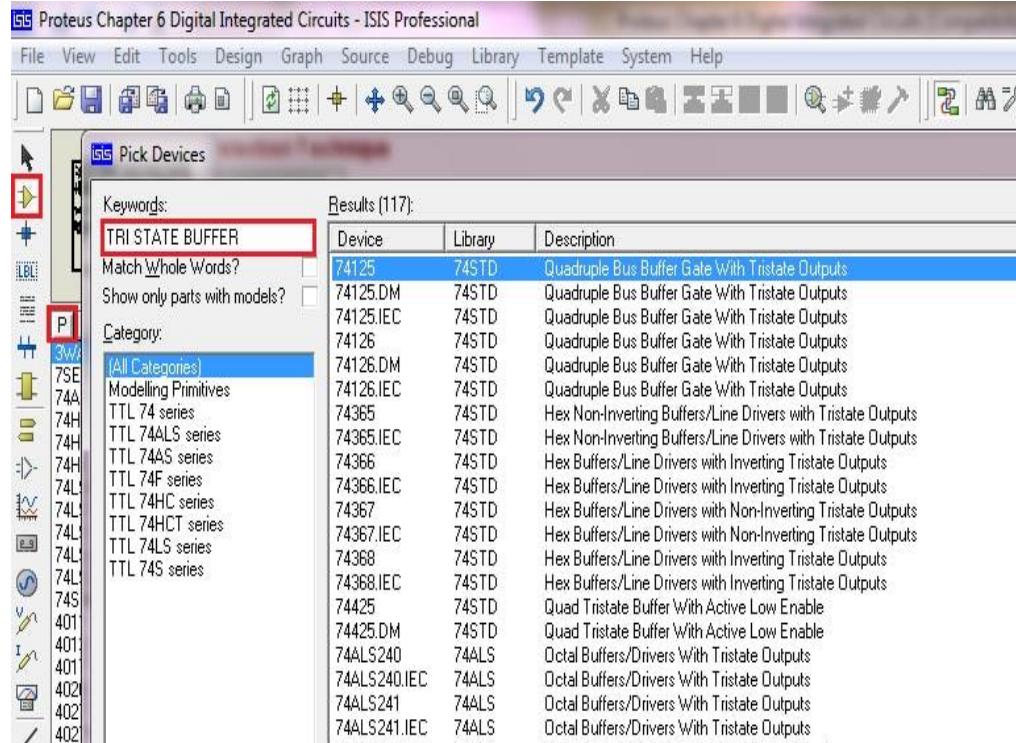


Buffers with Tri-state Output

- The output of this gate is same as that of its input if the buffer is enabled. If the enable input is not active, then the output is in High impedance state or the Tri-state.
- Outputs of two or more buffers can be connected together without the problem of short-circuiting. This property is useful in the input selection. IC packages with 6 Buffers are available.
- Data coming from one of the multiple channels can be selected using these buffers. This method can be employed to reduce the number of communication channels required in the processor, unless data from all the channels is required at a time.



Schematic Design



Tri-State Buffer Search

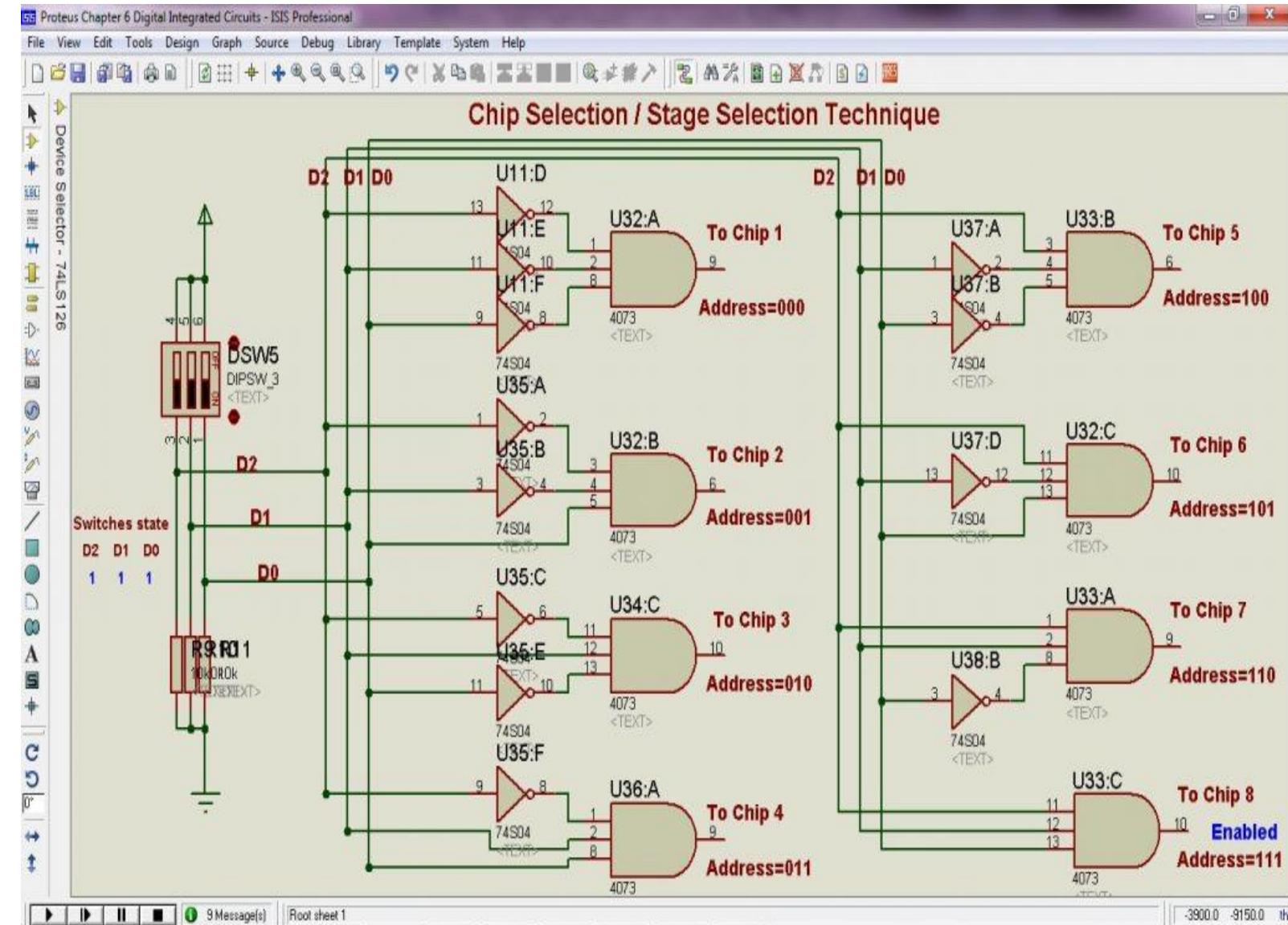


Chip Selection / Stage Selection Technique

- In large Digital circuits or multiple input/output systems, the central processor has to exchange data with its peripherals. The address lines of the processor contain the address of the particular peripheral. In order to enable the chip with a particular address, this chip selection technique is used.
- This is achieved by using AND Gate with a suitable number of inputs as that of the address lines and some Inverters. For instance, let us not mind the source of address and consider three address lines through which addresses are obtained. So, AND Gate with 3 inputs is used. The number of possible addresses with 3-lines is $2^3=8$.
- With these 8 addresses, one of the 8 chips can be chosen. Each chip should be given a dedicated AND Gate, such that o/p of this gate is HIGH only when the address of the chip matches the address generated by address lines. This is typically called as **3 to 8 Decoder**.
- In the case of Binary counters, this technique is used for counter stage identification or selection to reset the counter or to start some other process. The number of chips addressed could be increased by increasing inputs of the AND Gate.



Data Lines	I/Ps to AND Gate
D ₂ D ₁ D ₀	I ₂ I ₁ I ₀
000	2 1 0
001	2 1 D ₀
010	2 D ₁ 0
011	2D ₁ D ₀
100	D ₂ 1 0
101	D ₂ 1 D ₀
110	D ₂ D ₁ 0
111	D ₂ D ₁ D ₀





JK-Flip Flop

- This is a two input Flip Flop whose output changes according to the inputs during the positive or negative edge of the clock signal. Hence, J and K are the synchronous inputs. They affect the output during the clock application.
- The clock for the Flip Flop can be selected i.e. Positive or Negative edge. Both are available. Asynchronous inputs are also included in the IC package, giving an option to Set/Reset the Flip Flop at any instant irrespective of the synchronous inputs and the clock signal. IC's are fabricated with dual, triple, quadruple JK-Flip Flops in a single package with common as well as independent clock and asynchronous inputs.
- **JK Flip Flop operation**
- $J=1, K=1$ is the toggle state of the flip-flop, which leads to Toggle flip-flop i.e. output toggles continuously when positive clock edges are applied.

State Transition of JK-Flip Flop

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	n

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Chip Selection / Device Selection

Pick Devices

Keywords: **jk flip flop**

Match Whole Words?

Show only parts with models?

Category: **(All Categories)**

Device	Library	Description
10135	ECL	Dual JK Master-Slave Flip-Flop
4027	CMOS	Dual JK Flip-Flop
4027.IEC	CMOS	Dual JK Flip-Flop
4095	CMOS	JK Flip-Flop With Triple ANDed JK Inputs
4096	CMOS	JK Flip-Flop With Triple ANDed JK Inputs (One Inverted)
74111	74STD	Dual JK Flip-Flops Master-Slave
74111.IEC	74STD	Dual JK Flip-Flops Master-Slave
74276	74STD	Quad JK Edge-Triggered Flip-Flops With Set And Reset
74276.IEC	74STD	Quad JK Edge-Triggered Flip-Flops With Set And Reset
74376	74STD	4-Bit JK Flip-Flop With Reset
74376.IEC	74STD	4-Bit JK Flip-Flop With Reset
7470	74STD	AND Gated JK Flip-Flop Positive Edge Trigger
7470.IEC	74STD	AND Gated JK Flip-Flop Positive Edge Trigger
7472	74STD	JK Flip-Flop With Triple ANDed J And K Inputs
7472.IEC	74STD	JK Flip-Flop With Triple ANDed J And K Inputs
7476	74STD	Dual JK Flip-Flops With Set And Reset
7476.IEC	74STD	Dual JK Flip-Flops With Set And Reset
74ALS113	74ALS	Dual Negative-Edge-Triggered JK Flip-Flop With Set
74ALS113.IEC	74ALS	Dual Negative-Edge-Triggered JK Flip-Flop With Set
74ALS114	74ALS	Dual Negative-Edge-Triggered JK Flip-Flop With Set Common Clock And Com



D-Flip Flop

- This is a Single input Flip Flop whose output changes according to the input during the positive or negative edge of the clock signal. This is also called as transparent Flip Flop.
- The clock for the Flip Flop can be selected i.e. Positive or Negative edge. Both are available. Asynchronous inputs are also included in the IC package, giving an option to Set/Reset the Flip Flop at any instant irrespective of the synchronous inputs and the clock signal. IC's are fabricated with dual, triple, quadruple, hex, octal D Flip Flops in a Single package with output and input latch enable signal inputs. Hence, these flip-flops are used as latches.
- D Flip Flop is used as a base element in designing Sequential circuits, counters, latches etc. Tri-state output option is also available in some IC's like 74LS373. This allows Shunting of several similar ICs for selective data exchange, like extending PORTS of a microcontroller.

State Transition of D-Flip Flop



D	Q_{n+1}
0	0
1	1

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Pick Devices

Keywords: d flip flop

Match Whole Words?

Show only parts with models?

Category: (All Categories)

Device Library Description

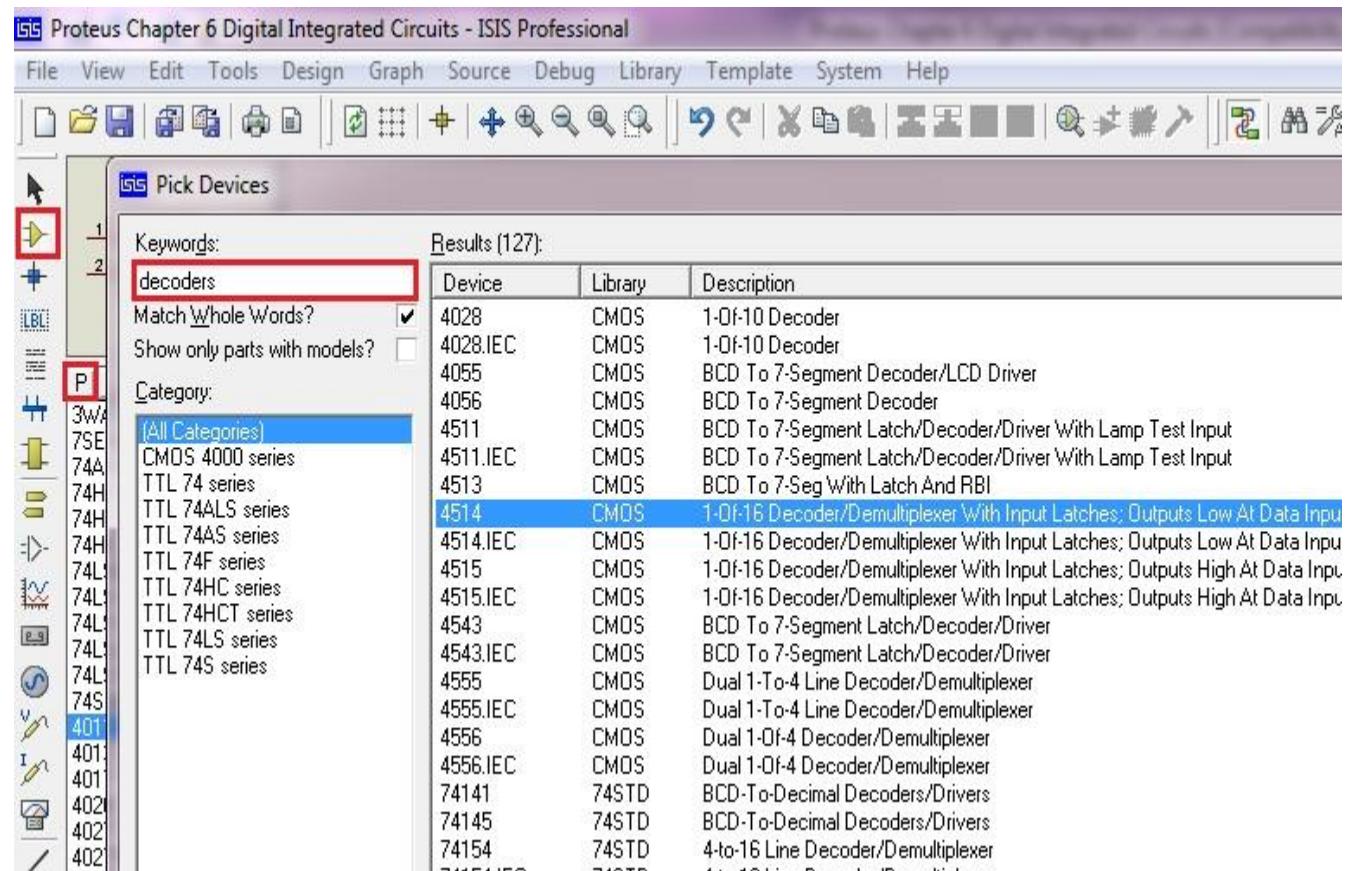
10131	ECL	Dual D-Type Master-Slave Flip-Flop
10176	ECL	Hex D-Type Master-Slave Flip-Flop
10186A	ECL	Hex D-Type Master-Slave Flip-Flop With Reset
4013	CMOS	Dual D-Type Flip-Flop
4013.IEC	CMOS	Dual D-Type Flip-Flop
40174	CMOS	Hex D-Type Flip-Flop With Reset; Positive-Edge Trigger
40174.IEC	CMOS	Hex D-Type Flip-Flop With Reset; Positive-Edge Trigger
40175	CMOS	Quad D-Type Flip-Flop With Reset; Positive-Edge Trigger
40175.IEC	CMOS	Quad D-Type Flip-Flop With Reset; Positive-Edge Trigger
74F377	74F	Octal D-Type Flip-Flop With Clock Enable
74F377.IEC	74F	Octal D-Type Flip-Flop With Clock Enable
74HC377	74HC	Octal D-Type Flip-Flop With Clock Enable
74HC377.IEC	74HC	Octal D-Type Flip-Flop With Clock Enable
74HCT377	74HCT	Octal D-Type Flip-Flop With Clock Enable
74HCT377.IEC	74HCT	Octal D-Type Flip-Flop With Clock Enable
74LS377	74LS	Octal D-Type Flip-Flop With Clock Enable
74LS377.IEC	74LS	Octal D-Type Flip-Flop With Clock Enable
74LS379	74LS	6-Bit D-Type Flip-Flop With Clock Enable And Complementary Outputs
DTFF	ACTIVE	Animated D-Type Flip-Flop model
DTFF	DSIMMDLS	Universal D-Type Flip-Flop Digital Primitive Model With D/Clock/Set/Reset Inp

Decoders



- Decoders are multi-input and multi-output combinational circuits. In case of address decoders only one of the outputs will be High at any instant. In the case of display decoders like the BCD to Seven segment decoders, the output will be according to the input data to lighten the desired segments of the display. Decoders with multiple enable inputs are called as De-Multiplexers.
- As in case of chip selection application, 4-Bit address is generated by a processor to the decoder. The decoder activates one of the outputs corresponding to the address at its inputs.

Pin	Description	Logic
INH	Output Disable	High
STB	Output Latch Enable	High



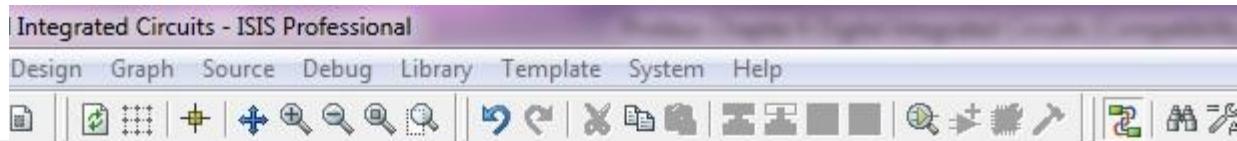


BCD to Seven segment decoder

- BCD to Seven segment decoder is used to display BCD Values in decimal form. As in the binary counter example discussed above under JK-Flip Flop, the output is in binary form. By using this decoder, the count value can be displayed in decimal form.
- There are decoders for common cathode as well as common anode displays. Fonts are also different from one IC to other.



PIN	Description	Logic
LT	Lamp Test, to test the segments	Active Low
RBI=Ripple Banking Output	To avoid showing leading zeroes	Active low
RBO=Ripple Banking Input	Turns off the digit, used in brightness controlling by PWM	Active Low



Pick Devices

Keywords: **bcd decoders**

Match Whole Words?

Show only parts with models?

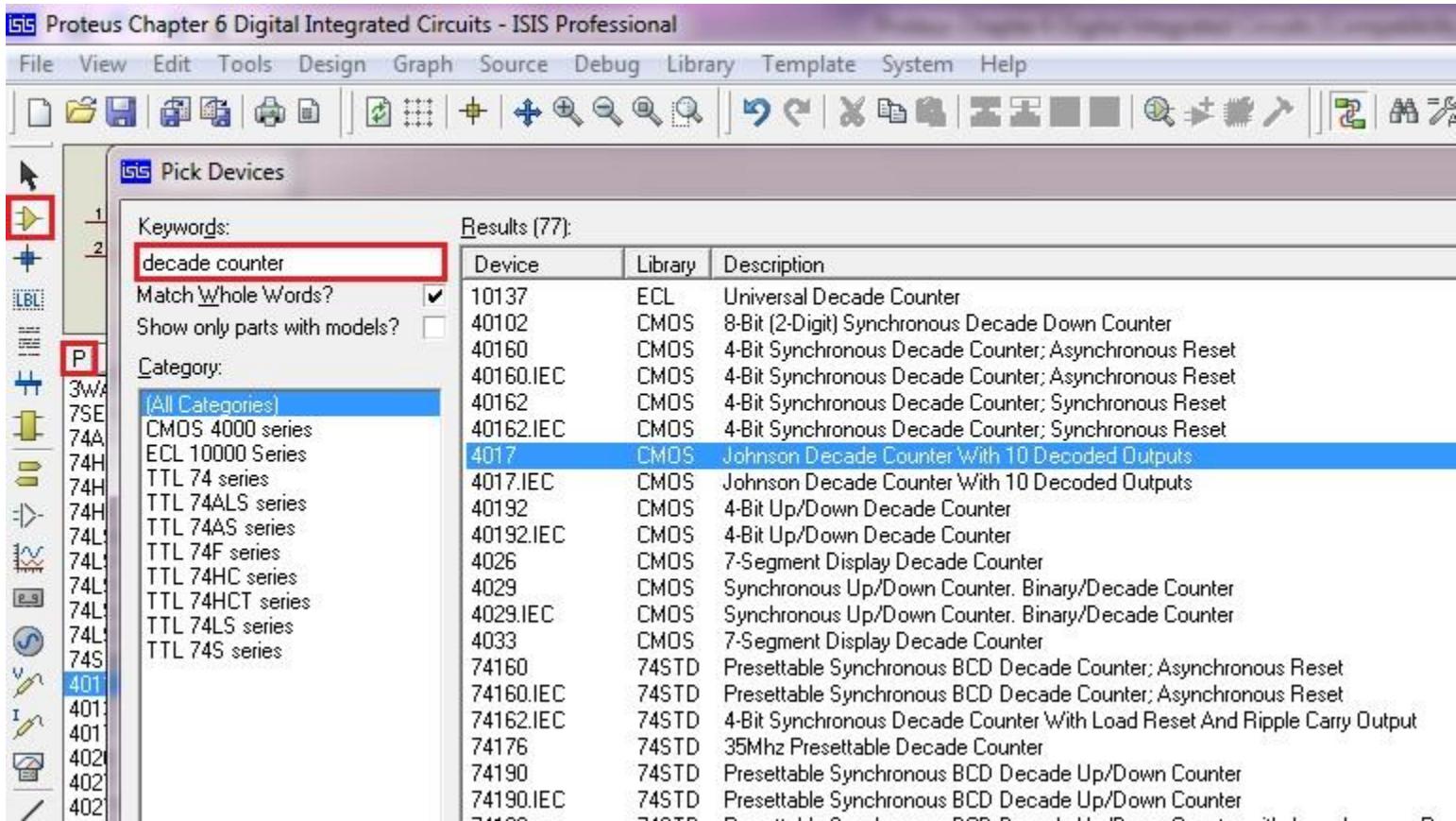
Category: **(All Categories)**

Device	Library	Description
4055	CMOS	BCD To 7-Segment Decoder/LCD Driver
4056	CMOS	BCD To 7-Segment Decoder
4511	CMOS	BCD To 7-Segment Latch/Decoder/Driver With Lamp Test Input
4511.IEC	CMOS	BCD To 7-Segment Latch/Decoder/Driver With Lamp Test Input
4513	CMOS	BCD To 7-Seg With Latch And RBI
4543	CMOS	BCD To 7-Segment Latch/Decoder/Driver
4543.IEC	CMOS	BCD To 7-Segment Latch/Decoder/Driver
74141	74STD	BCD-To-Decimal Decoders/Drivers
74145	74STD	BCD-To-Decimal Decoders/Drivers
74184	74STD	BCD To Binary Converter
74185	74STD	Binary To BCD Converter
74247	74STD	BCD-To-Seven-Segment Decoders/Drivers
74248	74STD	BCD To 7-Segment Decoder/Common-Cathode Led Driver With RBI
74248	USERDVC	BCD To 7-Segment Decoder/Common-Cathode Led Driver With RBI
74249	74STD	BCD To 7-Segment Open-Collector Decoder Driver
7442	74STD	1-of-10 BCD to Decimal Decoder
7442.IEC	74STD	1-of-10 BCD to Decimal Decoder
7445	74STD	BCD-To-Decimal Decoders/Drivers
7445.IEC	74STD	BCD-To-Decimal Decoders/Drivers
7446	74STD	Open-Collector BCD To 7-Segment Decoder/Common-Anode Led Driver With

Decade counter



- This is also one kind of decoder, which counts the input clock pulses and one of the ten outputs is made high corresponding to the counted incoming pulses.

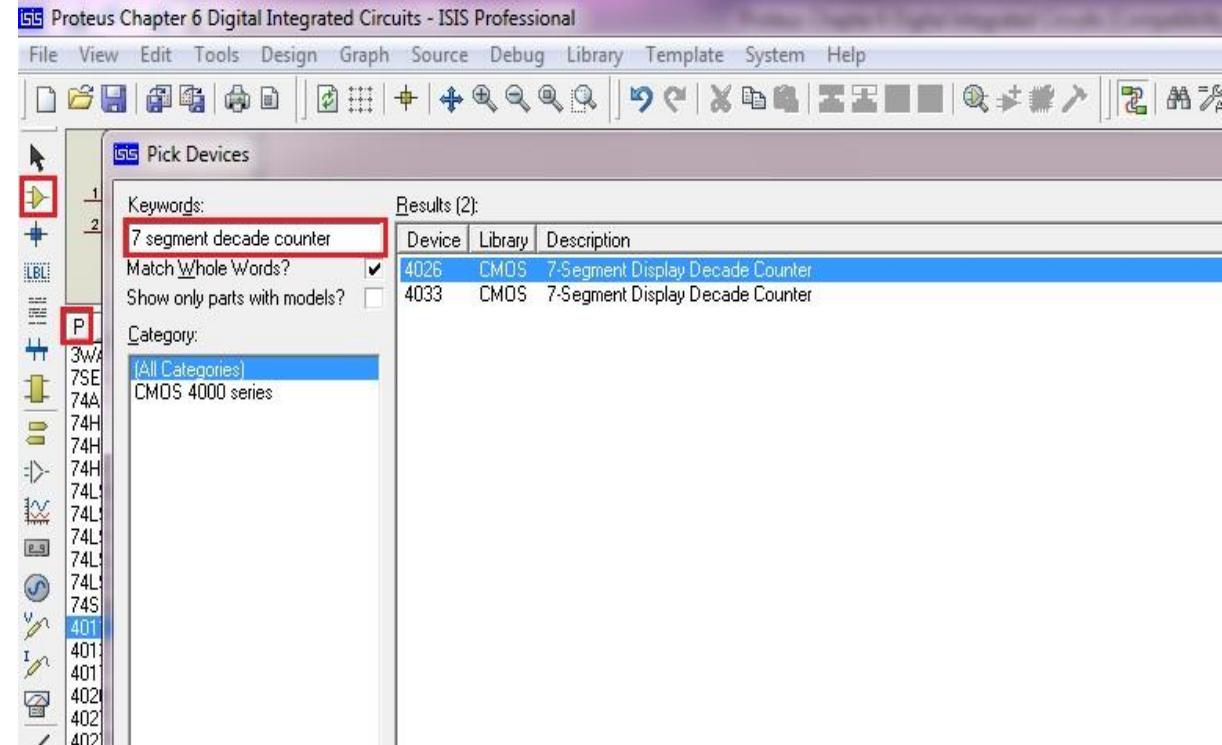


PI N	Description	Logic
CL K	Clock input	Positive edge
E	Clock enable input	Active low
C O	Carry Out, used as clock for succeeding counters, divided by 10 counter	Toggles after Q4 and Q9
M R	Master Reset to reset the counter	Active High

Pulse counter with seven segment output



- This counter is a combination of binary counter, binary to BCD Converter, BCD to seven segment decoder. It has carry out and Un-gated C-segment outputs, which are used in Divided by 10 and Divided by 12 counters. These outputs are available even if display is disabled in power saving mode.





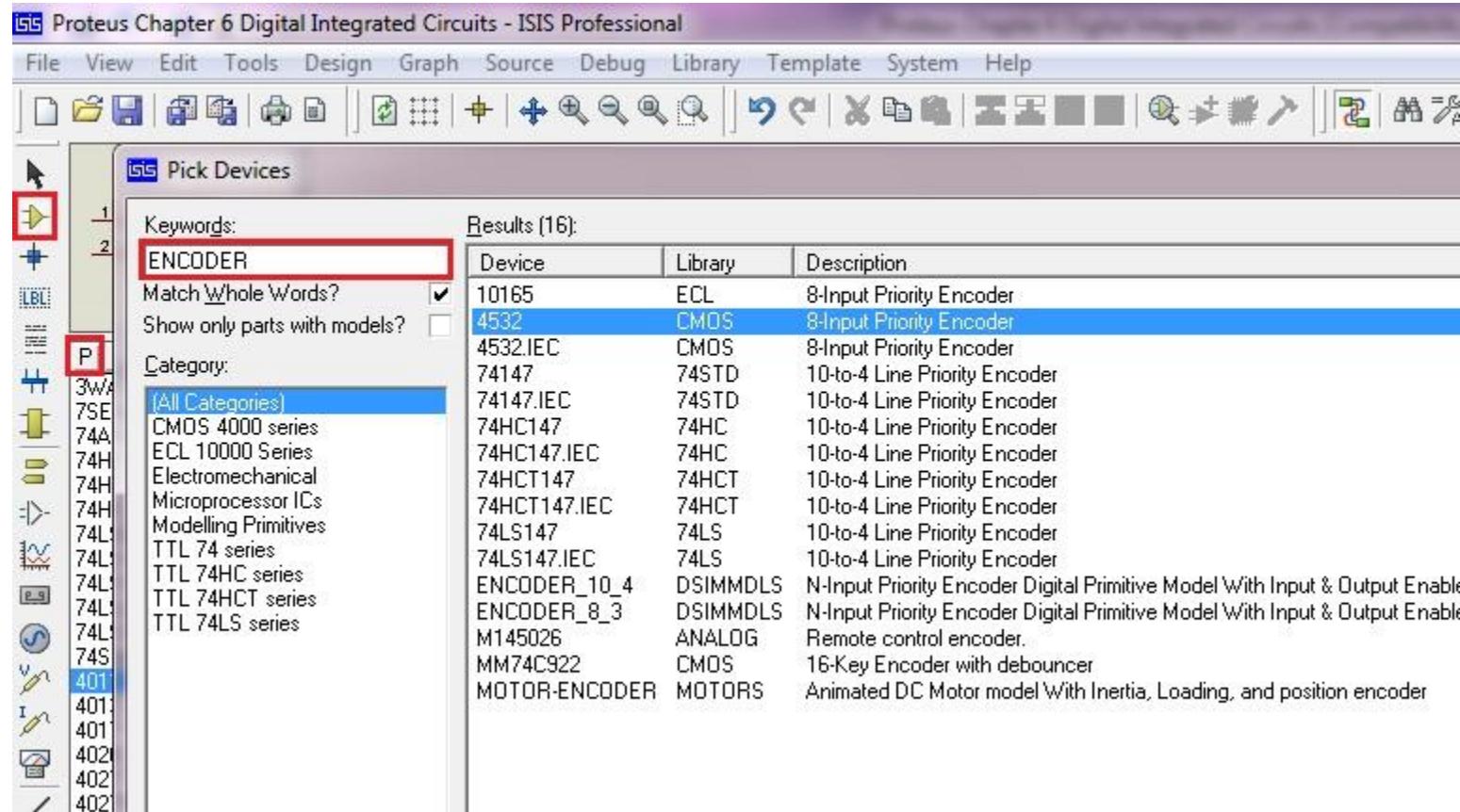
PIN	Description	Logic
CLK	Clock input	Positive edge
DEI	Display enable input	Active High
INH	Inhibit input	High to stop counting
CO	Carry Out, used as clock for succeeding counters, divided by 10 counter	Become low for one clock period after every 10 cycles
MR	Master Reset to reset the counter	Active High
UCS	Un-gated C Segment output. Used for divided by 12 counters.	Same as C segment of the display, independent of DEI.
DEO	Display Enable Output	Same as DEI



Priority Encoder

- It is a multiple input multiple output IC, operates in reverse mode of 4 to 16 decoder. The output of the encoder is the binary value of the numerically highest active input. Hence, it is called as priority encoder. Consider a 16 to 4 Encoder with active high inputs. It has 16 inputs from D0 to D15 and 4-bit binary output. Under enabled state,
- If D0=High, and all other inputs are low, then binary output = 0000.
- If D15=High, irrespective of all other inputs, then binary output = 1111.
- GS=Group Signal pin avoids the ambiguity of no active input state and D0 active state.
- GS=High if at least one of the inputs is active. So, if output is binary 000 and GS=High, then it indicates that D0 is the active input. If output is binary 000 and GS=Low, then it indicates that no input is active. EO pin is used in cascading encoders for extending the overall encoder range.

PI N	Description	Logic
EI	Enable input	Active High
EO	Enable Output, used for cascading encoders	High only when all inputs are inactive
GS	Group Signal	High if at least one of the inputs is active, with EI=High.





THANK YOU

Reference

<http://www.circuiststoday.com/digital-integrated-circuits-proteus>

