江西理工大学
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Digital System Design

Clip Lecture series

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Sequential Circuits

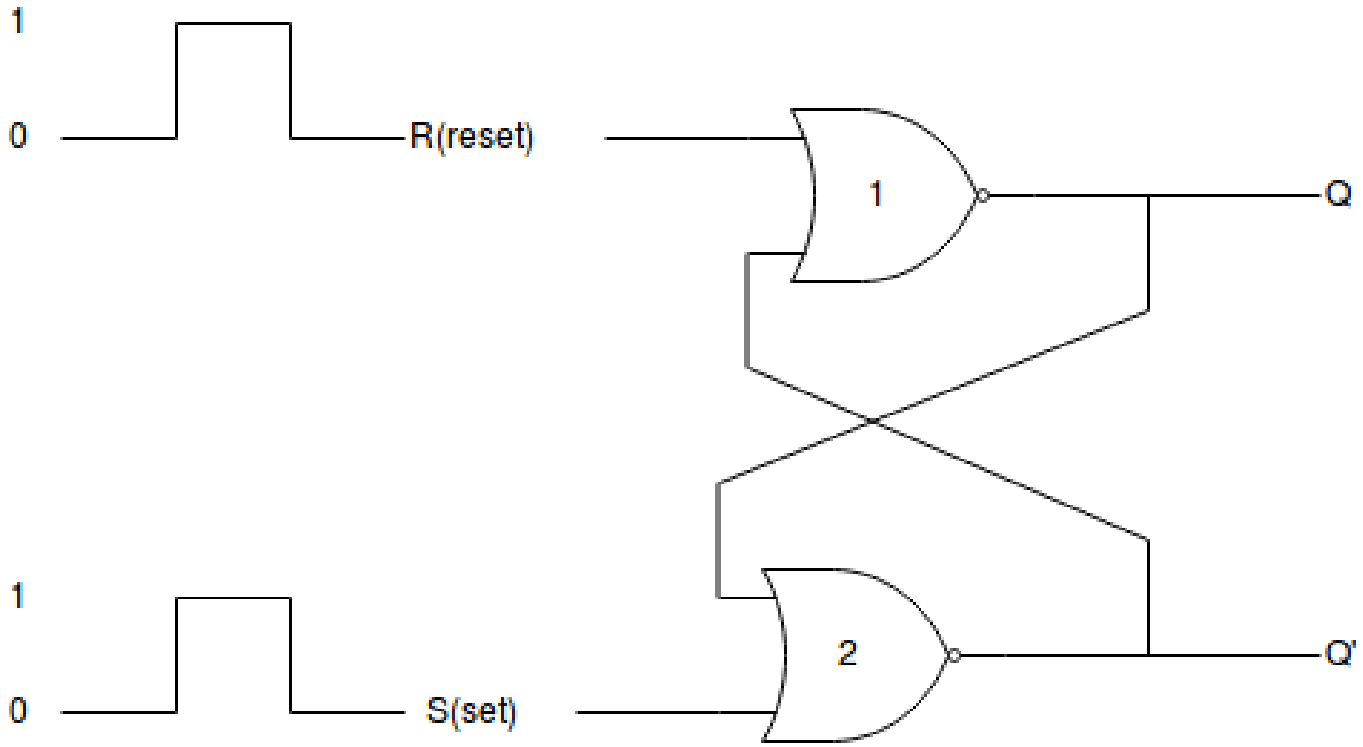
Flip-flop/Basic Flip-Flop

S-R Flip-flop/Basic Flip-Flop

Flip flops are an application of logic gates. A flip-flop circuit can remain in a binary state indefinitely (as long as power is delivered to the circuit) until directed by an input signal to switch states

- S-R flip-flop stands for SET-RESET flip-flops.
- The SET-RESET flip-flop consists of two NOR gates and also two NAND gates.
- These flip-flops are also called S-R Latch.
- The design of these flip flops also includes two inputs, called the SET [S] and RESET [R]. There are also two outputs, Q and Q'.

S-R Flip-flop/Basic Flip-Flop



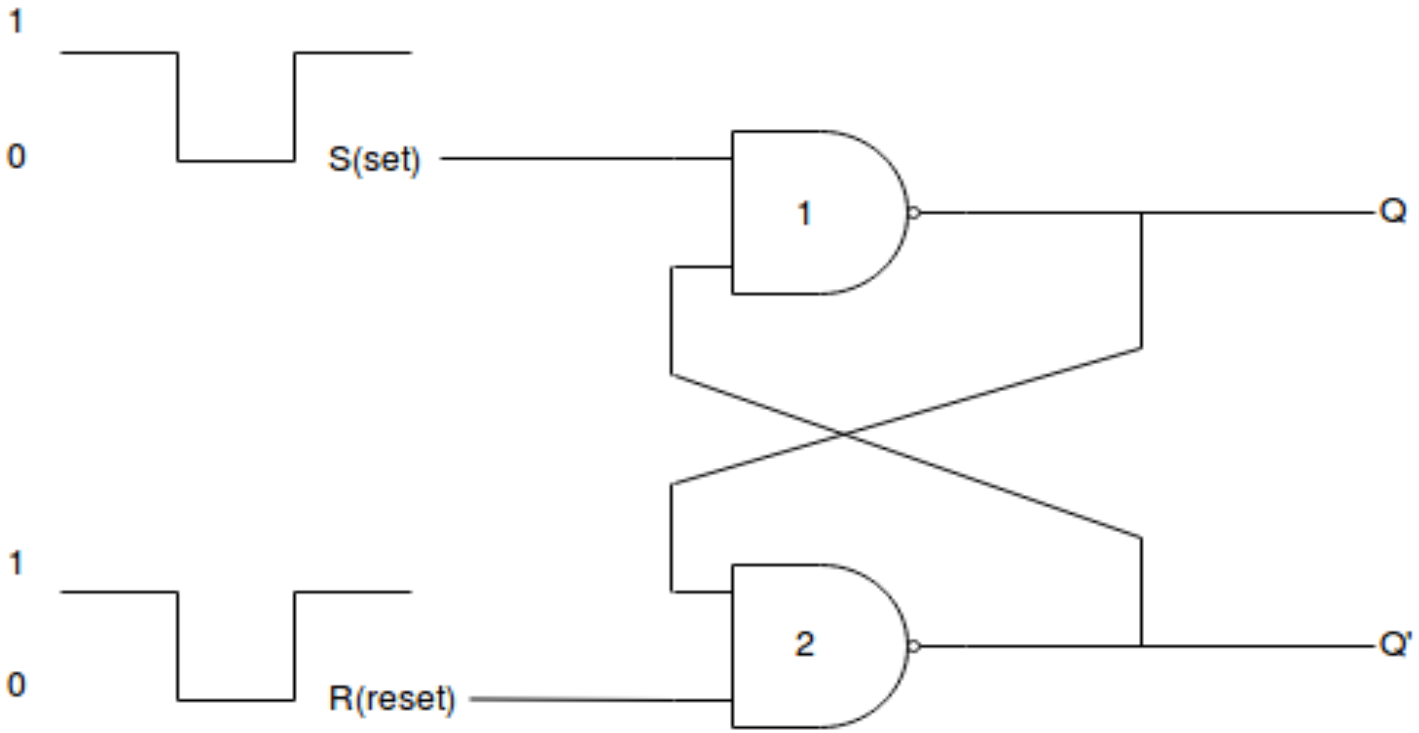
a) Logic diagram

S	R	Q	Q'
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0

b) Truth table

fig: Basic flip-flop circuit with NOR gates

S-R Flip-flop/Basic Flip-Flop



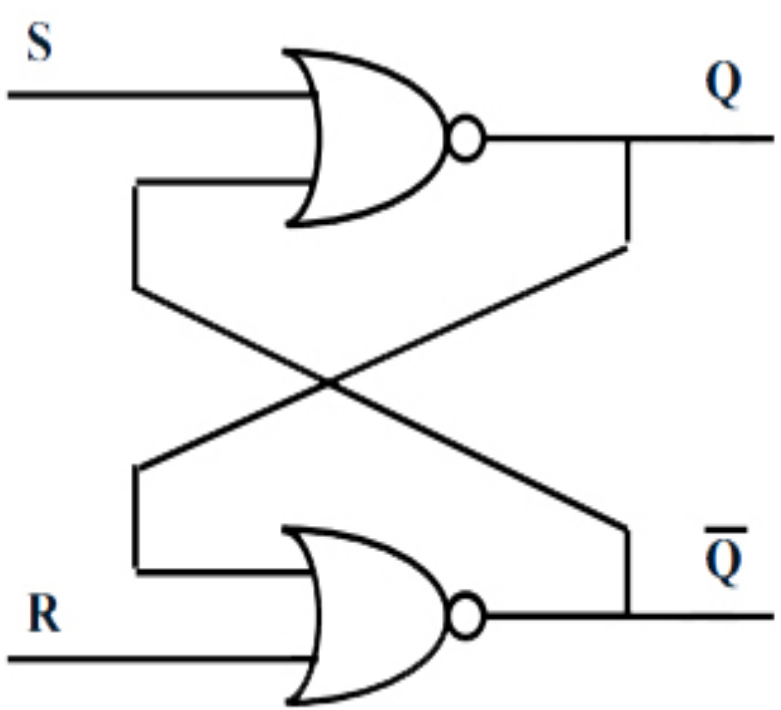
a) Logic diagram

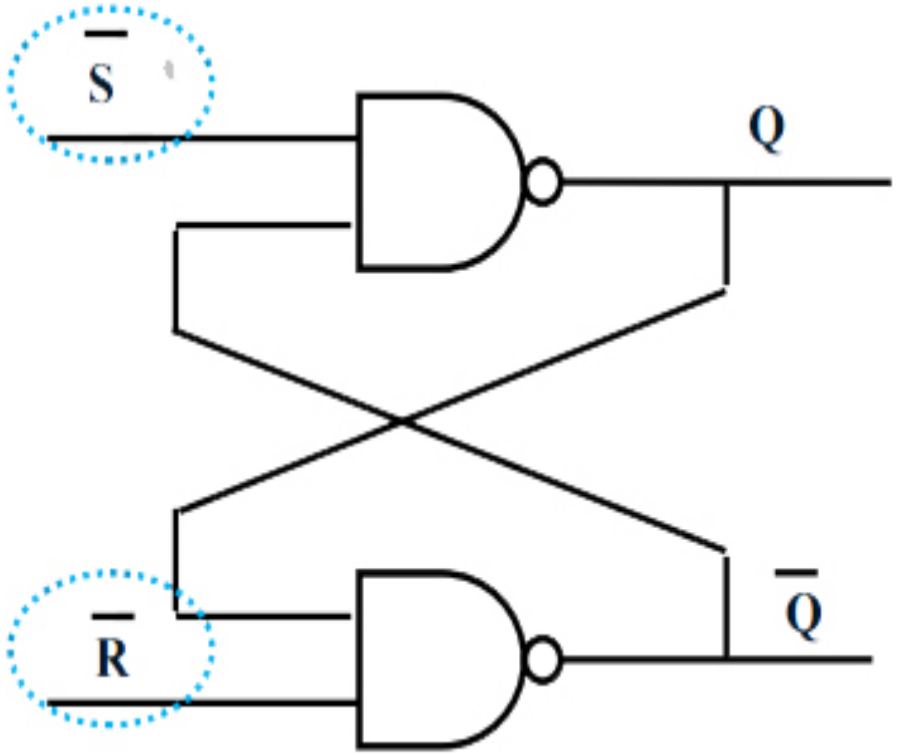
S	R	Q	Q'
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	1	1

b) Truth table

fig: Basic flip-flop circuit with NAND gates

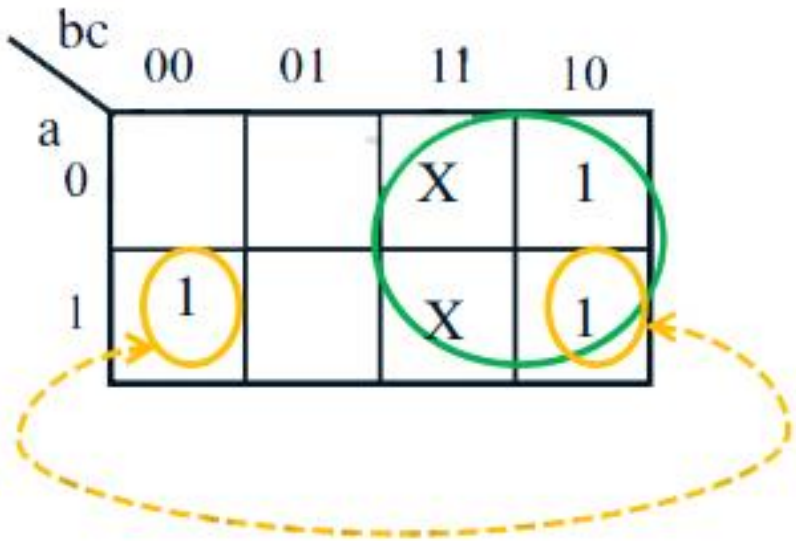
SR Latch





SR Latch

Current		Next	
S	R	Q	Q*	
0	0	0	0	HOLD
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	0	Invalid
1	1	1	0	



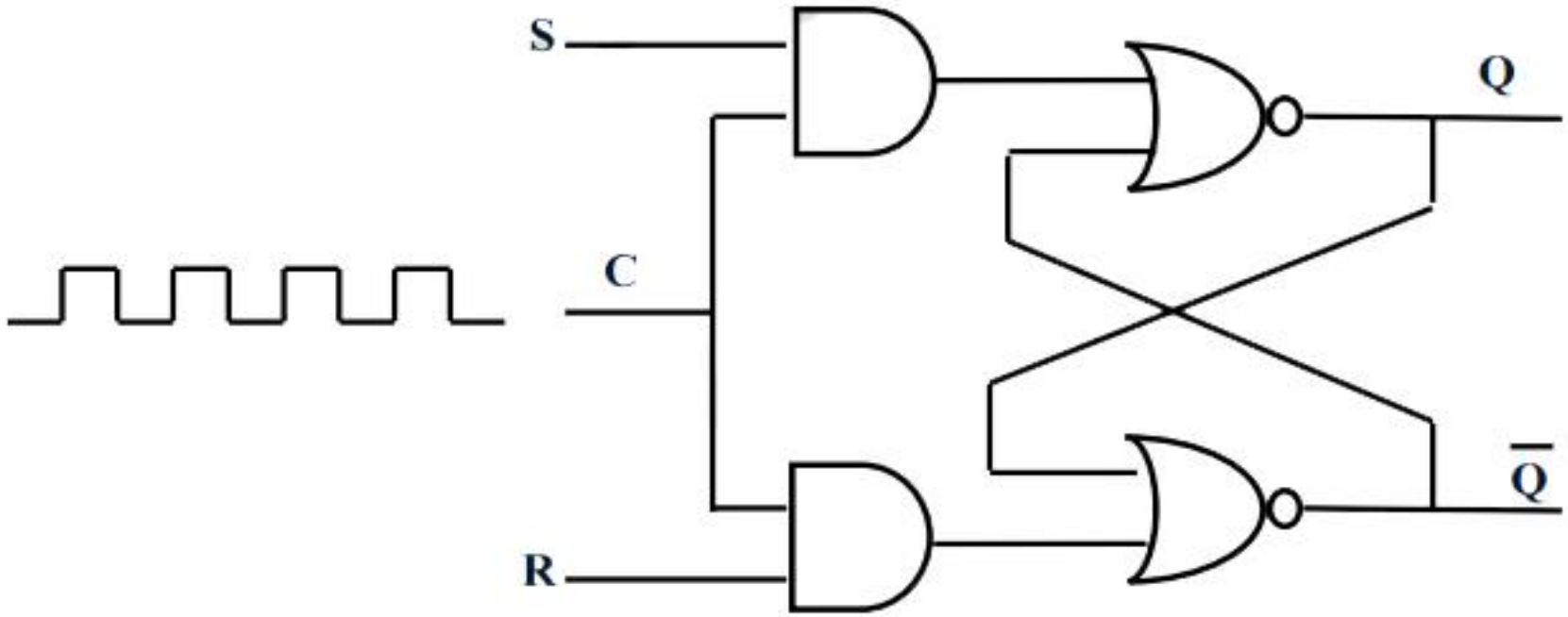
S	R	Q*
0	0	Q
0	1	0
1	0	1
1	1	X

$$Q^* = S + \overline{R}.Q$$

$$S.R = 0$$

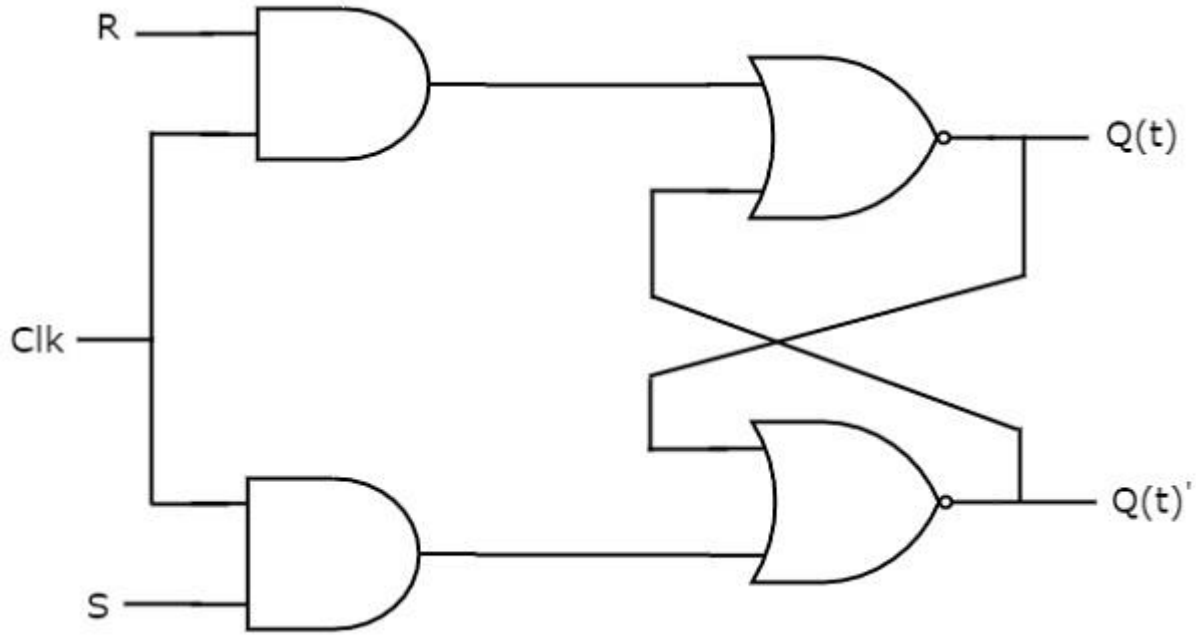
Flip Flop

- If we add the **clk** to the input latch control its become FF
- Please not FF are sensitive to clock edge and latch are sensitive to level



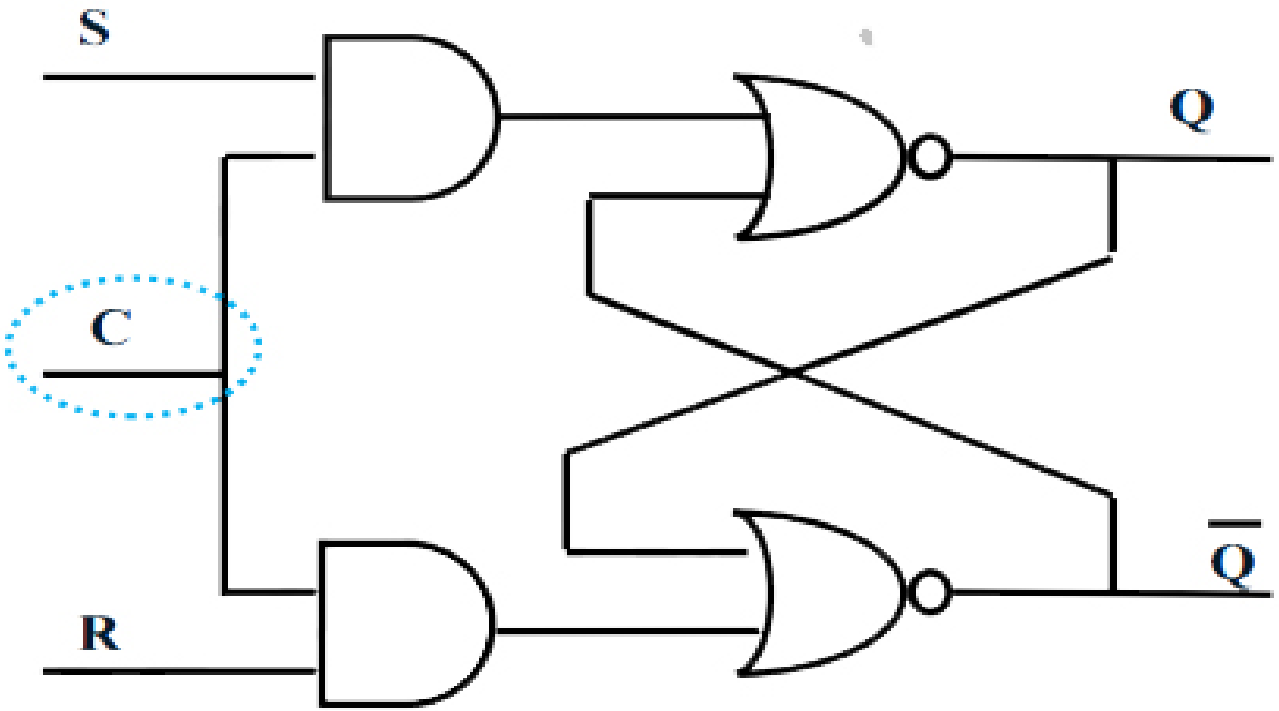
SR Flip-Flop

- SR flip-flop operates with only positive clock transitions or negative clock transitions. Whereas, SR latch operates with enable signal.
- The **circuit diagram** of SR flip-flop is shown in the following figure.



This circuit has two inputs S & R and two outputs Q(t) & Q(t)'. The operation of SR flipflop is similar to SR Latch. But, this flip-flop affects the outputs only when positive transition of the clock signal is applied instead of active enable.

SR Latch with control input



SR Flip-Flop

- The following table shows the **state table** of SR flip-flop.

S	R	Q(t + 1)
0	0	Q(t)
0	1	0
1	0	1
1	1	-

SR Flip-Flop

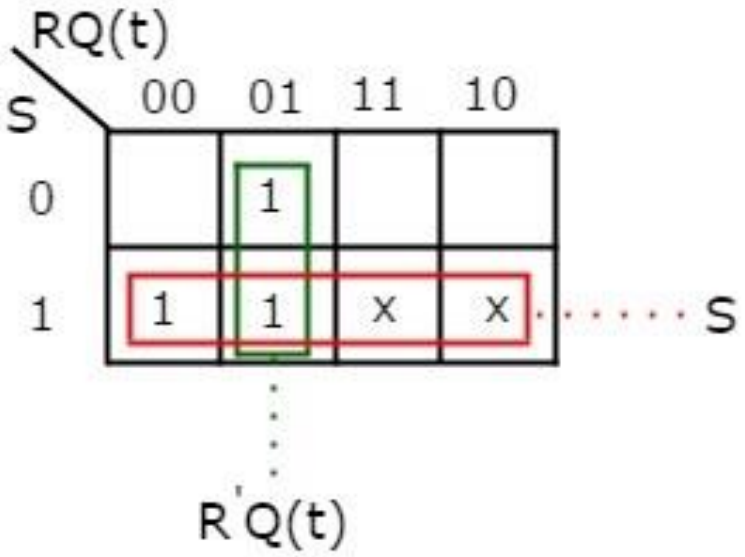
- Here, Q(t) & Q(t + 1) are present state & next state respectively. So, SR flip-flop can be used for one of these three functions such as Hold, Reset & Set based on the input conditions, when positive transition of clock signal is applied. The following table shows the **characteristic table** of SR flip-flop.

Present Inputs		Present State	Next State
S	**R**	**Q(t)**	**Q(t + 1)**
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

SR Flip-Flop

Present Inputs		Present State	Next State
S	**R**	**Q(t)**	**Q(t + 1)**
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

By using three variable K-Map, we can get the simplified expression for next state, Q(t + 1). The **three variable K-Map** for next state, Q(t + 1) is shown in the following figure.



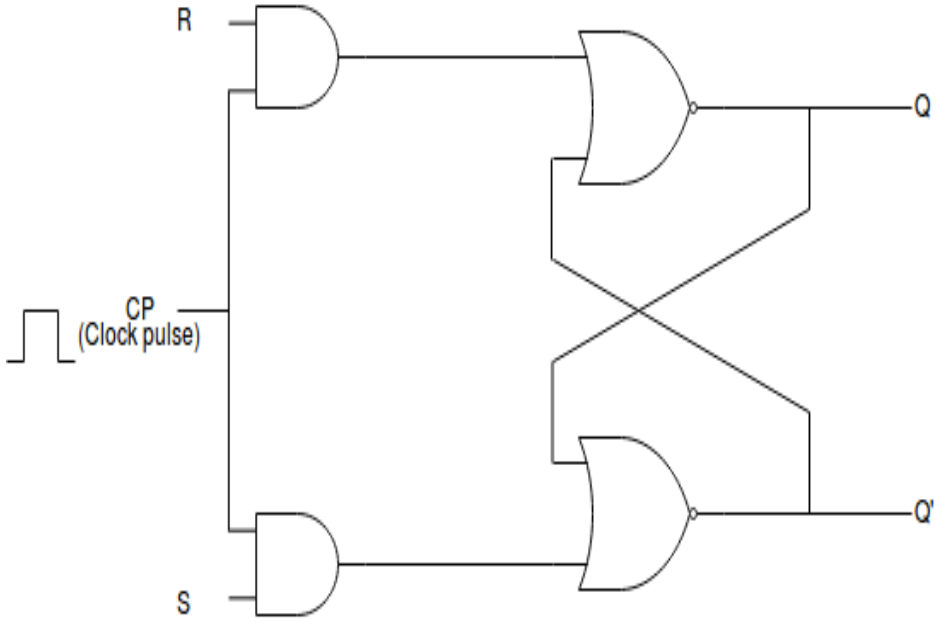
The maximum possible groupings of adjacent ones are already shown in the figure. Therefore, the **simplified expression** for next state Q(t + 1) is

$$Q(t+1)=S+R'Q(t)$$

Clocked S-R Flip-Flop

- The operation of a basic flip-flop can be modified by providing an additional control input that determines when the state of the circuit is to be changed.

The limitation with a S-R flip-flop using NOR and NAND gate is the invalid state. This problem can be overcome by using a stable SR flip-flop that can change outputs when certain invalid states are met, regardless of the condition of either the Set or the Reset inputs.



a) Logic diagram

fig: Clocked SR flip flop

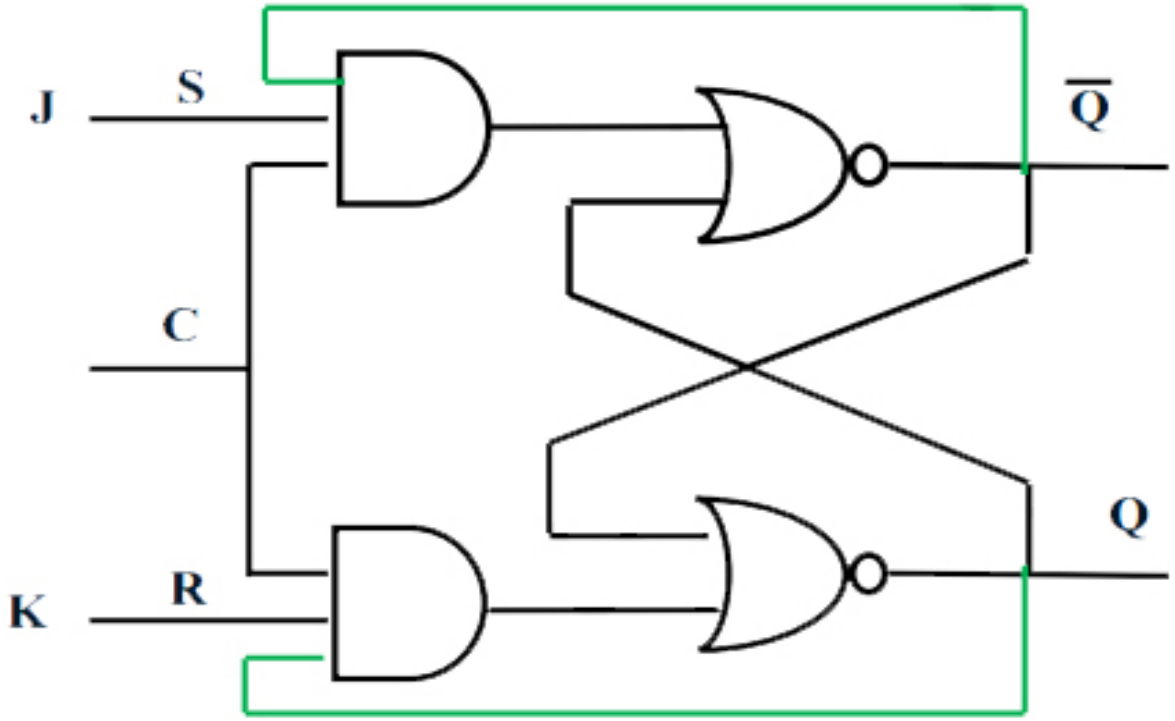
Q	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Intermediate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Intermediate

b) Truth table

- A clock pulse is given to the inputs of the AND Gate. If the value of the clock pulse is '0', the outputs of both the AND Gates remain '0‘.

JK Flip-Flop

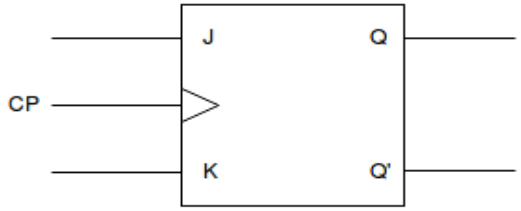
- If the SR Flip Flop have the Q feedback to the gate which have the R input and from Q to the S input we can have the JK FF.



J	K	Q*	
0	0	Q	HOLD
0	1	0	RESET
1	0	1	SET
1	1	$\overline{Q}$	Complement

$$Q^* = J.\overline{Q} + \overline{K}.Q$$

JK Flip-Flop

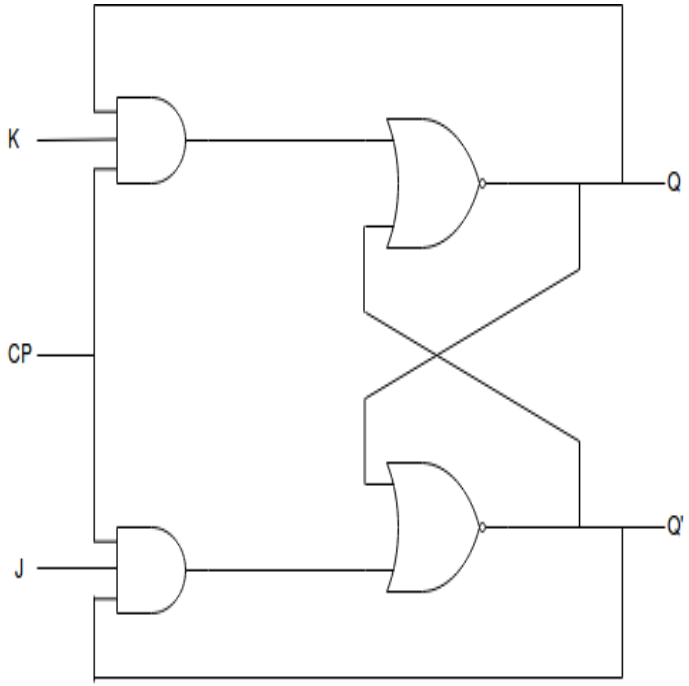


c) Graphical symbol

fig. Clocked JK flip flop

- J-K flip-flop can be considered as a modification of the S-R flip-flop.
- The main difference is that the intermediate state is more refined and precise than that of an S-R flip-flop.

The characteristics of inputs 'J' and 'K' is same as the 'S' and 'R' inputs of the S-R flip-flop.
J stands for SET, and 'K' stands for CLEAR.
When both the inputs J and K have a HIGH state, the flip-flop switches to the complement state, so, for a value of Q = 1, it switches to Q=0, and for a value of Q = 0, it switches to Q=1.



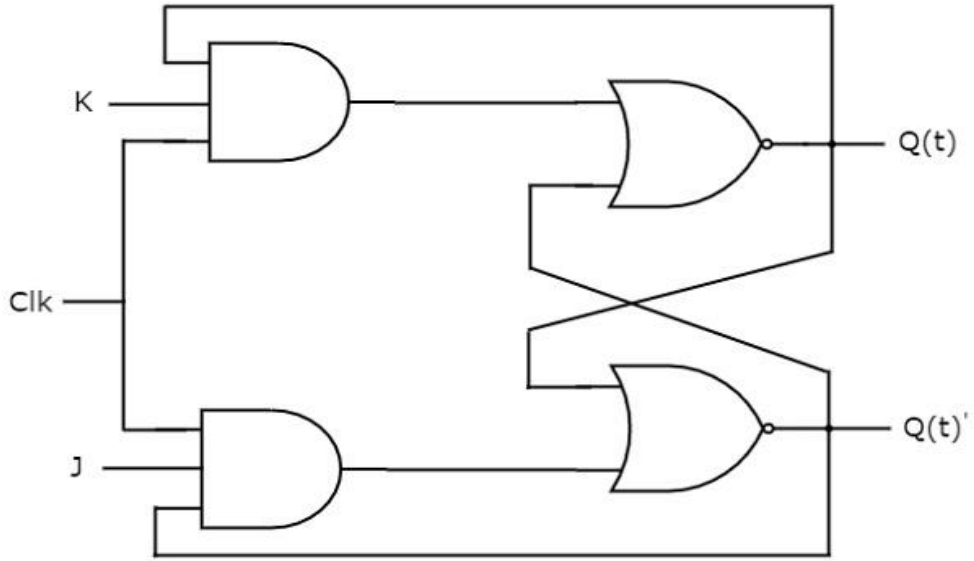
a) Logic diagram

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

b) Transition table

JK Flip-Flop

- JK flip-flop is the modified version of SR flip-flop. It operates with only positive clock transitions or negative clock transitions.
- The **circuit diagram** of JK flip-flop is shown in the following figure.



This circuit has two inputs J & K and two outputs Q(t) & Q(t)'.
The operation of JK flip-flop is similar to SR flip-flop.
Here, we considered the inputs of SR flip-flop as **S = J Q(t)'** and **R = KQ(t)** in order to utilize the modified SR flip-flop for 4 combinations of inputs.

JK Flip-Flop

- The following table shows the **state table** of JK flip-flop.

J	K	Q(t + 1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q(t)'

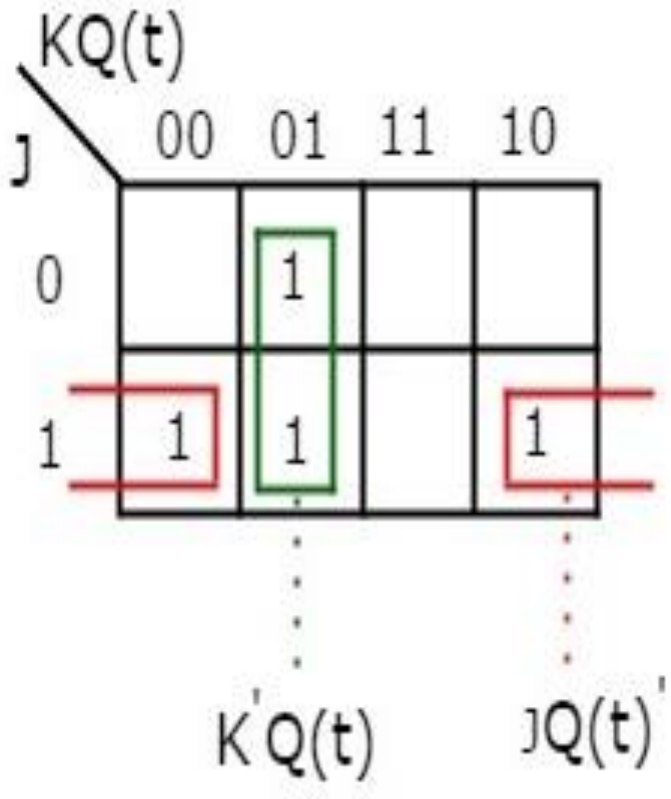
JK Flip-Flop

- Here, Q(t) & Q(t + 1) are present state & next state respectively. So, JK flip-flop can be used for one of these four functions such as Hold, Reset, Set & Complement of present state based on the input conditions, when positive transition of clock signal is applied.
- The following table shows the **characteristic table** of JK flip-flop.

Present Inputs		Present State	Next State
J	**K**	**Q(t)**	**Q(t+1)**
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

JK Flip-Flop

- By using three variable K-Map, we can get the simplified expression for next state, Q(t + 1).
- **Three variable K-Map** for next state, Q(t + 1) is shown in the following figure.

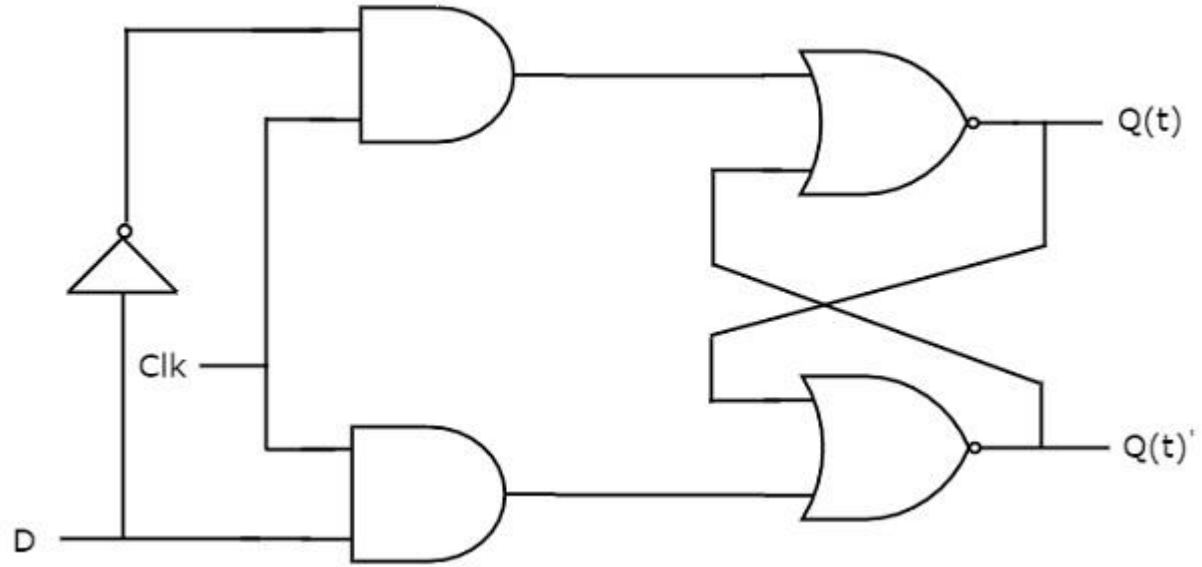


The maximum possible groupings of adjacent ones are already shown in the figure. Therefore, the **simplified expression** for next state Q(t+1) is

$$Q(t+1)=JQ(t)'+K'Q(t)$$

D Flip-Flop

- D flip-flop operates with only positive clock transitions or negative clock transitions. Whereas, D latch operates with enable signal.
- That means, the output of D flip-flop is insensitive to the changes in the input, D except for active transition of the clock signal.
- The **circuit diagram** of D flip-flop is shown in the following figure.



D Flip-Flop

- This circuit has single input D and two outputs Q(t) & Q(t)'.
- The operation of D flip-flop is similar to D Latch. But, this flip-flop affects the outputs only when positive transition of the clock signal is applied instead of active enable.
- The following table shows the **state table** of D flip-flop.

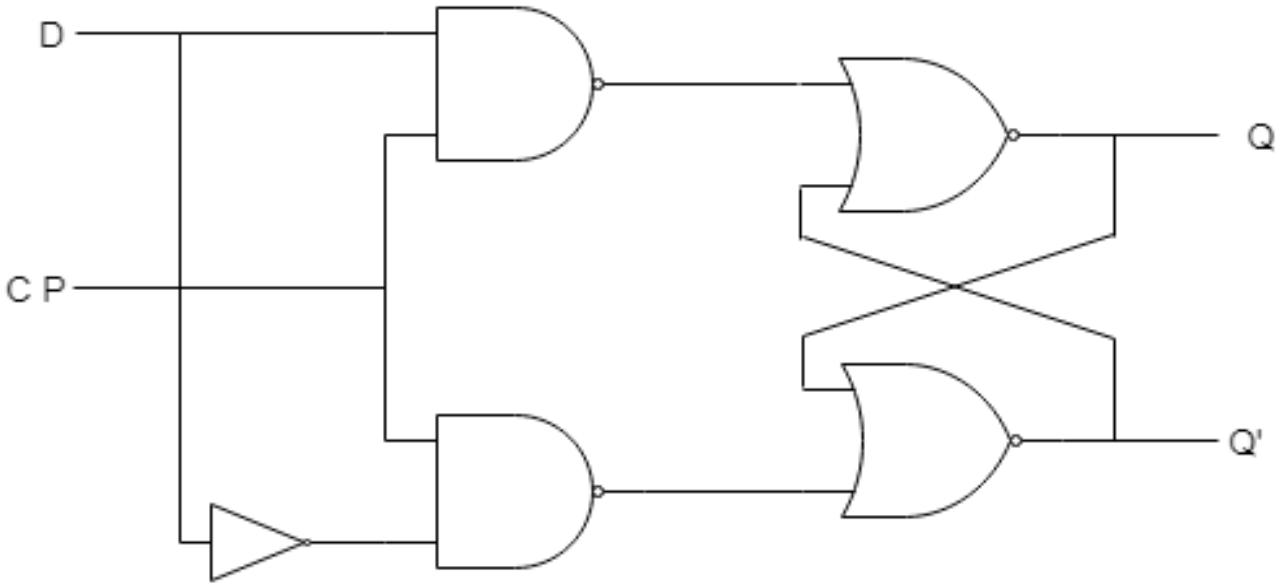
D	Q(t + 1)
0	0
0	1

Therefore, D flip-flop always Hold the information, which is available on data input, D of earlier positive transition of clock signal. From the above state table, we can directly write the next state equation as

$$Q(t + 1) = D$$

Next state of D flip-flop is always equal to data input, D for every positive transition of the clock signal. Hence, D flip-flops can be used in registers, **shift registers** and some of the counters.

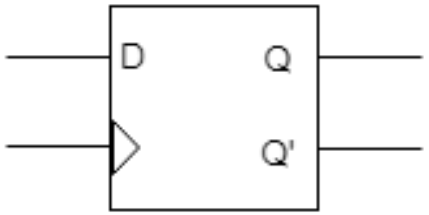
The D flip-flop



(a) Logic diagram with Nand gates

Q	D	Q (t + 1)
0	0	0
0	1	1
1	0	0
1	1	1

(c) Transition table



(b) Graphic Symbol

fig. Clocked D flip flop

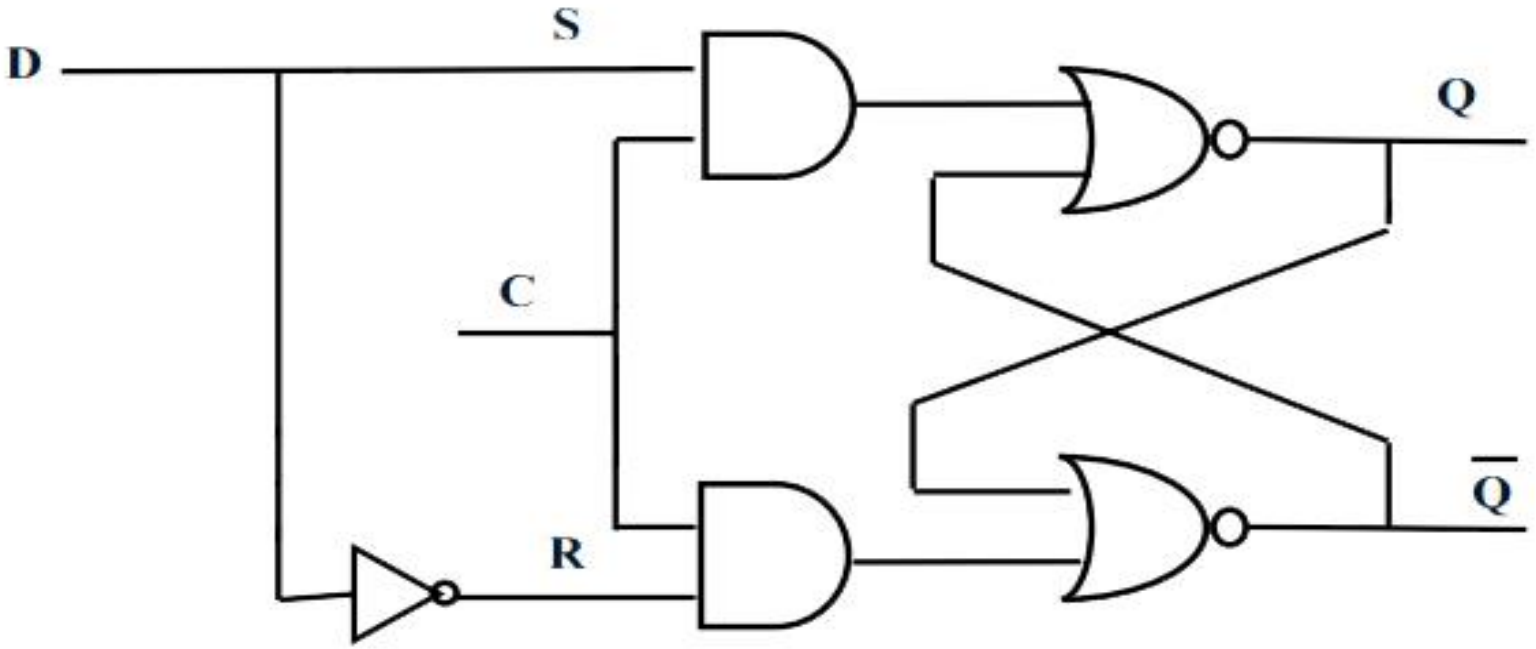
From the above figure, you can see that the D input is connected to the S input and the complement of the D input is connected to the R input.

When the value of CP is '1' (HIGH), the flip-flop moves to the SET state if it is '0' (LOW), the flip-flop switches to the CLEAR state.

D Flip-Flop

$$Q^* = D$$

- If we connct the input FF D to S and its complement to R the D Flip Flop will be made



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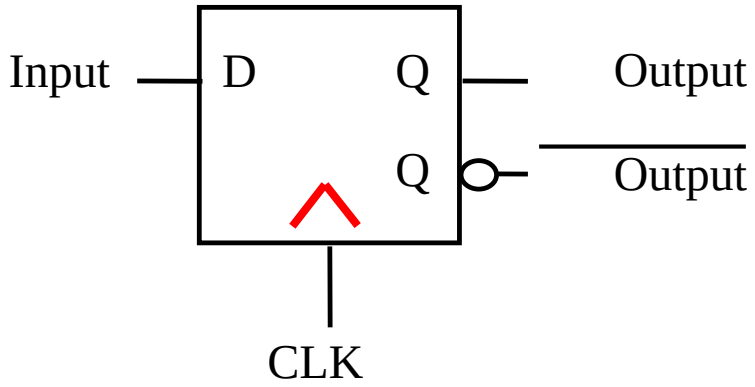
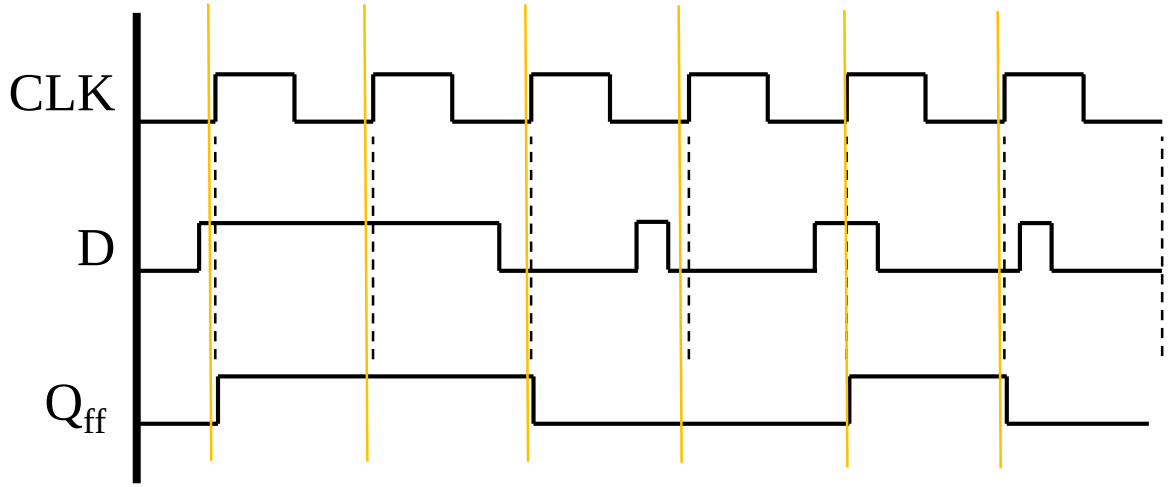
The D flip-flop

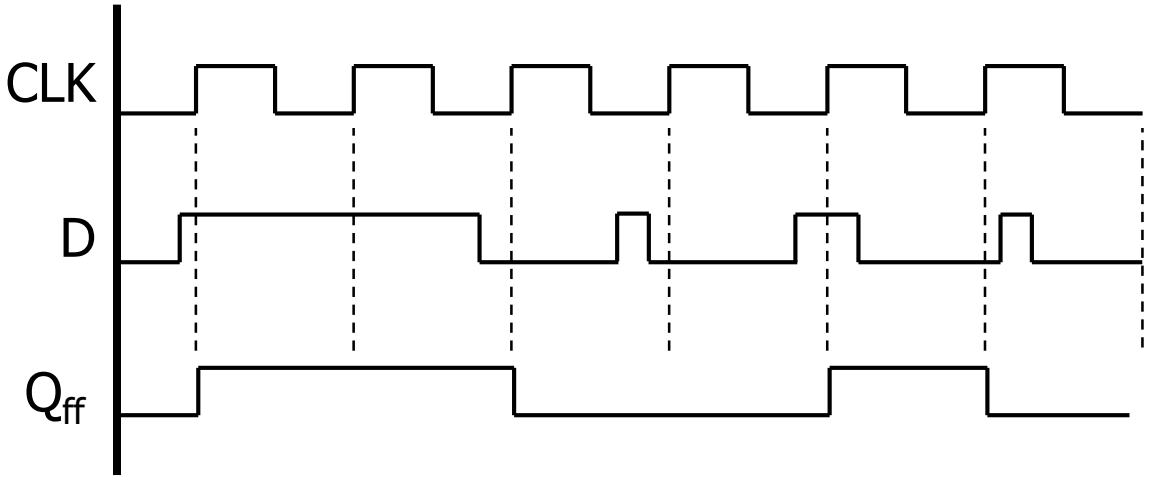
- Input sampled at clock edge
  - Rising edge: Input passes to output
  - Otherwise: Flip-flop holds its output
- Flip-flops can be rising-edge triggered or falling-edge triggered

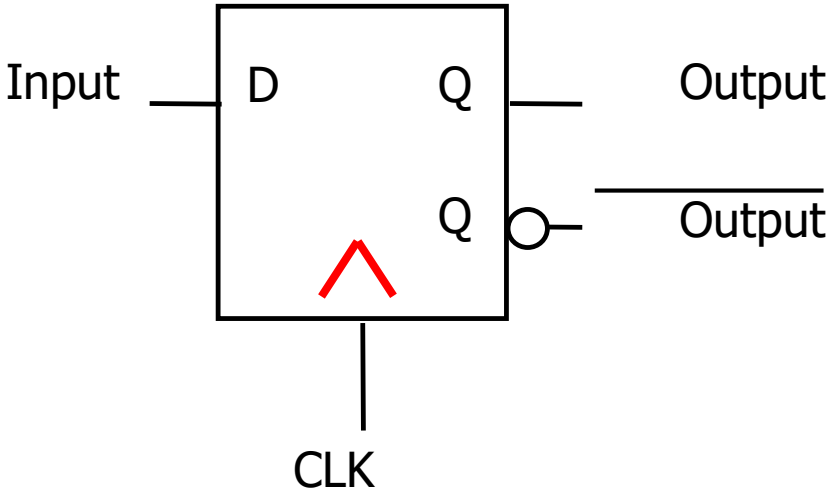




The D flip-flop

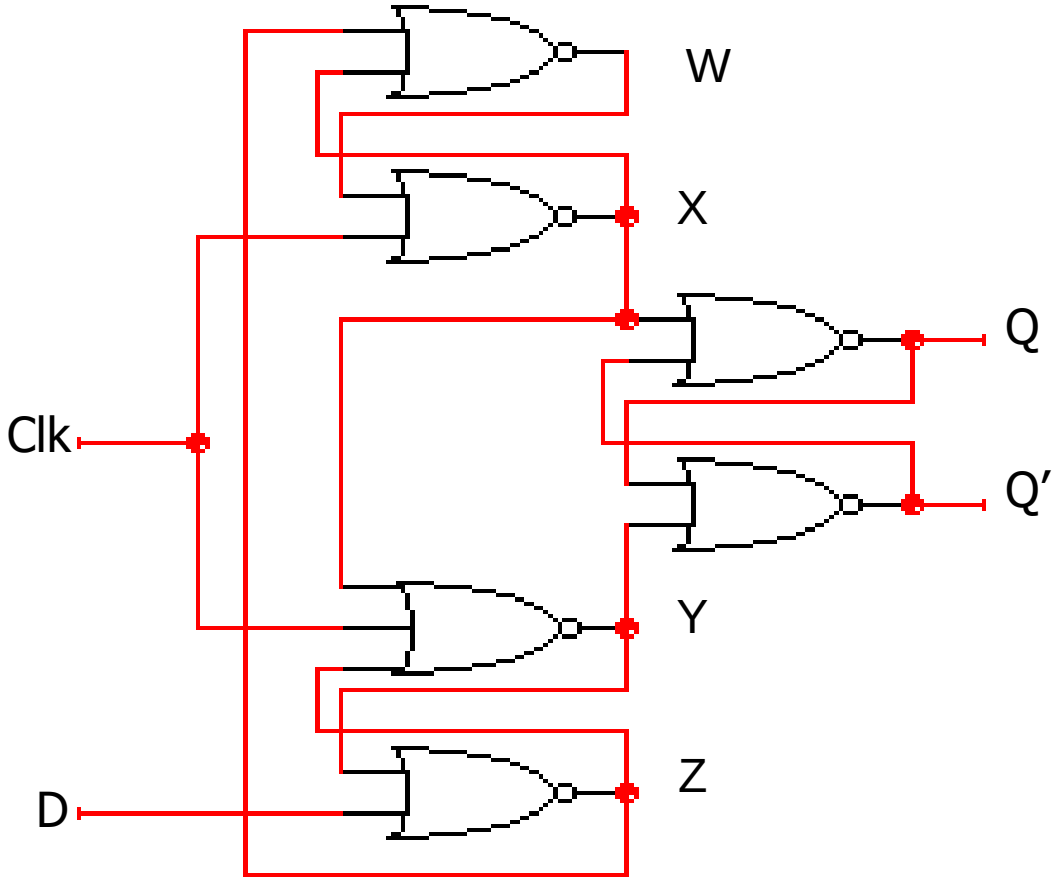
- D flip-flop is a slight modification of clocked SR flip-flop.





How do we make a D flip flop?

- Edge triggering is difficult
  - You can do this at home:
    - Label the internal nodes
    - Draw a timing diagram
    - Start with Clk=1



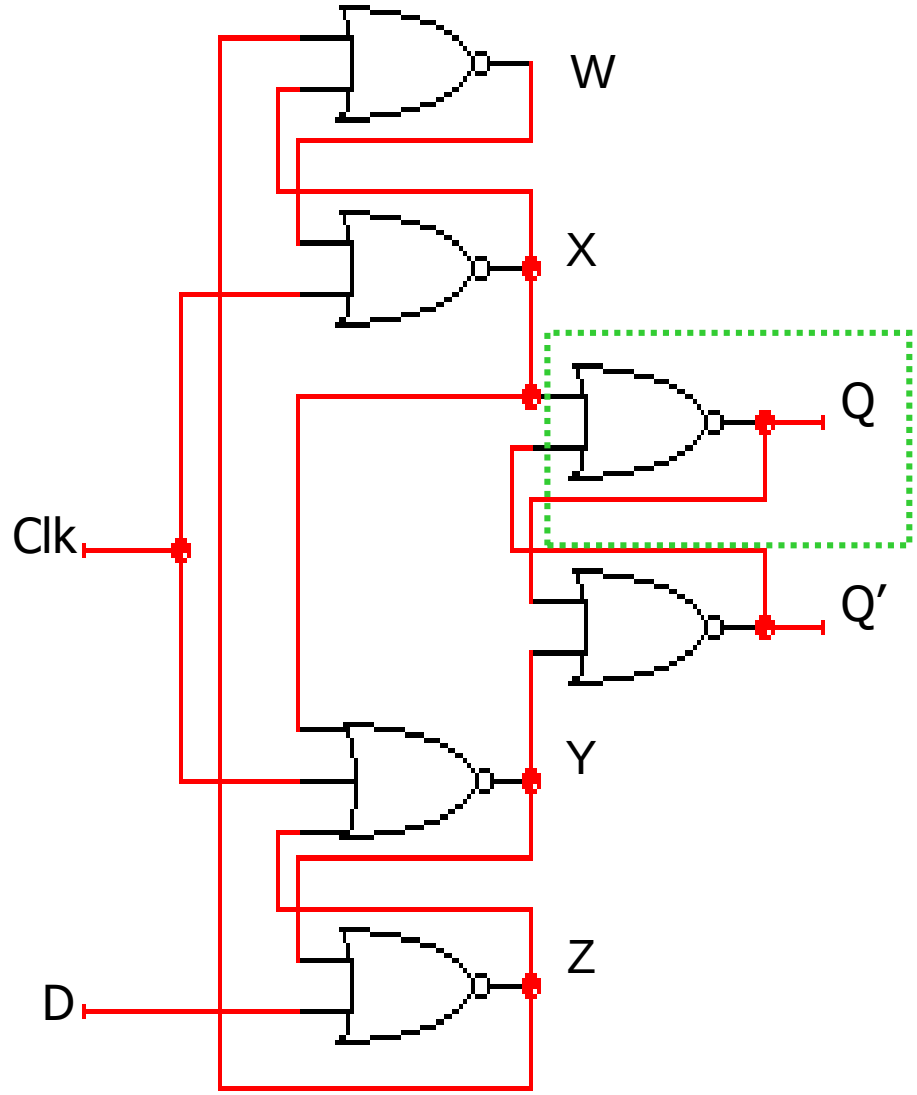
How do we make a D flip flop?

Falling edge-triggered flip-flop

If **Clk=1** then **X=Y=0** and SR-latch block
holds previous values of **Q,Q'**
also **Z=D'** and **W=Z'=D**

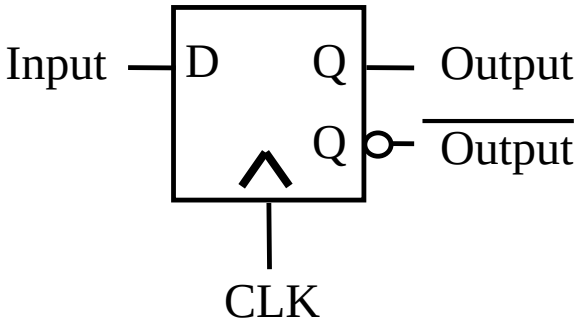
When **Clk→0** then **Y** (set for SR-latch block)
becomes **Z'=D**
and **X** (reset for SR-latch block)
becomes **W'=D'**
so **Q** becomes **D**
This is stable until **D** or the **Clk** switches

While **Clk=0**, if **D** switches then **Z** becomes **0** and
X and **W** hold their previous values and **Y=X'=D** as before.

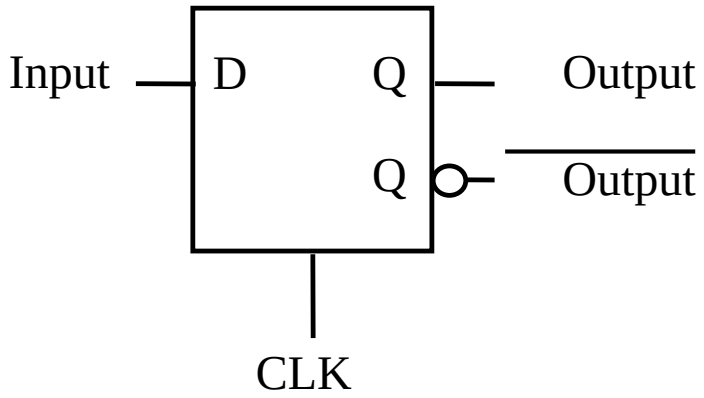


Terminology & notation

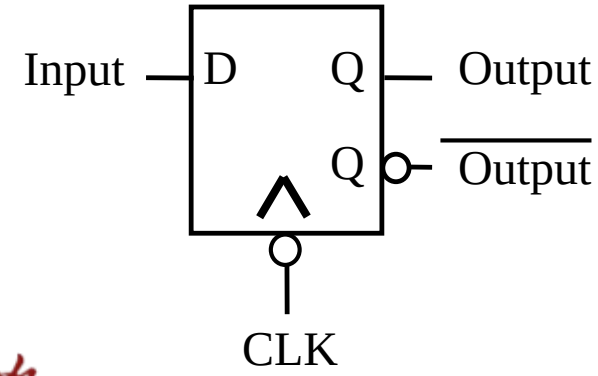
Rising-edge triggered D flip-flop



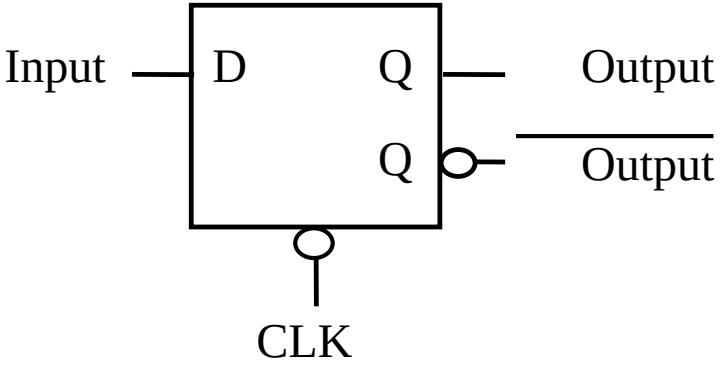
Positive D latch



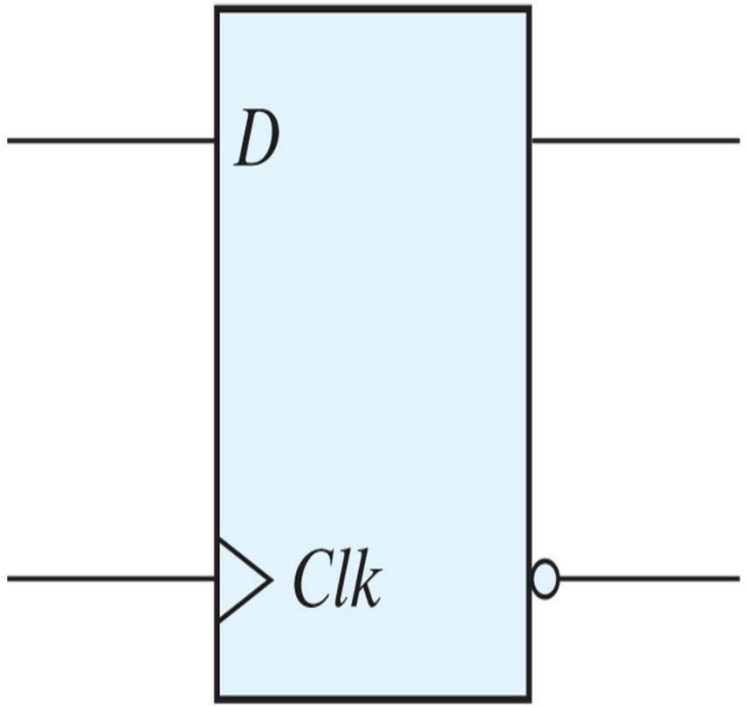
Falling-edge triggered D flip-flop



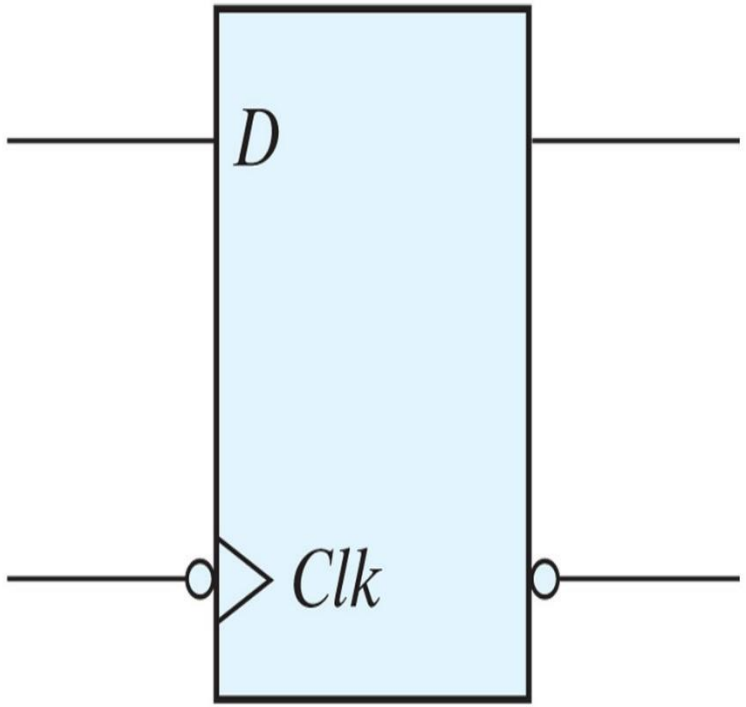
Negative D latch



Graphic symbol for edge-triggered *D* flip-flop

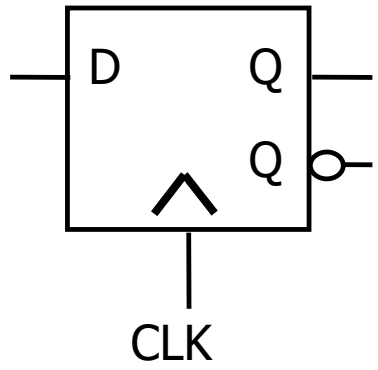


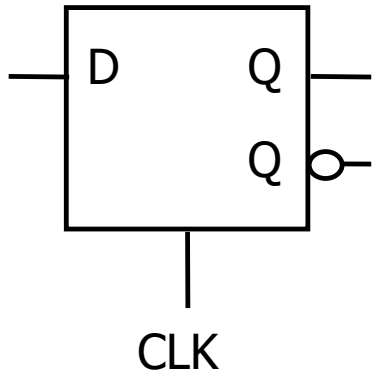
(a) Positive-edge

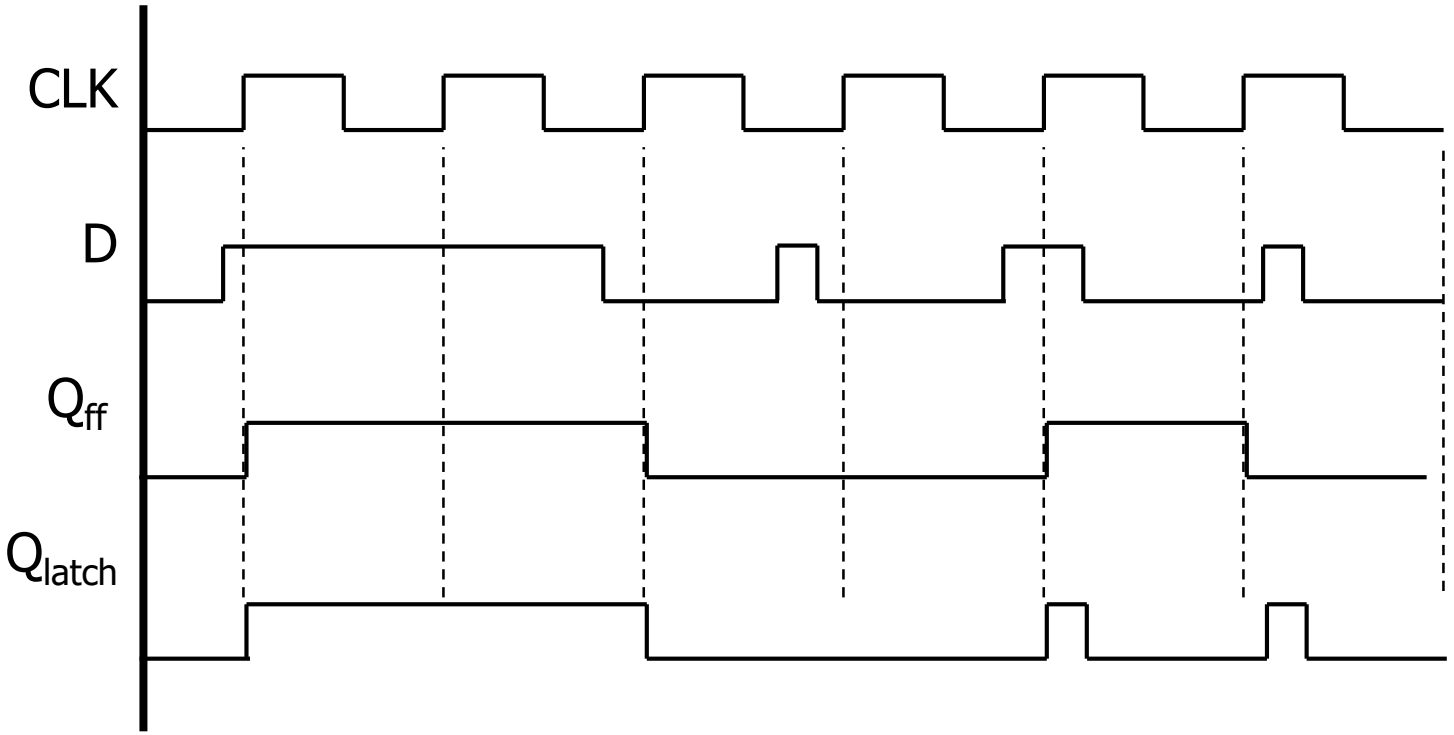


(a) Negative-edge

Latches versus flip-flops

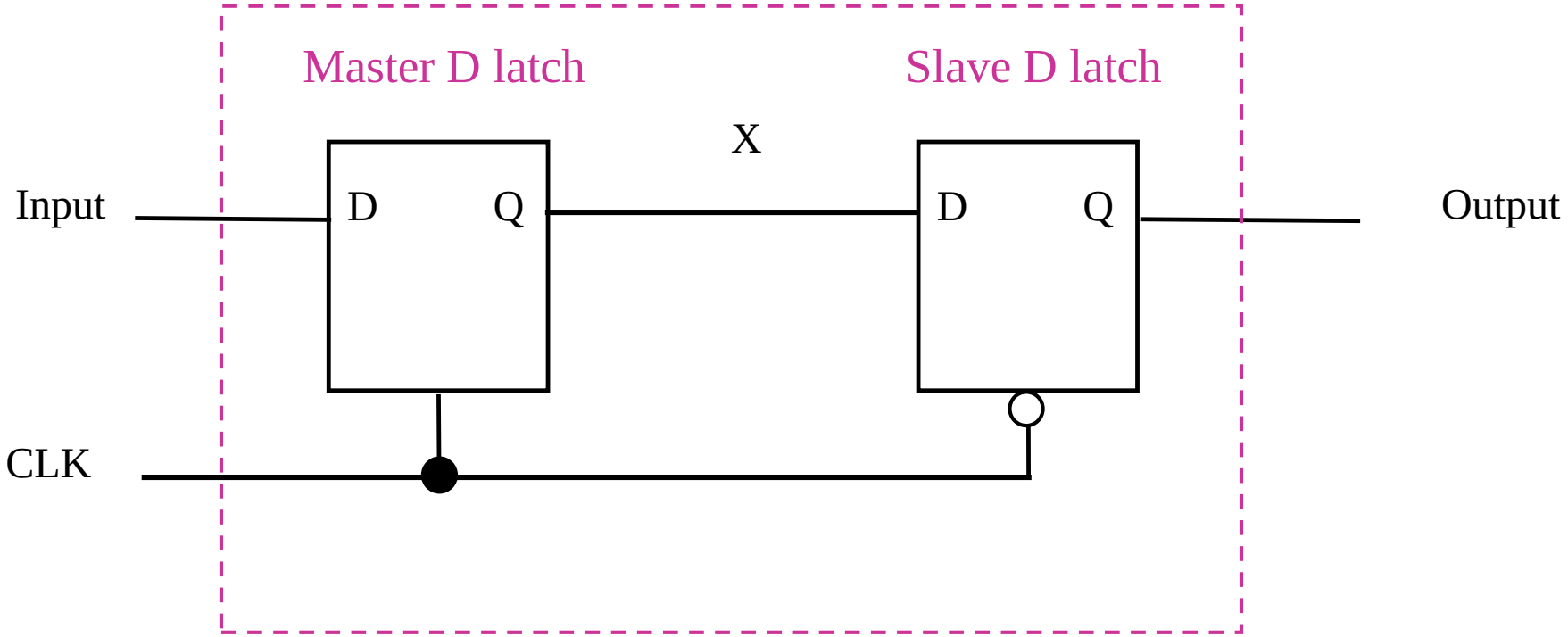




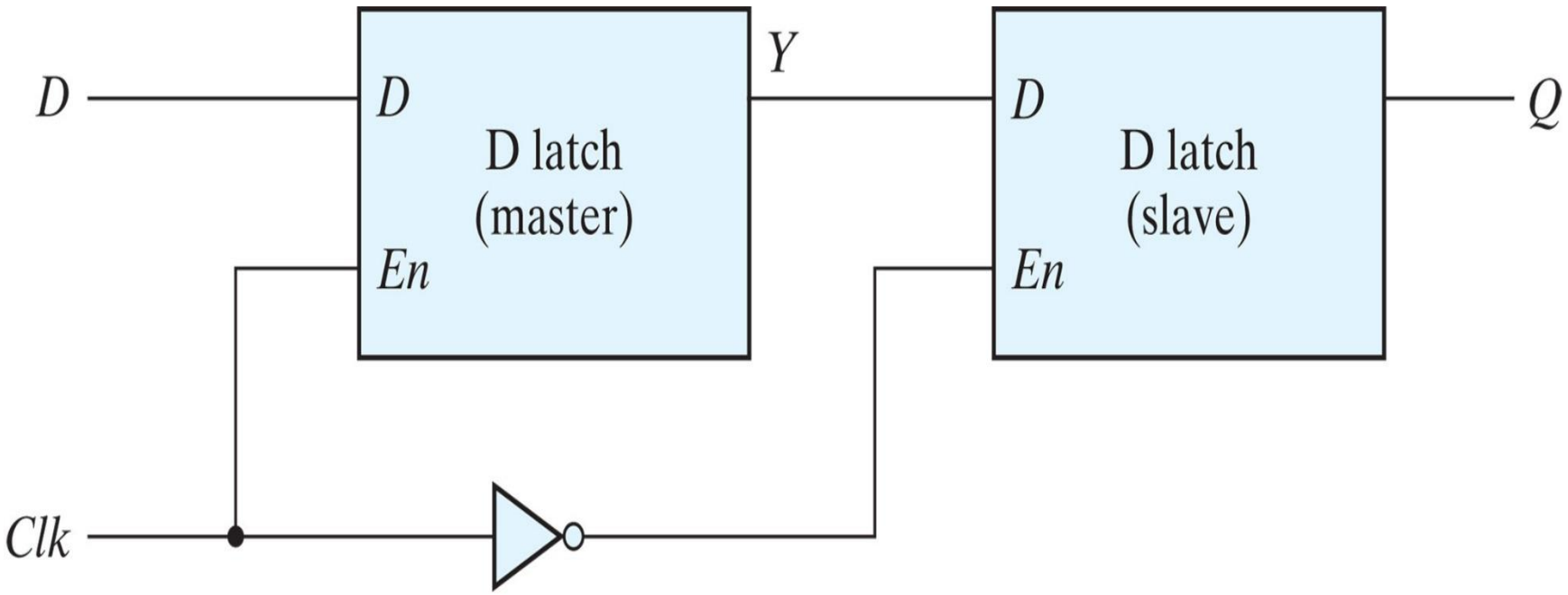


behavior is the same unless input changes while the clock is high

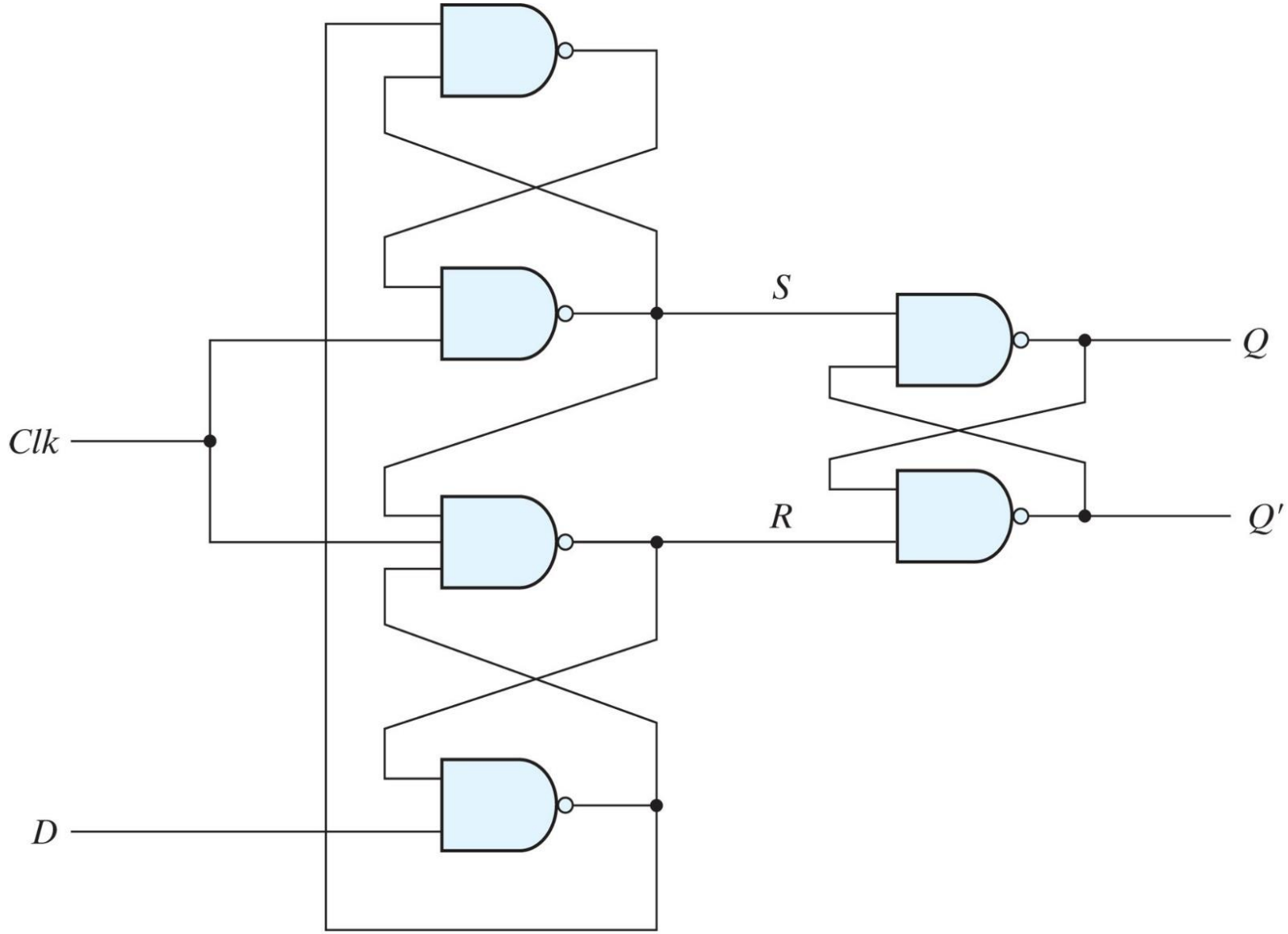
The master-slave D



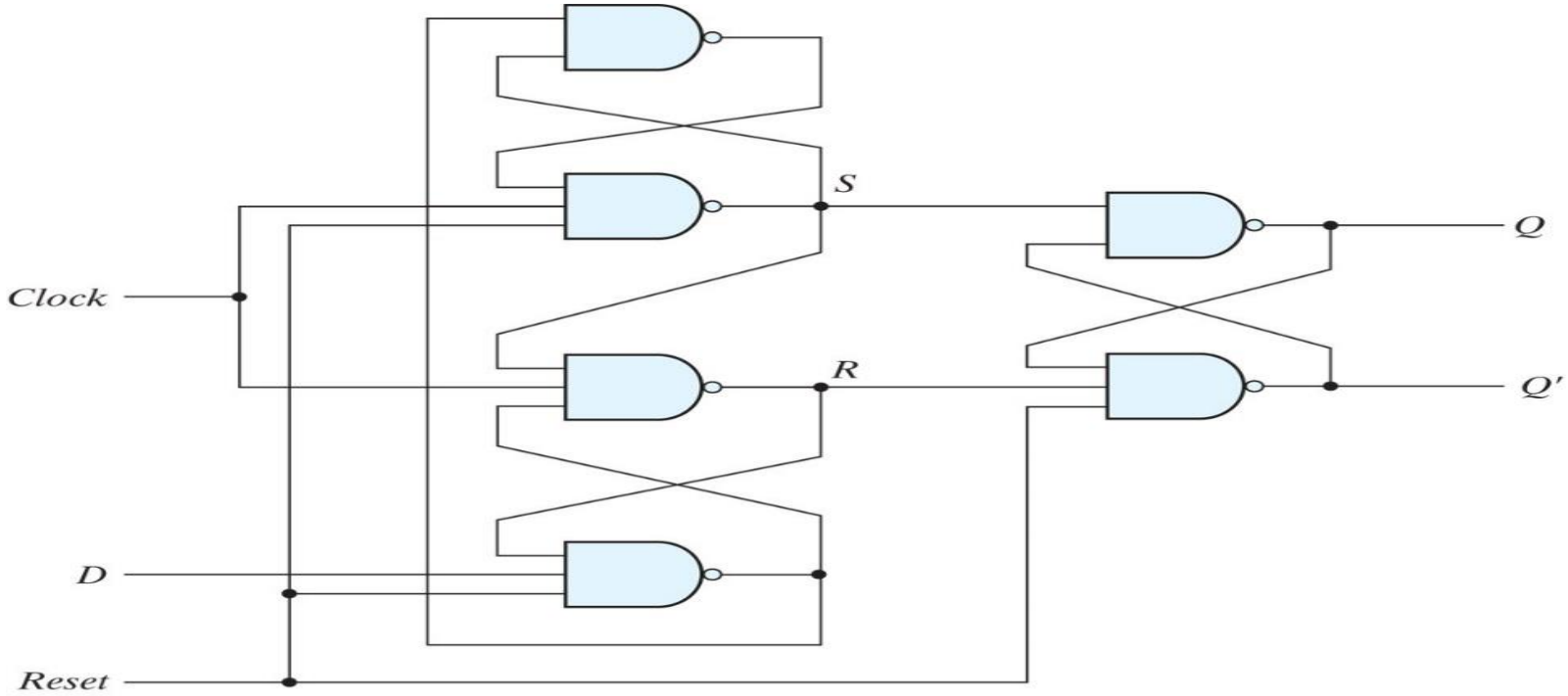
Master–slave *D* flip-flop



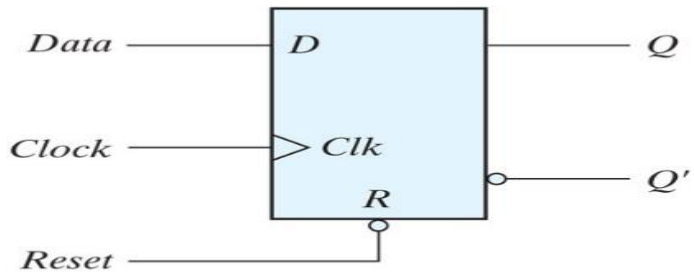
D-type positive-edge-triggered flip-flop



D flip-flop with asynchronous reset



(a) Circuit diagram

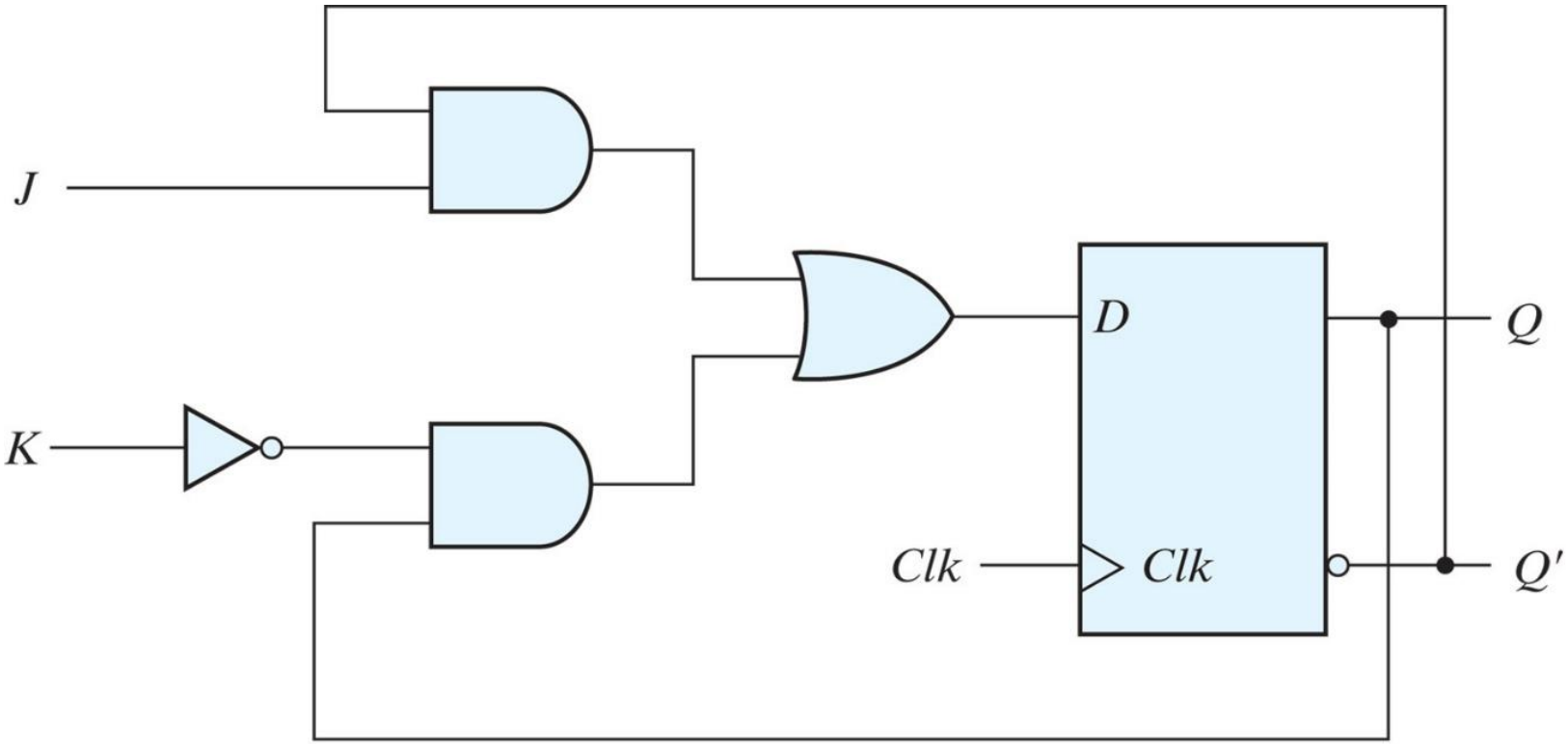


(b) Graphic symbol

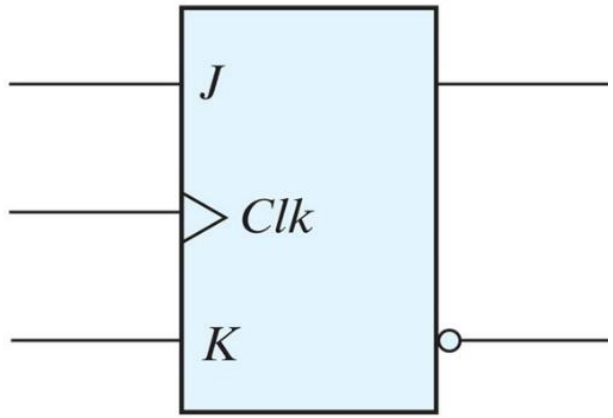
R	*Clk*	*D*	*Q*	*Q′*
0	X	X	0	1
0	↑	0	0	1
0	↑	1	1	0

(b) Function table

JK flip-flop



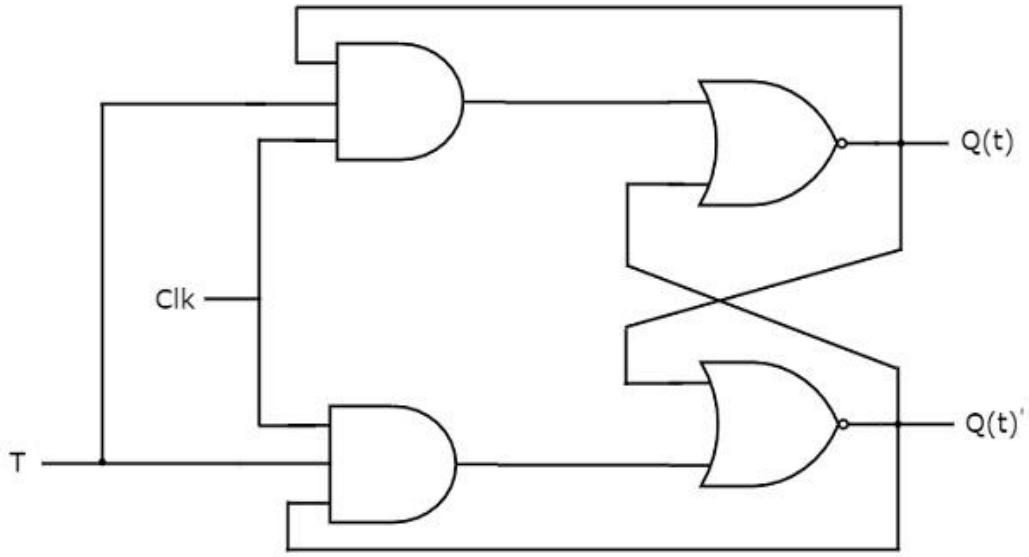
(a) Circuit diagram



(b) Graphic symbol

T Flip-Flop

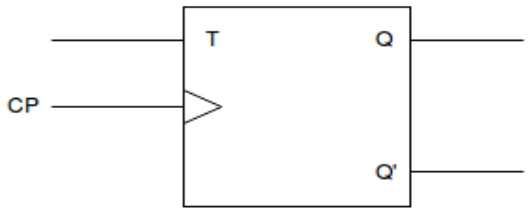
- T flip-flop is the simplified version of JK flip-flop. It is obtained by connecting the same input 'T' to both inputs of JK flip-flop.
- It operates with only positive clock transitions or negative clock transitions.
- **The circuit diagram of T flip-flop is shown in the following figure**



This circuit has single input T and two outputs Q(t) & Q(t)'.
The operation of T flip-flop is same as that of JK flip-flop.

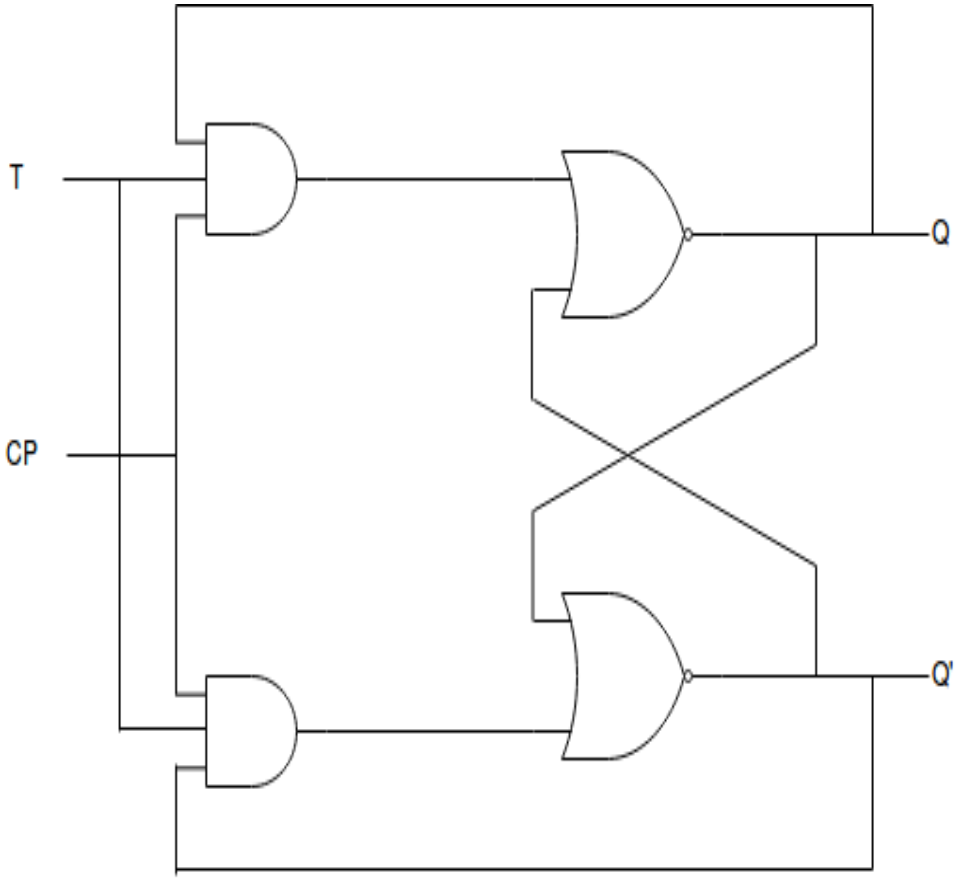
Here, we considered the inputs of JK flip-flop as **J = T** and **K = T** in order to utilize the modified JK flip-flop for 2 combinations of inputs. So, we eliminated the other two combinations of J & K, for which those two values are complement to each other in T flip-flop.

T Flip-Flop



c) Graphical symbol

fig. Clocked T flip flop



a) Logic diagram

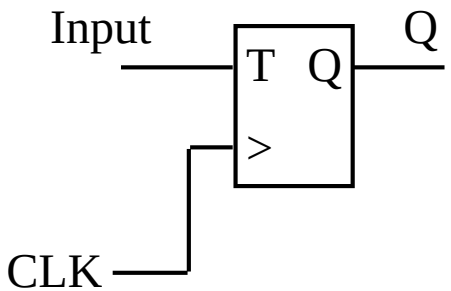
Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

b) Transition table

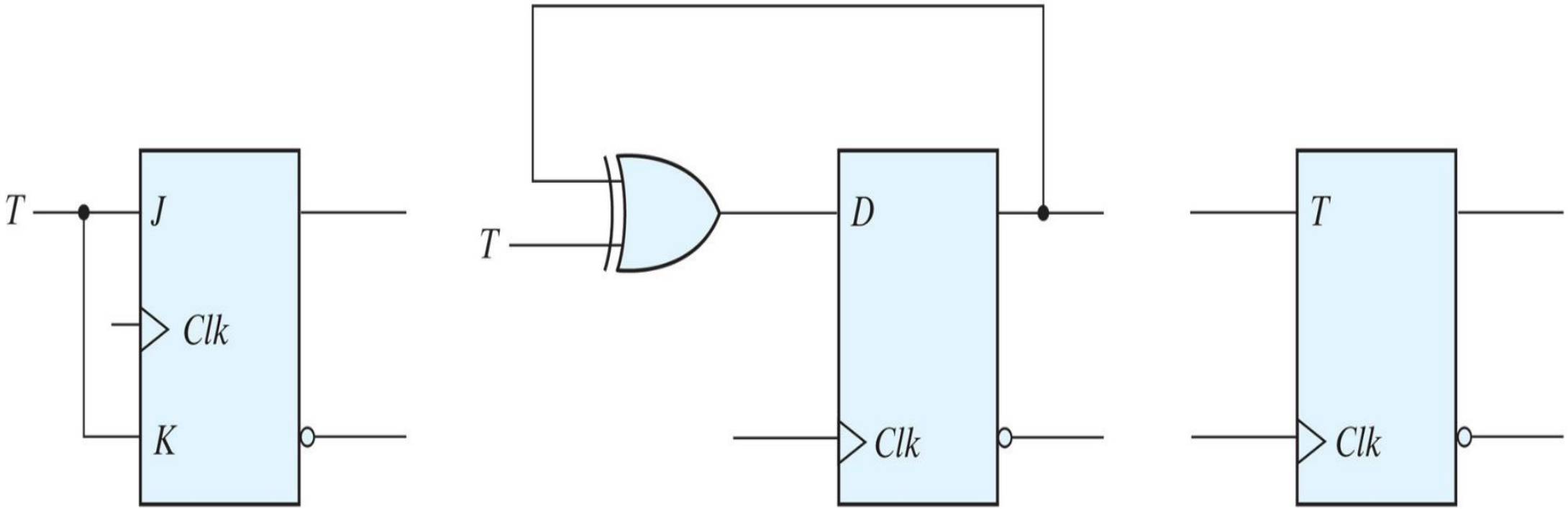
T flip-flop

- Full name: Toggle flip-flop
- Output toggles when input is asserted
  - If T=1, then Q → Q' when CLK ↑
  - If T=0, then Q → Q when CLK ↑

Input(t)	Q(t)	Q($t + \Delta t$)
0	0	0
0	1	1
1	0	1
1	1	0



T flip-flop



(a) From *JK* flip-flop (b) From *D* flip-flop (c) Graphic symbol

T flip-flop

- Here, Q(t) & Q(t + 1) are present state & next state respectively.
- So, T flip-flop can be used for one of these two functions such as Hold, & Complement of present state based on the input conditions, when positive transition of clock signal is applied.
- The following table shows the **characteristic table** of T flip-flop.

Inputs	Present State	Next State
T	**Q(t)**	**Q(t + 1)**
0	0	0
0	1	1
1	0	1
1	1	0

T flip-flop

From the above characteristic table, we can directly write the **next state equation** as

$$Q(t+1)=T'Q(t)+TQ(t)'Q(t+1)=T'Q(t)+TQ(t)'$$

$$\Rightarrow Q(t+1)=T\oplus Q(t)\Rightarrow Q(t+1)=T\oplus Q(t)$$

The output of T flip-flop always toggles for every positive transition of the clock signal, when input T remains at logic High (1). Hence, T flip-flop can be used in **counters**.

https://www.tutorialspoint.com/digital_circuits/digital_circuits_conversion_of_flip_flops.htm

https://www.electronics-tutorials.ws/sequential/seq_1.html

Flip-Flop Characteristic Tables

Table 5.1
Flip-Flop Characteristic Tables

JK Flip-Flop

J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

D Flip-Flop

D	Q(t + 1)	
0	0	Reset
1	1	Set

T Flip-Flop

T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

Clear and preset in flip-flops

- Clear and Preset set flip-flop to a known state
  - Used at startup, reset
- Clear or Reset to a logic 0
  - Synchronous: Q=0 when next clock edge arrives
  - Asynchronous: Q=0 when reset is asserted
    - Doesn't wait for clock
    - Quick but dangerous
- Preset or Set the state to logic 1
  - Synchronous: Q=1 when next clock edge arrives
  - Asynchronous: Q=1 when reset is asserted
    - Doesn't wait for clock
    - Quick but dangerous

Reference

1. Mano book
2. ee.hawaii.edu/~sasaki/EE361/Fall06/Lab/7disp.html
3. https://www.tutorialspoint.com/computer_logical_organization/combinational_circuits.htm
4. https://www.electronics-tutorials.ws/sequential/seq_1.html