江西理工大学
Jiangxi University of Science and Technology
信息工程学院
School of information engineering

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Digital System Design

Clip Lecture series

Spring_2020

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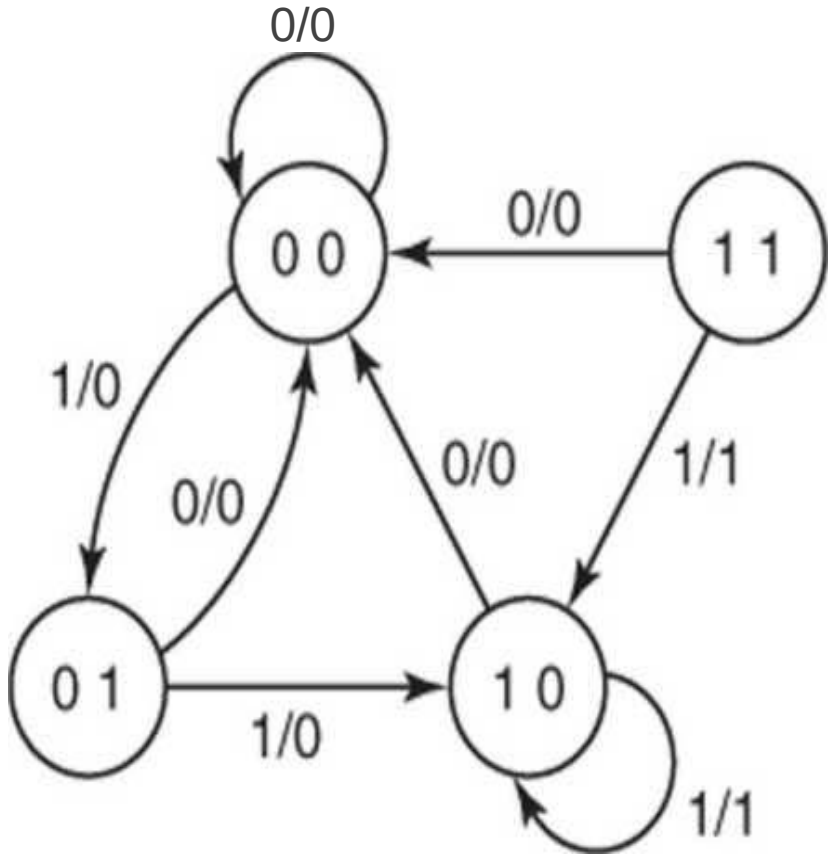
Jiangxi University of Science and Technology

Sequential circuits

3 example with detail solution

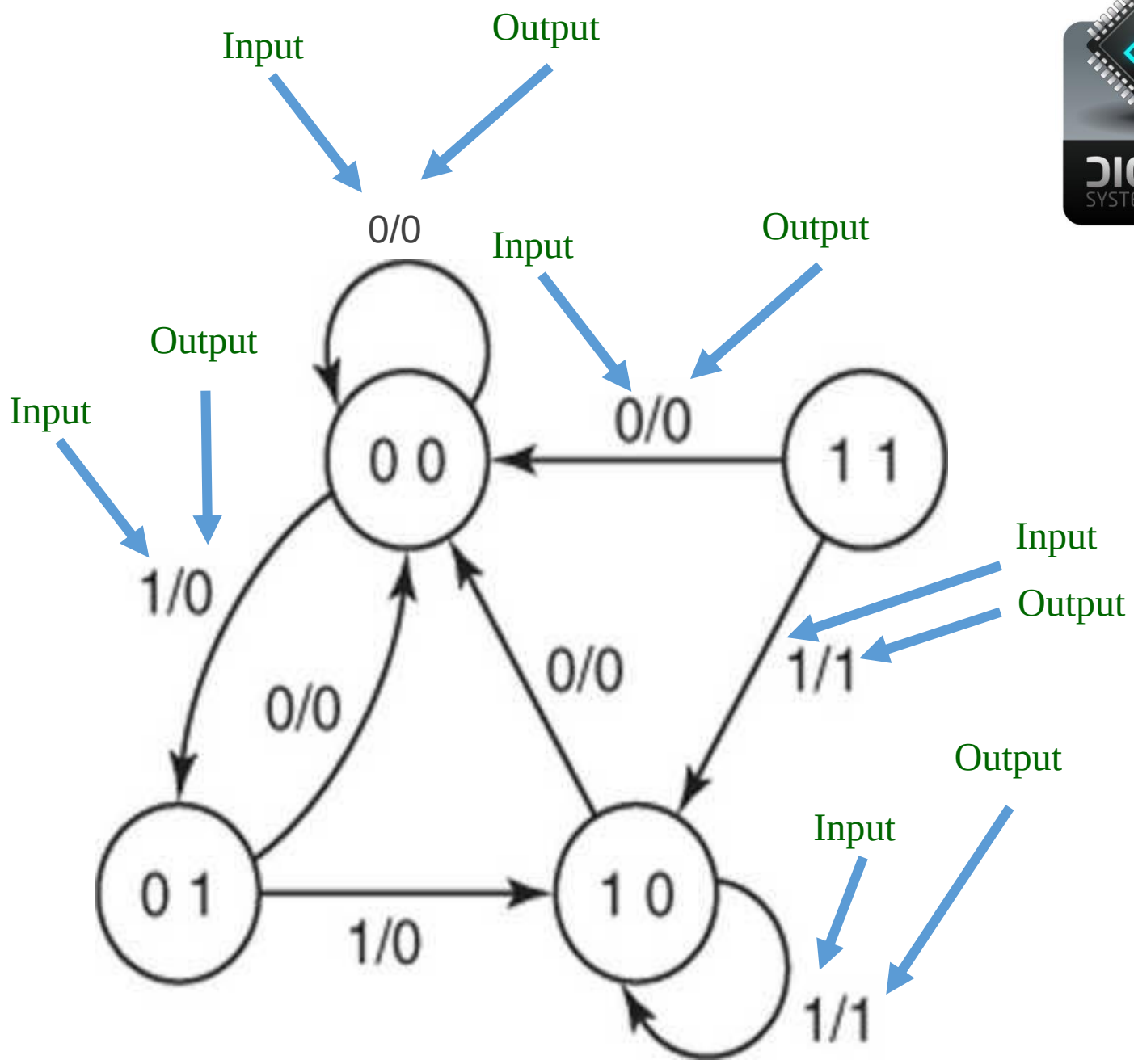
Example 1

Design the circuit with the help of D flip Flop and write the State Table for the below State Diagram,



Example 1

Design the circuit with the help of D flip Flop and write the State Table for the below State Diagram,



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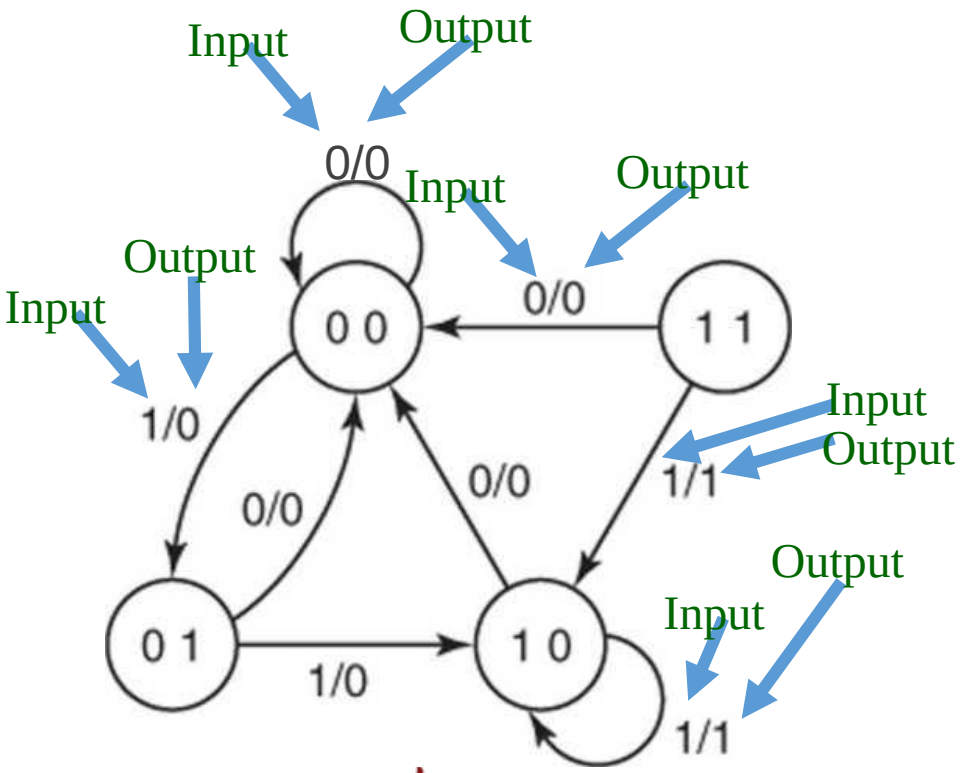
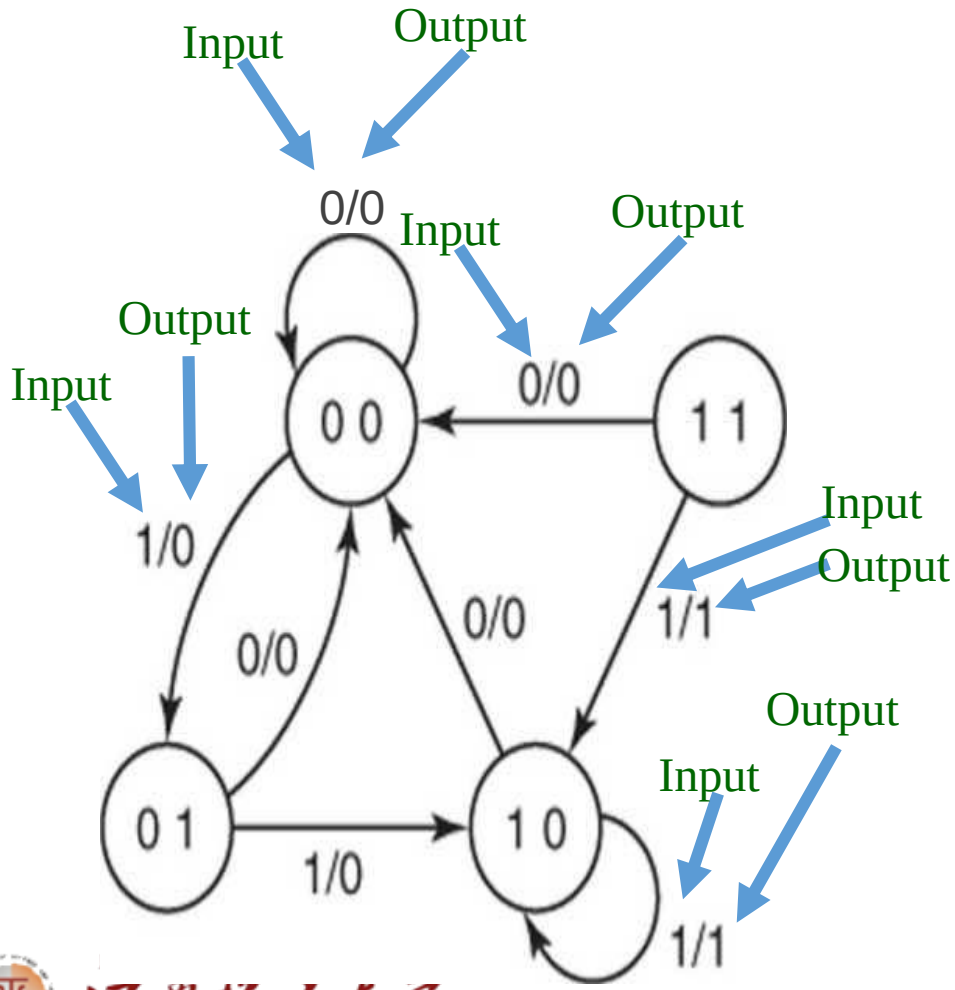


The ckt input			Next state		OUTPUT Z
Input	Current state				
X=0	*A*	*B*	*A*	*B*	X=0
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0

Example 1

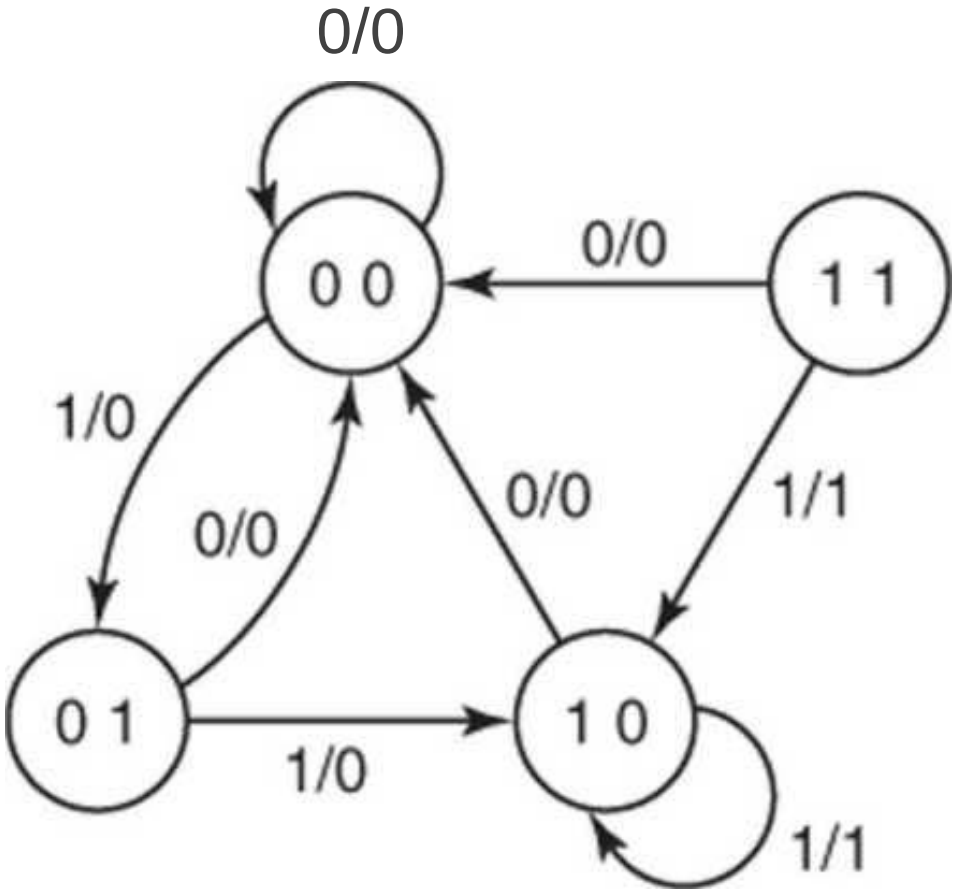
Design the circuit with the help of D flip Flop and write the State Table for the below State Diagram,



The ckt input			Next state		OUTPUT Z
Input	Current state				
X=1	*A*	*B*	*A*	*B*	X=1
1	0	0	0	1	0
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	0	1

Example 1

Design the circuit with the help of D flip Flop and write the State Table for the below State Diagram,

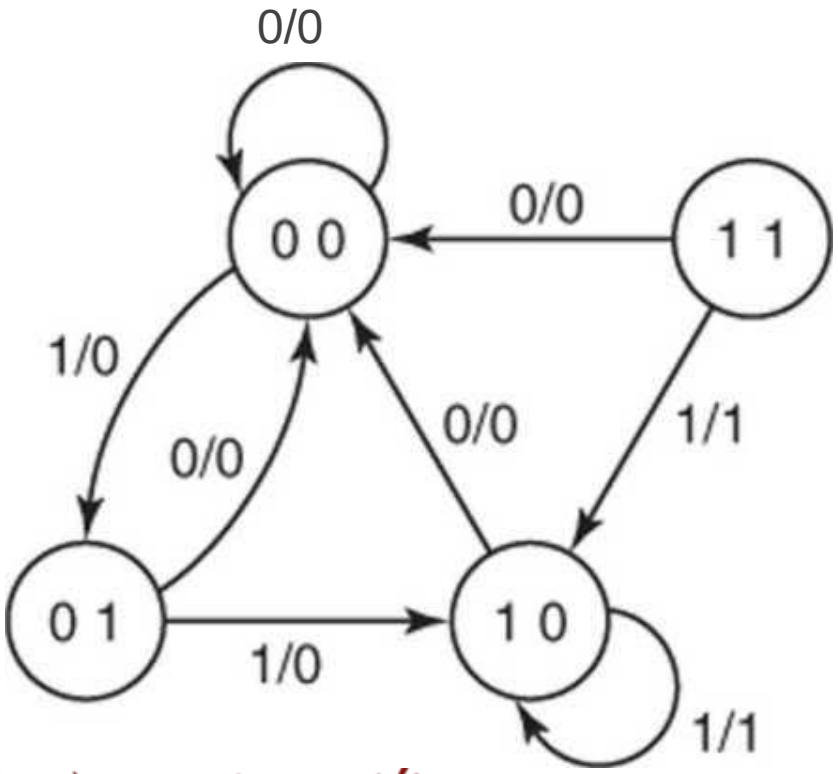


The ckt input			Next state		OUTPUT Z
Input	Current state				
X=0	*A*	*B*	*A*	*B*	X=0
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0

The ckt input			Next state		OUTPUT Z
Input	Current state				
X=1	*A*	*B*	*A*	*B*	X=1
1	0	0	0	1	0
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	0	1

Example 1

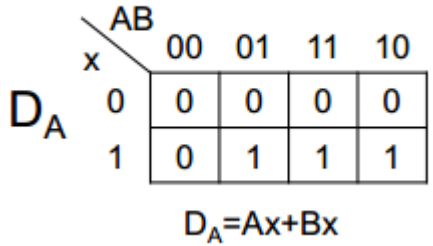
Design the circuit with the help of D flip Flop and write the State Table for the below State Diagram,



q (A B)	q^* $x=0$ (A B)	q^* $x=1$ (A B)	z $x=0$	z $x=1$
0 0	0 0	0 1	0	0
0 1	0 0	1 0	0	0
1 0	0 0	1 0	0	1
1 1	0 0	1 0	0	1

D-FF characteristic eq: D = Q*

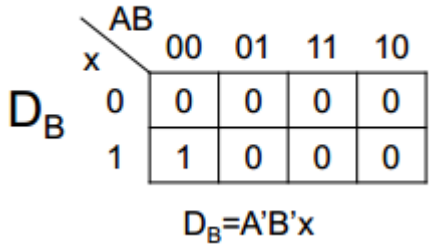
Example 1



D_A	AB: 00	01	11	10
x=0	0	0	0	0
x=1	0	1	1	1

$D_A = Ax + Bx$

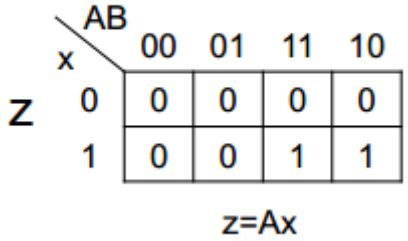
A	B	X
0	1	1
1	0	1
1	1	1



D_B	AB: 00	01	11	10
x=0	0	0	0	0
x=1	1	0	0	0

$D_B = A'B'x$

A	B	X
0	0	1



z	AB: 00	01	11	10
x=0	0	0	0	0
x=1	0	0	1	1

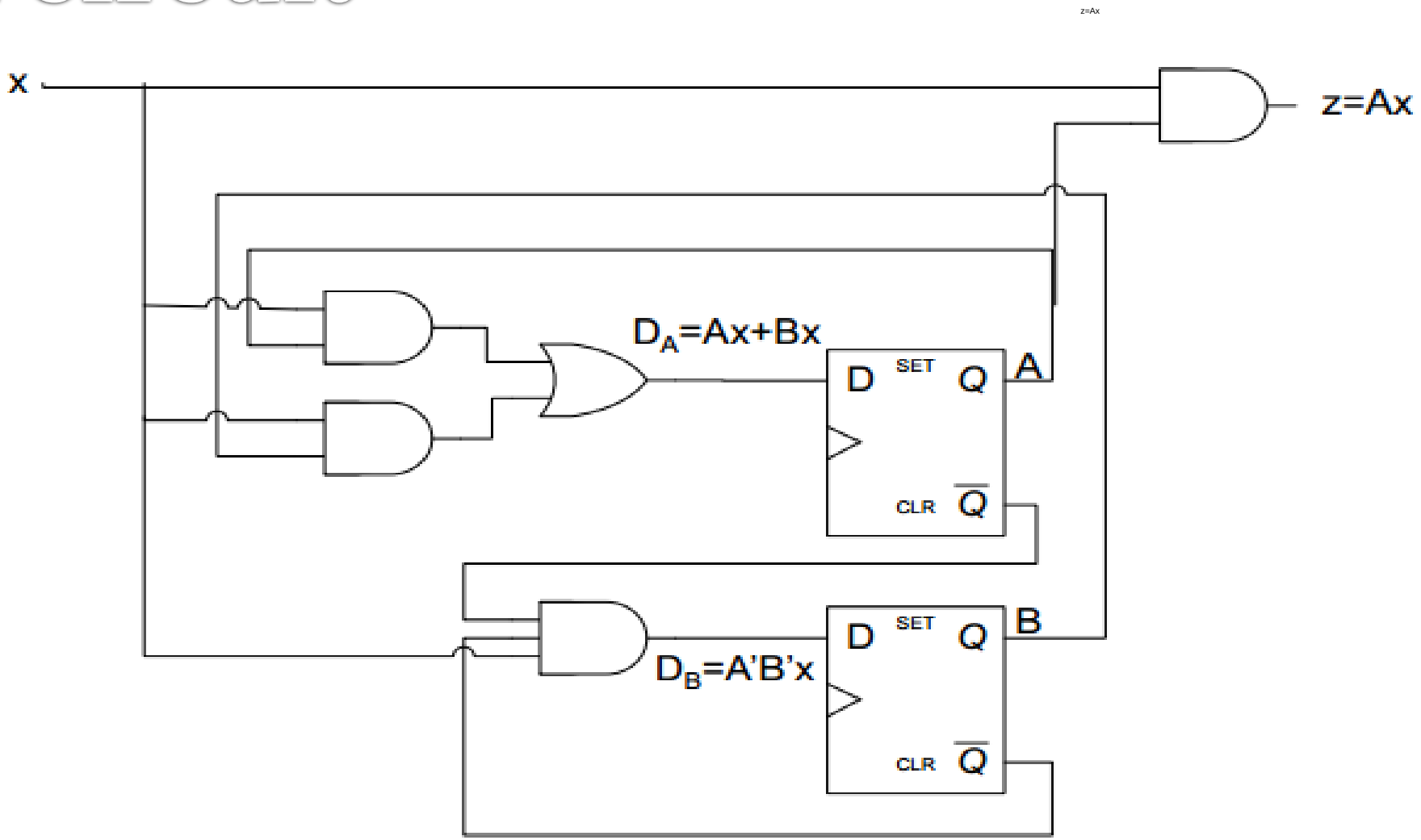
$z = Ax$

A	B	X
1	1	1
1	0	1

q	q^* x=0	q^* x=1	z x=0	z x=1
A B	A B	A B		
0 0	0 0	0 1	0	0
0 1	0 0	1 0	0	0
1 0	0 0	1 0	0	1
1 1	0 0	1 0	0	1

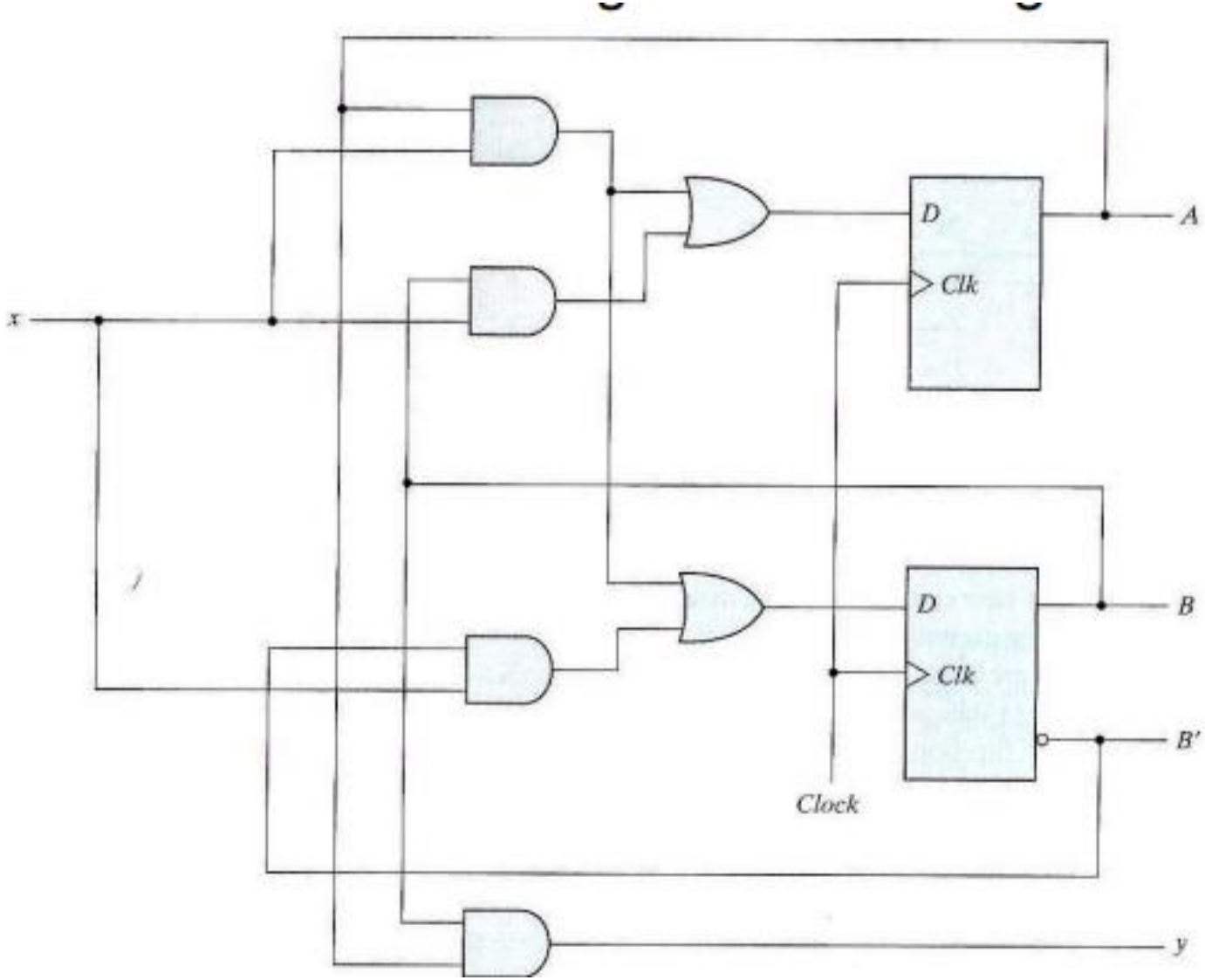
D-FF characteristic eq: D = Q*

Example 1
Design circuit



Example 2

Show the state diagram of following circuit



Example 2
Show the state diagram of following circuit

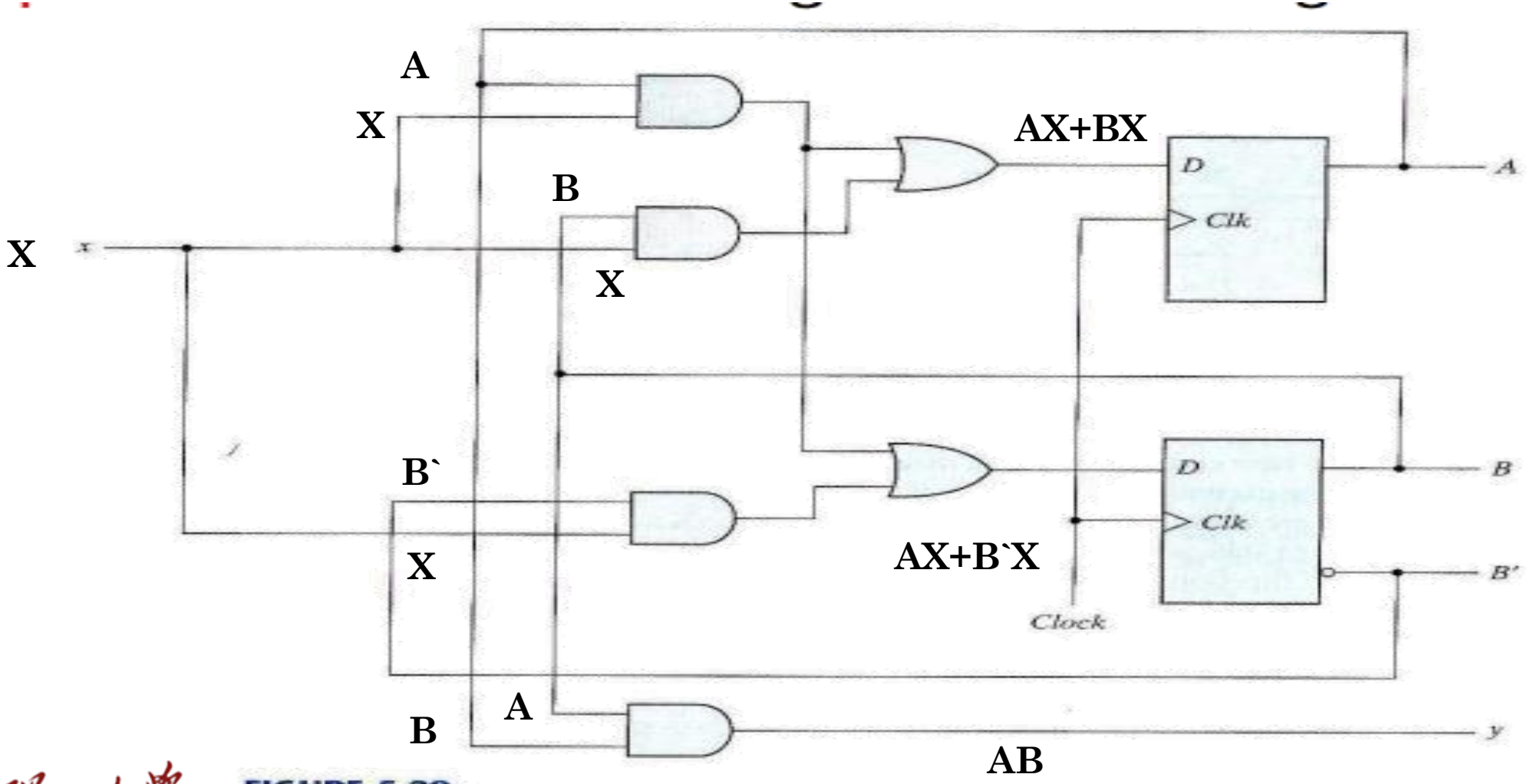


FIGURE 5.29
Logic diagram of sequence detector

Example 2
Show the state diagram of following circuit

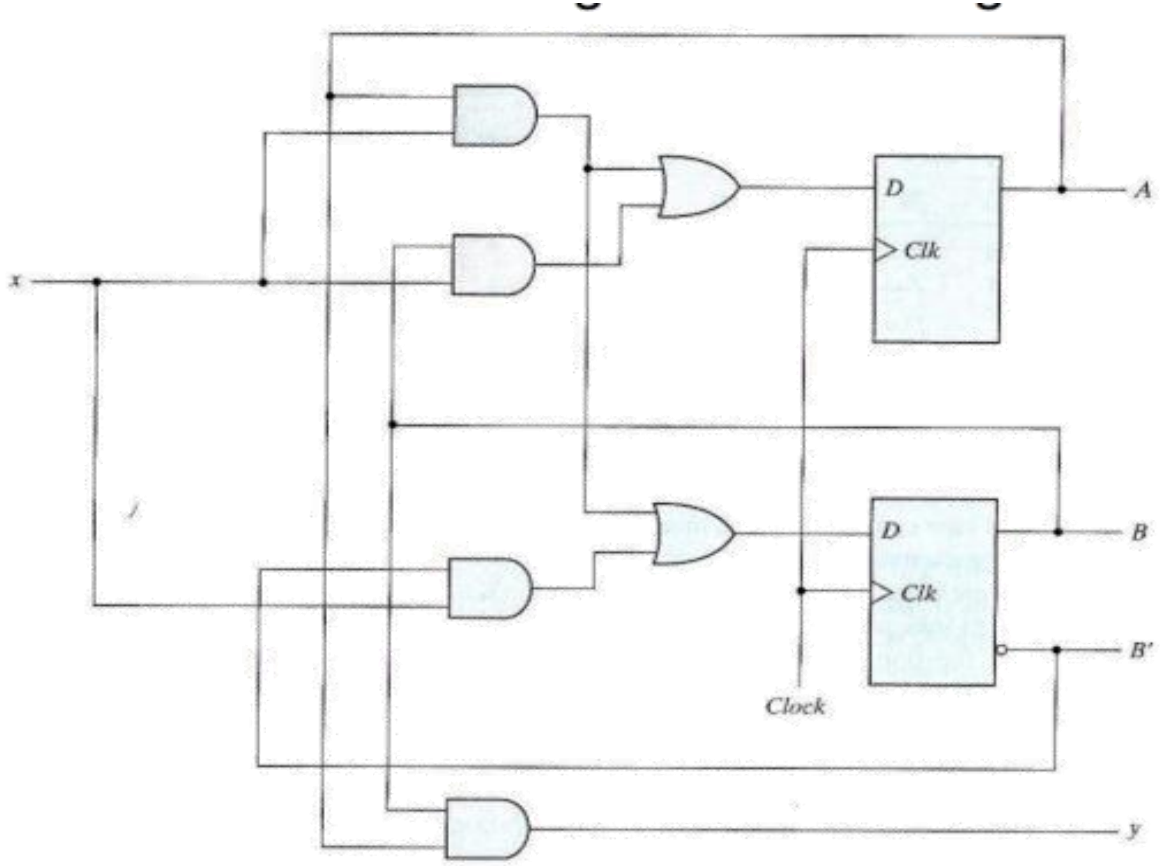


FIGURE 5.29
Logic diagram of sequence detector

$y = AB$
$D_A = Ax + Bx$
$D_B = Ax + B'x$

$y = AB$
$D_A = Ax + Bx$
$D_B = Ax + B'x$

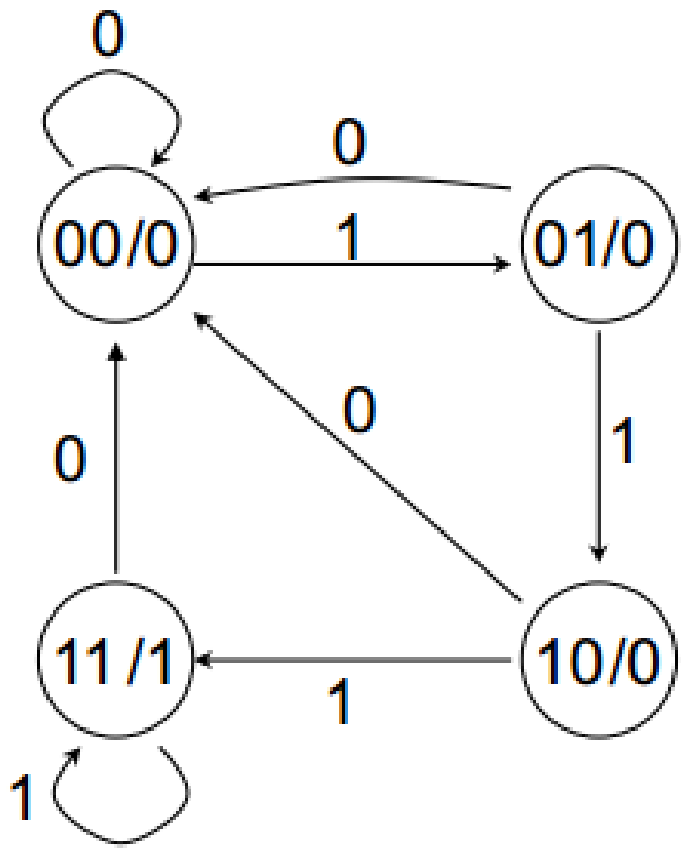
x: input, y: output
A, B: present state
D_A, D_B: next state (D-FF)

Example 2

The ckt input			Next state		OUTPUT Y
Input	Current state				
X=0	*A*	*B*	*A*	*B*	X=0
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	1

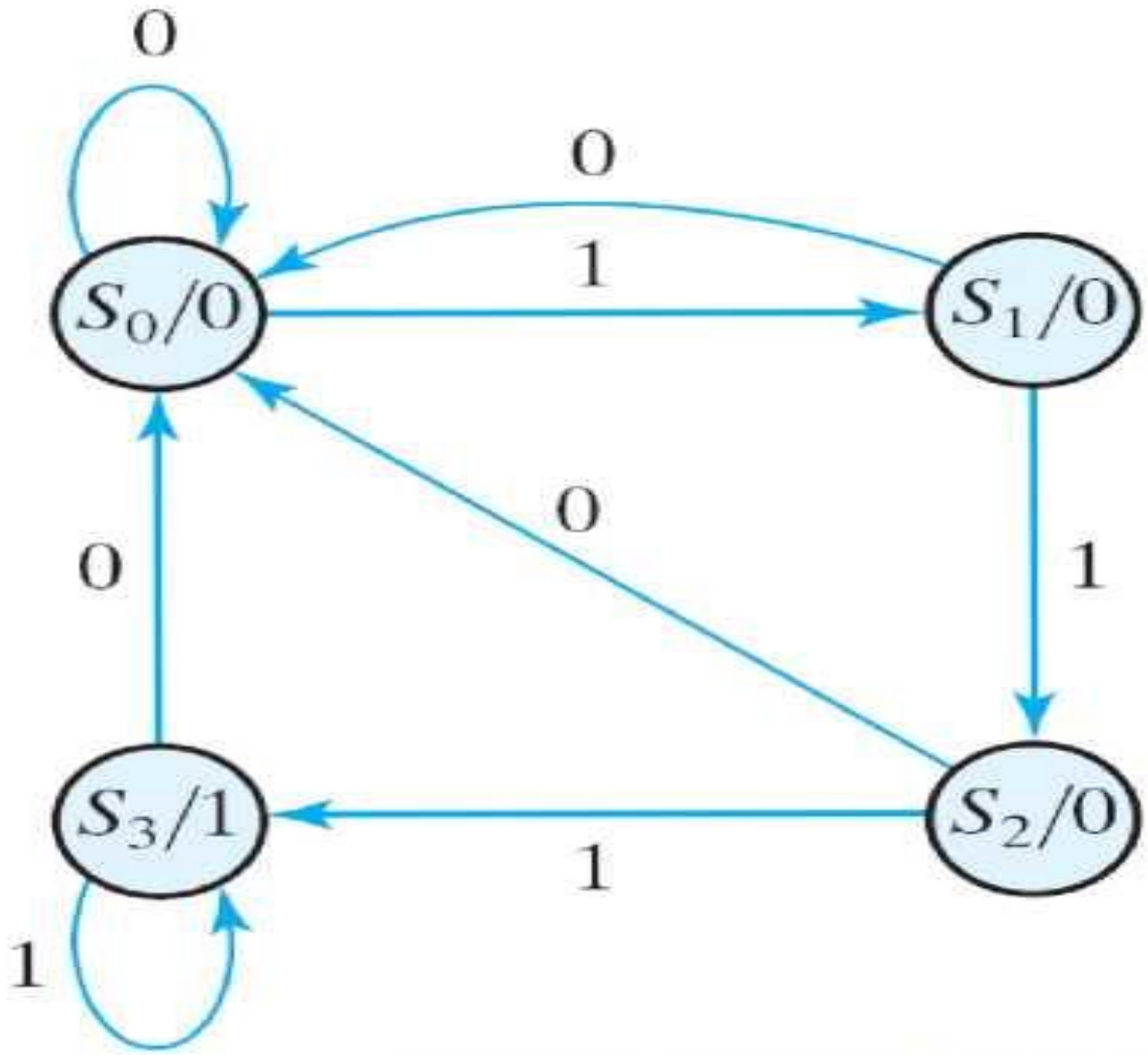
The ckt input			Next state		OUTPUT Y
Input	Current state				
X=1	*A*	*B*	*A*	*B*	X=1
1	0	0	0	1	0
1	0	1	1	0	0
1	1	0	1	1	0
1	1	1	1	1	1

Example 2



Present State		Next State				Output
		$x = 0$		$x = 1$		
A	B	A	B	A	B	y
0	0	0	0	0	1	0
0	1	0	0	1	0	0
1	0	0	0	1	1	0
1	1	0	0	1	1	1

Example 2



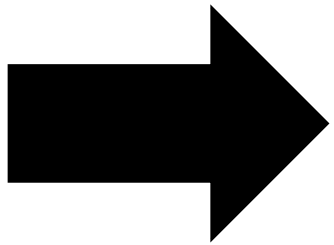
Example 3

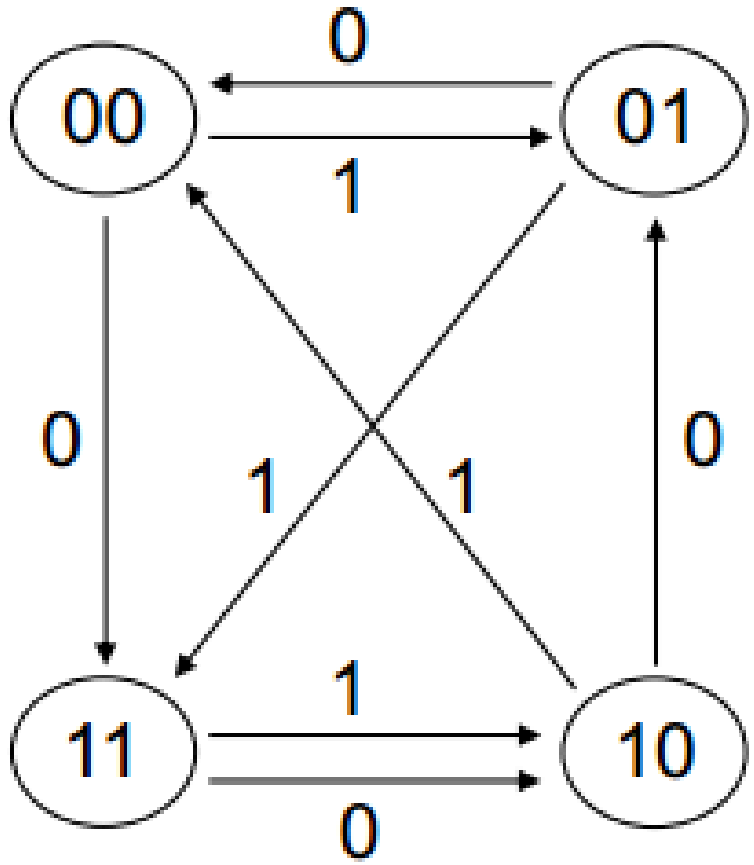
Design a 2-bit complex counter with one input x that can be
- a down counter when x=0 (...→11 → 10 → 01 → 00 → 11 →...)
- a Johnson counter when x=1 (... → 00 → 01 → 11 → 10 → 00 →...)

PRESENT STATE		**NEXT STATE**	
		x=0	**x=1**
A	B	A B	**A B**
0	0	1 1	**0 1**
0	1	0 0	**1 1**
1	0	0 1	**0 0**
1	1	1 0	**1 0**

Example 3

PRESENT STATE		NEXT STATE	
		x=0	x=1
A	B	A B	**A B**
0	0	1 1	**0 1**
0	1	0 0	**1 1**
1	0	0 1	**0 0**
1	1	1 0	**1 0**





Example 3

PRESENT STATE		NEXT STATE			
		x=0		x=1	
A	B	A	B	A	B
0	0	1	1	0	1
0	1	0	0	1	1
1	0	0	1	0	0
1	1	1	0	1	0

D_A

x \ AB	00	01	11	10
0	1	0	1	0
1	0	1	1	0

$D_A = AB + Bx + A'B'x'$

Example 3

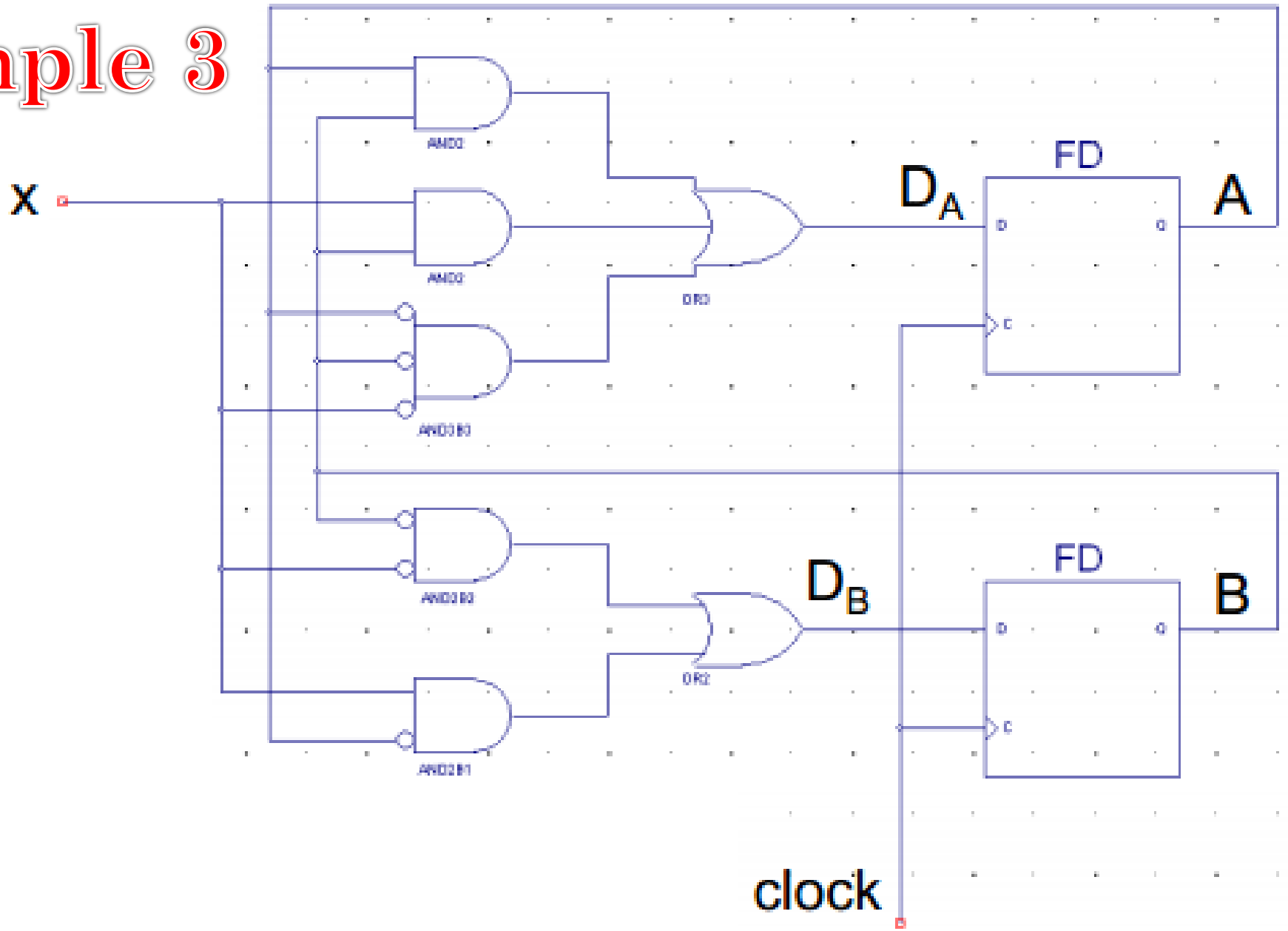
PRESENT STATE		NEXT STATE			
		x=0		x=1	
A	B	A	B	A	B
0	0	1	1	0	1
0	1	0	0	1	1
1	0	0	1	0	0
1	1	1	0	1	0

D_B

x \ AB	00	01	11	10
0	1	0	0	1
1	1	1	0	0

$D_B = B'x' + A'x$

Example 3



Reference