江西理工大学
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Digital System Design

Clip Lecture series

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Jiangxi University of Science and Technology

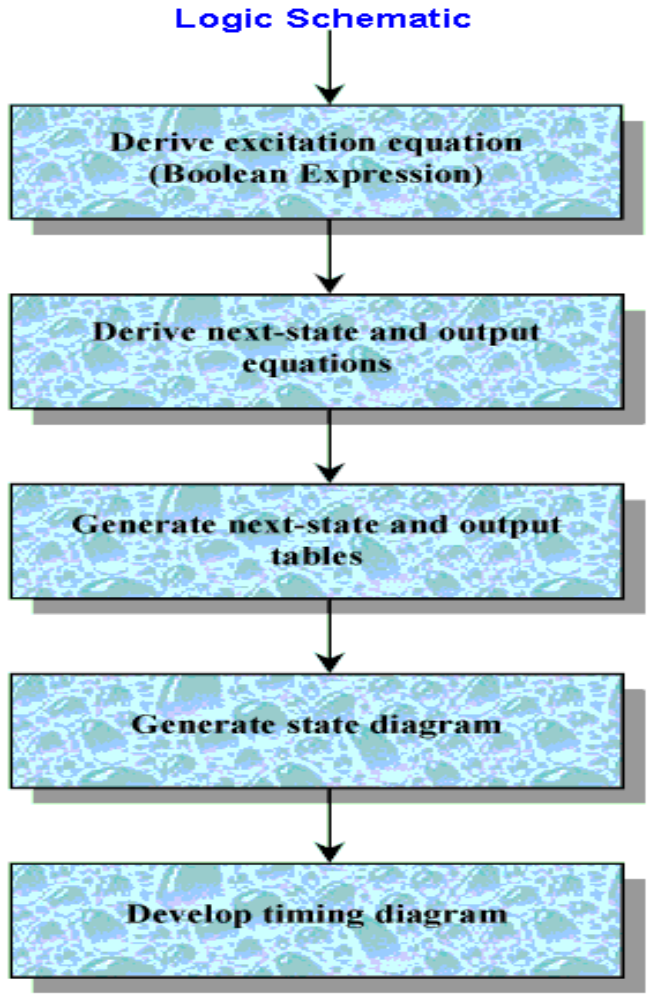
Analysis of Sequential circuits

5 important example

Design of Sequential Circuits

The behavior of a sequential circuit is determined from the inputs, the outputs and the states of its flip-flops.
Both the output and the next state are a function of the inputs and the present state.
The suggested analysis procedure of a sequential circuit is set out in Figure below.

- We start with the logic schematic from which we can derive excitation equations for each flip-flop input.
- Then, to obtain next-state equations, we insert the excitation equations into the characteristic equations.
- The output equations can be derived from the schematic, and once we have our output and next-state equations, we can generate the next-state and output tables as well as state diagrams.
- When we reach this stage, we use either the table or the state diagram to develop a timing diagram which can be verified through simulation.



Design of Sequential Circuits

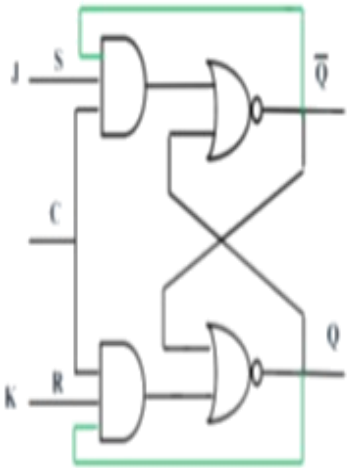
- The main step to design the sequential circuits
  - Analyses and understand the question
  - Extract the state table based on given data
  - Assign a number of required FF
  - Select the type of FF
  - Finding the excitation table base on state table
  - Simplification od input function of FF
  - Design the circuit

Review.....

Table 5.1
Flip-Flop Characteristic Tables

JK Flip-Flop

J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

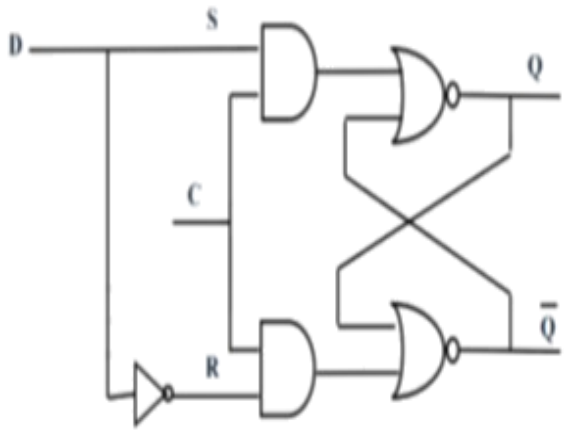


$Q^* = J\bar{Q} + \bar{K}Q$

D Flip-Flop

D	Q(t + 1)	
0	0	Reset
1	1	Set

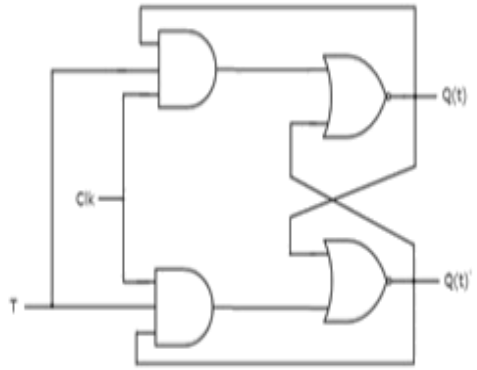
$Q^* = D$



(b) Graphic Symbol

T Flip-Flop

T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement



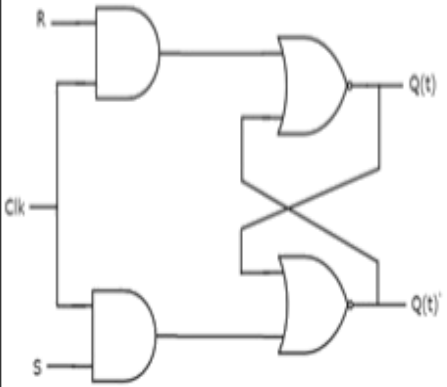
$Q(t+1) = T \oplus Q(t)$

SR FF

S	R	Q*
0	0	Q
0	1	0
1	0	1
1	1	X

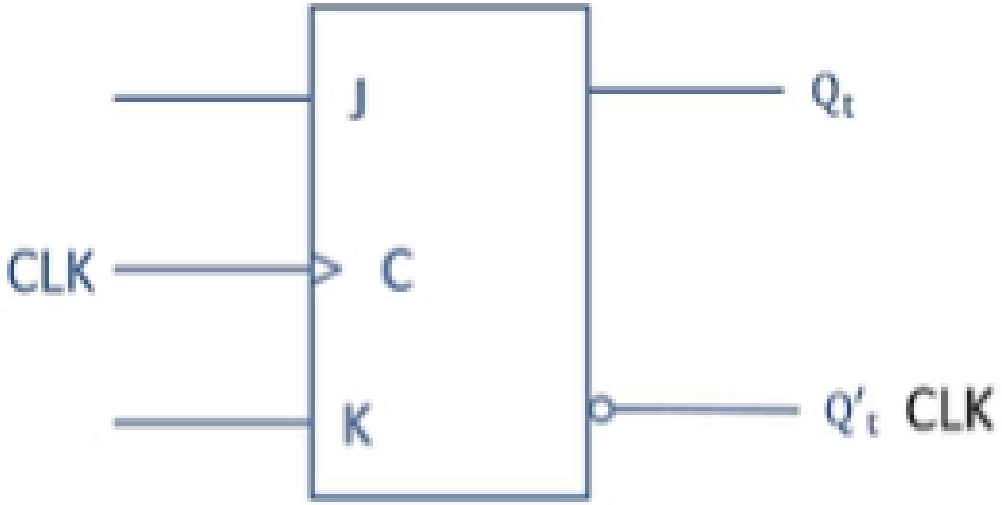
$Q^* = S + \bar{R}.Q$

$S.R = 0$



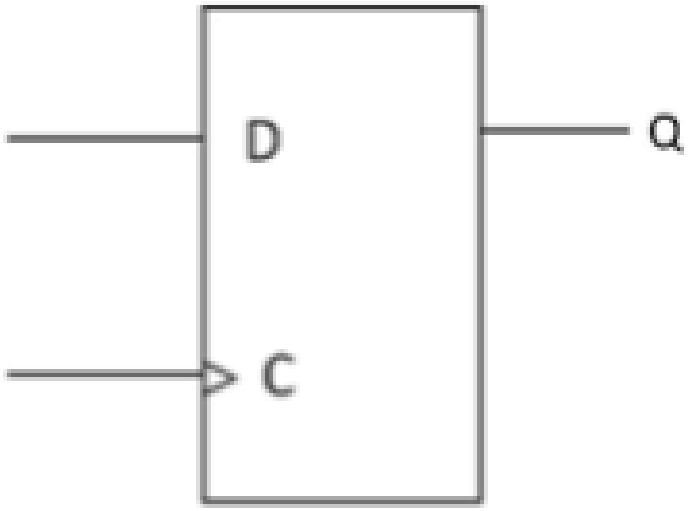
All FF type

JK-FF



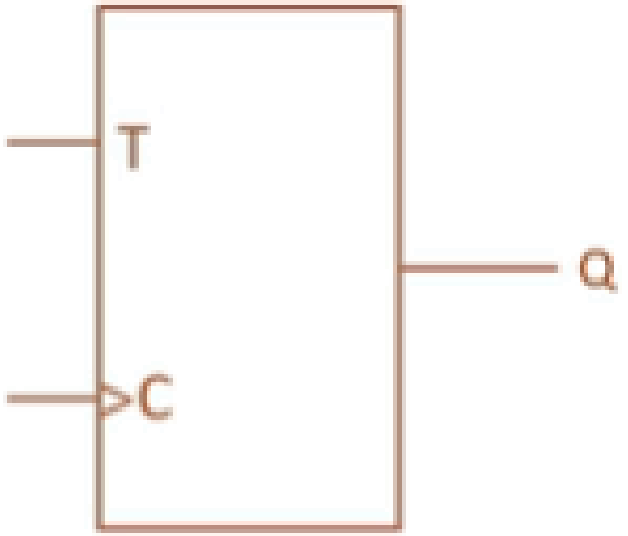
J	K	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	Q'_t

D-FF



D	Q_{t+1}
0	0
1	1

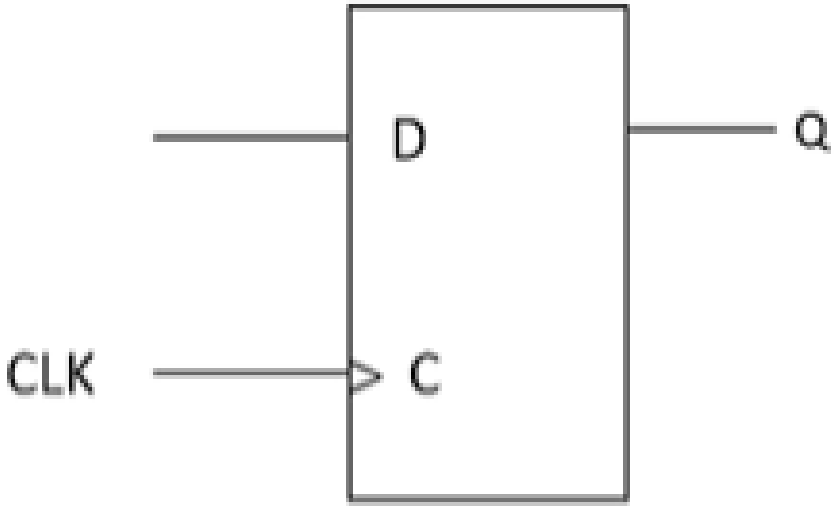
T-FF



T	Q_{t+1}
0	Q_t
1	Q'_t

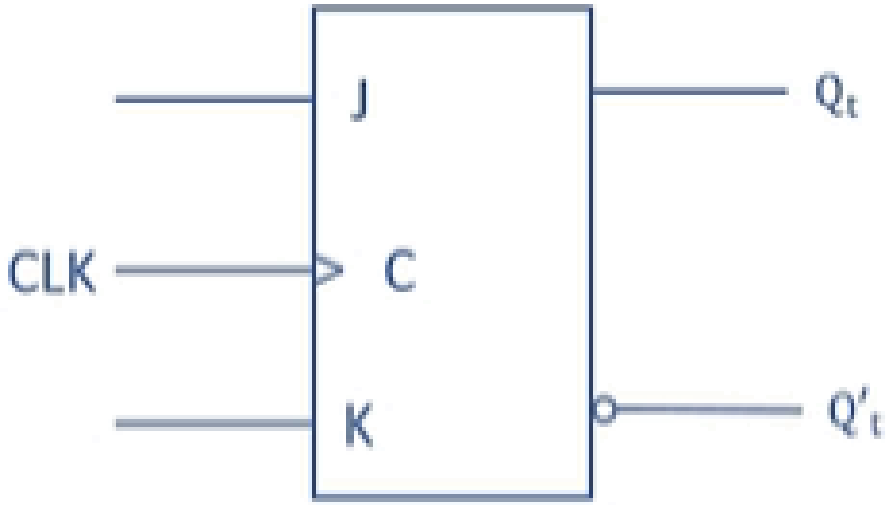
All FF type

D-FF



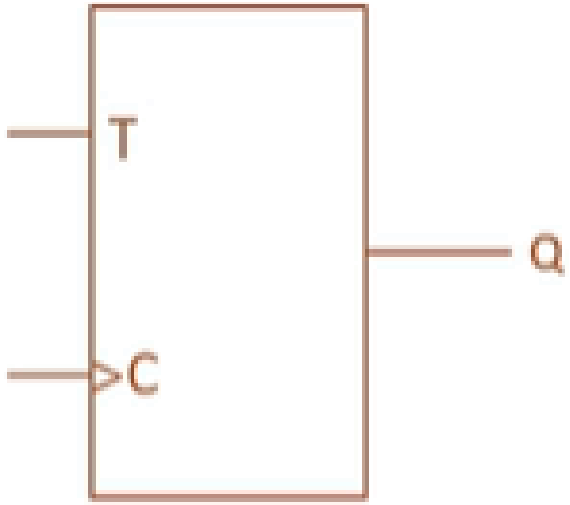
D	Q_{t+1}
0	0
1	1

JK-FF



J	K	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	Q'_t

T-FF



T	Q_{t+1}
0	Q_t
1	Q'_t

JK-FF

CHARACTERISTIC TABLE

J	K	Q_{t+1}
0	0	$Q_t = 0$
0	1	0
1	0	1
1	1	$Q'_t = 1$

CHARACTERISTIC EQUATION

Q(next) = JQ' + K'Q

EXCITATION TABLE

Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

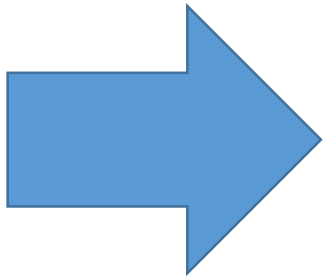
Example 1

Design a sequential circuit which work based on below table with JK FF

Current state		Input	Next state	
A	B	X	A	B
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	1	1	1
1	1	0	0	0

Example 1

Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



Current state		Input	Next state		FF A Input	
A	B	X	A	B	J_A	K_A
0	0	0	0	0	0	X
0	0	1	0	1		
0	1	0	1	0		
0	1	1	0	1		
1	0	0	1	0		
1	0	1	1	1		
1	1	1	1	1		
1	1	0	0	0		

Example 1

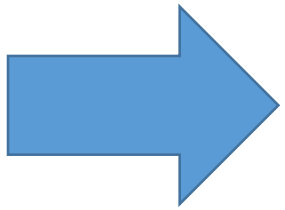
Now You
TRY To Solve

Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Current state		Input	Next state		FF A Input	
A	B	X	A	B	J_A	K_A
0	0	0	0	0	0	X
0	0	1	0	1		
0	1	0	1	0		
0	1	1	0	1		
1	0	0	1	0		
1	0	1	1	1		
1	1	1	1	1		
1	1	0	0	0		

Example 1

Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



Current state		Input	Next state		FF A Input		FF B Input	
A	B	X	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0				
0	0	1	0	1				
0	1	0	1	0				
0	1	1	0	1				
1	0	0	1	0				
1	0	1	1	1				
1	1	1	1	1				
1	1	0	0	0				

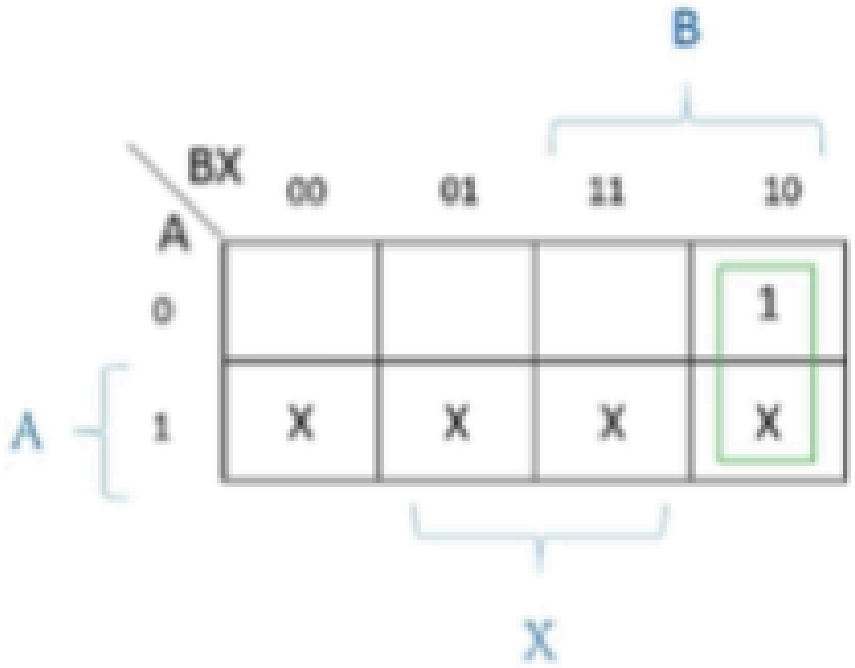
Example 1

Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Current state		Input	Next state		FF A Input		FF B Input	
A	B	X	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	1	1	1	X	0	X	0
1	1	0	0	0	X	1	X	1

State table

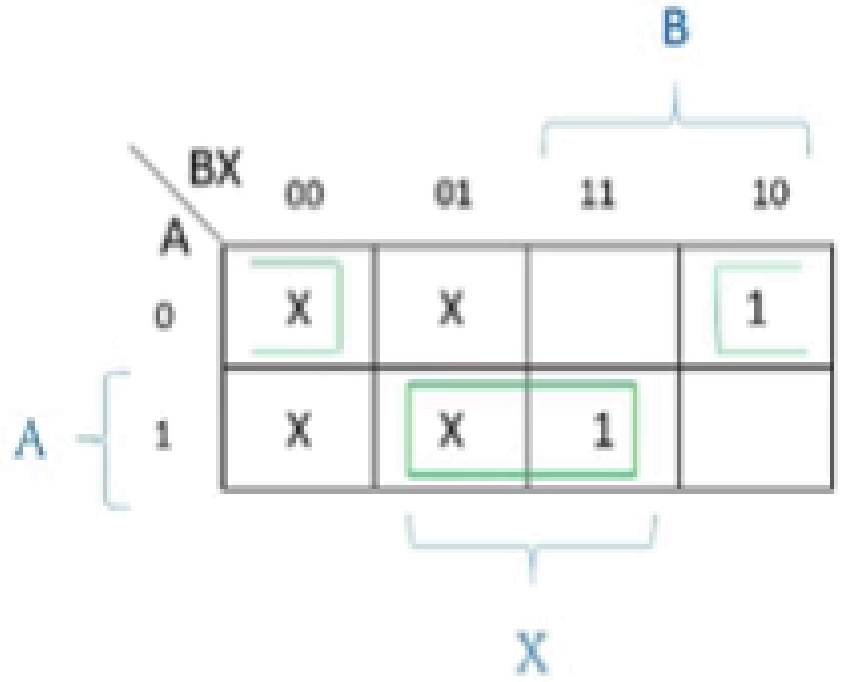
FF A Input		FF B Input	
J_A	K_A	J_B	K_B
0	X	0	X
0	X	1	X
1	X	X	1
0	X	X	0
X	0	0	X
X	0	1	X
X	0	X	0
X	1	X	1



A	B	X	
0	1	0	1
1	0	0	X
1	0	1	X
1	1	1	X
1	1	0	X

$$J_A = B X'$$

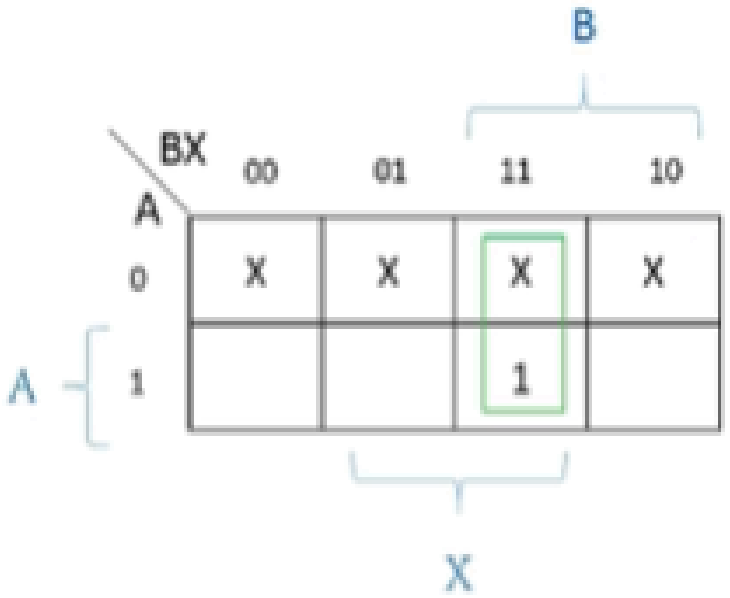
FF A Input		FF B Input	
J_A	K_A	J_B	K_B
0	X	0	X
0	X	1	X
1	X	X	1
0	X	X	0
X	0	0	X
X	0	1	X
X	0	X	0
X	1	X	1



A	B	X	
0	0	0	X
0	0	1	X
0	1	0	1
1	0	0	1
1	0	1	X
1	1	1	1

$$K_{B=} A X + A' X'$$

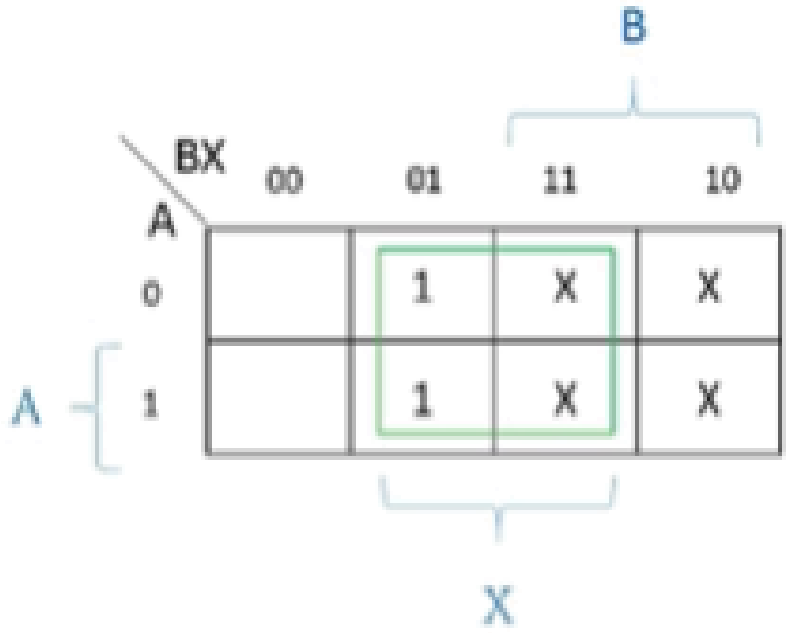
FF A Input		FF B Input	
J_A	K_A	J_B	K_B
0	X	0	X
0	X	1	X
1	X	X	1
0	X	X	0
X	0	0	X
X	0	1	X
X	0	X	0
X	1	X	1



$$K_A = B\,X$$

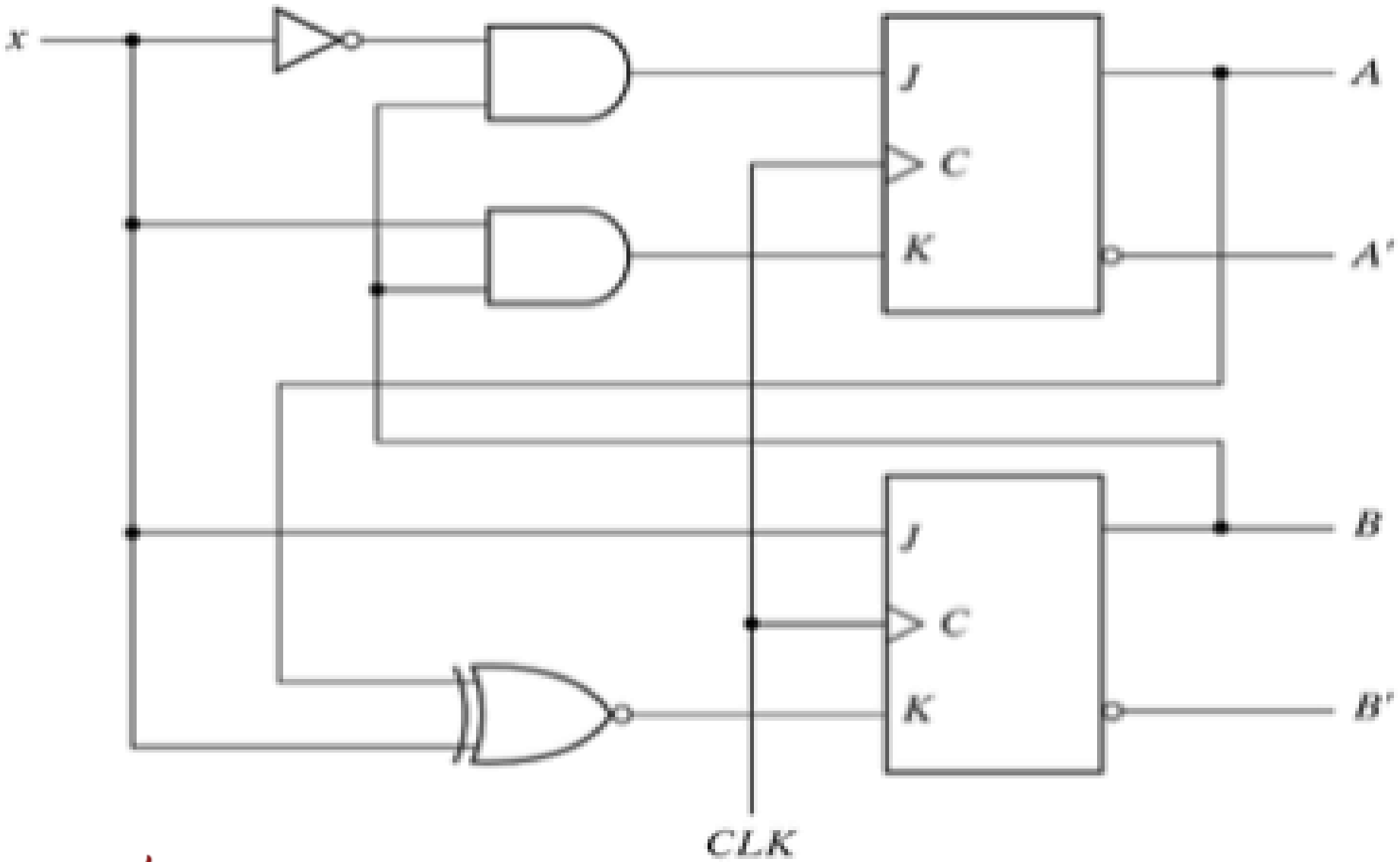
A	B	X	
0	0	0	X
0	0	1	X
0	1	1	X
0	1	0	X
1	1	1	1

FF A Input		FF B Input	
J_A	K_A	J_B	K_B
0	X	0	X
0	X	1	X
1	X	X	1
0	X	X	0
X	0	0	X
X	0	1	X
X	0	X	0
X	1	X	1

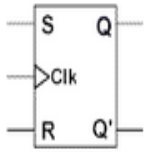
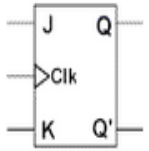
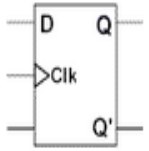
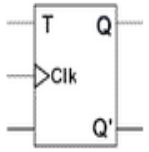


$$J_B = X$$

A	B	X	
0	0	1	1
0	1	1	X
0	1	0	X
1	1	0	X
1	0	1	X
1	1	1	X


X
J
C
K
A
A'
J
C
K
B
B'
CLK

Flip-flop Types

FLIP-FLOP NAME	FLIP-FLOP SYMBOL	CHARACTERISTIC TABLE	CHARACTERISTIC EQUATION	EXCITATION TABLE
SR		S R Q(next): 0 0 Q; 0 1 0; 1 0 1; 1 1 ?	$Q_{(next)} = S + R'Q$ $SR = 0$	Q Q(next) S R: 0 0 0 X; 0 1 1 0; 1 0 0 1; 1 1 X 0
JK		J K Q(next): 0 0 Q; 0 1 0; 1 0 1; 1 1 Q'	$Q_{(next)} = JQ' + K'Q$	Q Q(next) J K: 0 0 0 X; 0 1 1 X; 1 0 X 1; 1 1 X 0
D		D Q(next): 0 0; 1 1	$Q_{(next)} = D$	Q Q(next) D: 0 0 0; 0 1 1; 1 0 0; 1 1 1
T		T Q(next): 0 Q; 1 Q'	$Q_{(next)} = TQ' + T'Q$	Q Q(next) T: 0 0 0; 0 1 1; 1 0 1; 1 1 0

Example2

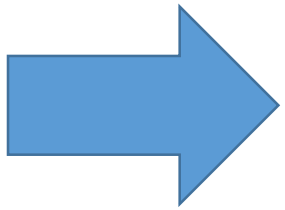
Design a sequential circuit
with the JK FF
which work based on below table

Current state		Input	Next state	
A	B	X	A	B
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

Example2(design)

Based on JK FF the excitation table will be like below

Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

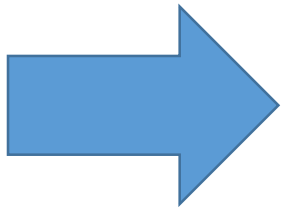


The ckt input			Next state		The ckt o/p			
Current state		Input			FF input			
A	*B*	*x*	*A*	*B*	*JA*	*KA*	*JB*	*KB*
0	0	0	0	0				
0	0	1	0	1				
0	1	0	1	0				
0	1	1	0	1				
1	0	0	1	0				
1	0	1	1	1				
1	1	0	1	1				
1	1	1	0	0				

Example2(design)

Based on JK FF the excitation table will be like below

Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

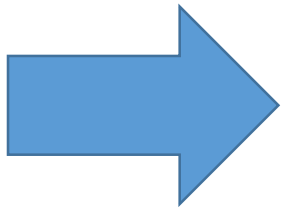


The ckt input			Next state		The ckt o/p			
Current state		Input			FF input			
A	*B*	*x*	*A*	*B*	*JA*	*KA*	*JB*	*KB*
0	0	0	0	0	0	X	0	X
0	0	1	0	1				
0	1	0	1	0				
0	1	1	0	1				
1	0	0	1	0				
1	0	1	1	1				
1	1	0	1	1				
1	1	1	0	0				

Example2(design)

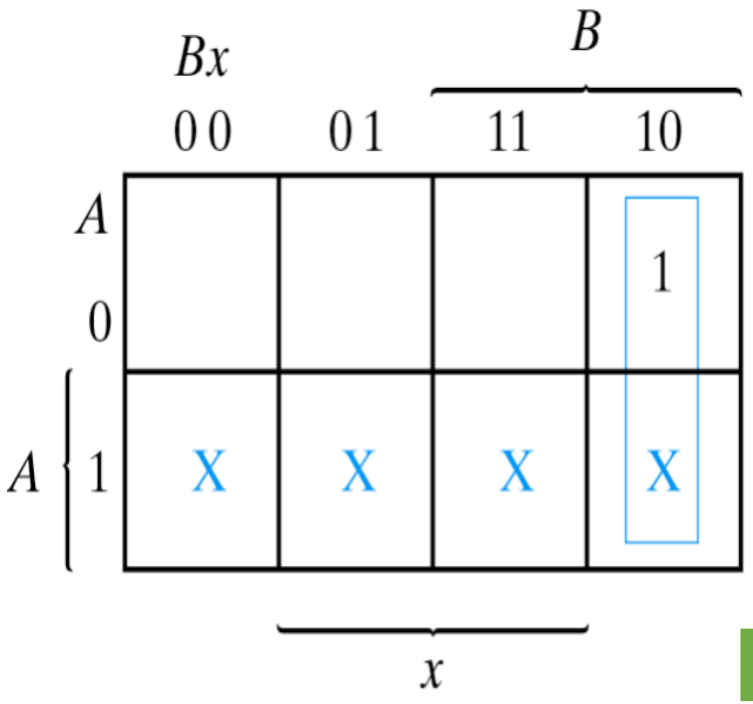
Based on JK FF the excitation table will be like below

Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



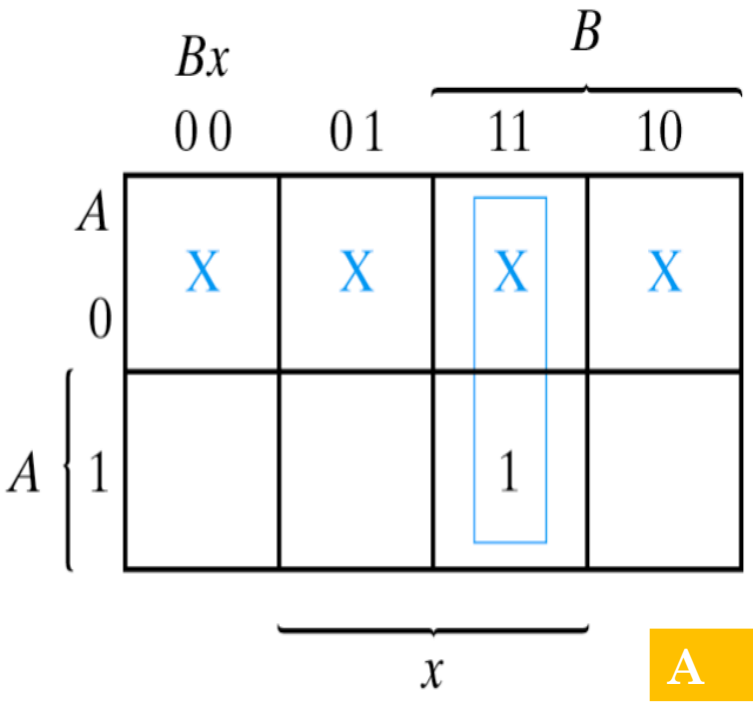
The ckt input			Next state		The ckt o/p			
Current state		Input			FF input			
A	*B*	*x*	*A*	*B*	*JA*	*KA*	*JB*	*KB*
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

K map for FF



$$J_A = Bx'$$

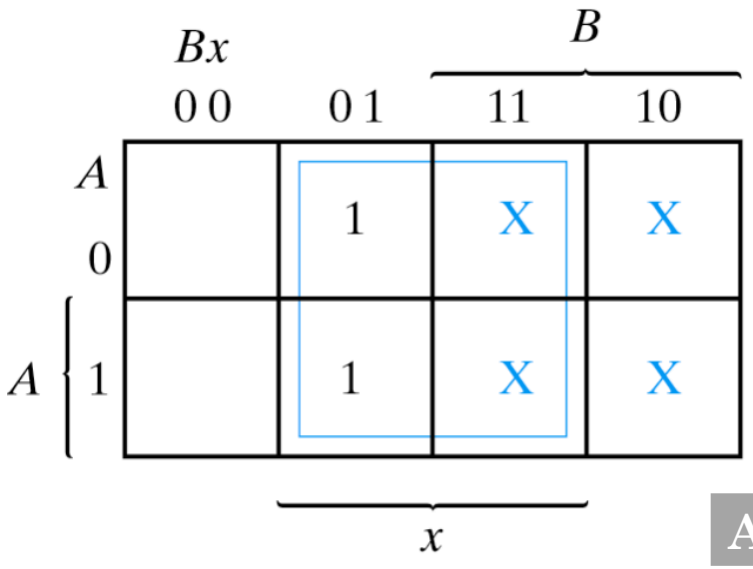
A	B	X	
0	1	0	1
1	0	0	X
1	0	1	X
1	1	1	X
1	1	0	X



$$K_A = Bx$$

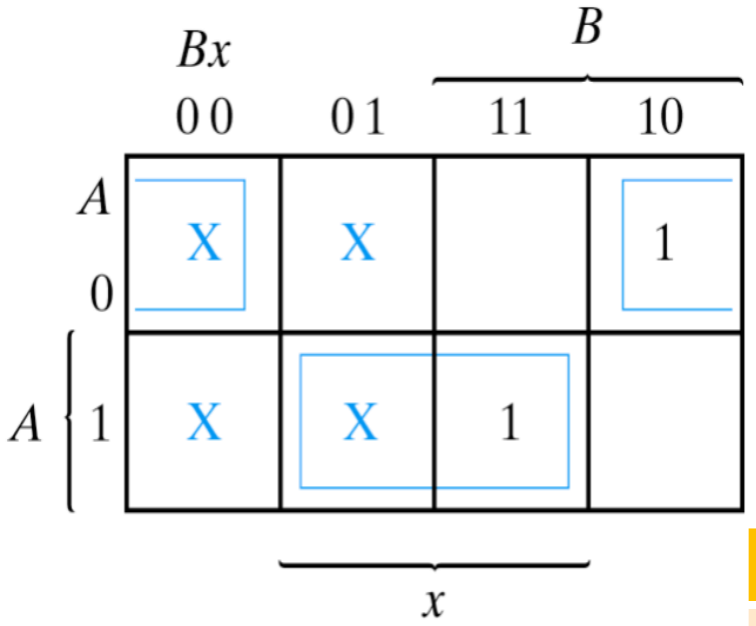
A	B	X	
0	0	0	X
0	0	1	X
0	1	1	X
0	1	0	X
1	1	1	1

K map for FF



$$J_B = x$$

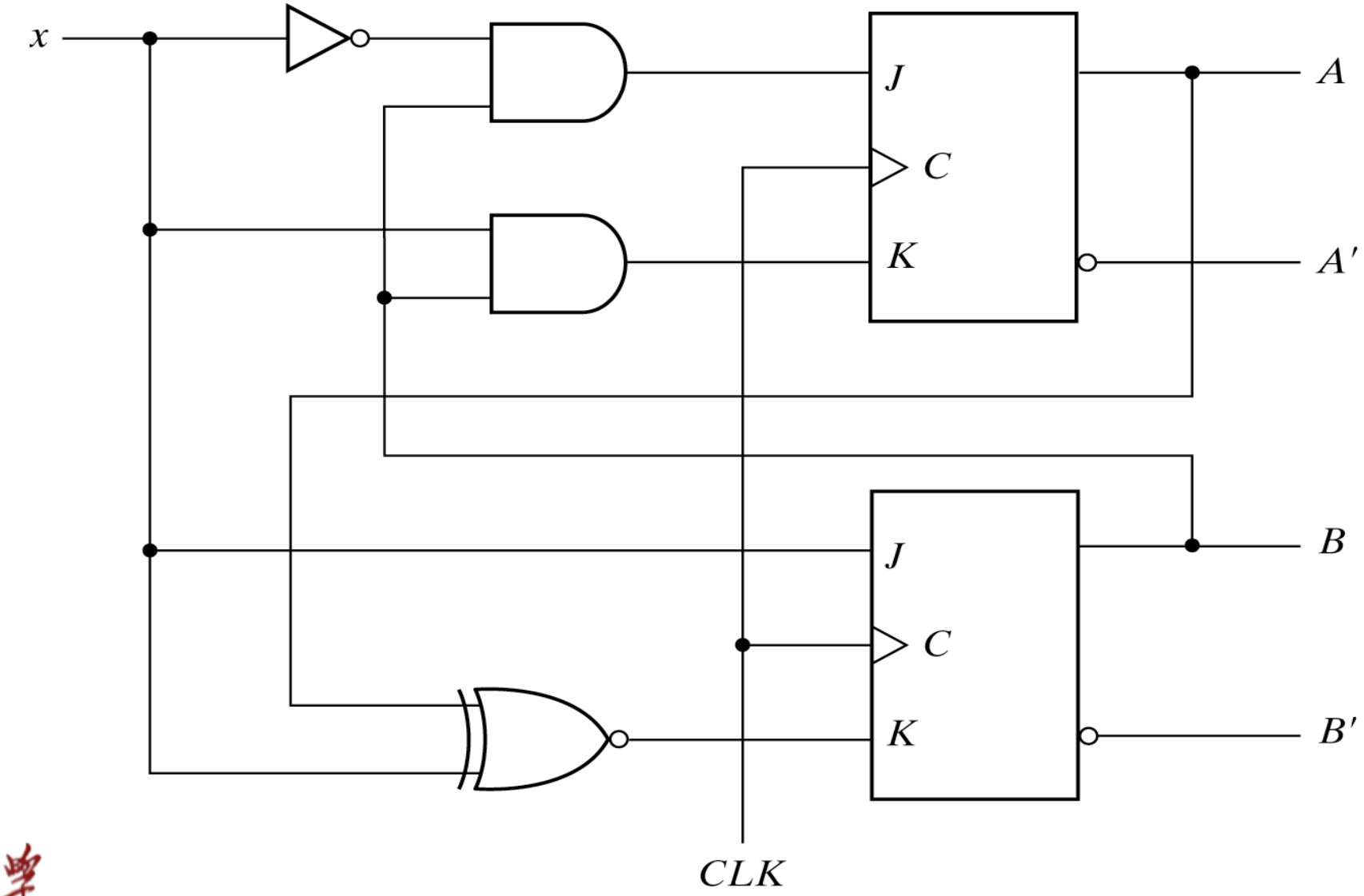
A	B	X	
0	0	1	1
0	1	1	X
0	1	0	X
1	0	1	1
1	1	1	X
1	1	0	X



$$K_B = (A \oplus x)'$$

A	B	X	
0	0	0	X
0	0	1	X
0	1	0	1
1	0	0	X
1	0	1	X
1	1	1	1

Design Circuit

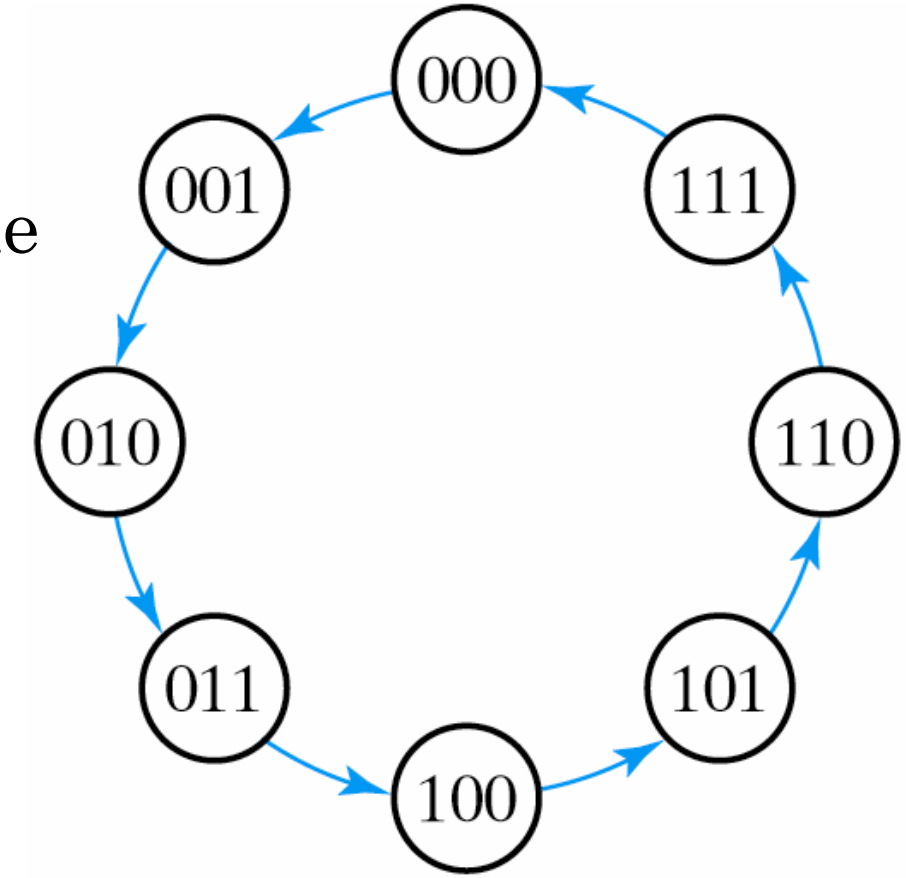


Example 3

- Design a 3 bit counter with the T flip flop ,which start from 000 to 111

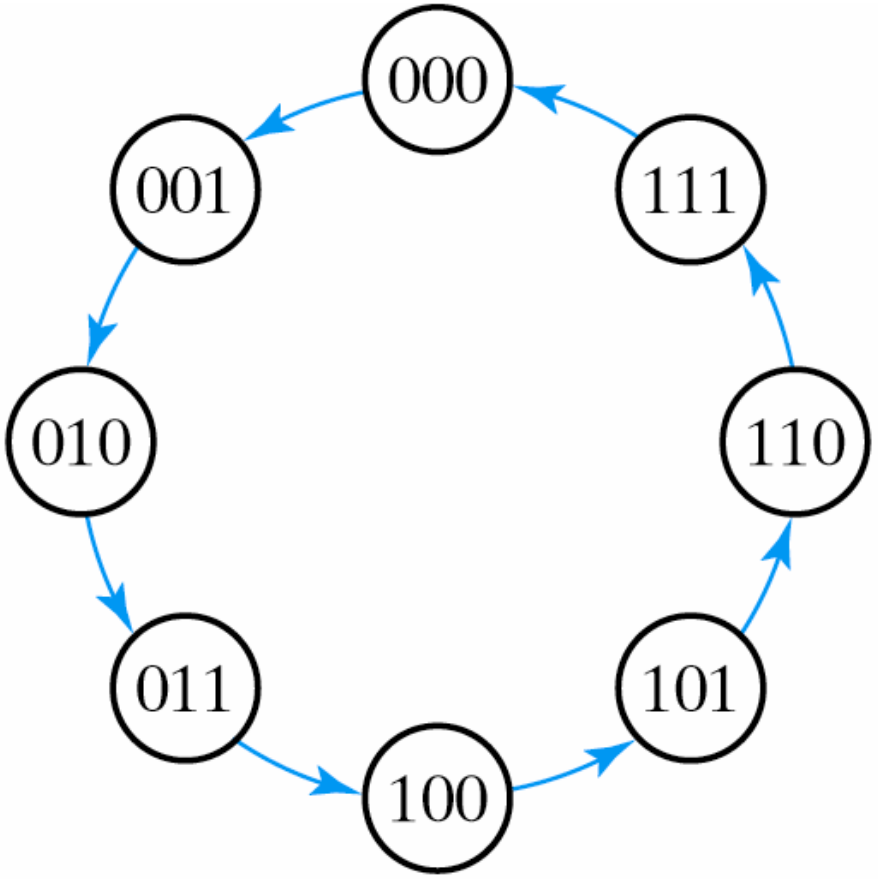
More Example:

Binary Counter – show state diagram and table



Example 3

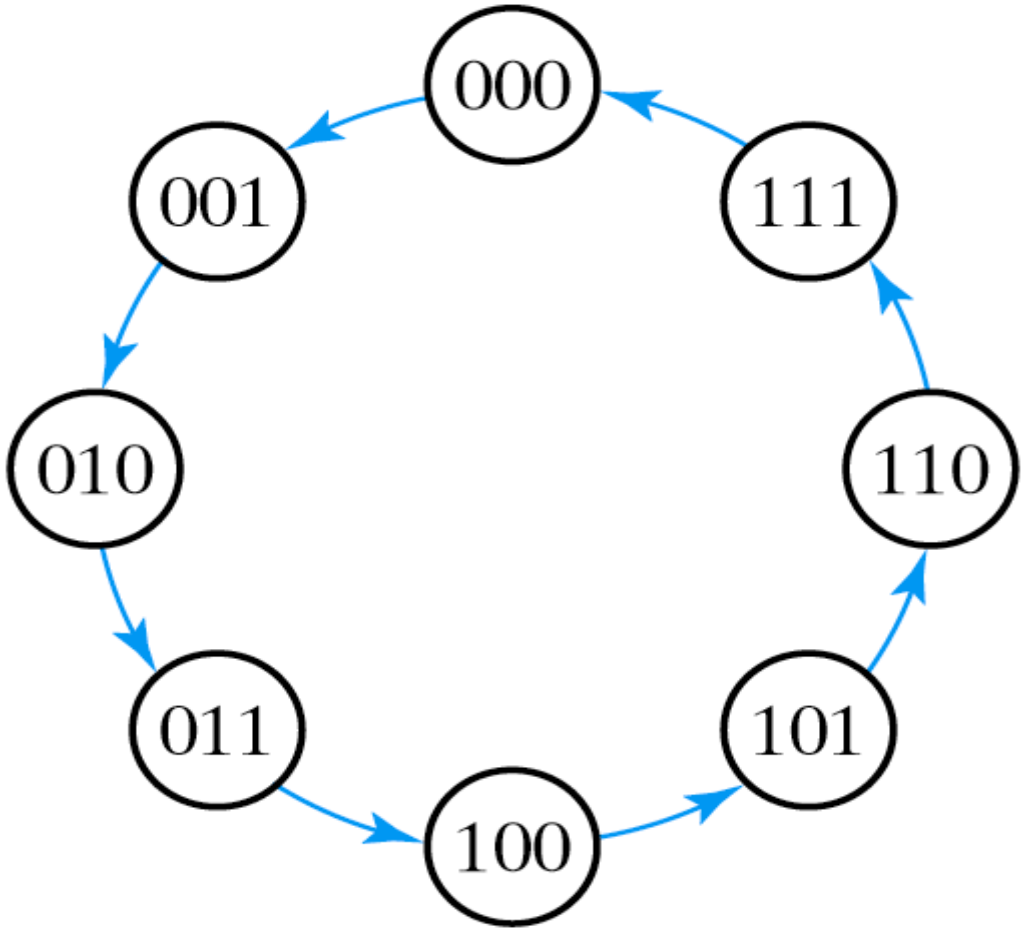
- The excitation circuit



Current state			Next state			FF inputs		
A_2	A_1	A_0	A_2	A_1	A_0	TA_2	TA_1	TA_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0			
0	1	0	0	1	1			
0	1	1	1	0	0			
1	0	0	1	0	1			
1	0	1	1	1	0			
1	1	0	1	1	1			
1	1	1	0	0	0			

Example 3

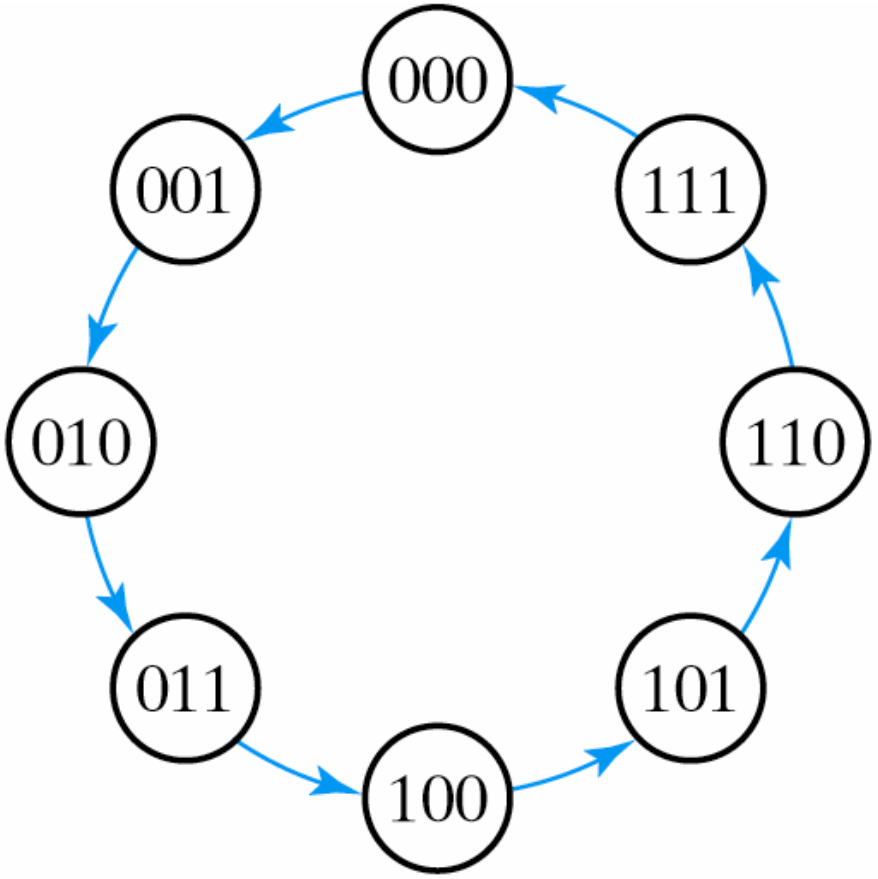
- The excitation circuit



Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

Example 3

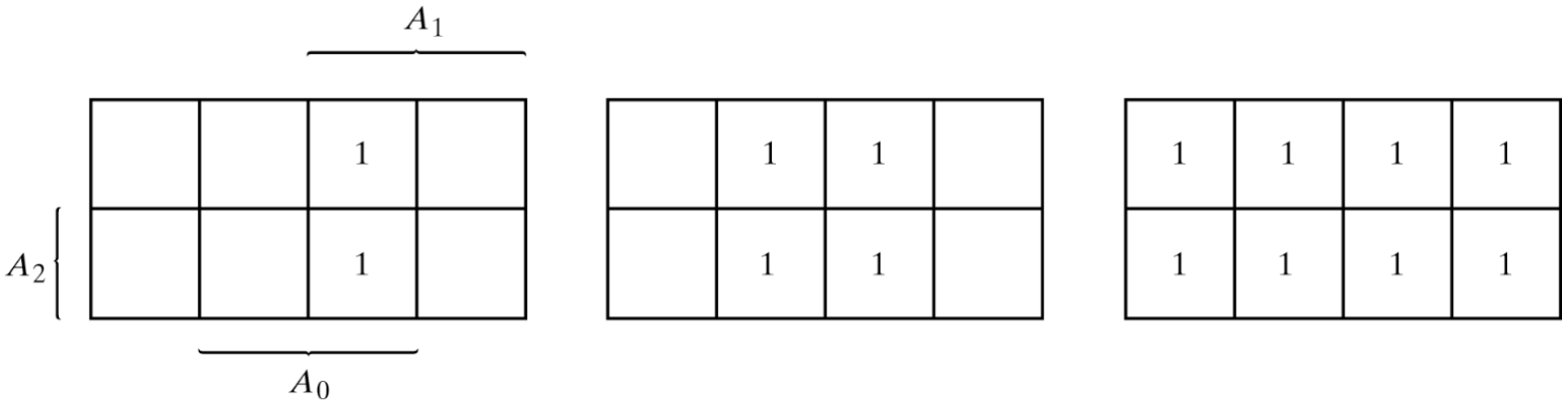
- The excitation circuit



Current state			Next state			FF inputs		
A_2	A_1	A_0	A_2	A_1	A_0	TA_2	TA_1	TA_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0			
0	1	0	0	1	1			
0	1	1	1	0	0			
1	0	0	1	0	1			
1	0	1	1	1	0			
1	1	0	1	1	1			
1	1	1	0	0	0			

Example 3

- K map



$T_{A2} = A_1 A_0$

A2	A1	A3	TA2
0	1	1	1
1	1	1	1

$T_{A1} = A_0$

A2	A1	A3	TA1
0	0	1	1
0	1	1	1
1	0	1	1
1	1	1	1

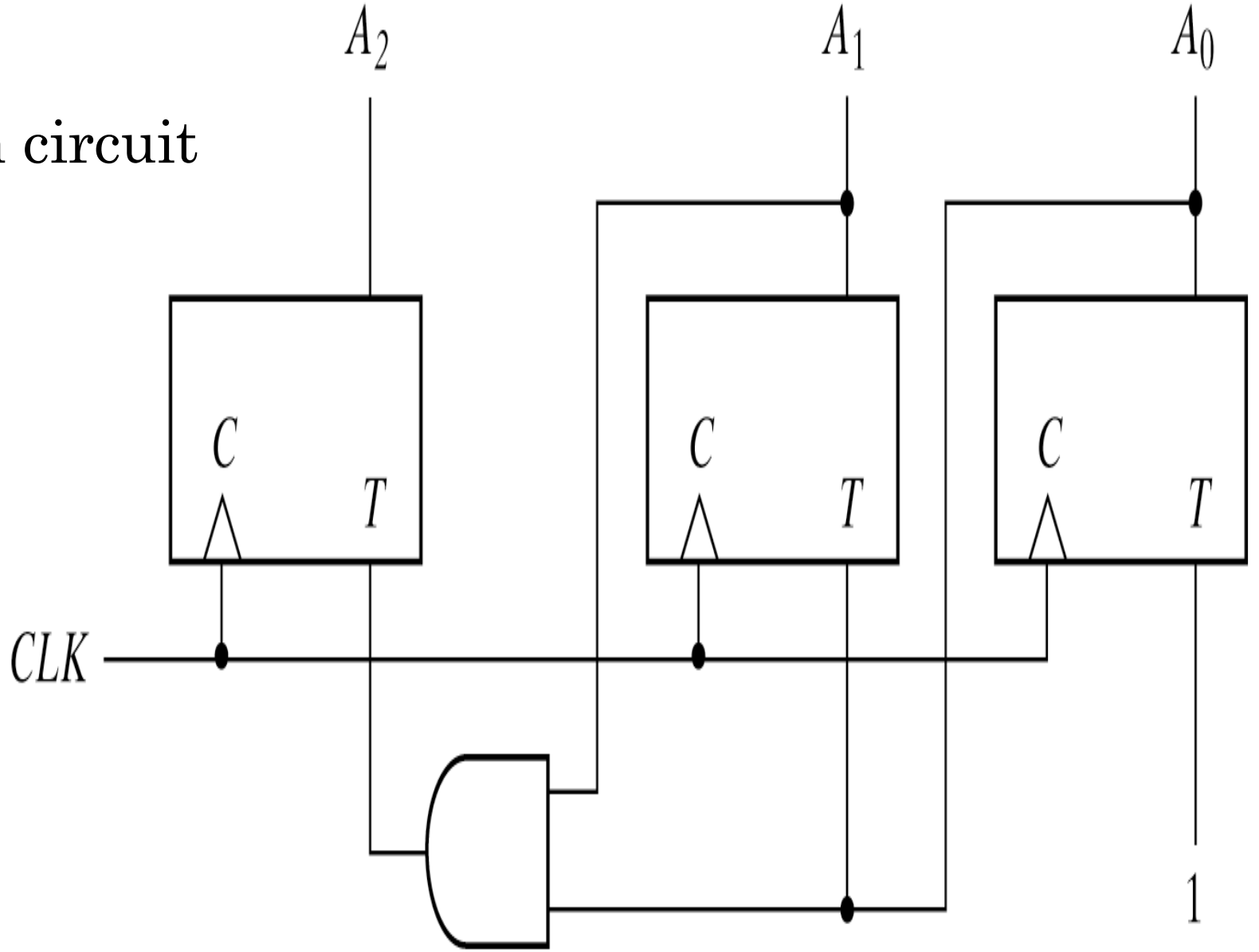
$T_{A0} = 1$

- The design circuit

Current state			Next state			FF inputs		
A_2	A_1	A_0	A_2	A_1	A_0	TA_2	TA_1	TA_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

Example 3

- The design circuit



3 bit counter with JK

Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Bit 0

Bit 1

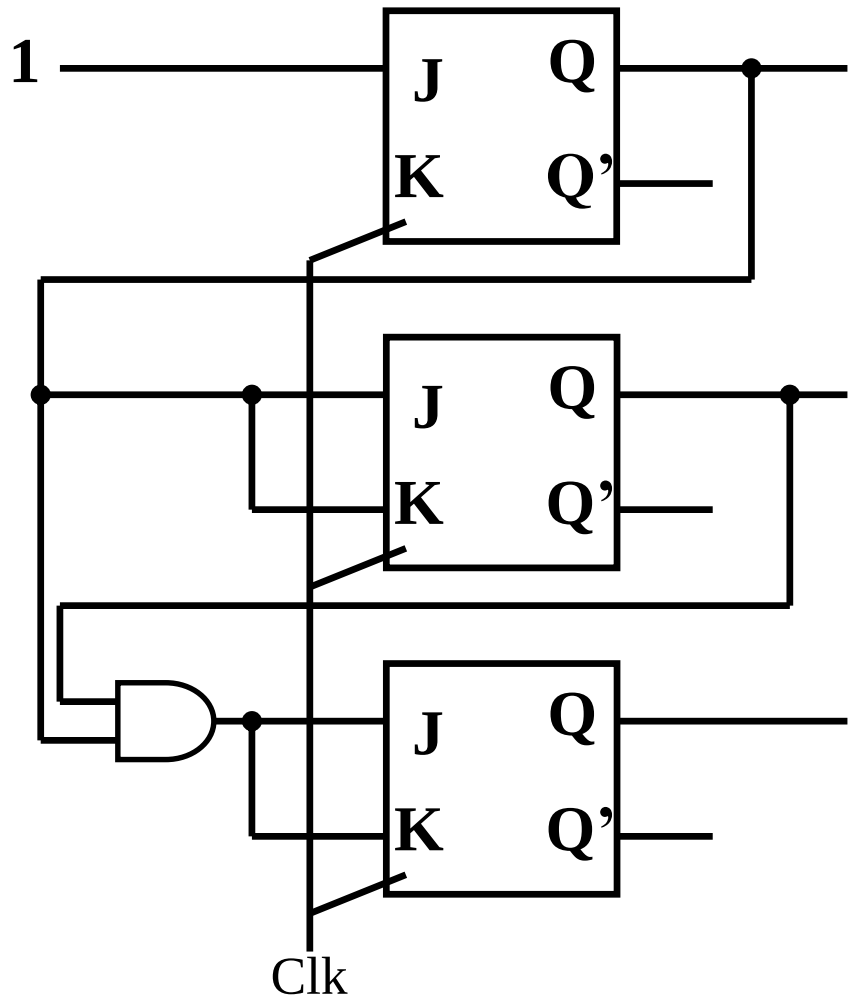
Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

3 bit counter

Solve and make the K map and check your design

Bit 2

Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1



FF- The excitation table

Q(t)	Q(t+1)	D	T	R	S	J	K
0	0	0	0	X	0	0	X
0	1	1	1	0	1	1	X
1	0	0	1	1	0	X	1
1	1	1	0	0	X	X	0

Most Important Table

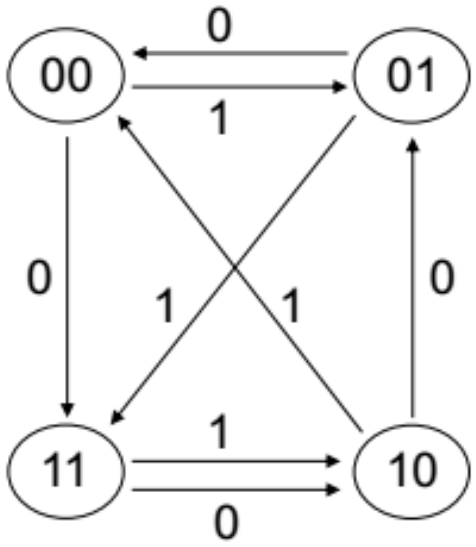
Example 4

Solve and make the K map and check your design

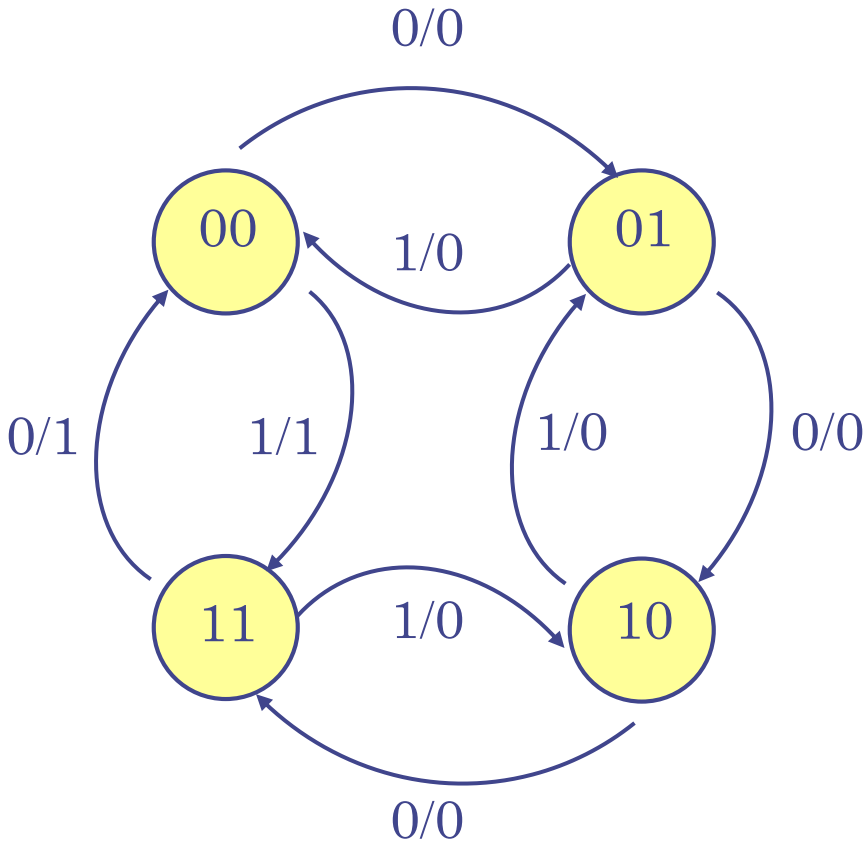
- Design a 2 bit counter which count with the 0 input up counter and 1 Down counter (Use JK ff)

- With the 0 input :00 → 01 → 10 → 11 → 00 → 01 → …
- With the 1 input : 00 → 11 → 10 → 01 → 00 → 11 → …

Example 4: State Diagram



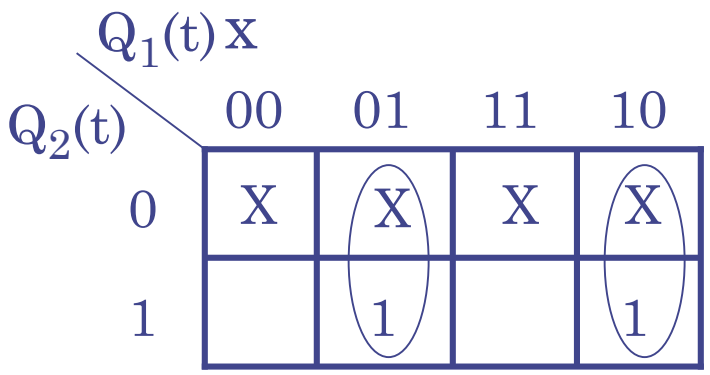
present state	next state x=0	next state x=1
A B	A B	A B
0 0	1 1	0 1
0 1	0 0	1 1
1 0	0 1	0 0
1 1	1 0	1 0



Example 4: The state table

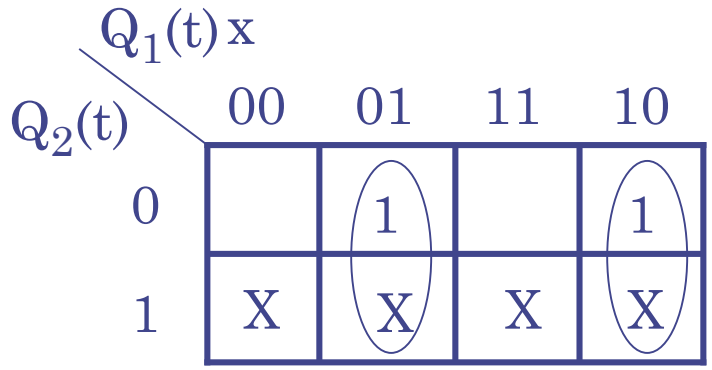
$Q_2(t)$	$Q_1(t)$	x	$Q_2(t+1)$	$Q_1(t+1)$	J_2	K_2	J_1	K_1	Z
0	0	0	0	1	0	X	1	X	0
0	0	1	1	1	1	X	1	X	1
0	1	0	1	0	1	X	X	1	0
0	1	1	0	0	0	X	X	1	0
1	0	0	1	1	X	0	1	X	0
1	0	1	0	1	X	1	1	X	0
1	1	0	0	0	X	1	X	1	1
1	1	1	1	0	X	0	X	1	0

Example 4: k_map



$$K_2 = Q_1(t) \oplus x$$

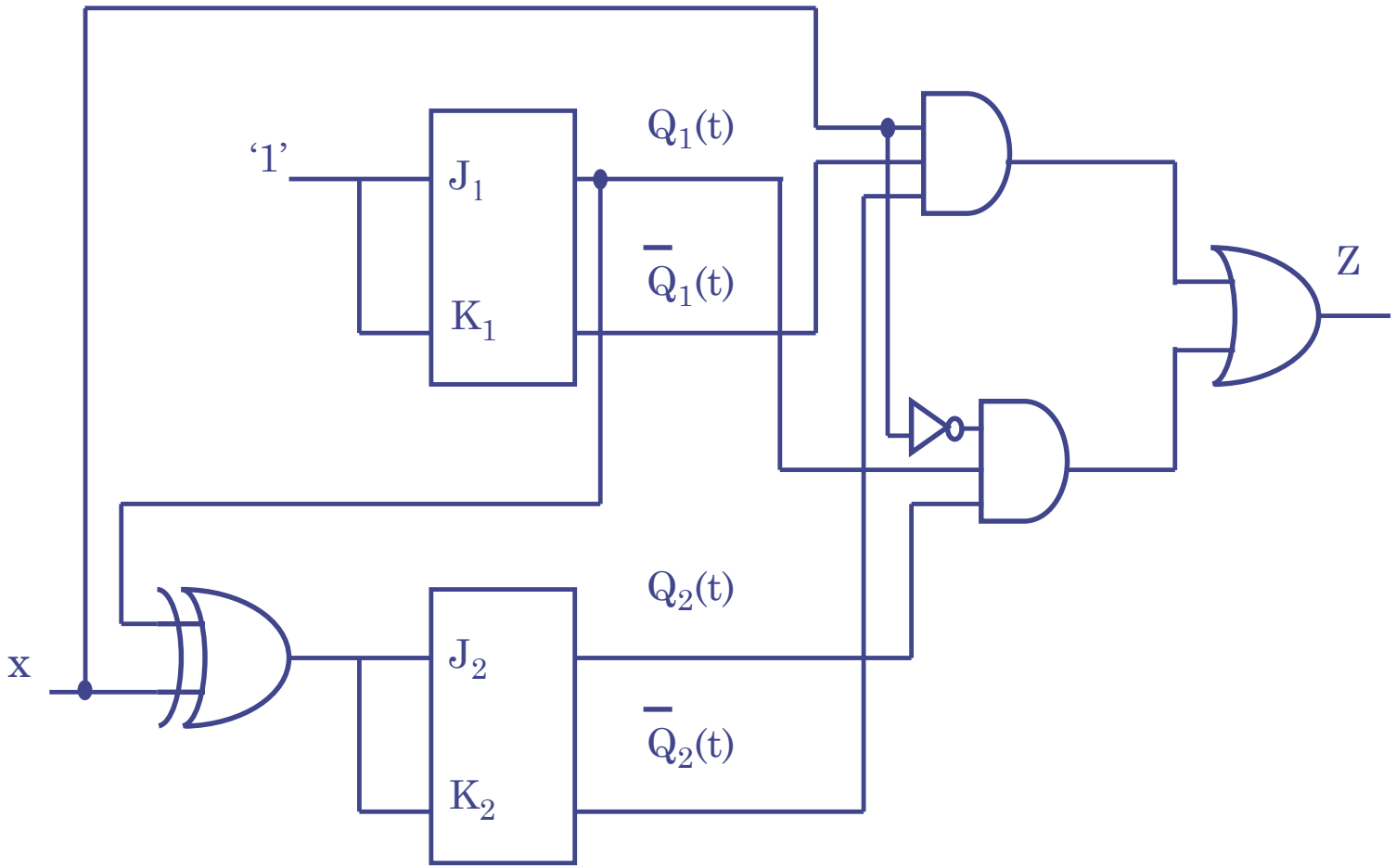
Q2	Q1	X	K2
0	0	0	X
0	0	1	X
0	1	1	X
0	1	0	X
1	0	1	1
1	1	0	1



$$J_2 = Q_1(t) \oplus x$$

Q2	Q1	X	K2
0	0	1	1
0	1	0	1
1	0	0	X
1	0	1	X
1	1	1	X
1	1	0	X

Example 4: Design



Design with D type FF

present state	next state x=0	next state x=1
A B	A B	A B
0 0	1 1	0 1
0 1	0 0	1 1
1 0	0 1	0 0
1 1	1 0	1 0

Solve and make the K map and check your design

D_A

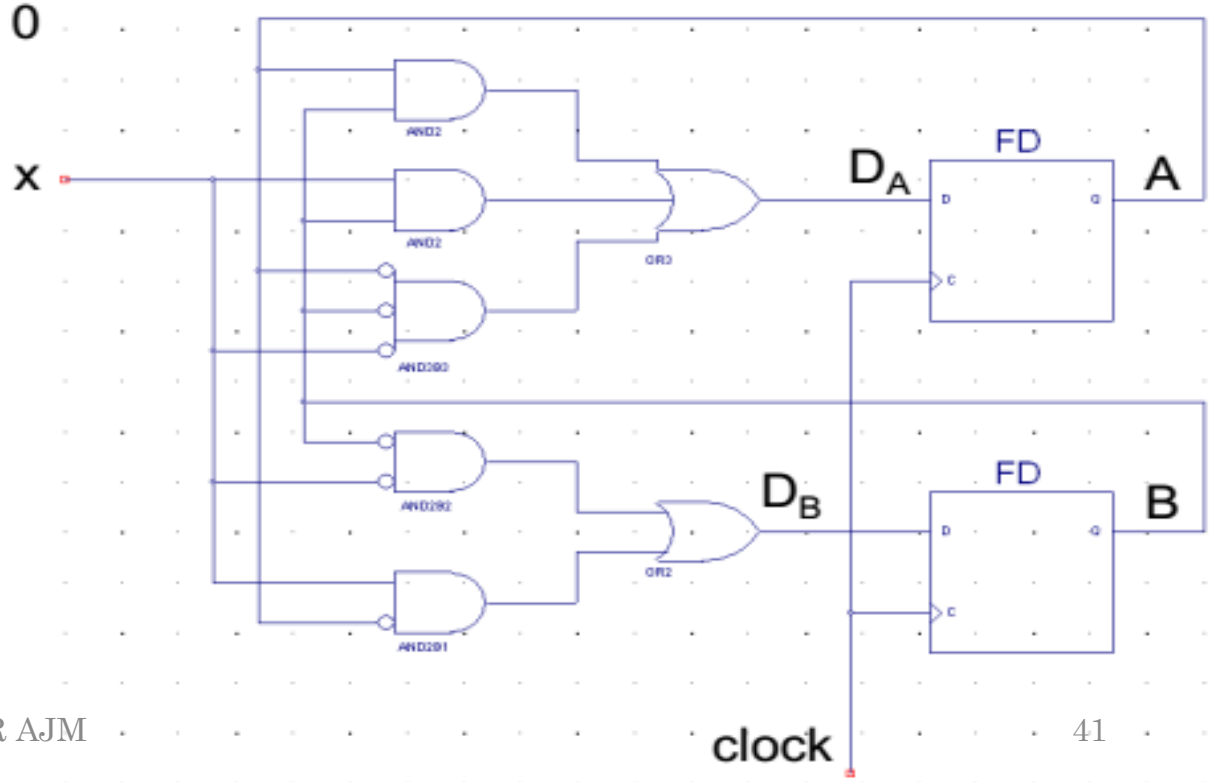
x \ AB	00	01	11	10
0	1	0	1	0
1	0	1	1	0

$D_A = AB + Bx + A'B'x'$

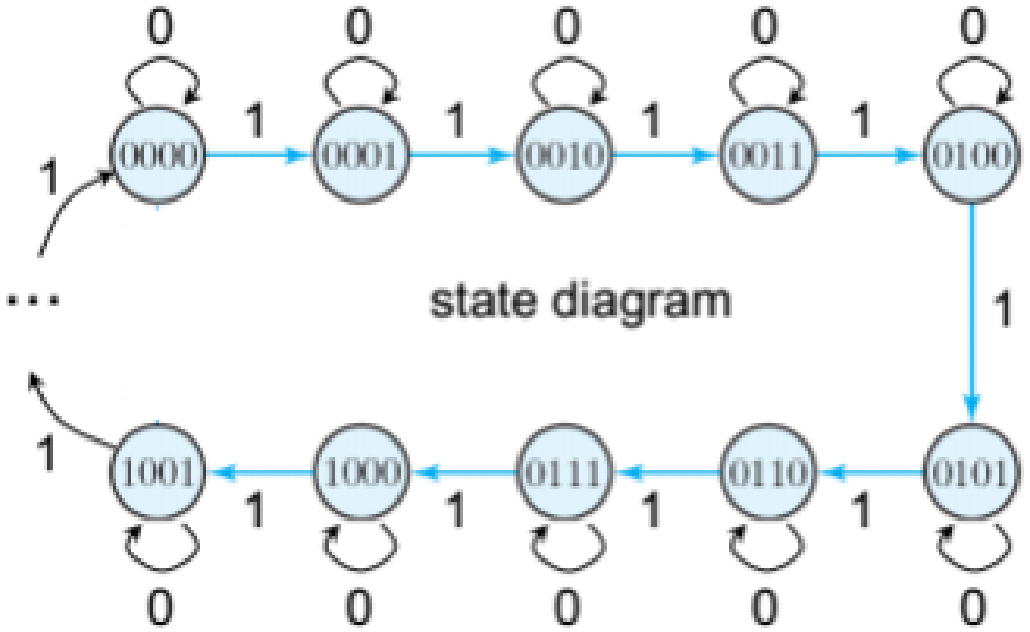
D_B

x \ AB	00	01	11	10
0	1	0	0	1
1	1	1	0	0

$D_B = B'x' + A'x$



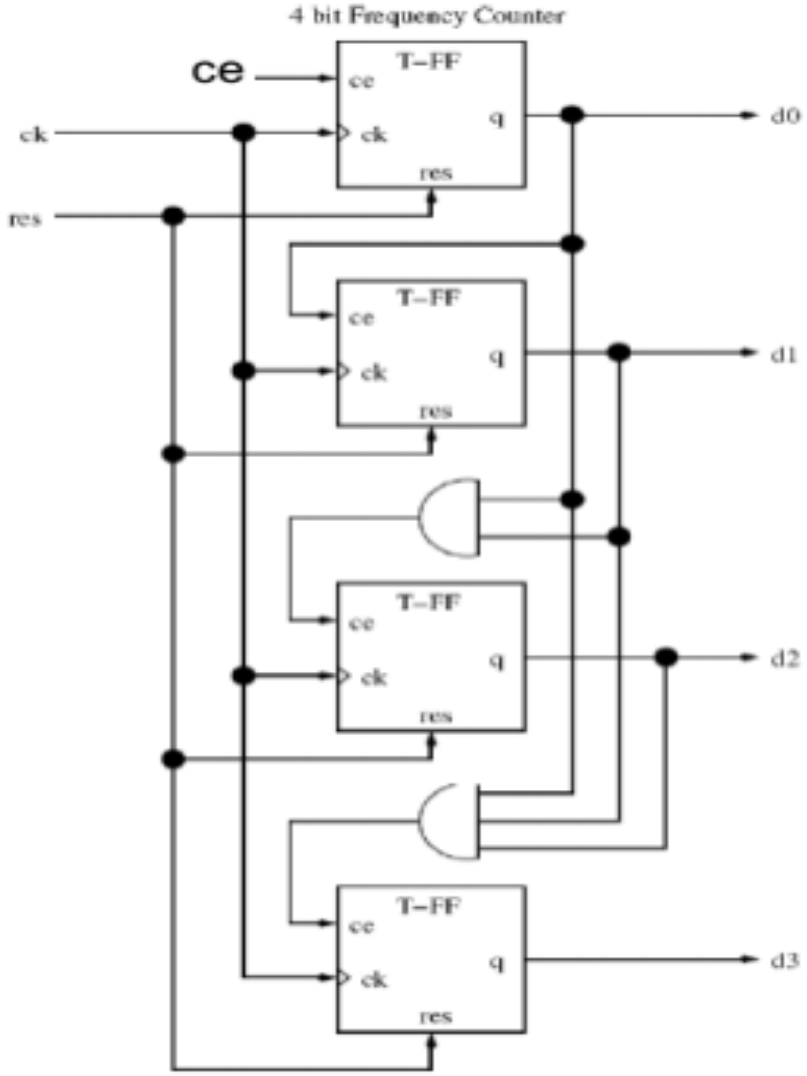
Example 5: Binary Counter



… → 1110 → 1111 → 0000 → 0001 → 0010 → 0011 → 0100 → 0101 → …

Solve and make the K map and check your design

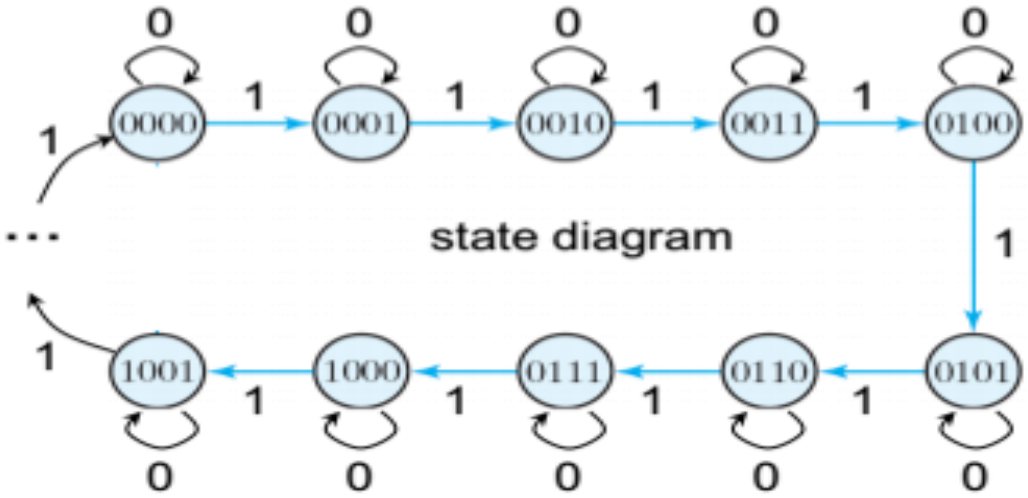
Example 5: Binary Counter



… → 1110 → 1111 → 0000 → 0001 →
0010 → 0011 → 0100 → 0101 → …

present state		next state ce=0	next state ce=1
16 states	0000	0000	0001
	0001	0001	0010
	0010	0010	0011
	…	…	…
	1101	1101	1110
	1110	1110	1111
	1111	1111	0000

→ state table



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