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Digital System Design

Clip Lecture series

Spring_2020

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Sequential circuits

Counters

Counters

Counter is a sequential circuit. A digital circuit which is used for a counting pulses is known counter. Counter is the widest application of flip-flops.

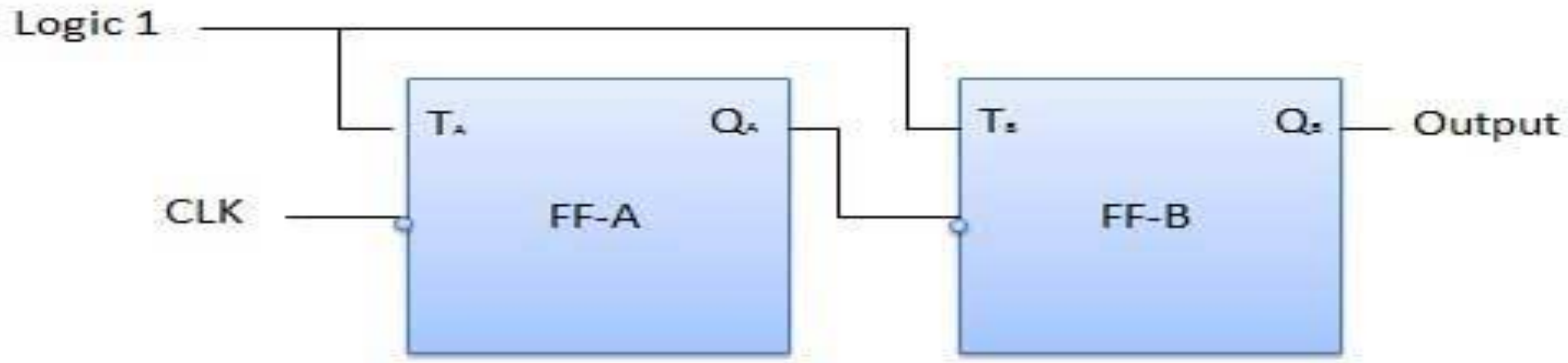
It is a group of flip-flops with a clock signal applied. Counters are of two types.

- Asynchronous or ripple counters.(each part has a specific CLk)
- Synchronous counters.(All the circuits are working with the same CLK)

- Regular
  - Up count
  - Down Conunt
- Irregular

Asynchronous or ripple counters

- The logic diagram of a 2-bit ripple up counter is shown in figure. The toggle (T) flip-flop are being used. But we can use the JK flip-flop also with J and K connected permanently to logic 1.
- External clock is applied to the clock input of flip-flop A and Q_A output is applied to the clock input of the next flip-flop i.e. FF-B.

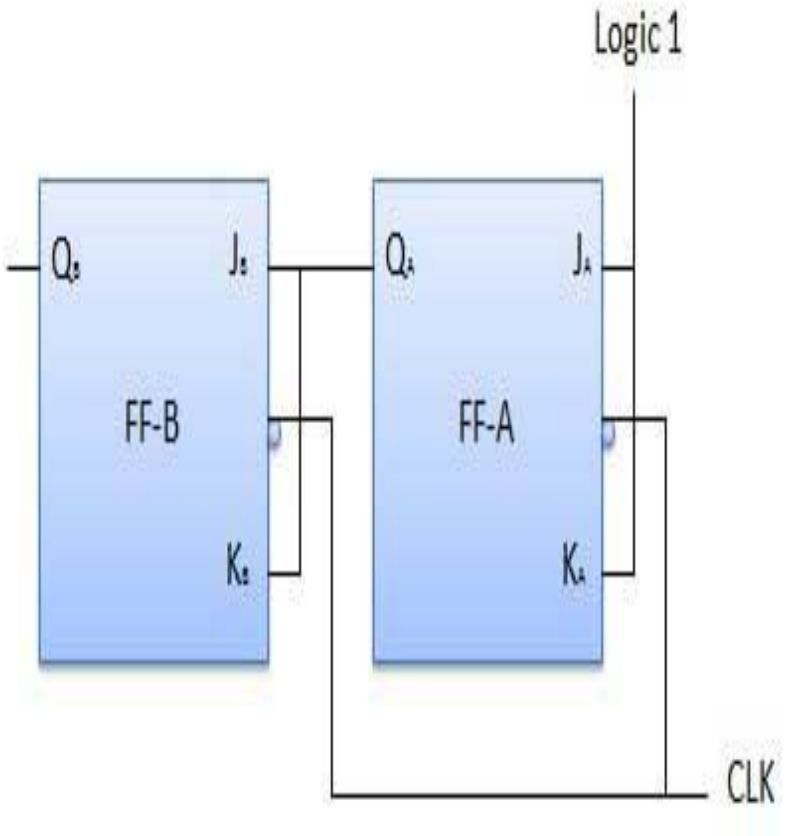


	Condition	Operation
1	Initially let both the FFs be in the reset state	Q_BQ_A = 00 initially
2	After 1st negative clock edge	As soon as the first negative clock edge is applied, FF-A will toggle and Q_A will be equal to 1. Q_A is connected to clock input of FF-B. Since Q_A has changed from 0 to 1, it is treated as the positive clock edge by FF-B. There is no change in Q_B because FF-B is a negative edge triggered FF. Q_BQ_A = 01 after the first clock pulse.
3	After 2nd negative clock edge	On the arrival of second negative clock edge, FF-A toggles again and Q_A = 0. The change in Q_A acts as a negative clock edge for FF-B. So it will also toggle, and $Q_B$will be 1. Q_BQ_A = 10 after the second clock pulse.
4	After 3rd negative clock edge	On the arrival of 3rd negative clock edge, FF-A toggles again and Q_A become 1 from 0.Since this is a positive going change, FF-B does not respond to it and remains inactive. So Q_B does not change and continues to be equal to 1. Q_BQ_A = 11 after the third clock pulse.
5	After 4th negative clock edge	On the arrival of 4th negative clock edge, FF-A toggles again and Q_A becomes 1 from 0. This negative change in $Q_A$acts as clock pulse for FF-B. Hence it toggles to change $Q_B$from 1 to 0.Q_BQ_A = 00 after the fourth clock pulse.

Clock	Counter output		State number	Deciimal Counter output
	Q_B	Q_A		
Initially	0	0	—	0
1st	0	1	1	1
2nd	1	0	2	2
3rd	1	1	3	3
4th	0	0	4	0

Synchronous counters

- If the "clock" pulses are applied to all the flip-flops in a counter simultaneously, then such a counter is called as **synchronous counter.**
- 2-bit Synchronous up counter
- The J_A and K_A inputs of FF-A are tied to logic 1.
- So FF-A will work as a toggle flip-flop. The J_B and K_B inputs are connected to Q_A.



S.N.	Condition	Operation
1	Initially let both the FFs be in the reset state	Q_BQ_A = 00 initially.
2	After 1st negative clock edge	As soon as the first negative clock edge is applied, FF-A will toggle and Q_A will change from 0 to 1. But at the instant of application of negative clock edge, Q_A , J_B = K_B = 0. Hence FF-B will not change its state. So Q_B will remain 0. Q_BQ_A = 01 after the first clock pulse.
3	After 2nd negative clock edge	On the arrival of second negative clock edge, FF-A toggles again and Q_A changes from 1 to 0. But at this instant Q_A was 1. So J_B = K_B= 1 and FF-B will toggle. Hence Q_B changes from 0 to 1. Q_BQ_A = 10 after the second clock pulse.
4	After 3rd negative clock edge	On application of the third falling clock edge, FF-A will toggle from 0 to 1 but there is no change of state for FF-B. Q_BQ_A = 11 after the third clock pulse.
5	After 4th negative clock edge	On application of the next clock pulse, Q_A will change from 1 to 0 as Q_B will also change from 1 to 0. Q_BQ_A = 00 after the fourth clock pulse.

Classification of counters

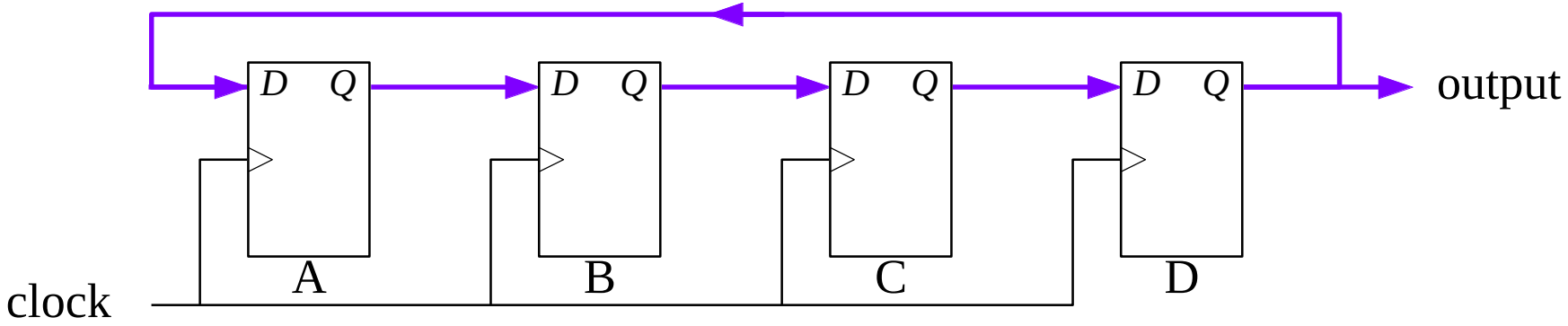
- Depending on the way in which the counting progresses, the synchronous or asynchronous counters are classified as follows –
  - Up counters
  - Down counters
  - Up/Down counters

UP/DOWN Counter

- Up counter and down counter is combined together to obtain an UP/DOWN counter. A mode control (M) input is also provided to select either up or down mode. A combinational circuit is required to be designed and used between each pair of flip-flop in order to achieve the up/down operation.
- Type of up/down counters
  - UP/DOWN ripple counters
  - UP/DOWN synchronous counter

Ring counter

A shift register with its output fed back to its input forms a **ring counter**.



This can be used to generate an arbitrary binary pattern of length *N*, where *N* is the number of stages in the ring counter. It must be preloaded with the sequence desired, which then rotates around the counter indefinitely.

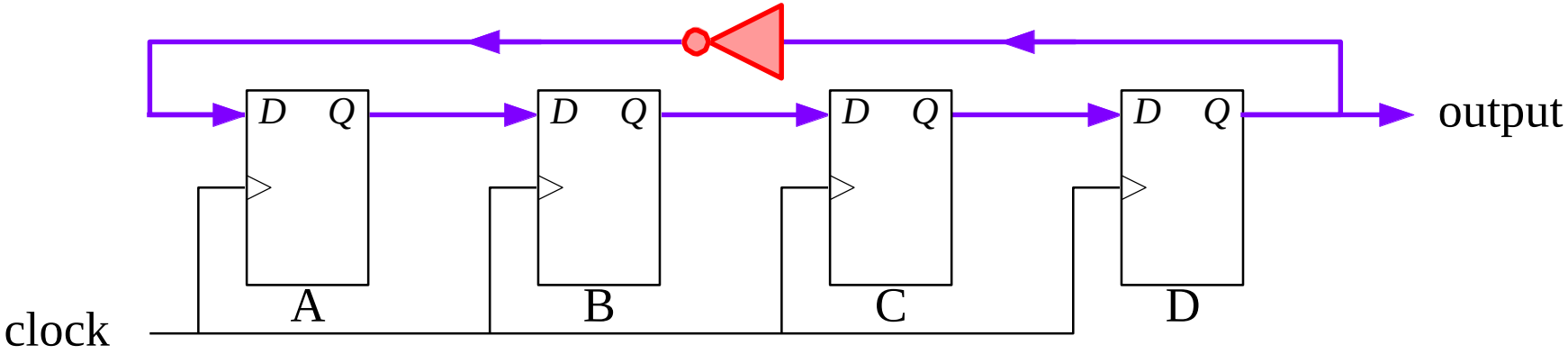
One application is to divide down the clock frequency for a slower part of a digital system, while keeping everything synchronous. Modern computers have several 'buses' running at different speeds, where a ring counter is used to create the clocks for the various buses.

It is much harder to multiply a given frequency to obtain a higher frequency signal.

A **phase locked loop (PLL)** is often used.

Johnson counter

A ring counter with the **complement** of its output fed back is a **Johnson counter**.



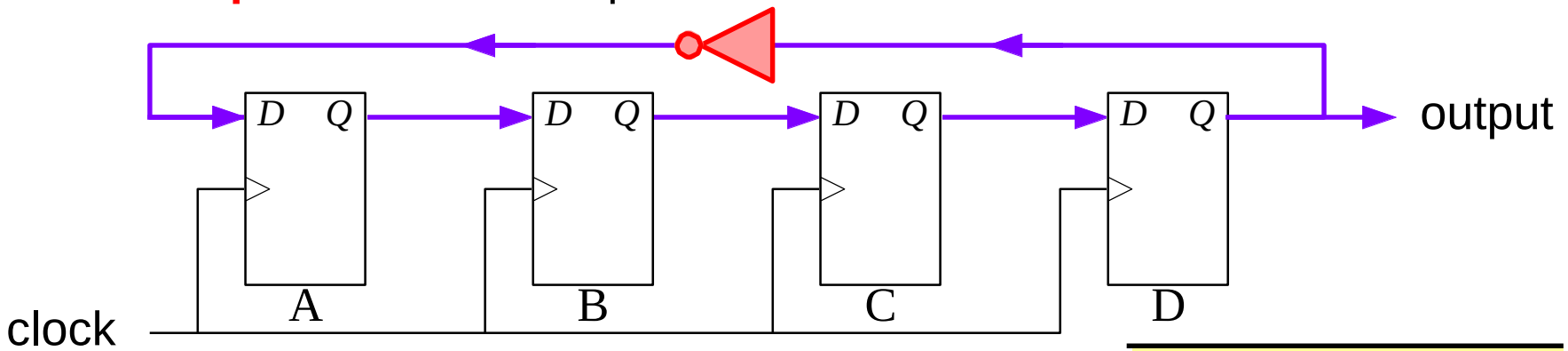
This generates longer sequences than a simple ring counter.

For example, a ring counter with 3 stages produces a cycle of 3 states — a waste as there are $2^3 = 8$ states in all.

A Johnson counter with 3 stages has a cycle of 6 and a separate cycle of 2. It is important to ensure that it follows the correct one!

Johnson counter

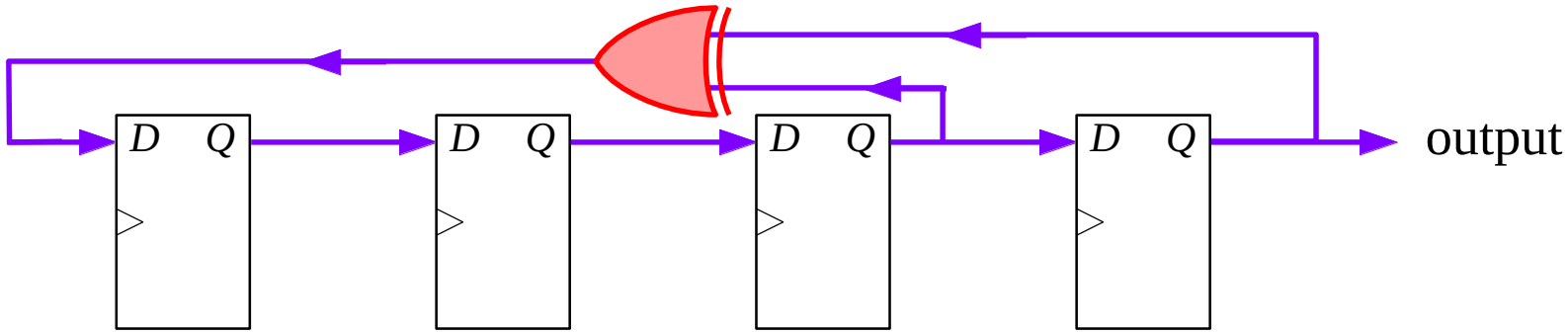
A ring counter with the **complement** of its output fed back is a **Johnson counter**.



Q_A	Q_B	Q_C
0	0	0
1	0	0
1	1	0
1	1	1
0	1	1
0	0	1
1	0	1
0	1	0

Pseudo-random number generator

A ring counter with feedback through an **exclusive-or gate** makes a simple pseudo-random number generator.



- Pseudo-random sequences of 1s and 0s have many applications, notably in encryption. They appear to be random over 'short' times but the sequence eventually repeats, hence the more accurate term 'pseudo-random'.
- Also, they can be reproduced perfectly if you know both:
  - **the method used to generate the sequence**
  - **the state in the sequence at which to start**
- This is an important feature! — see next sheet.
- The circuit above has a period of $2^4 - 1 = 15$
- (the missing state is 0000 —why?).

Transmission of data — serial format

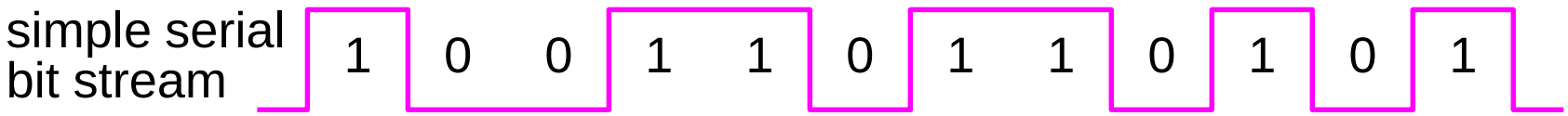
Data often has to be transmitted from one computer to another, or from a computer to peripheral equipment (printer, modem, …). This can be done in:

- **serial format**, one bit at a time
- **parallel format**, several bits at a time (e.g. byte at a time, 8 bits)

Serial format is most commonly used because it is simpler. Only a few wires are needed:

- traditional **serial 'COM' ports (RS-232)** need only 3 wires (transmitted data, received data and ground — but more may be used for control)
- **universal serial bus** (USB, common on modern computers) uses 4 wires (two for differential data plus power and ground)

Traditional serial transmission was slow but modern systems use much faster rates (USB version 1 up to 12 Mbits per second, FireWire 1 up to 400 Mbits per second), version 2 of both even faster.



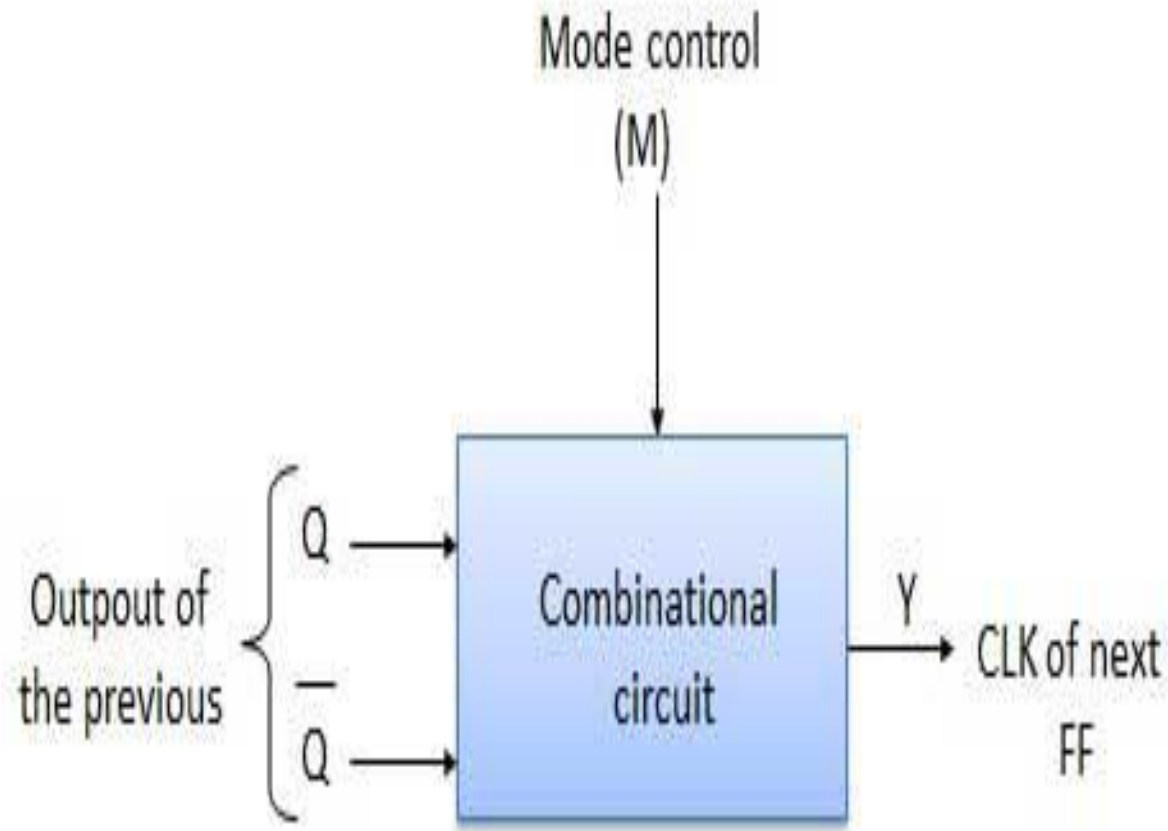
UP/DOWN Ripple Counters

- In the UP/DOWN ripple counter all the FFs operate in the toggle mode. So either T flip-flops or JK flip-flops are to be used. The LSB flip-flop receives clock directly. But the clock to every other FF is obtained from (Q = Q bar) output of the previous FF.
- **UP counting mode (M=0)** − The Q output of the preceding FF is connected to the clock of the next stage if up counting is to be achieved. For this mode, the mode select input M is at logic 0 (M=0).
- **DOWN counting mode (M=1)** − If M = 1, then the Q bar output of the preceding FF is connected to the next FF. This will operate the counter in the counting mode.

3-bit binary up/down ripple counter.

- 3-bit – hence three FFs are required.
- UP/DOWN – So a mode control input is essential.
- For a ripple up counter, the Q output of preceding FF is connected to the clock input of the next one.
- For a ripple up counter, the Q output of preceding FF is connected to the clock input of the next one.
- For a ripple down counter, the Q bar output of preceding FF is connected to the clock input of the next one.
- Let the selection of Q and Q bar output of the preceding FF be controlled by the mode control input M such that, If M = 0, UP counting. So connect Q to CLK. If M = 1, DOWN counting. So connect Q bar to CLK.

Block Diagram



Inputs			Outputs	
M	Q	$\overline{Q}$	Y	
0	0	0	0	Y = Q for up counter
0	0	1	0	
0	1	0	1	
0	1	1	1	
1	0	0	0	$Y = \overline{Q}$ for up counter
1	0	1	1	
1	1	0	0	
1	1	1	1	

S.N.	Condition	Operation
1	Case 1 – With M = 0 (Up counting mode)	If M = 0 and M bar = 1, then the AND gates 1 and 3 in fig. will be enabled whereas the AND gates 2 and 4 will be disabled. Hence Q_A gets connected to the clock input of FF-B and $Q_B$gets connected to the clock input of FF-C. These connections are same as those for the normal up counter. Thus with M = 0 the circuit work as an up counter.
2	Case 2: With M = 1 (Down counting mode)	If M = 1, then AND gates 2 and 4 in fig. are enabled whereas the AND gates 1 and 3 are disabled. Hence Q_A bar gets connected to the clock input of FF-B and Q_B bar gets connected to the clock input of FF-C. These connections will produce a down counter. Thus with M = 1 the circuit works as a down counter.

Modulus Counter (MOD-N Counter)

- The 2-bit ripple counter is called as MOD-4 counter and 3-bit ripple counter is called as MOD-8 counter. So in general, an n-bit ripple counter is called as modulo-N counter. Where, MOD number = 2^n.
- Type of modulus
  - 2-bit up or down (MOD-4)
  - 3-bit up or down (MOD-8)
  - 4-bit up or down (MOD-16)

Application of counters

- Frequency counters
- Digital clock
- Time measurement
- A to D converter
- Frequency divider circuits
- Digital triangular wave generator

Reference

- mano BOOK

http://osp.mans.edu.eg/cs212/Seq_circuits_analysis.htm

Logic and Computer Design Fundamentals, Charles Kime & Thomas Kaminski
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(Edited by Dr. Muhamed Mudawar for COE 202 and EE 200 at KFUPM)

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