SOAREX GROUP

Miller Effect (MOSFETS)

Dave VE3OOI

August 2023

Another riveting VE3OOI presentation....

AGENDA

1. **Fundamentals:**
   - ✓**MOSFET Construction**
   - ✓**Observations**

2. **Miller Effect, Capacitance and Theorem.**

3. ***Addressing Miller Effect***
   - ✓***CASCODE/HYCAS***
   - ✓***"Scotty" Approach***

4. ***BONUS: Feedback Amplifiers***
   - ✓***What's not explained in EMRFD et. al.***

Captain, we need to kick Miller in the bag pipes

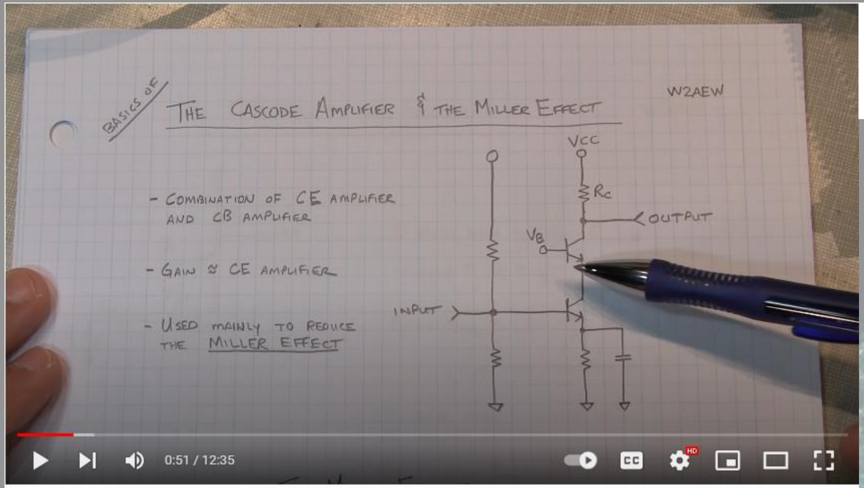
Danger Will Robinson…

Quote Charlie Morris, ZL2CTM:

This NOT a tutorial.

It's a log of my journey. Right or wrong.

REFERENCES

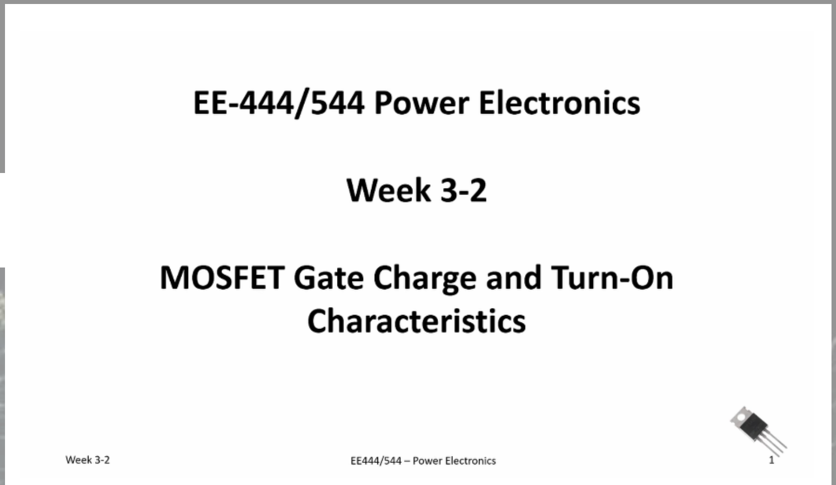


#207: Basics of a Cascode Amplifier and the Miller Effect

w2aew
193K subscribers

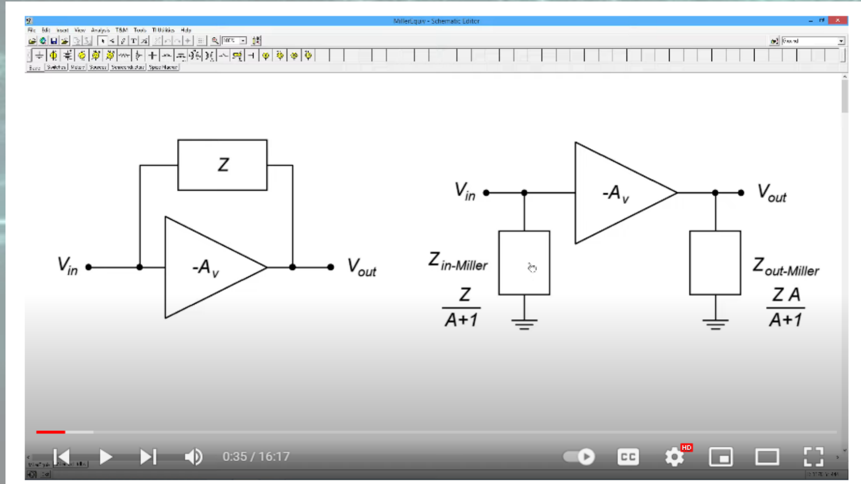
https://youtu.be/Op_I3Ke7px0

Power Electronics with Dr. K
8.37K subscribers



Power Electronics WK3_2 MOSFET Turn On Characteristics

https://youtu.be/f1yt0s3gpcE

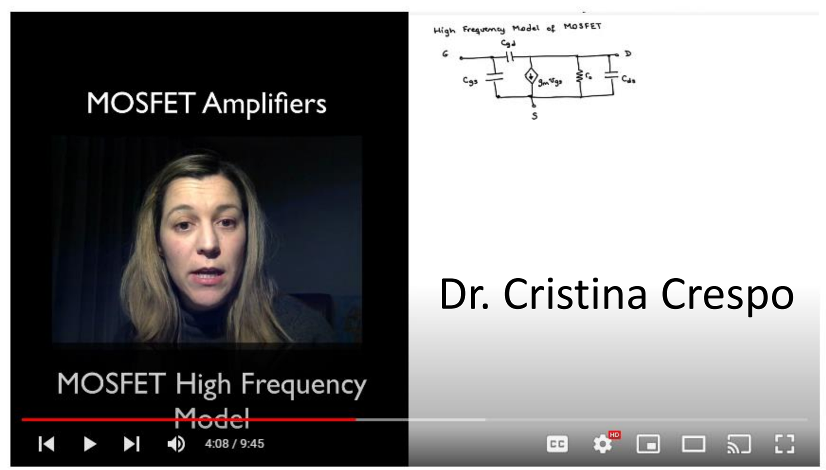


Semiconductor Devices: Miller's Theorem

Electronics with Professor Fiore
7.24K subscribers

https://youtu.be/yM9xlbAf43Q

Mateo Aboy
14.2K subscribers



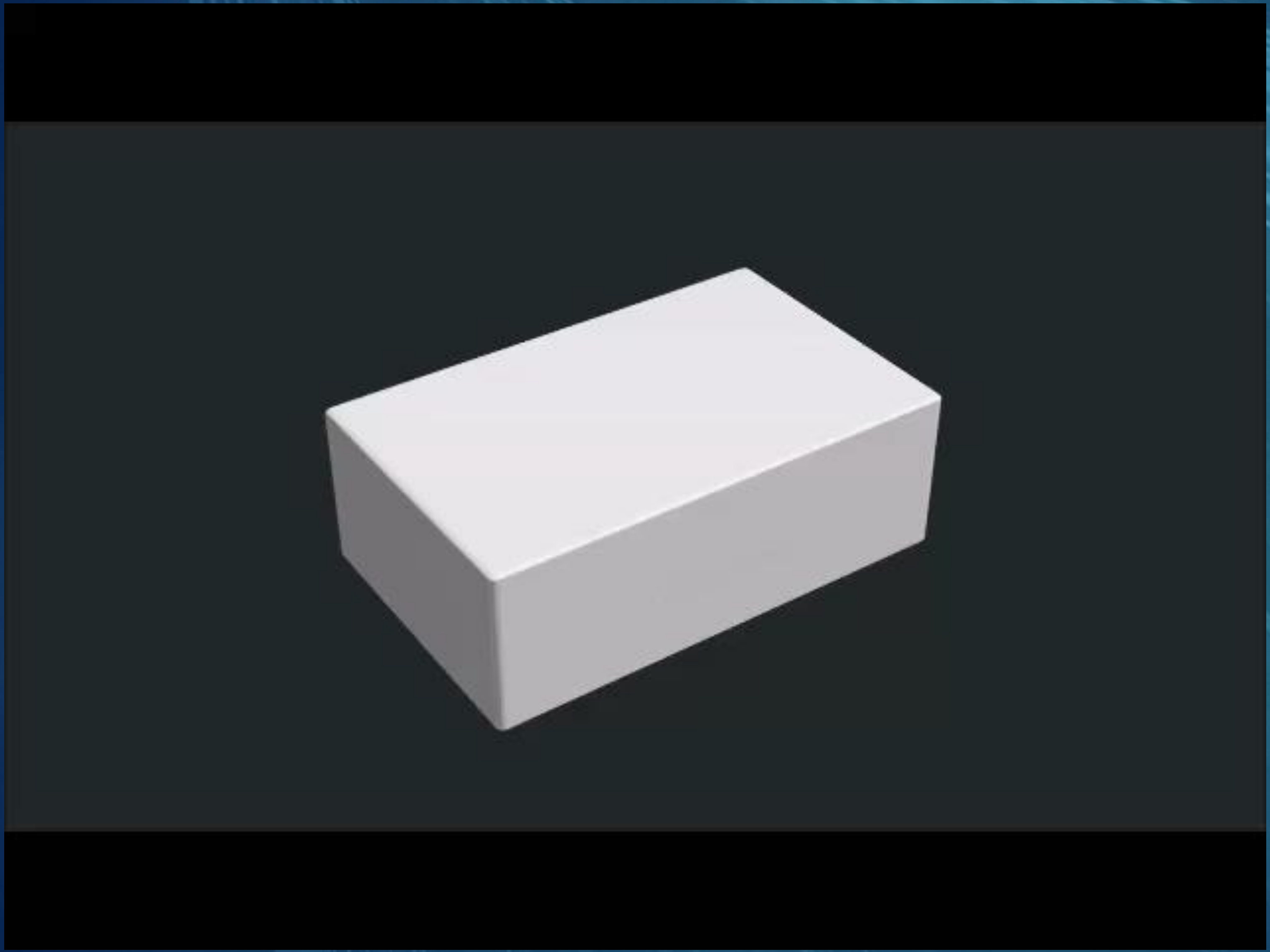
MOSFET High Frequency Model

https://youtu.be/19kXfUPdF9I

This won’t hurt at all…

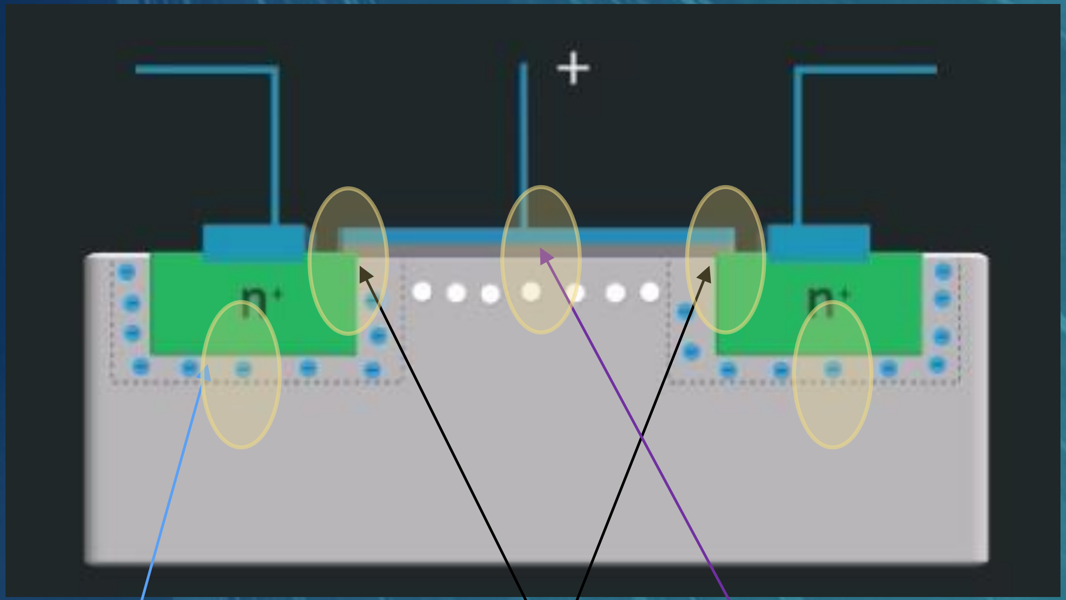
MOSFET CONSTRUCTION

N Channel
Enhancement Mode



1. Created by applying two “N” doped semiconductors to a based on “P” doped semiconductor
2. N-Doped has impurity added with excess electrons and P-Doped has impurity added with more holes (missing electrons)
3. The N doped semiconductors are source and drain (Collector/Emitter)
4. A metal plate with an insulator is added to the P-doped base to create a capacitor.
5. When a voltage is applied to the gate with **respect to the source**, elections are attracted to the gate, and a channel is formed.
6. Once a threshold gate voltage is applied, current flows between drain and source

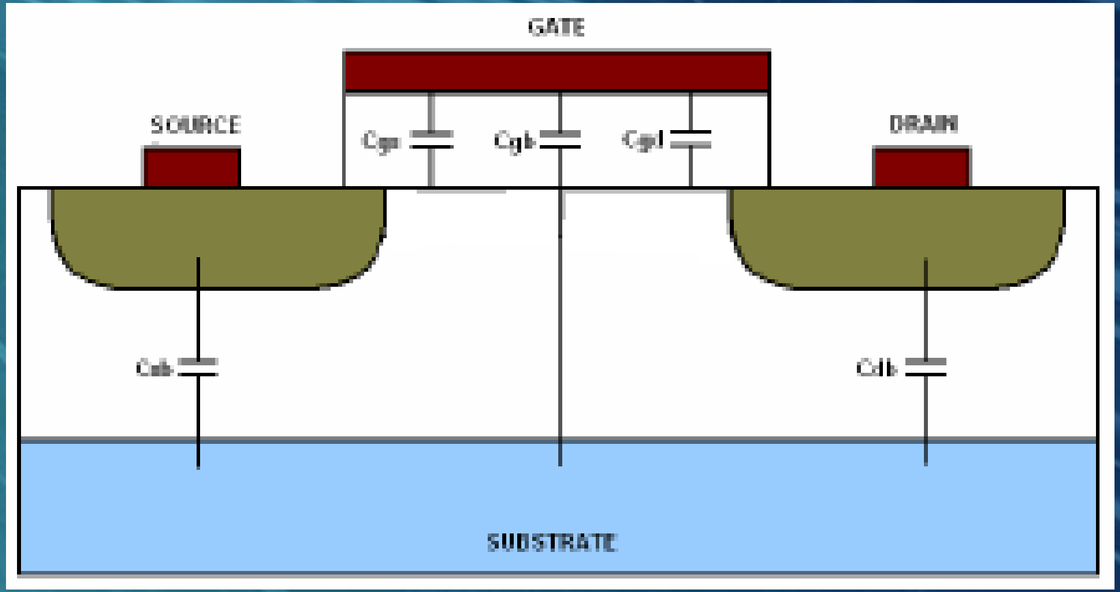
Capacitors

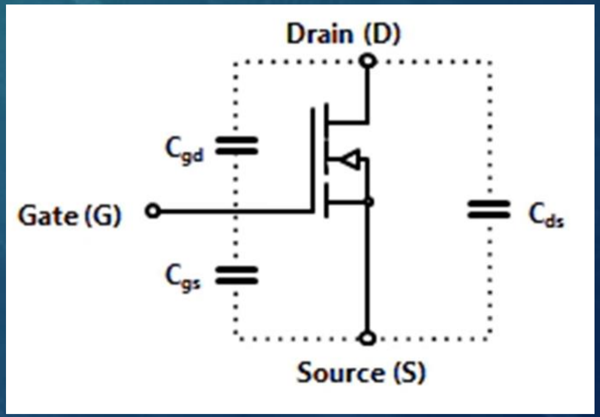


Depletion region

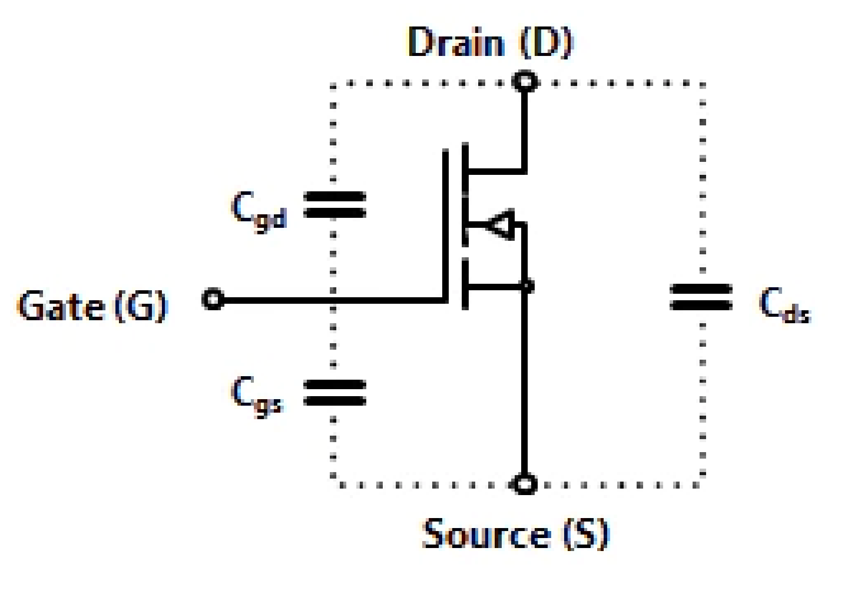
Overlap

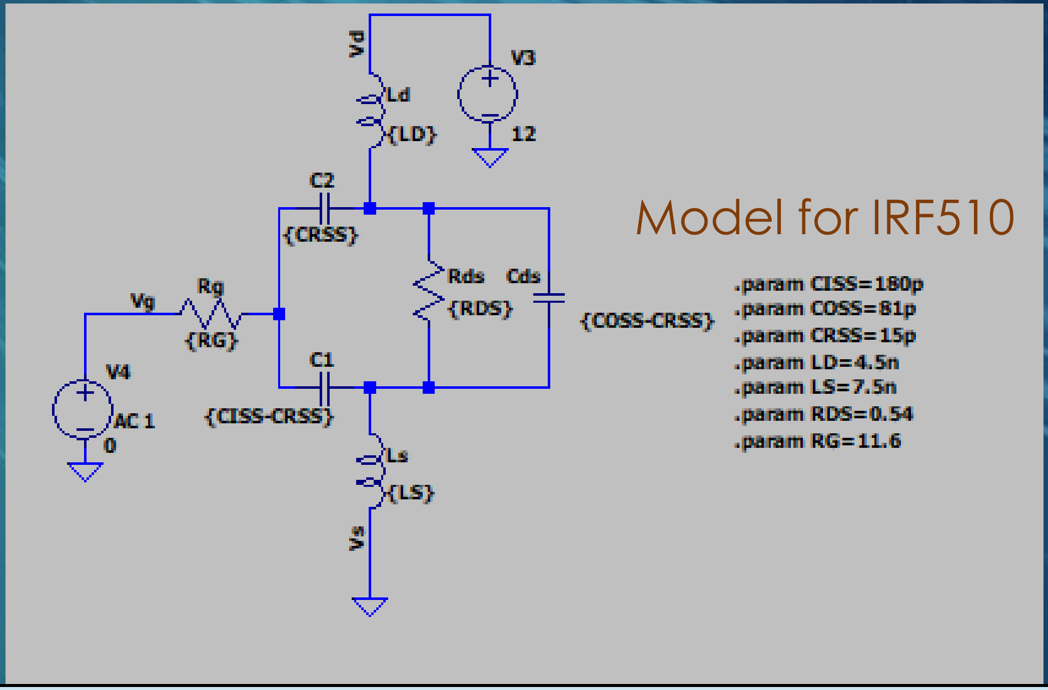
Oxide/dielectric



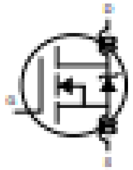


MOSFET CAPACITANCE DEFINED





IRF510

Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	180	-	pF
Output capacitance	C_{oss}		-	81	-	
Reverse transfer capacitance	C_{rss}		-	15	-	
Gate input resistance	R_g	f = 1 MHz, open drain	2.5	-	11.6	Ω
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal source inductance	L_S		-	7.5	-	

Typical datasheet values:

Equivalent input capacitance: C_{iss}

Forward / Reverse Transfer Capacitance: C_{rss}

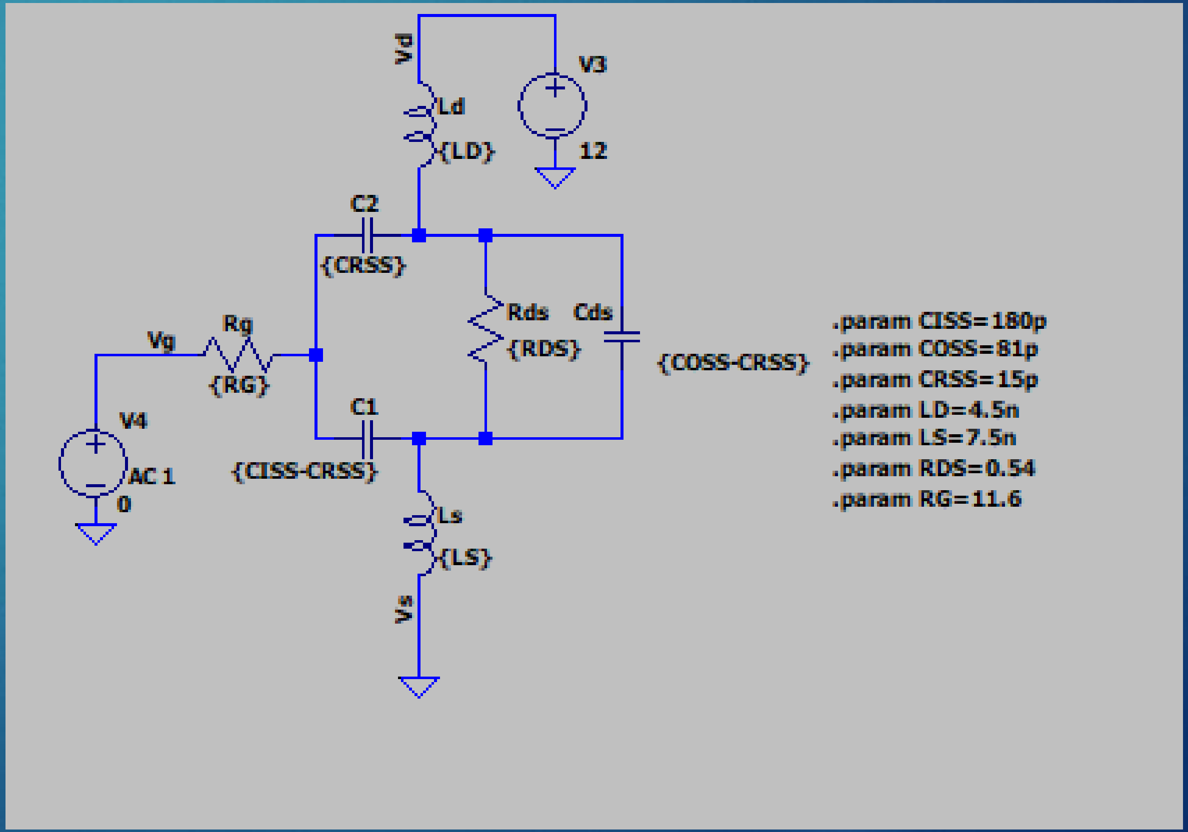
Equivalent output capacitance: C_{oss}

$C_{iss} = C_{gs} + C_{gd}$

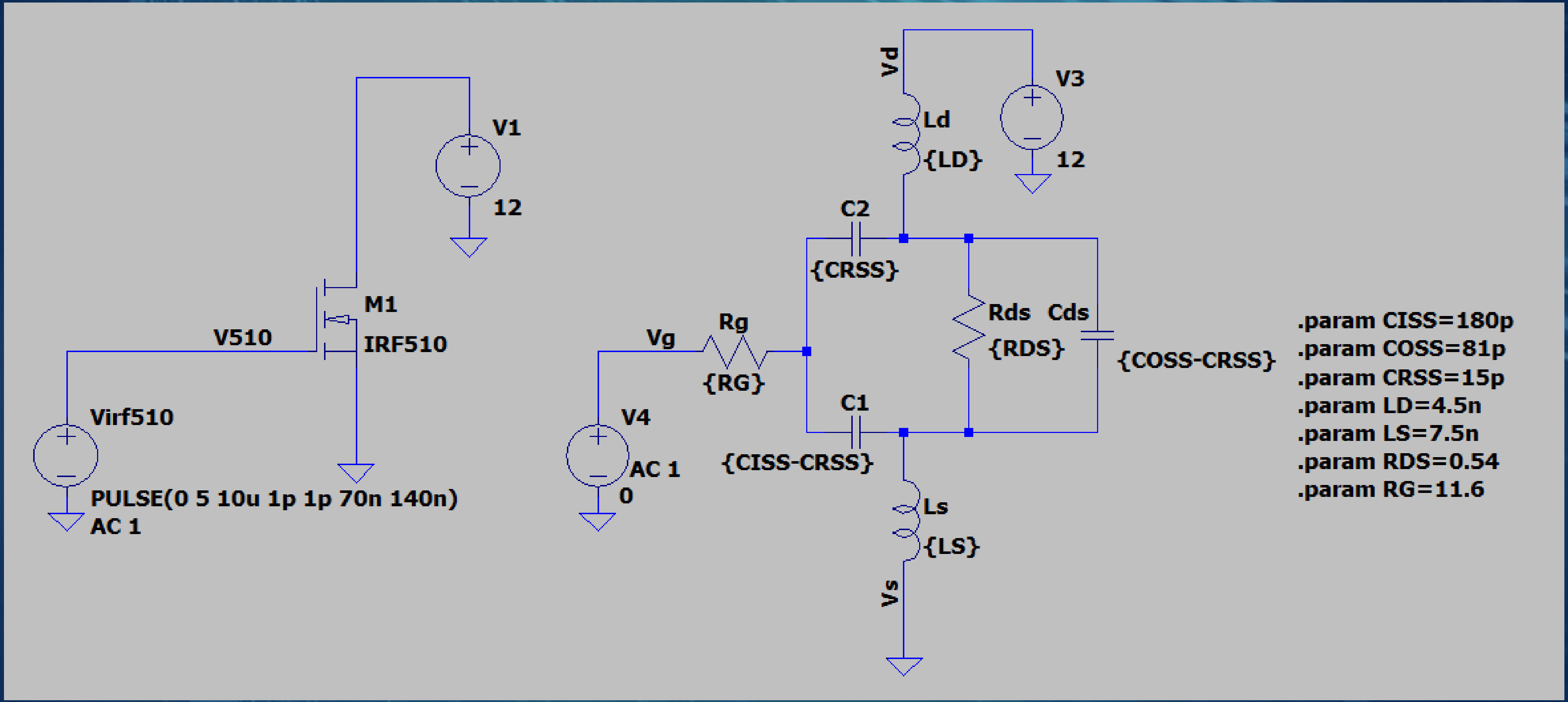
$C_{rss} = C_{gd}$

$C_{oss} = C_{gd} + C_{ds}$

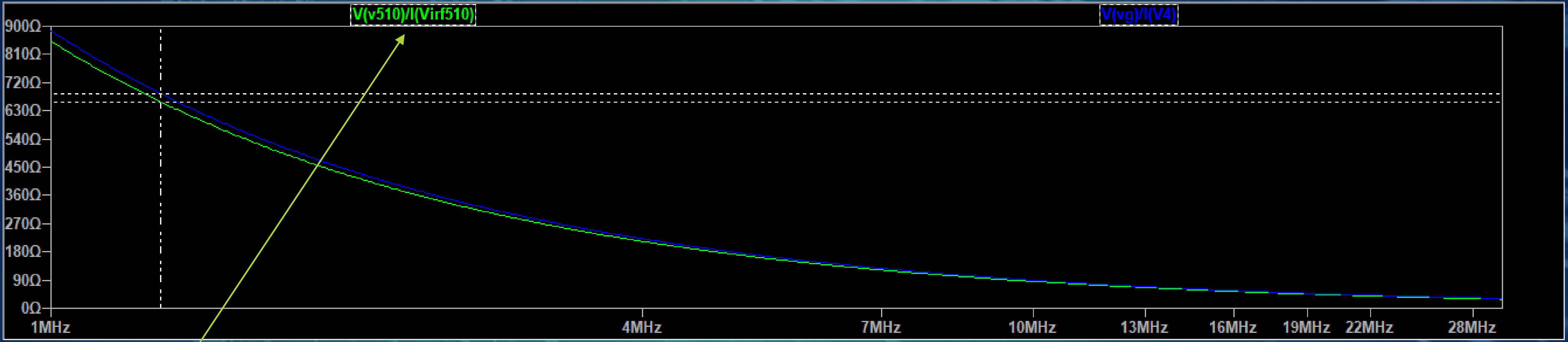
Dr. Cristina Crespo
https://youtu.be/19kXfUPdF9I



Model Comparison



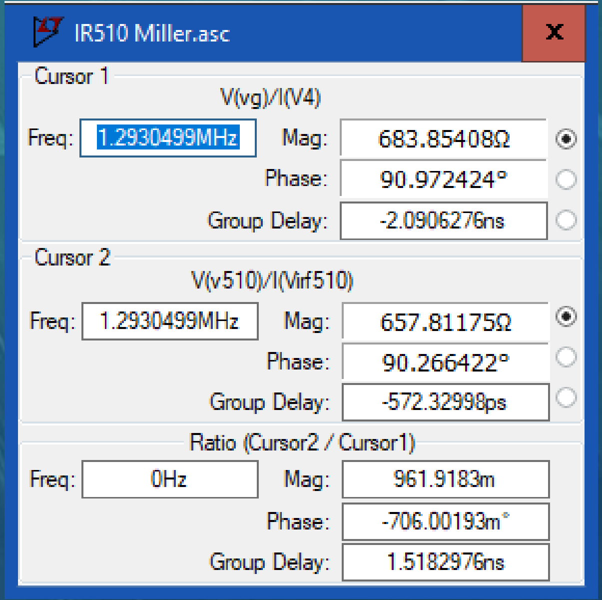
Winner…Winner…



LTSpice Trick:

- ✓ right clk Select "Add Plot"
- ✓ select what you want to plot
- ✓ Can use * / + - fun()

http://ltwiki.org/index.php?title=Waveform_Arithmetic



SUMMARY: THE ISSUE

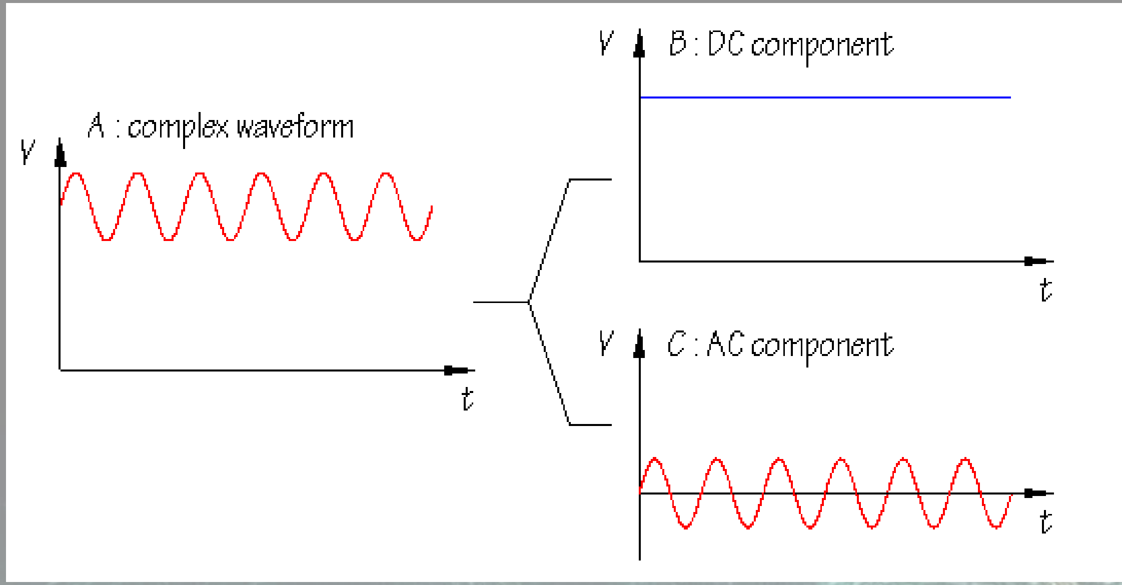
Due to the internal capacitors, the MOSFET is frequency dependant

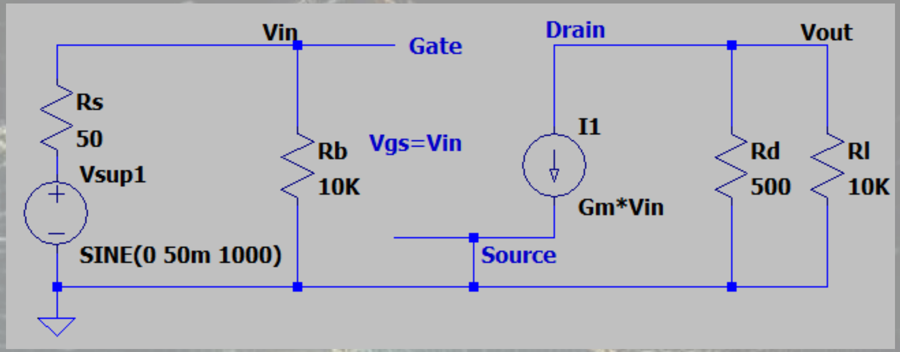
- **The MOSFET internal capacitors acts as a short circuit from gate to source**
- **Input impedance is very small**

...but it gets worst!

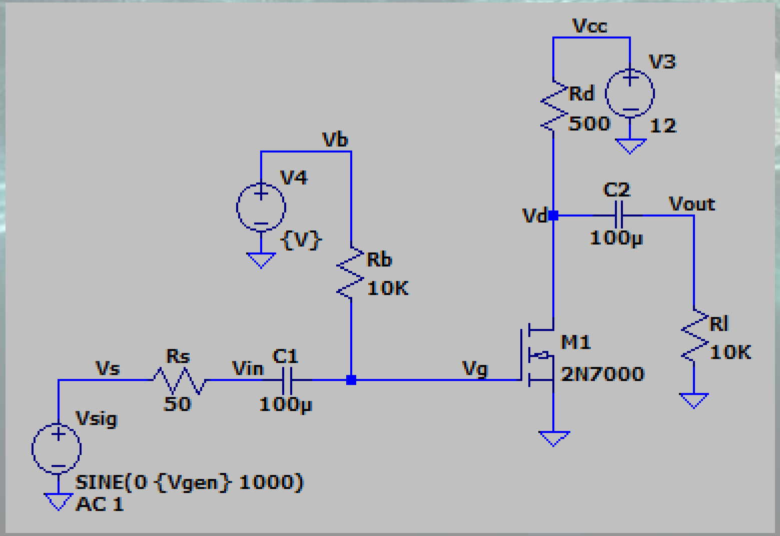
John Milton Miller

TRANSISTOR MODELS

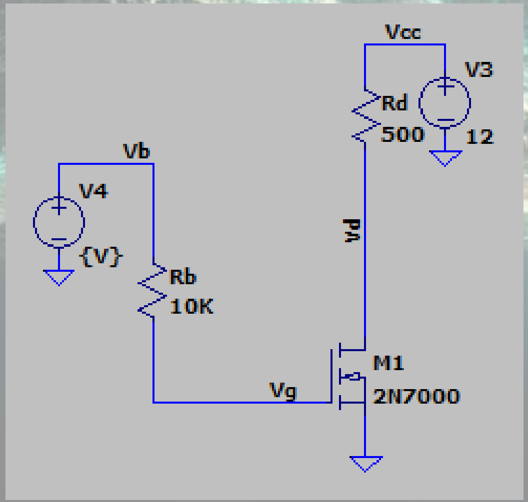




AC (Small Signal) Model

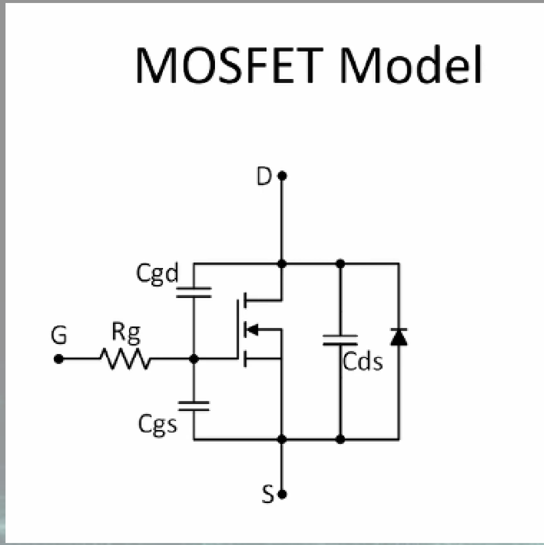


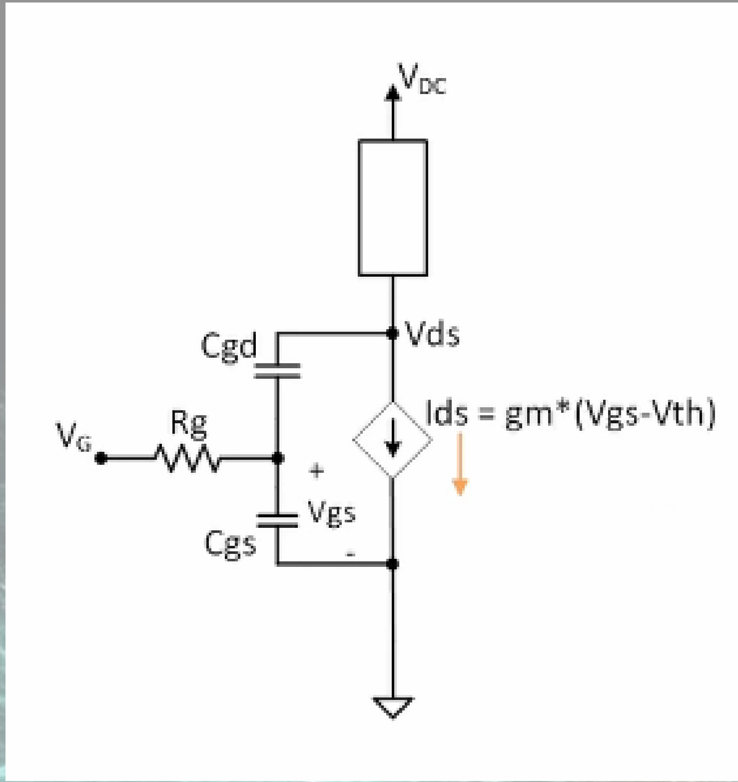
Common Source Amplifier



DC Model

FUNDEMANTALS





1. **The model of a MOSFET is basically an ideal current source that driven by the gate to source voltage**

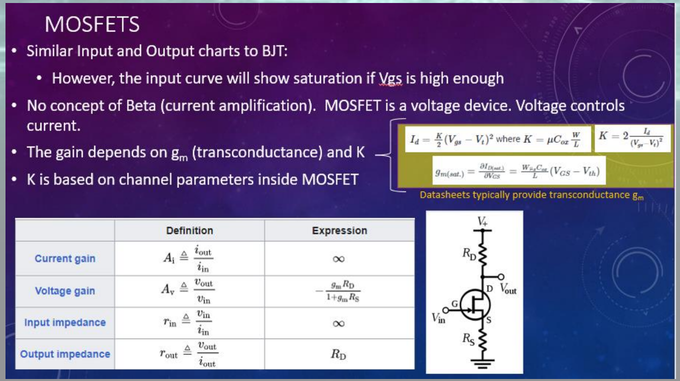
2. **When gate voltage is zero, MOSFET is off and Cgd is charged with respect to Vdc.**

3. **When gate voltage starts to rise (small voltage), all current flows to Cgs and that starts to charge.**

4. **Once Vgs threshold reached, Ids begins to increase and Vds starts to drop. Cgd starts to discharge.**

5. **Once Ids reaches maximum, then Vds is close to zero and Cgd is discharged. As Vgs increases, Cgd now charges with opposite polarity. Once Cgd is fully charged, the MOSFET is on.**

6. **The time for the MOSFET to turn on is from charge time of BOTH Cgs and Cgd. This is critical for MOSFET as a switch (e.g. buck converter)**



MOSFETS

- Similar Input and Output charts to BJT:
  - However, the input curve will show saturation if Vgs is high enough
- No concept of Beta (current amplification). MOSFET is a voltage device. Voltage controls current.
- The gain depends on g_m (transconductance) and K
- K is based on channel parameters inside MOSFET

$I_d = \frac{K}{2}(V_{gs} - V_t)^2$ where $K = \mu C_{ox}\frac{W}{L}$

$K = 2\frac{I_d}{(V_{gs}-V_t)^2}$

$g_{m(sat.)} = \frac{\partial I_{D(sat.)}}{\partial V_{GS}} = \frac{W \mu_n C_{ox}}{L}(V_{GS} - V_{th})$

Datasheets typically provide transconductance g_m

	Definition	Expression
Current gain	$A_i \triangleq \frac{i_{out}}{i_{in}}$	∞
Voltage gain	$A_v \triangleq \frac{v_{out}}{v_{in}}$	$-\frac{g_m R_D}{1+g_m R_S}$
Input impedance	$r_{in} \triangleq \frac{v_{in}}{i_{in}}$	∞
Output impedance	$r_{out} \triangleq \frac{v_{out}}{i_{out}}$	R_D

https://youtu.be/t6_chWRdSyg?si=I5OjAjNdn_JZtLlY

IRF510 DATASHEET

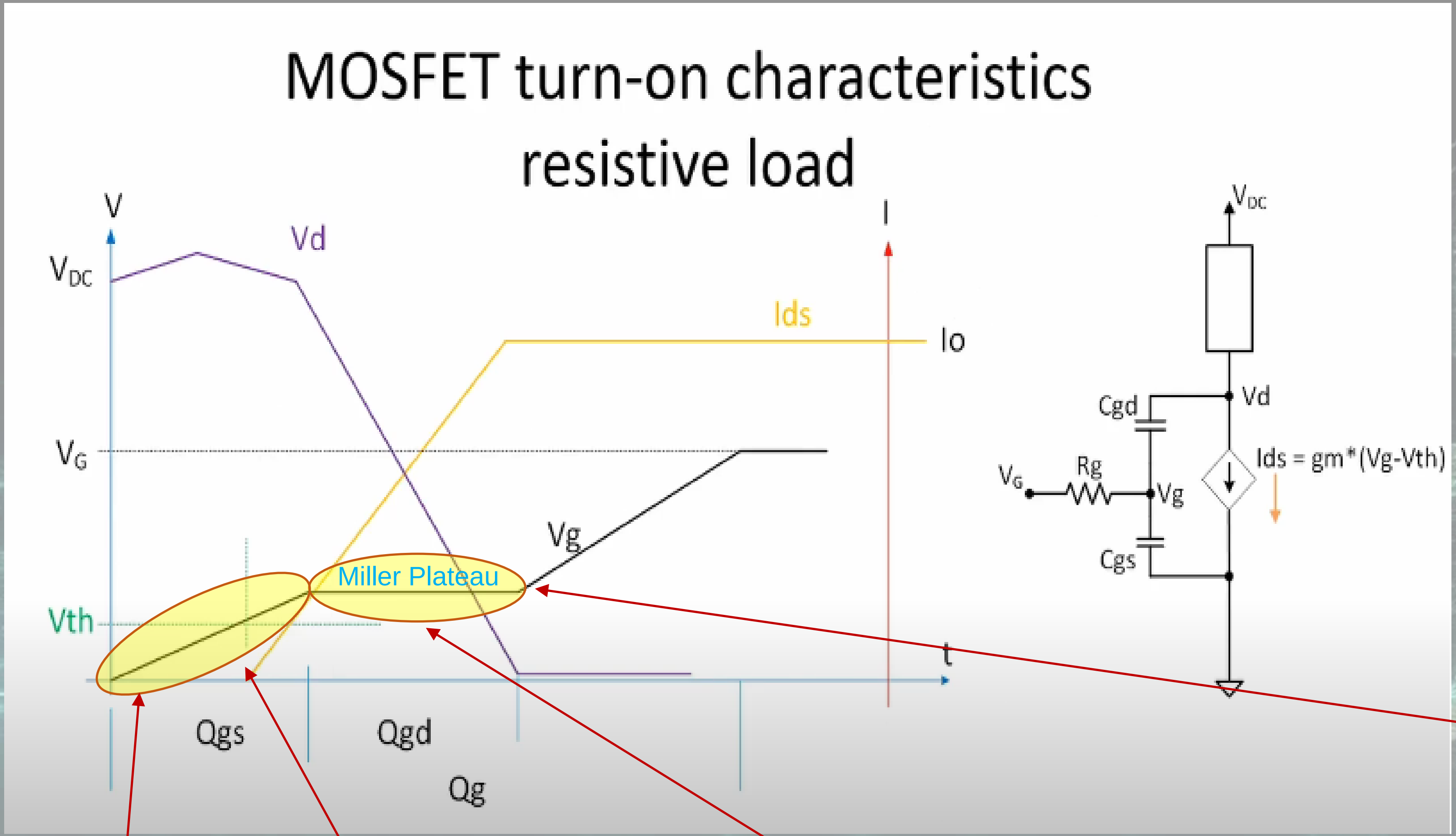
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	100	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.12	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	-	4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	-	-	25	μA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 150 °C	-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D =3.4 A [b]	-	-	0.54	Ω
Forward transconductance	g_{fs}	V_{DS} = 50 V, I_D = 3.4 A [b]	1.3	-	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	180	-	pF
Output capacitance	C_{oss}		-	81	-	
Reverse transfer capacitance	C_{rss}		-	15	-	
Total gate charge	Q_g	V_{GS} = 10 V; I_D = 5.6 A, V_{DS} = 80 V V_{DS} = 10 V, see fig. 6 and fig. 13 [b]	-	-	8.3	nC
Gate-source charge	Q_{gs}		-	-	2.3	
Gate-drain charge	Q_{gd}		-	-	3.8	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 5.6 A R_g = 24 Ω, R_D = 8.4 Ω, see fig. 10 [b]	-	6.9	-	ns
Rise time	t_r		-	16	-	
Turn-off delay time	$t_{d(off)}$		-	15	-	
Fall time	t_f		-	9.4	-	
Gate input resistance	R_g	f = 1 MHz, open drain	2.5	-	11.6	Ω
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal source inductance	L_S		-	7.5	-	

One ampere is equal to 1 coulomb moving past a point in 1 second, or $6.241509074 \times 10^{18}$ electrons' worth of charge moving past a point in 1 second.

SCOPING A MOSFET

Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	180	-	pF
Output capacitance	C_{oss}		-	81	-	
Reverse transfer capacitance	C_{rss}		-	15	-	

MILLER CAPACITANCE: THEORY



Cgd & Cgs Almost Fully Charged

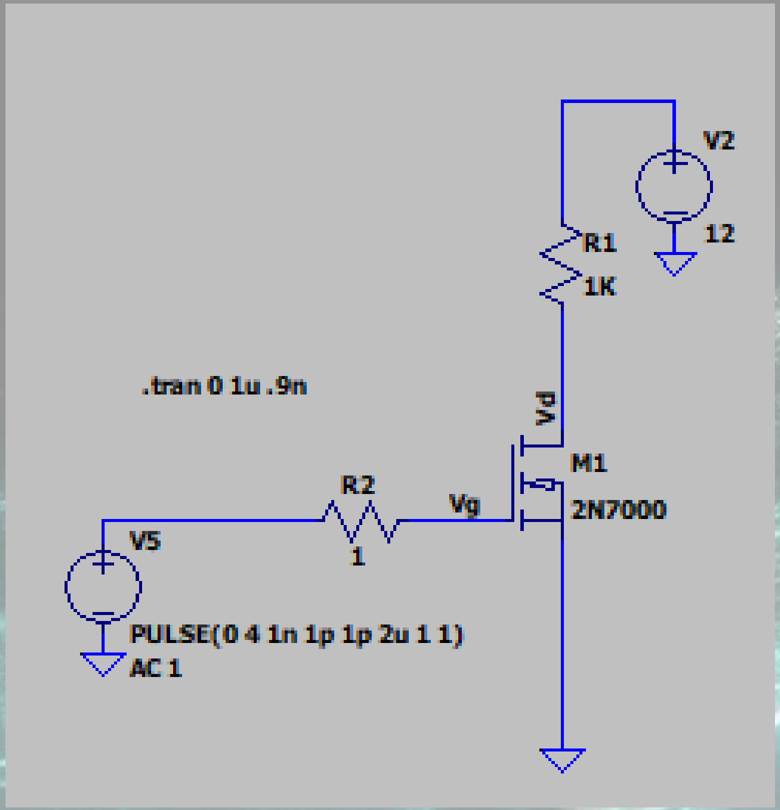
Max Current and Zero Voltage drop

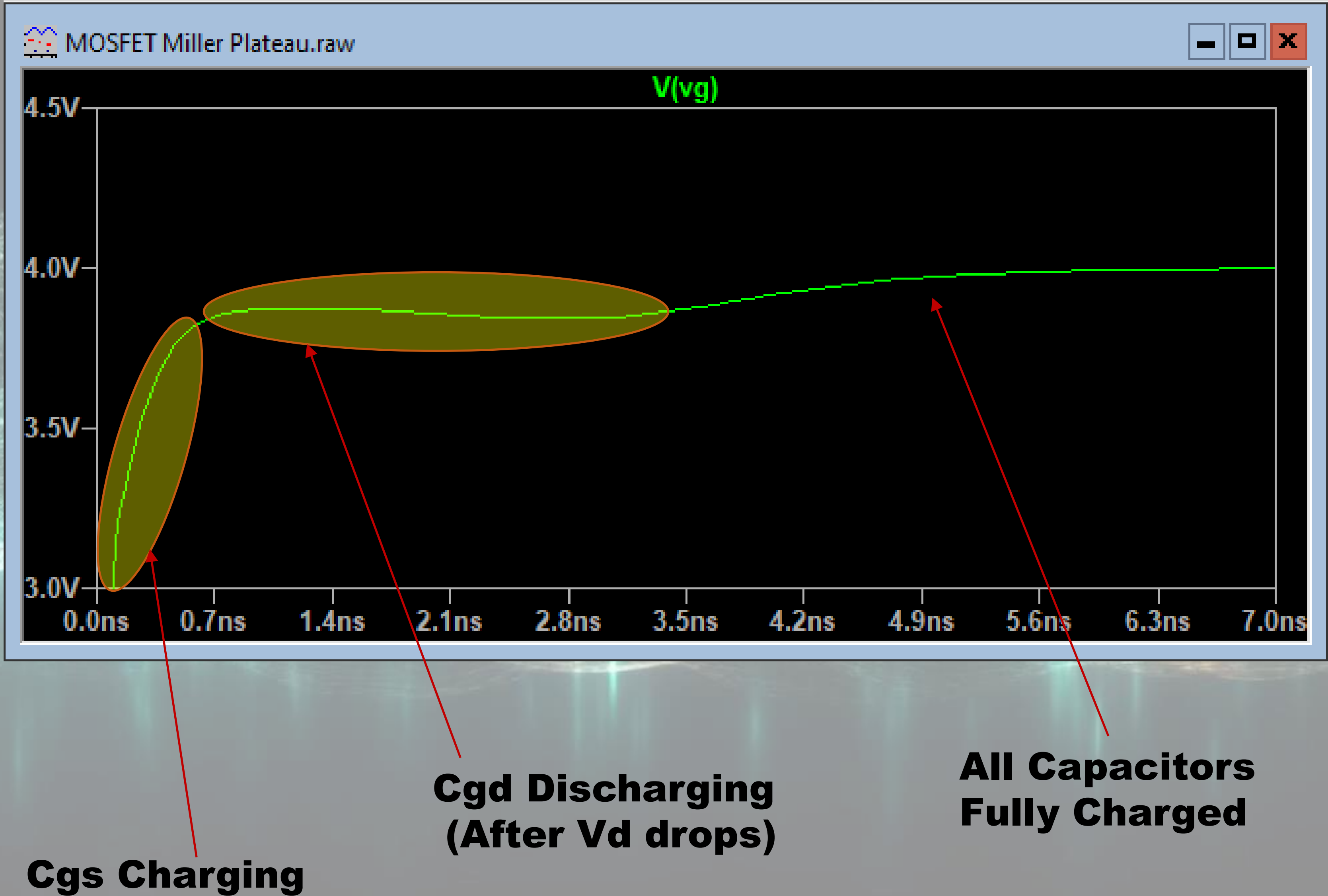
Cgs Charging

MOSFET Threshold Voltage

Cgd Discharging (After Vd Drops)

MILLER CAPACITANCE: 2N7000





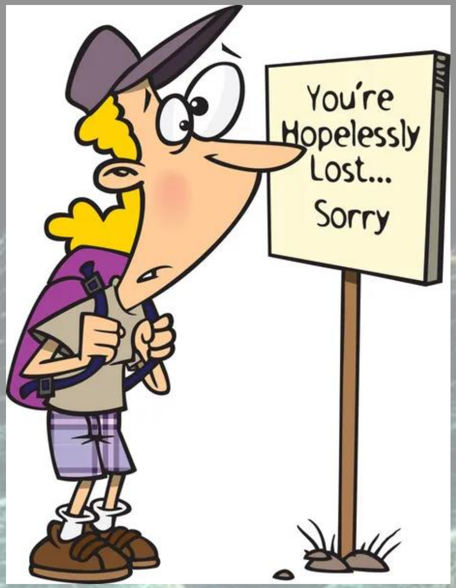
The plot thickens….

1. **Due to the internal capacitors, the MOSFET is frequency dependant. At high frequencies, the input impedance is reduced (almost short circuit)**

2. **The time for the MOSFET to turn on completely is dependent on the Cgs and Cgd capacitors charging**

Total gate charge	Q_g	$V_{GS} = 10$ V	$I_D = 5.6$ A, $V_{DS} = 80$ V $V_{DS} = 10$ V, see fig. 6 and fig. 13 [b]	-	-	8.3	nC
Gate-source charge	Q_{gs}			-	-	2.3	
Gate-drain charge	Q_{gd}			-	-	3.8	

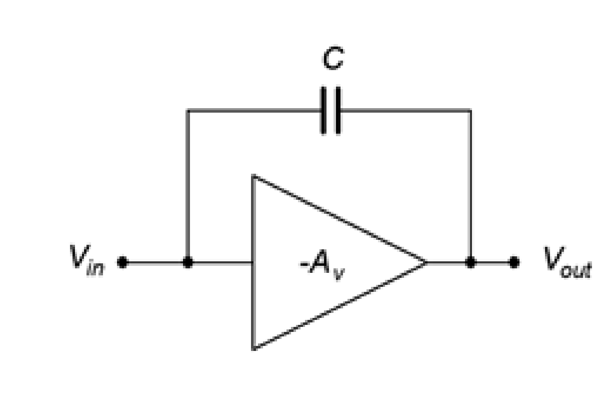
MILLER EFFECT, CAPACITANCE & THEOREM

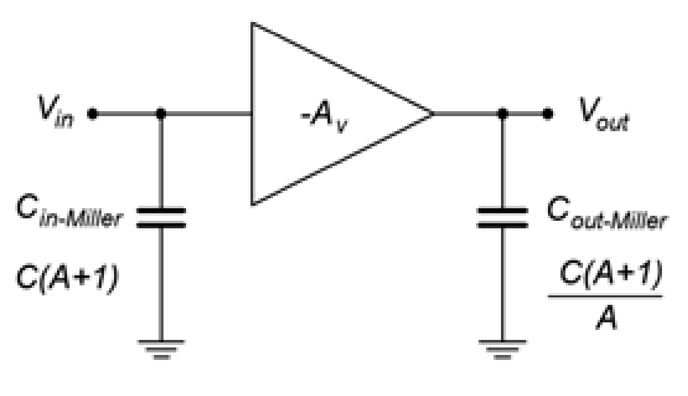


This is a cycle of resistance and capacitance occurring between the input and output of an amplifier circuit, which can create a primitive low-pass filter that is signal dependant. The effective input impedance of an amplifier depends on the impedance connected from input to output of the amplifier. The apparent scaling of this impedance often dominates the input impedance and frequency response of the amplifier. This effect was first reported by John Miller in 1919 and is now commonly known as the Miller Effect or Miller Capacitance.

Although the term *Miller effect* normally refers to capacitance, any impedance connected between the input and another node exhibiting gain can modify the amplifier input impedance via this effect. These properties of the Miller effect are generalized in the Miller theorem. The Miller capacitance due to parasitic capacitance between the output and input of active devices like transistors and vacuum tubes is a major factor limiting their gain at high frequencies. Miller capacitance was identified in 1920 in triode vacuum tubes by John Milton Miller.

MILLER EFFECT/THEOREM



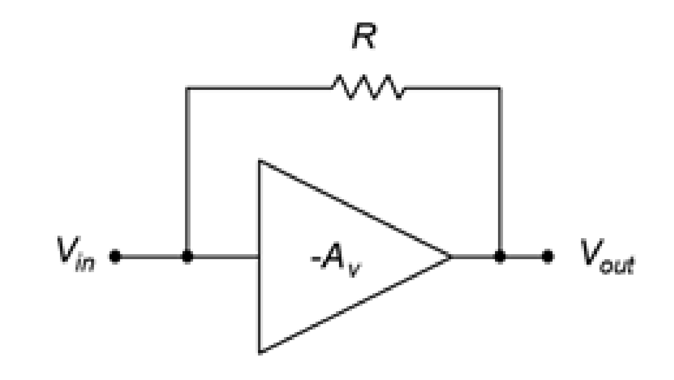


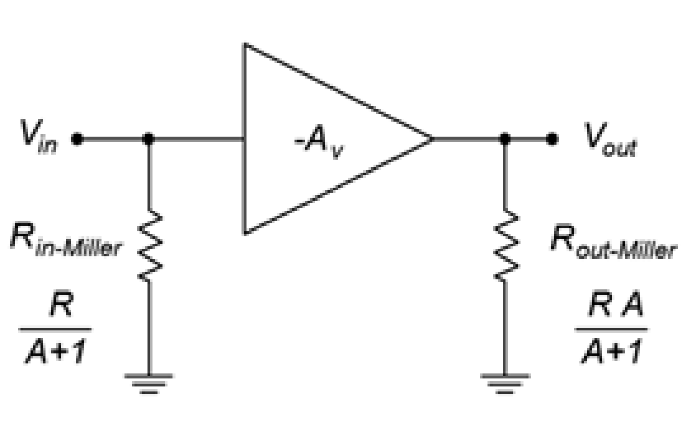
In electronics, the **Miller effect** accounts for the increase in the equivalent input capacitance of an inverting voltage amplifier due to amplification of the effect of capacitance between the input and output terminals. The virtually increased input capacitance due to the Miller effect is given by

$$C_M = C(1 + A_v)$$

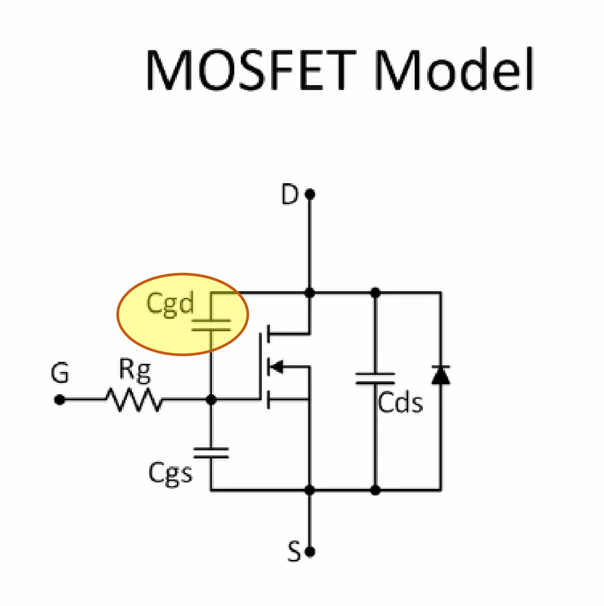
where $-A_v$ is the voltage gain of the inverting amplifier (A_v positive) and C is the feedback capacitance.

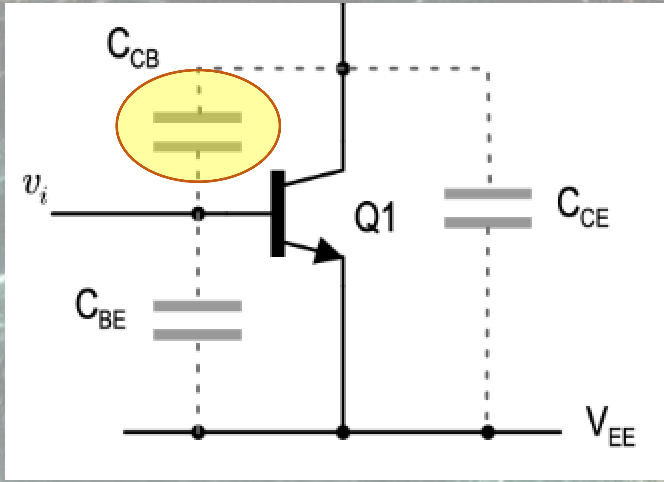
Although the term *Miller effect* normally refers to capacitance, any impedance connected between the input and another node exhibiting gain can modify the amplifier input impedance via this effect. These properties of the Miller effect are generalized in the Miller theorem.





MILLER CAPACITANCE

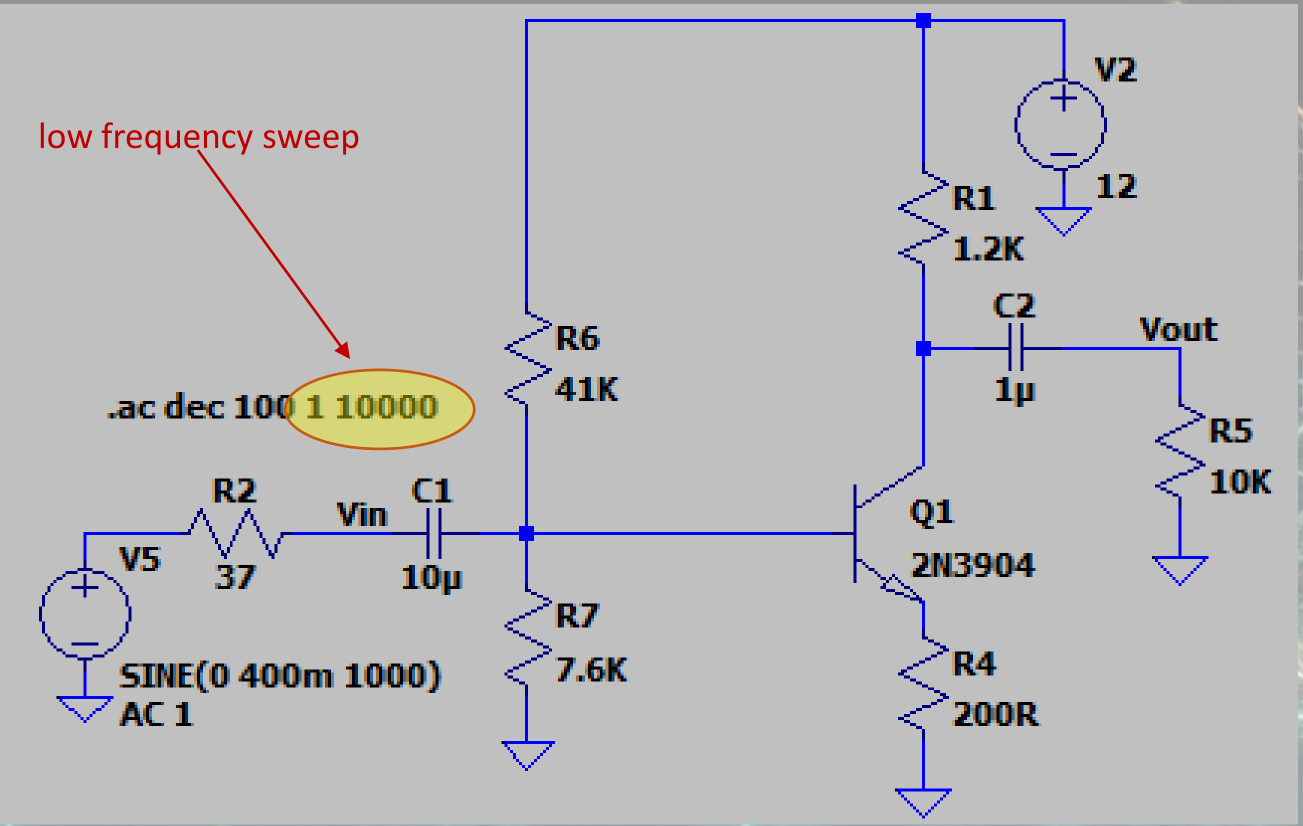


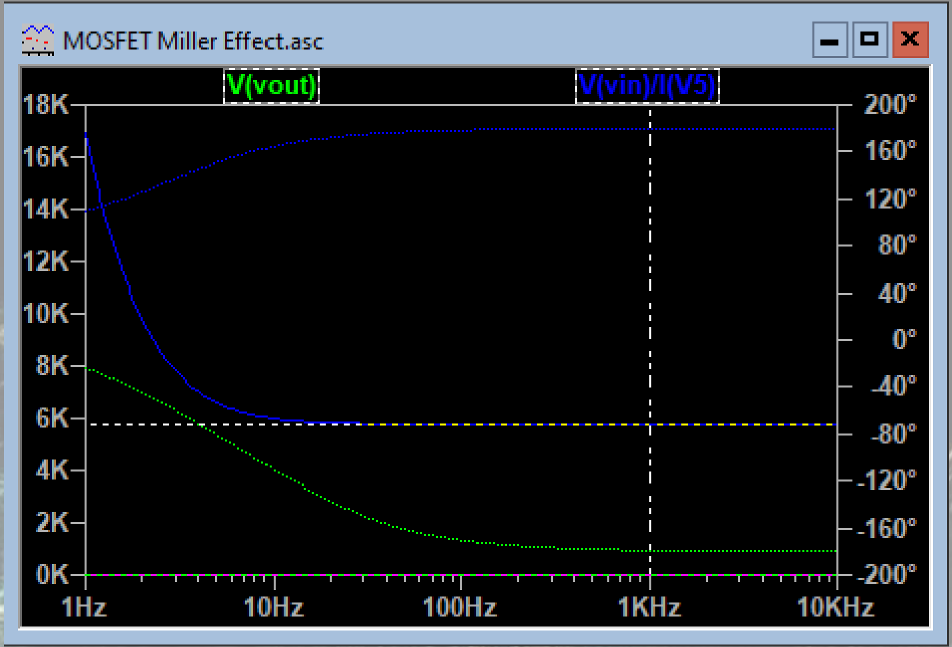


Miller Impedance Calculations

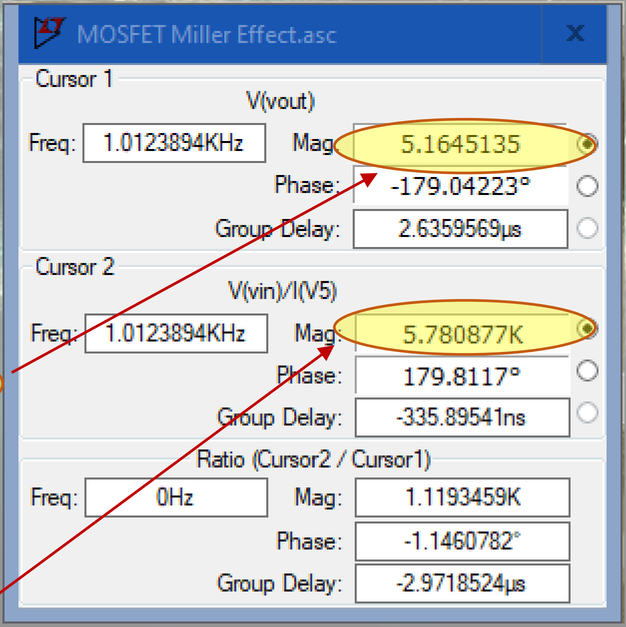
John Milton Miller

NO MILLER EFFECT: 2N3904

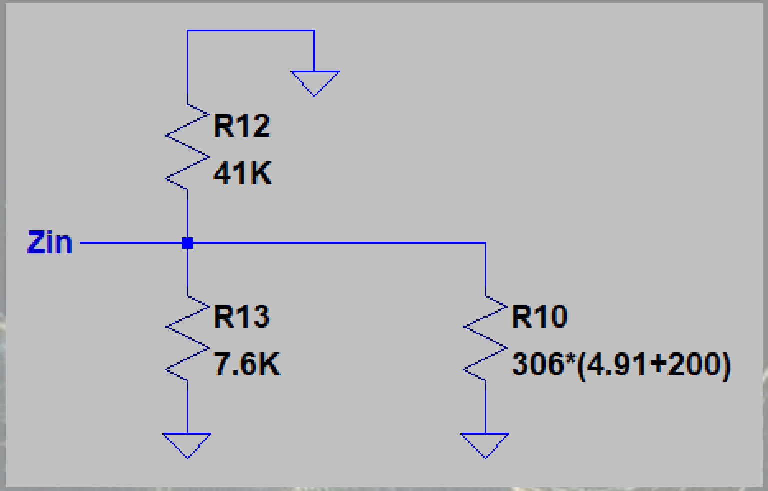




Calculated	
Beta	306
re	4.91
rc	1071
re+re'	205
Av	5.2
Zin	5817
Zmiller	0
Zin	5817



NO MILLER EFFECT: MATH



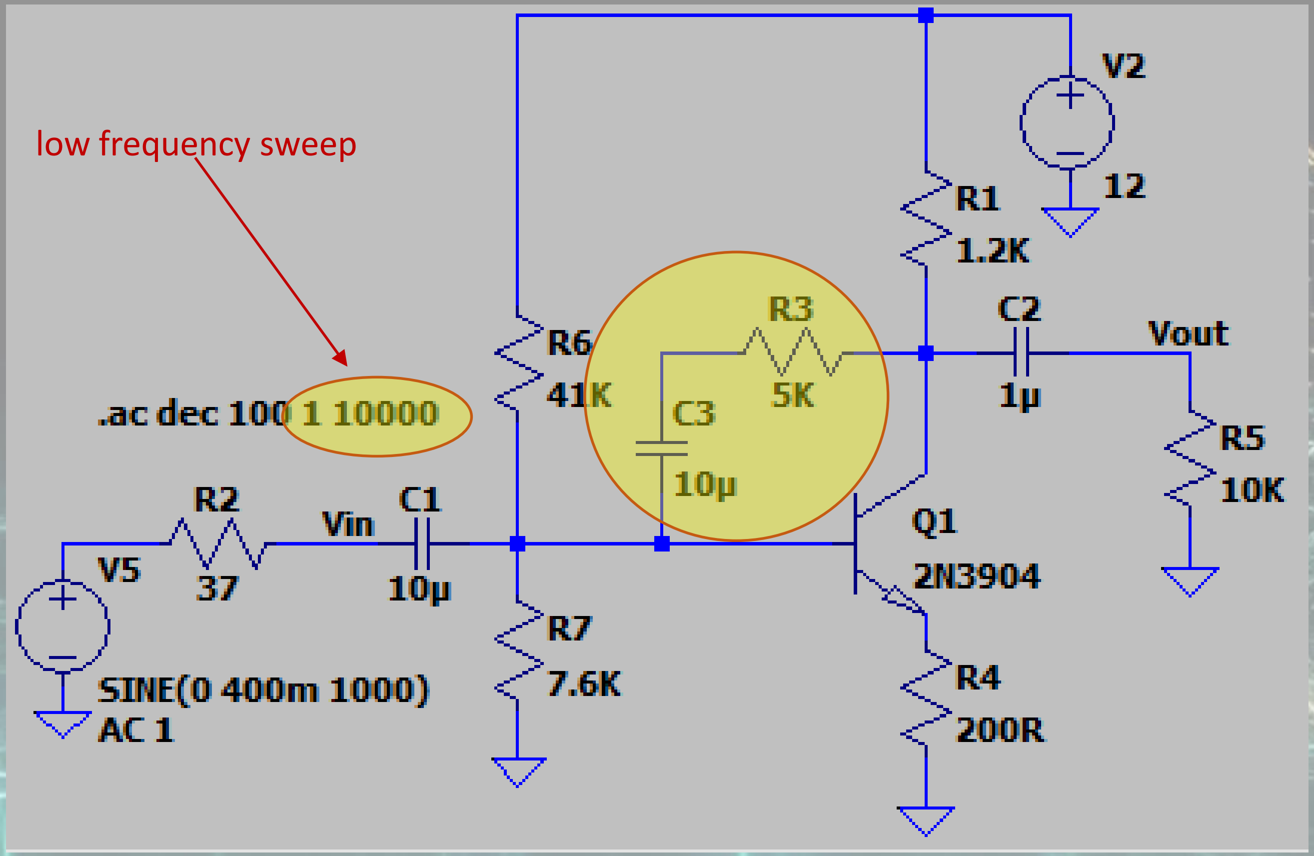
For low frequency, input impedance:

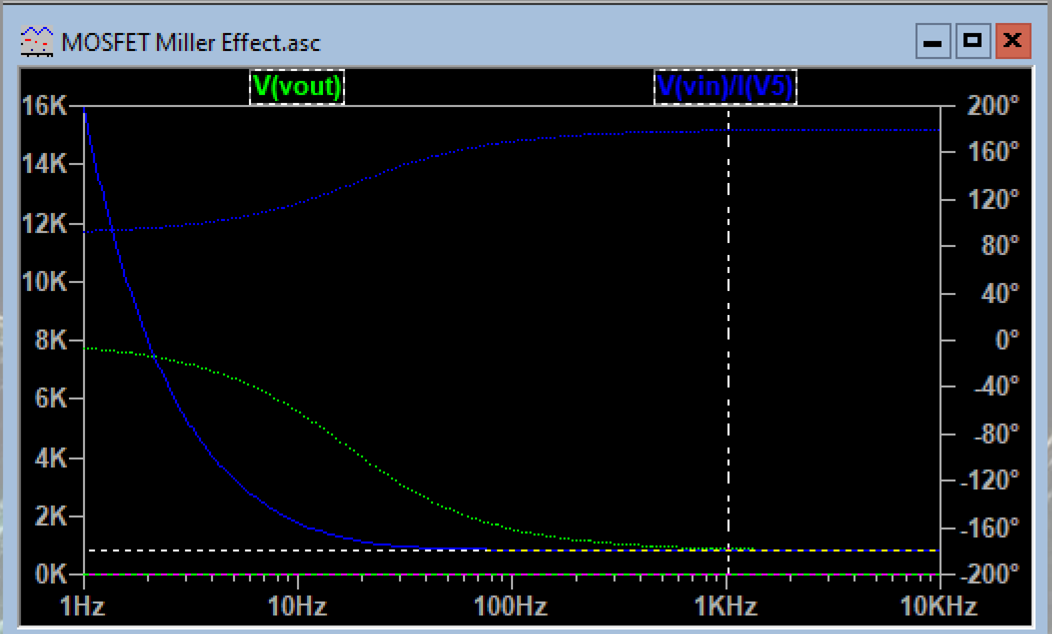
1. Ground all DC sources
   - For BJT, re = Vt/Ic (intrinsic resistance from base to emitter)
   - For BJT we calculate Rin = Beta * (re + Re) which is grounded
   - For MOSFET@Saturation, its removed due to high input impedance
2. Short all DC blocking capacitors (i.e., large value caps)
3. We take a parallel combination of all resistors
   - At low frequencies, we can ignore Miller Capacitance to ground. At RF frequencies we need to account for Miller Capacitance

$1/Zin = 1/41K + 1/7.6K + 1/62744 = 0.00172$

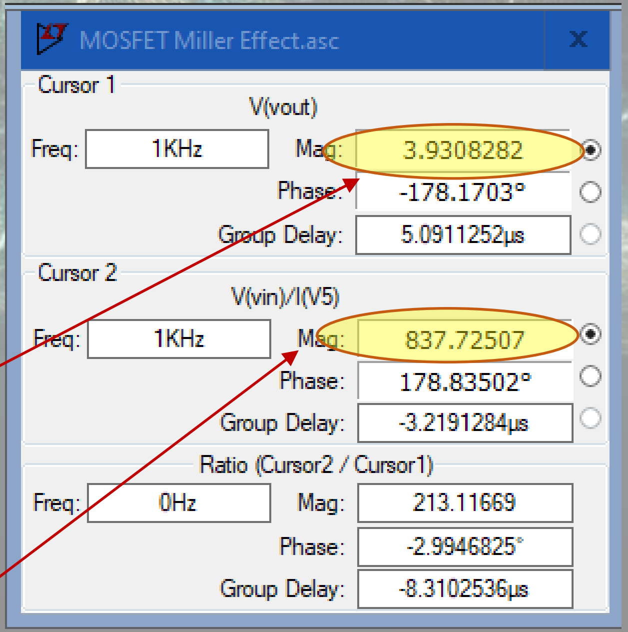
$Zin = 5817$

MILLER EFFECT: Z 2N3904





Calculated	
Beta	306
re	4.91
rc	882
re+re'	205
Av	4.3
Zin	5817
Zmiller	942
Zin	811

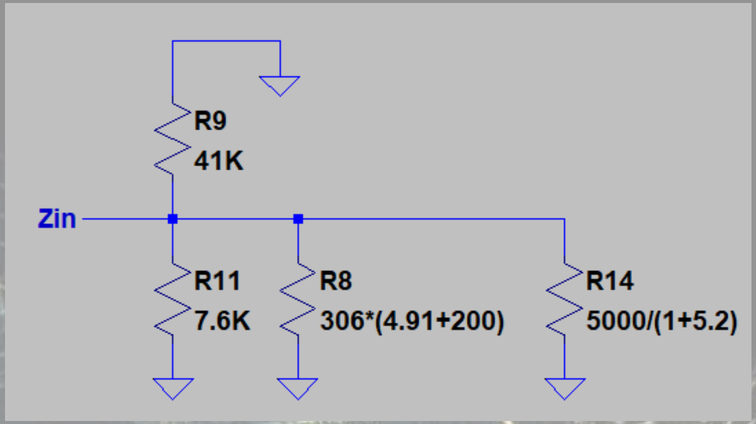


At low frequencies,
"Intrinsic" Capacitance" is negligible.
C3 is DC Blocker

MILLER EFFECT: Z MATH

For low frequency, input impedance:

1. Ground all DC sources
   - For BJT, re = Vt/Ic (intrinsic resistance from base to emitter)
   - For BJT we calculate Rin = Beta * (re + Re) which is grounded
   - For MOSFET, its removed because it has very high input impedance
2. Short all DC blocking capacitors (i.e., large value caps)
3. Need to add Miller Impedance to ground Rmiller = Zfeedback/(1+A)
4. We take a parallel combination of all resistors
   - At low frequencies, we can ignore Miller Capacitance to ground. At RF frequencies we need to account for Miller Capacitance



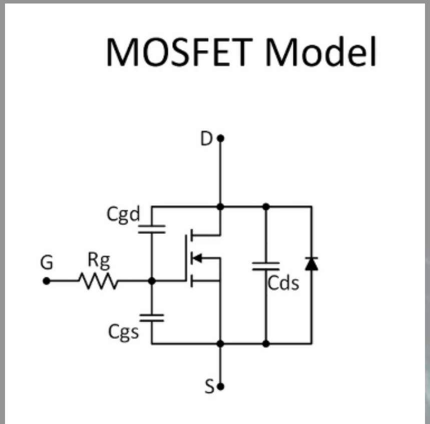
$$1/Zin = 1/41K + 1/7.6K + 1/62744 + 1/942 = 0.001233$$

$$Zin = 811$$

Miller Capacitance Calculations

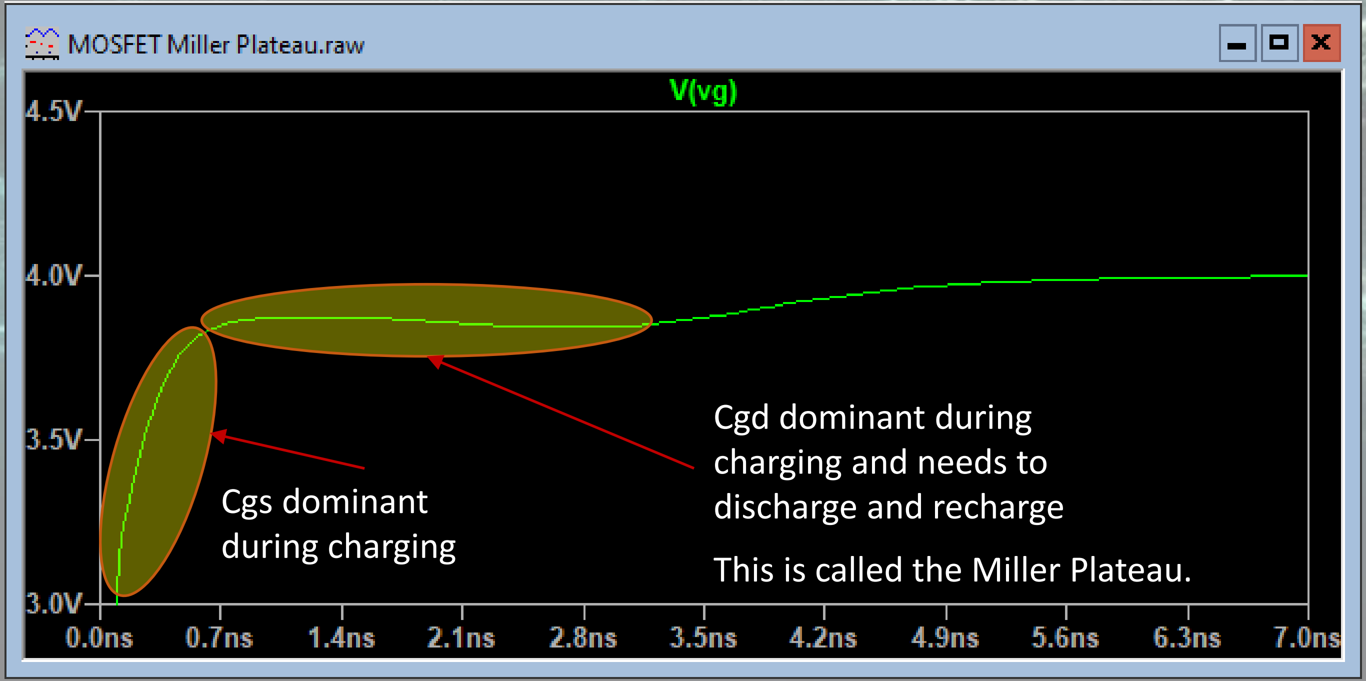
John Milton Miller

MILLER CAPACITANCE



1. *Without any feedback network*, internal MOSFET capacitors take time to charge especially if current is limited (i.e., the R in RC time constant)

2. Cgs charges, Cgd needs to discharge, then Cgd needs to recharge.

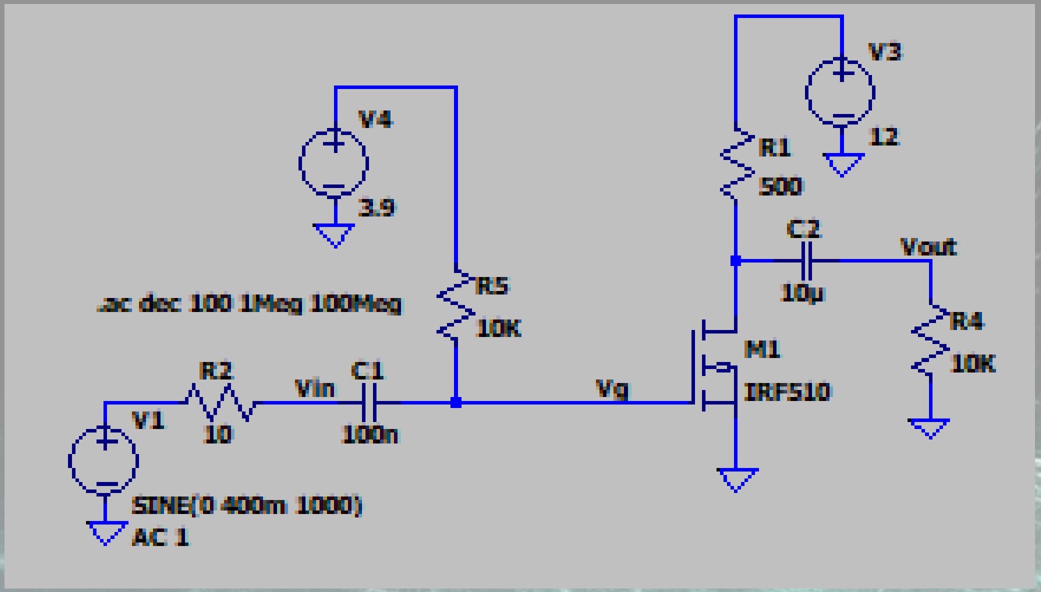


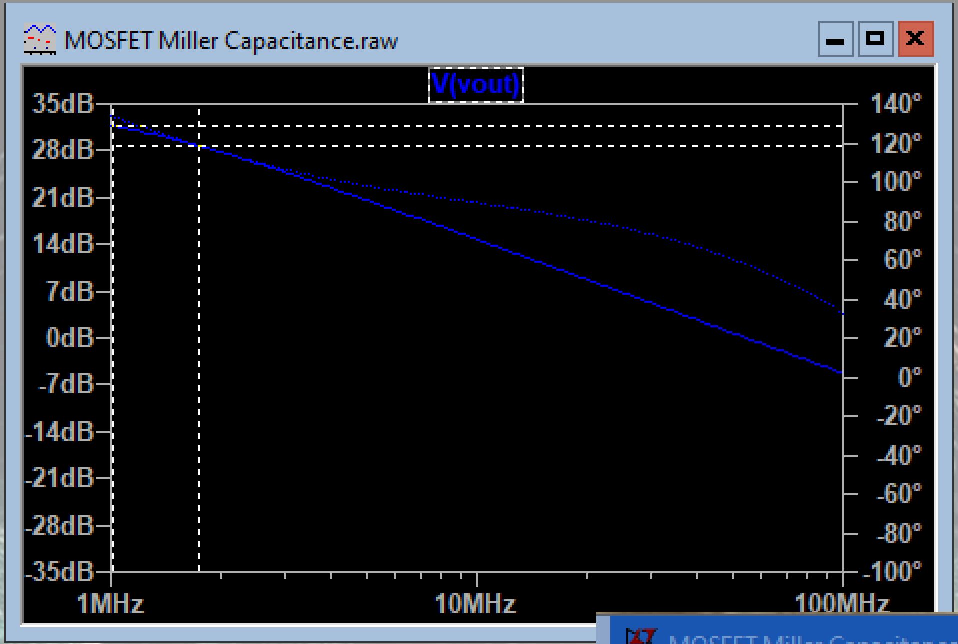
1. Cgd is dominant and charges much slowly. This is called the Miller Plateau.

2. Once Cgd is discharges, Vgs can continue to rise as Cgs recharge. Vgs is allowed to reach full voltage.

Need time or current for capacitors to charge!

MILLER EFFECT: C IR510





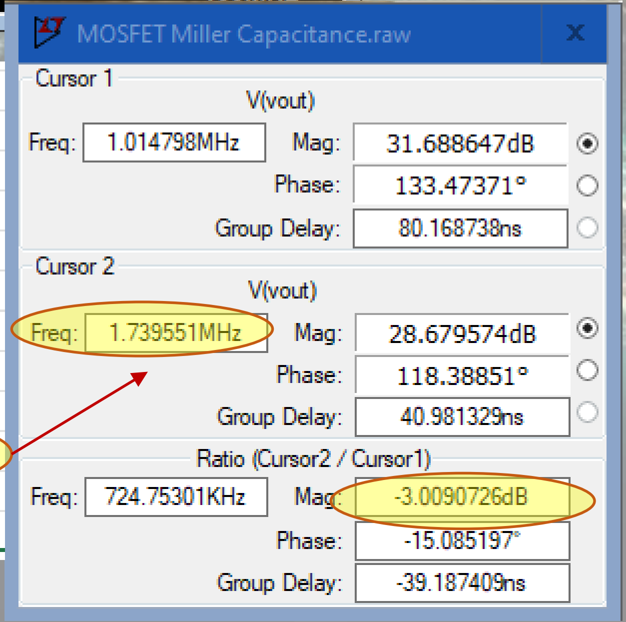
Circuit (DataSheet)		
Rbias	10000	
Rd	500	
Rs	10	
Rout	10000	
Cgd	15	pF
Cgs	165	pF
Cfb	0	pF

Calculated	
Cmiller	615
Cin	780
Rin	10

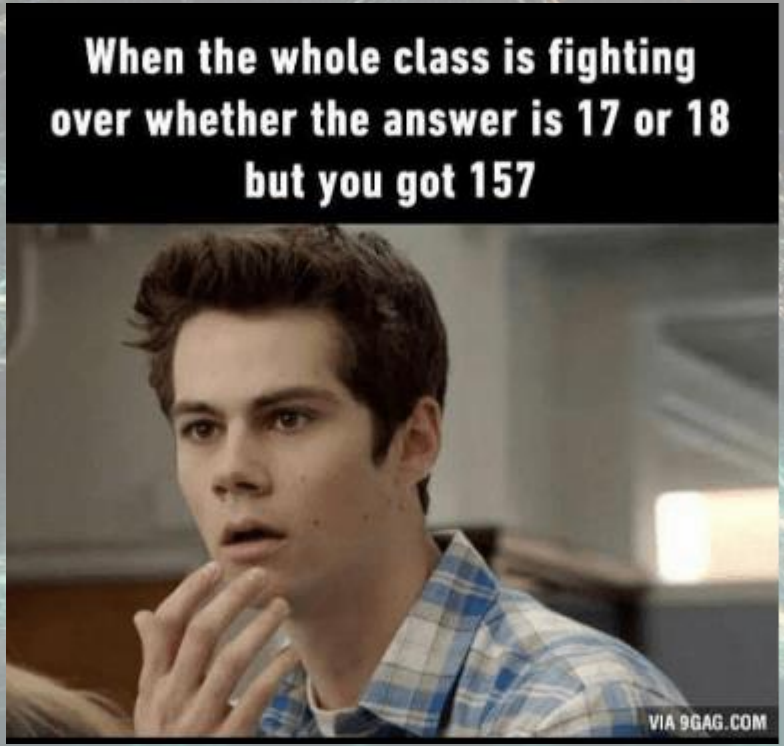
IRF510 Datasheet

Measured	
Av	40.0
Zin	25.0

Fc	20.833



WTF?!


When the whole class is fighting over whether the answer is 17 or 18 but you got 157
VIA 9GAG.COM

LTSPICE MODELS: Trustworthy?

Dynamic							
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	180	-	pF
Output capacitance	C_{oss}			-	81	-	
Reverse transfer capacitance	C_{rss}			-	15	-	
Total gate charge	Q_g	V_{GS} = 10 V	I_D = 5.6 A, V_{DS} = 80 V V_{DS} = 10 V, see fig. 6 and fig. 13 [b]	-	-	8.3	nC
Gate-source charge	Q_{gs}			-	-	2.3	
Gate-drain charge	Q_{gd}			-	-	3.8	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 5.6 A R_g = 24 Ω, R_D = 8.4 Ω, see fig. 10 [b]		-	6.9	-	ns
Rise time	t_r			-	16	-	
Turn-off delay time	$t_{d(off)}$			-	15	-	
Fall time	t_f			-	9.4	-	
Gate input resistance	R_g	f = 1 MHz, open drain		2.5	-	11.6	Ω
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal source inductance	L_S			-	7.5	-	

Datasheet

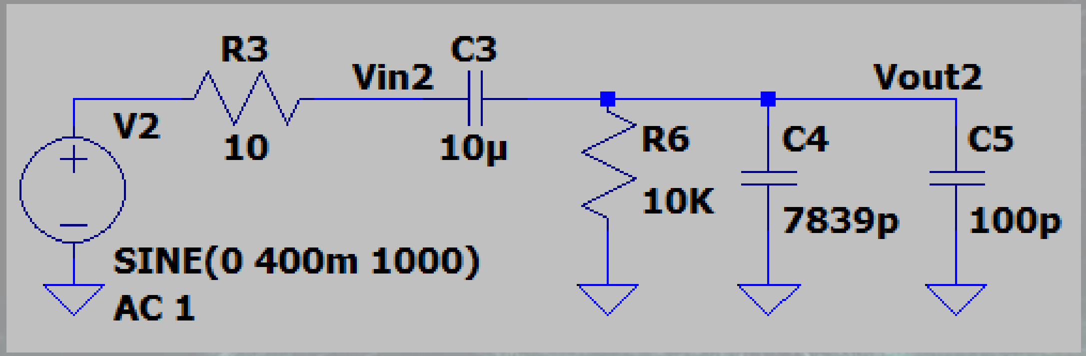
Cgd	15	pF
Cgs	165	pF

LTSpice (.op Analysis)

Name:	m1
Model:	irf510
Id:	1.18e-02
Vgs:	3.90e+00
Vds:	6.10e+00
Vth:	3.80e+00
Gm:	1.32e-01
Gds:	1.11e-04
Cgs:	1.00e-10
Cgd:	1.17e-10
Cbody:	6.38e-11

```
.model mosfet NMOS(VTO=1.899 RS=0.15519 KP=3.91 RD=0.1943 TC1RD=0.0231 RG=45.199 IS=1e-36
+ CGDMAX=7.40E-10 CGDMIN=1.00E-11 XG2CGD=1.6 XG1CGD=0.1 CBD=6.92E-11 VTCGD=0.2)
.model diode D( IS=2.61e-13 RS=0.0407 TT=1.614e-07)
```

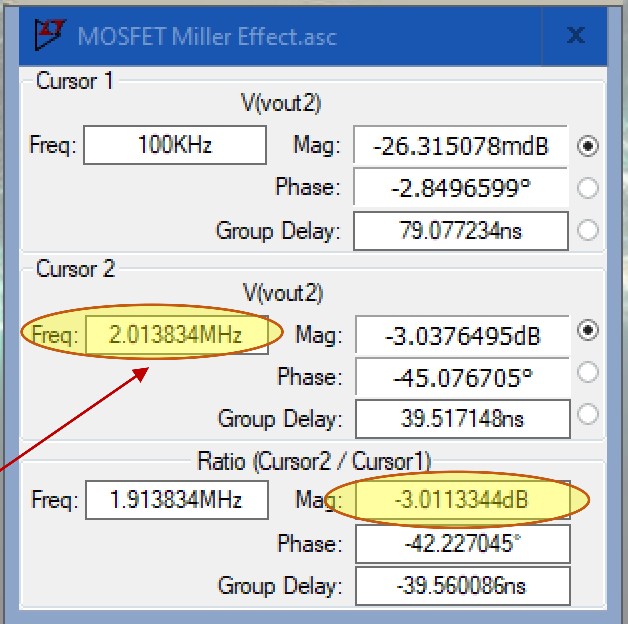
MILLER EFFECT: C IR510



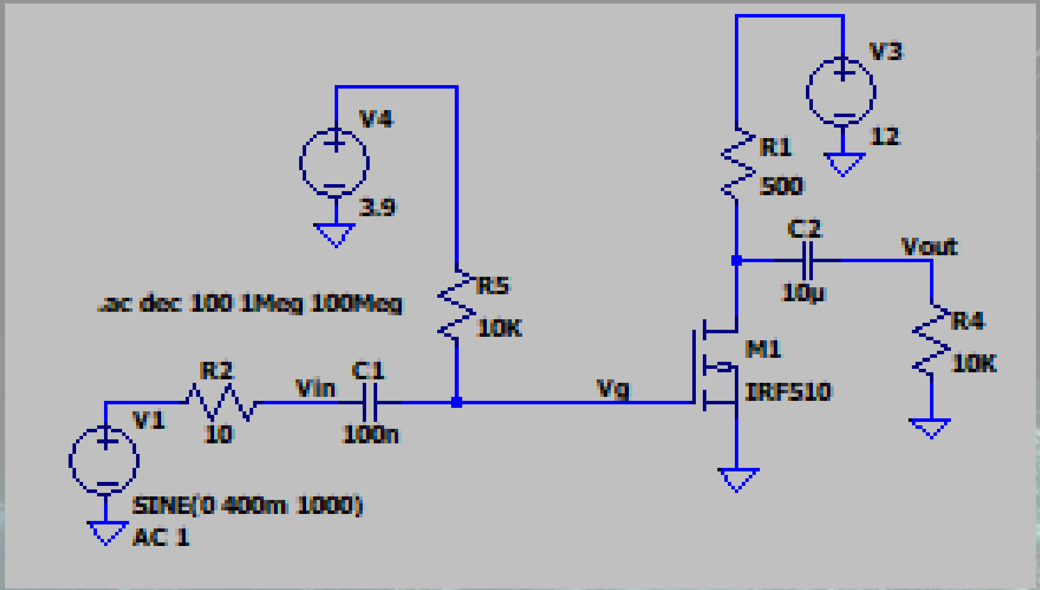
Simplified AC Model

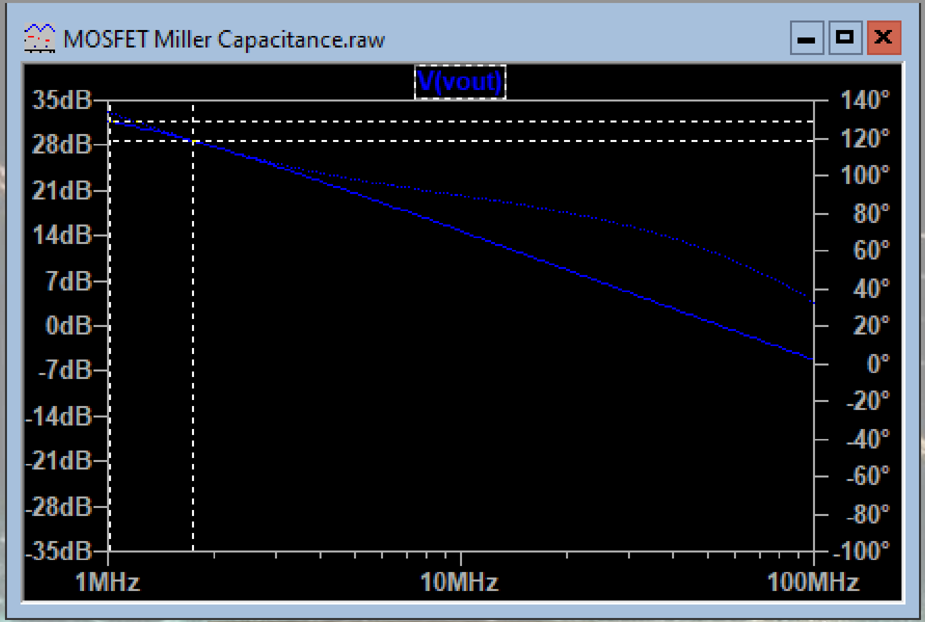
LTSpice Model

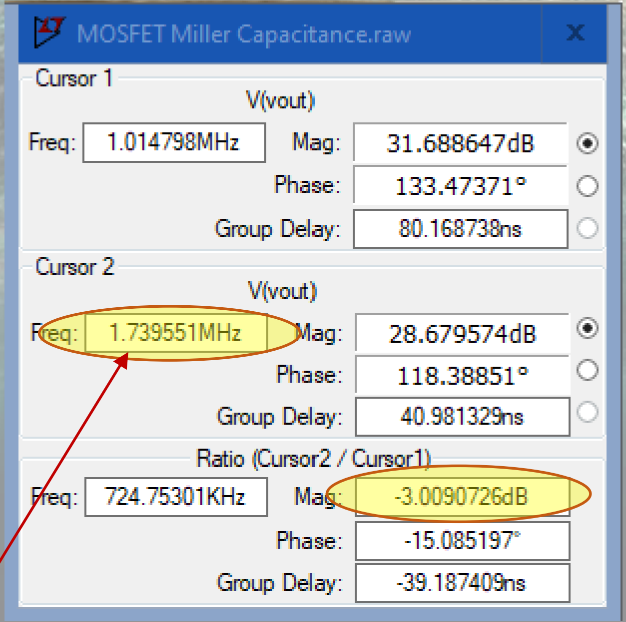
Circuit (LTSpice)			Calculated	
Rbias	10000			
Rd	500			
Rs	10		Gm	0.132
Rout	10000		Av	66
Cgd	117	pF	Cmiller	7839
Cgs	100	pF	Cin	7939
Cfb	0	pF	Rin	10
			Fc	2.047



MILLER EFFECT: C IRF510





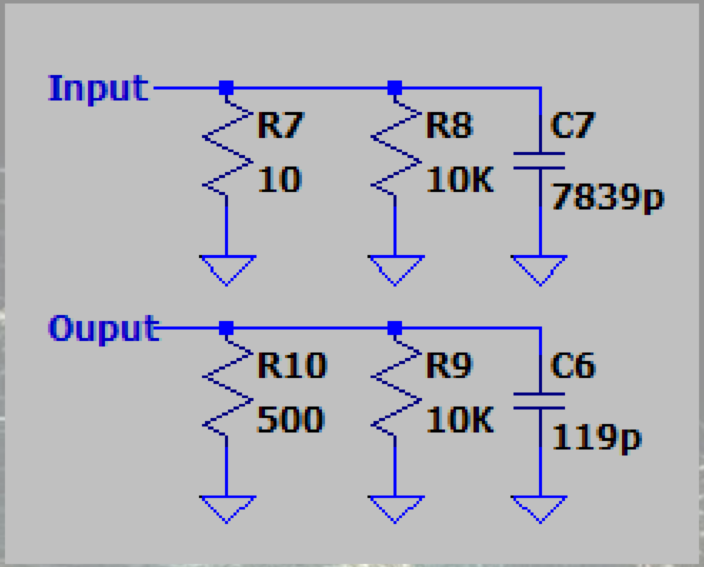


Circuit (LTSpice)				Calculated	
Rbias	10000				
Rd	500				
Rs	10			Gm	0.132
Rout	10000			Av	66
Cgd	117	pF		Cmiller	7839
Cgs	100	pF		Cin	7939
Cfb	0	pF		Rin	10
				Fc	2.047

MILLER EFFECT: C MATH

For RF frequency, high 3dB cutoff:

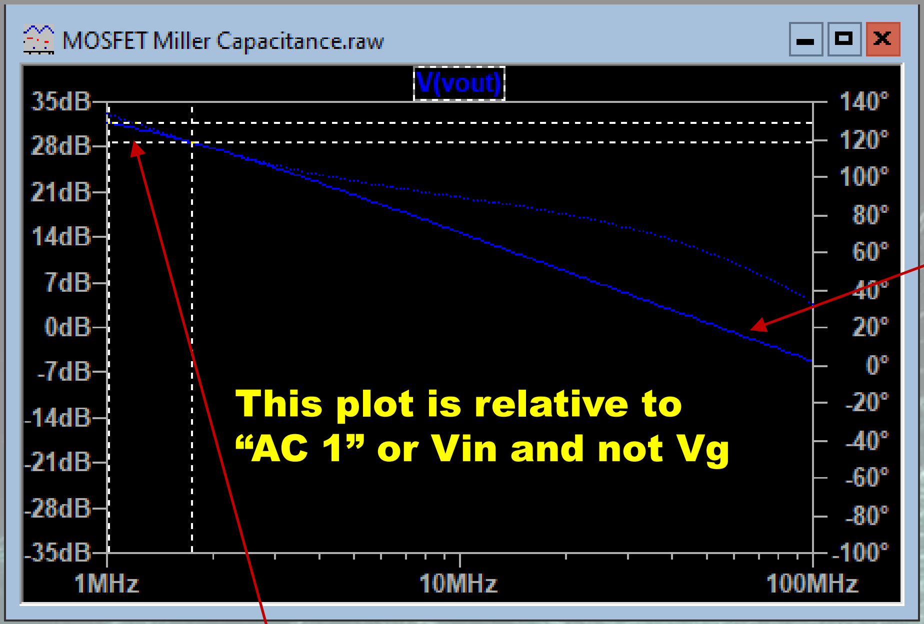
1. Ground all DC sources
   - For BJT, re = Vt/Ic (intrinsic resistance from base to emitter)
   - For BJT we calculate Rin = Beta * (re + Re) which is grounded
   - For MOSFET, its removed because it has very high input impedance
2. Short all DC blocking capacitors (i.e., large value caps)
3. Need to add Miller Capacitance to ground
   - Input: Cmiller_in = Cgd*(1+A) ***where A is gain <u>without</u> feedback***
   - Output: Cmiller_out = Cgd*(1+A) /A
4. Calculate input resistance including source resistance
   - For MOSFET Rin= 1/(1/Rb+1/Rs)
   - For BJT Rin = 1/[1/Rb1+1/Rb2+1/Rs+1/(beta*(Re+re))]
5. Calculate Output resistance including load resistance
   - For MOSFET Rout= 1/(1/Rd+1/Rl)
   - For BJT Rin = 1/[1/Rc+1/Rc+1/Re]
6. Calculate 3dB Frequency at input and output using
   - Rin and Cmiller_in for input Fc=1/(2*pie*Rin*Cmiller_in)
   - Rout and Cmiller_out for input Fc=1/(2*pie*Rout*Cmiller_out)



Fc1= 1/(2*3.14*10*7839pF)= 2.047 MHz

Fc2 = 1/(2*3.14*476*119pF)= 2.814 MHz

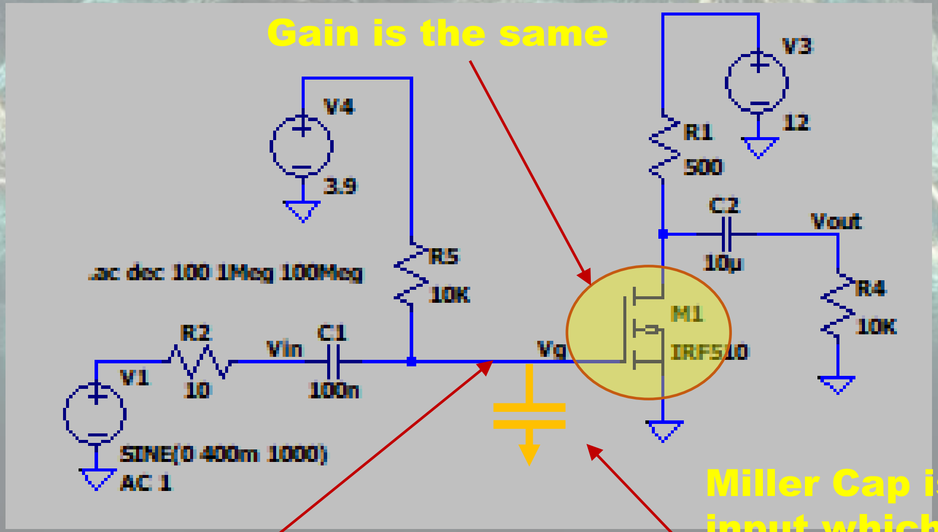
Wrap your head around this....



This is NOT the actual gain.

This is and ALWAYS will be the gain (maybe larger at lower frequencies)

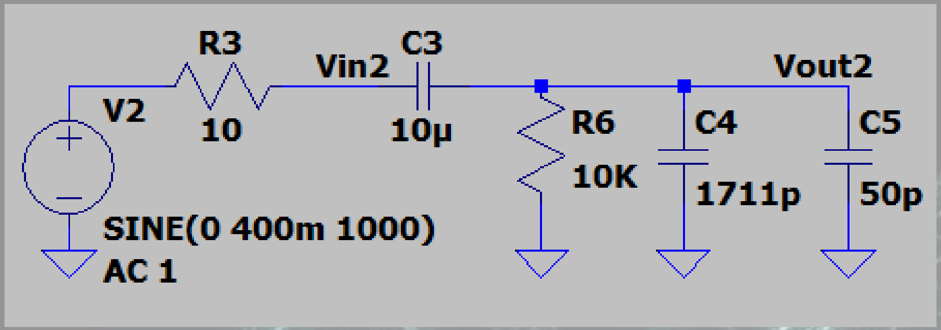
Gain is the same

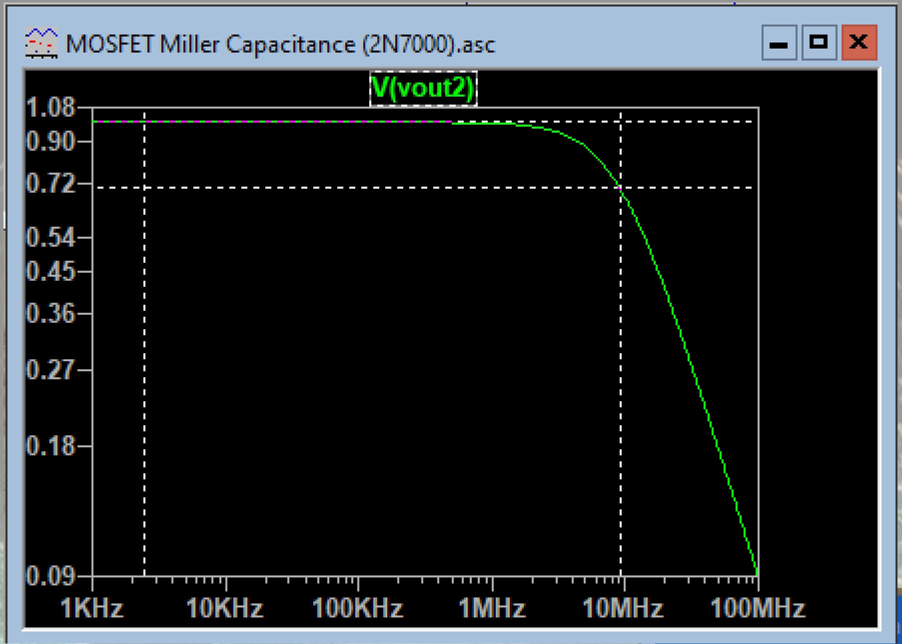


Miller Cap is causing lower input which is subjected to same gain at low frequency

Vin is shorted to ground

MILLER EFFECT: C 2N7000



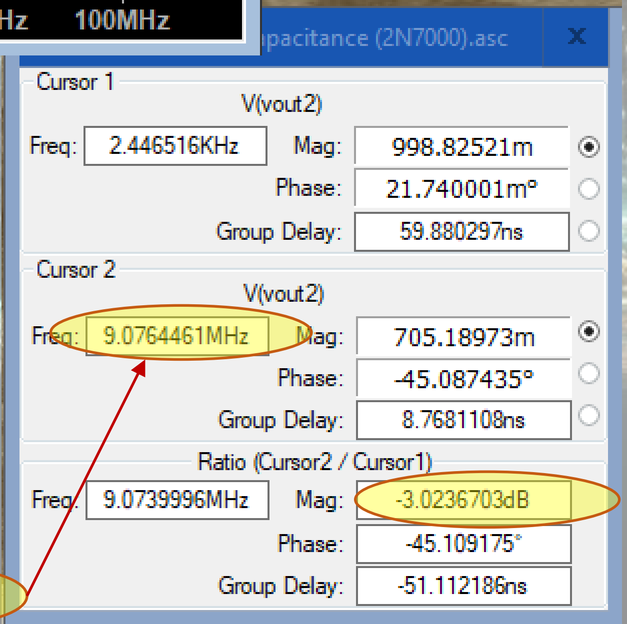


Simplified AC Model

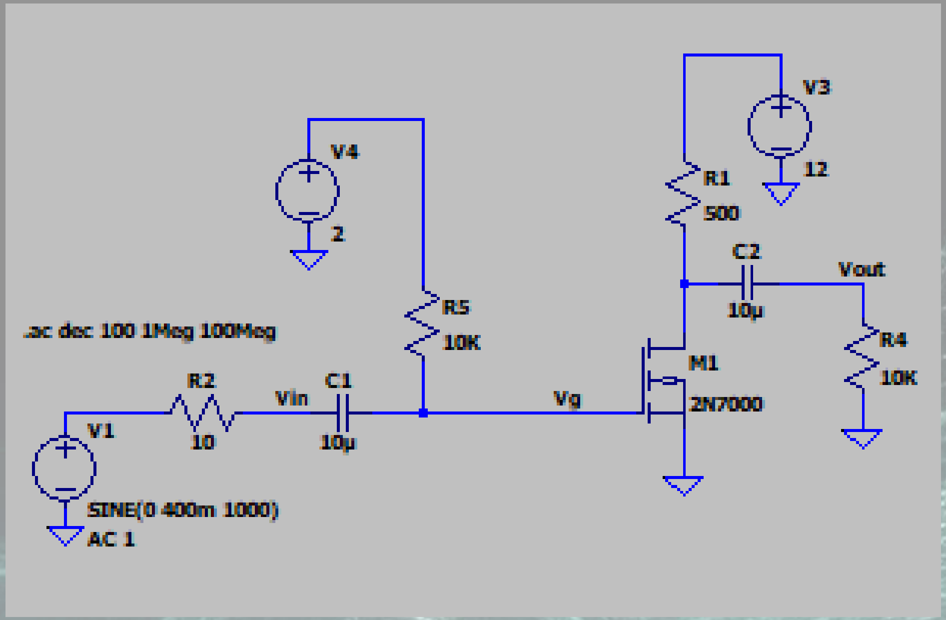
Input -3dB Frequency!!!

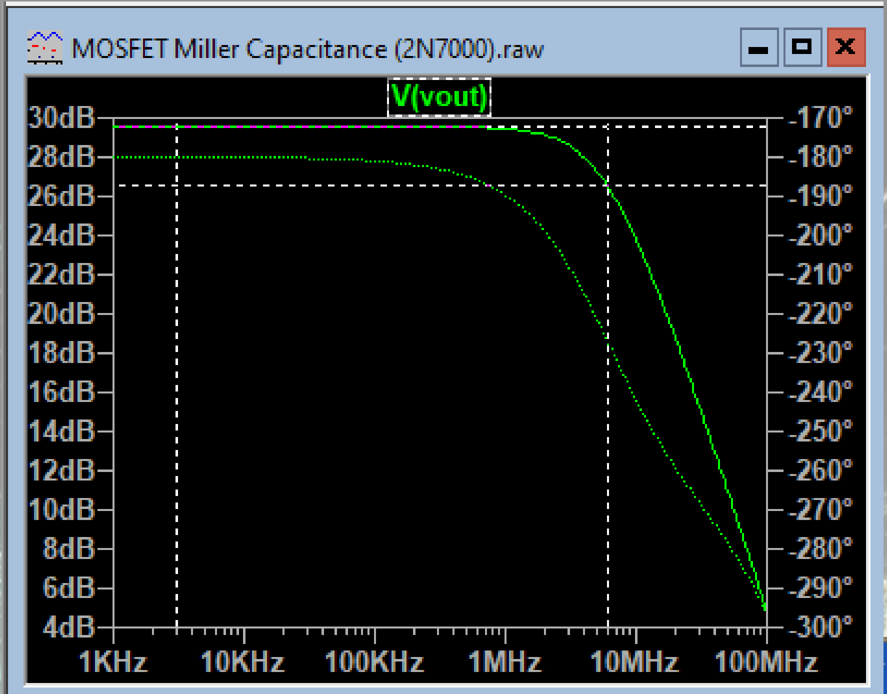
LTSpice Model

Circuit (LTSpice)			Calculated	
Rbias	10000			
Rd	500			
Rs	10		Gm	0.083
Rl	10000		Av	30
Rout	10000	pF	CmillerIn	1711
Cin	1000000	pF	Cin	1761
Cout	1000000	pF	Rin	10
Cgd	56.1	pF	CmillerOut	58
Cgs	50	pF	Rout	476
Cfb	0			
			Fhi	9.047



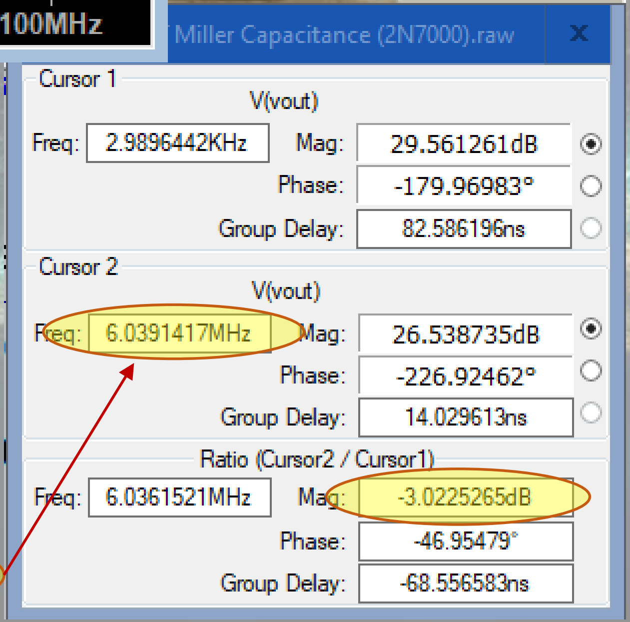
MILLER EFFECT: C 2N7000





Circuit (LTSpice)			Calculated	
Rbias	10000			
Rd	500			
Rs	10		Gm	0.083
Rl	10000		Av	30
Rout	10000	pF	CmillerIn	1711
Cin	1000000	pF	Cin	1761
Cout	1000000	pF	Rin	10
Cgd	56.1	pF	CmillerOut	58
Cgs	50	pF	Rout	476
Cfb	0			
			Fhi	9.047
			Fho	5.762

LTSpice Model



The universe makes more sense now....

1. **Observed: Due to the internal capacitors, the MOSFET is frequency dependant. At high frequencies, the input impedance is reduced (almost short circuit)**

2. **The time for the MOSFET to turn on completely is dependent on the Cgs and Cgd capacitors to charge**

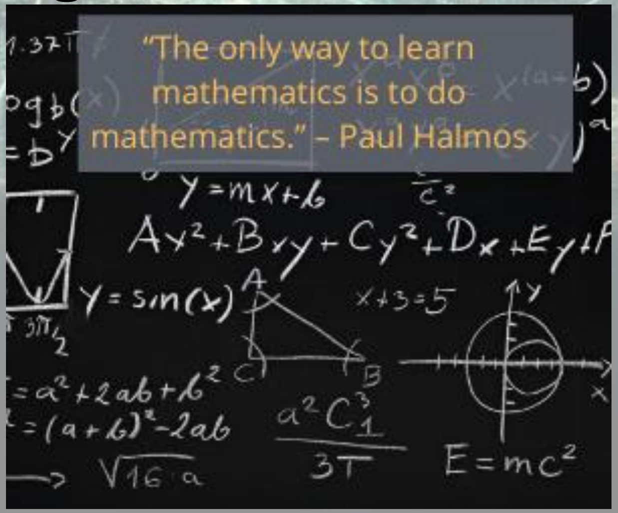
3. **The Miller Effect causes any Feedback Impedance of an Inverting Amplified to be shorted to ground and reduced by a factor of the gain**

   Zmiller = R / (1+A)

4. **The Miller Effect caused any Feedback Capacitance of an Inverting Amplifier to be shorted to ground and increased by a factor of the gain**

   Cmiller = C * (1+A)

5. **High gain RF amplifiers will be problematic!**
   - ✓ **Impedance will decrease. Input is shorted.**
   - ✓ **Internal Capacitance will increase. 3dB bandwidth decreases**
   - ✓ **High gain RF amplifiers will be problematic!**



DON’T TRUST “NON-NATIVE” LTSPICE MODELS!!

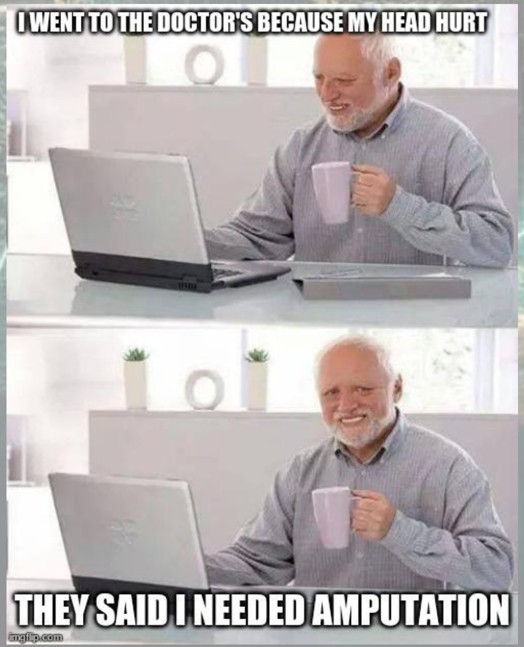
..to be continued

SOAREX GROUP

Addressing the Miller Effect (MOSFETS)

Dave VE3OOI

December 2023



AGENDA

Addressing Miller Effect using the "Scotty Approach"

1. ***Recap***
2. ***Approaches to neutralize Miller Effect***
   - ✓ ***Change amplifier type***
   - ✓ ***Reduce Gain***
   - ✓ ***Change RC Time Constant***

Captain, we need to kick Miller in the bag pipes

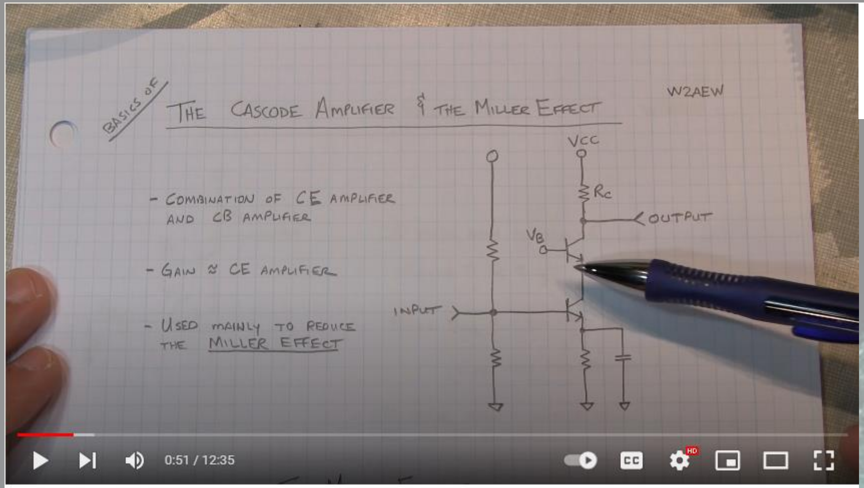
Danger Will Robinson…

Quote Charlie Morris, ZL2CTM:

This NOT a tutorial.

It's a log of my journey. Right or wrong.

REFERENCES

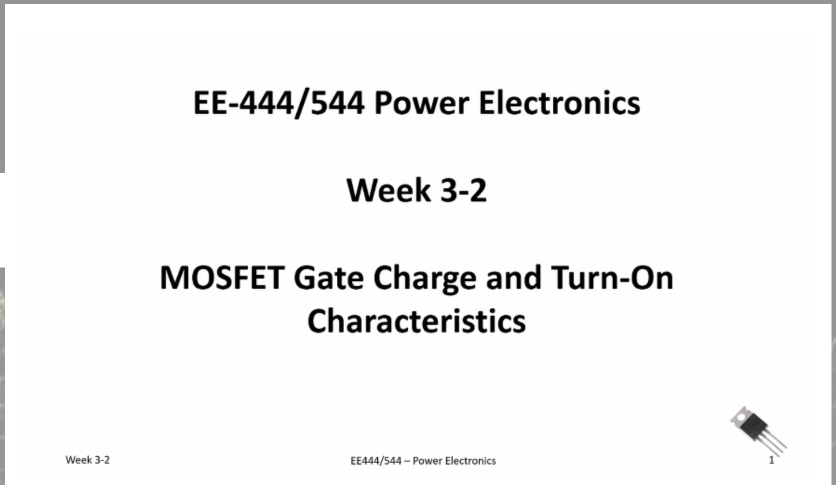


#207: Basics of a Cascode Amplifier and the Miller Effect

w2aew
193K subscribers

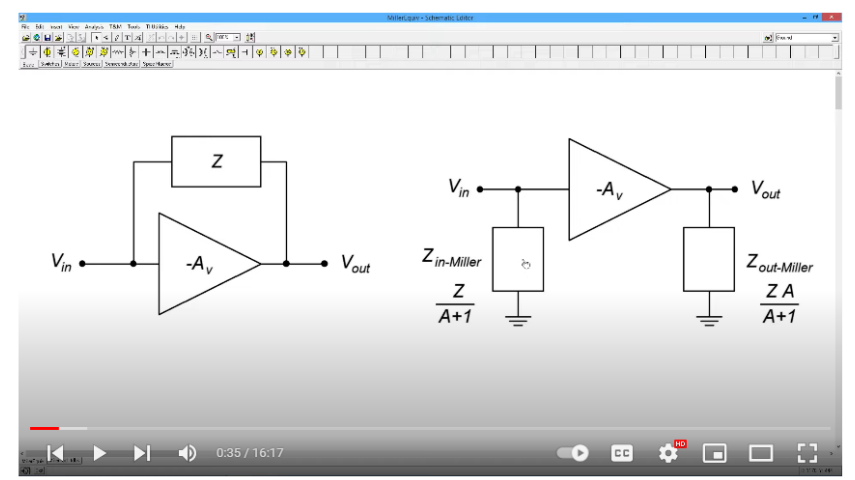
https://youtu.be/Op_I3Ke7px0

Power Electronics with Dr. K
8.37K subscribers



Power Electronics WK3_2 MOSFET Turn On Characteristics

https://youtu.be/f1yt0s3gpcE

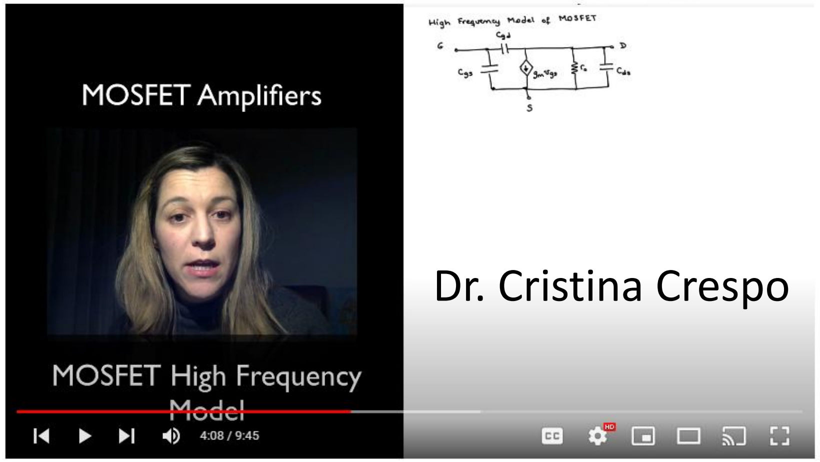


Semiconductor Devices: Miller's Theorem

Electronics with Professor Fiore
7.24K subscribers

https://youtu.be/yM9xlbAf43Q

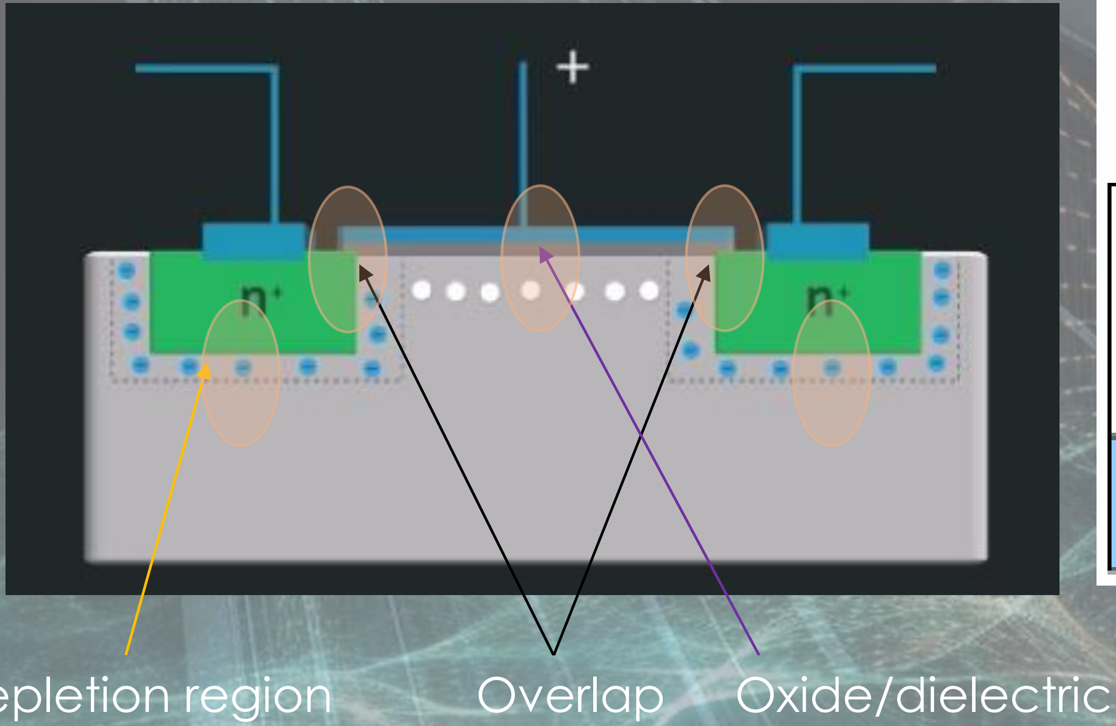
Mateo Aboy
14.2K subscribers

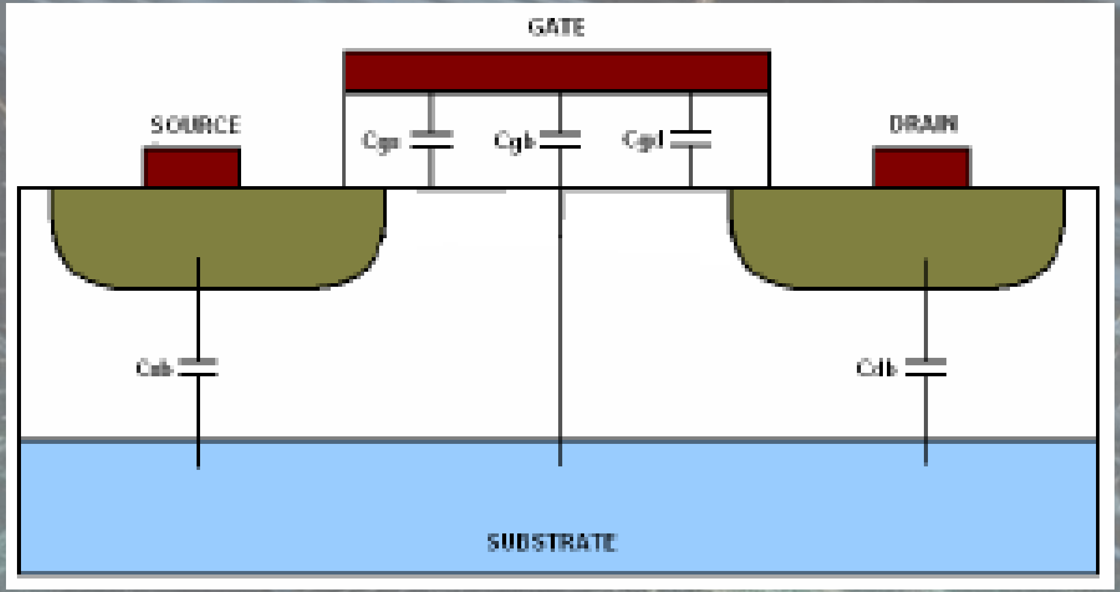


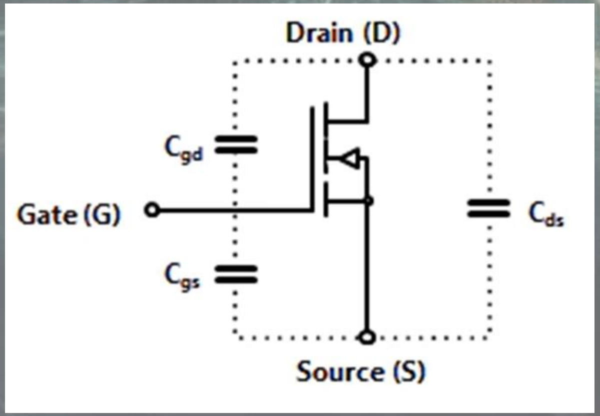
MOSFET High Frequency Model

https://youtu.be/19kXfUPdF9I

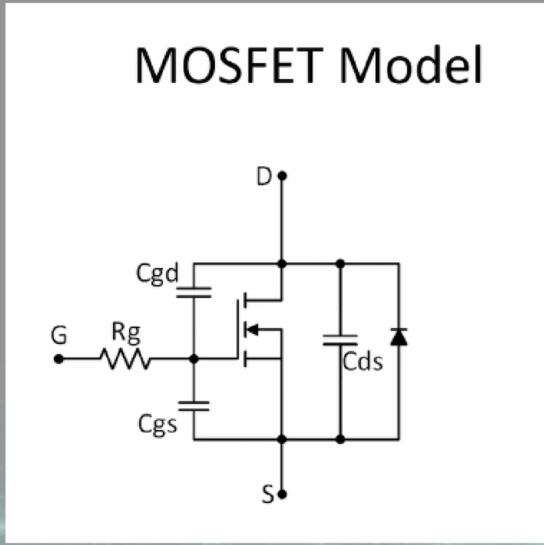
FUNDEMANTALS

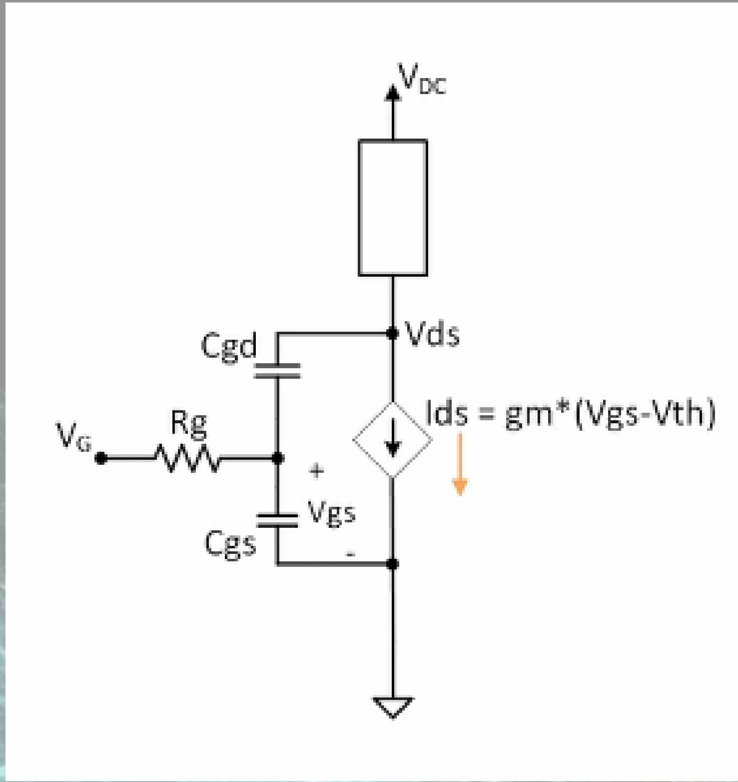


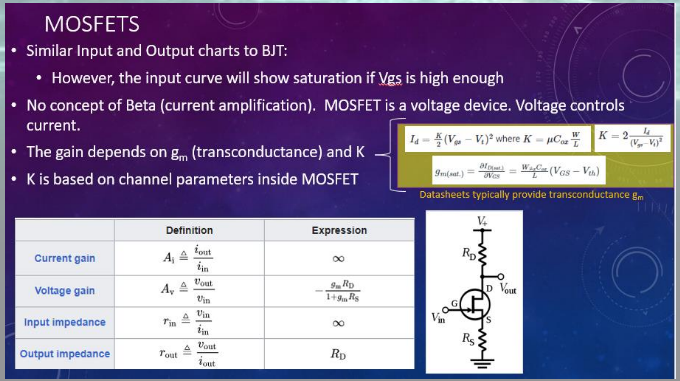




FUNDEMANTALS







MOSFETS

- Similar Input and Output charts to BJT:
  - However, the input curve will show saturation if Vgs is high enough
- No concept of Beta (current amplification). MOSFET is a voltage device. Voltage controls current.
- The gain depends on g_m (transconductance) and K
- K is based on channel parameters inside MOSFET

$I_d = \frac{K}{2}(V_{gs} - V_t)^2$ where $K = \mu C_{ox}\frac{W}{L}$ $K = 2\frac{I_d}{(V_{gs}-V_t)^2}$

$g_{m(sat.)} = \frac{\partial I_{D(sat.)}}{\partial V_{GS}} = \frac{W \mu_s C_{ox}}{L}(V_{GS} - V_{th})$

Datasheets typically provide transconductance g_m

	Definition	Expression
Current gain	$A_i \triangleq \frac{i_{out}}{i_{in}}$	∞
Voltage gain	$A_v \triangleq \frac{v_{out}}{v_{in}}$	$-\frac{g_m R_D}{1+g_m R_S}$
Input impedance	$r_{in} \triangleq \frac{v_{in}}{i_{in}}$	∞
Output impedance	$r_{out} \triangleq \frac{v_{out}}{i_{out}}$	R_D

https://youtu.be/t6_chWRdSyg?si=I5OjAjNdn_JZtLlY

1. **The model of a MOSFET is basically an ideal current source that driven by the gate to source voltage**

2. **When gate voltage is zero, MOSFET is off and Cgd is charged with respect to Vdc.**

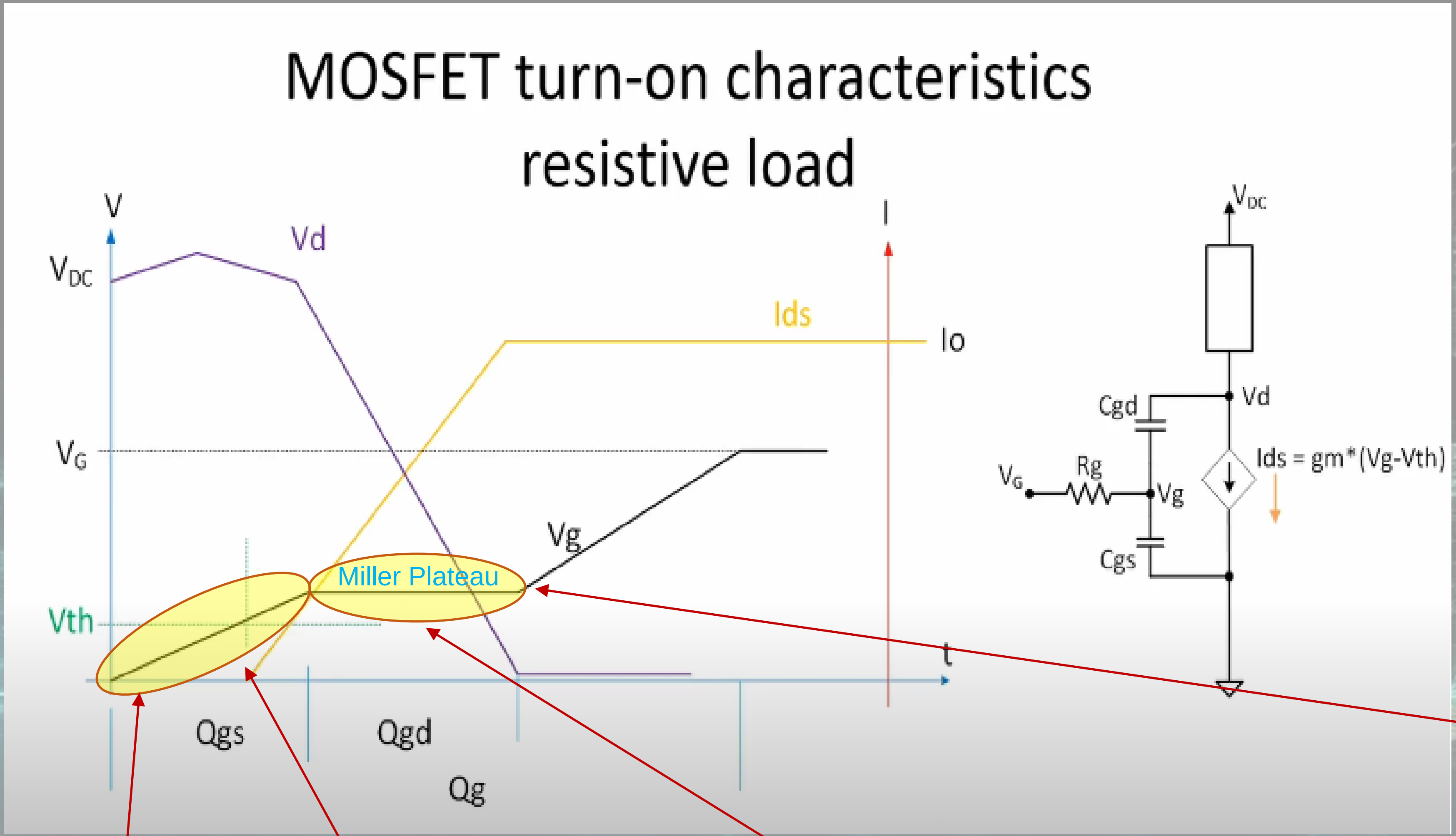
3. **When gate voltage starts to rise (small voltage), all current flows to Cgs and that starts to charge.**

4. **Once Vgs threshold reached, Ids begins to increase and Vds starts to drop. Cgd starts to discharge.**

5. **Once Ids reaches maximum, then Vds is close to zero and Cgd is discharged. As Vgs increases, Cgd now charges with opposite polarity. Once Cgd is fully charged, the MOSFET is on.**

6. **The time for the MOSFET to turn on is from charge time of BOTH Cgs and Cgd. This is critical for MOSFET as a switch (e.g. buck converter)**

MILLER CAPACITANCE: THEORY



Cgd & Cgs Almost Fully Charged

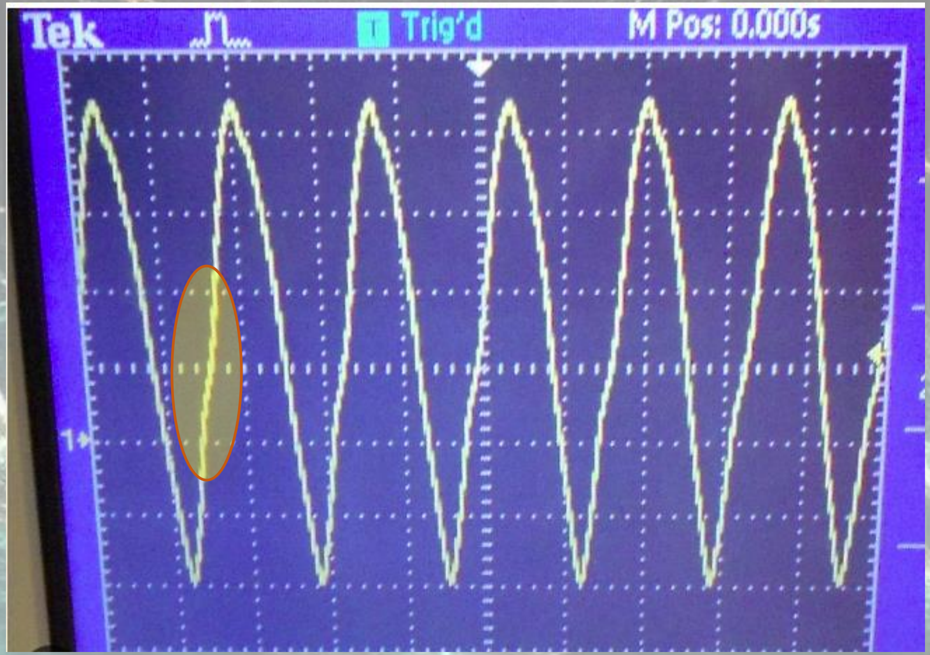
Max Current and Zero Voltage drop

Cgs Charging

MOSFET Threshold Voltage

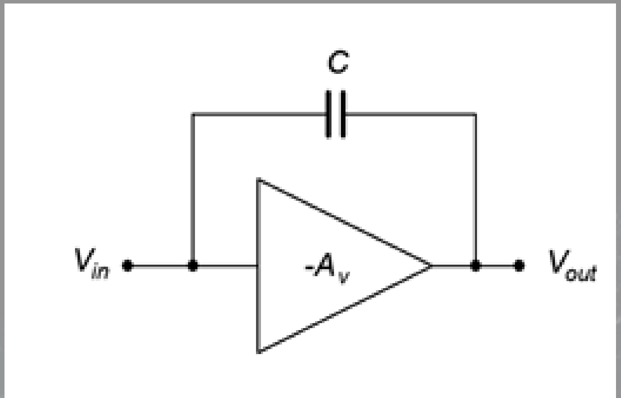
Cgd Discharging (After Vd Drops)

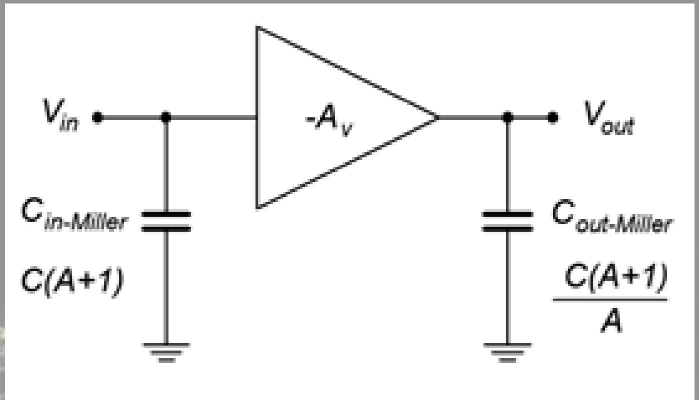
MILLER "DISTORTION"



This has been exaggerated for illustration purposes

MILLER EFFECT/THEOREM



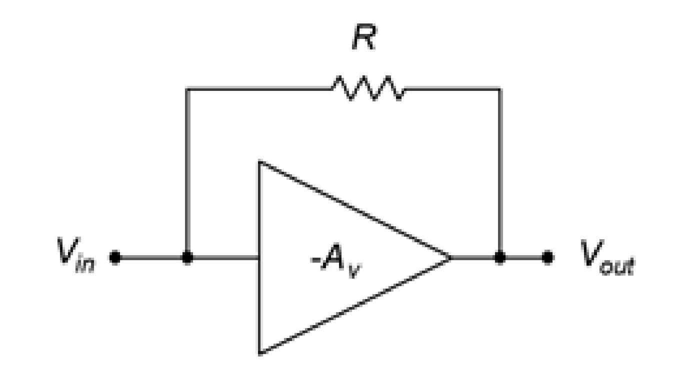


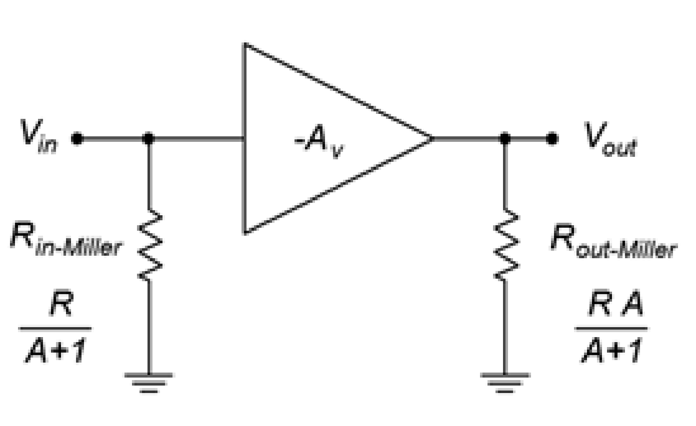
In electronics, the **Miller effect** accounts for the increase in the equivalent input capacitance of an inverting voltage amplifier due to amplification of the effect of capacitance between the input and output terminals. The virtually increased input capacitance due to the Miller effect is given by

$$C_M = C(1 + A_v)$$

where $-A_v$ is the voltage gain of the inverting amplifier (A_v positive) and C is the feedback capacitance.

Although the term *Miller effect* normally refers to capacitance, any impedance connected between the input and another node exhibiting gain can modify the amplifier input impedance via this effect. These properties of the Miller effect are generalized in the Miller theorem.





Miller Neutralization: Kick in Bag Pipes

1. **Reduce the gain hence reduce Miller Capacitance**
   - ✓ **Use HYCAS or *CASCODE* amplifiers. Add common base, common gate stage**
   - ✓ ***Negative feedback***

SAME

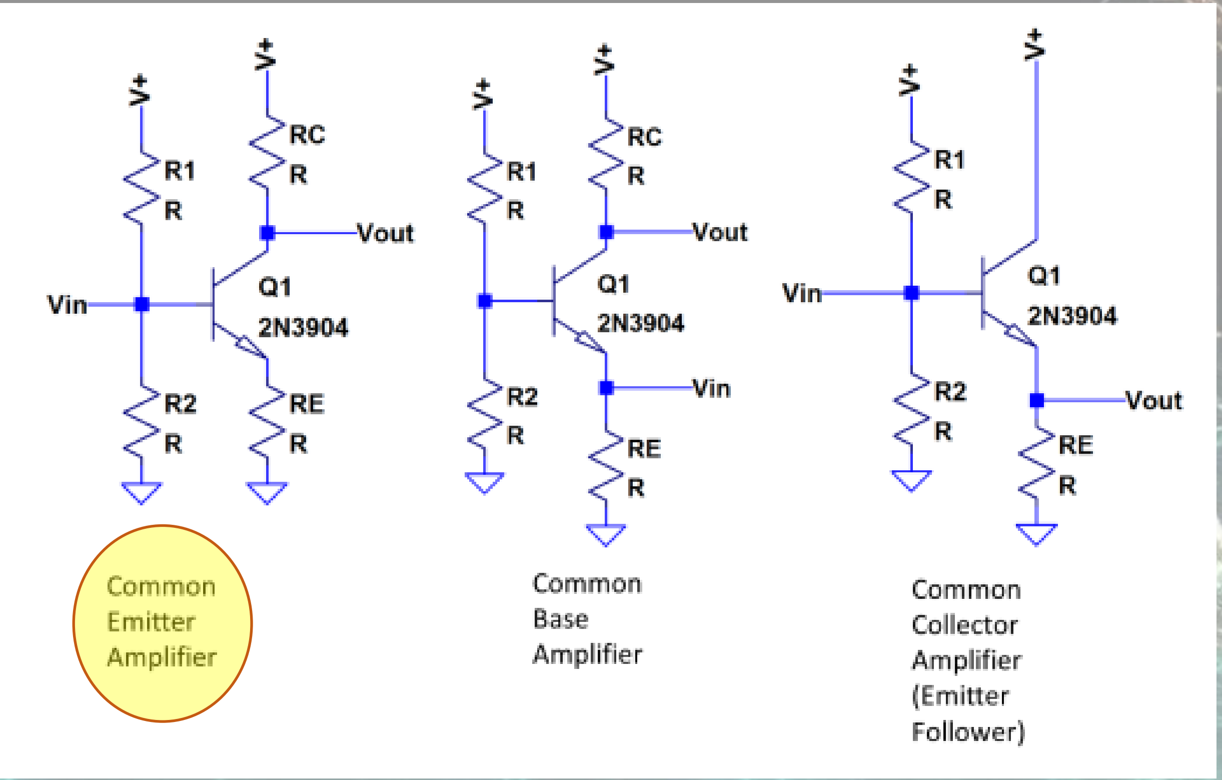
2. **Increase the input drive to compensate for the low input impedance**
   - ✓ **Use lower source impedance (transformer?) to compensate for voltage divider**

3. **Change the RC time constant for the internal capacitors (faster turn on)**
   - ✓ **Use *lower source impedance* (transformer?)**
   - ✓ **Reduce internal capacitance (different MOSFET)**

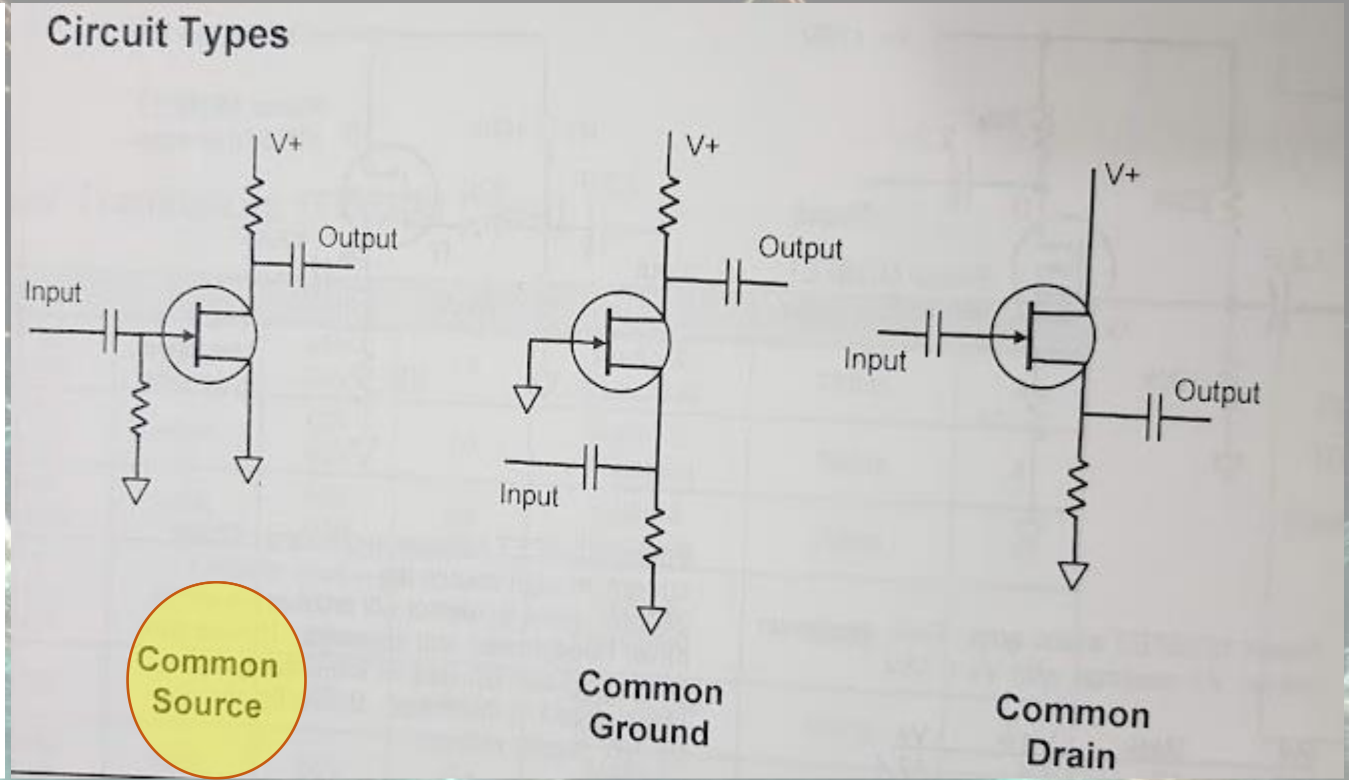
4. **Increase the current to reduce the charge time of the capacitors (faster turn on)**
   - ✓ **Use lower source impedance (transformer?)**
   - ✓ **Use a high current source (opamp)**
   - ✓ **Use *positive feedback***

CASCODE AMPLIFIER

MILLER EFFECT ON TRANSISTOR AMPLIFIERS



NPN BJT



N-Channel FET/MOSFET

MILLER EFFECT ON TRANSISTOR AMPLIFIERS

Susceptible to Miller Effect

Amplifier type	R_{in}	A_{vo}	R_o	A_v	G_v
	Characteristics[a]				
Common source (Fig. 7.35)	∞	$-g_m R_D$	R_D	$-g_m(R_D \parallel R_L)$	$-g_m(R_D \parallel R_L)$
Common source with R_s (Fig. 7.37)	∞	$-\dfrac{g_m R_D}{1+g_m R_s}$	R_D	$\dfrac{-g_m(R_D \parallel R_L)}{1+g_m R_s}$ $-\dfrac{R_D \parallel R_L}{1/g_m + R_s}$	$-\dfrac{g_m(R_D \parallel R_L)}{1+g_m R_s}$ $-\dfrac{R_D \parallel R_L}{1/g_m + R_s}$
Common gate (Fig. 7.39)	$\dfrac{1}{g_m}$	$g_m R_D$	R_D	$g_m(R_D \parallel R_L)$	$\dfrac{R_D \parallel R_L}{R_{sig} + 1/g_m}$
Source follower (Fig. 7.42)	∞	1	$\dfrac{1}{g_m}$	$\dfrac{R_L}{R_L + 1/g_m}$	$\dfrac{R_L}{R_L + 1/g_m}$

[a] For the interpretation of R_{in}, A_{vo}, and R_o, refer to Fig. 7.34(b).

N-Channel FET/MOSFET

Susceptible to Miller Effect

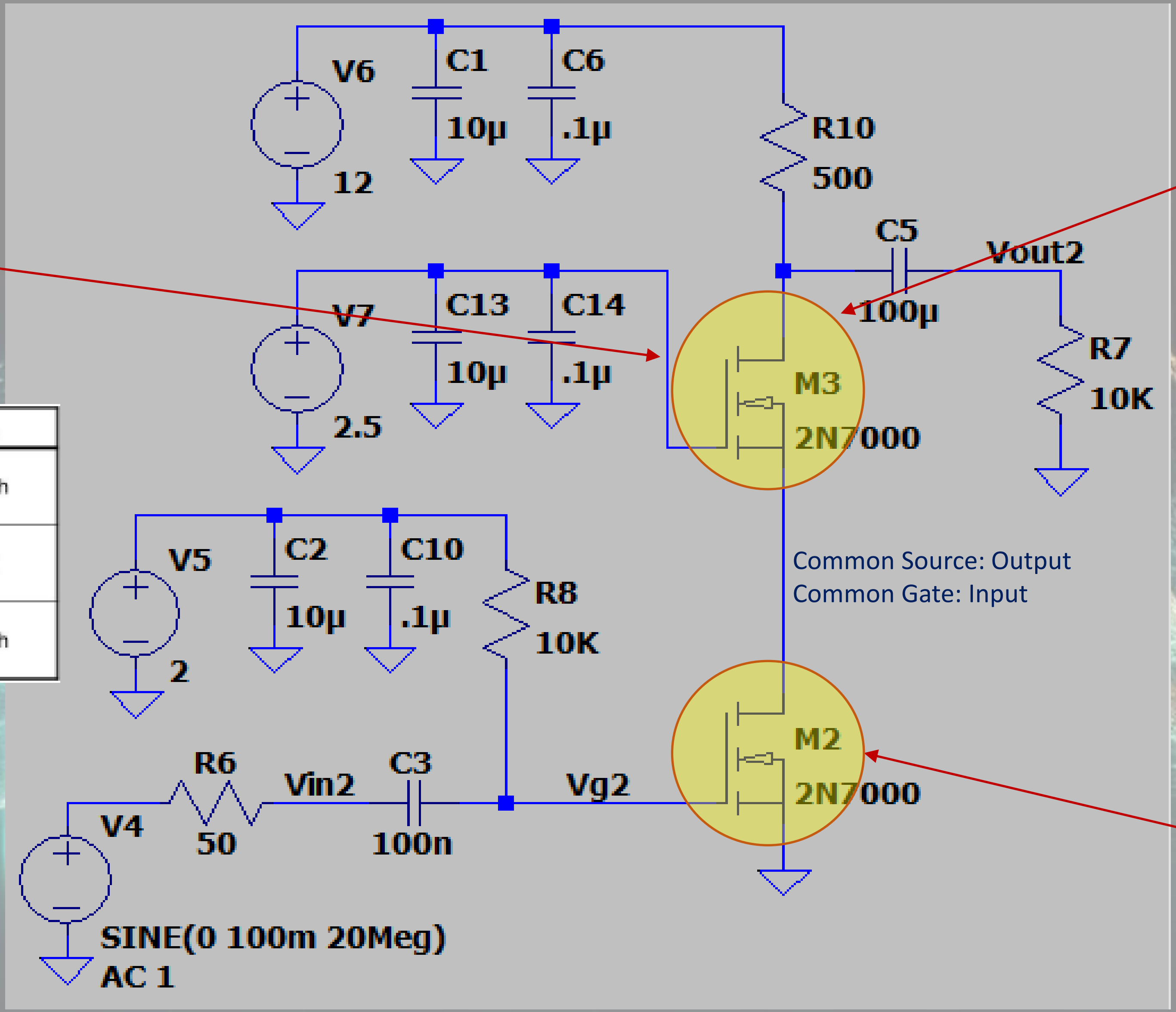
AMPLIFIER TYPE	COMMON BASE	COMMON EMITTER	COMMON EMITTER (Emitter Resistor)	COMMON COLLECTOR (Emitter Follower)
INPUT/OUTPUT PHASE RELATIONSHIP	0°	180°	180°	0°
VOLTAGE GAIN	HIGH $\dfrac{\alpha R_C}{R_s + r_e}$	MEDIUM $\dfrac{\beta(R_C \parallel r_o)}{R_s + r_\pi}$	MEDIUM $\dfrac{\beta R_C}{R_s + (\beta+1)(r_e + R_E)}$	LOW $\dfrac{(\beta+1)(R_L \parallel r_o)}{R_s + (\beta+1)[r_e + (R_L \parallel r_o)]}$
CURRENT GAIN	LOW α	MEDIUM $\beta \dfrac{r_o}{R_C + r_o}$	MEDIUM β	HIGH $(\beta+1)\dfrac{r_o}{r_o + R_L}$
POWER GAIN	LOW	HIGH	HIGH	MEDIUM
INPUT RESISTANCE	LOW r_e	MEDIUM $r_\pi = (\beta+1) r_e$	MEDIUM $(\beta+1)(r_e + R_E)$	HIGH $(\beta+1)[r_e + (r_o \parallel R_L)]$
OUTPUT RESISTANCE	HIGH R_C	MEDIUM $R_C \parallel r_o$	MEDIUM R_C	LOW $r_o \parallel \left[r_e + \dfrac{R_s}{(\beta+1)}\right]$

NPN BJT

MILLER NEUTRALIZATION: CASCODE

Miller Effect Negatable for common Gate

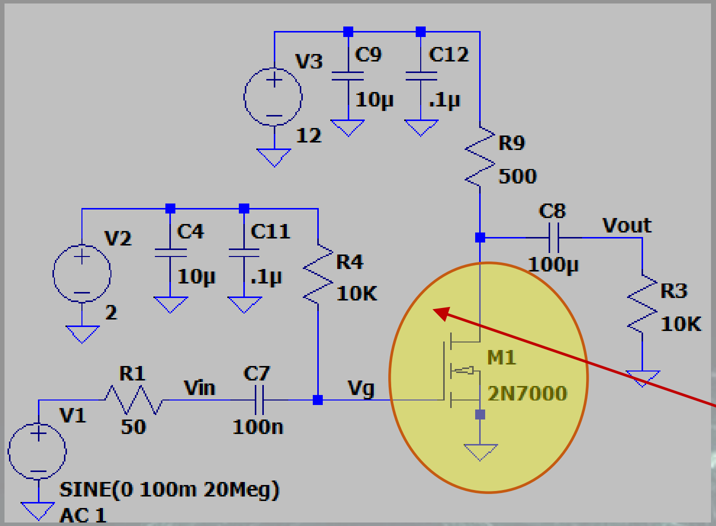
Amplifier Type	R_{in}	R_{out}	A_v	A_i
Common-source/emitter	High	High	High	High
Common-gate/base	Low	High	High	≈ 1
Common-drain/collector	High	Low	< 1	High



COMMON GATE (All Gain Here)

COMMON SOURCE (Unity Gain Here)

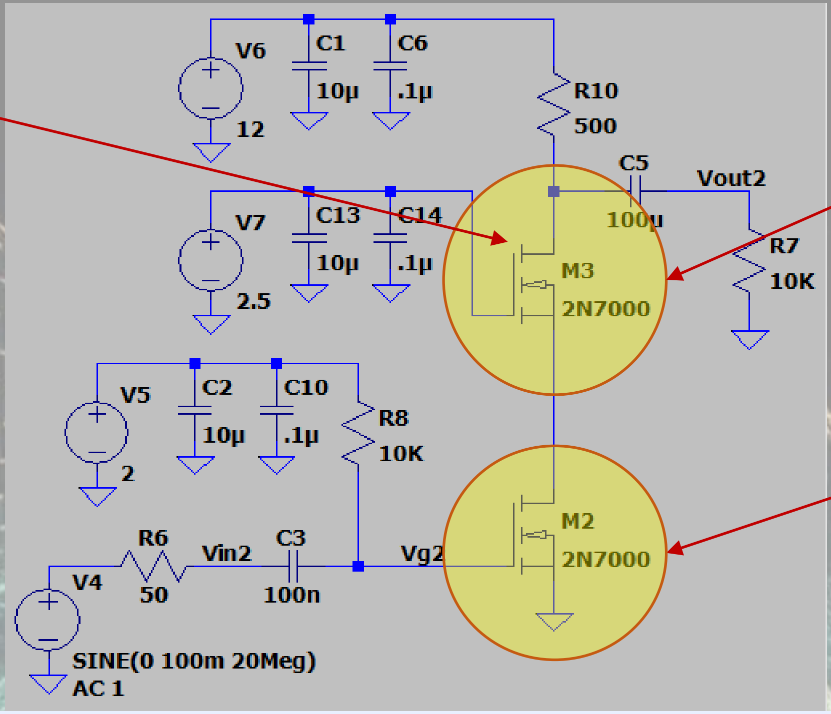
MILLER NEUTRALIZATION: CASCODE



CONTROL AMP

Miller Effect Substantial

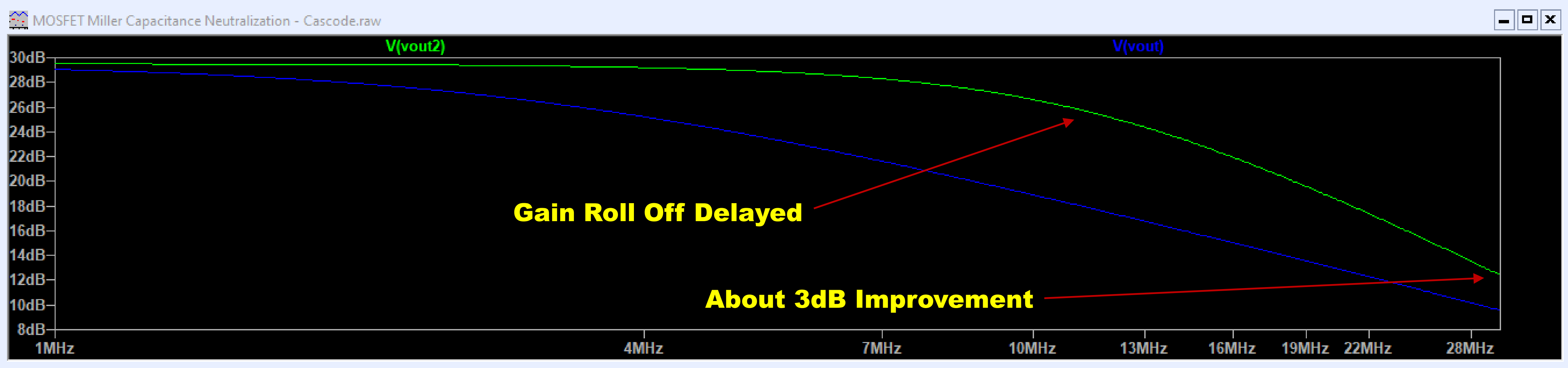
Miller Effect Negatable



COMMON GATE (All Gain Here)

COMMON SOURCE (Unity Gain Here)

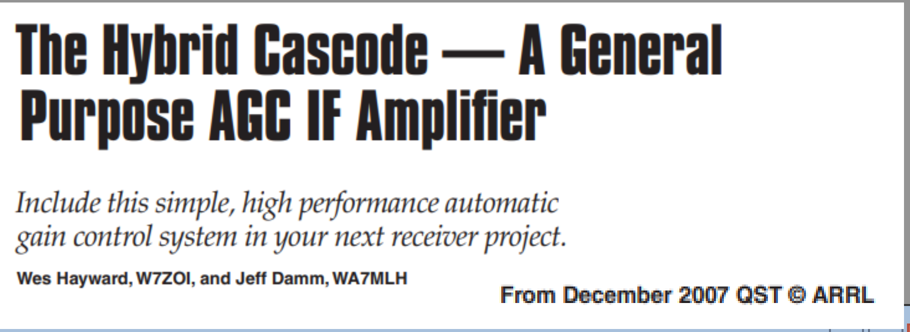
CASCODE AMP



Gain Roll Off Delayed

About 3dB Improvement

MILLER NEUTRALIZATION: HYCAS


The Hybrid Cascode — A General Purpose AGC IF Amplifier

Include this simple, high performance automatic gain control system in your next receiver project.

Wes Hayward, W7ZOI, and Jeff Damm, WA7MLH

From December 2007 QST © ARRL

Vgs < 0 (Vg must be below Vs)

Hybrid Cascode

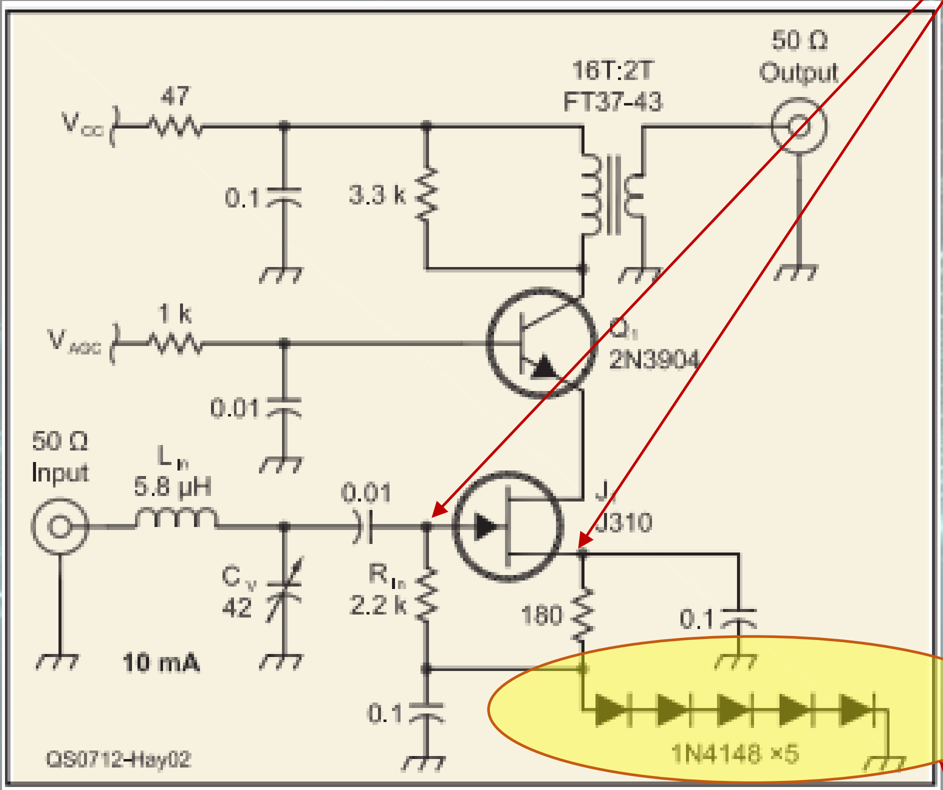
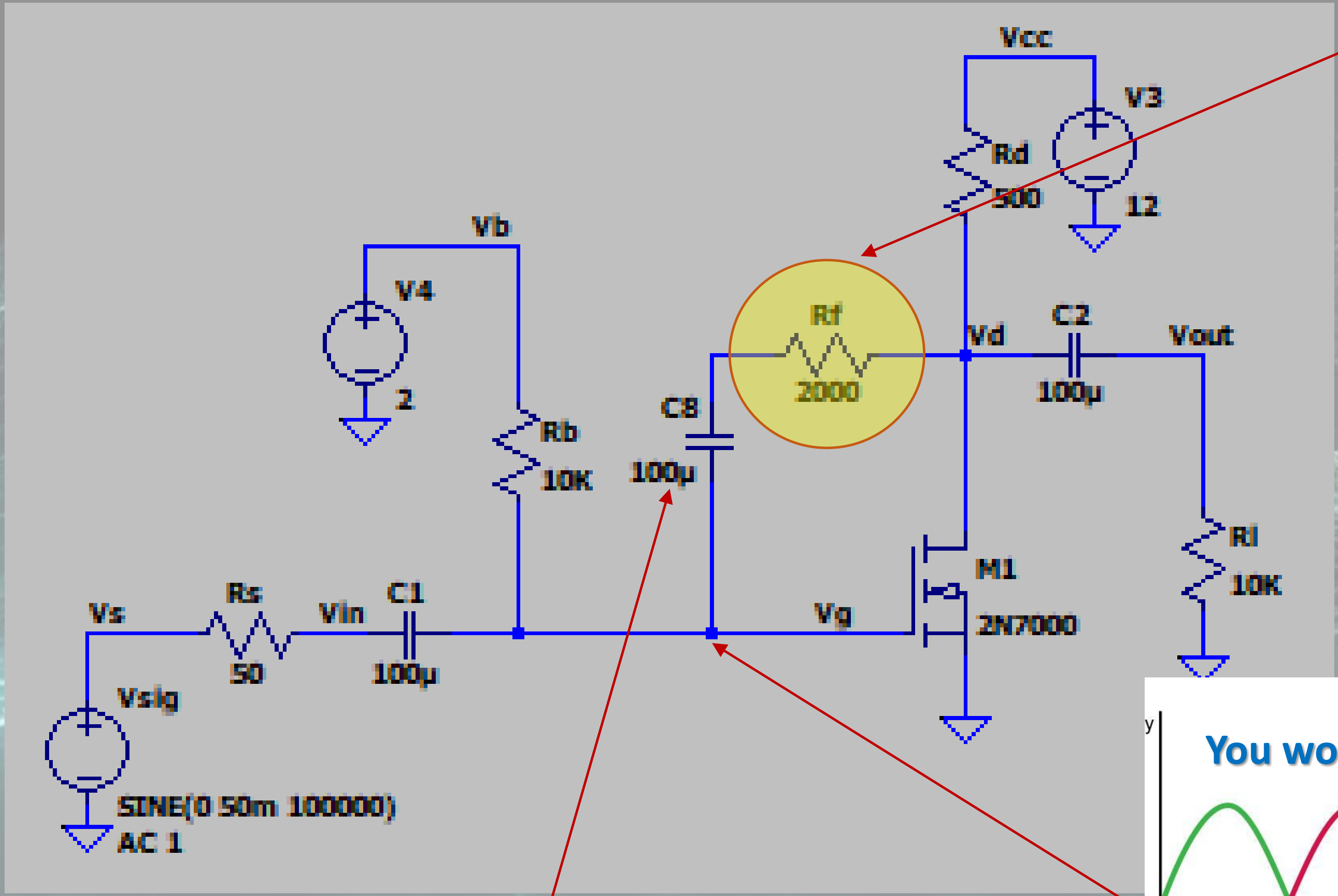


Figure 2 — Hybrid cascode. 9 MHz G_{MAX} of 23.9 dB when V_{AGC} is 8.5 V. Same tuning as Figure 1.

Diode drops raised Vs to a positive voltage…Say 3.5V. Vg must be 3.2V below Vs for JFET to turn on. If Vg is below 0.3V (relative to ground) JFET will turn on

NEGATIVE FEEDBACK AMPLIFIER

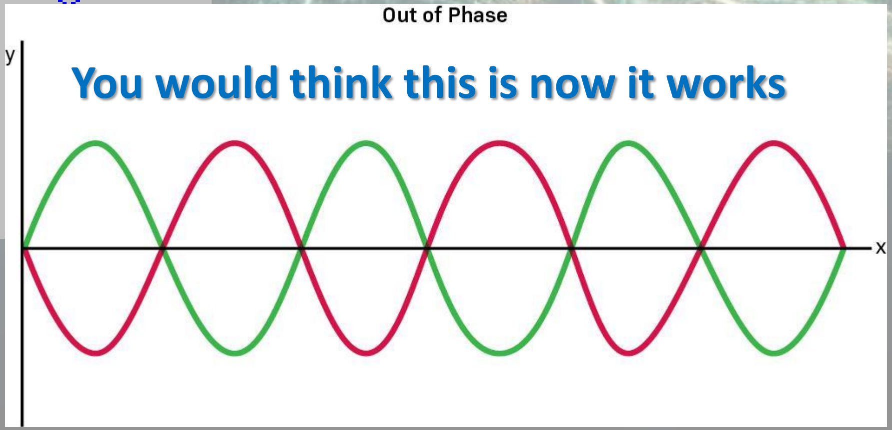
MILLER NEUTRALIZATION: -FEEDBACK



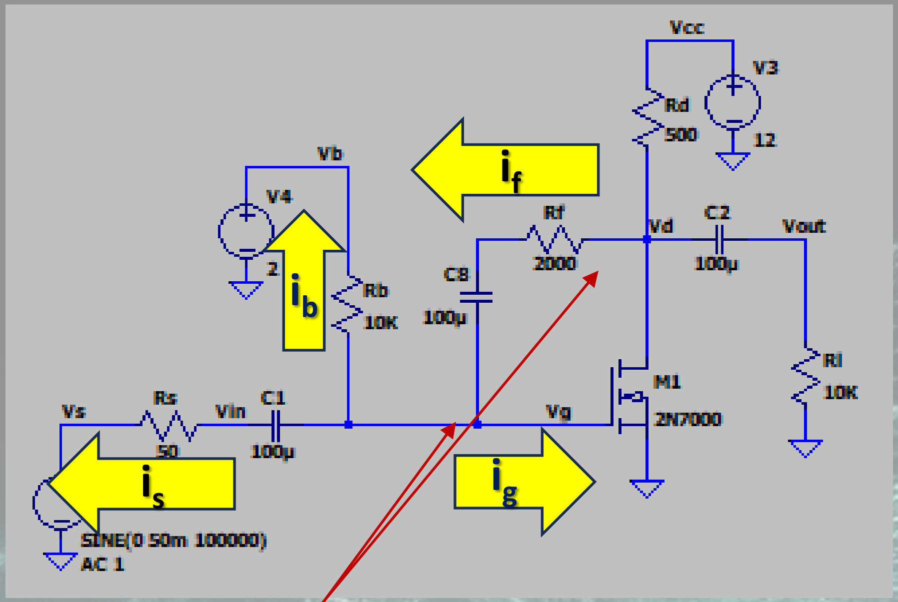
Negative Feedback Resistor

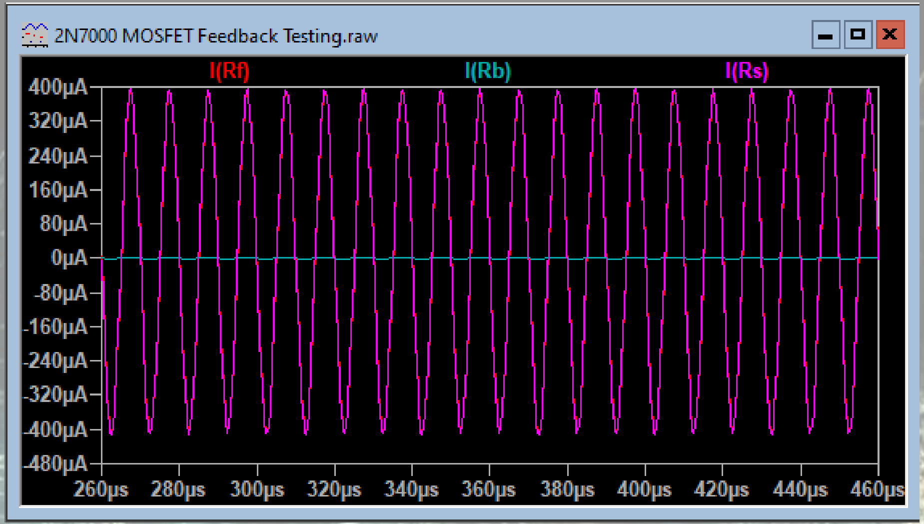
Reduces Gain and Reduces Miller Capacitance

DC Blocking Cap Negligible impact



MILLER NEUTRALIZATION: -FEEDBACK



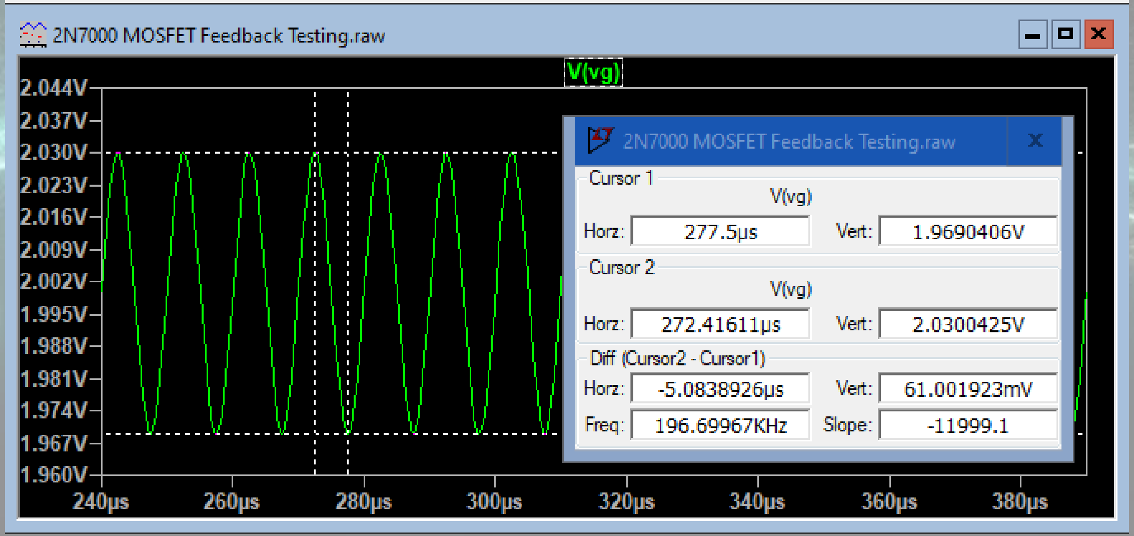


v_d: 5.5V
v_g: 2V

i_f: 271uA
i_s: 273uA

i_g: 7uA
i_b: 2uA

Voltage at output is larger than voltage at input (there is gain) Current flows to lower voltage



v_g: 61mV (pp)

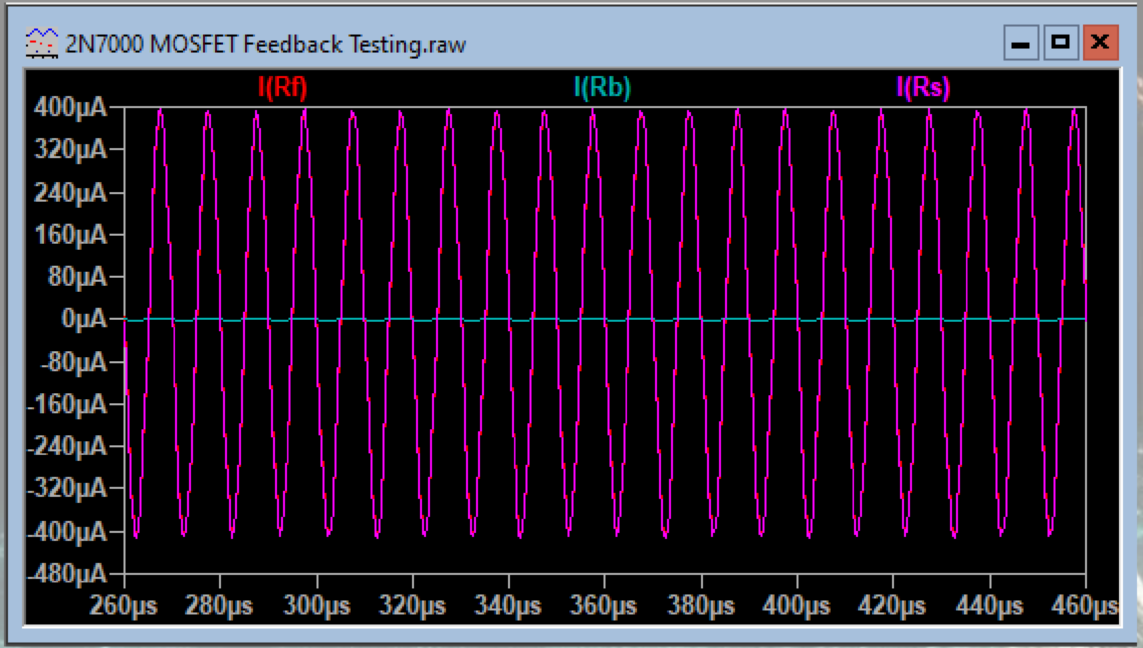
This is a current feedback amplifier.

Takes a voltage and feeds back a current

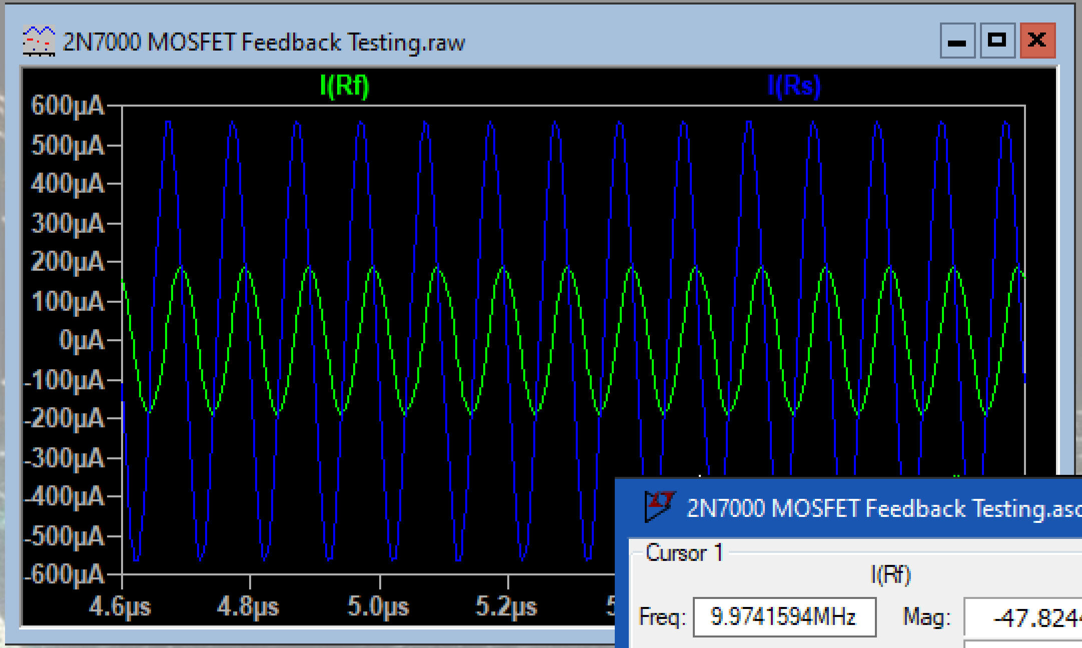
(At least at 100 KHz)

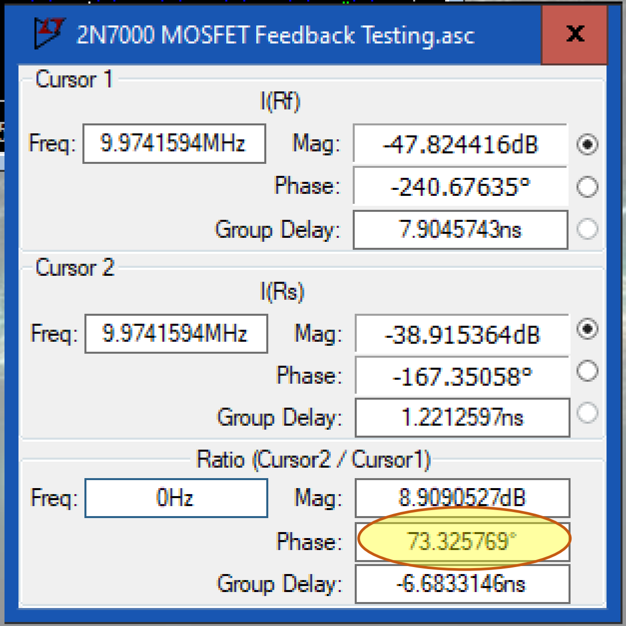
MILLER NEUTRALIZATION: -FEEDBACK

100 KHz



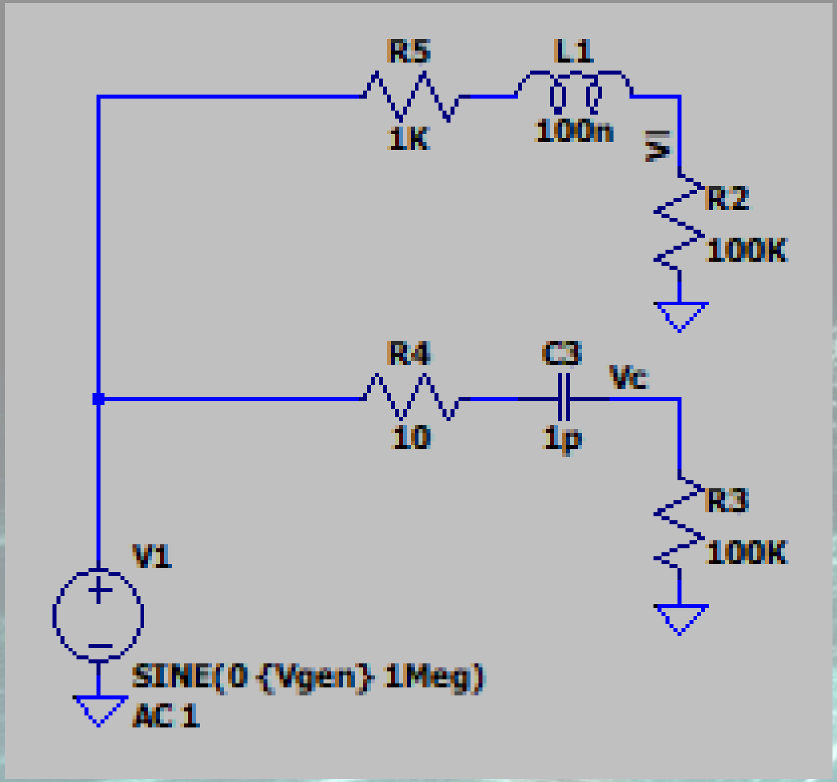
10 MHz

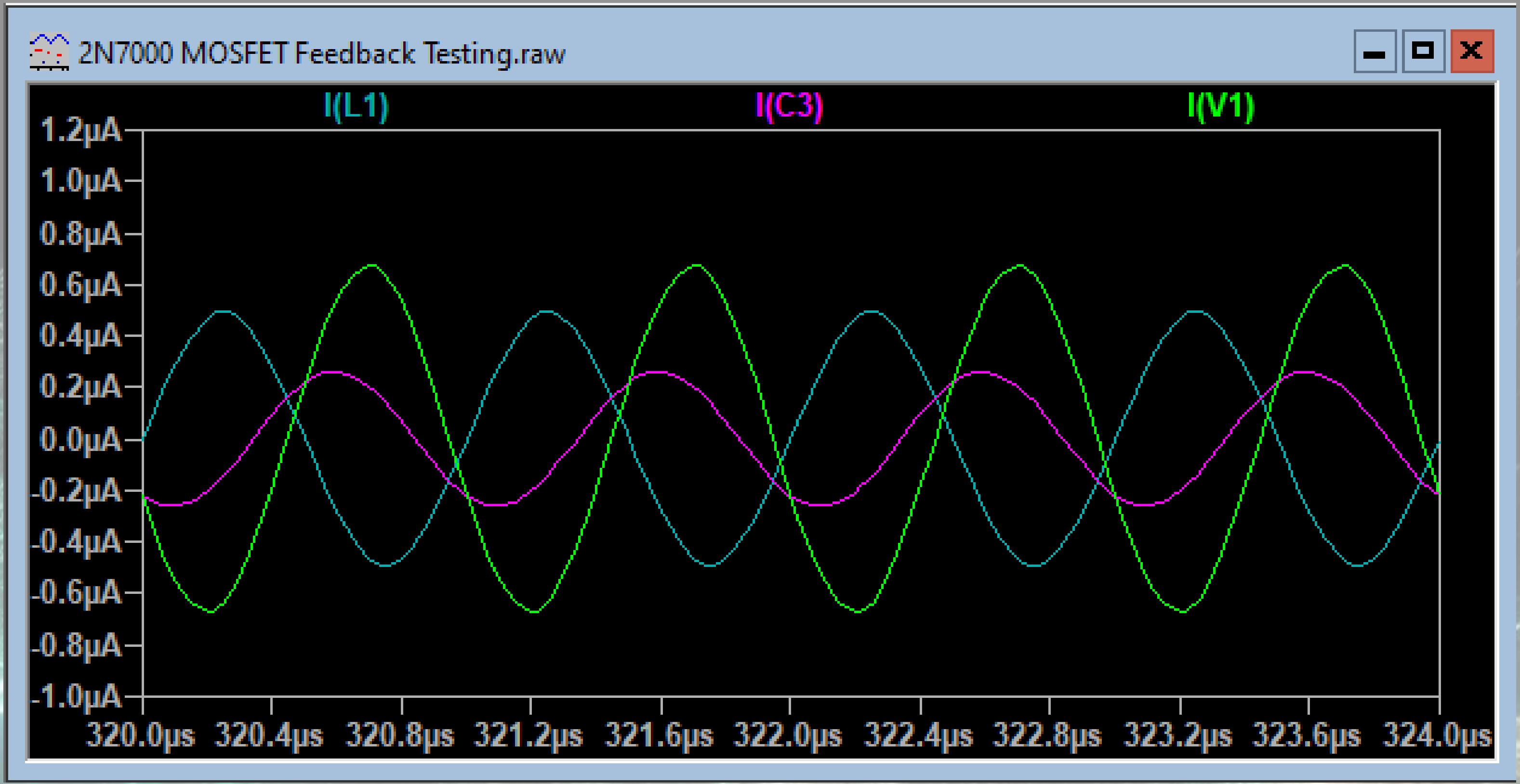




Welcome to my nightmare

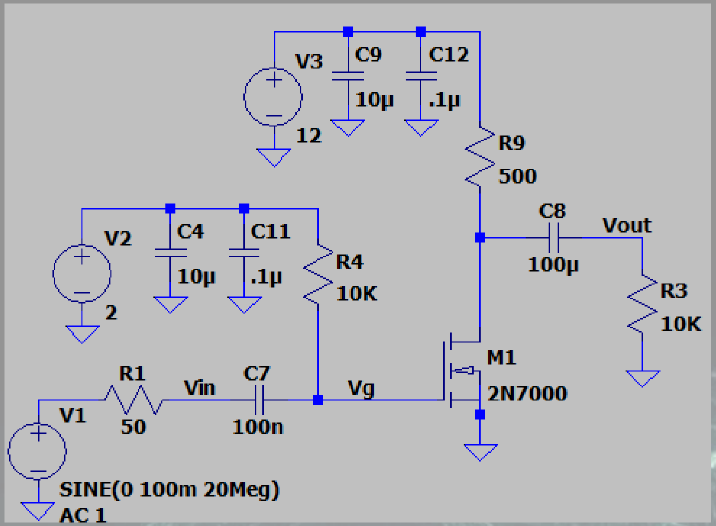
MILLER NEUTRALIZATION: PHASE



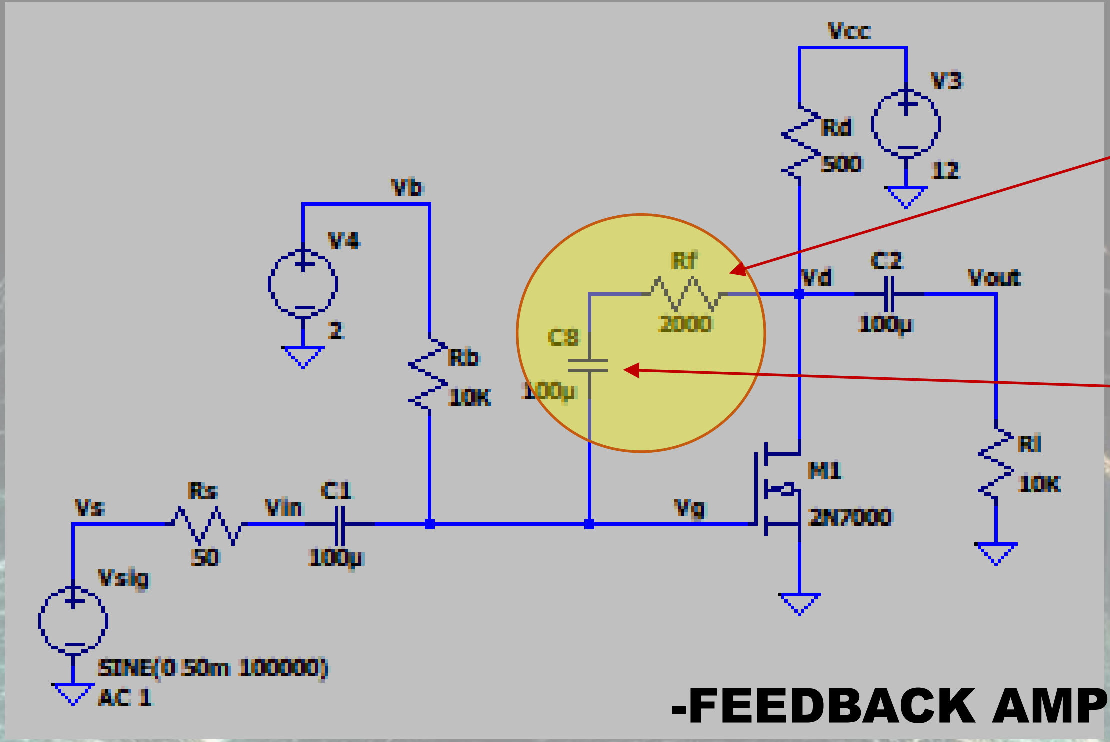


Analysis needs complex numbers that represents magnitude and phase

MILLER NEUTRALIZATION: -FEEDBACK



CONTROL AMP

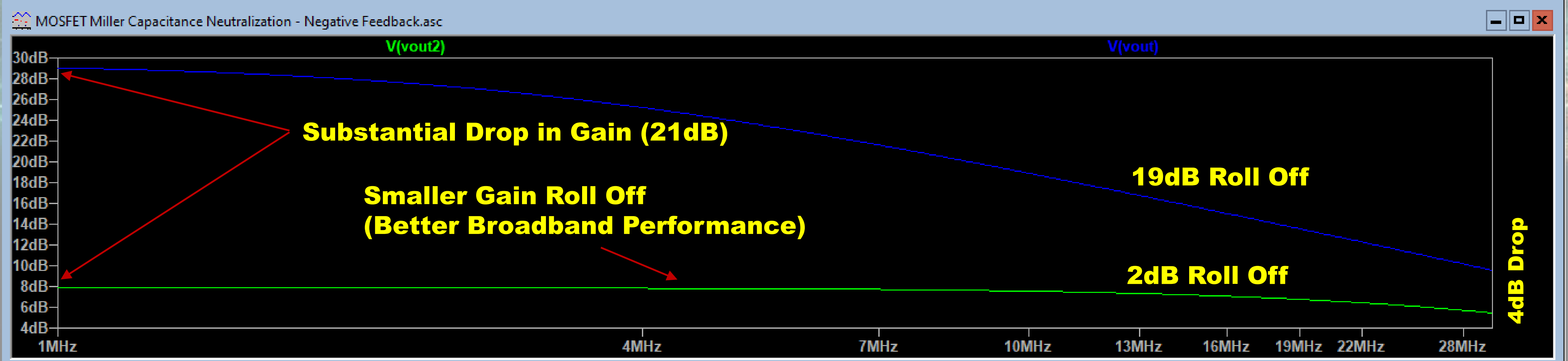


-FEEDBACK AMP

Negative Feedback Resistor

Reduces Gain and Reduces Miller Capacitance

DC Blocking Cap Negligible impact

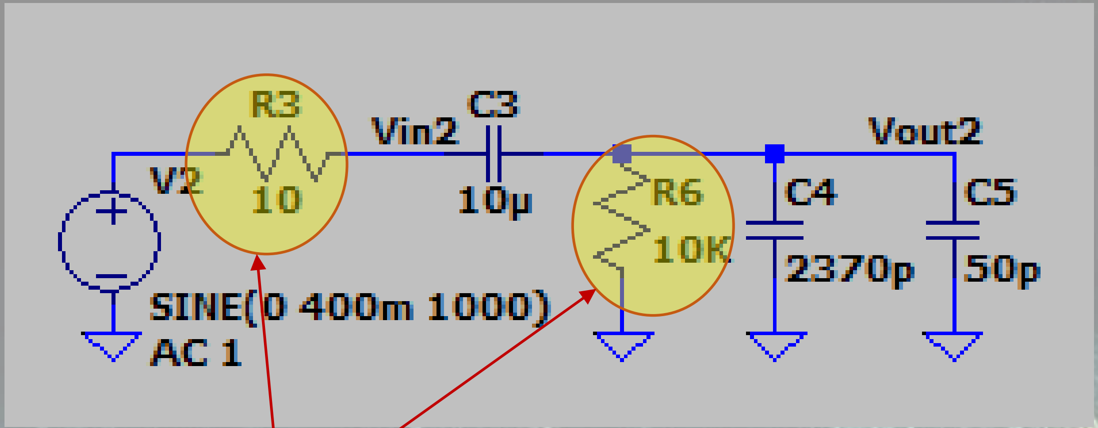


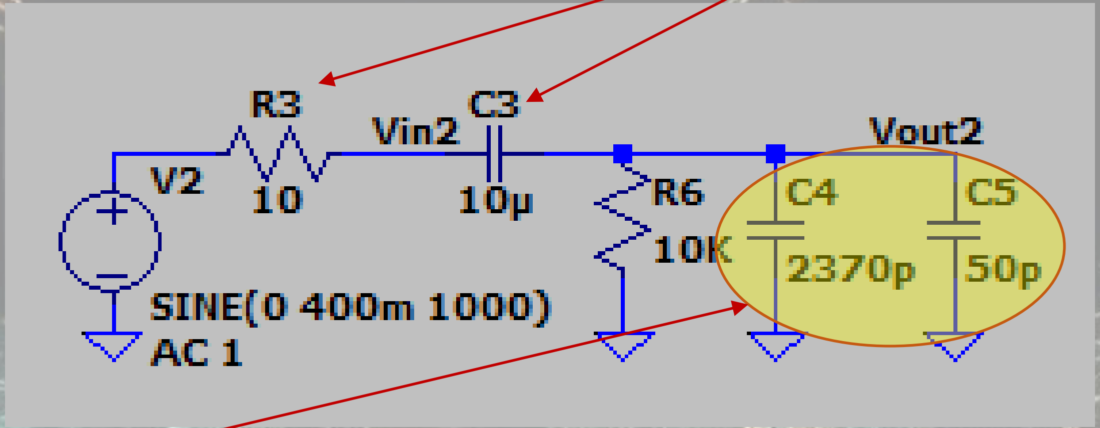
ADJUST RC TIME CONSTANT

MILLER EFFECT: C TIME CONSTANT

Simplified AC 2N7000 Model

Note: C3 and R3 form a "High Pass Filter" with F 10 KHz





"R" term in "RC" Time Constant

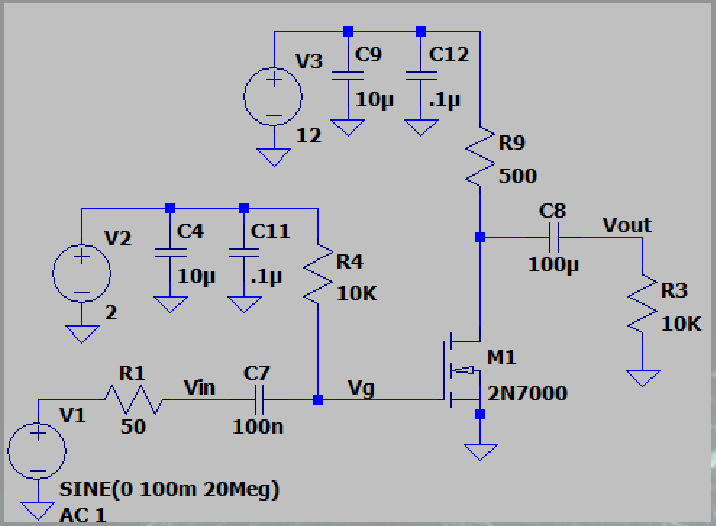
"C" term in "RC" Time Constant

Circuit (LTSpice)				Calculated	
Rbias	10000				
Rd	500				
Rs	10			Gm	0.083
Rl	10000			Av	41
Rout	10000	pF		Cmiller	2370
Cin	1000000	pF		Cin	2420
Cout	1000000	pF		Rin	10
Cgd	56.1	pF			
Cgs	50	pF			
Cfb	0				
				Fc	6.714

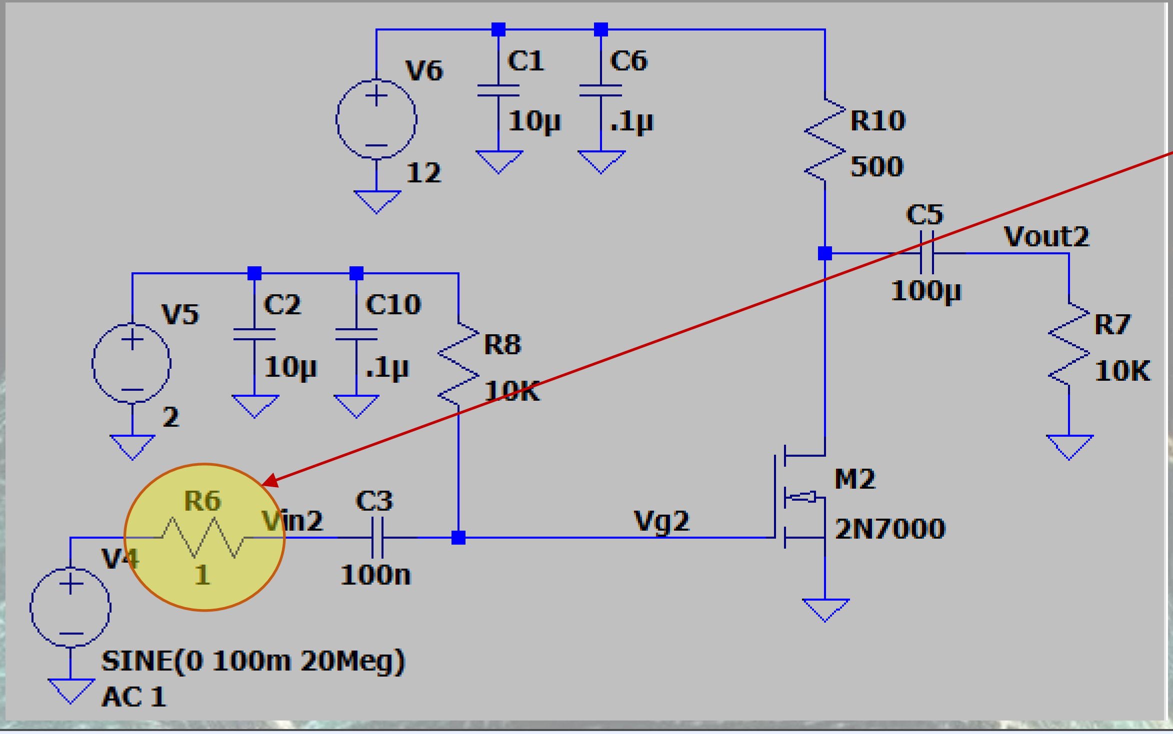
"C" (C4 + C5)

"R" (R3//R6)

MILLER NEUTRALIZATION: RC Constant

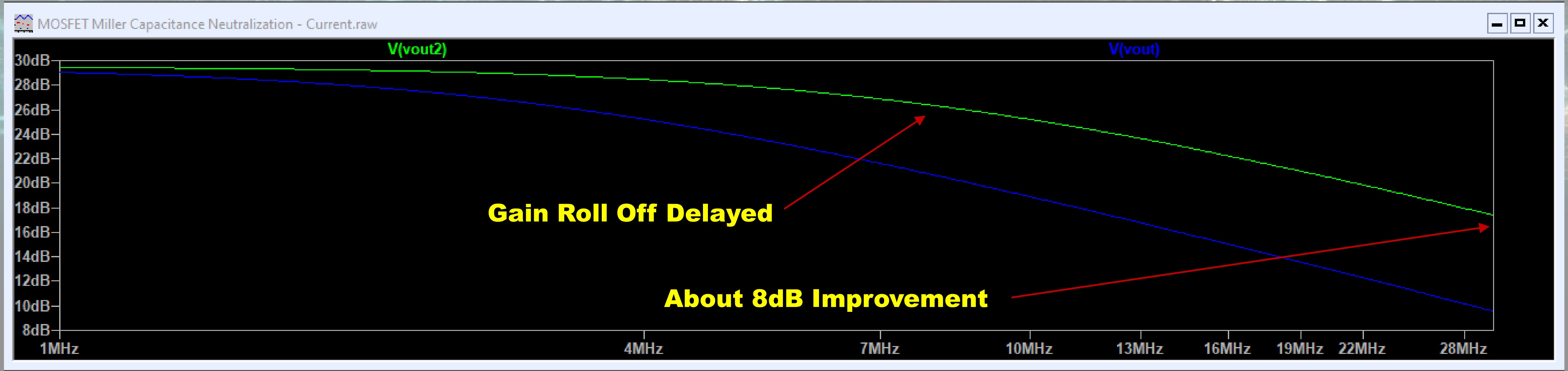


CONTROL AMP

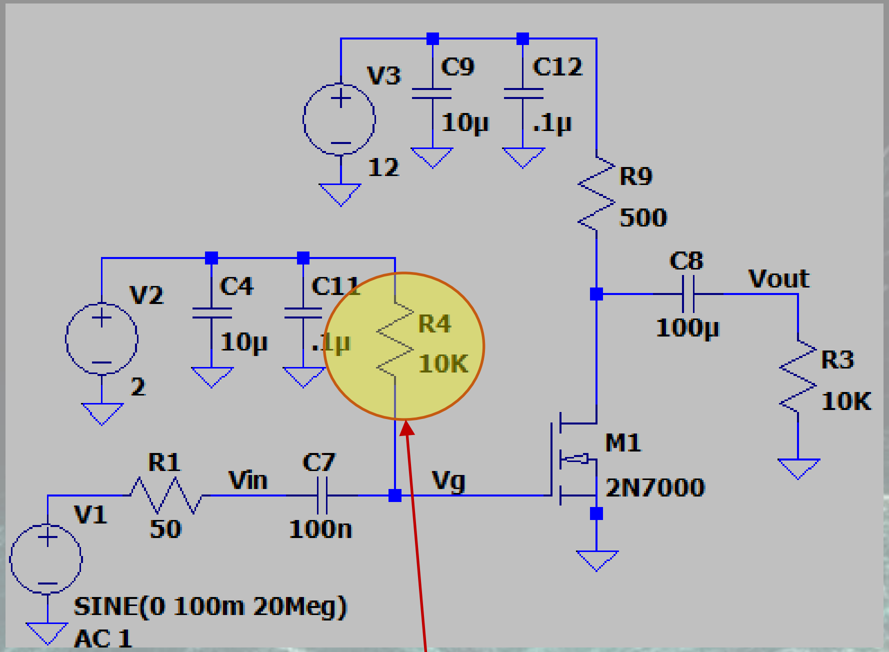


Reduce Source Z
Reduce RC Tau
Increase Current

LOWER RC TIME CONSTANT AMP

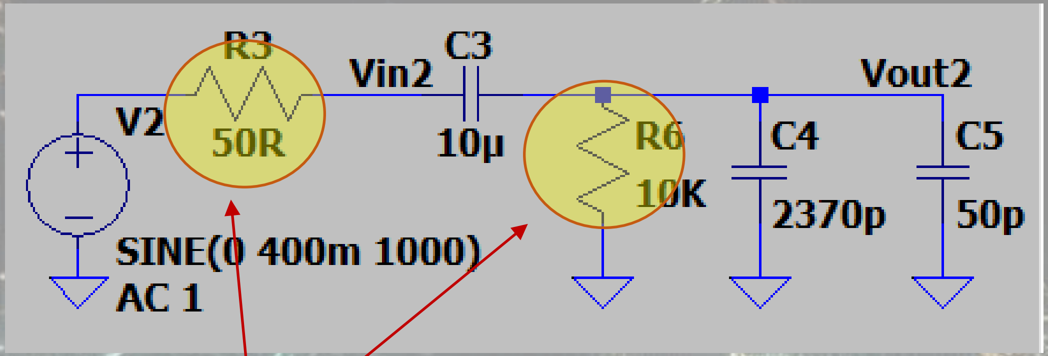


MILLER NEUTRALIZATION: RC Constant



If bias resistors are same as or lower than source impedance, RC time constant is reduced

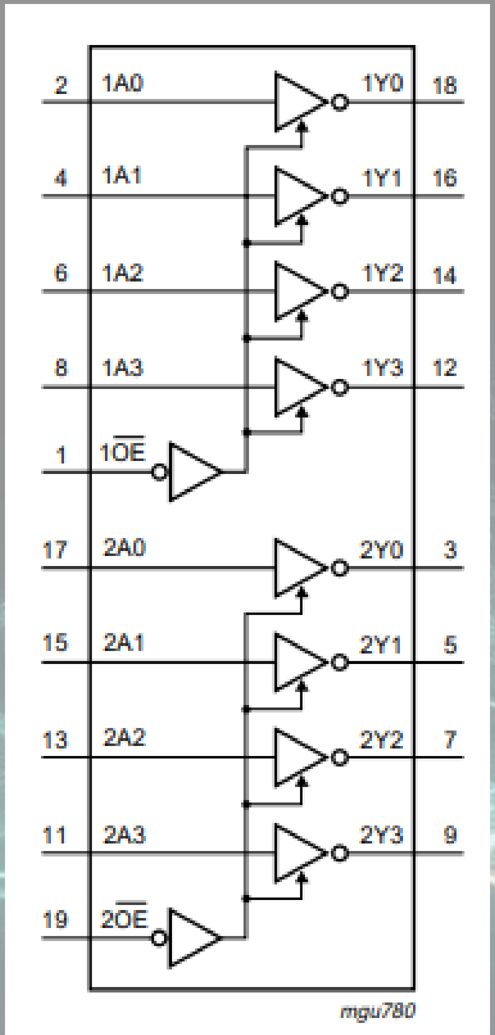
Simplified AC 2N7000 Model

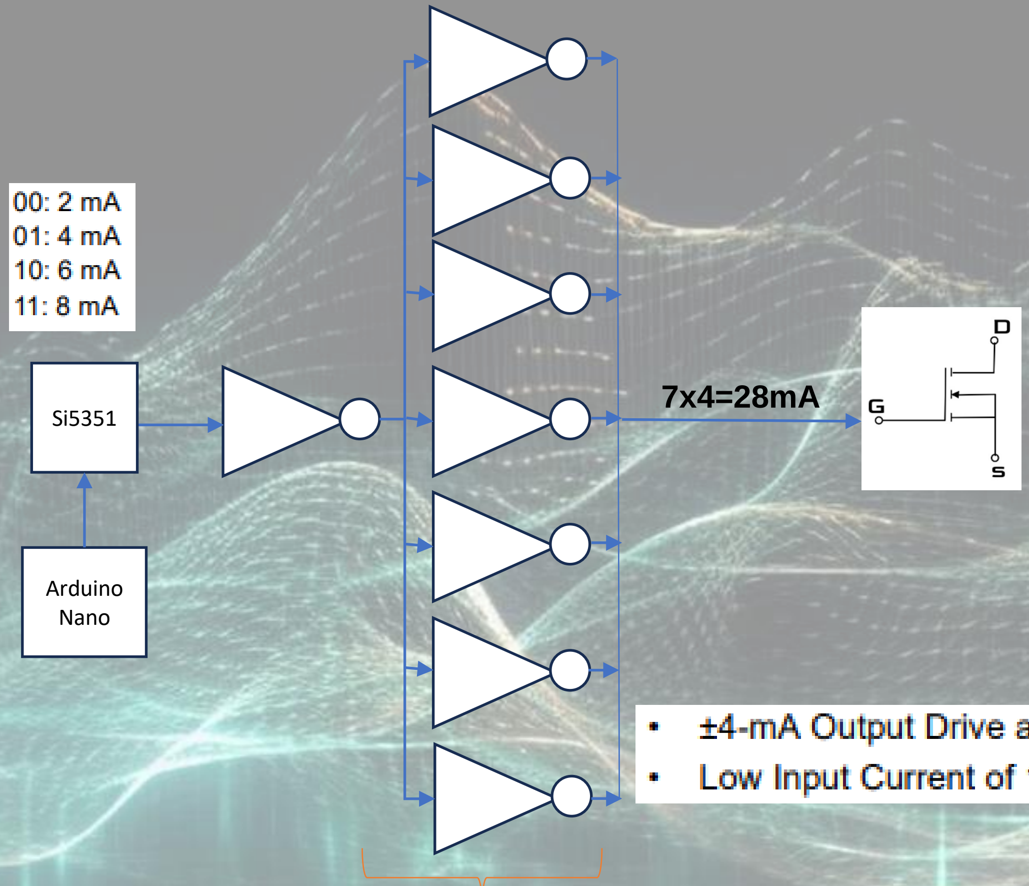


"R" term in "RC" Time Constant

Circuit (LTSpice)				Calculated	
Rbias	10000				
Rd	500				
Rs	50			Gm	0.083
Rl	10000			Av	41
Rout	10000	pF		CmillerIn	2370
Cin	1000000	pF		Cin	2420
Cout	1000000	pF		Rin	50
Cgd	56.1	pF		CmillerOut	57
Cgs	50	pF			
Cfb	0				

MILLER EFFECT: INCREASE CURRENT





Captain, we need more current...

- ±4-mA Output Drive at 5 V
- Low Input Current of 1 µA Maximum

Buffer driver in parallel for greater current output. Used for TTL Transmitters

74HC240; 74HCT240

Octal buffer/line driver; 3-state; inverting

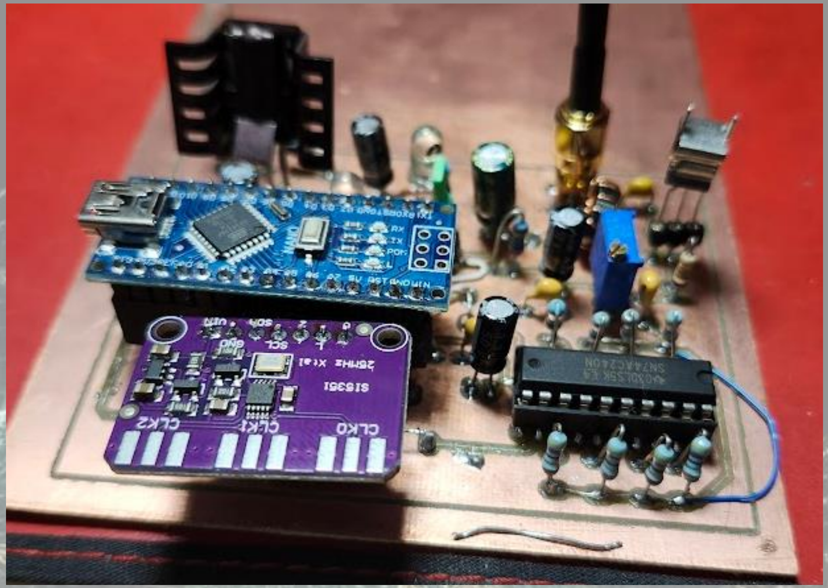
Octal: 8
Hex: 6

The **74HC** family has High-speed CMOS circuitry, combining the speed of TTL with the very low power consumption of the

The Si5351A/B/C features various output current drives ranging from 2 to 8 mA (default). It is recommended to configure the trace characteristics as shown in Figure 18 when an output drive setting of 8 mA is used.

MILLER EFFECT: INCREASE CURRENT

Si5351 driving BS170 MOSFET



Si5351 & 74HC140 driving BS170 MOSFET

Without 74HC240 Drivers				
Frequency (MHz)	Output (dBm)	Output (Watts)	Highest Harmonic (dBm)	Harmonic Attenuation
7	30.6	1.1	-21	-51.6
14	29.4	0.87	-21	-50.4
20	26.9	0.49	-24	-50.9
30	26.6	0.45	-24	-50.6

~8mA drive into 50R load

At least 3x
Current increase

Getting over 1W across HF band with more current from 74HC240 driver

With 74HC240 Drivers				
Frequency (MHz)	Output (dBm)	Output (Watts)	Highest Harmonic (dBm)	Harmonic Attenuation
7	32.8	1.9	-20	-52.8
14	31.8	1.5	-20	-51.8
20	31.2	1.3	-21	-52.2
30	30.5	1.1	-21	-51.5

~28mA drive into ?? load

POSITIVE FEEDBACK

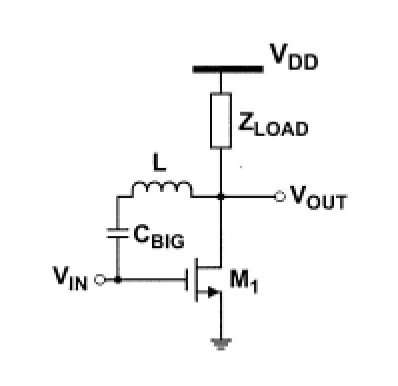
MILLER NEUTRALIZATION: +FEEDBACK

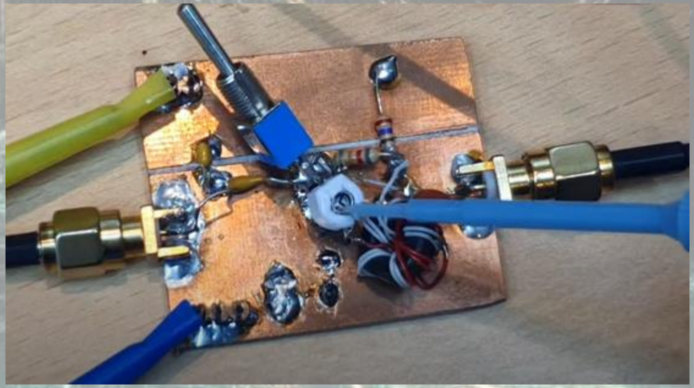
A 1-V Transformer-Feedback Low-Noise Amplifier for 5-GHz Wireless LAN in 0.18-μm CMOS

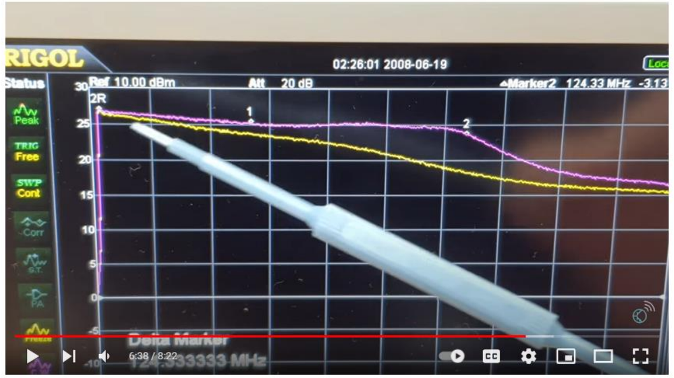
David J. Cassan, *Member, IEEE,* and John R. Long, *Member, IEEE*

III. Transformer-Feedback LNA

An alternative approach to neutralization uses transformer feedback, which introduces magnetic coupling between drain and source inductors of a common-source transistor, as shown in Fig. 2(c). Feeding back a portion of the output signal via the transformer can effectively cancel the feedback from output to input through the Miller capacitance (C_{gd}) and neutralize the amplifier. The circuit parameters that define this condition are derived in Sections III-A and B.





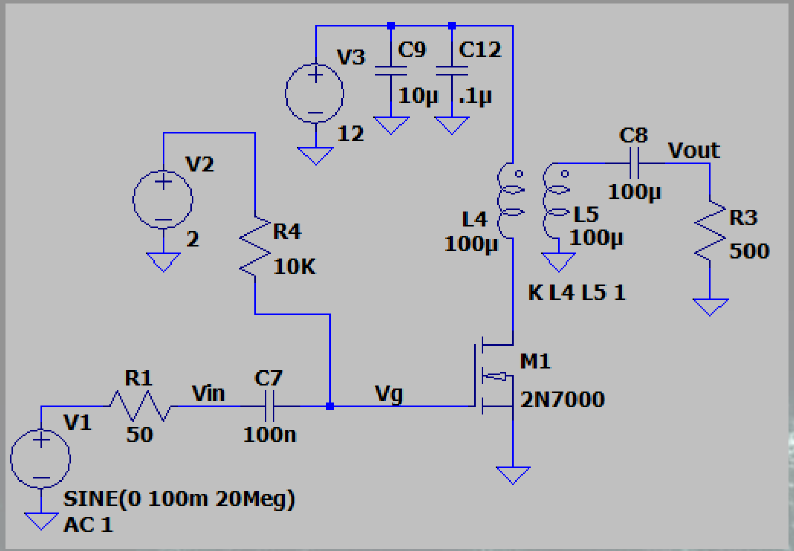


All Electronics Channel
10.3K subscribers

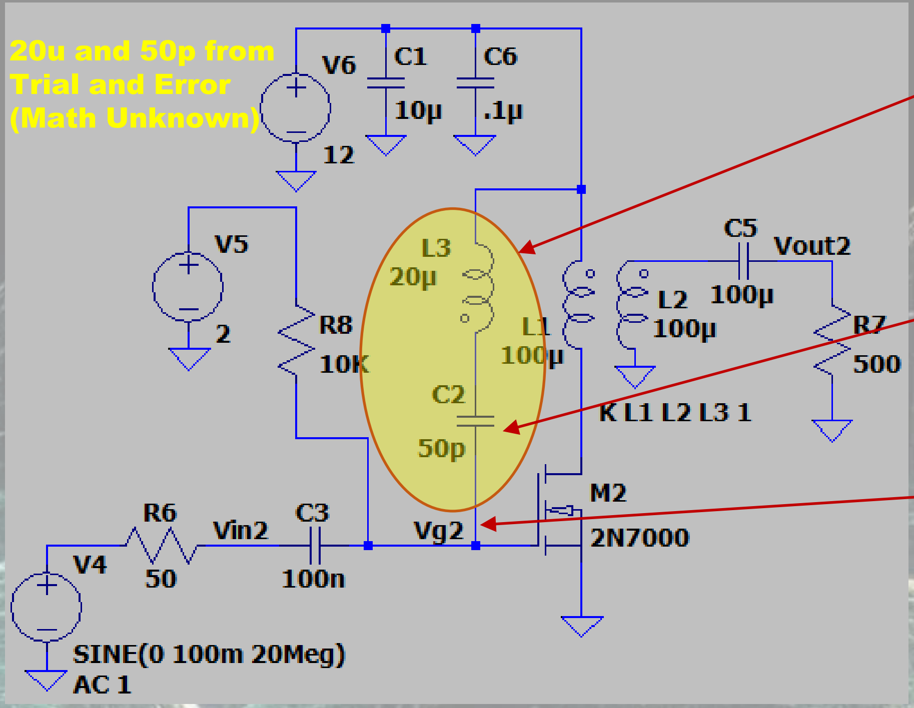
Transistor Miller Effect Neutralization

https://youtu.be/czk0I3ga3LQ?si=BfAECM6Ak_sQOEQT

MILLER NEUTRALIZATION: +FEEDBACK



CONTROL AMP



Add Turns with Inverted Phasing for Positive Feedback

DC Blocking Cap Restrict Feedback? Negates Miller?

Feedback adds to Input. Cancels Miller. DANGEROUS! Resonance or Runaway

+FEEDBACK AMP

Don’t take my word…

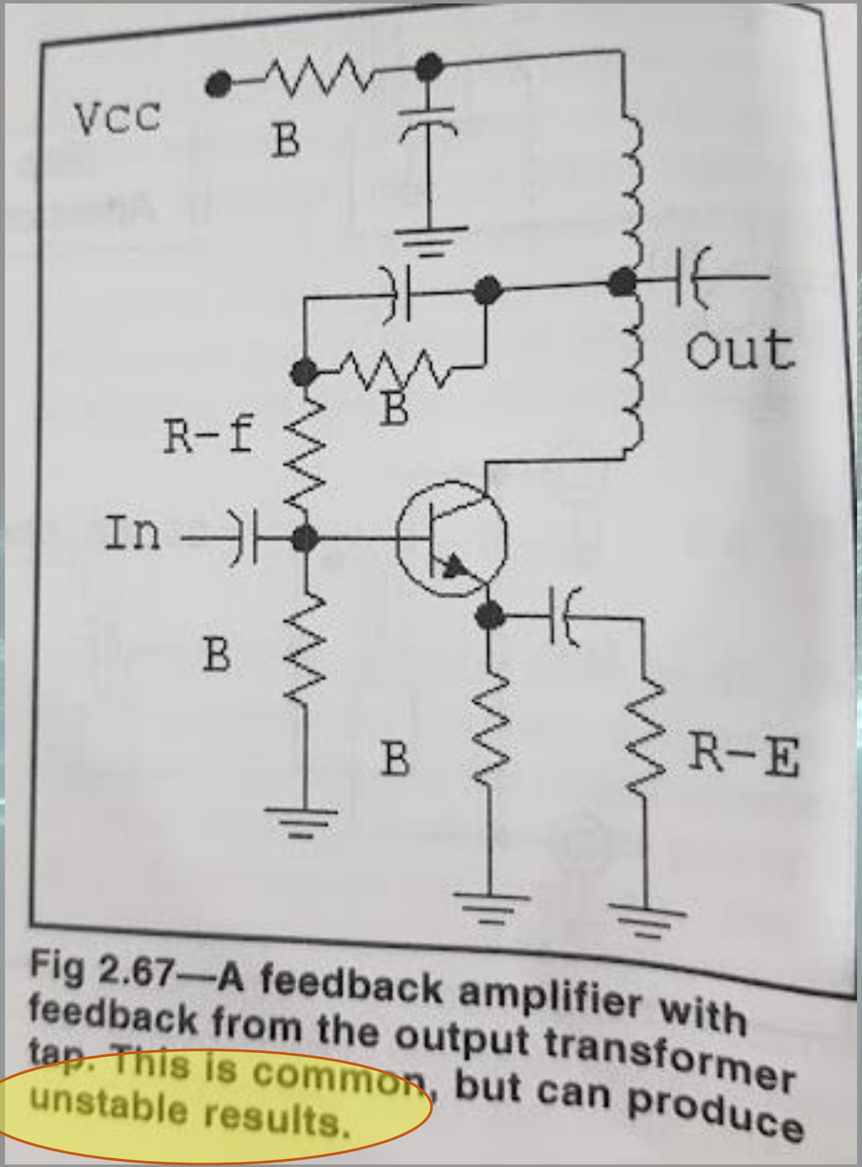
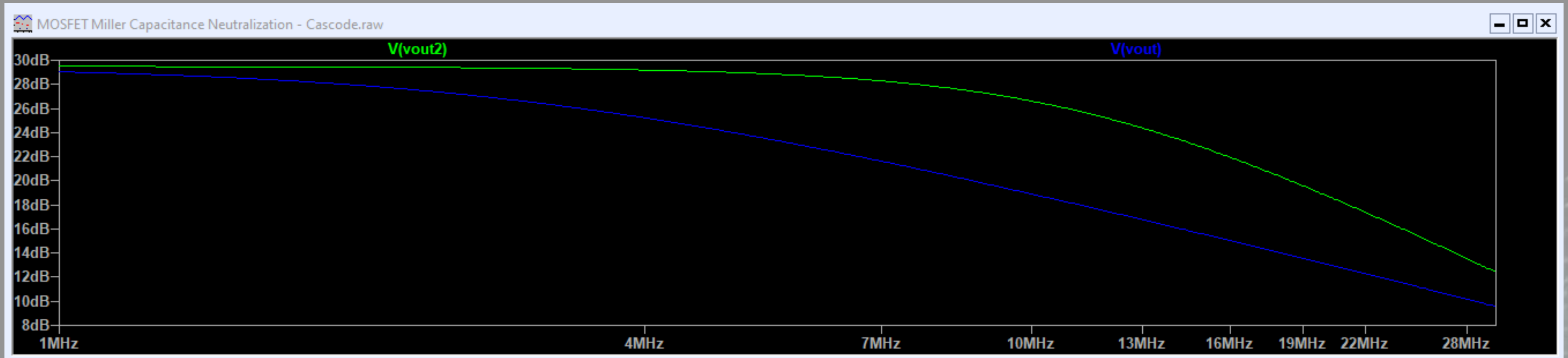


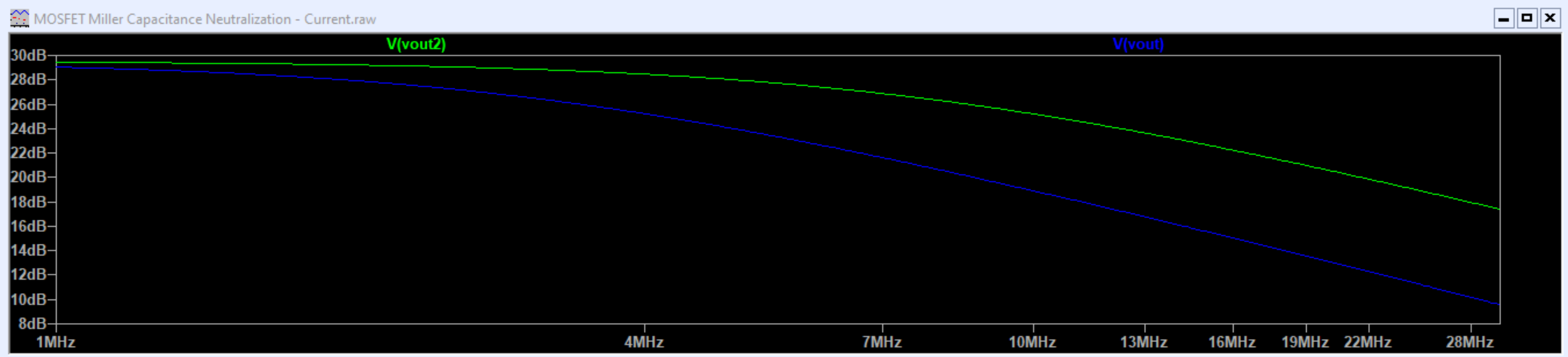
Fig 2.67—A feedback amplifier with feedback from the output transformer tap. This is common, but can produce unstable results.

EMRFD “Feedback Amplifiers”

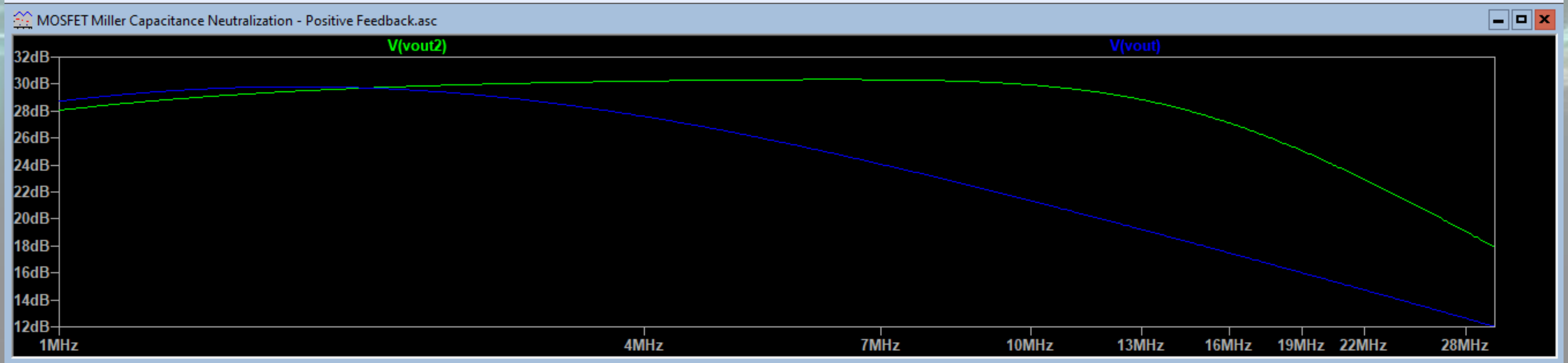
MILLER NEUTRALIZATION: COMPARISON



CASCODE



Lower Source Z



+FEEDBACK AMP

CONCLUSION:
RF AMPLIFIERS ARE PROBLEMATIC

1. **The intrinsic capacitance of transistor limits bandwidth.**
   - ➢ **Worst for high gain RF amplifiers**

2. **Extend bandwidth:**
   - ✓ **Use a RF transistor with low internal "parasitic" capacitance**
   - ✓ **Use a non-inverting amplifier to do the heavy lifting (CASCODE/HYCAS)**
   - ✓ **Use high current/low source impedance drive. Reduce the RC time constant.**
   - ✓ **Reduce Gain.**
     - ✓ **Use negative feedback**

...to be continued

RF Amplifier Negative Feedback:

How it works using math

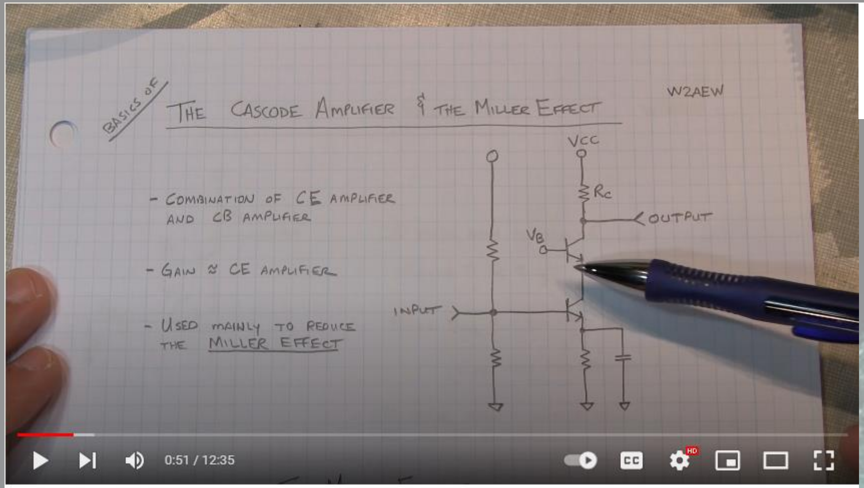
Danger Will Robinson…

Quote Charlie Morris, ZL2CTM:

This NOT a tutorial.

It's a log of my journey. Right or wrong.

REFERENCES

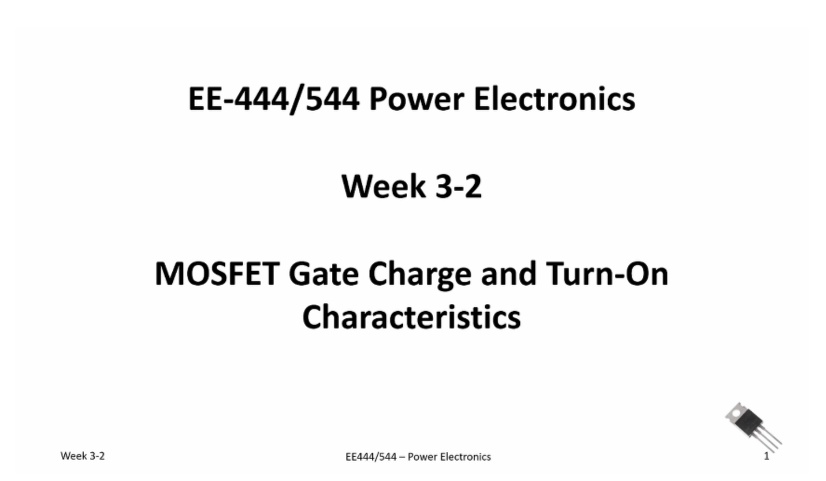


#207: Basics of a Cascode Amplifier and the Miller Effect

w2aew
193K subscribers

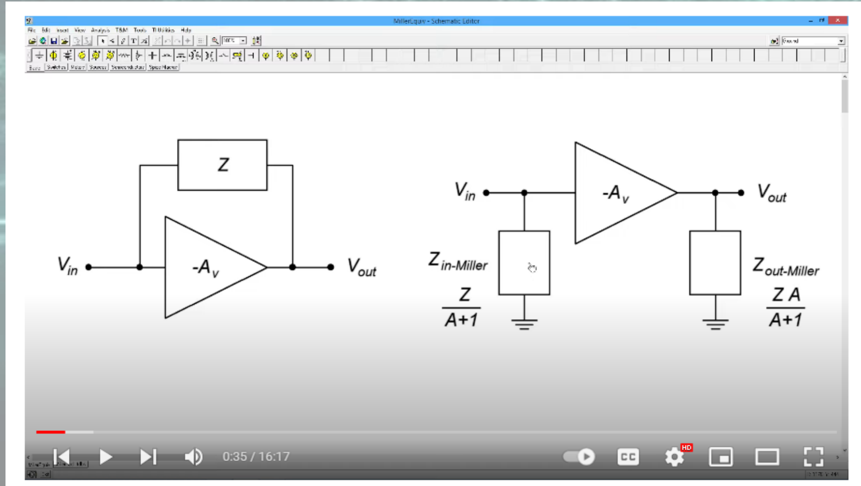
https://youtu.be/Op_I3Ke7px0

Power Electronics with Dr. K
8.37K subscribers



Power Electronics WK3_2 MOSFET Turn On Characteristics

https://youtu.be/f1yt0s3gpcE

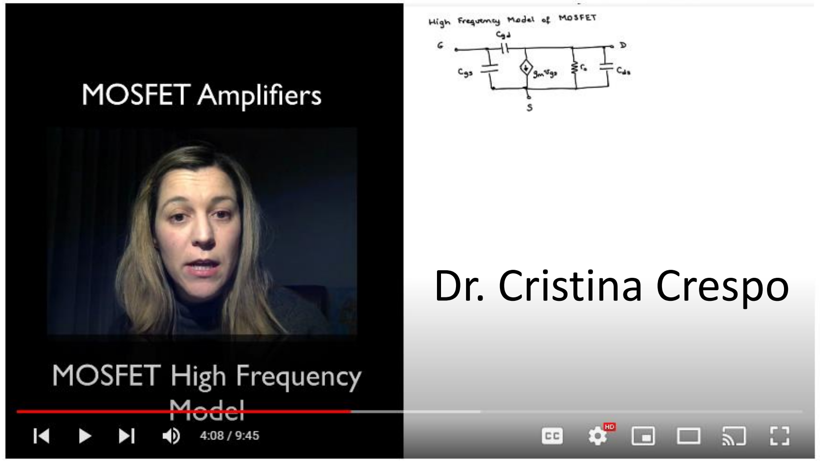


Semiconductor Devices: Miller's Theorem

Electronics with Professor Fiore
7.24K subscribers

https://youtu.be/yM9xlbAf43Q

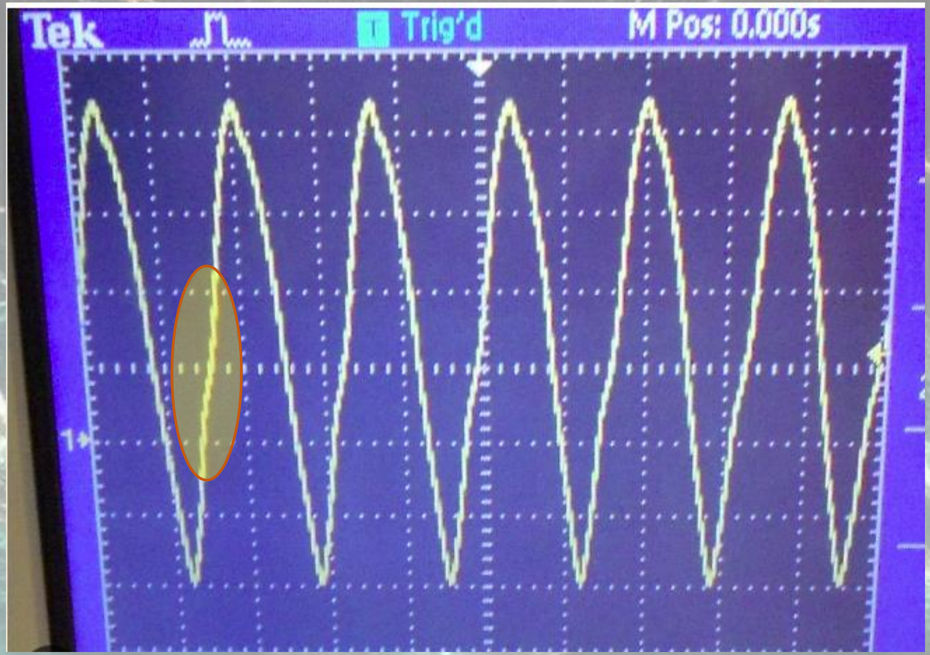
Mateo Aboy
14.2K subscribers



MOSFET High Frequency Model

https://youtu.be/19kXfUPdF9I

MILLER "DISTORTION"



This has been exaggerated for illustration purposes

Miller Neutralization: Kick in Bag Pipes

1. **Reduce the gain hence reduce Miller Capacitance**
   - ✓ **Use HYCAS or *CASCODE* amplifiers. Add common base, common gate stage**
   - ✓ ***Negative feedback***

SAME

2. **Increase the input drive to compensate for the low input impedance**

3. **Change the RC time constant for the internal capacitors (faster turn on)**

4. **Increase the current to reduce the charge time of the capacitors (faster turn on)**
   - ✓ **Use *positive feedback***

AGENDA

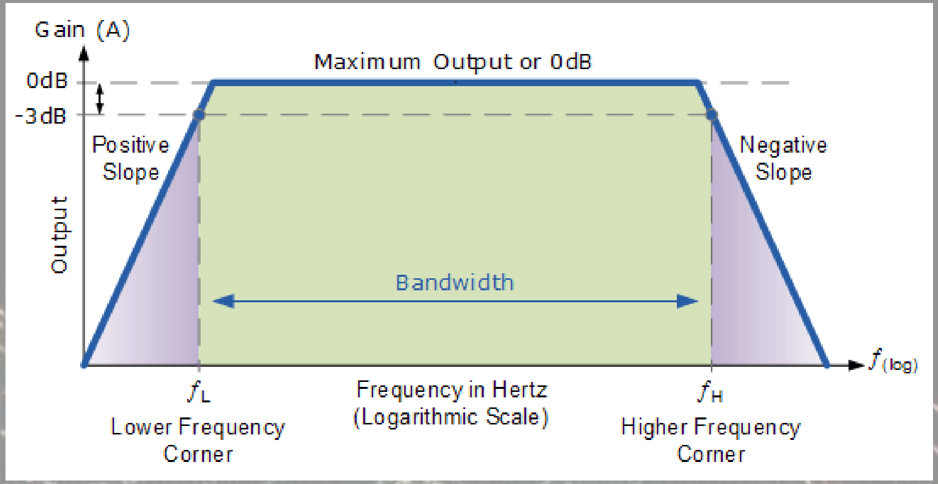
Captain, I kicked Dave in the bag pipes..twice

1. VE3OOI Simplified Model

2. "Feedback Amplifier" Model

3. Signal Flow Charts & Mason Gain Formula

GOALS



1. Need to calculate maximum gain **(Midband Analysis)**
   ✓Used for Miller impedance and capacitance

2. Need to calculate amplifier cut off frequency **(3dB Frequency Analysis)**
   ✓Used to ensure you have necessary performance

3. Need to calculate gain at frequency of interest **(High Frequency Analysis)**

Notice the word "calculate"

Mid Band Analysis
(Low Frequency Analysis)

3dB Frequency Analysis

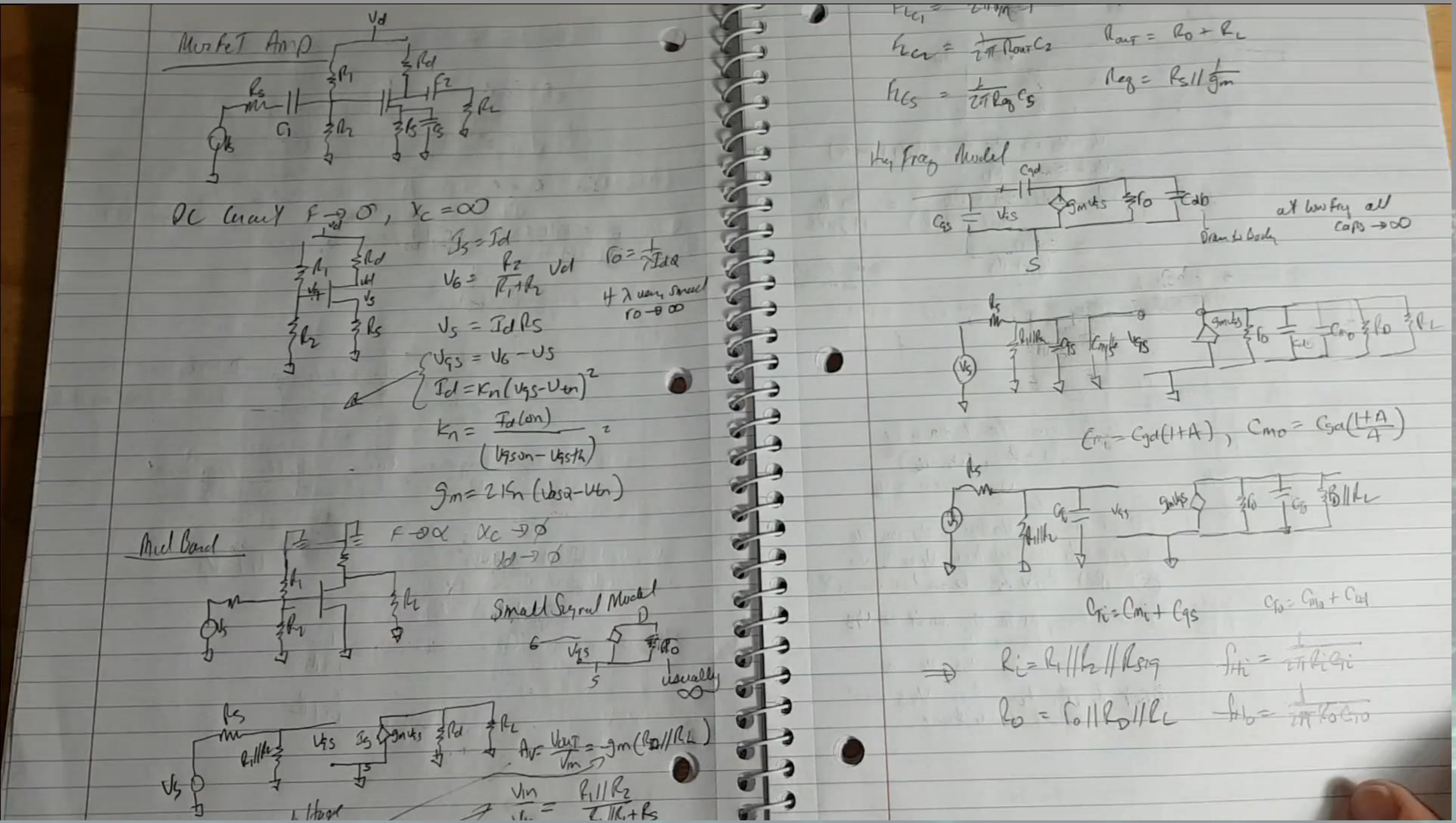
Another WTF!

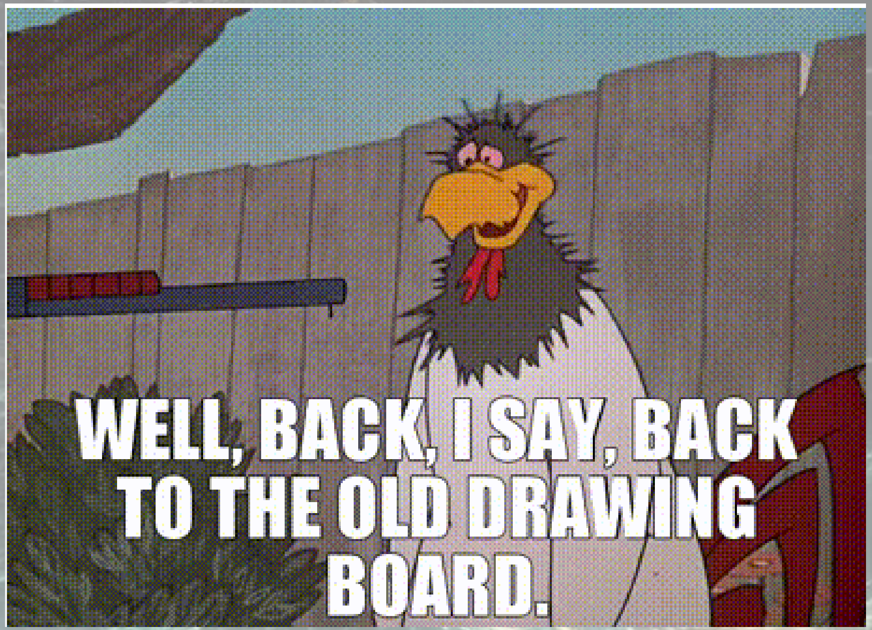
- I started out using 400mVp input signal for testing
- Spend weeks and weeks trying to understand why my simplified model was not working
- Learned a couple of things:
  1. If you have distortion, RMS values are skewed. Need to make sure amp is 100% linear (400mV input was overdriving MOSFET!)
  2. AC signal on a DC offset changes RMS values (painful memories of OWAEC)
  3. RMS current and voltages are scalars numbers and does not include phase. Can't add RMS signals that are out of phase.

Cannot make predictions without Sophisticated calculations!!

Can only make rough estimates

After many months of agony….





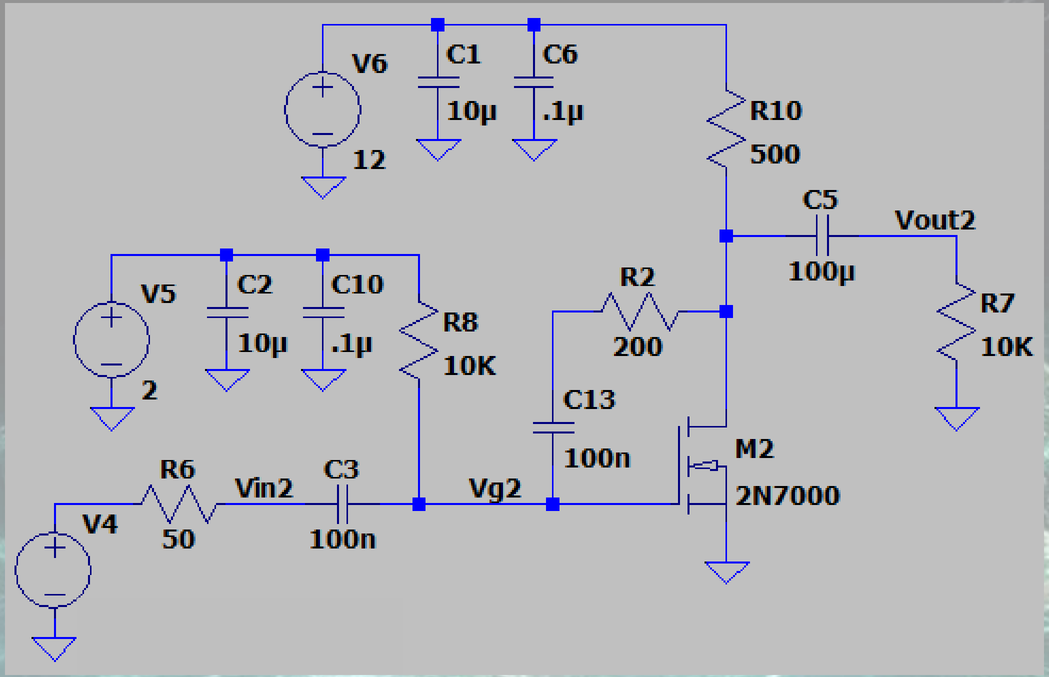
Cannot make predictions without Sophisticated calculations!!

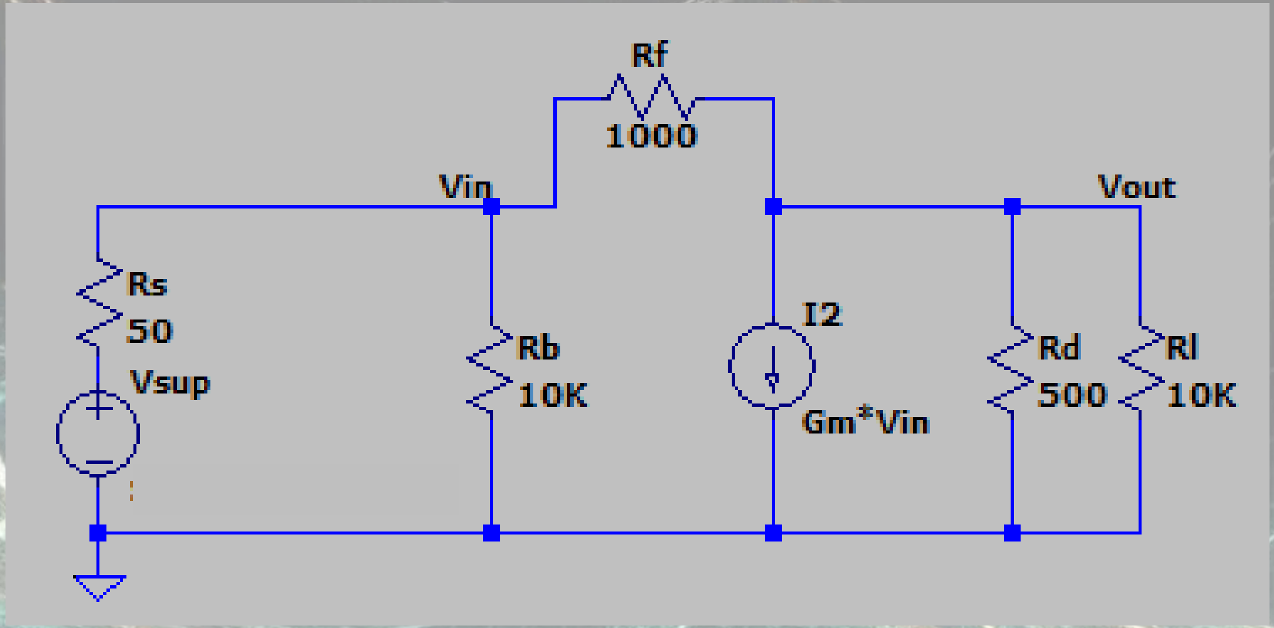
Can only make rough estimates

General Outcome

How to make RF amplifier measurements

Simplified Model: AC MODEL



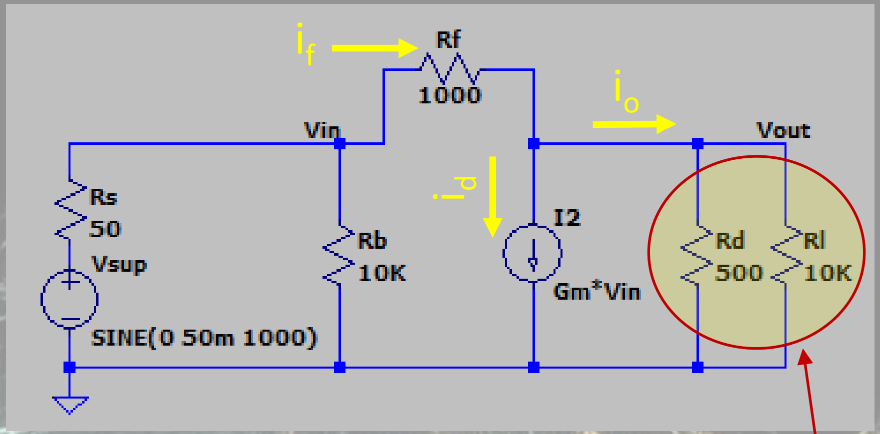


For low frequency/midband "AC" analysis:

1. Ground all DC sources
2. Short all DC blocking capacitors (i.e., large value caps)
3. Replace BJT or MOSFET with small signal model

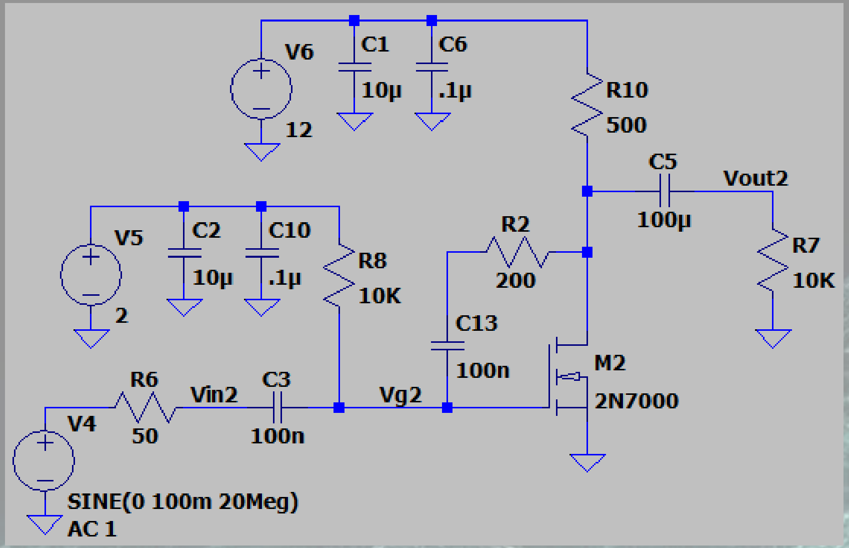
Simplified Model: Gain Math

- $i_f = i_d + i_o$
- $V_g = V_{in}$ & $V_d = V_{out}$
  - $R_o = R_D // R_L$
  - $i_o = V_{out}/R_o$
  - $i_d = G_m V_{in}$
  - $i_f = (V_{in} - V_{out})/R_f$
- $(V_{in} - V_{out})/R_f = G_m V_{in}/R_b + V_{out}/R_o$
- $V_{in}/R_f - V_{out}/R_f = V_{out}/R_o + G_m V_{in}$
- $V_{out}(1/R_f + 1/R_o) = V_{in}/R_f - G_m V_{in} = V_{in}\ (1/R_f - G_m V_{in})$
- $A_v = V_{out}/\ V_{in} = (1/R_f - G_m V_{in})\ /\ (1/R_f + 1/R_o)$
  - $R_F // R_o = 1/\ (1/R_f + 1/R_o)$
- $A_v = (1/R_f - G_m V_{in})\ R_F // R_o = (1/R_f - G_m)\ R_F // R_D // R_L$



$R_o = R_D // R_L$

Simplified Model: Gain Calculation



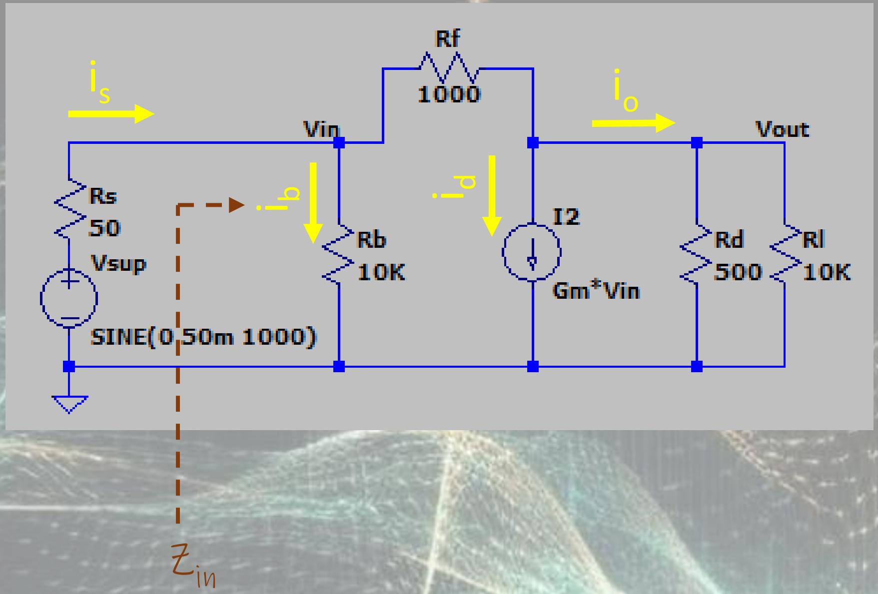
$$A_V = (1/R_f - G_m V_{in}) R_F // R_D // R_L$$

	RMS					
Input (Peak)	0.05	0.05	0.05	0.05	0.05	0.05
Gm	0.0663	0.0663	0.0663	0.0663	0.0663	0.0663
Cal No FB Gain	31.6	31.6	31.6	31.6	31.6	31.6
LTSpice No FB Gain	30.1	30.1	30.1	30.1	30.1	30.1
LTSpice FB Gain	4.4	8.2	14.9	18.0	20.0	24.1
FB Formula Gain	4.3	8.0	14.4	17.3	19.3	22.4
LTSpice Rin	18.6	21.8	31.4	39.4	47.4	79.1
LTSpice Rout	33.6	53.5	103.7	137.3	165.3	242.6
Rf	100	200	500	750	1000	2000
Rb	10000	10000	10000	10000	10000	10000
Rs	50	50	50	50	50	50
Rl	10000	10000	10000	10000	10000	10000
Rd	500	500	500	500	500	500
Vout	0.041889	0.0874874	0.202629	0.279525	0.343683	0.520511
Vd	3.52636	3.52786	3.53382	3.53942	3.54505	3.56435
Vg	1.99979	1.99975	1.99968	1.99964	1.99961	1.99956
Vgac	0.00953195	0.0106825	0.0135924	0.0155357	0.0171569	0.0216238
Vs	0.0353341	0.0353272	0.0353273	0.035325	0.0353223	0.0353147
Vin	0.0353341	0.0353272	0.0353273	0.035325	0.0353223	0.0353147
Vb	2	2	2	2	2	2
if	0.000513995	0.000490784	0.00043243	0.00039341	0.00036083	0.000271062
ig (Mosfet)	0.000000012	0.000000020	0.00000004	0.00000006	0.00000007	0.000000102
id (Mosfet)	0.012953400	0.012956300	0.01296650	0.01297580	0.01298500	0.013018800
is (Mosfet)	0.012953400	0.012956300	0.01296650	0.01297580	0.01298500	0.013018800
ib	0.000000953	0.000001068	0.00000136	0.00000155	0.00000172	0.000002162
is	0.000514948	0.000491853	0.00043379	0.00039496	0.00036255	0.000273224
id	0.012948000	0.012947600	0.01295030	0.01295530	0.01296150	0.012989500
il	0.000004189	0.000008749	0.00002026	0.00002795	0.00003437	0.000052051
Xc Miller at 1KHz	88609					

Av (1/Rf-gm)Rf//Ro	-4.7	-8.6	-15.7	-18.9	-21.1	-25.3
LTSpice Gain	4.4	8.2	14.9	18.0	20.0	24.1

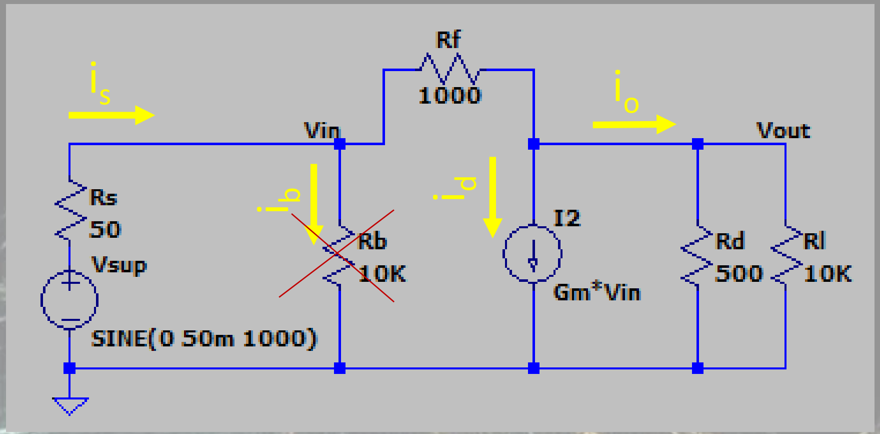
Simplified Model: Zin Math – 1st Way

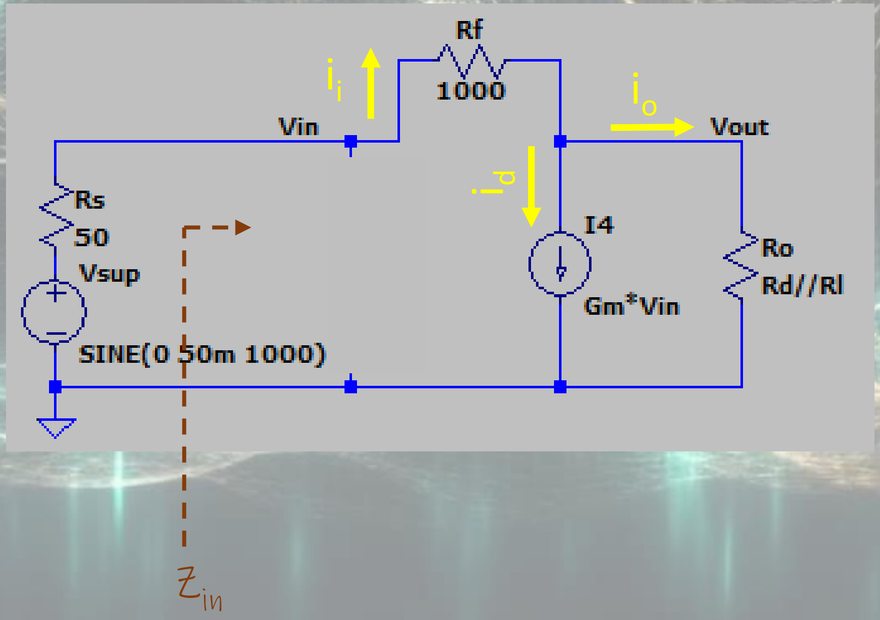
- $i_s = i_b + i_d + i_o$
  - ✓ $V_g = V_{in}$ & $V_d = V_{out}$
  - ✓ $i_b = V_{in}/R_b$
  - ✓ $i_o = V_{out}/R_o$
  - ✓ $i_d = G_m V_{in}$
- $i_s = V_{in}/R_b + G_m V_{in} + V_{out}/R_o$
- $V_{out}/R_o = i_s - V_{in}/R_b - G_m V_{in}$
- $V_{out} = i_s R_o - V_{in}/R_b R_o - G_m V_{in} R_o$
  - ✓ $i_f = (V_{in} - V_{out})/R_f$
  - ✓ $i_f = i_s - i_b = i_s - V_{in}/R_b$
  - ✓ $(V_{in} - V_{out}) = R_f i_s - R_f V_{in}/R_b$
  - ✓ $V_{out} = V_{in} - R_f i_s + R_f V_{in}/R_b$
- $V_{in} - R_f i_s + R_f V_{in}/R_b = i_s R_o - V_{in}/R_b R_o - G_m V_{in} R_o$
- $R_f i_s + i_s R_o = R_f V_{in}/R_b + V_{in}/R_b R_o + G_m V_{in} R_o$
- $i_s(R_f + R_o) = V_{in}(R_f/R_b + 1/R_b R_o + G_m R_o)$
- $Z_{in} = V_{in}/i_s = (R_f + R_o)/(R_f/R_b + 1/R_b R_o + G_m R_o) = R_b(R_f + R_o)/(R_f + R_o + G_m R_o R_b)$



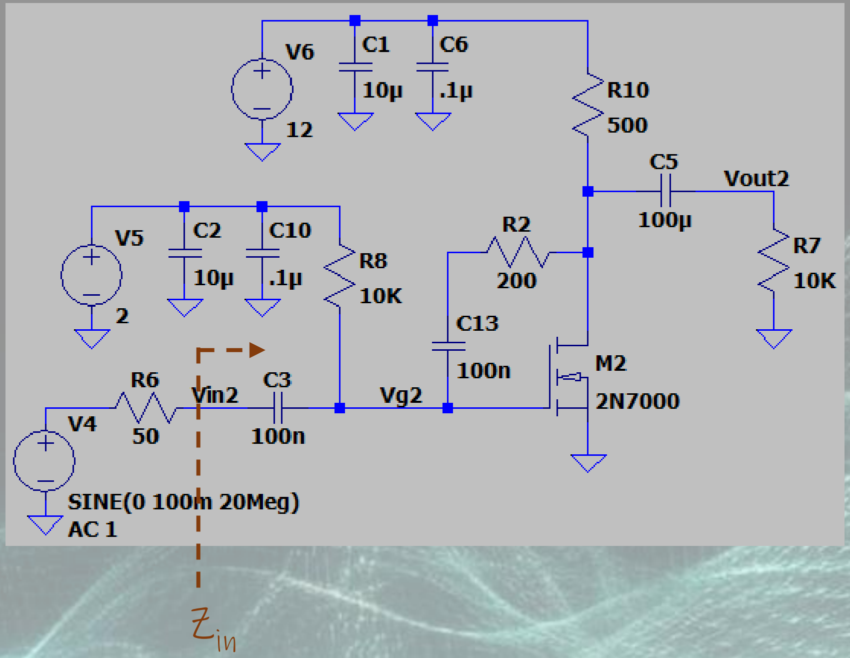
Simplified Model: Zin Math – 2nd Way

- $i_i = i_d + i_o$
  - ✓ $V_g = V_{in}$ & $V_d = V_{out}$ & $i_f = i_i$
  - ✓ $i_o = V_{out}/R_o$
  - ✓ $i_d = G_m V_{in}$
- $i_f = i_i = G_m V_{in} + V_{out}/R_o$
- $V_{out}/R_o = i_i - G_m V_{in}$
- $V_{out} = i_i R_o - G_m V_{in} R_o$
  - ✓ $i_i = i_f = (V_{in} - V_{out})/R_f$
  - ✓ $V_{out} = V_{in} - i_i R_f$
- $V_{in} - i_i R_f = i_i R_o - G_m V_{in} R_o$
- $V_{in} + G_m V_{in} R_o = i_i R_f + i_i R_o$
- $V_{in} (1 + G_m R_o) = i_i (R_f + R_o)$
- $Z_{in} = V_{in}/i_s = (R_f + R_o) / (1 + G_m R_o)$





Simplified Model: Zin Calculation



$$Z_{in} = V_{in}/i_s = R_b(R_f+R_o) / (R_f+R_o+GmR_oR_b)$$

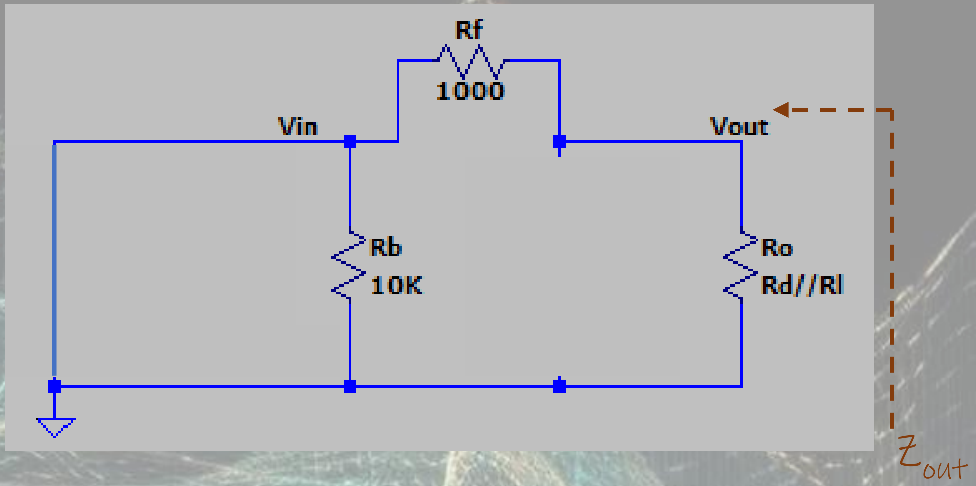
$$Z_{in} = V_{in}/i_s = (R_f+R_o) / (1+G_mR_o)$$

	RMS					
Input (Peak)	0.05	0.05	0.05	0.05	0.05	0.05
Gm	0.0663	0.0663	0.0663	0.0663	0.0663	0.0663
Cal No FB Gain	31.6	31.6	31.6	31.6	31.6	31.6
LTSpice No FB Gain	30.1	30.1	30.1	30.1	30.1	30.1
LTSpice FB Gain	4.4	8.2	14.9	18.0	20.0	24.1
FB Formula Gain	4.3	8.0	14.4	17.3	19.3	22.4
LTSpice Rin	18.6	21.8	31.4	39.4	47.4	79.1
LTSpice Rout	33.6	53.5	103.7	137.3	165.3	242.6
Rf	100	200	500	750	1000	2000
Rb	10000	10000	10000	10000	10000	10000
Rs	50	50	50	50	50	50
Rl	10000	10000	10000	10000	10000	10000
Rd	500	500	500	500	500	500
Vout	0.041889	0.0874874	0.202629	0.279525	0.343683	0.520511
Vd	3.52636	3.52786	3.53382	3.53942	3.54505	3.56435
Vg	1.99979	1.99975	1.99968	1.99964	1.99961	1.99956
Vgac	0.00953195	0.0106825	0.0135924	0.0155357	0.0171569	0.0216238
Vs	0.0353341	0.0353272	0.0353273	0.035325	0.0353223	0.0353147
Vin	0.0353341	0.0353272	0.0353273	0.035325	0.0353223	0.0353147
Vb	2	2	2	2	2	2
if	0.000513995	0.000490784	0.00043243	0.00039341	0.00036083	0.000271062
ig (Mosfet)	0.000000012	0.000000020	0.00000004	0.00000006	0.00000007	0.000000102
id (Mosfet)	0.012953400	0.012956300	0.01296650	0.01297580	0.01298500	0.013018800
is (Mosfet)	0.012953400	0.012956300	0.01296650	0.01297580	0.01298500	0.013018800
ib	0.000000953	0.000001068	0.00000136	0.00000155	0.00000172	0.000002162
is	0.000514948	0.000491853	0.00043379	0.00039496	0.00036255	0.000273224
id	0.012948000	0.012947600	0.01295030	0.01295530	0.01296150	0.012989500
il	0.000004189	0.000008749	0.00002026	0.00002795	0.00003437	0.000052051
Xc Miller at 1KHz	88609					

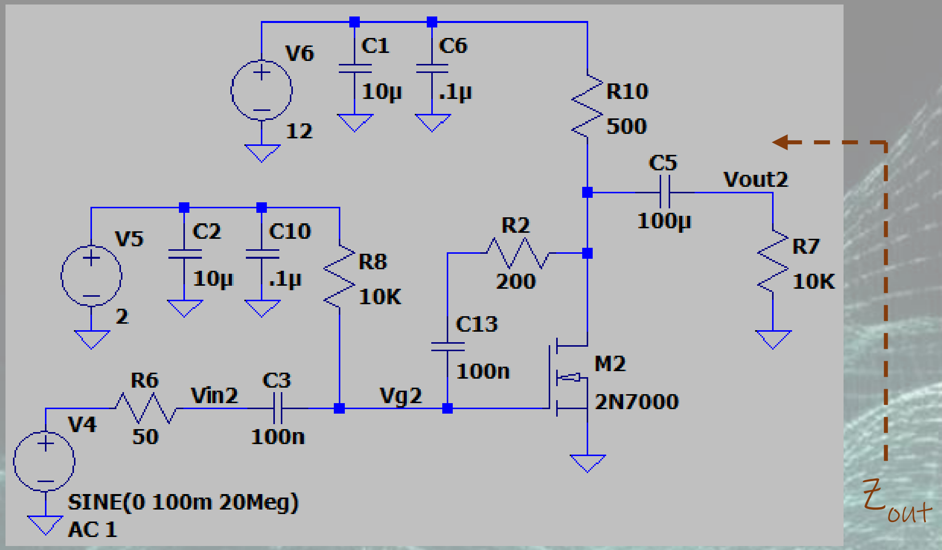
Rin Rb(Ro+Rf)/(Rf+Ro+gmRoRb)	26.2	21.4	30.8	38.7	46.5	77.8
Rin [(Ro+Rf)/(1+GmRo)]	25.2	20.8	30.0	37.6	45.3	76.0
LTSpice Rin	18.6	21.8	31.4	39.4	47.4	79.1

Simplified Model: Zout Math

- Remove Current source and short voltage source
  - ✓ R_b is shorted and can be removed
  - ✓ R_o and R_F are left
- $Z_{out} = R_f // R_o = R_f // R_D // R_L$



Simplified Model: Zout Calculation



$$Z_{out} = R_f // R_o = R_f // R_D // R_L$$

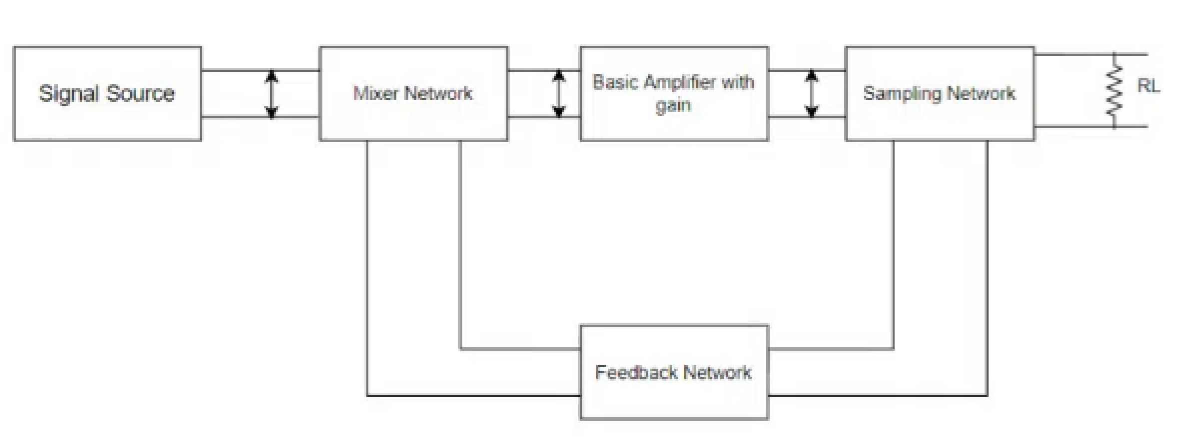
	RMS					
Input (Peak)	0.05	0.05	0.05	0.05	0.05	0.05
Gm	0.0663	0.0663	0.0663	0.0663	0.0663	0.0663
Cal No FB Gain	31.6	31.6	31.6	31.6	31.6	31.6
LTSpice No FB Gain	30.1	30.1	30.1	30.1	30.1	30.1
LTSpice FB Gain	4.4	8.2	14.9	18.0	20.0	24.1
FB Formula Gain	4.3	8.0	14.4	17.3	19.3	22.4
LTSpice Rin	18.6	21.8	31.4	39.4	47.4	79.1
LTSpice Rout	33.6	53.5	103.7	137.3	165.3	242.6
Rf	100	200	500	750	1000	2000
Rb	10000	10000	10000	10000	10000	10000
Rs	50	50	50	50	50	50
Rl	10000	10000	10000	10000	10000	10000
Rd	500	500	500	500	500	500
Vout	0.041889	0.0874874	0.202629	0.279525	0.343683	0.520511
Vd	3.52636	3.52786	3.53382	3.53942	3.54505	3.56435
Vg	1.99979	1.99975	1.99968	1.99964	1.99961	1.99956
Vgac	0.00953195	0.0106825	0.0135924	0.0155357	0.0171569	0.0216238
Vs	0.0353341	0.0353272	0.0353273	0.035325	0.0353223	0.0353147
Vin	0.0353341	0.0353272	0.0353273	0.035325	0.0353223	0.0353147
Vb	2	2	2	2	2	2
if	0.000513995	0.000490784	0.00043243	0.00039341	0.00036083	0.000271062
ig (Mosfet)	0.000000012	0.000000020	0.00000004	0.00000006	0.00000007	0.000000102
id (Mosfet)	0.012953400	0.012956300	0.01296650	0.01297580	0.01298500	0.013018800
is (Mosfet)	0.012953400	0.012956300	0.01296650	0.01297580	0.01298500	0.013018800
ib	0.000000953	0.000001068	0.00000136	0.00000155	0.00000172	0.000002162
is	0.000514948	0.000491853	0.00043379	0.00039496	0.00036255	0.000273224
id	0.012948000	0.012947600	0.01295030	0.01295530	0.01296150	0.012989500
il	0.000004189	0.000008749	0.00002026	0.00002795	0.00003437	0.000052051
Xc Miller at 1KHz	88609					

Zout (Ro//Rf)	82.6	140.8	243.9	291.3	322.6	384.6
LTSpice Rout	82.5	140.8	243.9	291.2	322.6	384.6

Mid Band Analysis (Low Frequency Analysis)

"Feedback Amplifier" Model

Feedback Amplifier Model: Egg Heads

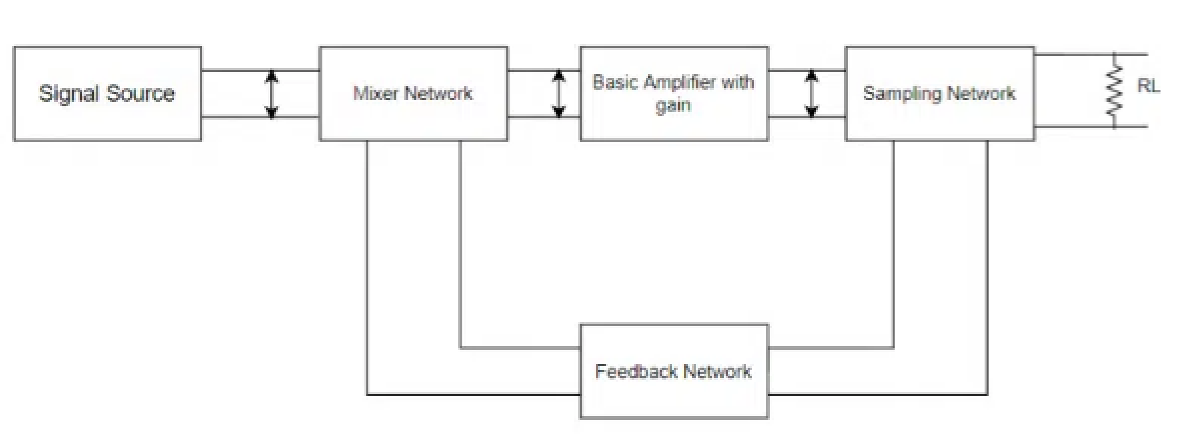


Characteristics	Types of Feedback			
	Voltage-Series	Voltage-Shunt	Current-Series	Current-Shunt
Voltage Gain	Decreases	Decreases	Decreases	Decreases
Bandwidth	Increases	Increases	Increases	Increases
Input resistance	Increases	Decreases	Increases	Decreases
Output resistance	Decreases	Decreases	Increases	Increases
Harmonic distortion	Decreases	Decreases	Decreases	Decreases
Noise	Decreases	Decreases	Decreases	Decreases

Topology	Closed-Loop Gain A_f	Input Resistance R_{if}	Output Resistance R_{of}
Voltage-Sampling Series-Mixing	$A/(1+A\beta)$	$R_i(1+A\beta)$	$R_o/(1+A\beta)$
Current-Sampling Series-Mixing	$A/(1+A\beta)$	$R_i(1+A\beta)$	$R_o(1+A\beta)$
Voltage-Sampling Shunt-Mixing	$A/(1+A\beta)$	$R_i/(1+A\beta)$	$R_o/(1+A\beta)$
Current-Sampling Shunt-Mixing	$A/(1+A\beta)$	$R_i/(1+A\beta)$	$R_o(1+A\beta)$

Beta is feedback factor or proportion of current/voltage fed back

Do you really think it was that easy?!



- **This assumes it's a "Transresistance" amplifier and the AC/Hybrid model is different.**
  - **Input is a current and output is a voltage**
    - **Gain is Rm = Vo/Is (Vo output voltage, Is input current)**
    - **Remember that V/I is a resistance hence a transresistance**

I could not get this approach to work.

Gave up…life is too short

Mid Band Analysis (Low Frequency Analysis)

Signal Flow Charts and Mason Gain Formula

SIGNAL FLOW CHARTS

Collection of Solved Feedback Amplifier Problems

This document contains a collection of solved feedback amplifier problems involving one or more active devices. The solutions make use of a graphical tool for solving simultaneous equations that is called the Mason Flow Graph (also called the Signal Flow Graph). When set up properly, the graph can be used to obtain by inspection the gain of a feedback amplifier, its input resistance, and its output resistance without solving simultaneous equations. Some background on how the equations are written and how the flow graph is used to solve them can be found at

http://users.ece.gatech.edu/~mleach/ece3050/notes/feedback/fdbkamps.pdf

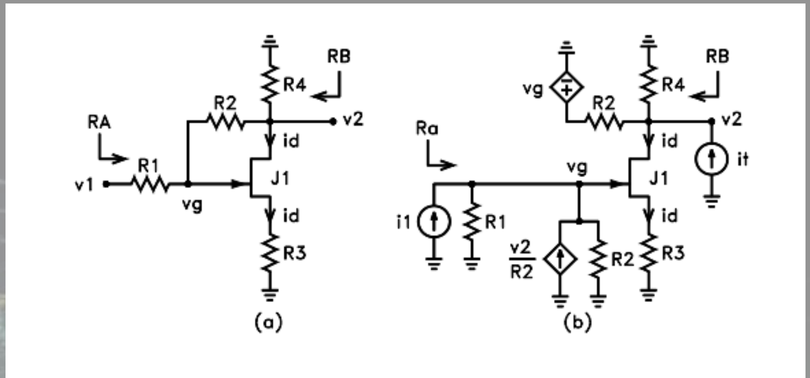


Figure 12: (a) Amplifier circuit. (b) Circuit with feedback removed.

https://leachlegacy.ece.gatech.edu/ece3050/notes/feedback/FBExamples.pdf

SIGNAL FLOW CHARTS

https://leachlegacy.ece.gatech.edu/ece3050/notes/feedback/FBExamples.pdf

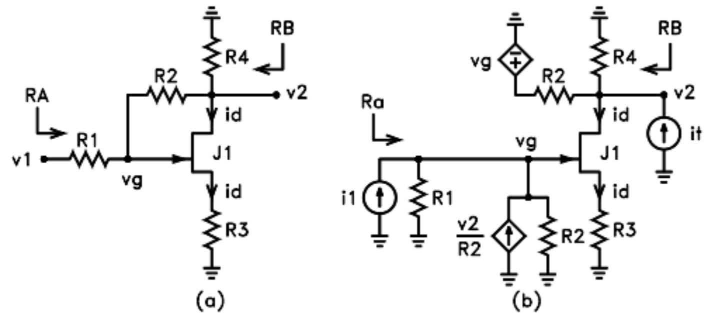
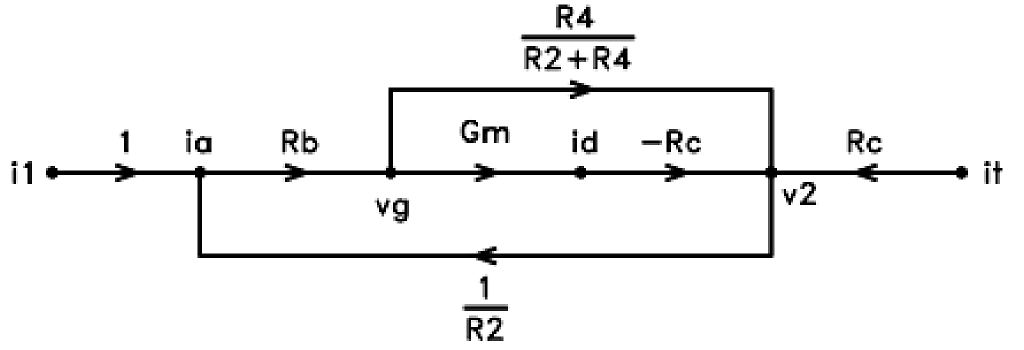


Figure 12: (a) Amplifier circuit. (b) Circuit with feedback removed.



For the circuit with feedback removed, we can write

$$v_g = i_1 R_b + \frac{v_2}{R_2} R_b \qquad R_b = R_1 \| R_2 \qquad i_d = G_m v_g \qquad G_m = \frac{1}{r_s + R_3}$$

$$v_2 = -i_d R_c + i_t R_c + v_g \frac{R_4}{R_2 + R_4} \qquad R_c = R_2 \| R_4$$

$$\begin{aligned} \Delta &= 1 - R_b \times \left[G_m \times -R_c + \frac{R_4}{R_2 + R_4} \right] \times \frac{1}{R_2} \\ &= 1 + R_b \times \left[G_m \times R_c - \frac{R_4}{R_2 + R_4} \right] \times \frac{1}{R_2} \end{aligned}$$

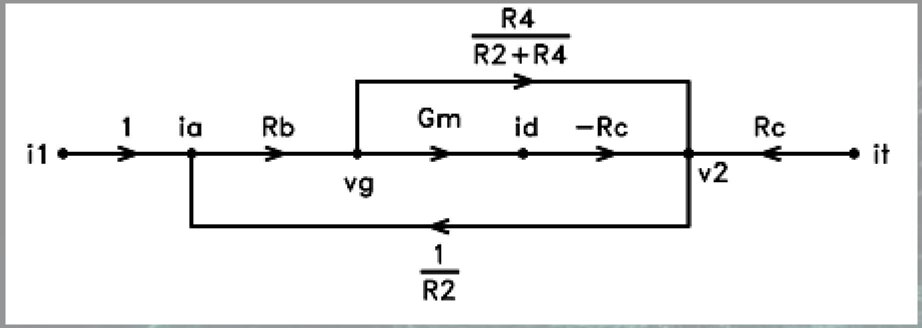
$$\begin{aligned} A &= -R_b \times \left[G_m \times R_c - \frac{R_4}{R_2 + R_4} \right] \\ &= -(R_1 \| R_2) \times \left[G_m \times R_2 \| R_4 - \frac{R_4}{R_2 + R_4} \right] \end{aligned}$$

$$R_a = \frac{v_g}{i_1} = \frac{R_b}{\Delta}$$

$$R_A = R_1 + \left(\frac{1}{R_a} - \frac{1}{R_1} \right)^{-1}$$

$$R_B = \frac{v_2}{i_t} = \frac{R_c}{\Delta}$$

Simplified Model: Zout Calculation



Input (Peak)	0.05	0.05	0.05	0.05	0.05	0.05
Gm	0.0663	0.0663	0.0663	0.0663	0.0663	0.0663
Cal No FB Gain	31.6	31.6	31.6	31.6	31.6	31.6
LTSpice No FB Gain	30.1	30.1	30.1	30.1	30.1	30.1
LTSpice FB Gain	4.4	8.1	14.8	17.9	20.0	24.1
FB Formula Gain	4.3	8.0	14.4	17.3	19.3	22.4
LTSpice Rin	18.7	21.9	31.5	39.5	47.4	79.2
LTSpice Rout (Input Unterminated)	15.4	15.6	16.0	16.4	16.8	18.3
LTSpice Rout (Input terminated)	33.6	53.5	103.7	137.3	165.3	242.6
Rf	100	200	500	750	1000	2000
Rb	10000	10000	10000	10000	10000	10000
Rs	0.0001	0.0001	0.0001	0.0001	0.0001	0.0001
Rl	10000	10000	10000	10000	10000	10000
Rd	500	500	500	500	500	500

Signal Flow Chart and Mason Gain Formula						
Req	99.01	196.08	476.19	697.67	909.09	1666.67
Rc	82.64	140.85	243.90	291.26	322.58	384.62
Rd'	476.19	476.19	476.19	476.19	476.19	476.19
Det	5.61	9.46	15.94	18.60	20.15	22.09
A	-460.68	-1692.90	-7468.06	-13201.63	-19149.56	-42179.49
Beta	-0.010000	-0.005000	-0.002000	-0.001333	-0.001000	-0.000500
Gain	-4.65	-8.63	-15.68	-18.92	-21.06	-25.31
Ralpha	17.66	20.72	29.88	37.51	45.12	75.45
Rin	17.66	20.72	29.88	37.51	45.12	75.45
Rout	14.74	14.88	15.31	15.66	16.01	17.41
LTSpice Rin	18.67	21.87	31.47	39.46	47.43	79.19
LTSpice Rout (Input Unterminated)	15.44	15.59	16.04	16.41	16.78	18.26
LTSpice FB Gain	4.4	8.1	14.8	17.9	20.0	24.1

GOALS

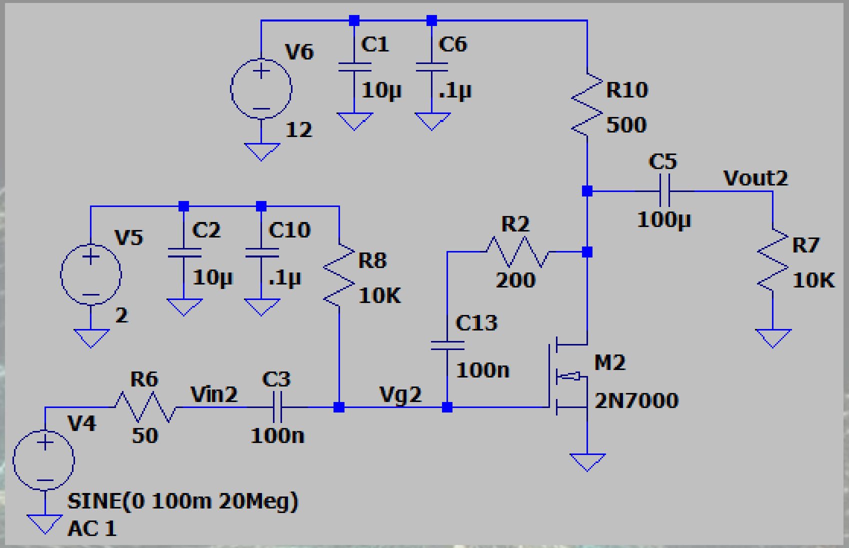
1. ~~Need to calculate maximum gain (Low Frequency Analysis)~~
   - ✓ ~~Used for Miller impedance and capacitance~~
2. Need to calculate amplifier bandwidth (3dB Frequency Analysis)
   - ✓ Used to ensure you have necessary performance
3. Need to calculate gain at frequency of interest (High Frequency Analysis)

-3dB Analysis (High Frequency Cutoff)

VE3OOI Simplified Model

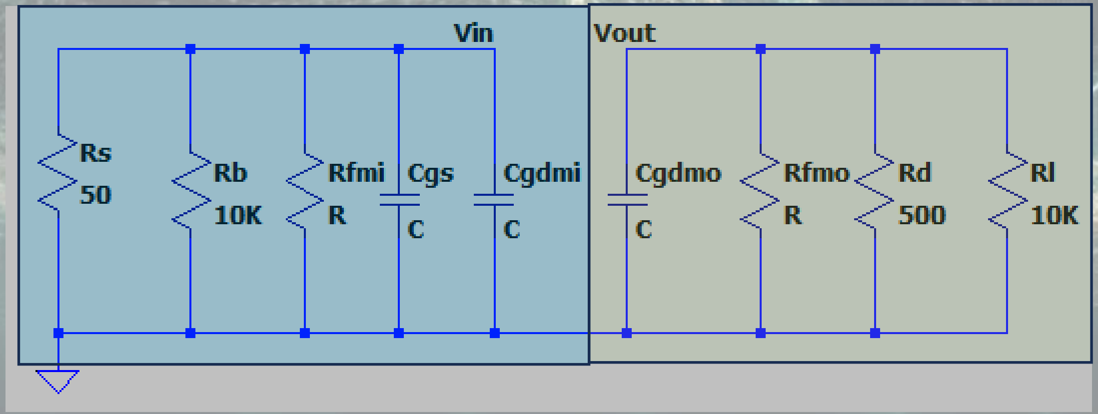
Simplified Model: Bandwidth

- Need to short voltage source and open current source. Separate Input side from Output side
- Need to add Miller intrinsic capacitance to input and outputs
- Need to move "Millerized" Feedback resistor to input and outputs
- Calculate 3dB cutoff frequency for LPF $F = 1/(2*\pi*R_{eq}*C_{eq})$



For Input Side

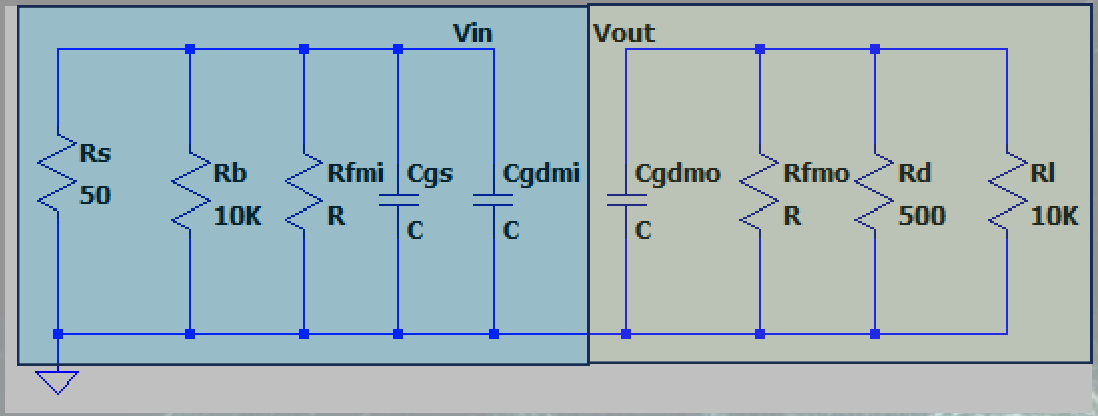
- $C_{miller(in)} = C_{gd}(1+A) + C_{gs}$
- $R_{miller(in)} = R_f/(1+A)$
- $C_{eq} = C_{miller(in)}$
- $R_{eq} = R_{miller(in)} // R_b // R_s$
- $\boxed{F_{in(3dB)} = 1/(2*\pi*R_{eq}*C_{eq})}$



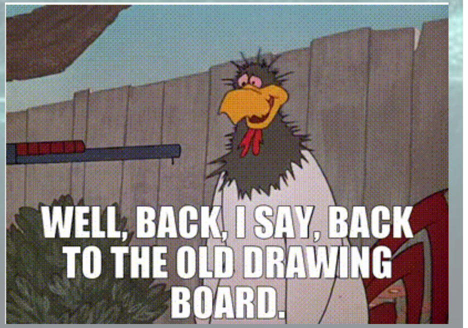
For Output

- $C_{miller(out)} = C_{gd}(1+A)/A$
- $R_{miller(out)} = R_f A/(1+A)$
- $C_{eq} = C_{miller(out)}$
- $R_{eq} = R_{miller(out)} // Rd // R_L$
- $\boxed{F_{out(3dB)} = 1/(2*\pi*R_{eq}*C_{eq})}$

Simplified Model: Bandwidth



LTSpice No FB Gain	30.1	30.1	30.1	30.1	30.1	30.1
Cgs	50	50	50	50	50	50
Cgd	19.3	19.3	19.3	19.3	19.3	19.3
Rf	100	200	500	750	1000	2000
Rb	10000	10000	10000	10000	10000	10000
Rs	50	50	50	50	50	50
Rl	10000	10000	10000	10000	10000	10000
Rd	500	500	500	500	500	500



Rf	100	200	500	750	1000	2000
Cin-Miller	600.7	600.7	600.7	600.7	600.7	600.7
Cout-Miller	19.9	19.9	19.9	19.9	19.9	19.9
Cin	650.7	650.7	650.7	650.7	650.7	650.7
Rfin-Miller	3.2	6.4	16.1	24.1	32.1	64.3
Rfout-Miller	96.8	193.6	483.9	725.9	967.9	1935.7
Rin	3.0	5.7	12.1	16.2	19.5	28.0
Rout	80.4	137.6	240.0	287.6	319.2	382.2
Fi	81.0	43.0	20.1	15.1	12.5	8.7
Fo	99.2	58.0	33.3	27.8	25.0	20.9
LTSpice Higher 3dB	63.0	34.7	15.7	11.6	9.5	6.3

LTSPICE MODELS: Bitten Again

2N7000 VDMOS (Rg=3 Vto=1.6 Rd=0 Rs=.75 Rb=.14 Kp=.17 mtriode=1.25 Cgdmax=80p Cgdmin=12p Cgs=50p Cjo=50p Is=.04p mfg=Fairchild Vds=60 Ron=2 Qg=1.5n)

Model:	2n7000
Id:	1.29e-02
Vgs:	2.00e+00
Vds:	5.53e+00
Vth:	1.60e+00
Gm:	6.63e-02
Gds:	0.00e+00
Cgs:	5.00e-11
Cgd:	1.93e-11
Cbody:	1.96e-11

I used these values which I thought were fixed

ON CHARACTERISTICS

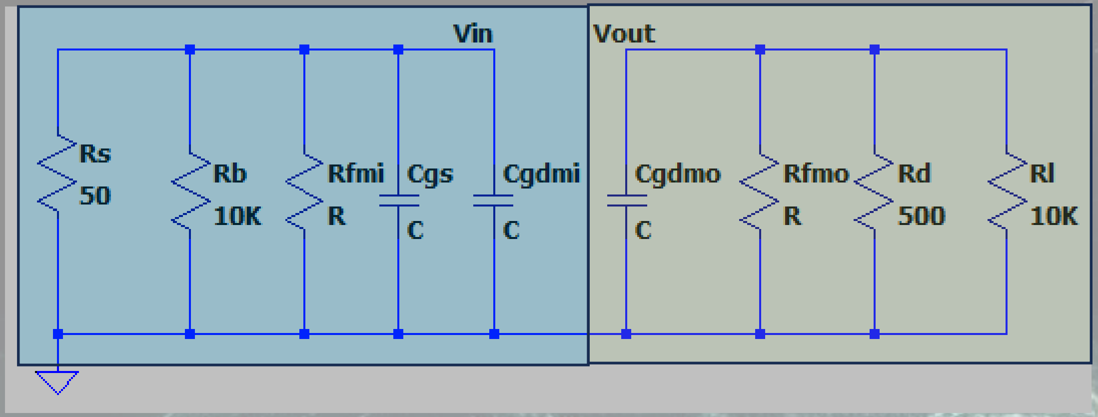
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, I_D = 1 mA	2N7000	0.8	2.1	3	V
		$V_{DS} = V_{GS}$, I_D = 250 µA	2N7002 NDS7002A	1	2.1	2.5	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 200 mA	2N7000	100	320	–	mS
		$V_{DS} \geq 2\ V_{DS(on)}$, I_D = 200 mA	2N7002	80	320	–	
		$V_{DS} \geq 2\ V_{DS(on)}$, I_D = 200 mA	NDS7002A	80	320	–	
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	All	–	20	50	pF
C_{oss}	Output Capacitance		All	–	11	25	
C_{rss}	Reverse Transfer Capacitance		All	–	4	5	

No lead resistances specified.
No range for Cgd provided (except for chart)

Created a custom model for testing purposes

.model 2N7000CUS VDMOS Vto=1.6 Kp=.17 Cgdmax=19.3p Cgdmin=19.3p Cgs=50p mfg=Fairchild Vds=60 Ron=2 Qg=1.5n)

Simplified Model: Bandwidth (Fixed C)



LTSpice No FB Gain	30.1	30.1	30.1	30.1	30.1	30.1
Cgs	50	50	50	50	50	50
Cgd	19.3	19.3	19.3	19.3	19.3	19.3
Rf	100	200	500	750	1000	2000
Rb	10000	10000	10000	10000	10000	10000
Rs	50	50	50	50	50	50
Rl	10000	10000	10000	10000	10000	10000
Rd	500	500	500	500	500	500

Rf	100	200	500	750	1000	2000
Cin-Miller	600.7	600.7	600.7	600.7	600.7	600.7
Cout-Miller	19.9	19.9	19.9	19.9	19.9	19.9
Cin	650.7	650.7	650.7	650.7	650.7	650.7
Rfin-Miller	3.2	6.4	16.1	24.1	32.1	64.3
Rfout-Miller	96.8	193.6	483.9	725.9	967.9	1935.7
Rin	3.0	5.7	12.1	16.2	19.5	28.0
Rout	80.4	137.6	240.0	287.6	319.2	382.2
Fi - Rin	81.0	43.0	20.1	15.1	12.5	8.7
Fo	99.2	58.0	33.3	27.8	25.0	20.9
LTSpice Higher 3dB	78.0	42.3	19.4	14.1	11.6	7.6

GOALS

1. ~~Need to calculate maximum gain (Low Frequency Analysis)~~
   - ✓~~Used for Miller impedance and capacitance~~

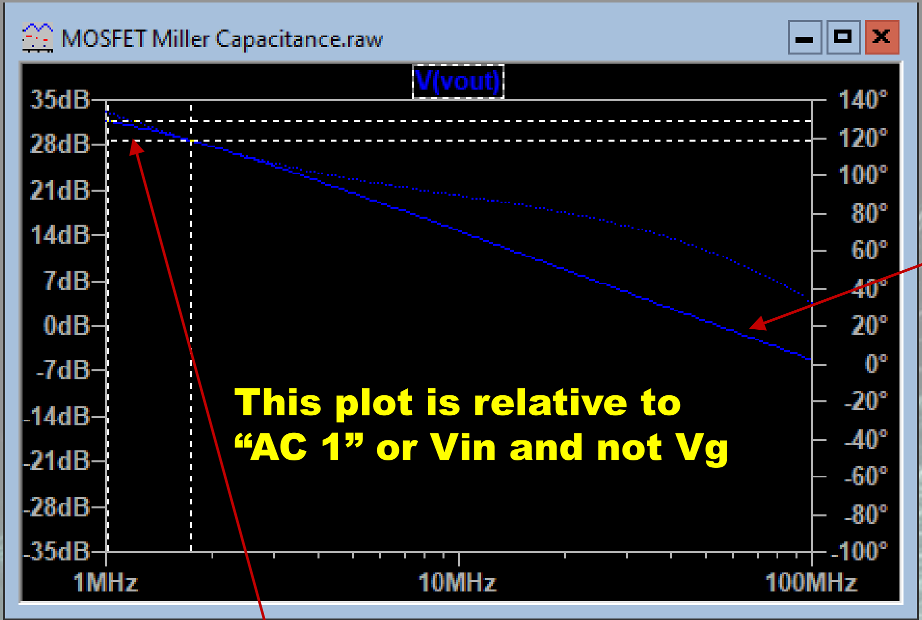
2. ~~Need to calculate amplifier bandwidth (3dB Frequency Analysis)~~
   - ✓~~Used to ensure you have necessary performance~~

3. Need to calculate gain at frequency of interest (High Frequency Analysis)

High Frequency Analysis

(VERY) Simplified Model

Wrap your head around this….

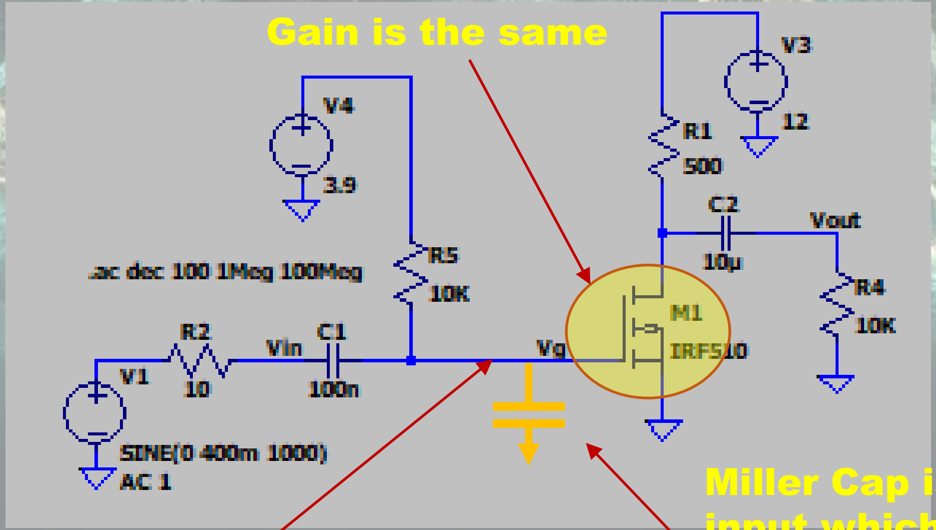


This plot is relative to “AC 1” or Vin and not Vg

This is NOT the actual gain.

This is and ALWAYS will be the gain (maybe larger at lower frequencies)

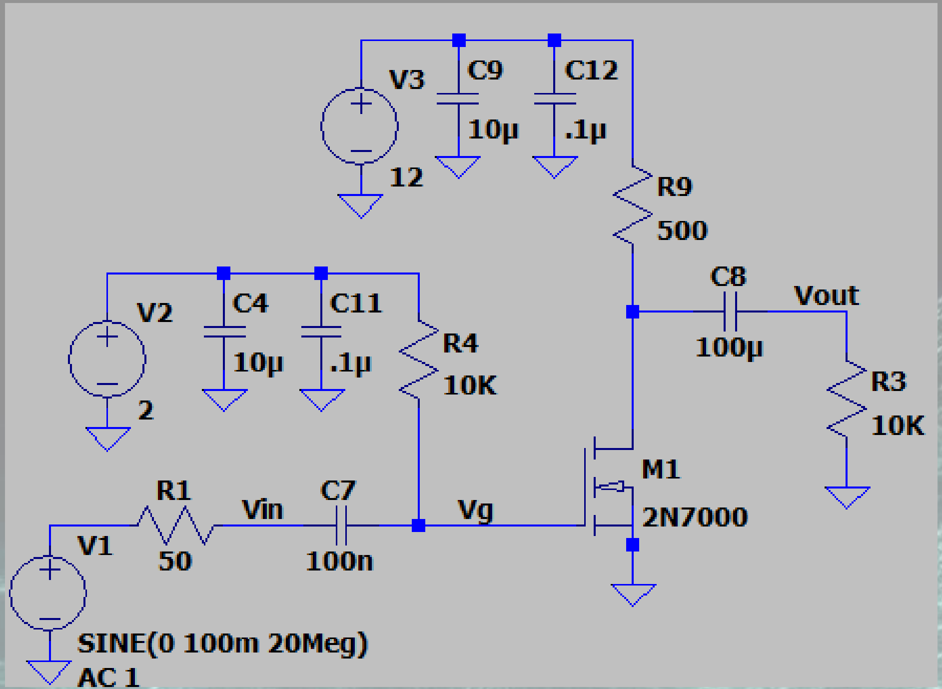
Gain is the same

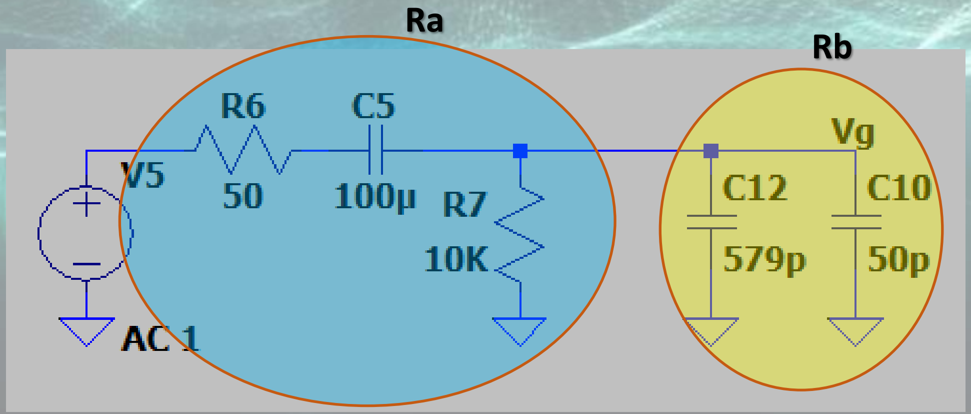


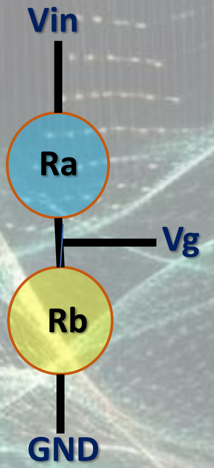
Vin is shorted to ground

Miller Cap is causing lower input which is subjected to same gain at low frequency

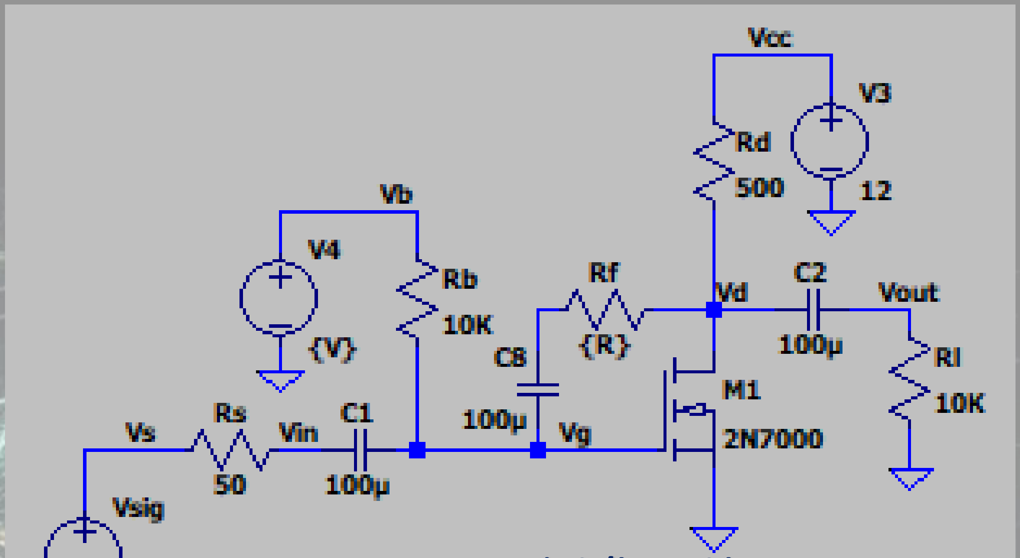
VOLTAGE DIVIDER APPROXIMATION







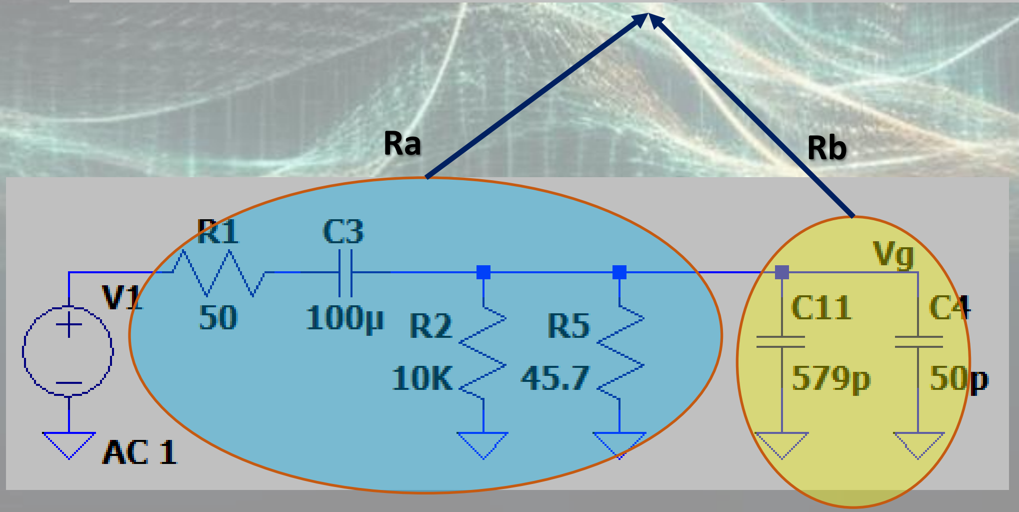
Vg = Vin*Rb/(Ra+Rb)



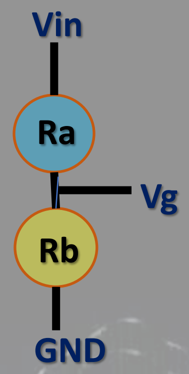
Vg = Vs*Rb/(Ra+Rb)

Vout = Vg*A,

A' = A* Rb/(Ra+Rb)

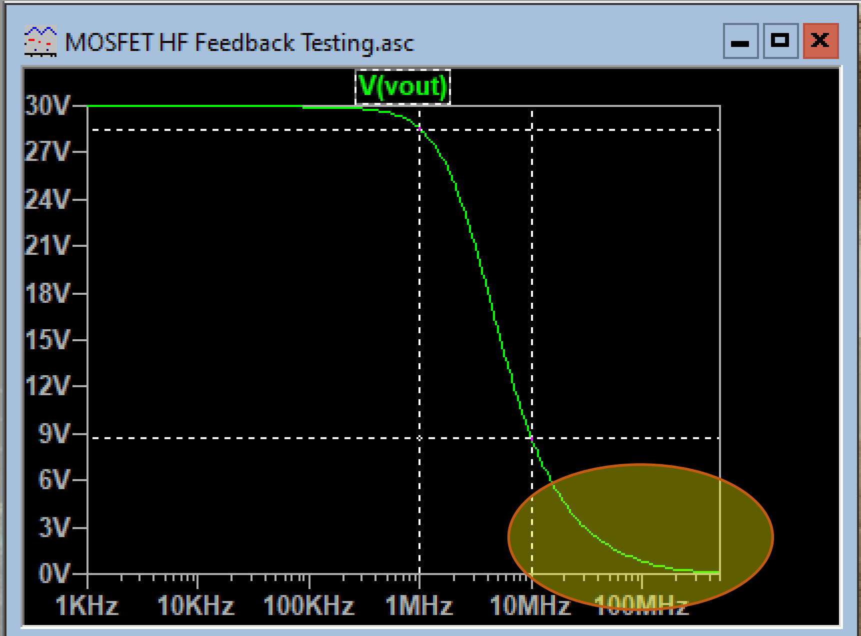


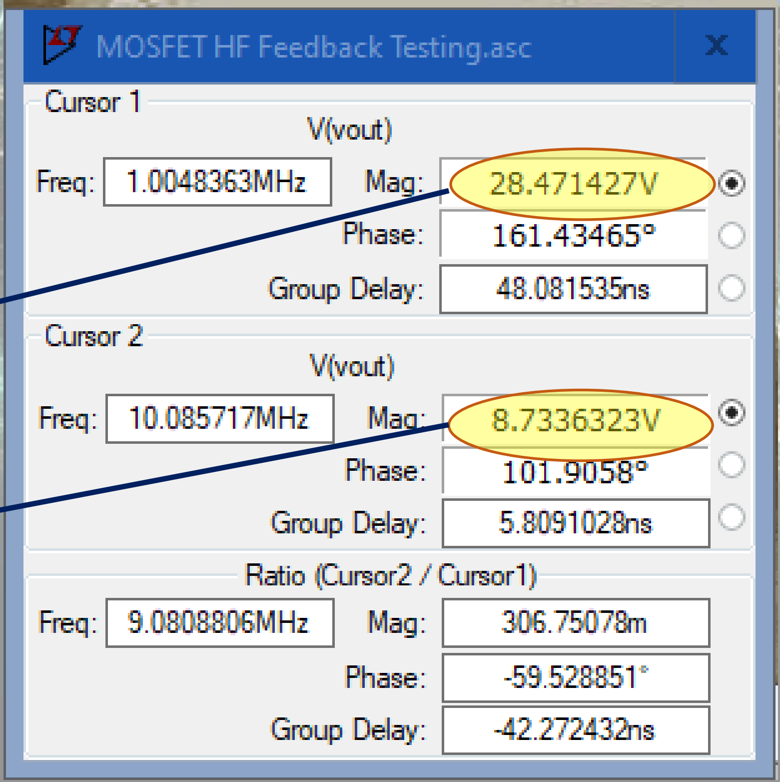
HIGH FREQUENCY ANALYSIS: No Feedback



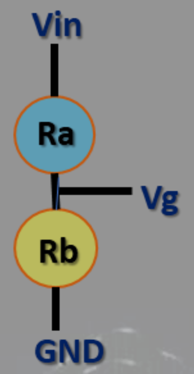
$V_g = V_s * R_b/(R_a+R_b)$
$V_{out} = V_g * A,$
$A' = A * R_b/(R_a+R_b)$

Frequency	Gain (NF)	Rs	Rb	Cgs	Cgd	Cm	Xc	-3dB Frequency	Divider	Gain Out
1000	32.4	50	1000	50	19.3	694.2	229253	4585052	0.9998	32.4
10000	32.4	50	1000	50	19.3	694.2	22925	4585052	0.9978	32.3
20000	32.4	50	1000	50	19.3	694.2	11463	4585052	0.9957	32.2
30000	32.4	50	1000	50	19.3	694.2	7642	4585052	0.9935	32.2
50000	32.4	50	1000	50	19.3	694.2	4585	4585052	0.9892	32.0
100000	32.4	50	1000	50	19.3	694.2	2293	4585052	0.9787	31.7
200000	32.4	50	1000	50	19.3	694.2	1146	4585052	0.9582	31.0
300000	32.4	50	1000	50	19.3	694.2	764	4585052	0.9386	30.4
500000	32.4	50	1000	50	19.3	694.2	459	4585052	0.9017	29.2
1000000	32.4	50	1000	50	19.3	694.2	229	4585052	0.8210	26.6
2000000	32.4	50	1000	50	19.3	694.2	115	4585052	0.6963	22.5
3000000	32.4	50	1000	50	19.3	694.2	76	4585052	0.6045	19.6
5000000	32.4	50	1000	50	19.3	694.2	46	4585052	0.4784	15.5
10000000	32.4	50	1000	50	19.3	694.2	23	4585052	0.3144	10.2
20000000	32.4	50	1000	50	19.3	694.2	11	4585052	0.1865	6.0
30000000	32.4	50	1000	50	19.3	694.2	8	4585052	0.1326	4.3
50000000	32.4	50	1000	50	19.3	694.2	5	4585052	0.0840	2.7

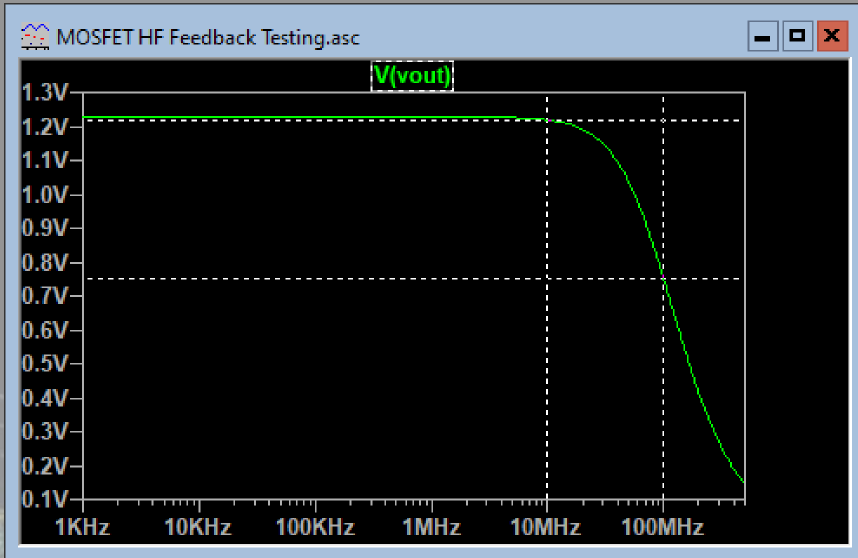




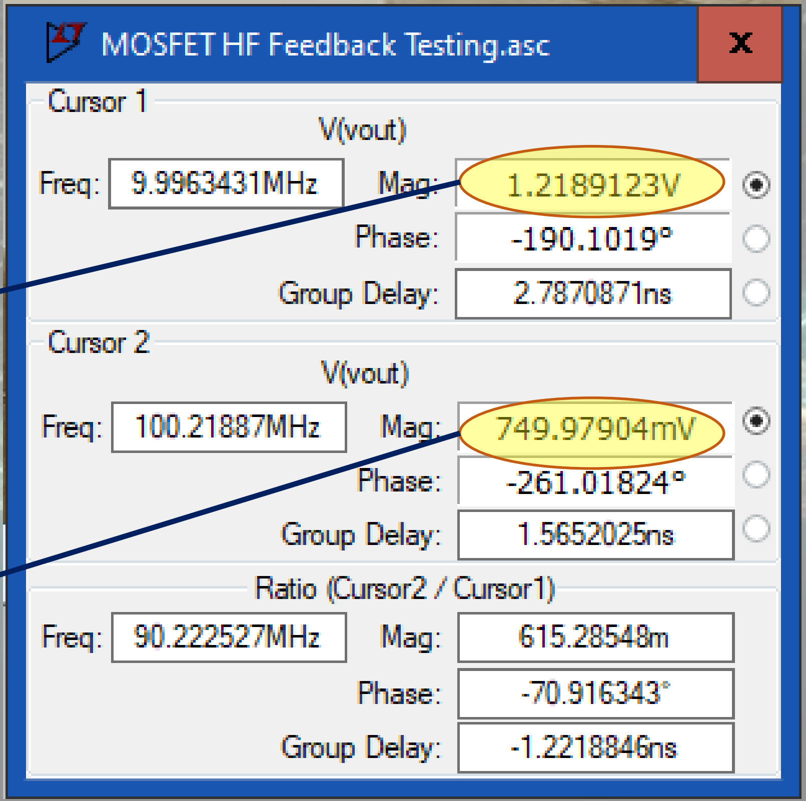
HIGH FREQUENCY ANALYSIS: 100R FB



Vg = Vs*Rb/(Ra+Rb)
Vout = Vg*A,
A' = A* Rb/(Ra+Rb)

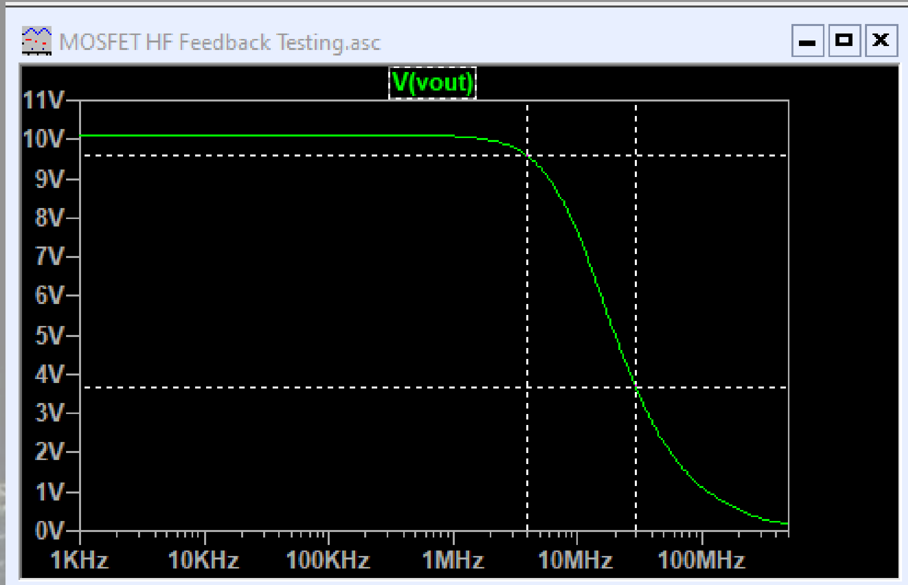


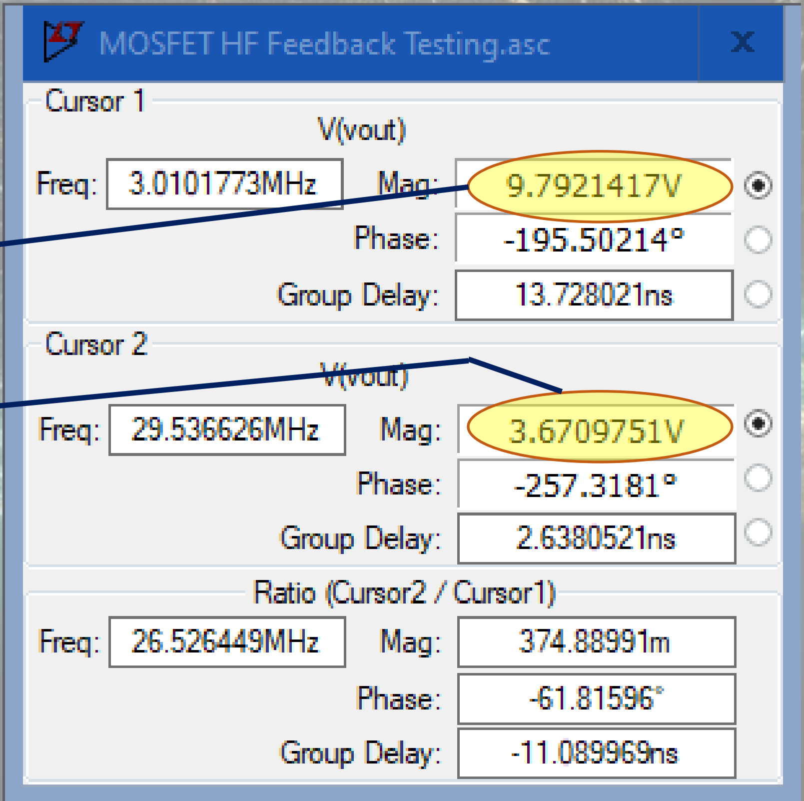
Frequency	Gain (FB)	Rs	Rb	Ri	Rf	Cgs	Cgd	Rm	Cm	-3dB Frequency	Xc	Real	Divider	Gain Out
1000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	1726022	23.8	1.00	1.19
10000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	172602	23.8	1.00	1.19
20000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	86301	23.8	1.00	1.19
30000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	57534	23.8	1.00	1.19
50000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	34520	23.8	1.00	1.19
100000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	17260	23.8	1.00	1.19
200000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	8630	23.8	1.00	1.18
300000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	5753	23.8	1.00	1.18
500000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	3452	23.8	0.99	1.18
1000000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	1726	23.8	0.99	1.17
2000000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	863	23.8	0.97	1.16
3000000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	575	23.8	0.96	1.14
5000000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	345	23.8	0.94	1.11
10000000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	173	23.8	0.88	1.04
20000000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	86	23.8	0.78	0.93
30000000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	58	23.8	0.71	0.84
50000000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	35	23.8	0.59	0.70
60000000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	29	23.8	0.55	0.65
70000000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	25	23.8	0.51	0.60
80000000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	22	23.8	0.48	0.56
90000000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	19	23.8	0.45	0.53
100000000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	17	23.8	0.42	0.50
200000000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	9	23.8	0.27	0.32
300000000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	6	23.8	0.19	0.23
500000000	1.19	50	10000	49.8	100	50	19.3	45.7	92.2	89701368	3	23.8	0.13	0.15



HIGH FREQUENCY ANALYSIS: 1000R FB

Frequency	Gain (FB)	Rs	Rb	Ri	Rf	Cgs	Cgd	Rm	Cm	-3dB Frequency	Xc	Real	Divider	Gain Out
1000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	601518	32.0	1.00	10.12
10000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	60152	32.0	1.00	10.11
20000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	30076	32.0	1.00	10.11
30000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	20051	32.0	1.00	10.10
50000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	12030	32.0	1.00	10.09
100000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	6015	32.0	0.99	10.06
200000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	3008	32.0	0.99	10.01
300000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	2005	32.0	0.98	9.96
500000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	1203	32.0	0.97	9.86
1000000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	602	32.0	0.95	9.61
2000000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	301	32.0	0.90	9.14
3000000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	201	32.0	0.86	8.72
5000000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	120	32.0	0.79	7.99
10000000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	60	32.0	0.65	6.60
20000000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	30	32.0	0.48	4.90
30000000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	20	32.0	0.38	3.90
50000000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	12	32.0	0.27	2.76
60000000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	10	32.0	0.24	2.41
70000000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	9	32.0	0.21	2.14
80000000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	8	32.0	0.19	1.92
90000000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	7	32.0	0.17	1.75
100000000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	6	32.0	0.16	1.60
200000000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	3	32.0	0.09	0.87
300000000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	2	32.0	0.06	0.60
500000000	10.1	50	10000	49.8	1000	50	19.3	89.9	264.6	19380065	1	32.0	0.04	0.37





Real World Comparison

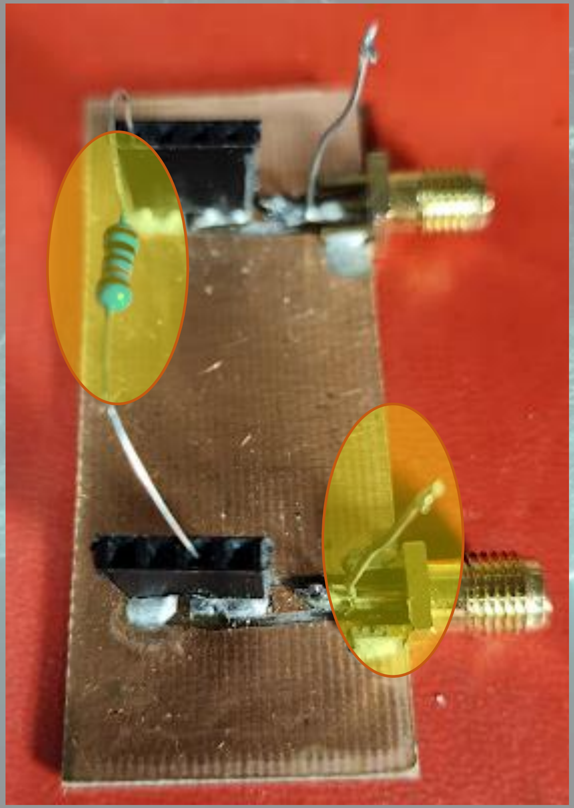
Approach

1. Build a test MOSFET Amplifier capable of “easily” changing key resistors (feedback and load)

2. Use scope to measure voltages (after used SA)

3. Calculate Rin, Rout, Gain and 3dB cutoff Frequencies

Real World Comparison: Test Setup



Real World Comparison: WTF!

- Used scope to measure input signal and output signal for each load and feedback resistor.
  - Need a scope to measure input/output impedance
- Method 1: Use the scope to measure output signal to identify -3dB frequencies
- Method 2: Use the SA to measure output signal (using resistor divider) to identify -3dB frequencies
- Observations:
  1. Scope and SA measurements differ significantly with -3 dB frequencies differing about 2X (e.g., 4.9 MHz vs 10.8 MHz)
  2. The SA could give accurate values for Mid Band baseline (i.e., max gain). Max gain was around 1.5 MHz and drop off below that
  3. Some Measurements vs calculations differ significantly. Operator? Equipment?

Update: How Stupid can I be?

The **half-power point** is the point at which the output power has dropped to half of its peak value, that is, at a level of approximately -3 dB.[1][a]

Amplifiers and filters [edit]

This occurs when the output voltage has dropped to $1/\sqrt{2}$ (~0.707) of the maximum output voltage[b] and the power has dropped by half.[a] A bandpass amplifier will have two half-power points, while a low-pass amplifier or a high-pass amplifier will have only one.

I only realized this today!!!

General Outcome

How to make RF measurements?

Real World Comparison: Data Collection

Gain | 3dB Frequency | Rin | Rout

	Rf	Rl	Cgs	Cgd	Rb	Rs	Rd	Ro	LTSpice Gm	ro @ Id 10.3mA	Vds @ Id 10.3mA	Open Loop Gain	Calculated Feedback Gain	LTSpice Gain @ 10KHz	Measured Gain @ 10KHz	Cin-Miller	Cout-Miller	Cin	Cout	Rfin-Miller	Rfout-Miller	Rin	Rout	Calculated -3dB Freq [MHz]	Fo	Measured -3dB Freq [MHz]	LTSpice -3dB Freq [MHz]	Calculated Zin	LTSpice Zin [10 KHz]	Measured Zin [10KHz]	Calculated Zout [Rs=0]	LTSpice Zout [Rs=0]	Calculated Zout [Rs=50]	LTSpice Zout [Rs=50]	Measured Zout [10KHz]
BS170		10000	19.9	6.1	10000	50	500	476.2	0.088295	605	11.0	42.0	42.0	20.2	31.0	262.4	6.2	282.3	6.2	0.0	0.0	49.8	476.2	11.9	59.5	4.5	12.7	10000	9970	2046	476	476	476	476	391
		1000	19.9	6.1	10000	50	500	333.3	0.088295	605	11.0	29.4	29.4	19.7	29.5	185.5	6.3	205.4	6.3	0.0	0.0	49.8	333.3	15.6	75.7	6.6	18.1	10000	9929	2046	333	333	333	333	545
		200	19.9	6.1	10000	50	500	142.9	0.088295	605	11.0	12.6	12.6	8.4	9.9	83.0	6.6	102.9	6.6	0.0	0.0	49.8	142.9	31.1	169.2	19.0	42.1	10000	9859	2055	143	143	143	143	516
	2200	10000	20	5.12	10000	50	500	476.2	0.088295	605	11.0	42.0	34.4	29.0	29.4	220.2	5.2	240.2	5.2	51.1	2140.9	25.9	383.0	25.4	77.9	7.7	15.4	69	91	89	391	391	290	260	429
	2200	1000	20	5.12	10000	50	500	333.3	0.088295	605	11.0	29.4	25.4	17.0	18.1	155.7	5.3	189.7	5.3	72.9	2450.0	29.5	293.4	29.4	102.5	10.4	20.0	85	121	100	289	289	196	210	287
	2200	200	20	5.12	10000	50	500	142.9	0.088295	605	11.0	12.6	11.0	7.9	8.0	69.7	5.5	97.7	5.5	161.7	2470.7	38.0	134.0	42.0	214.9	18.4	44.0	182	242	200	134	134	110	114	260
	1000	10000	20	5.12	10000	50	500	476.2	0.088295	605	11.0	42.0	20.1	18.0	18.5	220.2	5.2	240.2	5.2	29.2	976.0	15.0	320.1	40.5	94.0	12.5	18.7	35	50	47	329	329	249	174	179
	1000	1000	20	5.12	10000	50	500	333.3	0.088295	605	11.0	29.4	21.0	14.5	14.2	155.7	5.3	189.7	5.3	32.9	1209.5	19.0	264.9	49.0	119.5	14.6	24.1	45	64	59	250	250	170	140	175
	1000	200	20	5.12	10000	50	500	142.9	0.088295	605	11.0	12.6	10.9	7.9	7.1	69.7	5.5	97.7	5.5	79.5	1050.9	29.7	125.9	54.9	220.0	14.6	40.0	90	119	104	125	125	104	99	177
	200	10000	20	5.12	10000	50	500	476.2	0.088295	605	11.0	42.0	11.7	7.6	7.9	220.2	5.2	240.2	5.2	4.6	195.4	4.9	190.5	150.0	249.2	>120	42.7	16	29	21	141	141	129	56	115
	200	1000	20	5.12	10000	50	500	333.3	0.088295	605	11.0	29.4	10.4	6.0	6.4	155.7	5.3	189.7	5.3	6.6	515.0	5.0	282.5	149.1	140.5	>120	40.1	18	26	29	125	125	116	59	69
	200	200	20	5.12	10000	50	500	142.9	0.088295	605	11.0	12.6	6.9	4.5	4.4	69.7	5.5	97.7	5.5	14.7	917.7	11.9	90.5	149.6	292.9	>120	72.0	27	96	90	89	89	79	44	59

	Rf	Rl	Cgs	Cgd	Rb	Rs	Rd	Ro	Tracer Gm	ro @ Id 13mA	Vds @ Id 13mA	Open Loop Gain	Calculated Feedback Gain	LTSpice Gain @ 10KHz	Measured Gain @ 10KHz	Cin-Miller	Cout-Miller	Cin	Cout	Rfin-Miller	Rfout-Miller	Rin	Rout	Calculated -3dB Freq [MHz]	Fo	Measured -3dB Freq [MHz]	LTSpice -3dB Freq [MHz]	Calculated Zin	LTSpice Zin [10 KHz]	Measured Zin [10KHz]	Calculated Zout [Rs=0]	LTSpice Zout [Rs=0]	Calculated Zout [Rs=50]	LTSpice Zout [Rs=50]	Measured Zout [10KHz]
2N7000		10000	50	19.3	10000	50	500	476.2	0.0588	929	11.5	28.0	28.0	20.2	36.0	559.9	20.0	609.9	20.0	0.0	0.0	49.8	476.2	5.2	16.7	4.5	7.0	10000	9254	2149	514	476	514	476	449
		1000	50	19.3	10000	50	500	333.3	0.0588	929	11.5	19.6	19.6	19.7	25.1	397.7	20.3	447.7	20.3	0.0	0.0	49.8	333.3	7.1	29.5	6.9	11.2	10000	9500	2111	245	333	245	333	491
		200	50	19.3	10000	50	500	142.9	0.0588	929	11.5	8.4	8.4	8.4	10.0	181.5	21.6	231.5	21.6	0.0	0.0	49.8	142.9	19.0	51.6	19.2	26.0	10000	9006	1942	124	143	124	143	404
	2200	10000	50	19.3	10000	50	500	476.2	0.0588	929	11.5	28.0	22.0	23.0	23.5	559.9	20.0	609.9	20.0	75.0	2124.2	30.0	383.0	8.7	20.5	8.9	9.5	95	85	69	391	391	276	254	250
	2200	1000	50	19.3	10000	50	500	333.3	0.0588	929	11.5	19.6	16.9	17.0	17.0	397.7	20.3	447.7	20.3	106.0	2410.4	39.9	292.0	10.5	26.0	10.6	12.9	120	119	92	289	289	221	206	242
	2200	200	50	19.3	10000	50	500	142.9	0.0588	929	11.5	8.4	7.0	7.9	9.9	181.5	21.6	231.5	21.6	294.0	2899.7	41.0	139.7	16.0	55.1	10.0	27.7	274	220	176	134	134	117	119	296
	1000	10000	50	19.3	10000	50	500	476.2	0.0588	929	11.5	28.0	18.7	18.0	29.6	559.9	20.0	609.9	20.0	34.5	965.5	20.4	310.9	12.0	25.0	14.6	11.6	52	47	99	329	329	242	165	300
	1000	1000	50	19.3	10000	50	500	333.3	0.0588	929	11.5	19.6	14.5	14.5	10.4	397.7	20.3	447.7	20.3	40.5	1260.6	24.6	264.0	14.5	29.7	16.5	14.9	60	60	49	250	250	199	144	160
	1000	200	50	19.3	10000	50	500	142.9	0.0588	929	11.5	8.4	7.2	7.9	9.2	181.5	21.6	231.5	21.6	106.9	1021.9	39.9	125.9	20.9	50.0	29.0	29.7	194	119	99	125	125	111	91	156
	200	10000	50	19.3	10000	50	500	476.2	0.0588	929	11.5	28.0	7.6	7.6	8.0	559.9	20.0	609.9	20.0	6.9	199.1	6.1	197.4	49.1	50.0	102.0	26.4	24	22	17	141	141	139	59	82
	200	1000	50	19.3	10000	50	500	333.3	0.0588	929	11.5	19.6	6.7	6.0	8.9	397.7	20.3	447.7	20.3	9.7	587.5	8.1	201.2	49.0	99.0	109.0	29.0	27	24	21	125	125	124	51	40
	200	200	50	19.3	10000	50	500	142.9	0.0588	929	11.5	8.4	4.5	4.5	5.5	181.5	21.6	231.5	21.6	21.9	986.4	14.9	97.4	46.1	75.6	104.4	44.7	41	54	20	89	89	89	42	47

BS170 Would Not Behave

- Transistors were from China
- Parameters may be well off from LTSpice model/Datasheet
- I started to dust off my Transistor Tracer

LTSPICE MODELS: Bitten Yet Again

```
.model BS170 VDMOS VTO=1.824 RG=270 RS=1.572 RD=1.436 RB=.768 KP=.1233
Cgdmax=20p Cgdmin=3p CGS=28p Cjo=35p Rds=1.2E8 IS=5p Bv=60 Ibv=10u Tt=161.6n
```

Ciss	24	40
Coss	17	30
Crss	7	10
Cgd	7	10
Cgs	17	30
Cds	10	20

ON CHARACTERISTICS (Note 1)

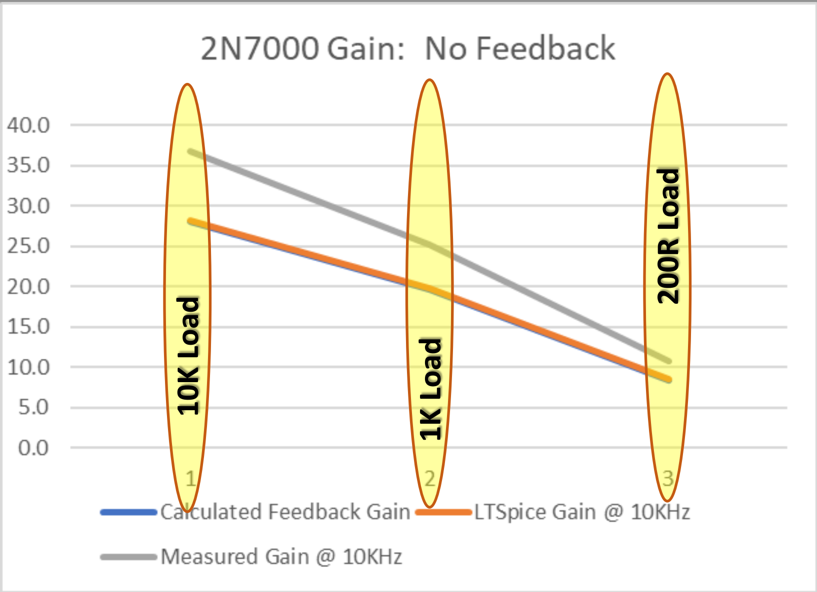
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 1$ mA	All	0.8	2.1	3	V
$R_{DS(ON)}$	Static Drain–Source On–Resistance	$V_{GS} = 10$ V, $I_D = 200$ mA	All	–	1.2	5	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10$ V, $I_D = 200$ mA	BS170	–	320	–	mS
		$V_{DS} \geq 2\ V_{DS(on)}$, $I_D = 200$ mA	MMBF170	–	320	–	

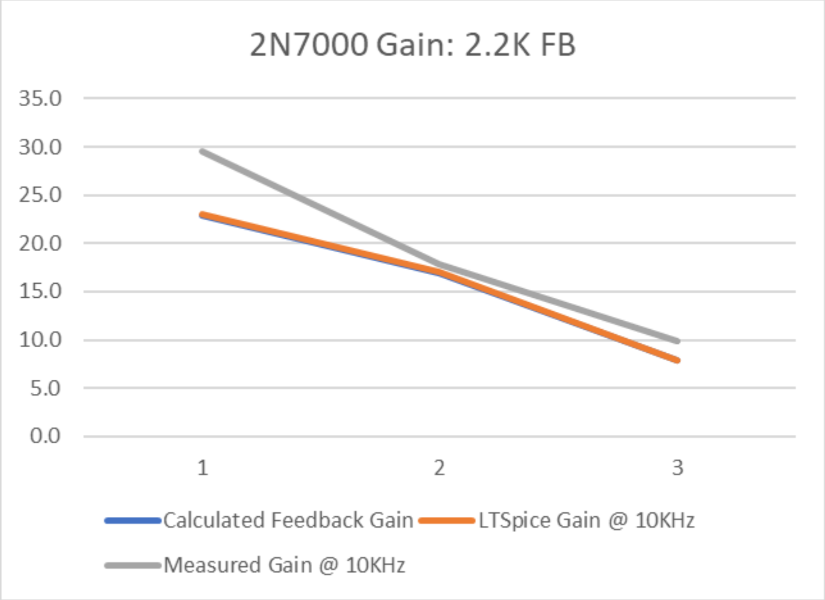
DYNAMIC CHARACTERISTICS

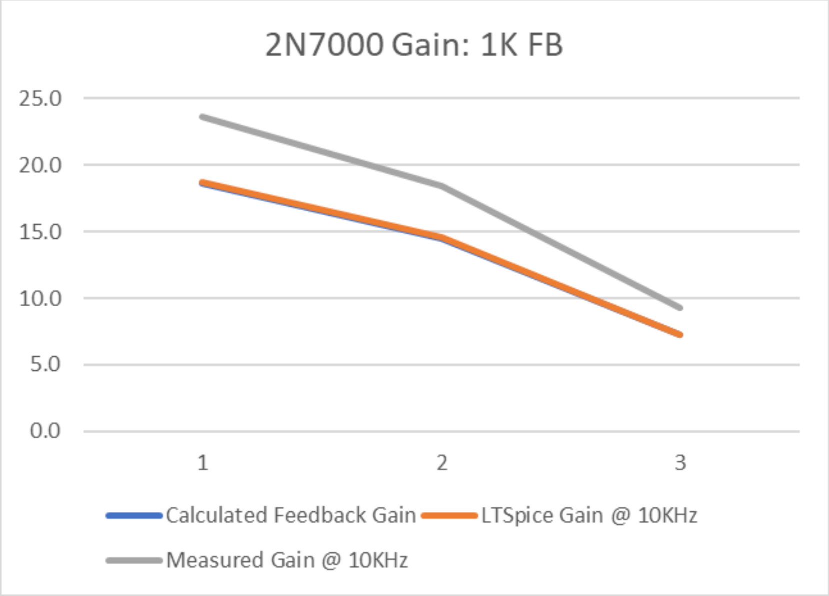
C_{iss}	Input Capacitance	$V_{DS} = 10$ V, $V_{GS} = 0$ V, f = 1.0 MHz	All	–	24	40	pF
C_{oss}	Output Capacitance		All	–	17	30	pF
C_{rss}	Reverse Transfer Capacitance		All	–	7	10	pF

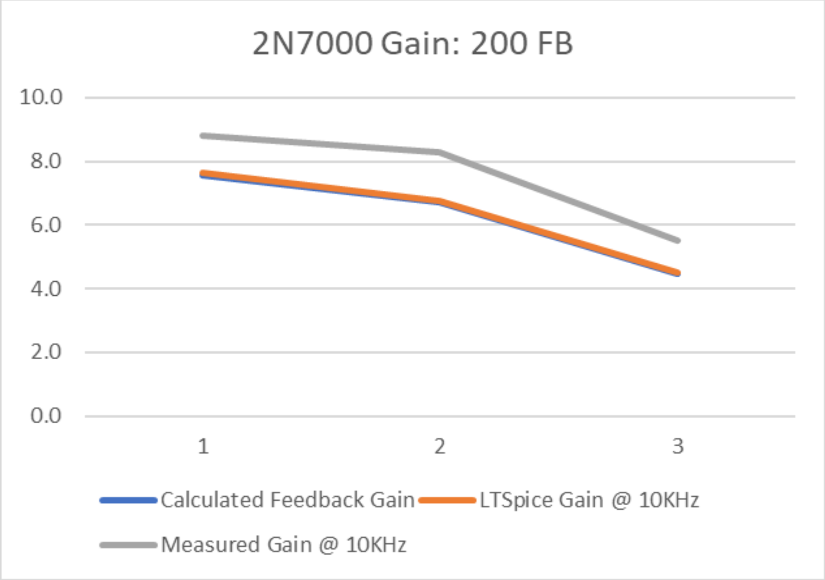
Furthermore, Transistor Tracer measurements are VERY different

Real World Comparison: Findings

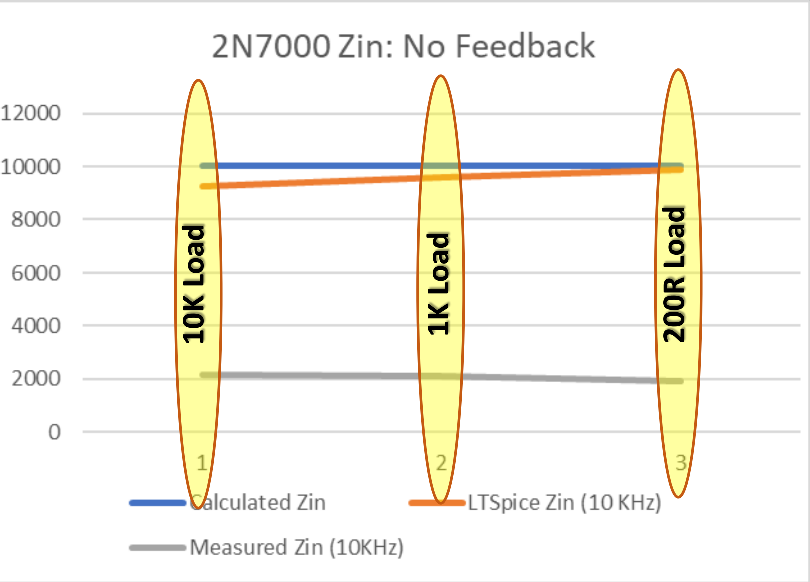


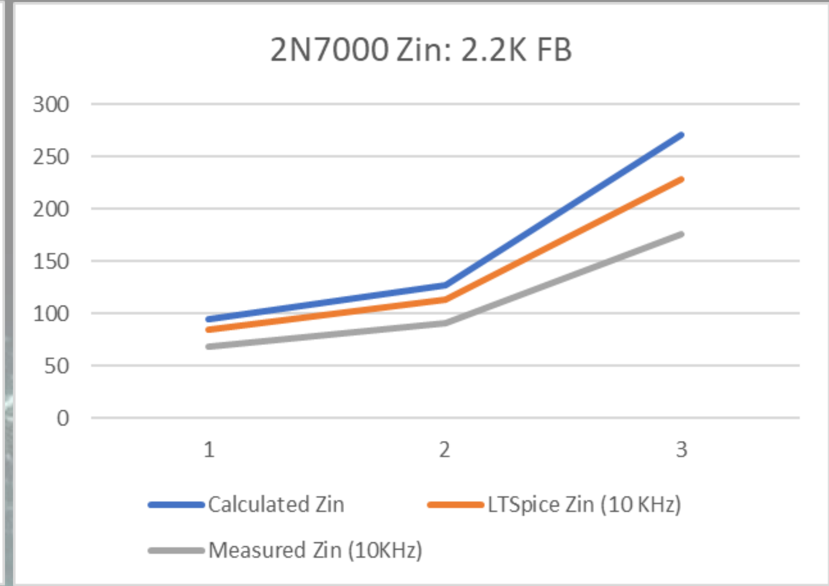


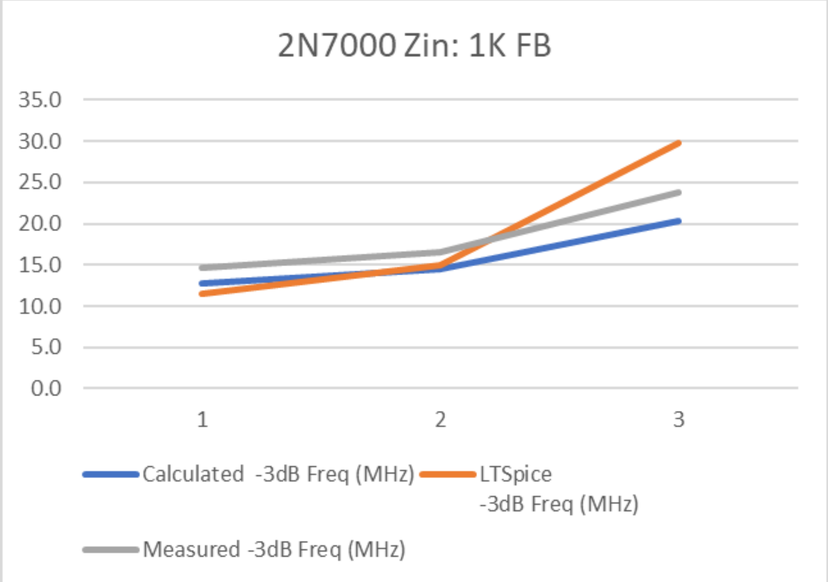


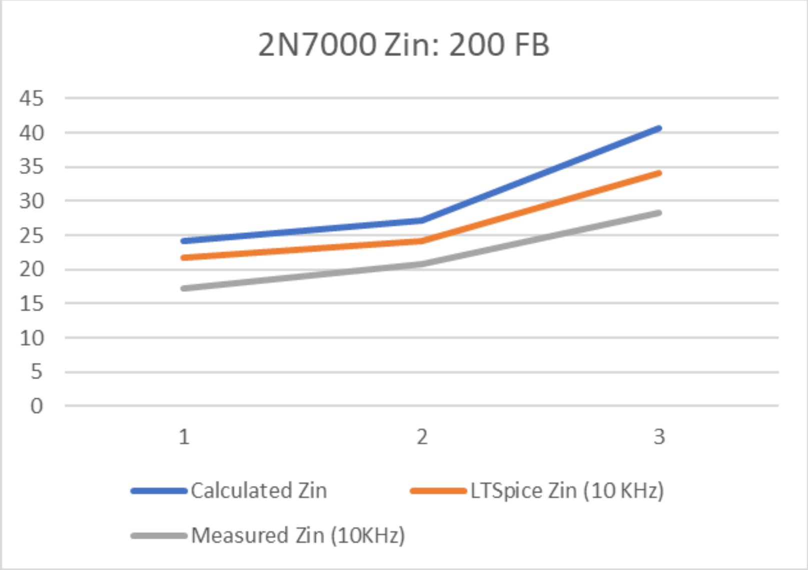


Real World Comparison: Findings

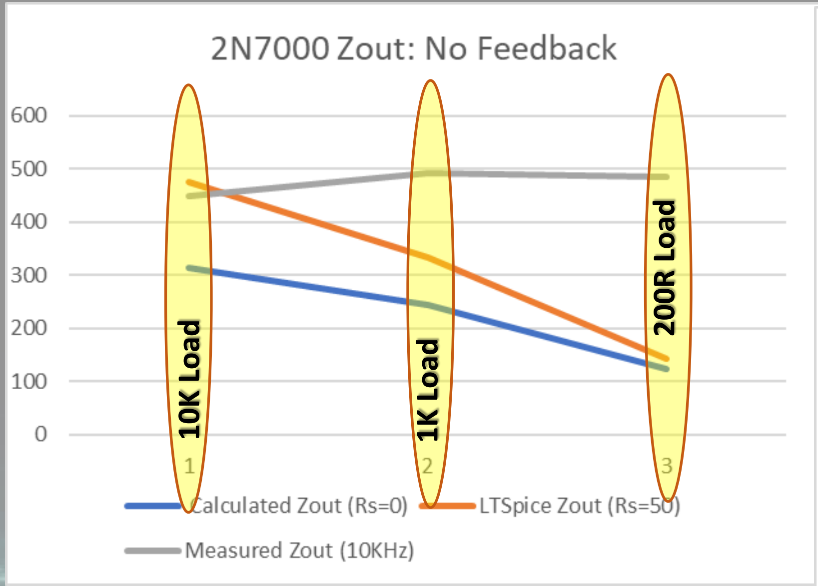


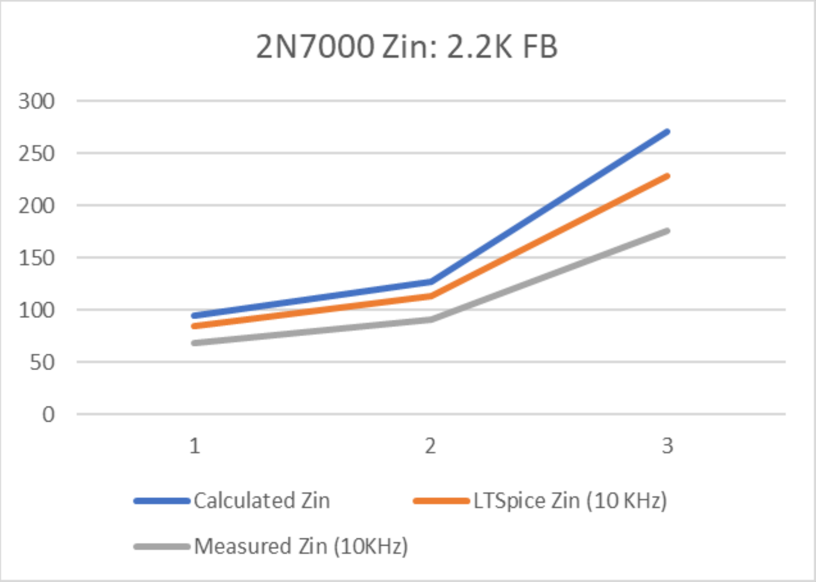


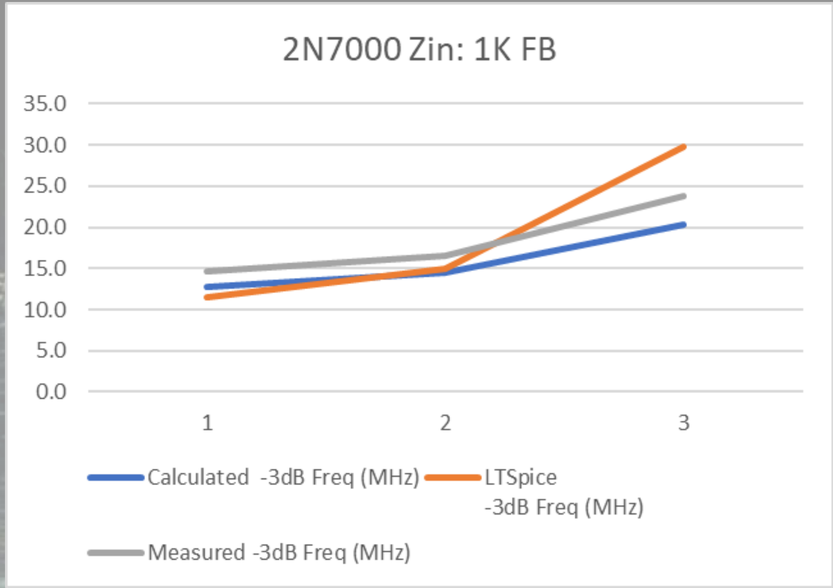


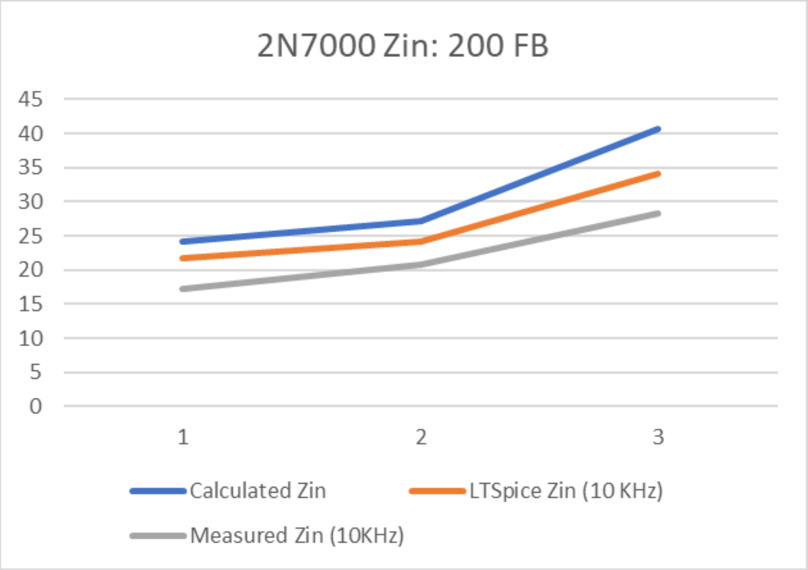


Real World Comparison: Findings

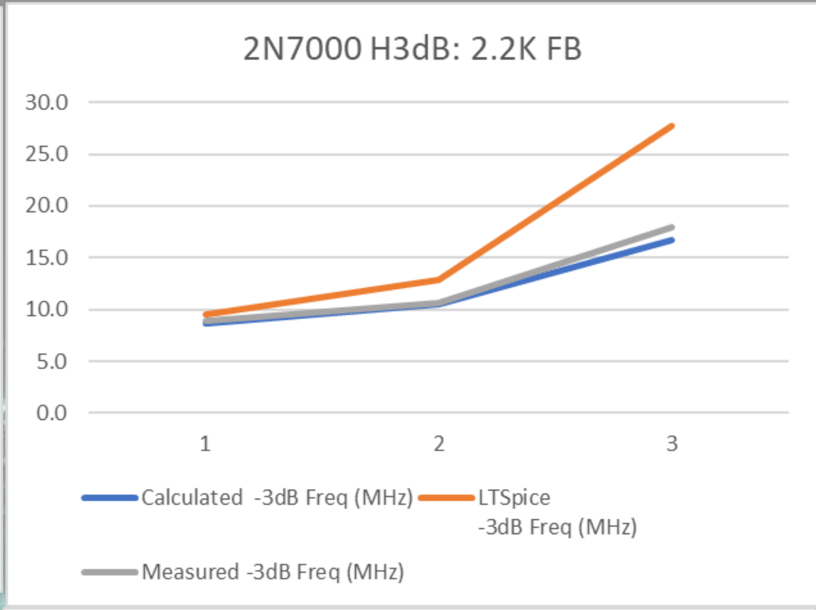


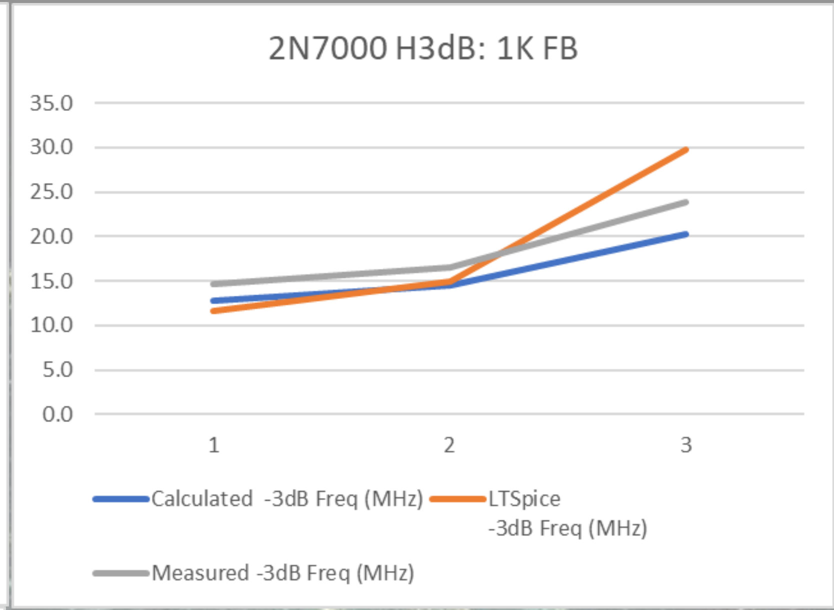


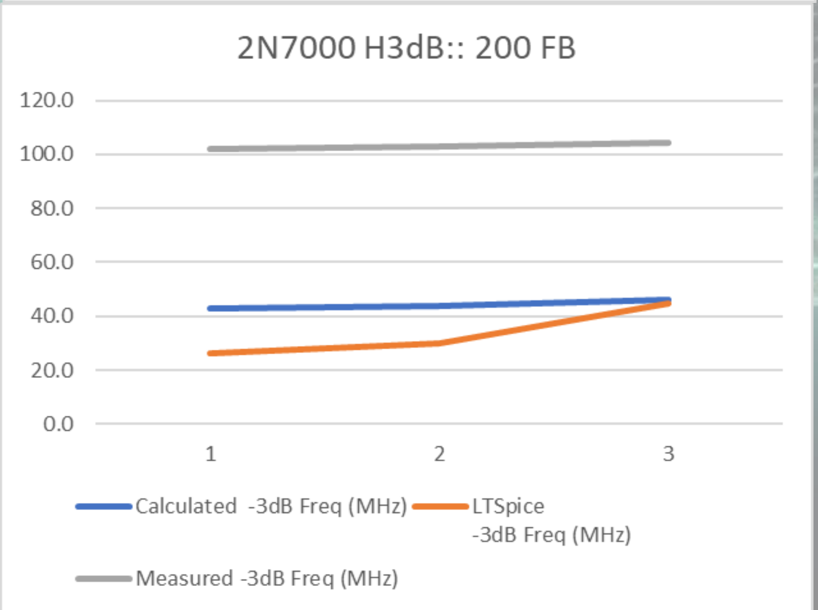




Real World Comparison: Findings





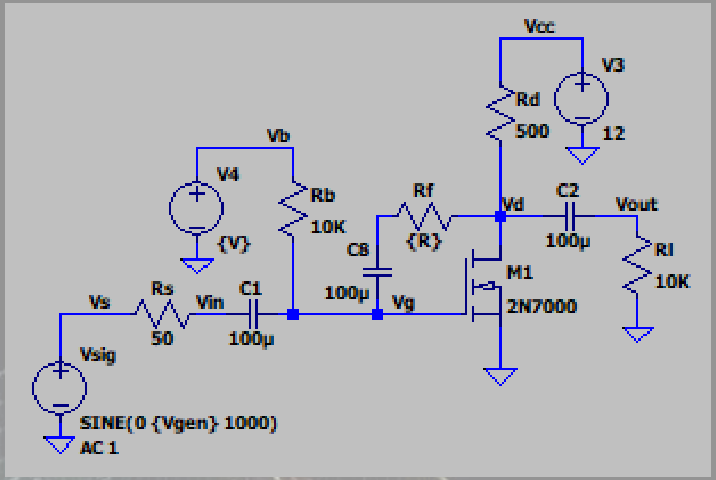


Half Power vs Voltage

General Outcome

How to make RF measurements?

EQUATION SUMMARY



Low Frequency (well below -3dB Frequency)

- Gain:
  - ✓ $A_V = (1/R_F - G_m) R_F // R_D // R_L$
- Input Impedance:
  - ✓ $Z_{in} = (R_F + R_O) / (1 + G_m R_O)$ (for R_B large)
  - ✓ $Z_{in} = R_B (R_F + R_O) / (R_F + R_O + G_m R_O R_B)$
    - For $R_O = R_D // R_L$
- Output Impedance:
  - ✓ $Z_{out} = R_F // R_D // R_L$

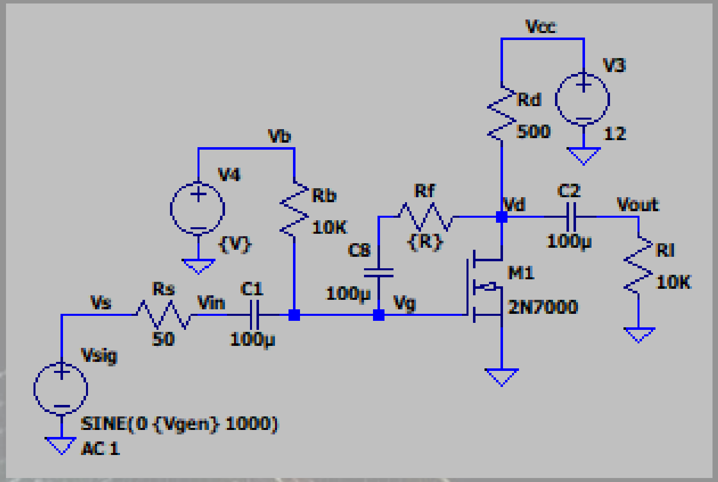
Notes:

Provided:

- ✓ Gain (without feedback) = $-G_m R_O$
- ✓ Z_{out} (without feedback) = R_O
- ✓ Z_{in} (without feedback) = R_B

1. Can solved For R_F for desired Gain (with feedback), G_m, R_D and R_L.

EQUATION SUMMARY

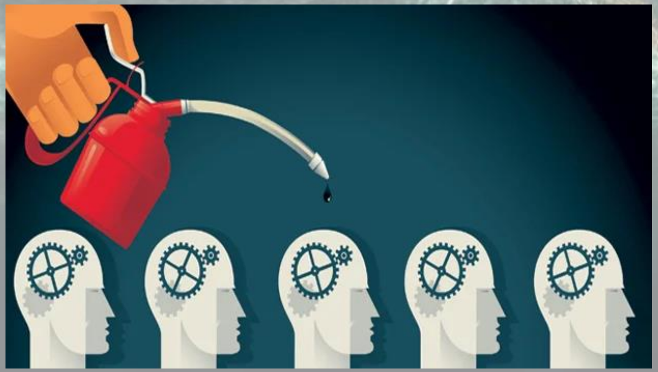


High Frequency (close to or beyond) -3dB Frequency)

- -3dB Cutoff Frequency
  - ✓ $F(-3dB) = 1/(2 * \pi * R_{eq} * C_{eq})$
    - For $C_{eq\,(input)} = C_{gd}(1+A) + C_{gs}$
    - For $C_{eq\,(output)} = C_{gd}(1+A)/A$
    - For $R_{eq\,(input)} = R_F/(1+A) \,//\, R_B \,//\, R_S$
    - For $R_{eq\,(output)} = R_F A/(1+A) \,//\, R_D \,//\, R_L$
- Gain at Frequency F:
  - ✓ $A_{V(F)} = A_V * X_M / (X_m + R_i)$
    - For $R_i = R_S \,//\, R_B \,//\, R_m$
    - $R_M = R_F/(1+A_V)$
    - $X_M = 1/(2 * \pi * F * C_{eq})$
    - For $C_{eq} = C_{gs} + C_{gd} * (1+A_V)$

Notes:

1. 3dB Frequencies are an approximation – it's a ballpark value.
2. Measurement vs Calculation???



SUMMARY:
RF FEEDBACK AMPLIFIERS ARE COMPLEX

✓$F(-3dB) = 1/(2 * \pi * R_{eq} * C_{eq})$

For $C_{eq\ (input)} = C_{gd}(1+A) + C_{gs}$

For $C_{eq\ (output)} = C_{gd}(1+A)/A$

For $R_{eq\ (input)} = R_F/(1+A) // R_B // R_S$

For $R_{eq\ (output)} = R_F A/(1+A) // R_D // R_L$

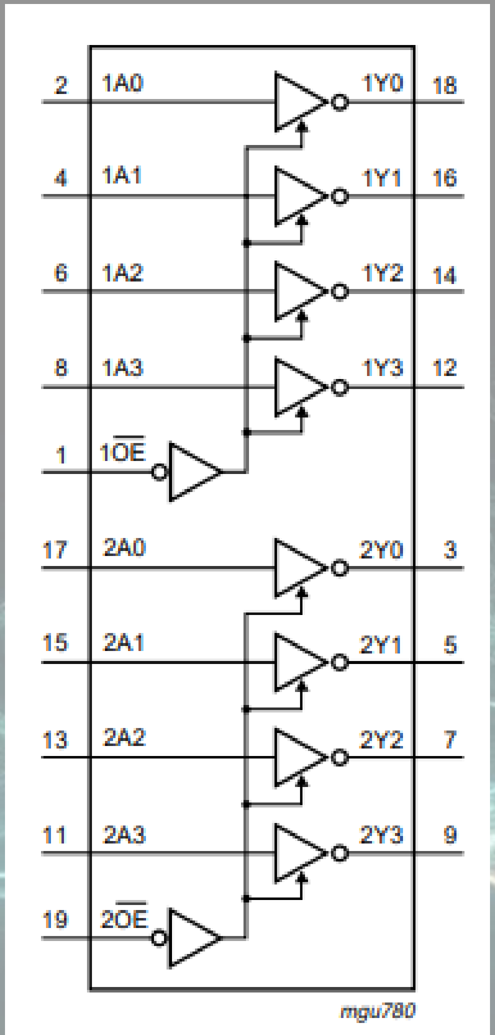
HINTS and TIPS

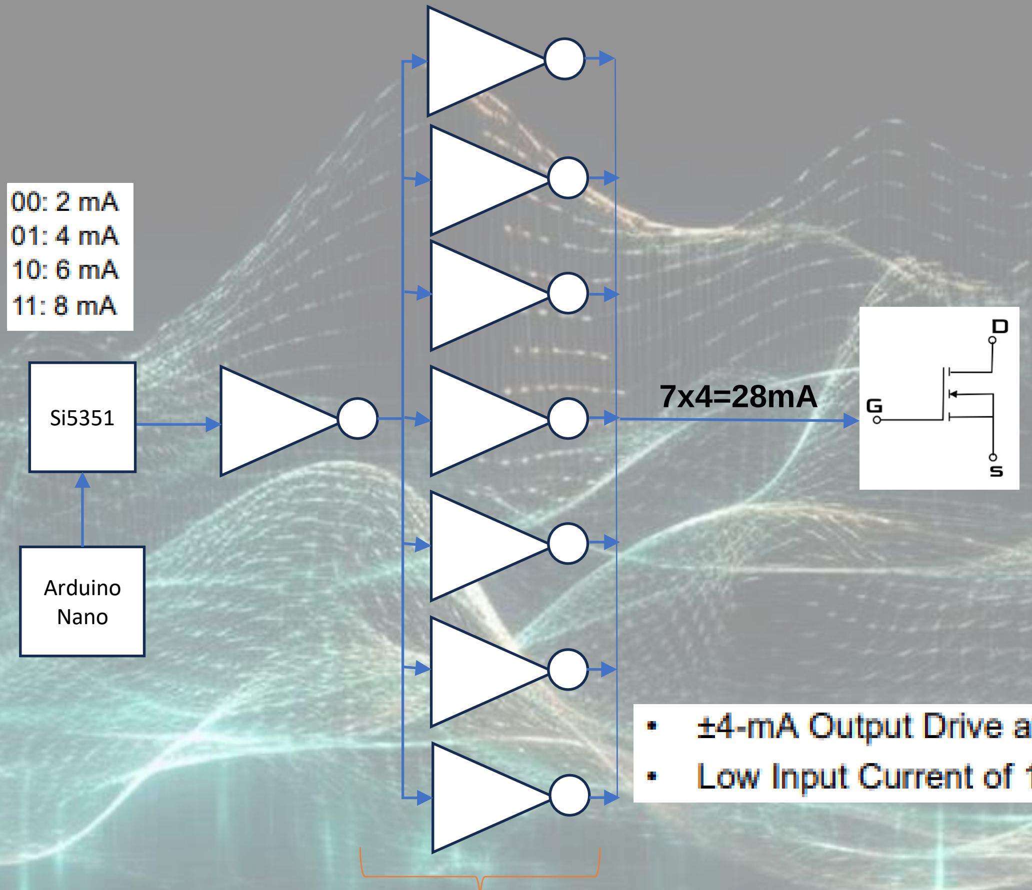
1. Use lower gain. Multiple stages?
2. Keep input/source resistance as low as possible (more current).
3. Keep output resistance R_D and R_L as low as possible
4. Use large feedback resistors with smaller resistors for R_S R_D and R_L

Good things happen when you understand…

Dave VE3OOI (Before he went insane doing math)

MILLER EFFECT: INCREASE CURRENT





Buffer driver in parallel for greater current output. Used for TTL Transmitters

Captain, we need more current…

- ±4-mA Output Drive at 5 V
- Low Input Current of 1 μA Maximum

74HC240; 74HCT240

Octal buffer/line driver; 3-state; inverting

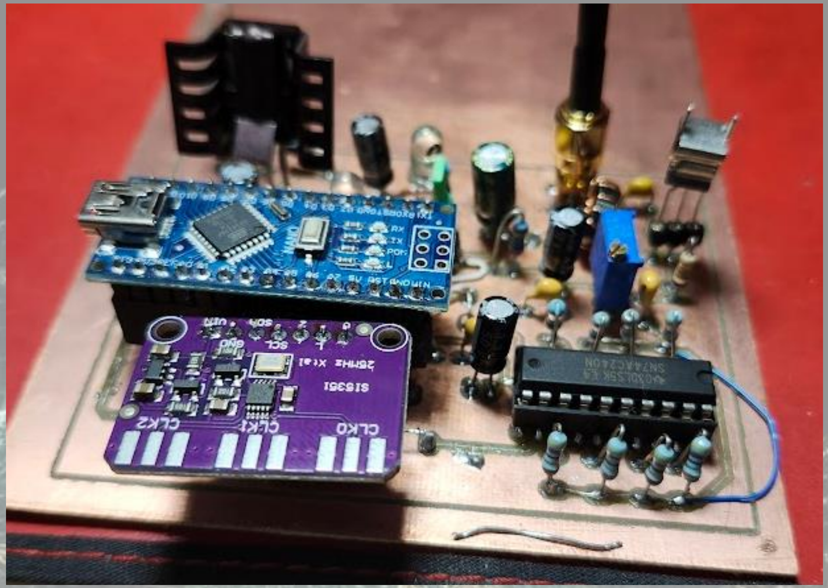
Octal: 8
Hex: 6

The **74HC** family has High-speed CMOS circuitry, combining the speed of TTL with the very low power consumption of the

The Si5351A/B/C features various output current drives ranging from 2 to 8 mA (default). It is recommended to configure the trace characteristics as shown in Figure 18 when an output drive setting of 8 mA is used.

MILLER EFFECT: INCREASE CURRENT

Si5351 driving BS170 MOSFET



Si5351 & 74HC140 driving BS170 MOSFET

Without 74HC240 Drivers				
Frequency (MHz)	Output (dBm)	Output (Watts)	Highest Harmonic (dBm)	Harmonic Attenuation
7	30.6	1.1	-21	-51.6
14	29.4	0.87	-21	-50.4
20	26.9	0.49	-24	-50.9
30	26.6	0.45	-24	-50.6

~8mA drive into 50R load

At least 3x
Current increase

Getting over 1W across HF band with more current from 74HC240 driver

With 74HC240 Drivers				
Frequency (MHz)	Output (dBm)	Output (Watts)	Highest Harmonic (dBm)	Harmonic Attenuation
7	32.8	1.9	-20	-52.8
14	31.8	1.5	-20	-51.8
20	31.2	1.3	-21	-52.2
30	30.5	1.1	-21	-51.5

~28mA drive into ?? load


That's all Folks!