I confirm that I will keep the content of this assignment confidential. I confirm that I have not received any unauthorized assistance in preparing for or writing this assignment. I acknowledge that a mark of 0 may be assigned for copied work. – Deni Rakovic 110081508

a) =
$$(1 \cdot 2^{7}) + (1 \cdot 2^{6}) + (1 \cdot 2^{5}) + (1 \cdot 2^{4}) + (1 \cdot 2^{3})$$

$$= 128 + 64 + 32 + 16 + 8$$

$$= (248)_{10}$$

M.

$$= (1 \cdot 2^{3}) + (1 \cdot 2^{6}) + (0) + (0) + (1 \cdot 2^{3}) + (0) + (1 \cdot 2^{3})$$

$$= 128 + 64 + 8 + 2 = (202)_{10}$$

$$a) = (0 \cdot 16^{7}) + (1 \cdot 16^{6}) + (2 \cdot 16^{5}) + (6 \cdot 16^{4}) + (15 \cdot 16^{3}) + (9 \cdot 16^{2}) + (16^{13} \cdot 16^{1}) + (4 \cdot 16^{6}) + (16^{13} \cdot 16^{1}) + ($$

$$= (6 \cdot 16^{7}) + (10 \cdot 16^{6}) + (12 \cdot 16^{5}) + (13 \cdot 16^{4}) + (15 \cdot 16^{3}) + (10 \cdot 16^{2}) + (9 \cdot 16^{1}) + (5 \cdot 16^{6})$$

- = 1610612736 + 167772160 + 12582912+ 851968 + 61440 + 2560 + 144 + 5= (1791883925)10
- 3. Number of inputs for a truth table with 3 variables x, y, Z = 23 = 8 inputs

4.

a)
$$(-72)_{10} = (1011 1000)_2$$

Hilroy

5. Assembly language is not fortable because it has a one to one relationship with machine language that corresponds to to a secific processor family. So because AL is secific to the aschitecture it is designed for, a program in AL for XBG won't run on ARM processors as an example.

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a)

Hilron

6.

- A) The carry flag is used for keeping track of the carry-out and borrow-in operations of arithmetic, while the sign flag is used to indicate the sign of a result. For addition a copy of the carry out of the MSB will be placed in the carry flag. In subtraction, if a larger unsigned integer is subtracted from a smaller one, the carry out bit will be placed in the carry flag. In the context of the sign flag, when the result of a signed arithmetic operation is negative the sign flag will be 1.
- **B**) The flat segment model consists of a single global descriptor table while the multi segment model has a local descriptor table for each process, hence the name. In the flat model, all segments are mapped to the entire 32-bit address space. The multi segment model holds a descriptor for each segment within the local descriptor table.
- **C**) The data bus transfers data and instructions between the CPU and memory while the control bus synchronizes the actions of all devices attached to the system. The control bus ensures communication is smooth between devices and not interfering with one another like a policeman on a highway. The address bus holds addresses of data and instructions when the instruction currently being executed transfers data between CPU and memory.
- **D)** While both addresses are used to identify a specific location in memory, a logical address is generated by the CPU while a program is running that corresponds to a physical address. A physical address corresponds to an actual physical location in memory. The user never directly deals with the physical address but can access it via the corresponding logical address.