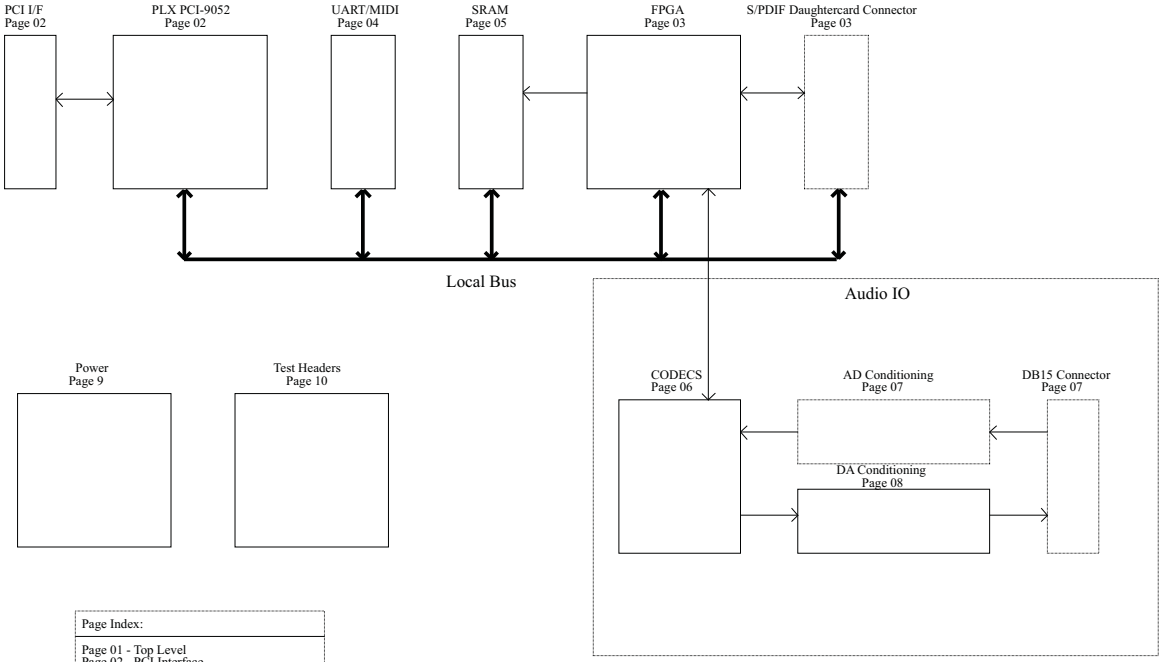
Wave/496-000

October 13, 1999



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PCI Interface

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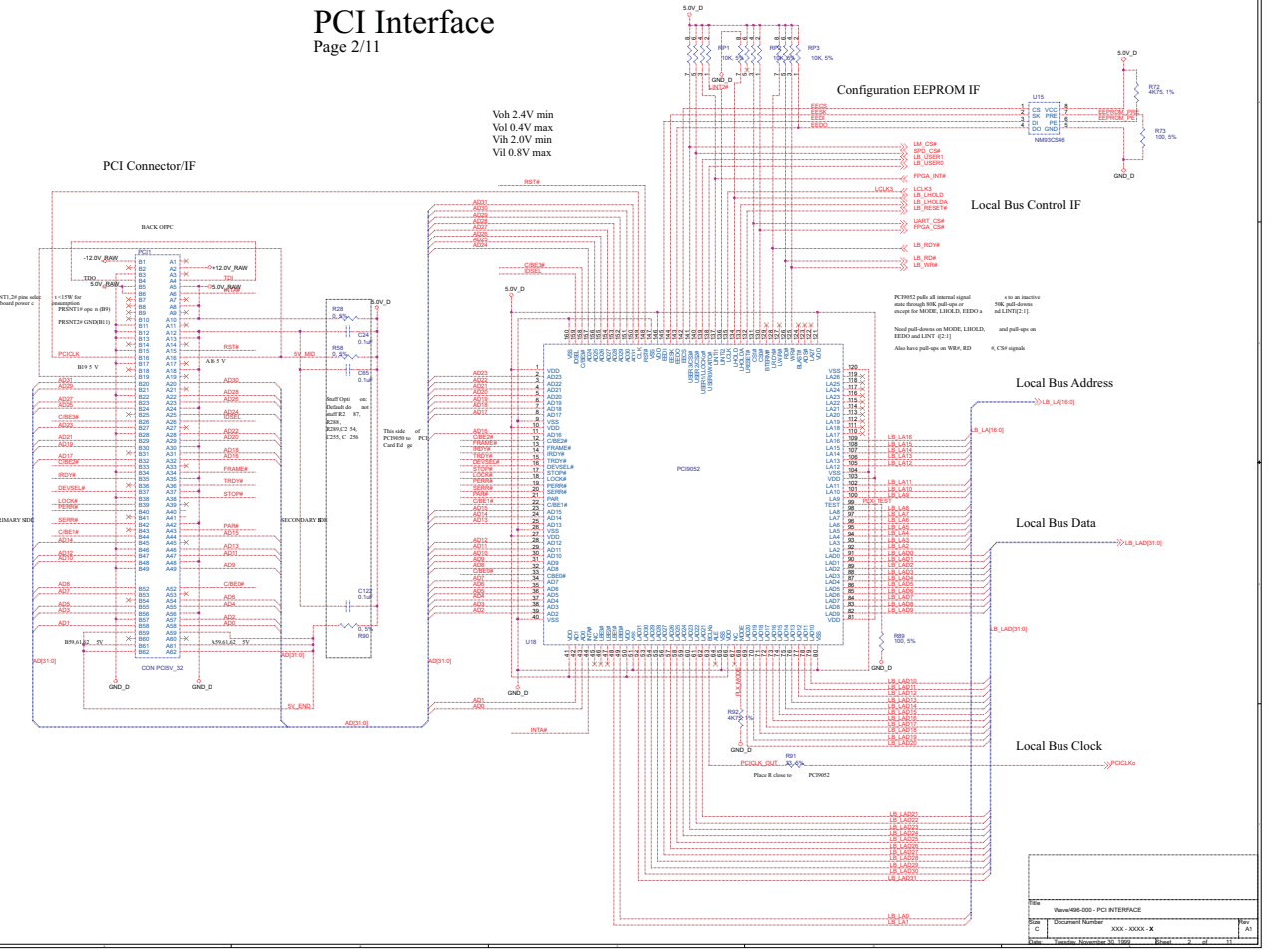

FPGA/Control ol

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VCCINT = 3.3V (6016A)

VCCIO = 3.3V

Vih 1.75 min, 3.3V max
Vil 0.8V max, 0.0V min
Voh3.0V TTL min, 3.3V cmos min
Vol 0.05V TTL max, 0.2V cmos max

Local Bus Address

Local Bus Misc

Local Bus Data

S/PDIF DIO Daughtercard Connector

DIO Configuration IF

FPGA Configuration IF

SRAM IF

CODEC Serial Control IF

CODEC Digital IF

Test Signals

Multi-board Sync

Clock In

Clock Out

Programmable Crystal Oscillator for 32-96 kHz Sample RatesRates

Local BusBus Controlol IF

DIO Control IF

Analog Gain and Monitor Control

Clock Buffer

Caps and Series R's go near source

MIDI/UART

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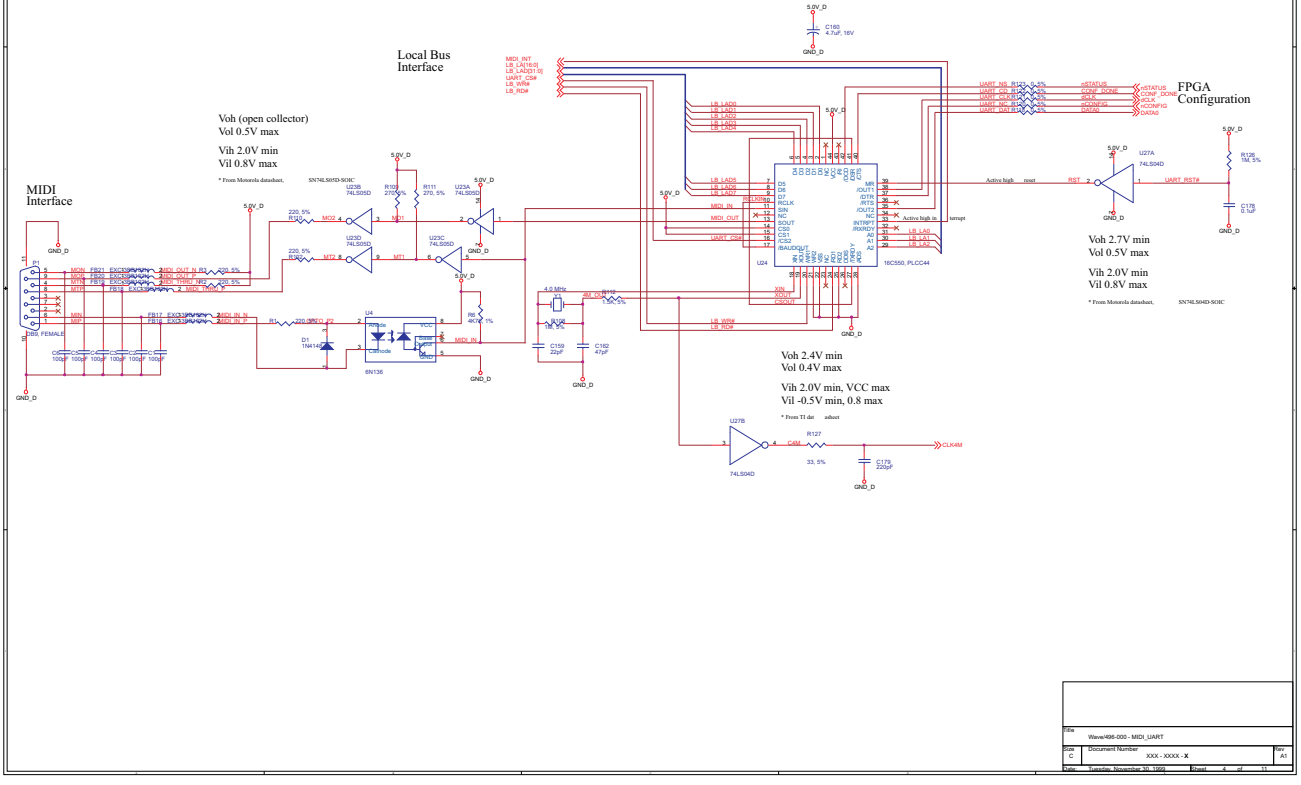

SRAM/Local Memory

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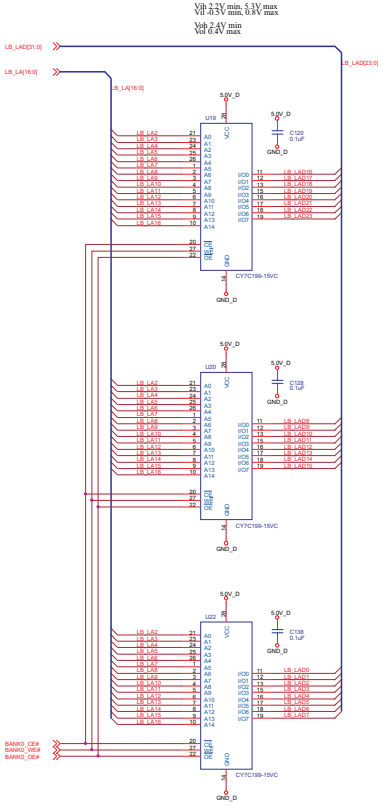
Local Bus Address and Data



Local Bus Control

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CODECs

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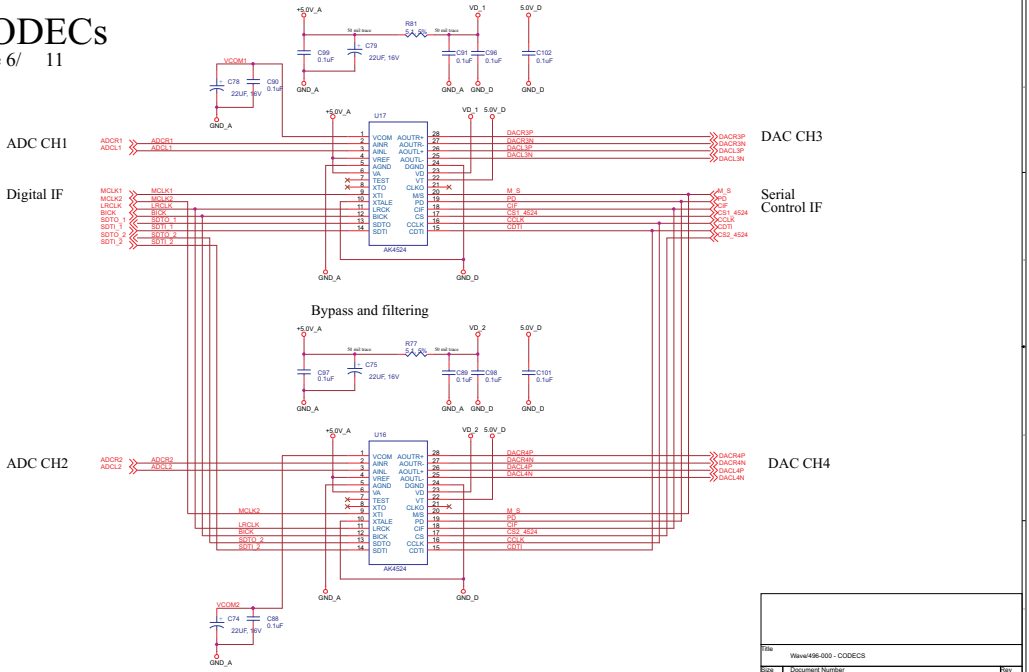

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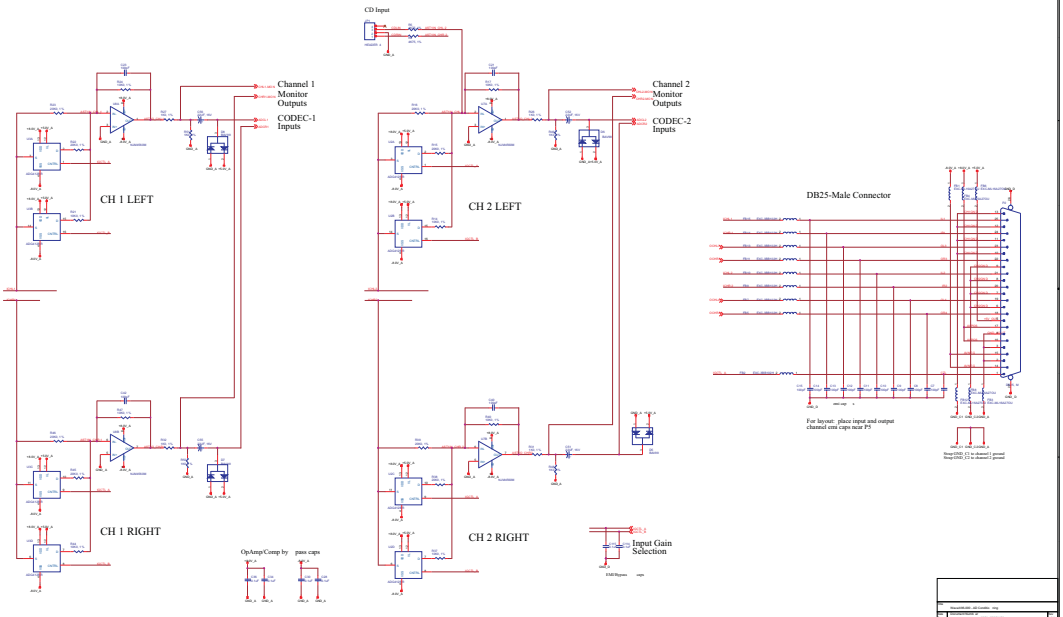
ADC Analog Conditioning



DAC Analog Conditioning

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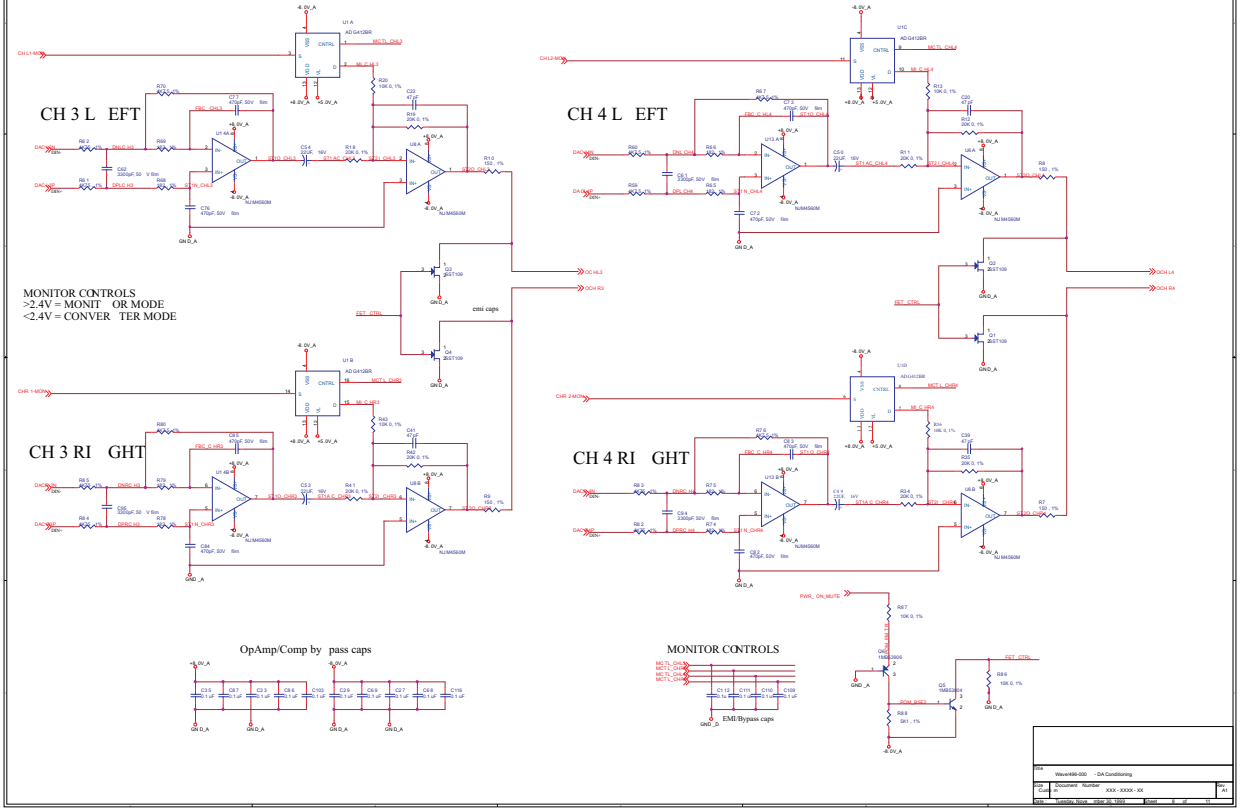
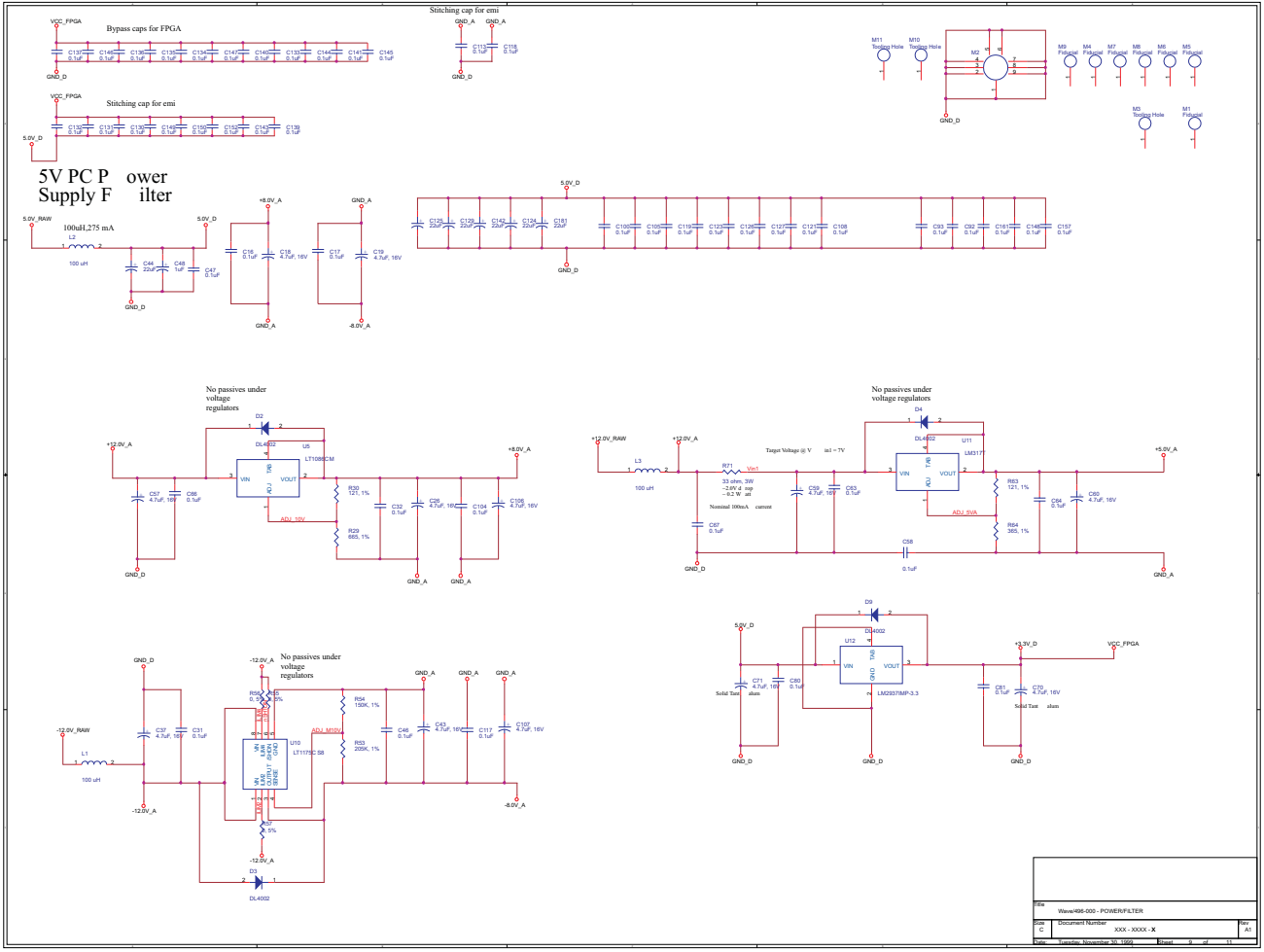
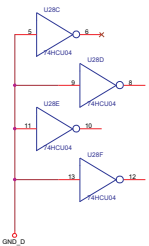
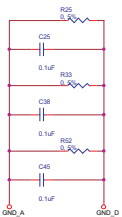
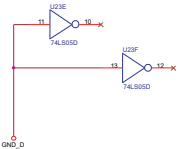



Bypass caps for FPGA
Stitching cap for emi
Stitching cap for emi
5V PC P ower
Supply F ilter
100uH,275 mA
No passives under voltage regulators
No passives under voltage regulators
No passives under voltage regulators
Solid Tant ohsm
Solid Tant ohsm
Wave496-000 - POWER/FILTER
XXX - XXXX - X
Tuesday, November 30, 1999

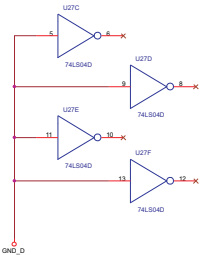
Test Headers







Spare gates



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REVISION HISTORY

A1 - Wave/424-000: Schematic Review 03/03/99
A2 - Wave/424-000: Schematic Review 03/17/99
A3 - Wave/424-000: Freeze Design 04/05/99
A4 - Wav e/424-000: 256*Fs - 24.576MHz and 11.2896MHz Crystals only
A5 - Wave/424-000: Use FS6377-01 Prog. Osc. 5/10/99
A6 - Wave/ 424-000: Final clean-up and release for inital build 5/19/99
B1 - Wave/42 4-001: See ECO-001.xls for edits. Design review held 08/20/99
A1 - Wave/496-000: See WAV496.xls for design modifications

STUFF OPTIONS

Digital 5V from PCI connector	5V_D through R55 only	If EMI radiated around PCI connector, more 5V_D taps
	DNI - R73, R103	Install - R73, R103, C73, C128
Reference for Master Clock	P.O. Reference on base card only	Reference on base card or daughtercard
	DNI - R120,R136,R137,C157, C169,C177,C178,U27,Y3 Install - Y1	DNI - Y1 Install - R120,R136,R137,C157,C169,C177,C178,U27,Y3
Observability	Maximize for proto/debug	Minimize for production/emi testing
	Install - R116,R131,R132	DNI - R116,R131,R132
FPGA Configuration	Byte Blaster configuration	UART Configuration (production)
	DNI - R123,R124,R125,R126,130	Install - R123,R124,R125,R126,130
CODEC bypass caps	As per eval board, app note	Bypass filtered +5V_A to analog ground
	DNI - C78,C90 Install - C80,C92	DNI - C80,C92 Install - C78,C90
EMI stitching caps	Install - C131,C132,C140,C159, C158,C151,C147,C137,C114,C107	DNI - C131,C132,C140,C159, C158,C151,C147,C137,C114,C107
Ground Plane Jumpers	Install - R1,R51,R16,R68, R52,R71,R74,R17,R32,R61	