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**Professional Experience:**

* Total **4+ years of Experience in Pre and Post Silicon Validation**.SOC Architecture, FPGA Emulation platform and Zebu, Design and Developed Embedded System Software for Various Peripherals.
* Currently Working as Software Engineer in **EmWare Technologies (INDIA) Pvt. Ltd** Bangalore-48, since January 2015 to till date.

**Profile Summary:**

* Worked on entire life cycle of Pre and Post Silicon Validation methodology for various IP’s of different SOCs.
* Knowledge on Palladium Emulation Platform.
* Proficient knowledge in **C** and **Embedded C.**
* **Involved in C content development during Pre and Post silicon validation.**
* Experience in memory interface protocols such as **DDR3, DDR4, LPDDR3** and **LPDDR4**.
* **Commit to the development of new validation procedures.**
* Embedded coding in C and Assembly Language with knowledge of processor micro-architecture.
* Good understanding of **Hardware Schematics**.
* Working experience on IIC/I2C Firmware Development.
* Worked on Windows and Linux Operating systems.
* Hands on Experience on **LED, LCD, EEPROM and RELAY**.
* Worked on 8,16,32-bit Microcontrollers.
* **Hands on experience on RS-232, MAX-232.**
* Working experience on Debugging tools like: **GDB, JTAG, Trace 32,Lauterbach.**
* Work with SOC development team and platform team for trouble shooting of hardware and software issues.
* Testing the Hardware Boards with Oscilloscope, Multi-Meter and Debugging the Firmware.

Emulation Tools Used:

|  |  |  |
| --- | --- | --- |
| Skill(Tool) | Years of Experience | Description |
| Emulation | 4 years | DDR4 Controller, SD Host controller, UART,TWI,ADC |
| Zebu | 2 years | DDR4 Controller, UART, ADC |

**Technical Summary:**

* Programming Languages : C and Embedded C.
* Protocols : UART, IIC/I2C, SPI.
* IDEs : KEIL µvision 4.0 and 5.0, VIM Editor.
* Emulation Tools : FPGA, Zebu.
* Debugging Tools : GDB, JTAG, CRO and DMM.
* Compiler Tools Used : GCC, ARM GCC Cross Compiler.
* Operating System : Linux, Windows.
* Scripting Language : Python.
* Hardware Modules : LED,LCD,SEVEN SEGMENT

DISPLAY, EEPROM and RELAY.

**Projects Executed:**

**As a Validation Engineer, I have worked Silicon Validation for various IPs of several SOCs.**

**Key roles played:**

* Quick walkthrough the IP specifications for what I am responsible.
* Identifying and making a list of features to be validated as part of Post Silicon Validation.
* Preparation of Test Plan and interacting with the designer to get more knowledge on particular feature to be validated.
* Tracking and reviewing the features to be validated.
* Development of code in C, for all features to be validated.
* Raised JIRA tickets and tracked the issue till it gets resolved.
* Trouble shooting hardware issues with the help of Oscilloscope.
* Co-ordination with Software Team.

## PROJECTS:

**Project #05**:  **PRE AND POST SILICON VALIDATION OF DDR4 CONTROLLER**

**Roles and Responsibilities:**

* Quick walk through the specifications of DDR4 from JEDEC.
* Used Zebu emulation Environment for Pre-Silicon Validation.
* Understood the legacy test plan and code.
* Actively interacted with the designer team through mail chains and conferences.
* Developed feature to print test case execution time stampings in every test case.
* Developed algorithm for the features to be validated.
* Worked on DDR4 Controller validation test plan enhancement and updated as per the features that I have owned.
* Validated features like:
* DDR4 SDRAM Memory initialization.
* Data read and write for 32-bit data bus width.
* Data read and write for 64-bit data bus width.
* CAS latencies of 13, 15,17and 18.
* Burst length of 8.
* Burst type of Sequential.
* Self Refresh and Power-Down modes for low power.
* Save and Restore Mode.

**Project#04: PRE AND POST SILICON VALIDATION OF SOC IP: SECURE DIGITAL HOST CONTROLLER**

**Roles and Responsibilities:**

* Understood the SD Host controller 3.0 specification.
* Used FPGA Emulation Platform in Pre Silicon Validation.
* Gone through SDHC3.0 compliance test related specifications.
* Prepared test plan and developed code in C for the following compliance features.
* Card Initialization and Identification.
* Host Initialization.
* PIO data transfer for 1 bit Bus width and 4 bit Bus width.
* Validated various types of SDSC, SDHC and SDXC cards of various speed classes: 2, 4,6,10 etc.

**Project#03: UART IP PRE AND POST SILICON VALIDATION.**

**Roles and Responsibilities:**

* In Pre silicon validation used Zebu emulation Environment.
* Created libraries for UART and DMA features
* Validated UART features like Baud rate, data bits, number of stop bits, parity check support.
* Also validated the same features on multiple UARTs of same SOC.
* Worked on validation of Hardware flow control features.
* Worked on Rx FIFO and Tx FIFO feature Validation.
* Transfers with no flow control settings set.
* Worked on developing validation scripts to run all diagnostics in automated environment and separated all the manual test features where ever hardware connection changes etc required.

**Project# 02: PRE and POST SILICON VALIDATION OF TWI IP.**

**Roles and Responsibilities:**

* Understanding the project requirements and preparing a project system test plan.
* Used FPGA Emulation Platform in Pre Silicon Validation.
* Understood specifications of TWI.
* The frame format and working of TWI protocol.
* Understood the customer requirements and prepared a test plan with purpose, understood algorithm, execution environment, Pass/Fail Criteria and dependencies as part of the each and every test case.
* Developed the application code for TWI.
* Validated features like
* Write operation in Standard Speed mode with 7-bit address.
* Read operation in Standard Speed mode with 7-bit address.

**Project#01: PRE AND POST SILICON VALIDATION OF ADC**

**Roles and Responsibilities**:

* In Pre silicon validation used Zebu emulation Environment.
* Gone through the 10 bit resolution ADC specification.
* Listed the features to be validated as per the requirement.
* Test plan preparation for below features.
* Validated features like:
* Validated 10 bit mode resolutions with various reference Voltages.
* Validated step size, max clock support, resolution features etc.
* Verified the data conversion period.

**Qualification:**

* Master of Technology (CSP) from G.Pulla Reddy Engineering College (Autonomous), Kurnool Affiliated to JNTUA, Anantapur with 7.35 CGPA.
* Bachelor of Technology(ECE) from ALFA College of Engineering & Technology, Allagadda Affiliated to JNTUA, Anantapur with an aggregate of 66.97%.
* Intermediate from The Nandyal Junior College, Nandyal with an aggregate of 94.4%.
* SSC from YPPM Govt. High School, Allagadda with an aggregate of 89.33%.