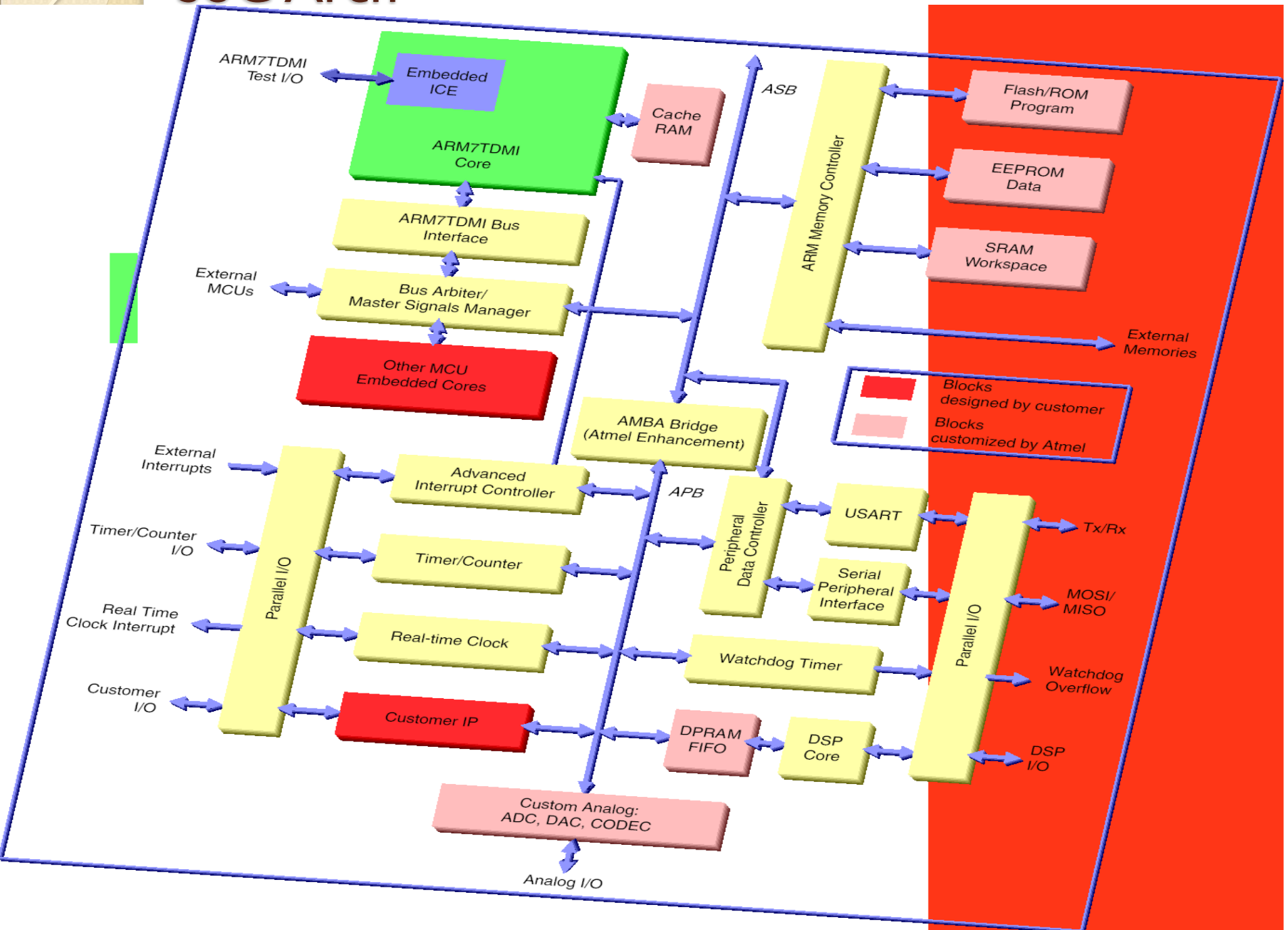
Intel Atom Architecture – Next Generation Computing

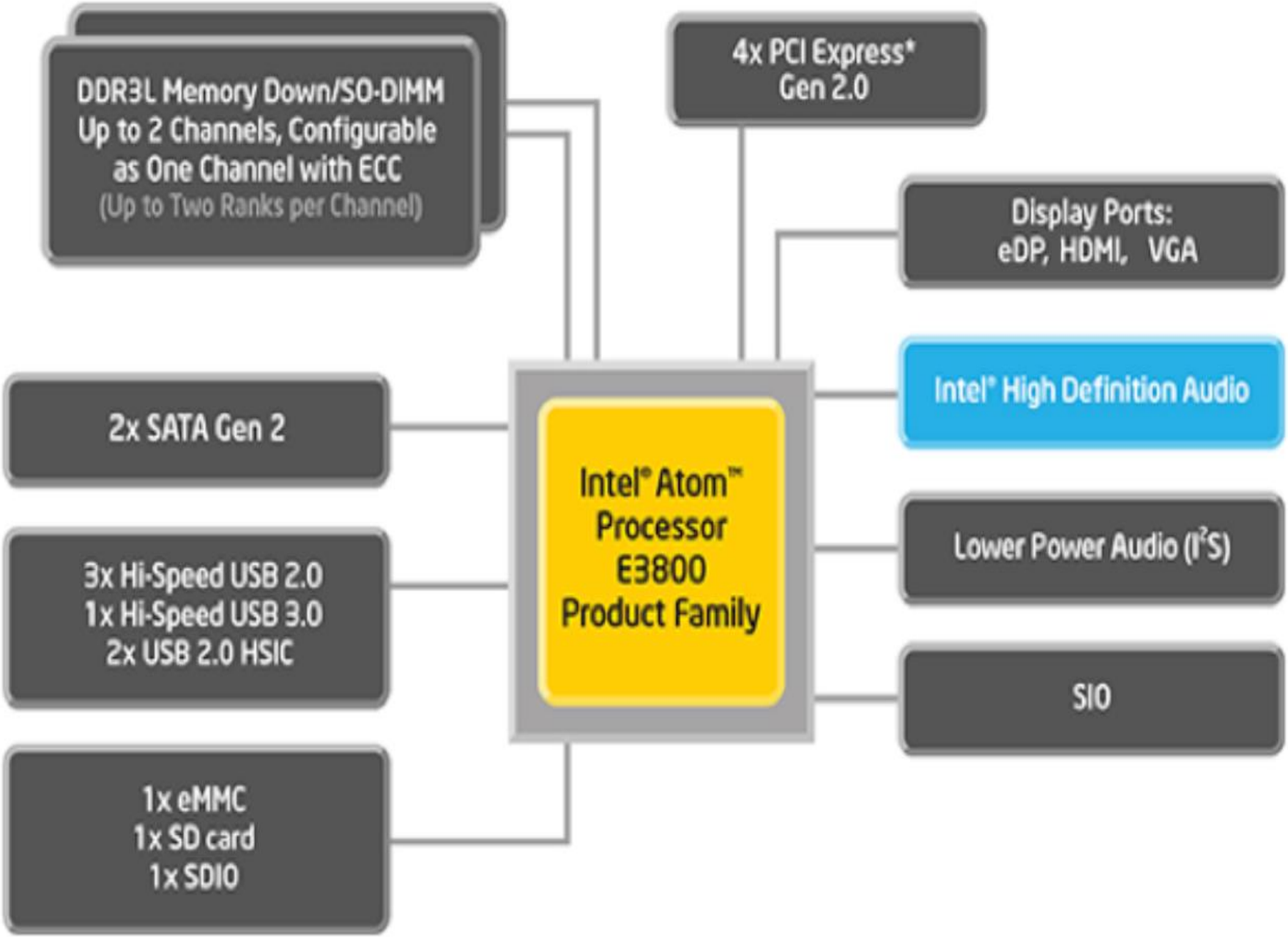
SoC Arch


ARM7TDMI Test I/O
Embedded ICE
ARM7TDMI Core
Cache RAM
ASB
ARM Memory Controller
Flash/ROM Program
EEPROM Data
SRAM Workspace
External Memories
ARM7TDMI Bus Interface
External MCUs
Bus Arbiter/ Master Signals Manager
Other MCU Embedded Cores
Blocks designed by customer
Blocks customized by Atmel
AMBA Bridge (Atmel Enhancement)
External Interrupts
Advanced Interrupt Controller
APB
Peripheral Data Controller
USART
Tx/Rx
Timer/Counter I/O
Timer/Counter
Serial Peripheral Interface
MOSI/ MISO
Real Time Clock Interrupt
Real-time Clock
Watchdog Timer
Watchdog Overflow
Parallel I/O
Customer I/O
Customer IP
DPRAM FIFO
DSP Core
DSP I/O
Custom Analog: ADC, DAC, CODEC
Analog I/O

Overview

- Intel's smallest and lowest power processor 1.6 GHz (TDP 2.5 W)
  - TDP – Thermal Design Power
    - maximum amount of power the cooling system in a computer is required to dissipate.

- The Intel® Atom™ processor enables the industry to create pocket-sized and low power Mobile Internet Devices (MIDs), and Internet-focused notebooks (netbooks) and desktops (nettops).


DDR3L Memory Down/SO-DIMM
Up to 2 Channels, Configurable
as One Channel with ECC
(Up to Two Ranks per Channel)
4x PCI Express*
Gen 2.0
Display Ports:
eDP, HDMI, VGA
Intel® High Definition Audio
Lower Power Audio (I²S)
SIO
2x SATA Gen 2
3x Hi-Speed USB 2.0
1x Hi-Speed USB 3.0
2x USB 2.0 HSIC
1x eMMC
1x SD card
1x SDIO
Intel® Atom™
Processor
E3800
Product Family

Atom Intended Usage

- Portable internet capable devices
- Not computationally as capable as a desktop
- Used in mobile phones and Netbooks also in desktops

Types of Intel Atom

- Three series of Atom processors released
- N series and Z series are both single core
  - Used in mobile phones and netbooks
- D series are dual core processors and are used in desktops and even servers
- The TDP can vary from as low as 0.65 W to 13 W

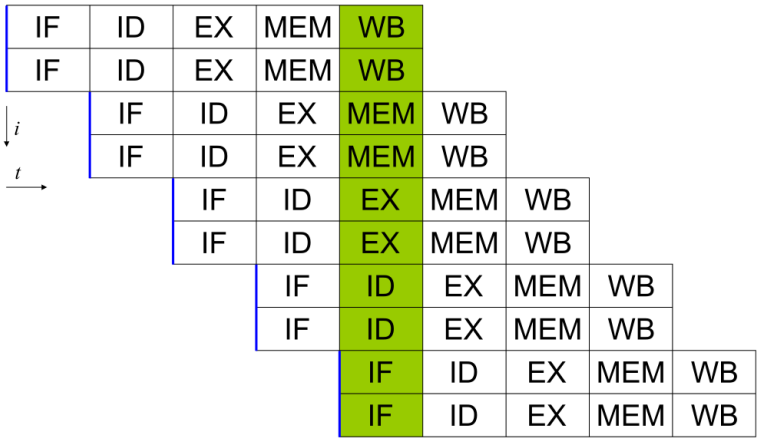
Atom Architecture

- Superscalar – 2 issue
  - Multiple instruction processed at the same time by the processor
  - Different from instruction pipelining
  - Uses multiple redundant hardware components in the processor at the same time

Instruction Pipelining

Instr No.	Pipeline Stage						
1	IF	ID	EX	MEM	WB		
2		IF	ID	EX	MEM	WB	
3			IF	ID	EX	MEM	WB
4				IF	ID	EX	MEM
5					IF	ID	EX
Clock Cycle	1	2	3	4	5	6	7

Superscalar – 2 issue



In-order and Out of order execution

In-order

- Instruction fetch.
- If input operands are available (in registers for instance), the instruction is dispatched to the appropriate functional unit.
- If one or more operand is unavailable during the current clock cycle (generally because they are being fetched from memory), the processor stalls until they are available.
- The instruction is executed by the appropriate functional unit.
- The functional unit writes the results back to the register file.

Out-Of-Order

- Instruction fetch.
- Instruction dispatch to an instruction queue (also called instruction buffer)
- The instruction waits in the queue until its input operands are available.
- The instruction is then allowed to leave the queue before earlier, older instructions.
- The instruction is issued to the appropriate functional unit and executed by that unit.
- The results are queued.
- Only after all older instructions have their results written back to the register file, then this result is written back to the register file.

Advantages and Disadvantages of in-order processing

Advantages

- Eliminates Instruction Reordering Logic
  - Reduces Power Consumption
  - Reduces Die Space

Disadvantages

- Lower Performance
  - Data dependencies are more critical
  - Memory Accesses and slow floating point operations stall the pipeline for longer time
  - Inefficiency in CPU hardware usage

Safe Instruction Recognition

- Start the execution of a low latency integer operation when a floating point operation is waiting for resources

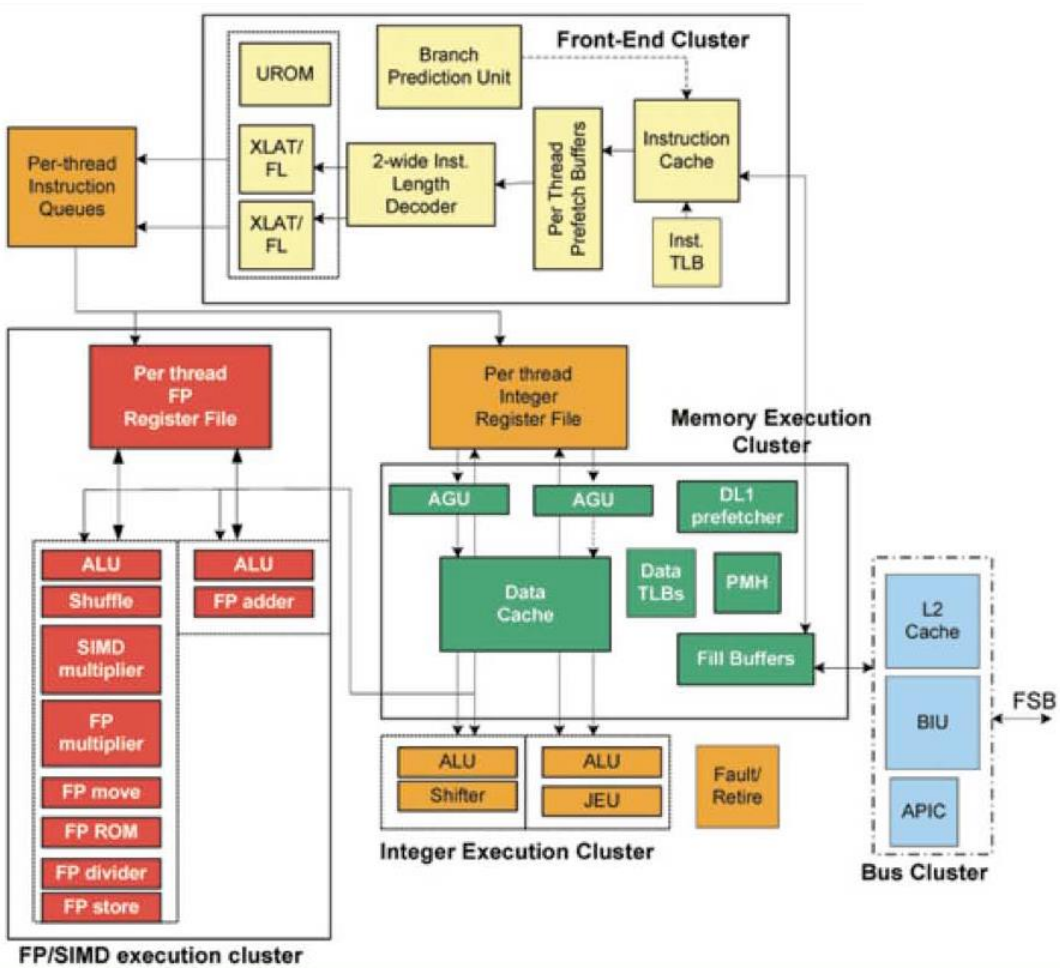
Instruction Set and Functional Units

ISA

- Intel x86 compatible instruction Set
  - Just like any desktop computer
- Instruction length are variable (CISC)
- Support for SIMD instructions

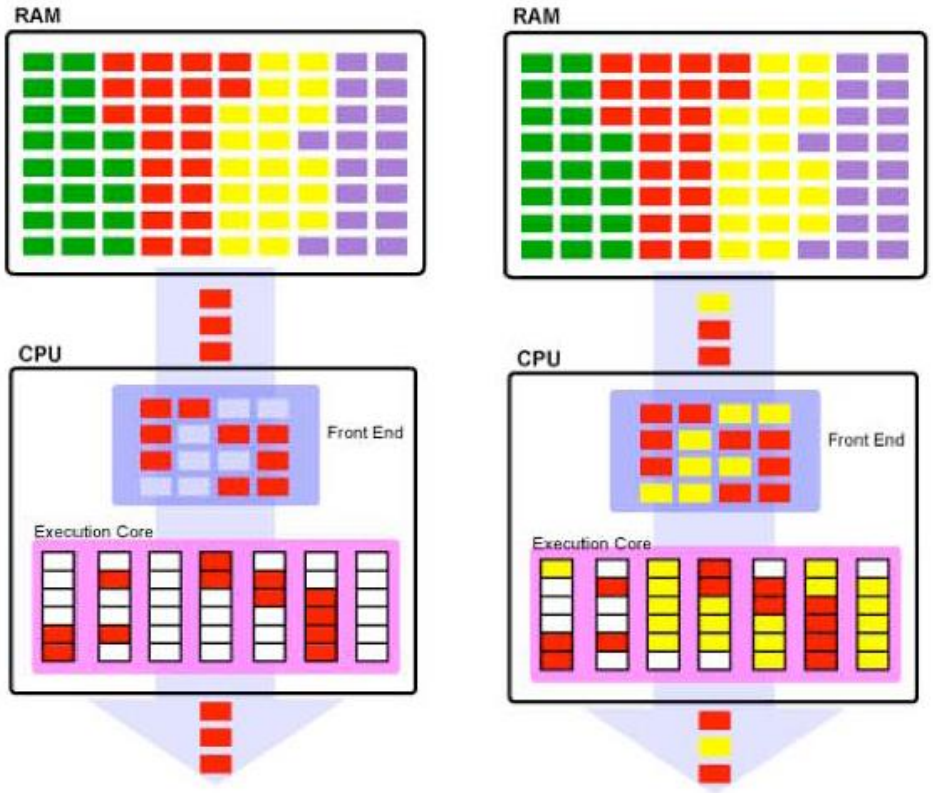
Functional Units

- Minimum number of functional units to reduce power
- 2 Integer ALUs
- 2 Floating Point ALUs



Simultaneous Multi-threading

- Hyper-threading technology
- 2 threads can execute simultaneously
- Leads to increase in power consumption by less than 20 %
- Performance improves by about 40 %

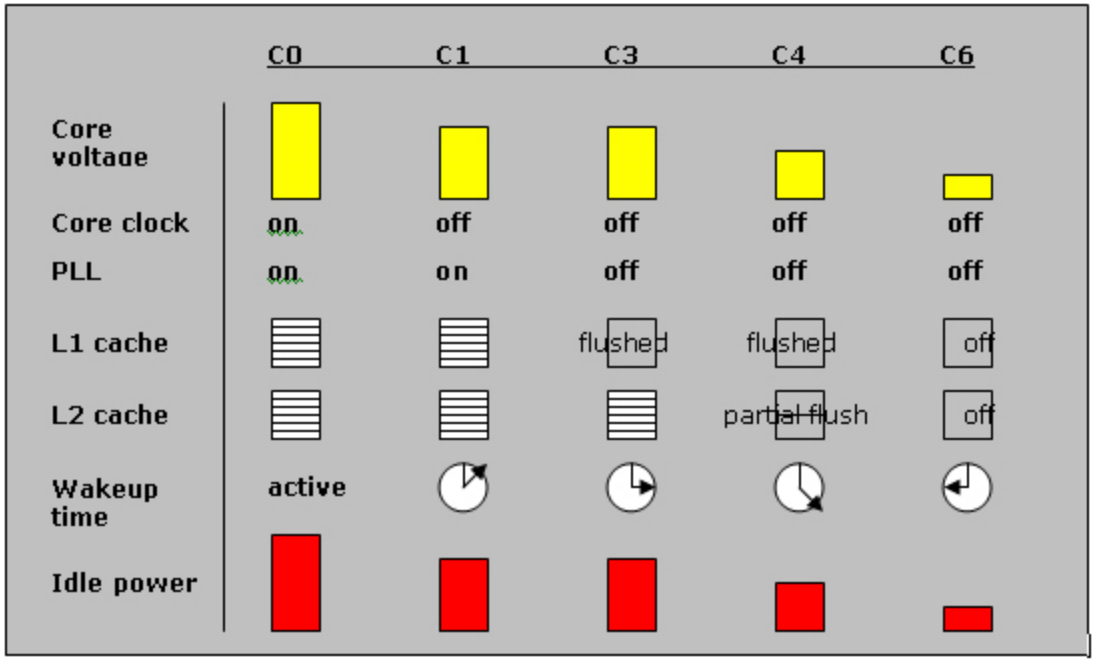


Power Management Options – Frequency Scaling

- Frequency Scaling
  - 8 different operating frequency.
  - Can reduce the frequency to up to 13 % of maximum (1.6 GHz).
  - Reducing frequency reduces power consumption
  - May increase execution time and hence energy consumption
  - Will definitely control operating temperature

Power Management Options – Sleep Scheduling

- 6 sleep states C1 through C6
- Sleep states mainly drains or shuts down the cache
- Also shuts down the core clock
- However, there is time penalty to wake up from the sleep states
- Computation can only take place in C1 state



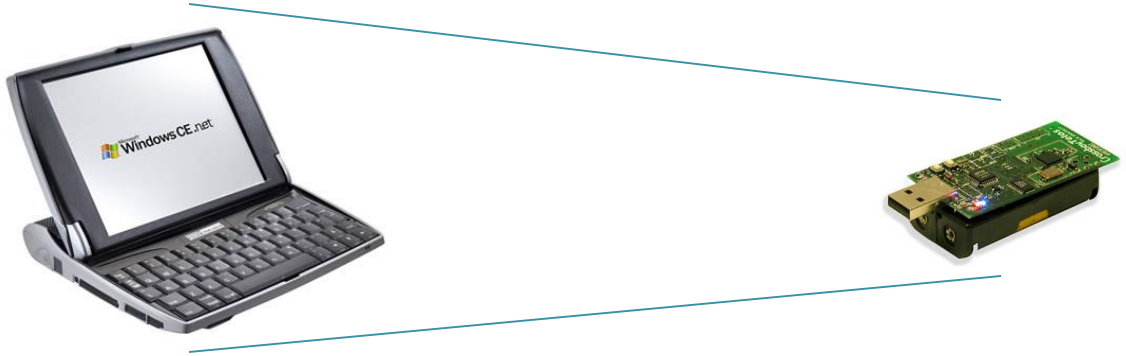
Software Control on Power Management

- Advanced Configuration and Power Interface (ACPI)
- Linux based set of commands
- Sleep scheduling –
  - echo NUM > /proc/acpi/sleep, NUM = 1 … 6
- For waking up alarm can be set in the real time clock
- Frequency scaling –

echo NUM>/proc/acpi/processor/CPU0/performance, NUM = 0…7

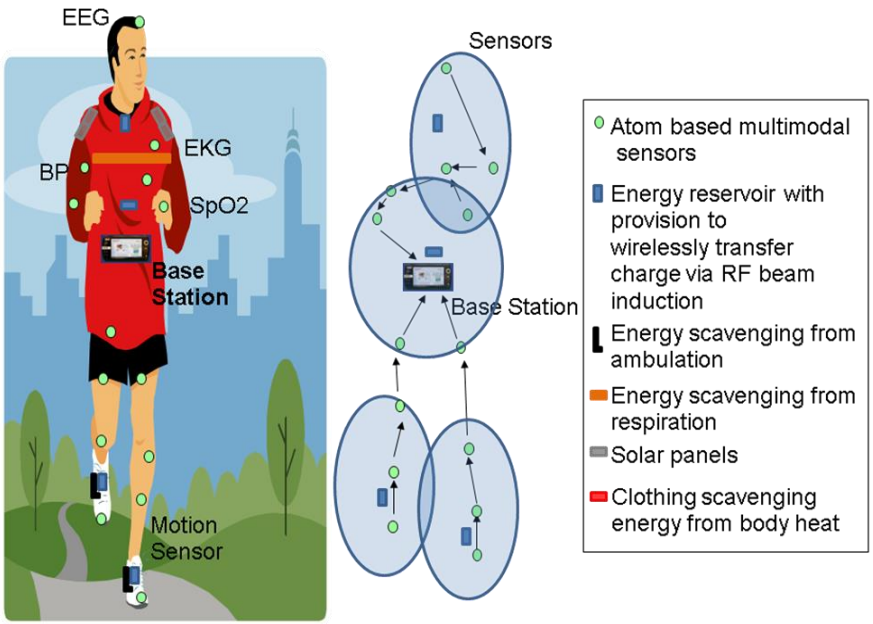
Innovative Idea at IMPACT Lab

- Usage of Atom processors in sensors on body

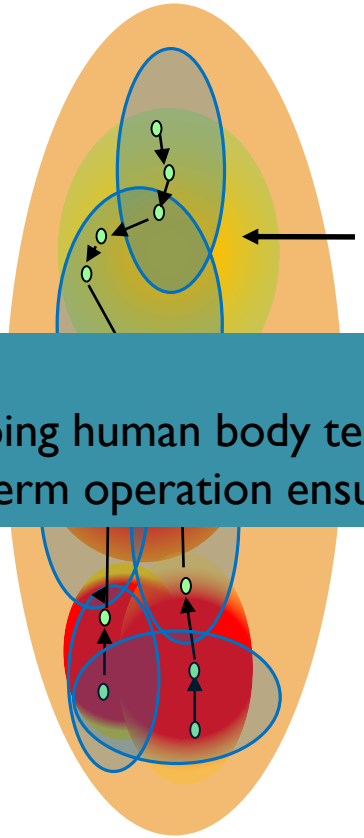


Body Sensor Networks

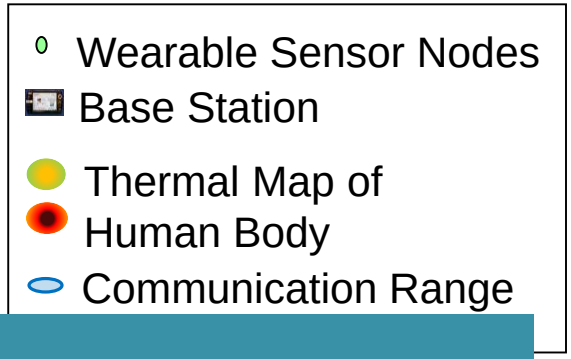
- Sensors sense physiological signals
- Communicate with each other through wireless channel
- Simple computation capabilities
- Very low power



Problems



Heating effects

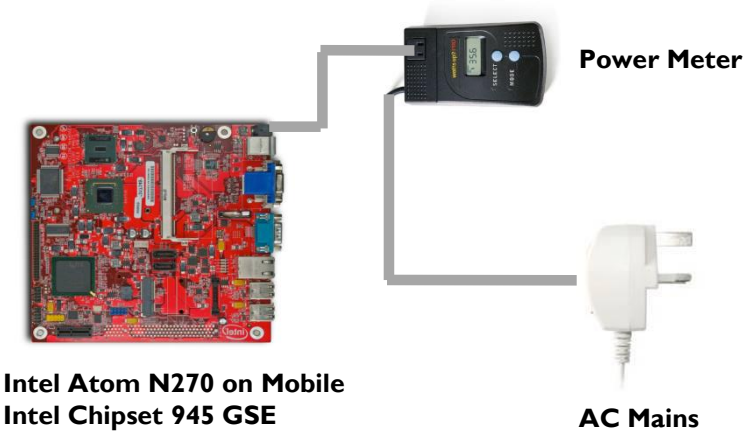


Concerns:

1. Thermal safety – Keeping human body temperature within safe limits
2. Sustainability – Long term operation ensuring minimum battery drainage

Body Sensor Network (BSN)

Power Measurements



Power Measurement Set up

Operating Mode (Percent throttling)	Power (W)
0	0.191
13	0.1864
25	0.17
37, 50, 62, 75	0.167
87	0.164

Table showing Atom power consumption at different operating frequencies

The entire platform takes around 11 W of power as the chipset is elaborate

Temperature Profiling

- The temperature rise of human skin due to contact with Atom based BSN node has to be evaluated
- The temperature rise occurs due to several physical phenomenon and is modeled using the Penne's bioheat equation -

$$\rho C_p \frac{dT}{dt} = K\nabla^2 T - b(T - T_b) + \rho SAR + P_c + A\sigma(T^4{}_r - T^4)$$

Heat accumulated | Heat transfer by conduction | Heat transfer by convection | Heat by electromagnetic radiation | Heat by power dissipation | Heat by radiation

Operating Mode (Percent Throttling)	Atom Processor Operating Temperature (°C)	Maximum Skin Temperature (°C) after 24 hrs of operation	Thermal Damage Temperature (°C)
0, 13, 25	43	39.4365	39.2
37, 50	42	39.3325	
62, 75	41	39.2295	
87	39	39.0264	

Thermal damage parameter calculated according to Henrique and Moritz [5]. Maximum temperature must not exceed this.

5. F. C. J. Henriques et al. Studies of thermal injury: I. the conduction of heat to and through skin and the temperatures attained therein. A theoretical and an experimental investigation. In *Am J Pathol.*, *pages* 530–549, July. 1947.

Research Questions

- Use frequency control and processor sleep scheduling to reduce the power consumption of Atom to the level of a sensor
- Limit the heating effect of Atom to safe levels
- Ultimate Goal
  - A safe and sustainable Body Sensor Network with Intel Atom processors

Thank You