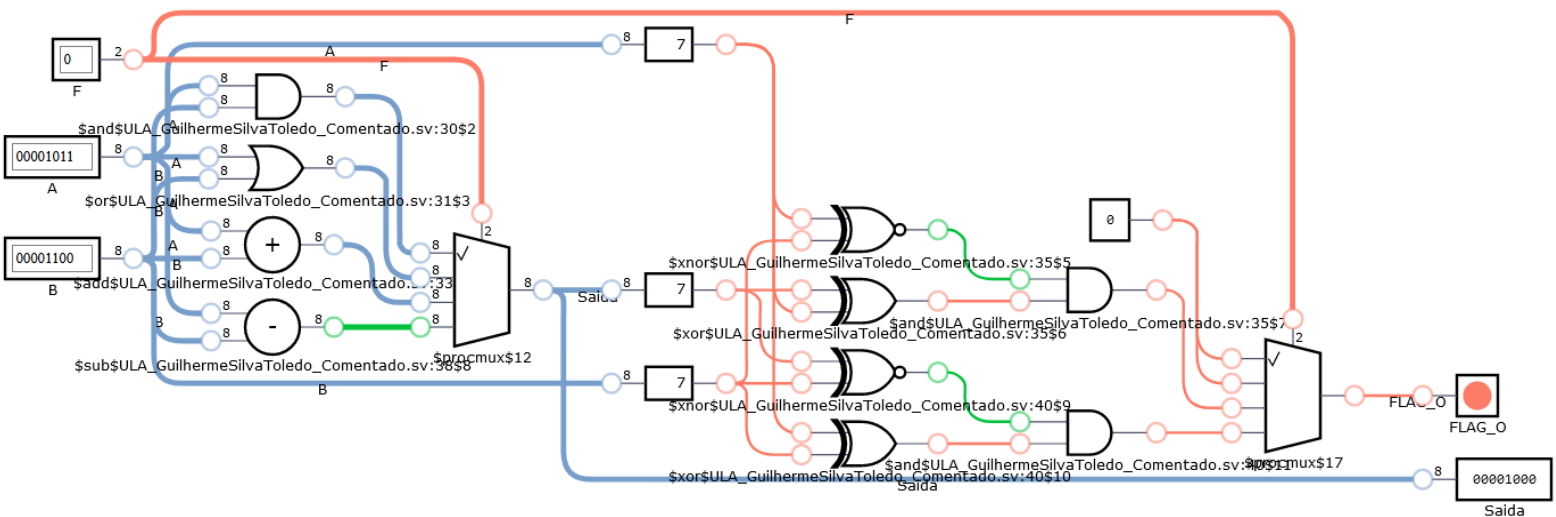
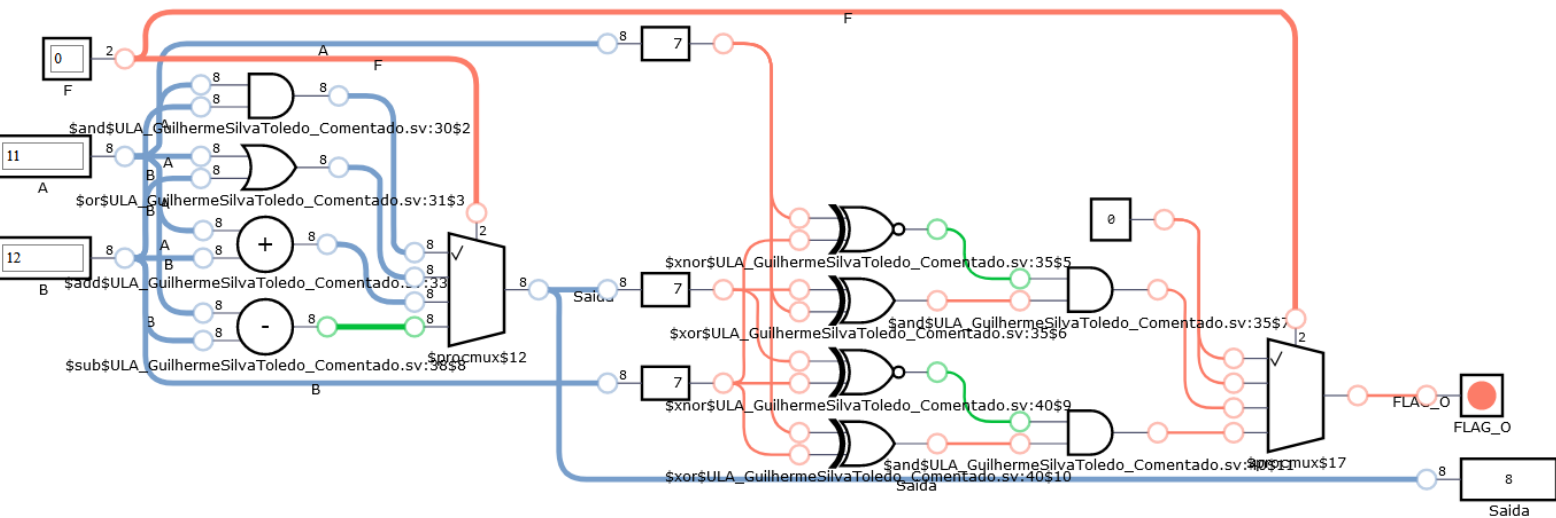


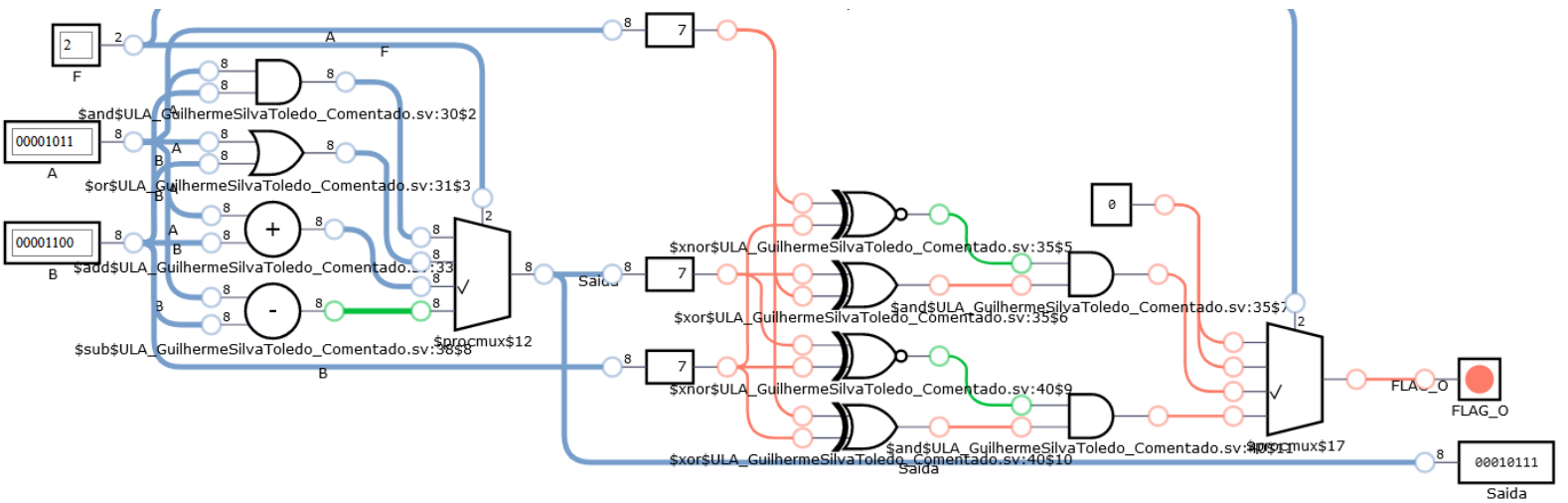
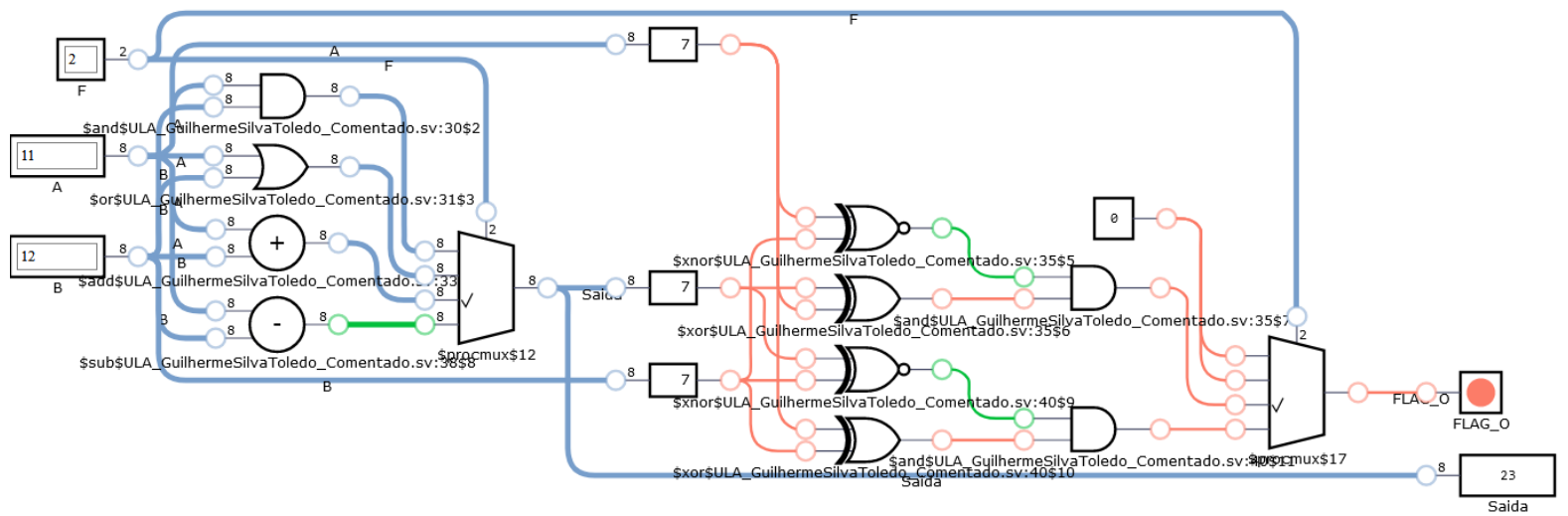
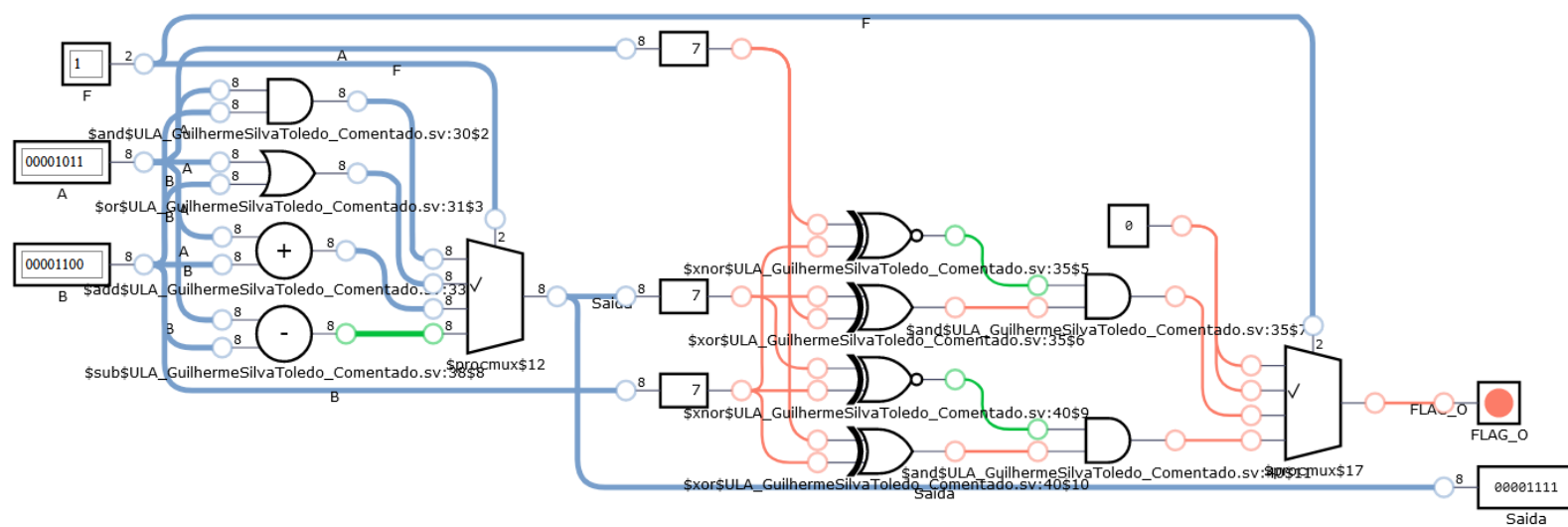
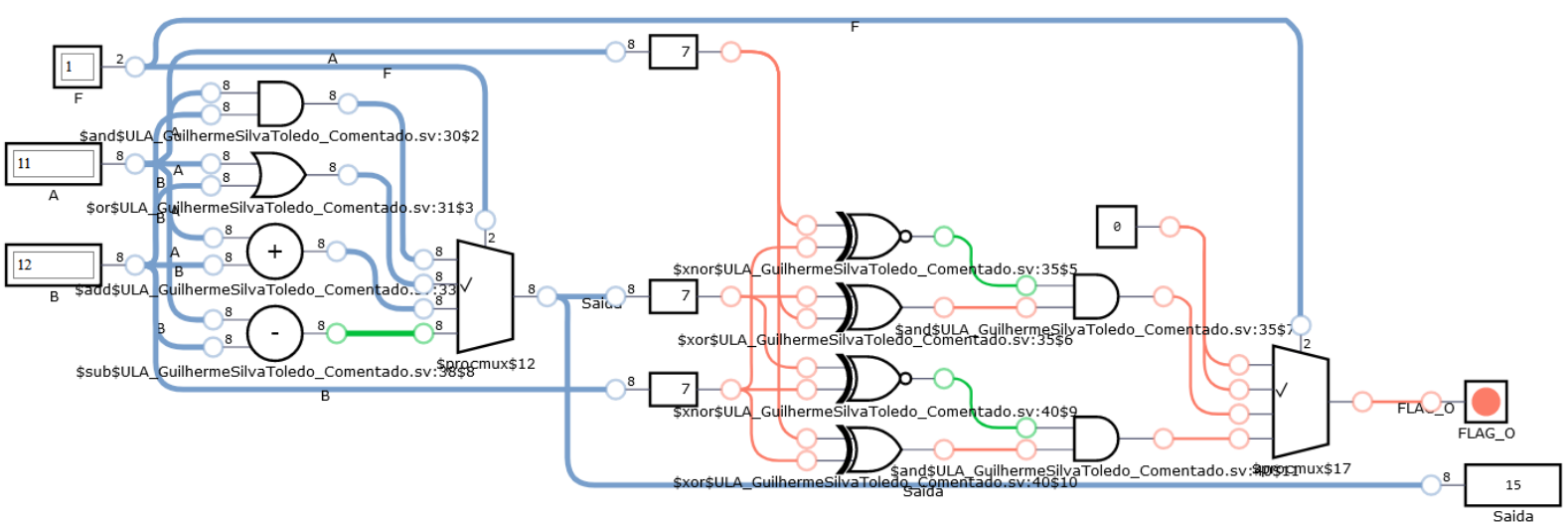
ULA feita com as operações pedidas no roteiro 3

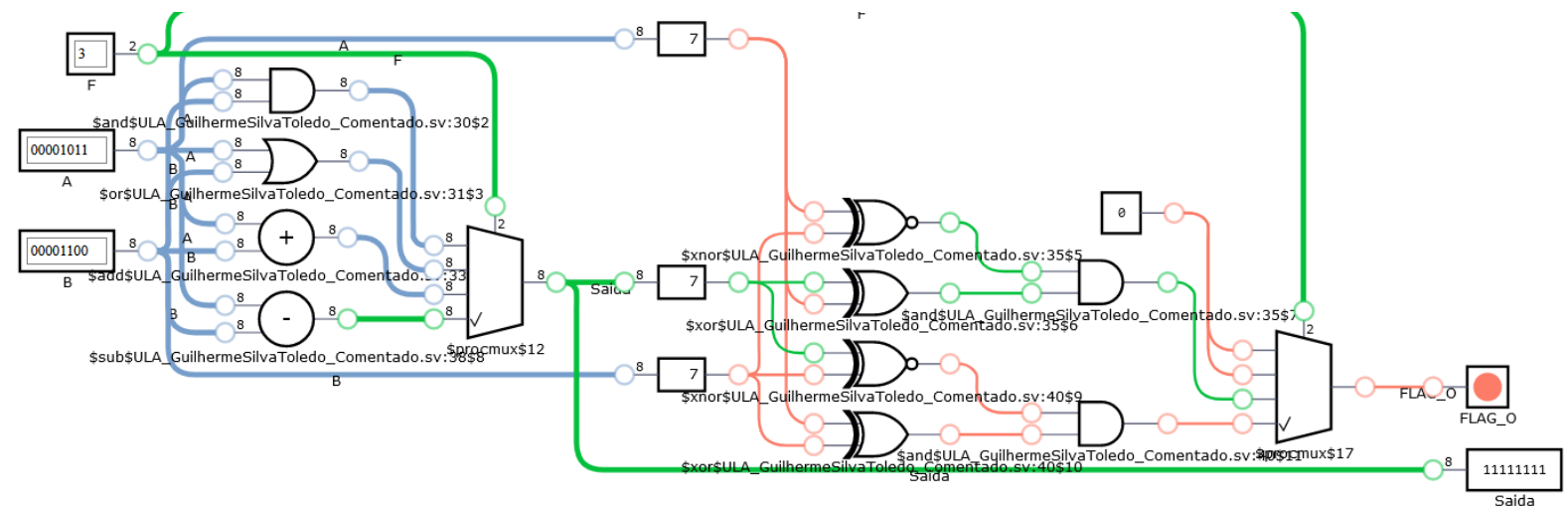
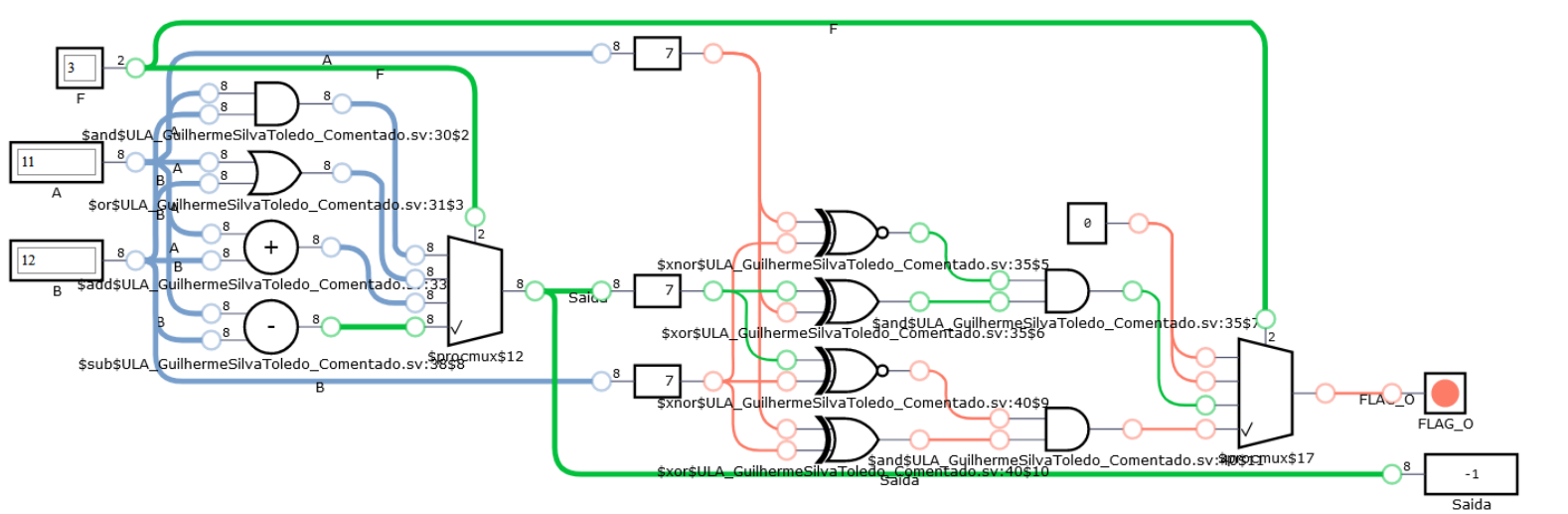
Algumas observações interessantes podem ser feitas:

- Mesmo apenas existindo um 'Case' no código, a existência de duas saídas utiliza dois multiplexadores em vez de apenas 1;
- Como descrito no código em System-Verilog todo o problema lógico de calcular overflow e underflow pode ser simplificado para algumas portas xor, xnor e and;
- A forma implementada permite o fácil escalonamento para quaisquer N bits;

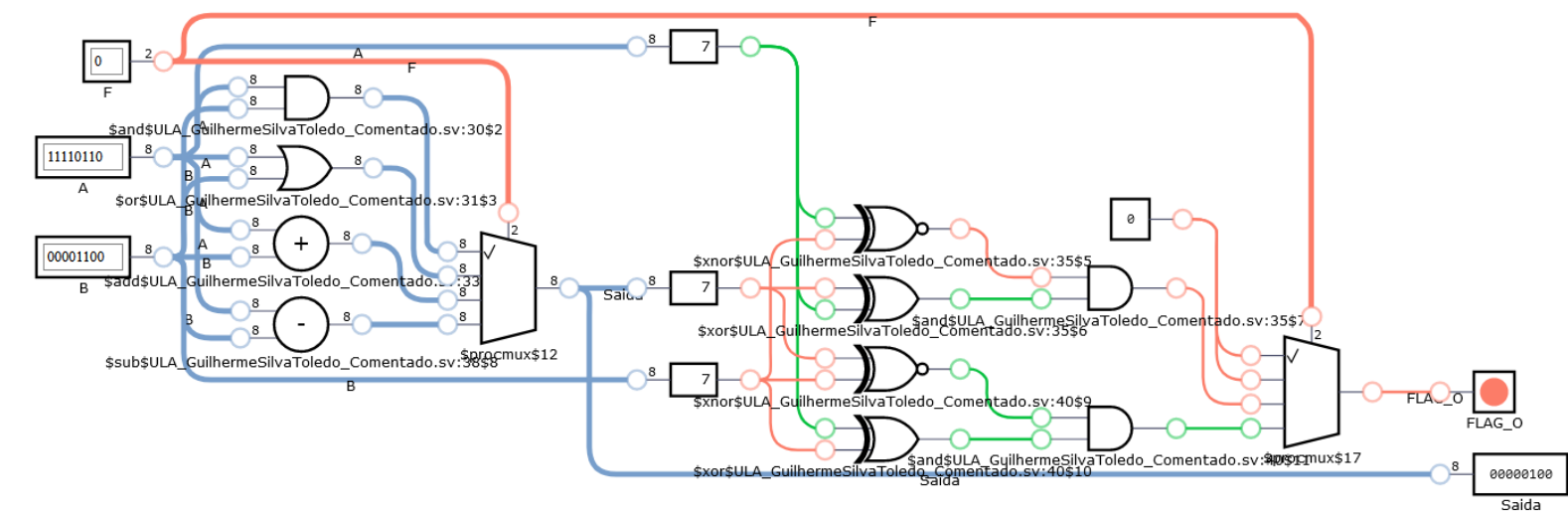
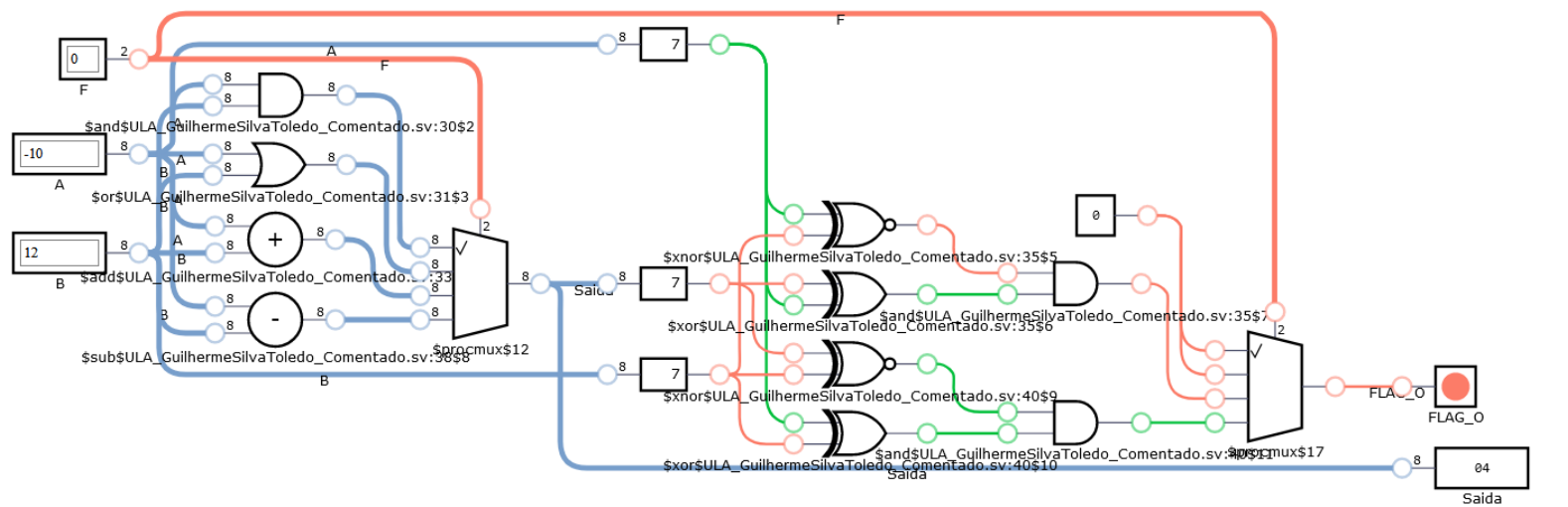
A = 11 e B = 12: AND, OR, SOMA & SUBTRAÇÃO. RESPECTIVAMENTE

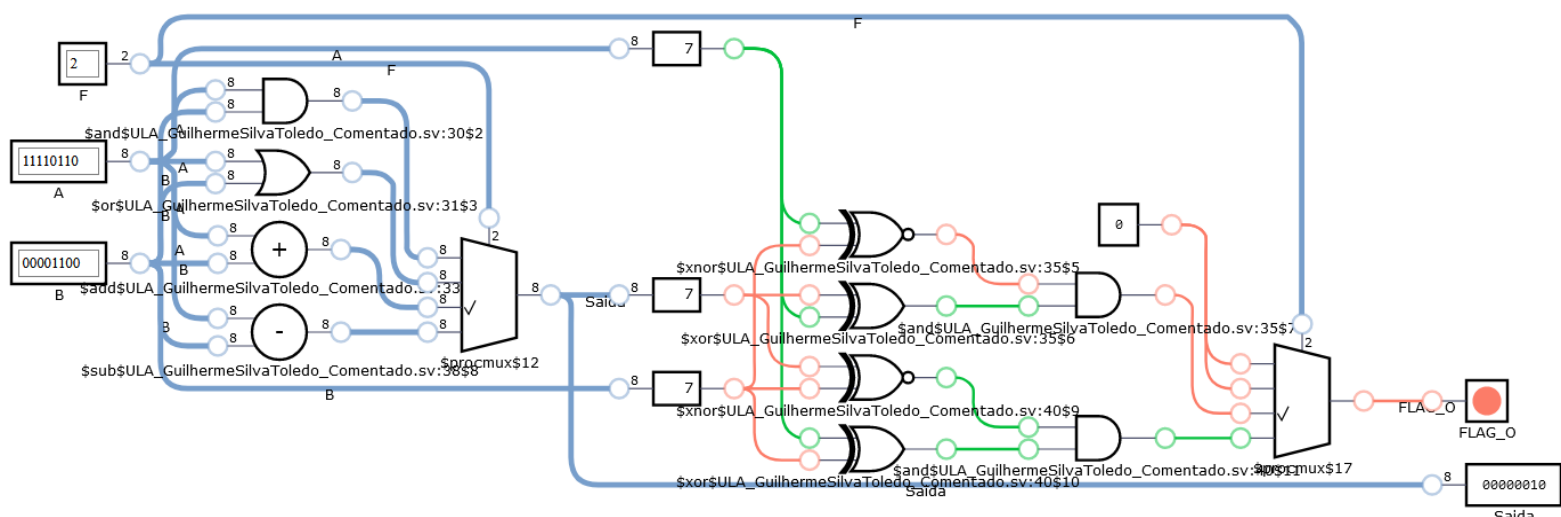
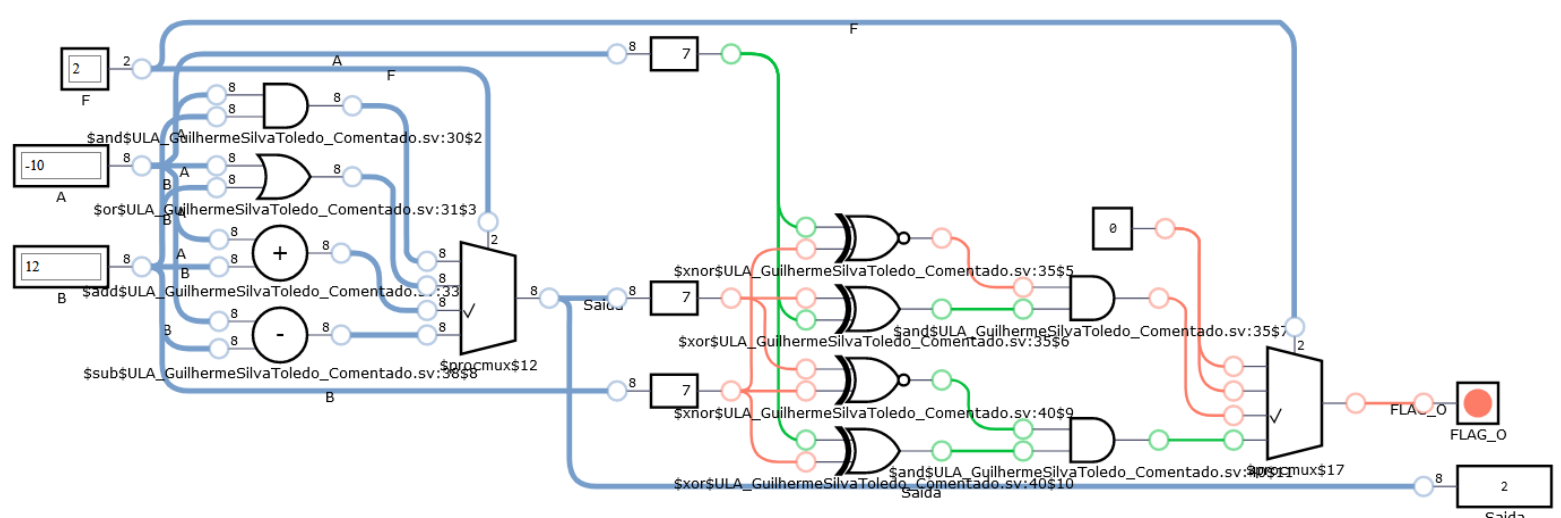
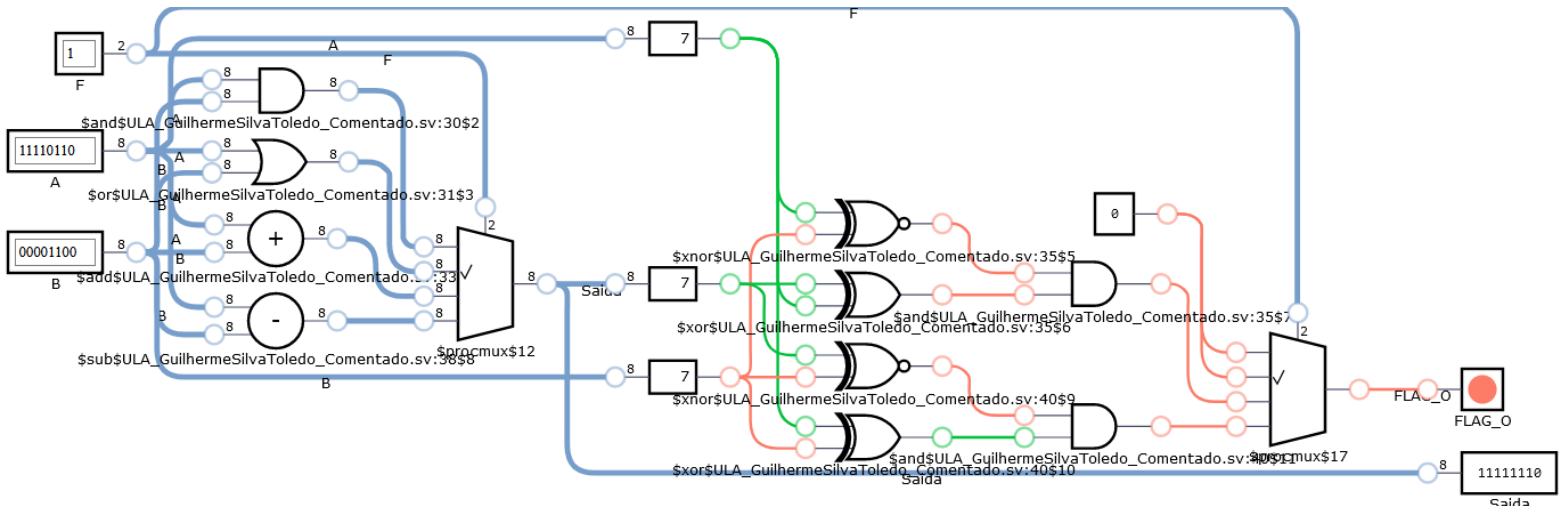
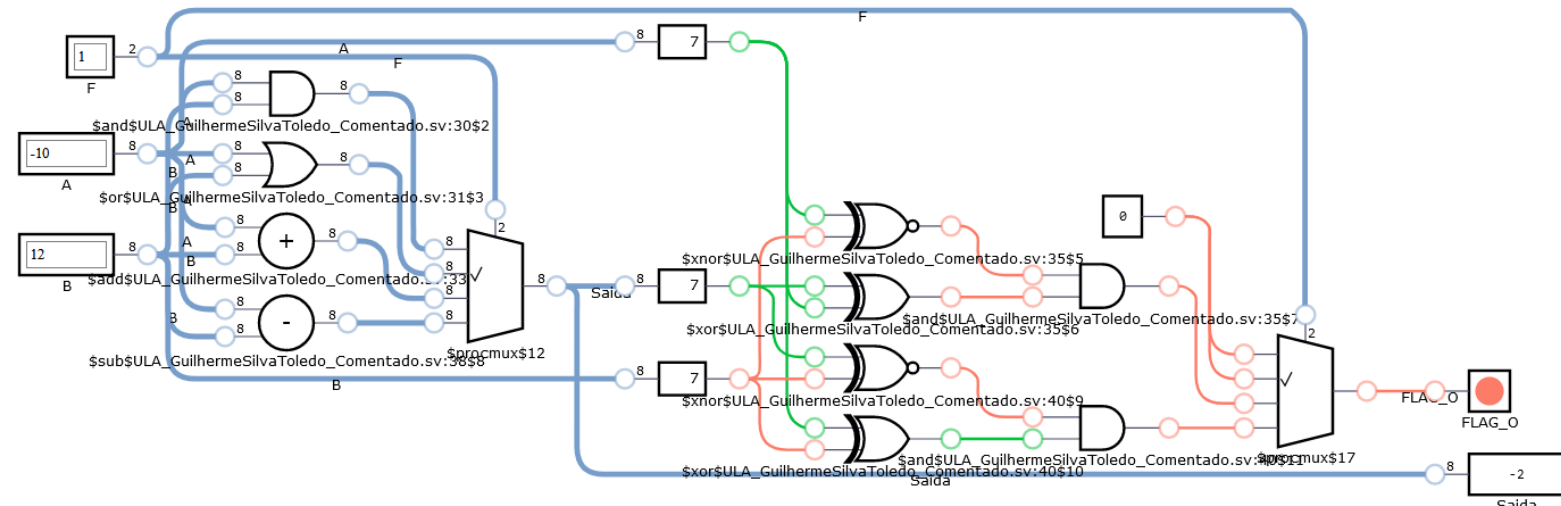


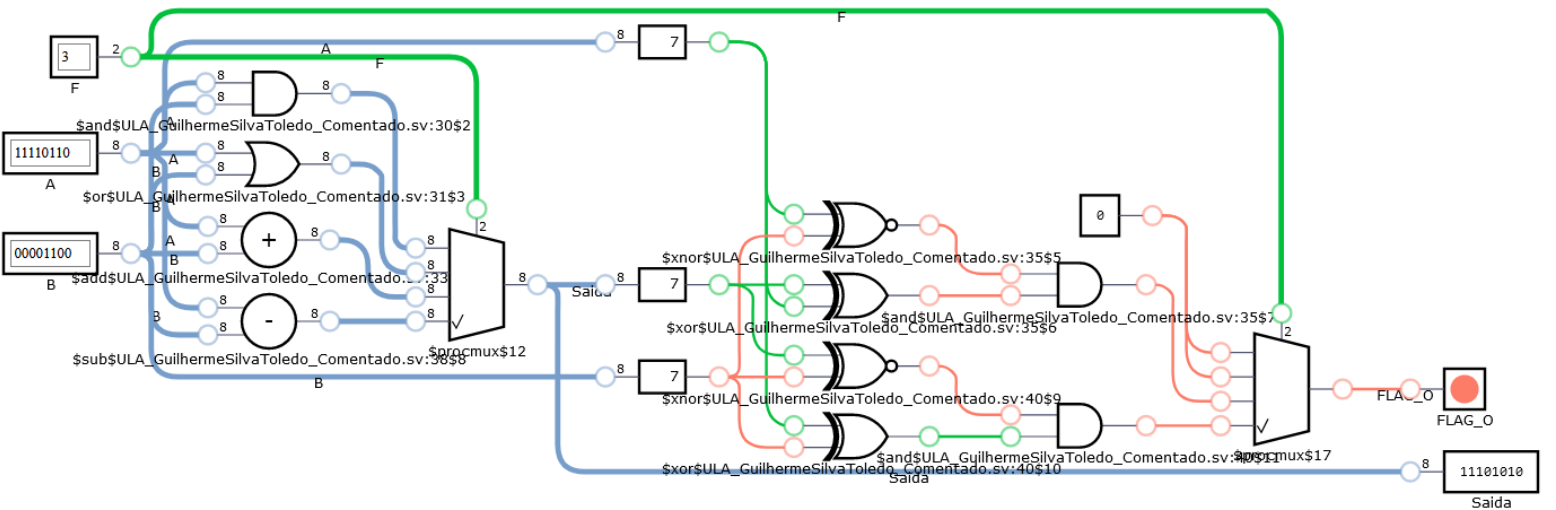
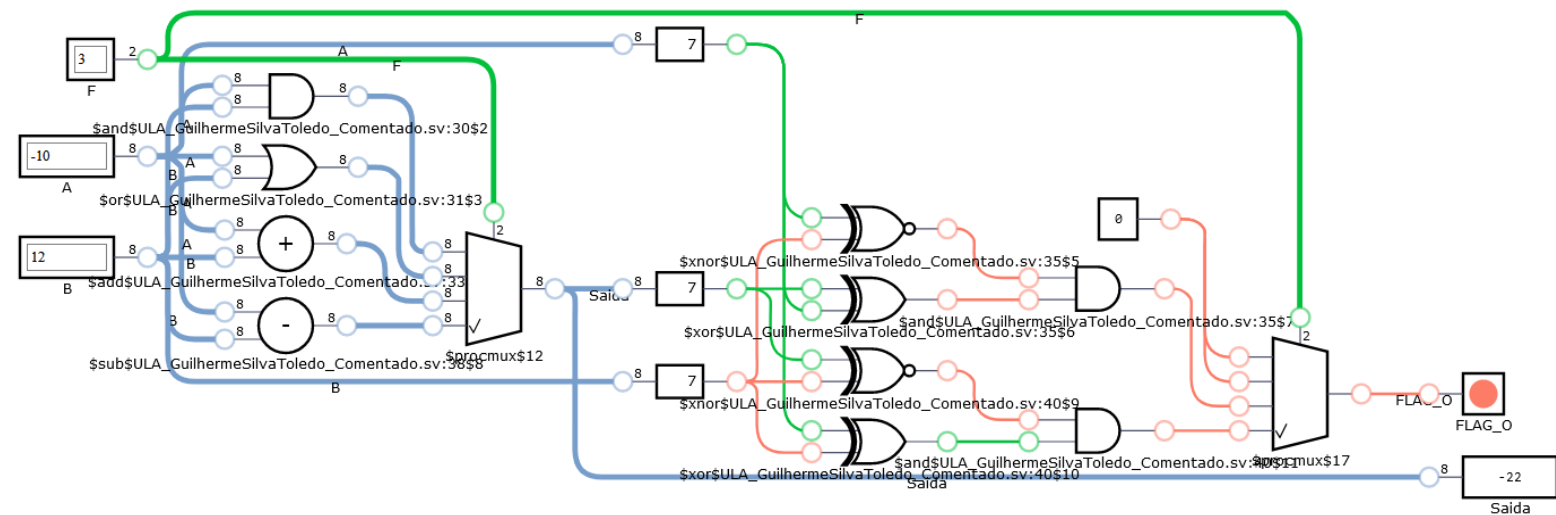




A = -10 e B = 12: AND, OR, SOMA & SUBTRAÇÃO. RESPECTIVAMENTE







A = 127 e B = 2: AND, OR, SOMA & SUBTRAÇÃO. RESPECTIVAMENTE

