Program File List

Name	Number	Type	Rungs	Debug	Bytes
[SYSTEM]	0	SYS	0	No	0
	1	SYS	0	No	0
MAIN_PROG	2	LADDER	7	No	71
UTILITY	3	LADDER	10	No	294
INSPECTION	4	LADDER	19	No	841
IO_COUNTER	5	LADDER	12	No	273
REJ TIMERS	9	LADDER	235	No	10613
1MS_SCAN	10	LADDER	1	No	3
HSC0	11	LADDER	4	No	67
EII_COUNTS	12	LADDER	1	No	3
STI_SPEED	13	LADDER	6	No	115

TensorVisionZ
==========
New MicroLogix1100 Master Program
Timed or with Encoder
==========

PLC IO:
If using encoder: I1.0/00 - 03 = HSC INPUT (from Encoder)
Otherwise

I:0/0 = Encoder Pulse	O:0/0 = Rejector Output (pulse duration via timer)
I:0/1 = Inspect Trigger	O:0/1 = Linestop Output
I:0/2 = Reject Trigger	O:0/2 = Red Lamp
I:0/3 = Reject Confirm	O:0/3 = Green Lamp
I:0/4 = Pass1	O:0/4 = Power Cycle Cameras
I:0/5 = Fail1A	O:0/5 = not used
I:0/6 = Fail1B	O:0/6 = not used
I:0/7 = Pass2	O:0/7 = not used
I:0/8 = Fail2A	
i:0/9 = Fail2B	

PLC Registers accessed by C#-based operator GUI/HMI
COMMENT IS OUT OF DATE (UPDATE!)
- B13:0/0 = Heartbeat indication. from GUI (not implemented)
- B13:0/1 = Heartbeat indication. to GUI
- B13:0/2 = Rejection Mode ON/OFF command. from GUI
- B13:0/3 = Red Lamp Test Command. from GUI; oneshot
- B13:0/4 = Green Lamp Test Command. from GUI; oneshot
- B13:0/5 = Reject Pusher Solenoid Test Command. from GUI; oneshot
- B13:0/6 = Linestop Test Command. from GUI; oneshot; simulates Linestop Active Command for 5s
- B13:0/7 = Linestop Active Command, from GUI
- B13:0/10 = Use Reject Trigger, setting. from GUI (not implemented in this version, as of 2023-07-07)
- B13:0/11 = Use Encoder-based location model, from GUI; if 0, use timing to model movement of cans along conveyor
- B13:0/12 = Reset Counter Command, from GUI; oneshot
- B13:0/15 = Reject Can Now Command, to GUI; 1 => encoder -based model detects failed can is at pusher location
- N17:0 = High Speed Reject Offset, from GUI
- N17:1 = Low Speed Reject Offset, from GUI !!!!!value must be larger than High Speed Reject Offset!!!!!!???is that still true???
- N17:2 = Actual Offset, to GUI; Calculated in PLC based on line speed)
- N17:5 = Rejection Pulse Duration (in milliseconds), from GUI
- N7:11 = Encoder Hi Preset, from GUI; number of encoder counts that triggers the High-Speed Counter interrupt to call routine HSC0
- F18:* = Counters' values, to GUI
- C5:*.ACC = Counters' values, to GUI
- C15:*.ACC = Counters' values, to GUI
- ST19:* = Version and other information as strings, to GUI

comment anchor

0000

Heartbeat: S:4/12 is bit 12 of 16-bit 10kHz Free-Running Clock
in the PLC, so it cycles between 0 and 1 with a period of 819.2ms

0001

Time Base
S:4
12

HEARTBEAT_TO_GUI
B13:0
1

Enable the High-Speed Counter Function whenever commanded, by the operator GUI/HMI, to use an encoder

0002

Use encoder inputs
on I:0/0
USE_ENCODER
B13:0
11

Inspection Code
Bitshift
HSC:0
FE

On each continuous scan cycle, call each of the three main routines: UTILITY; INSPECTION; I/O COUNTERS
- The INSPECTION routine will call the REJ TIMERS routine, if the use of the encoder is not enabled
- The 1MS_SCAN and EII_COUNTS routines are obsolete, empty, and never called

Two other routines will be called asynchronously:
- HSC0: called by High-Speed Counter Interrupt each time the HSC:0 count of encoder pulses reaches its high preset and resets, if enabled (see Rung 0002 above)
- STI_SPEED called by Selectable Timed Interrupt (STI) every 300ms

N.B. the HSC0 routine has the highest priority and will interrupt and suspend any other routine;
the STI_SPEED routine has the next highest priority and will interrupt and suspend the scan cycle routines
the scan cycle routines has the lowest priority and can be interrupted and suspended at any time by the other routines

0003

Utility Code
JSR
Jump To Subroutine
SBR File Number U:3

0004

Inspection Code
JSR
Jump To Subroutine
SBR File Number U:4

0005

Input Counters
JSR
Jump To Subroutine
SBR File Number U:5

0006

END

This Program File routine, LAD 3 UTILITY, is unconditionally called from the main routine (LAD 2 MAIN_PROG) once per continuous scan cycle

- Respond to test command bits (see below)
- Respond to internal SIM_REJECT bit
- Clamp the actual offset value, then load it as a timer preset
- Enforce a lower limit of 500ms for the preset of a timer that does nothing

==========

Rungs 000-0003: respond to test command bits (see below)

Timers' /TT bits ar used as pulse stretchers for test commnand bits to test pieces of the system: green lamp; red lamp; line stop; reject pusher solenoid.

N.B. the test bits are from the operator GUI/HMI, which uses the Set-and-Forget pattern i.e. the GUI wrties a 1 ("Set") as the value of the bit on this PLC, and then "Forgets" about it, The PLC detects the bit value is 1 and in response does two things: (i) resets the bit value to 0 so it can detect the next time the value becomes 1 on a future scan cycle; (ii) "stretches" the command by starting a Timer ON-delay (TON), the /TT bit of which will drive the commanded action and have a value of 1 for some duration.

0000

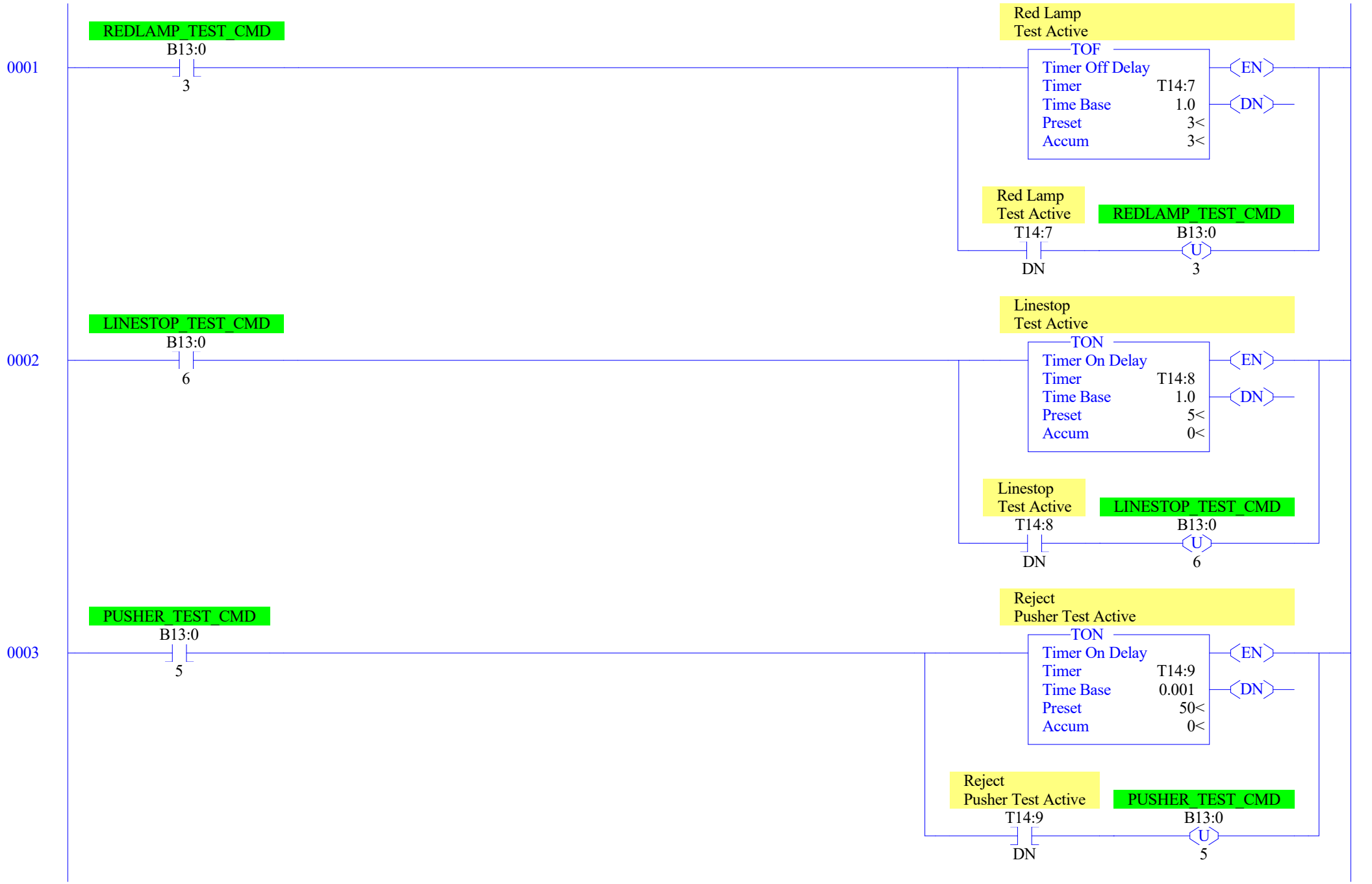
GREENLAMP_TEST_CMD
B13:0
4

Green Lamp Test Active

TOF
Timer Off Delay
Timer T14:6
Time Base 1.0
Preset 3<
Accum 3<
EN
DN

Green Lamp Test Active
T14:6
DN

GREENLAMP_TEST_CMD
B13:0
U
4


0001
REDLAMP_TEST_CMD
B13:0
3
Red Lamp
Test Active
TOF
Timer Off Delay
Timer T14:7
Time Base 1.0
Preset 3<
Accum 3<
EN
DN
Red Lamp
Test Active
T14:7
DN
REDLAMP_TEST_CMD
B13:0
U
3
0002
LINESTOP_TEST_CMD
B13:0
6
Linestop
Test Active
TON
Timer On Delay
Timer T14:8
Time Base 1.0
Preset 5<
Accum 0<
EN
DN
Linestop
Test Active
T14:8
DN
LINESTOP_TEST_CMD
B13:0
U
6
0003
PUSHER_TEST_CMD
B13:0
5
Reject
Pusher Test Active
TON
Timer On Delay
Timer T14:9
Time Base 0.001
Preset 50<
Accum 0<
EN
DN
Reject
Pusher Test Active
T14:9
DN
PUSHER_TEST_CMD
B13:0
U
5

Respond to internal SIM_REJECT bit, which selects the value to use for the reject pusher solenoid duration

0004

SIM_REJECT
B3:0
11

Reject
Pusher Test Active

MOV
Move
Source N17:5
55<
Dest T14:9.PRE
50<

SIM_REJECT
B3:0
11

Reject
Pusher Test Active

MOV
Move
Source 50
50<
Dest T14:9.PRE
50<

Clamp the actual offset value, then load it as a timer preset

TODO: determine if these rungs are unnecessary, as routine LAD 4 INSPECTION, Rung 8 may overwrite the actual offset value in ACTUAL_OFFSET_CALCD N17:2 with the rejector (reject pusher) duration

0005

ACTUAL_OFFSET_CALCD

GRT
Greater Than (A>B)
Source A N17:2
0<
Source B 32000
32000<

ACTUAL_OFFSET_CALCD

MOV
Move
Source 32000
32000<
Dest N17:2
0<

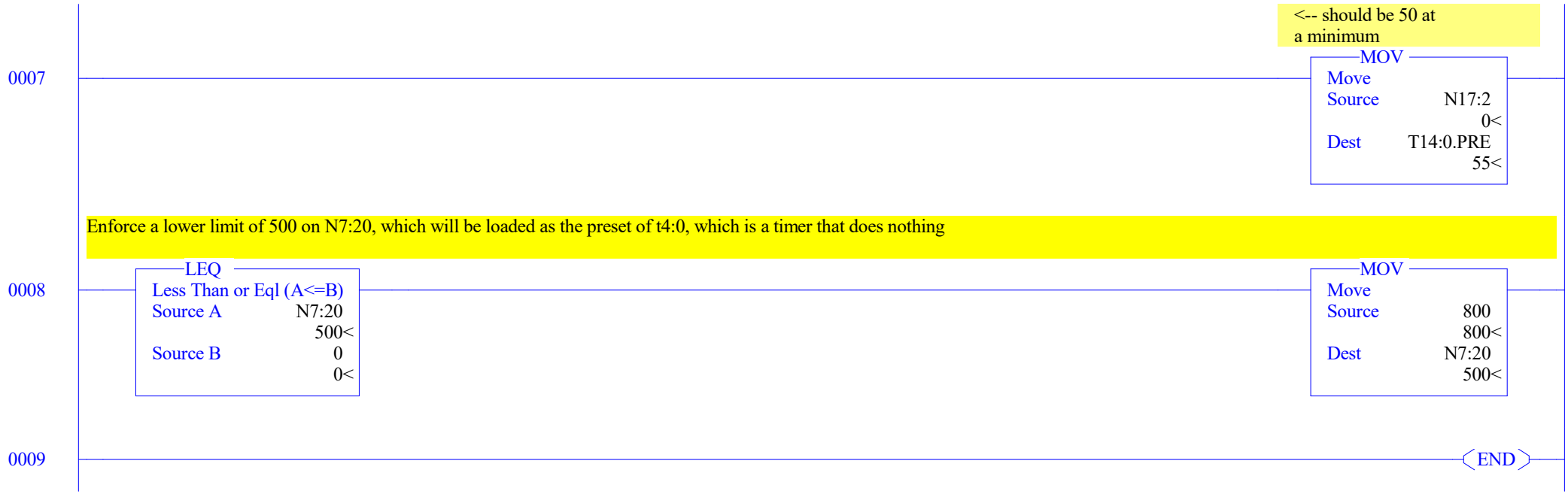
0006

ACTUAL_OFFSET_CALCD

LES
Less Than (A<B)
Source A N17:2
0<
Source B 0
0<

ACTUAL_OFFSET_CALCD

MOV
Move
Source 0
0<
Dest N17:2
0<


<-- should be 50 at
a minimum
0007
MOV
Move
Source N17:2
0<
Dest T14:0.PRE
55<
Enforce a lower limit of 500 on N7:20, which will be loaded as the preset of t4:0, which is a timer that does nothing
0008
LEQ
Less Than or Eql (A<=B)
Source A N7:20
500<
Source B 0
0<
MOV
Move
Source 800
800<
Dest N7:20
500<
0009
END

Can inspection logic - control output per camera and operator HMI/GUI inputs

This Program File routine, LAD 4 INSPECTION is unconditionally called from the main routine (LAD 2 MAIN_PROG) once per continuous scan cycle

==========

Rung 0000: Not sure what to do with USE_REJECT_TRIGGER yet

These bits USE_REJECT_TRIGGER (B12:0/10; from HMI/GUI) and INSPECTING (B13:5/1) are not used anywhere else in this program as of 2023-07-07.

0000

Wait for REJECT_TRIGGER to REJECT

USE_REJECT_TRIGGER
B13:0
10

INSPECTING
B13:5
1

0001

Use encoder inputs on I:0/0

USE_ENCODER
B13:0
11

BitShift Left 1 Control Register

MOV
Move
Source 2000
2000<
Dest R16:0.LEN
2000<

Update High-Speed Counter presets, if encoder is to be used and a new preset (ENCODER_HIPRESET_SP) has been provided by the operator GUI/HMI.

N.B. evaluating/executing the HSL instruction and transitioning /SP bit from 0 to 1 may be redundant

0002

Use encoder inputs on I:0/0

USE_ENCODER
B13:0
11

ENCODER_HIPRESET_SP

NEQ
Not Equal
Source A N17:11 30<
Source B HSC:0.HIP 30<

HSL
High Speed Counter Load
HSC Number HSC0
High Preset N17:11
Low Preset N17:11
Output High Source 0
Output Low Source 0

Inspection Code Bitshift
HSC:0
SP

Use encoder inputs
on I:0/0

0003

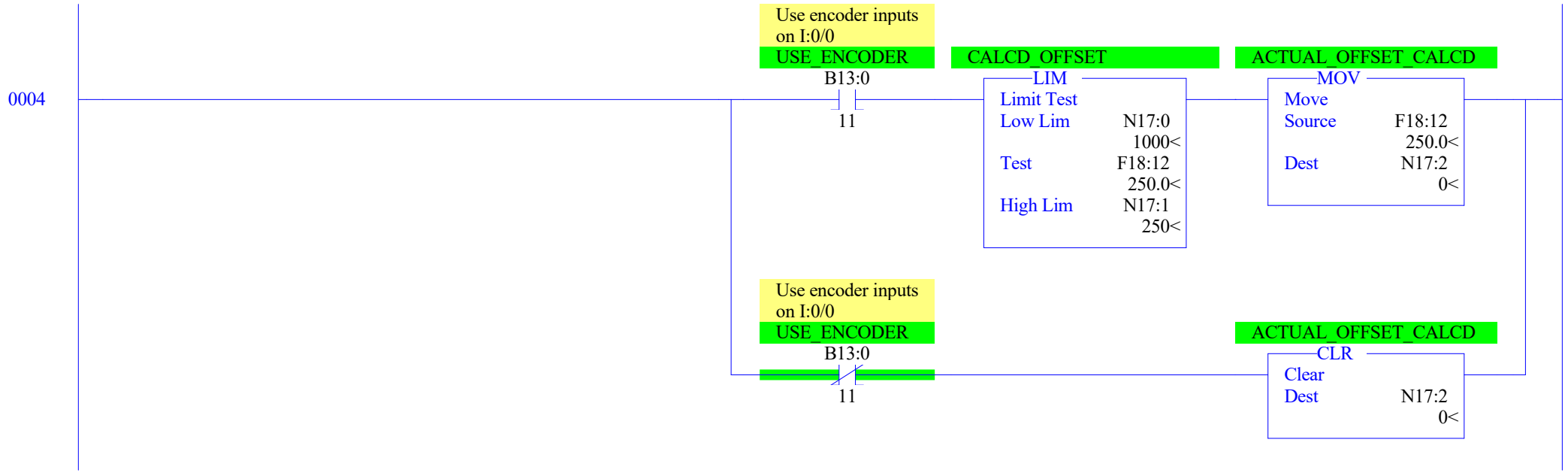
USE_ENCODER
B13:0
11

REG1
DIV
Divide
Source A F18:10 0.0<
Source B F18:18 710.0<
Dest F18:31 0.0<

REG2
SUB
Subtract
Source A N17:1 250<
Source B N17:0 1000<
Dest F18:32 -750.0<

REG3
MUL
Multiply
Source A F18:32 -750.0<
Source B F18:31 0.0<
Dest F18:33 0.0<

CALCD_OFFSET
SUB
Subtract
Source A N17:1 250<
Source B F18:33 0.0<
Dest F18:12 250.0<


0004
Use encoder inputs on I:0/0
USE_ENCODER
B13:0
11
CALCD_OFFSET
LIM
Limit Test
Low Lim N17:0 1000<
Test F18:12 250.0<
High Lim N17:1 250<
ACTUAL_OFFSET_CALCD
MOV
Move
Source F18:12 250.0<
Dest N17:2 0<
Use encoder inputs on I:0/0
USE_ENCODER
B13:0
11
ACTUAL_OFFSET_CALCD
CLR
Clear
Dest N17:2 0<

This subroutine fires each time HSC0 accumulated counts meets the HI or LO preset. Since we do not care (and should never get a LO, this logic executes a bitshift. If the bits are shifted too much, increas the HI preset. It is suggested that we get close to 10 shifts per can, the better "resolution" the better the kickout accuracy. Please remember that varied latency in the assignment of the PASS or FAIL result may place this status in inconsistent locations of the bitshift so resolution must be adequate for that but not too fine as to be shift intensive.

0005

FAIL_1A input-causes REJECT
FAIL_1A
I:0
5
Bul.1763

FAIL_1B input-causes REJECT
FAIL_1B
I:0
6
Bul.1763

FAIL_2A input-causes REJECT
FAIL_2A
I:0
8
Bul.1763

FAIL_2B input-causes REJECT
FAIL_2B
I:0
9
Bul.1763

A_ONESHOT0
B13:2
ONS
0

Bitshift 1

MVM
Masked Move
Source N7:10
1<
Mask N7:11
0003h<
Dest B11:0
0000000000000001<

Rejection Logic

The bitshift conveys the fail status from the point of origin each time the HSC Hi Preset is reached. The REJECT output should fire at a point in the future as assigned by the value of N17:5 which is changeable in the data table. Once this REJECT signal is set, it should be tied to the actual output to trigger the reject actuator then this bit should be reset once kickout has fired.

0006

Use encoder inputs on I:0/0
USE_ENCODER
B13:0
11

Bitshift 1
B11:0/[ACTUAL_OFFSET_CALCD]
B11:0
[N17:2]

A_ONESHOT1
B13:2
ONS
1

Force a Reject (timing=?)
REJECT_NOW_CMD
B13:0
L
15

Use the time-based model of the cans' locations if the encoder pulses are being ignored.

0007

Use encoder inputs on I:0/0
USE_ENCODER
B13:0
11

REJECTION TIMERS
JSR
Jump To Subroutine
SBR File Number U:9

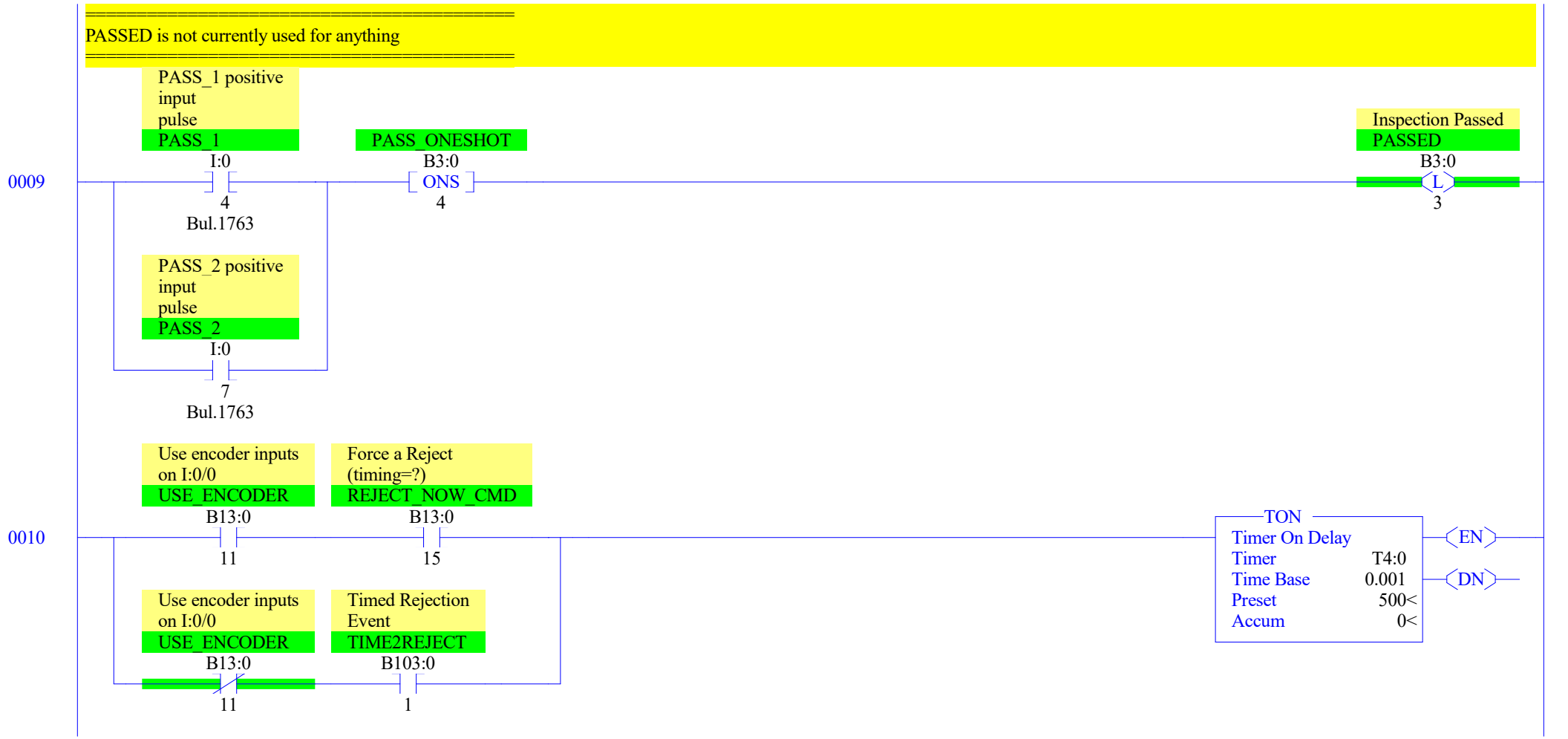
0008

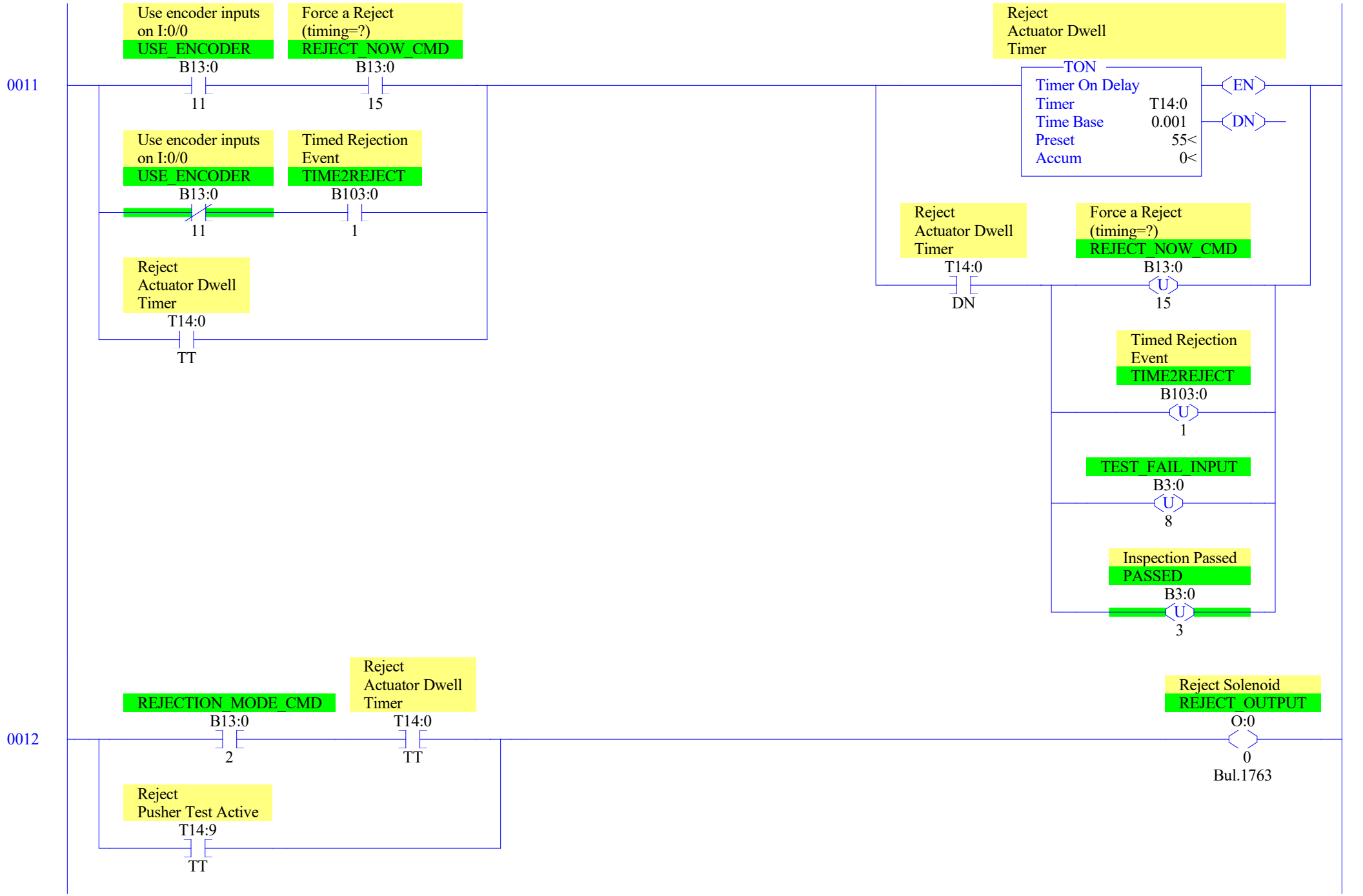
REJECTOR_DURATION_SP
LIM
Limit Test
Low Lim 0
0<
Test N17:5
55<
High Lim 1000
1000<

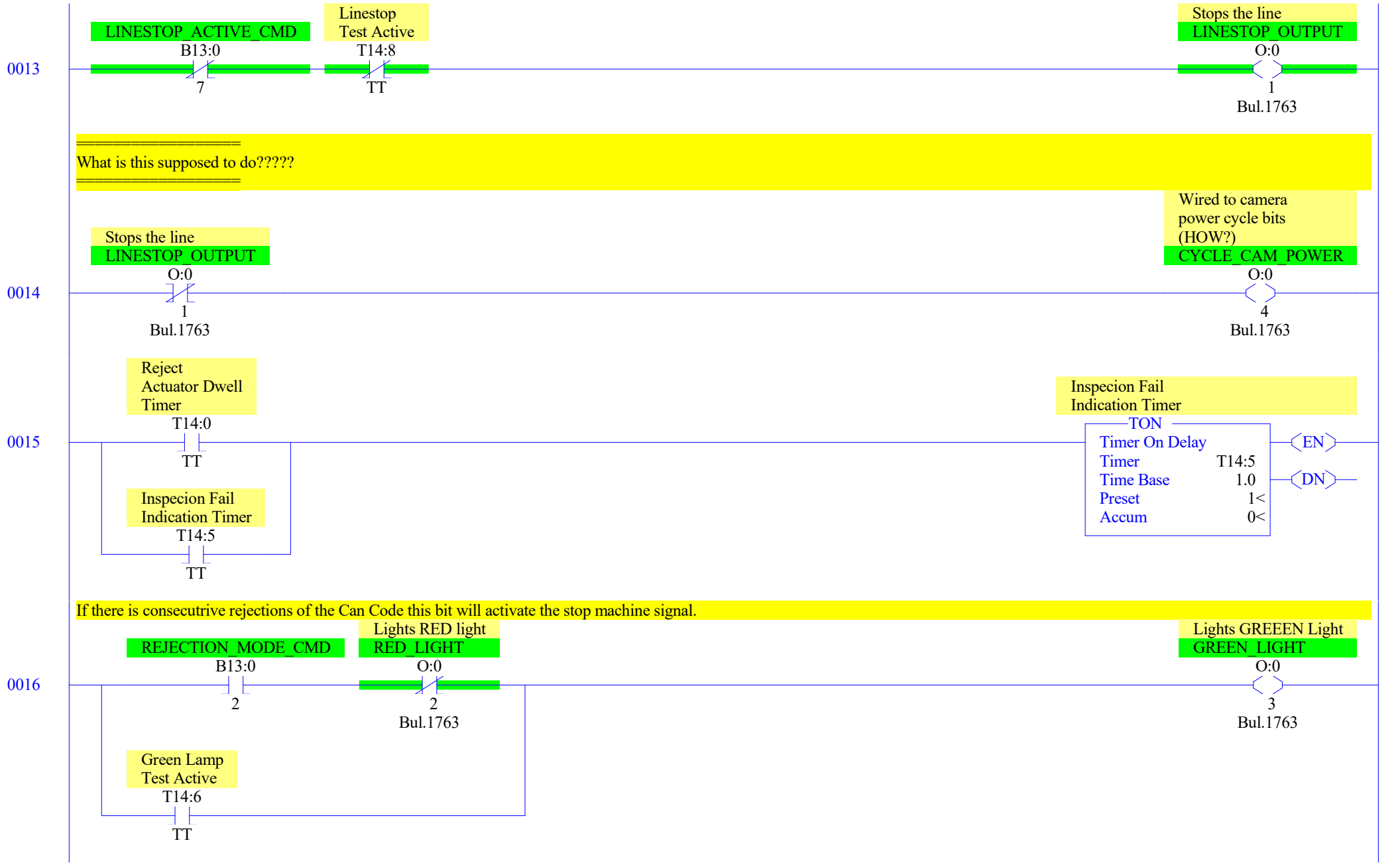
REJECTOR_DURATION_SP
NEQ
Not Equal
Source A N17:5
55<
Source B T14:0.PRE
55<

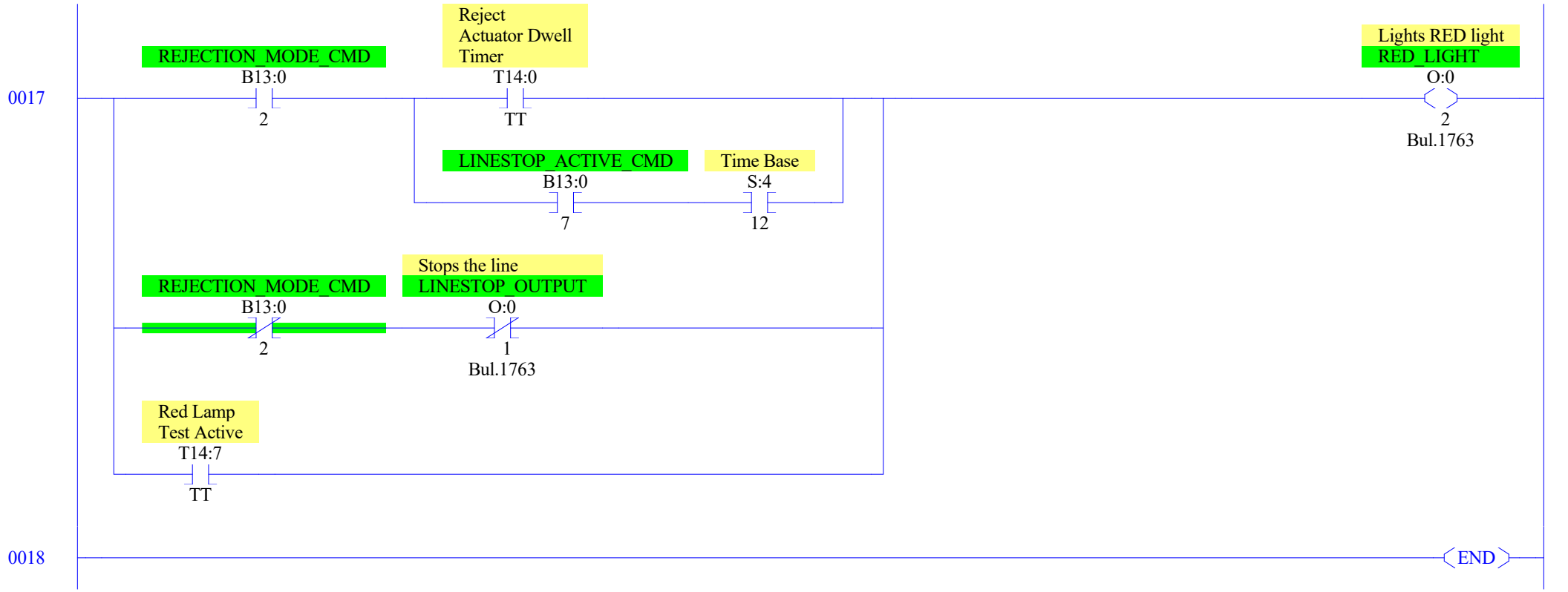
<-- should be 50 at a minimum
MOV
Move
Source N17:5
55<
Dest T14:0.PRE
55<

MOV
Move
Source N7:20
500<
Dest T4:0.PRE
500<


PASSED is not currently used for anything
PASS_1 positive input pulse
PASS_1
I:0
4
Bul.1763
PASS_ONESHOT
B3:0
ONS
4
Inspection Passed
PASSED
B3:0
L
3
0009
PASS_2 positive input pulse
PASS_2
I:0
7
Bul.1763
Use encoder inputs on I:0/0
USE_ENCODER
B13:0
11
Force a Reject (timing=?)
REJECT_NOW_CMD
B13:0
15
0010
TON
Timer On Delay
Timer T4:0
Time Base 0.001
Preset 500<
Accum 0<
EN
DN
Use encoder inputs on I:0/0
USE_ENCODER
B13:0
11
Timed Rejection Event
TIME2REJECT
B103:0
1


0011
Use encoder inputs on I:0/0
USE_ENCODER
B13:0
11
Force a Reject (timing=?)
REJECT_NOW_CMD
B13:0
15
Use encoder inputs on I:0/0
USE_ENCODER
B13:0
11
Timed Rejection Event
TIME2REJECT
B103:0
1
Reject Actuator Dwell Timer
T14:0
TT
Reject Actuator Dwell Timer
TON
Timer On Delay
Timer T14:0
Time Base 0.001
Preset 55<
Accum 0<
EN
DN
Reject Actuator Dwell Timer
T14:0
DN
Force a Reject (timing=?)
REJECT_NOW_CMD
B13:0
U
15
Timed Rejection Event
TIME2REJECT
B103:0
U
1
TEST_FAIL_INPUT
B3:0
U
8
Inspection Passed
PASSED
B3:0
U
3
0012
REJECTION_MODE_CMD
B13:0
2
Reject Actuator Dwell Timer
T14:0
TT
Reject Pusher Test Active
T14:9
TT
Reject Solenoid
REJECT_OUTPUT
O:0
0
Bul.1763


0013
LINESTOP_ACTIVE_CMD
B13:0
7
Linestop
Test Active
T14:8
TT
Stops the line
LINESTOP_OUTPUT
O:0
1
Bul.1763
What is this supposed to do?????
0014
Stops the line
LINESTOP_OUTPUT
O:0
1
Bul.1763
Wired to camera
power cycle bits
(HOW?)
CYCLE_CAM_POWER
O:0
4
Bul.1763
0015
Reject
Actuator Dwell
Timer
T14:0
TT
Inspecion Fail
Indication Timer
T14:5
TT
Inspecion Fail
Indication Timer
TON
Timer On Delay
Timer T14:5
Time Base 1.0
Preset 1<
Accum 0<
EN
DN
If there is consecutrive rejections of the Can Code this bit will activate the stop machine signal.
0016
REJECTION_MODE_CMD
B13:0
2
Lights RED light
RED_LIGHT
O:0
2
Bul.1763
Lights GREEEN Light
GREEN_LIGHT
O:0
3
Bul.1763
Green Lamp
Test Active
T14:6
TT


0017
REJECTION_MODE_CMD
B13:0
2
Reject
Actuator Dwell
Timer
T14:0
TT
LINESTOP_ACTIVE_CMD
B13:0
7
Time Base
S:4
12
Lights RED light
RED_LIGHT
O:0
2
Bul.1763
REJECTION_MODE_CMD
B13:0
2
Stops the line
LINESTOP_OUTPUT
O:0
1
Bul.1763
Red Lamp
Test Active
T14:7
TT
0018
END

I/O Counters (and a way to clear them)

0000

Part ready to inspect
INSPECT_TRIGGER
I:0
1
Bul.1763

INSPECT_TRIGGER_CTR
CTU
Count Up
Counter C5:1
Preset 0<
Accum -32737<
CU
DN

0001

Reject Solenoid
REJECT_OUTPUT
O:0
0
Bul.1763

REJECT_OUTPUT_CTR
CTU
Count Up
Counter C5:2
Preset 0<
Accum 348<
CU
DN

0002

If USE_REJECT_TRIGGER, this causes the reject to happen
REJECT_TRIGGER
I:0
2
Bul.1763

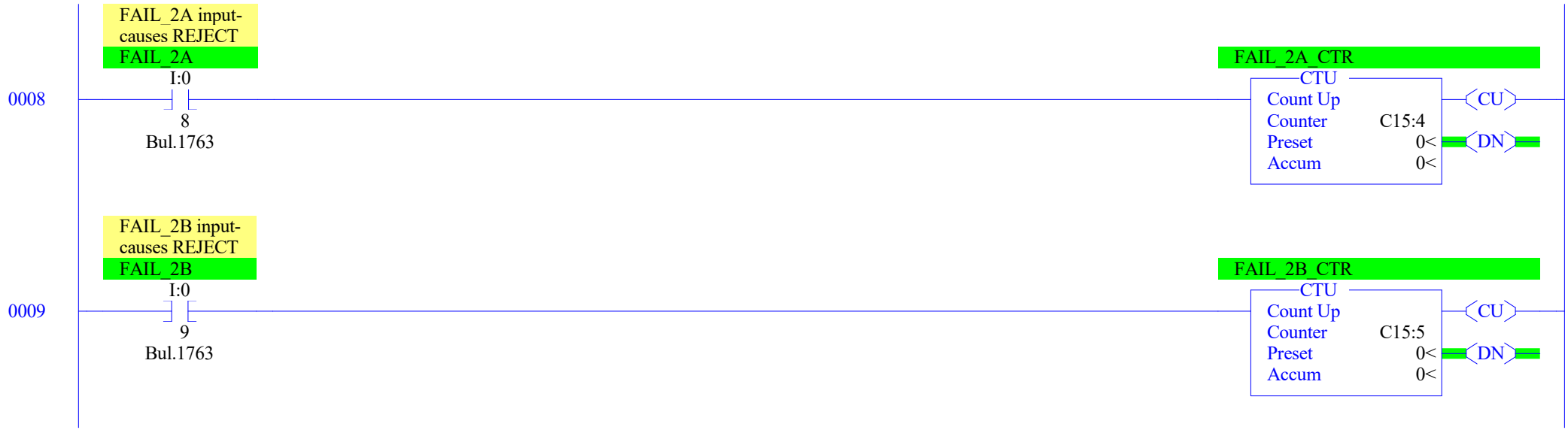
REJECT_TRIGGER_CTR
CTU
Count Up
Counter C5:3
Preset 0<
Accum 0<
CU
DN

0003

Optional reject confirmation sensor
REJECT_CONFIRM
I:0
3
Bul.1763

REJECT_CONFIRM_CTR
CTU
Count Up
Counter C5:4
Preset 0<
Accum 0<
CU
DN


PASS_1 positive input pulse
PASS_1
I:0
4
Bul.1763
0004
PASS_1_CTR
CTU
Count Up
Counter C15:0
Preset 0<
Accum -32756<
CU
DN
FAIL_1A input-causes REJECT
FAIL_1A
I:0
5
Bul.1763
0005
FAIL_1A_CTR
CTU
Count Up
Counter C15:1
Preset 0<
Accum 951<
CU
DN
FAIL_1B input-causes REJECT
FAIL_1B
I:0
6
Bul.1763
0006
FAIL_1B_CTR
CTU
Count Up
Counter C15:2
Preset 0<
Accum 0<
CU
DN
PASS_2 positive input pulse
PASS_2
I:0
7
Bul.1763
0007
PASS_2_CTR
CTU
Count Up
Counter C15:3
Preset 0<
Accum 0<
CU
DN


FAIL_2A input-causes REJECT
FAIL_2A
I:0
8
Bul.1763
0008
FAIL_2A_CTR
CTU
Count Up
Counter C15:4
Preset 0<
Accum 0<
CU
DN
FAIL_2B input-causes REJECT
FAIL_2B
I:0
9
Bul.1763
0009
FAIL_2B_CTR
CTU
Count Up
Counter C15:5
Preset 0<
Accum 0<
CU
DN

The GUI/HMI executes the Set-And-Forget pattern to reset the counters

The RESET_COUNTERS_CMD (B13:0/12) bit is driven by the operator GUI/HMI, which sets its value to 1 and expects this program to detect that, execute the counter resets, and reset the bit value back to 0 so the counter reset is a one-shot event.

N.B. if any of the XICed operands (e.g. FAIL_2B I:0.0/9) feeding the counters are 1 on the scan cycly when the reset is commanded, then those counters .ACC values will immediately increment to 1, if the operand are still 1, on the next scan cycle

0010

Clear all of the counters assigned to the inputs

RESET_COUNTERS_CMD
B13:0
12

INSPECT_TRIGGER_CTR
C5:1
RES

REJECT_OUTPUT_CTR
C5:2
RES

REJECT_TRIGGER_CTR
C5:3
RES

REJECT_CONFIRM_CTR
C5:4
RES

PASS_1_CTR
C15:0
RES

FAIL_1A_CTR
C15:1
RES

FAIL_1B_CTR
C15:2
RES

PASS_2_CTR
C15:3
RES

FAIL_2A_CTR
C15:4
RES

FAIL_2B_CTR
C15:5
RES

Clear all of the
counters assigned to
the inputs
RESET_COUNTERS_CMD
B13:0
U
12

0011

END

Timed reject logic when encoder pulses are being ignored

This Program File routine is executed if the use of the encoder as the clock has been disabled
via the operator GUI/HMI.

Pulses have been accumulating into the value of WORKING_REGISTER by the
High-Speed Counter interrupt routine (LAD11 HSC0).

==========

Calculate combined inspection cameras' failed can signal as any (logical OR) of all possible* failed signals

* Any camera (FAIL_1/2/A/B), when not disabled, or
synthetic test event (TEST_FAIL_INPUT; set-and-forget) from the operator GUI/HMI

- Ensure synthetic test event is a one-shot i.e.is 1 for at most 1 scan cycle

0000

FAIL_1A input-causes REJECT
FAIL_1A
I:0
5
Bul.1763

DISABLE_FAIL
B3:0
10

FAIL_RESULT
B13:5
3

TEST_FAIL_INPUT
B3:0
U
8

FAIL_1B input-causes REJECT
FAIL_1B
I:0
6
Bul.1763

FAIL_2A input-causes REJECT
FAIL_2A
I:0
8
Bul.1763

FAIL_2B input-causes REJECT
FAIL_2B
I:0
9
Bul.1763

TEST_FAIL_INPUT
B3:0
8

Evaluate rising edge, during the current scan cycle, of the combined failed signal (FAIL_RESULT) from the previous rung

- FAIL_OS => FAILed inspection One-Shot

N.B. the [XIO USE_ENCODER] is redundant, because this routine will only be executing if the encoder is being ignored

0001

Use encoder inputs on I:0/0
USE_ENCODER
B13:0
11

FAIL_RESULT
B13:5
3

oneshot
B103:0
ONS
5

Inspection Fail for Timed Logic
FAIL_OS
B103:0
L
0

Clamp Low-speed offset value to a range of [0:32000], since this is an integer

0002

LOSPEED_OFFSET_SP
GRT
Greater Than (A>B)
Source A N17:1 250<
Source B 32000 32000<

LOSPEED_OFFSET_SP
MOV
Move
Source 32000 32000<
Dest N17:1 250<

0003

LOSPEED_OFFSET_SP
LES
Less Than (A<B)
Source A N17:1 250<
Source B 0 0<

LOSPEED_OFFSET_SP
MOV
Move
Source 0 0<
Dest N17:1 250<

Set reject delay timers

The next five rungs of logic cycles thru all 112 timer objects (T104:0 thru T104:111) to update a changed PRESET

N.B. it will take 223 scan cycles to complete the updates to all timer objects

TODO: why are the LIM instruction limits [0:30000] on this rung, when the previous rungs use [0:32000]?

TODO: refactor these 4 rungs and 14 instructions to do the same task more clearly and concisely (half the rungs, instructions, and scan cycles)

0004

NEQ Not Equal — Source A T104:0.PRE 9< — Source B N17:1 250<

LOSPEED_OFFSET_SP

LIM Limit Test — Low Lim 0 0< — Test N17:1 250< — High Lim 30000 30000<

update reject delay timers B3:0 (L) 2

0005

update reject delay timers B3:0 2

oneshot B3:0 ONS 6

LOOP C5:9 (RES)

0006

update reject delay timers B3:0 2

T104:[LOOP.ACC].PRE

MOV Move — Source N17:1 250< — Dest T104:[C5:9.ACC].PRE 250<

0007

update reject delay timers B3:0 2

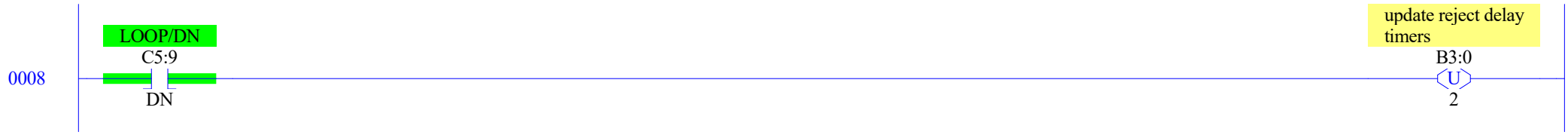
LOOP/CU C5:9 CU

LOOP/DN C5:9 DN

LOOP

CTU Count Up — Counter C5:9 — Preset 112< — Accum 112<

(CU) (DN)


0008
LOOP/DN
C5:9
DN
update reject delay timers
B3:0
U
2

Multiple Overlapping Rejection Timers

Handling a rejected can involves two primary process steps:

1) Detecting when that can fails inspection at the cameras station (see FAIL_OS on Rung 001 above)
2) Triggering the reject pusher solenoid, when the can arrives at the reject station, to eject the can from the conveyor

This program use Timer ON-delay instructions to model the time between steps (1) and (2) above:

- Start a timer when a can fails inspection at the cameras station
- Run the timer as the failed can travels from the cameras station to the reject station
- Activate the reject pusher solenoid when the timer expires as the failed can arrives at the reject station
  - This will be accomplished by latching the TIME2REJECT B102:0/1 bit value to 1

The following code implements that model for one or more failed cans, while all of those cans are simultaneously
- BETWEEN the upstream camera station where they failed inspection,
- AND the downstream reject pusher solenoid where they will be ejected from the conveyor

There are 112 timer objects, T104:0 through T104:111, in the Data File array T104.

There are 112 bits, ...REJECTn, each representing the busy state of one of those timer objects:

- A bit value of 0 means the timer object is not timing a failed can's travel and is available to time a new failed can
- A bit value of 1 means the timer object is timing a failed can's travel and is unavailable to time a new failed can

Each consecutive pair of rungs that follow control the logic for one timer object that can model one failed cans travel
from the camera station to the reject station. E.g. Rungs 0009-0010 control the logic for timer object T104:0.

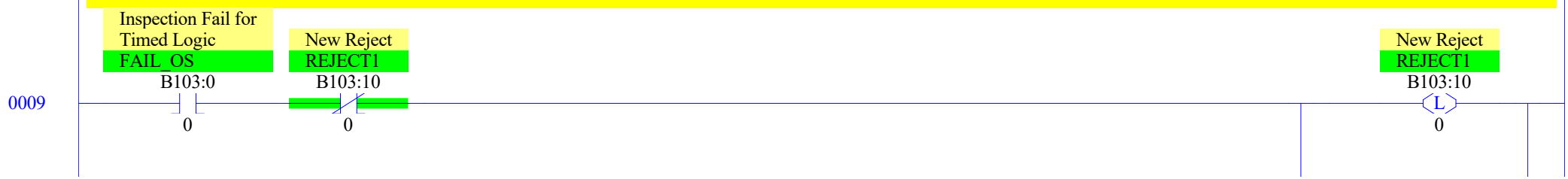
The first rung of each pair tests whether
- BOTH a new failed can still needs to have a timer assigned to it => FAIL_OS bit value is still 1,
- AND if the timer object of the rung pair is not busy => ...REJECTn bit value is 0,

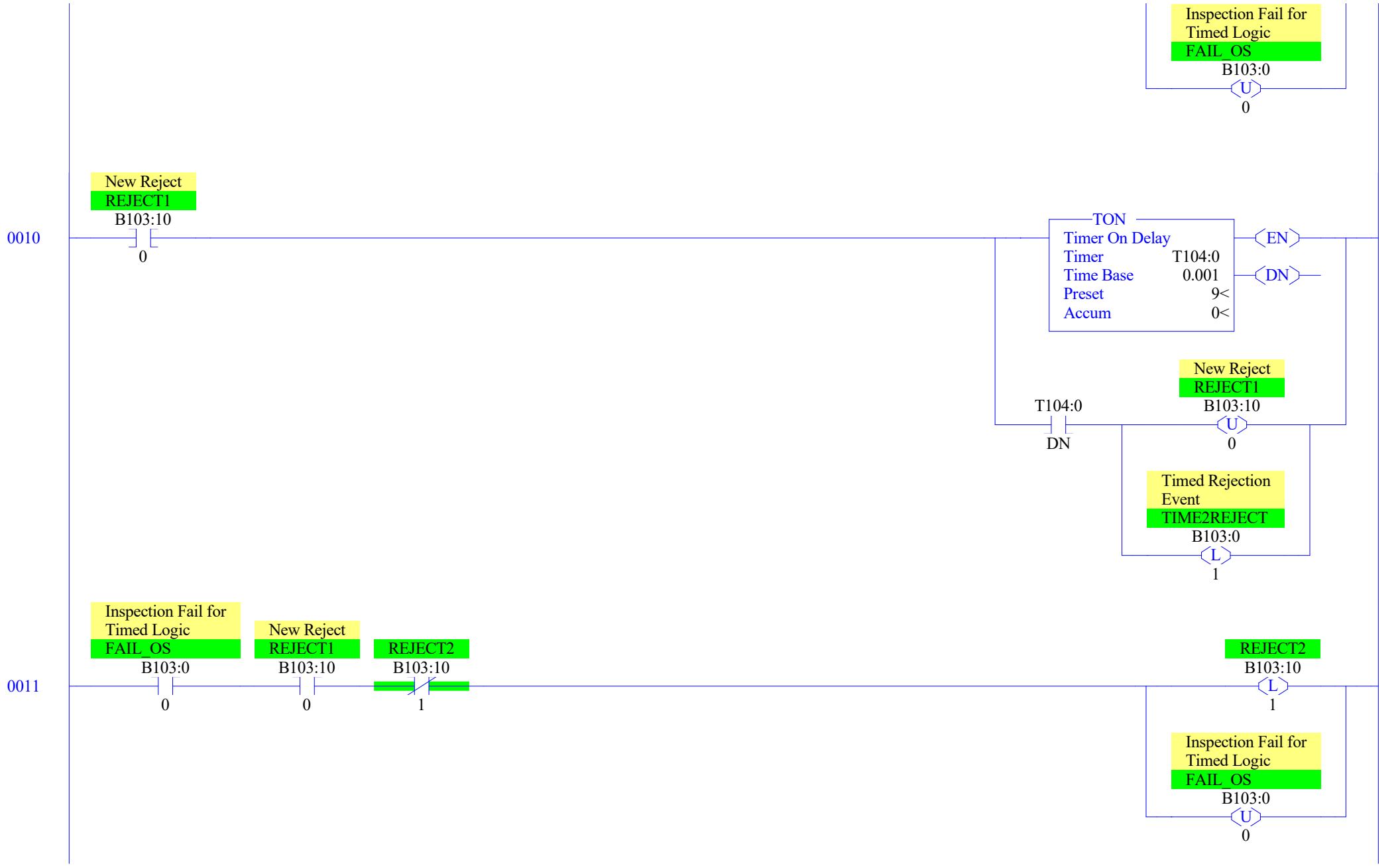
and, if those conditions are both true, then that first rung assigns the timer object the the new failed can by
- Marking the timer object as busy => latch the timer object's ...REJECTn bit value to 1, and
- Canceling the new failed can status => unlatch FAIL_OS value to 0, so no other timer will be assigned to the new failed can

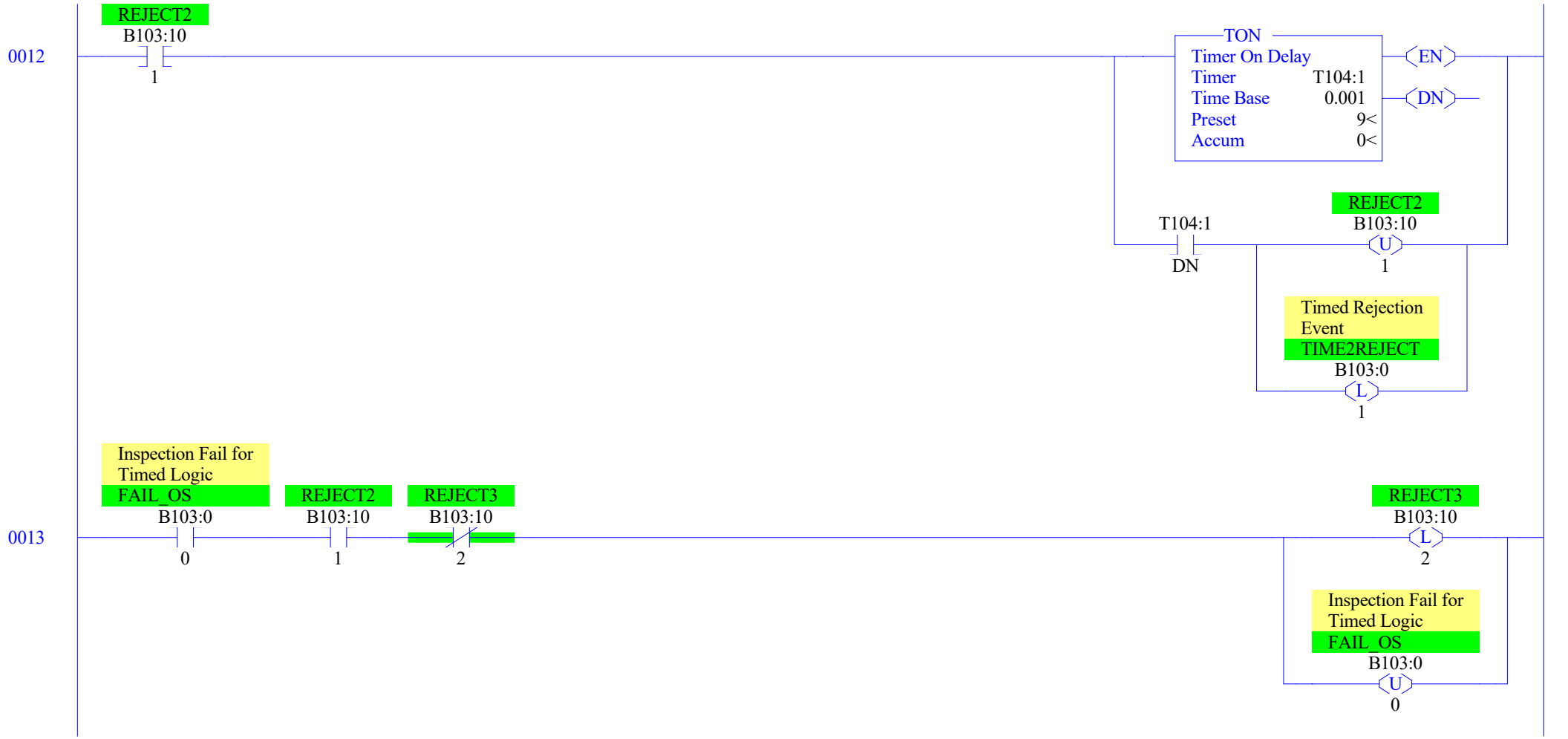
The second rung of each pair controls the TON instruction for the timer object of the rung:
- If the can has not reached the reject station (=> ...REJECTn bit value is 1), then continue running the timer,
- When the can reaches the reject station (timer object /DN bit is 1),
  - Unlatch the timer object ...REJECTn bit value to 0, and
  - Latch the TIME2REJECT bit value to 1, to trigger the reject pusher solenoid in the routine LAD 4 INSPECTION

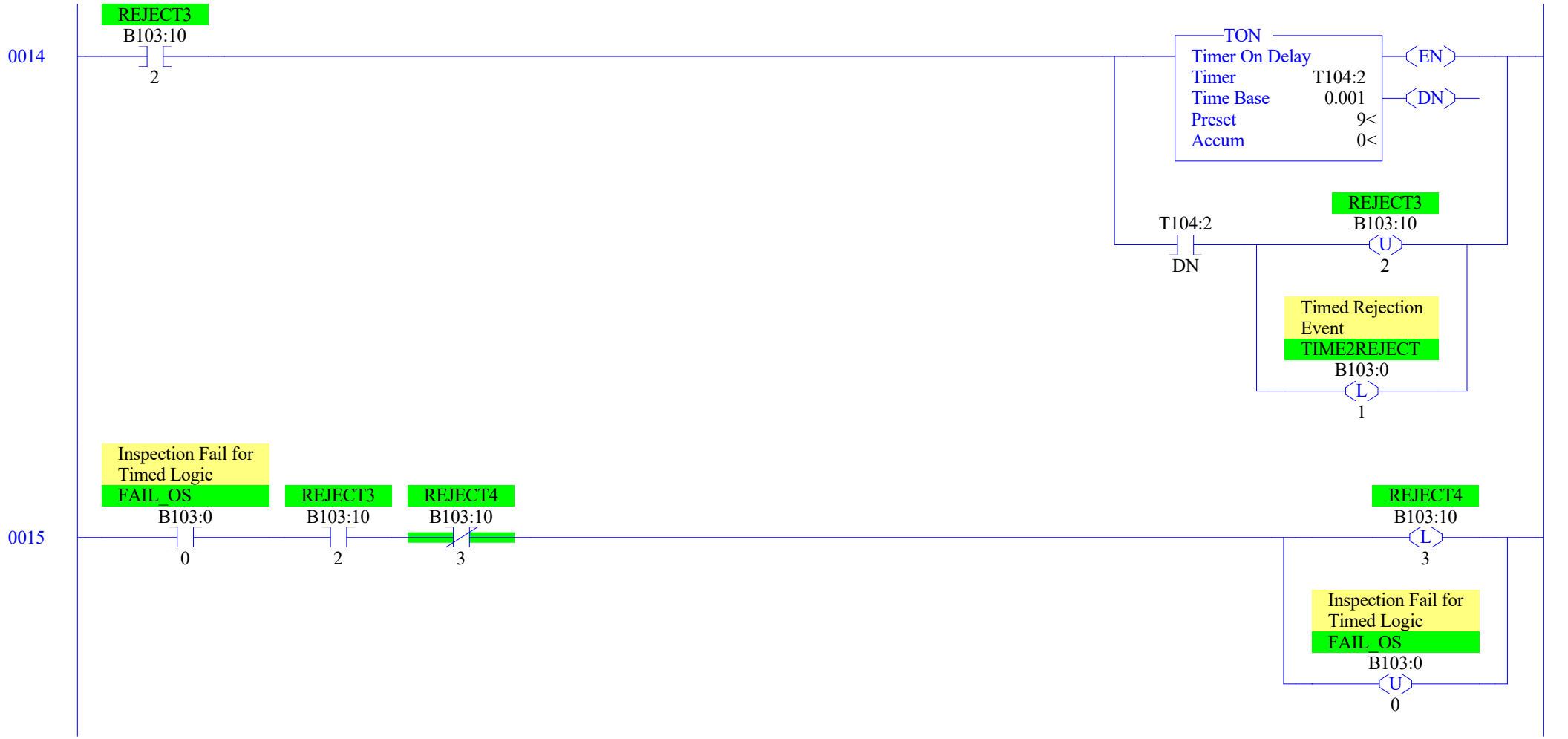
TODO: look into simplifying this logic, e.g. the timer objects' /TT bits could be used instead of the ...REJECTn bits

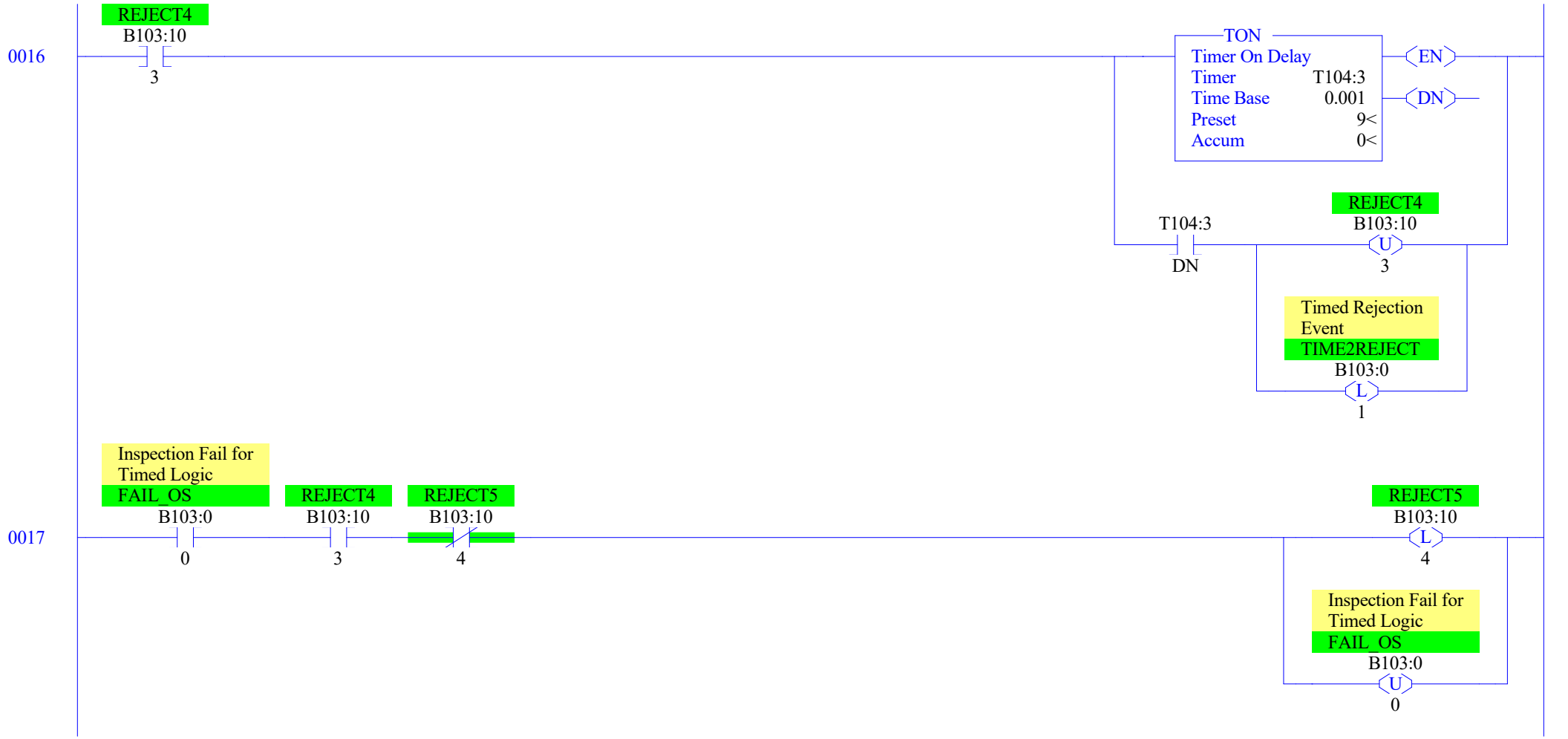
TODO: refactor the second rung of the pair by removing the unnecessary [XIC ...REJECT(n-1)] instructions

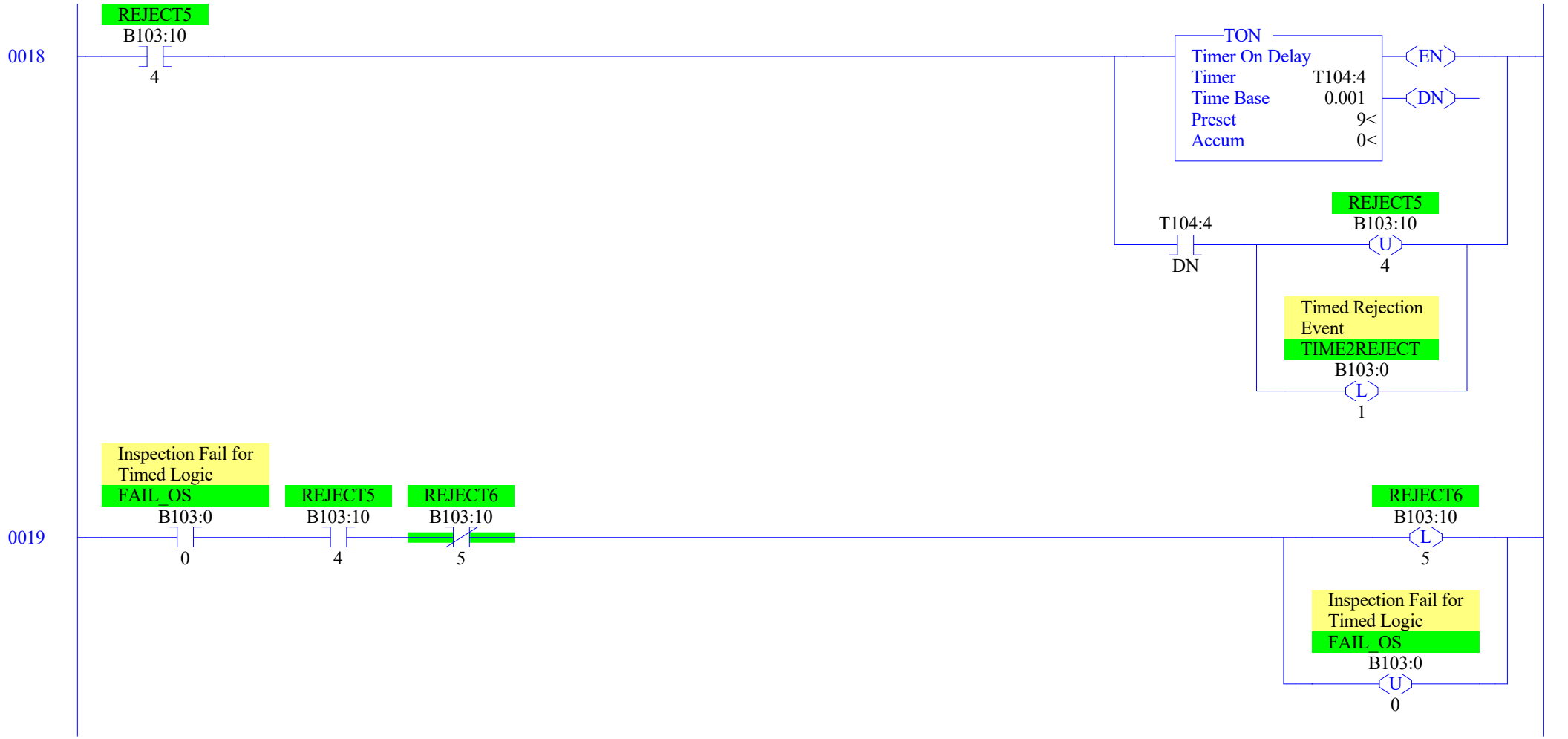


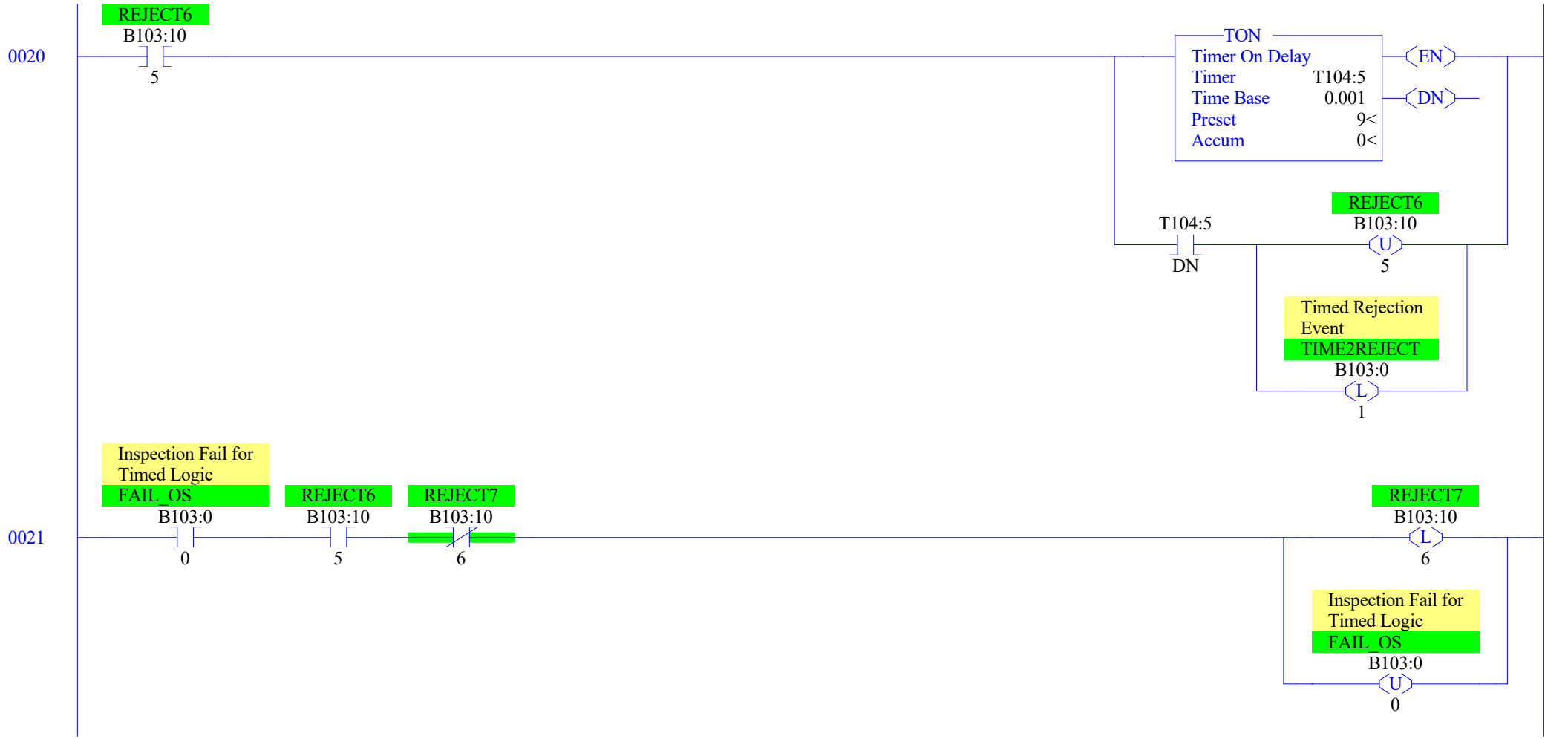

Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0
New Reject
REJECT1
B103:10
0010
0
TON
Timer On Delay
Timer T104:0
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:0
DN
New Reject
REJECT1
B103:10
U
0
Timed Rejection Event
TIME2REJECT
B103:0
L
1
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
New Reject
REJECT1
B103:10
0
REJECT2
B103:10
1
0011
REJECT2
B103:10
L
1
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

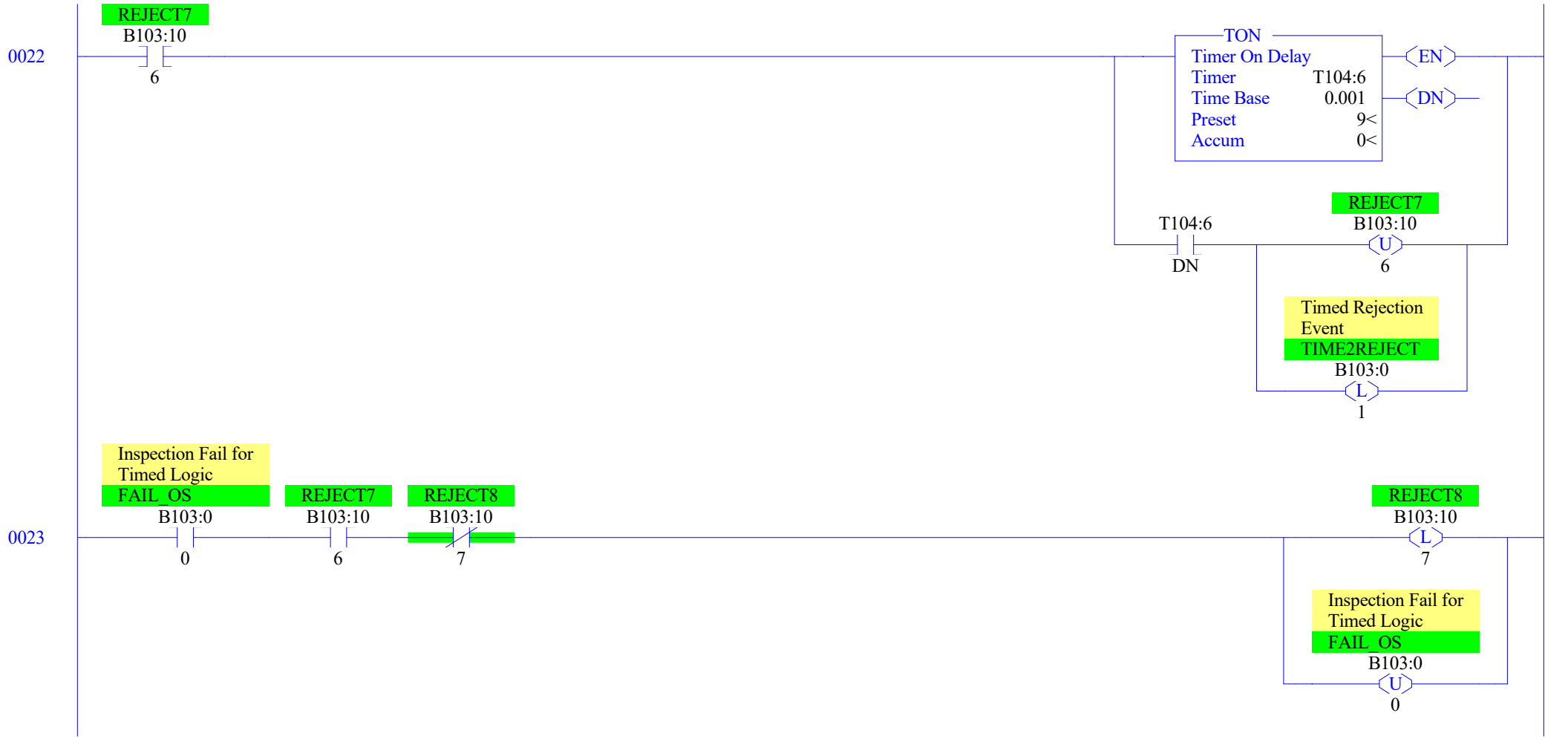

0012
REJECT2
B103:10
1
TON
Timer On Delay
Timer T104:1
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:1
DN
REJECT2
B103:10
U
1
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0013
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
REJECT2
B103:10
1
REJECT3
B103:10
2
REJECT3
B103:10
L
2
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

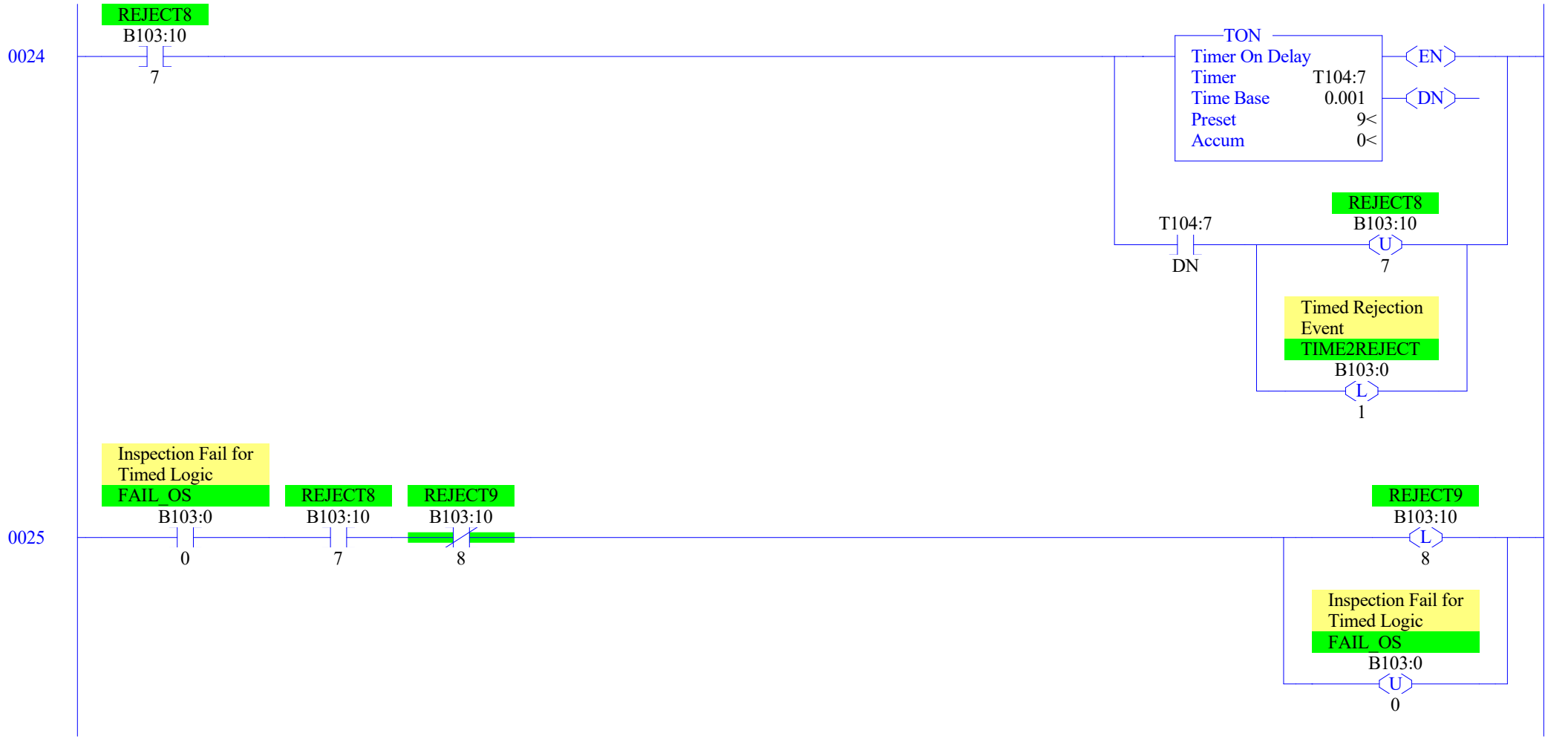

0014
REJECT3
B103:10
2
TON
Timer On Delay
Timer T104:2
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:2
DN
REJECT3
B103:10
U
2
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0015
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
REJECT3
B103:10
2
REJECT4
B103:10
3
REJECT4
B103:10
L
3
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

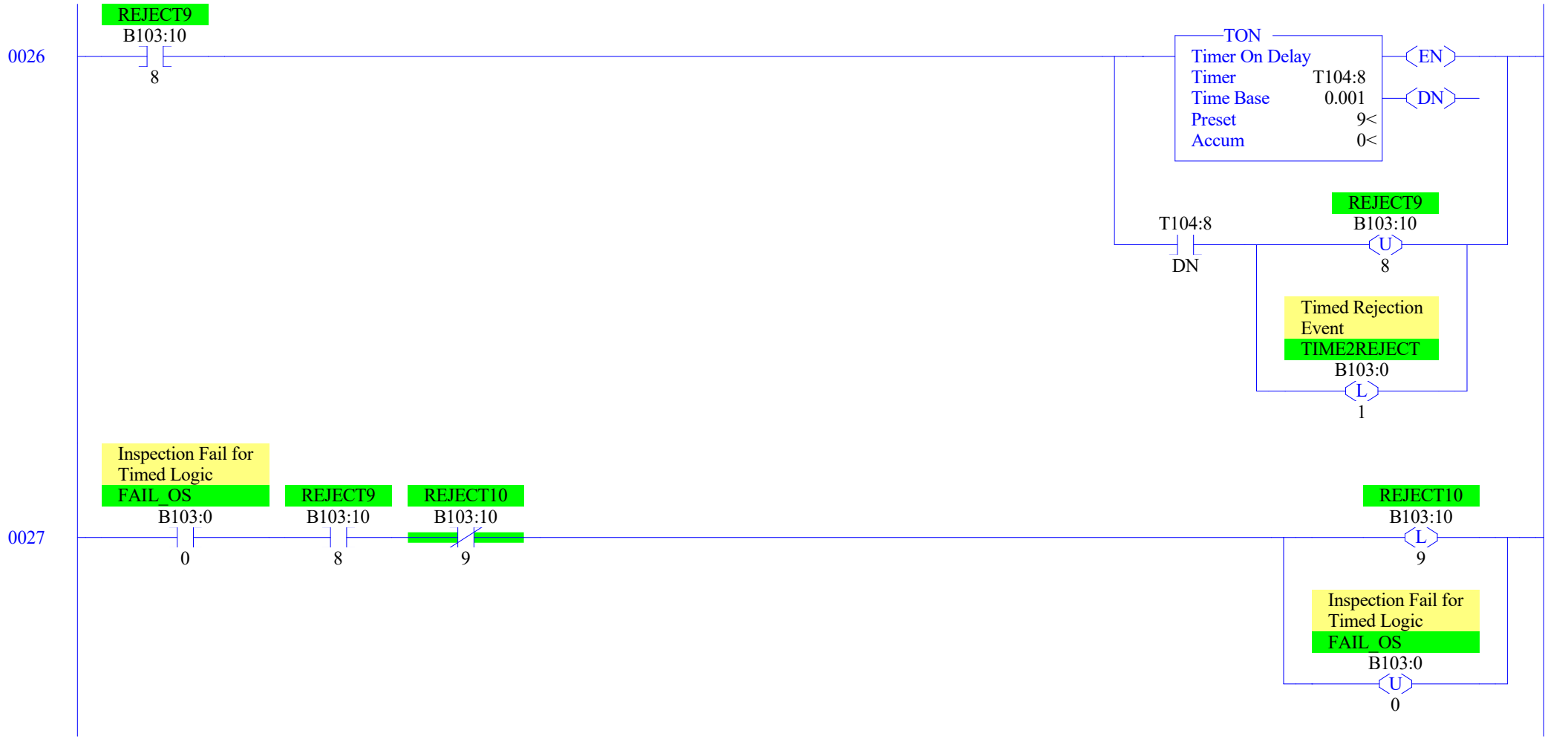

0016
REJECT4
B103:10
3
TON
Timer On Delay
Timer T104:3
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:3
DN
REJECT4
B103:10
U
3
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0017
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
REJECT4
B103:10
3
REJECT5
B103:10
4
REJECT5
B103:10
L
4
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

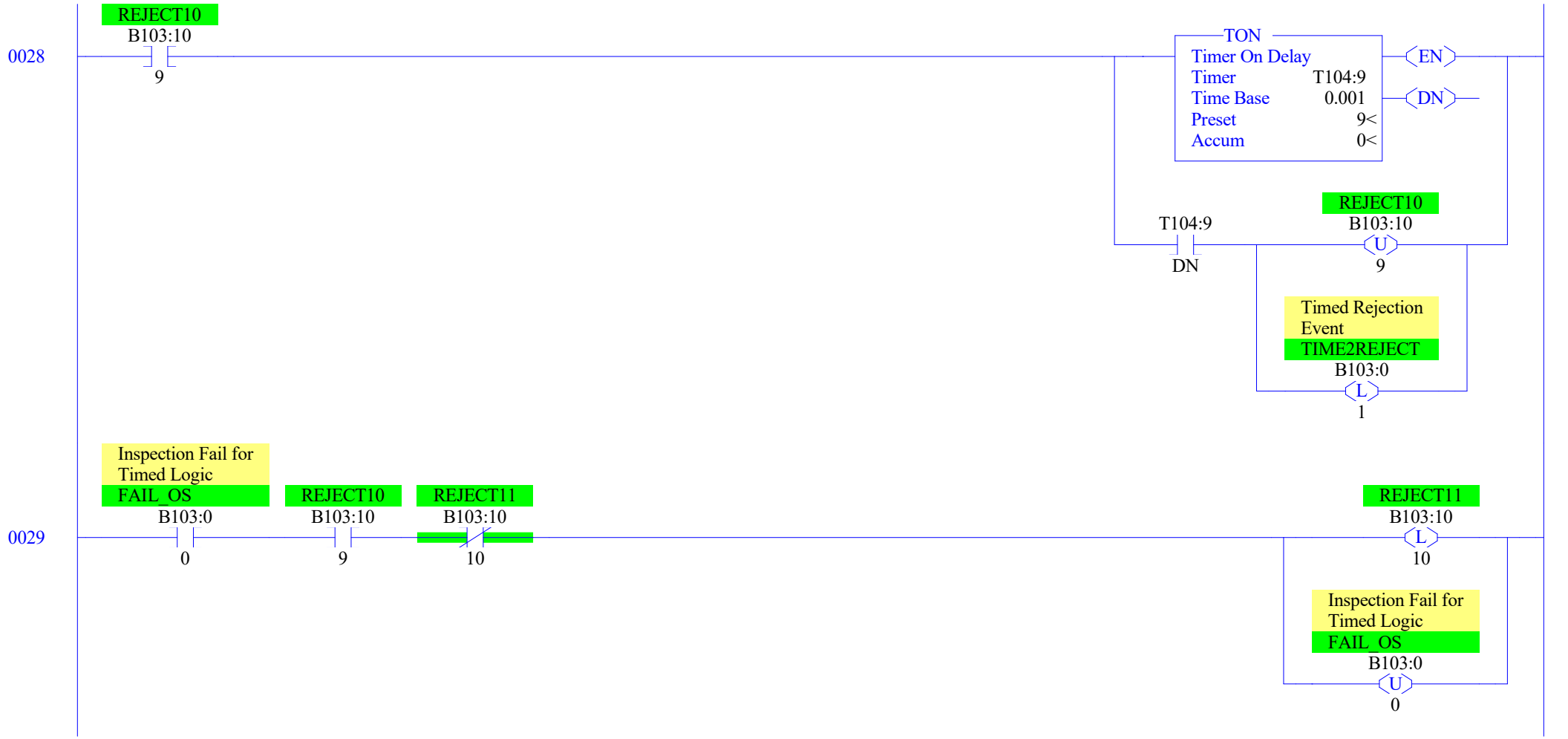

0018
REJECT5
B103:10
4
TON
Timer On Delay
Timer T104:4
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:4
DN
REJECT5
B103:10
U
4
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0019
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
REJECT5
B103:10
4
REJECT6
B103:10
5
REJECT6
B103:10
L
5
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

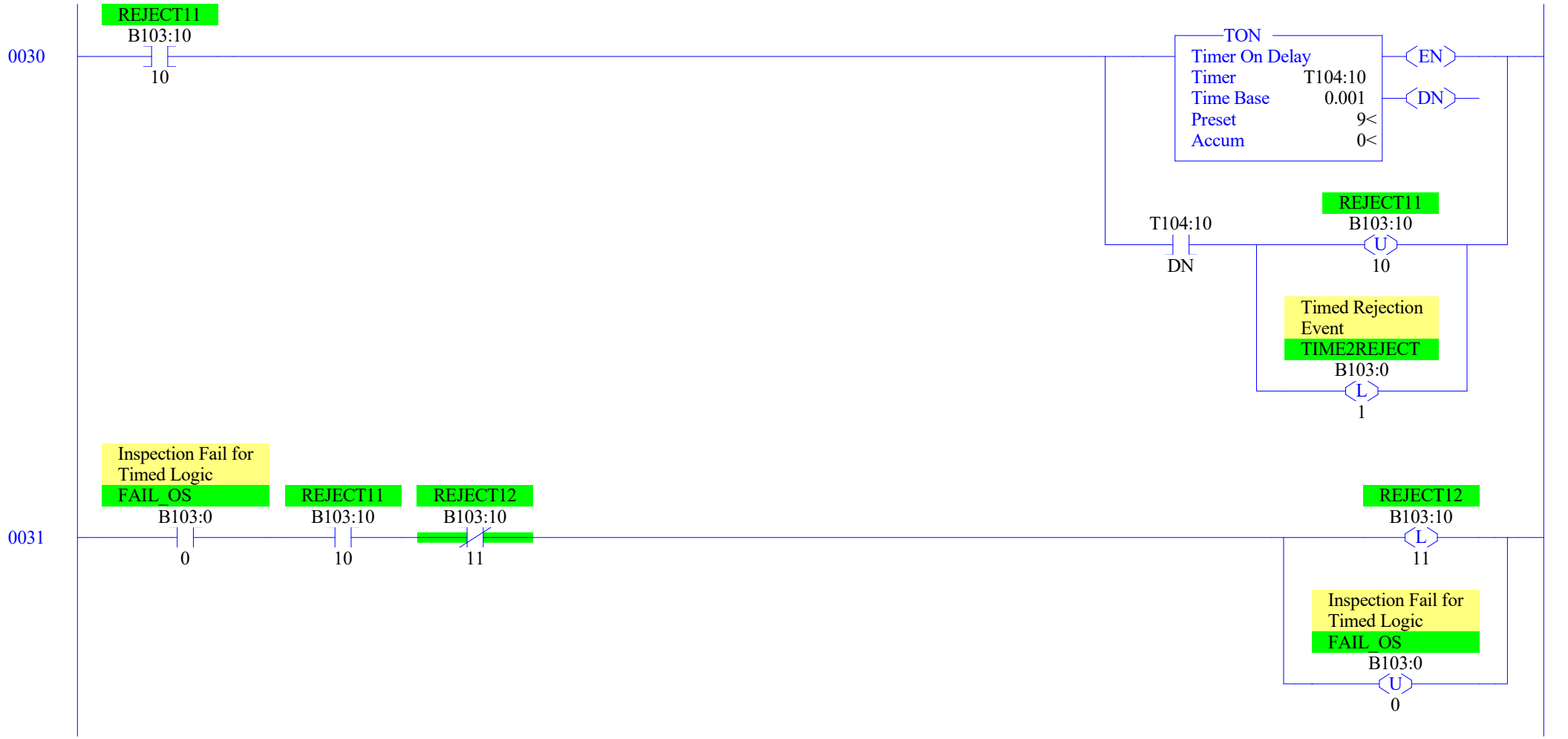

0020
REJECT6
B103:10
5
TON
Timer On Delay
Timer T104:5
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:5
DN
REJECT6
B103:10
U
5
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0021
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
REJECT6
B103:10
5
REJECT7
B103:10
6
REJECT7
B103:10
L
6
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

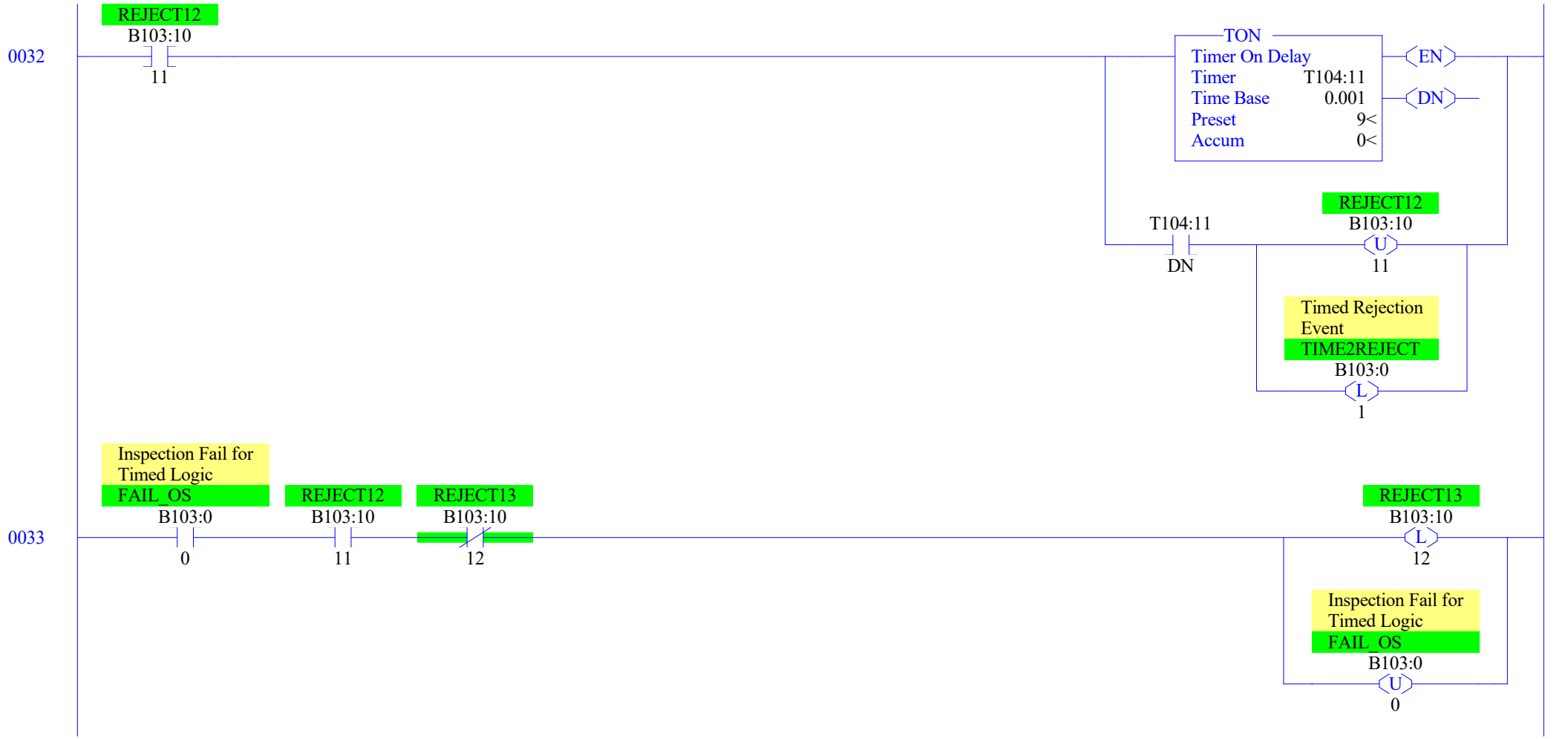

0022
REJECT7
B103:10
6
TON
Timer On Delay
Timer T104:6
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:6
DN
REJECT7
B103:10
U
6
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0023
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
REJECT7
B103:10
6
REJECT8
B103:10
7
REJECT8
B103:10
L
7
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

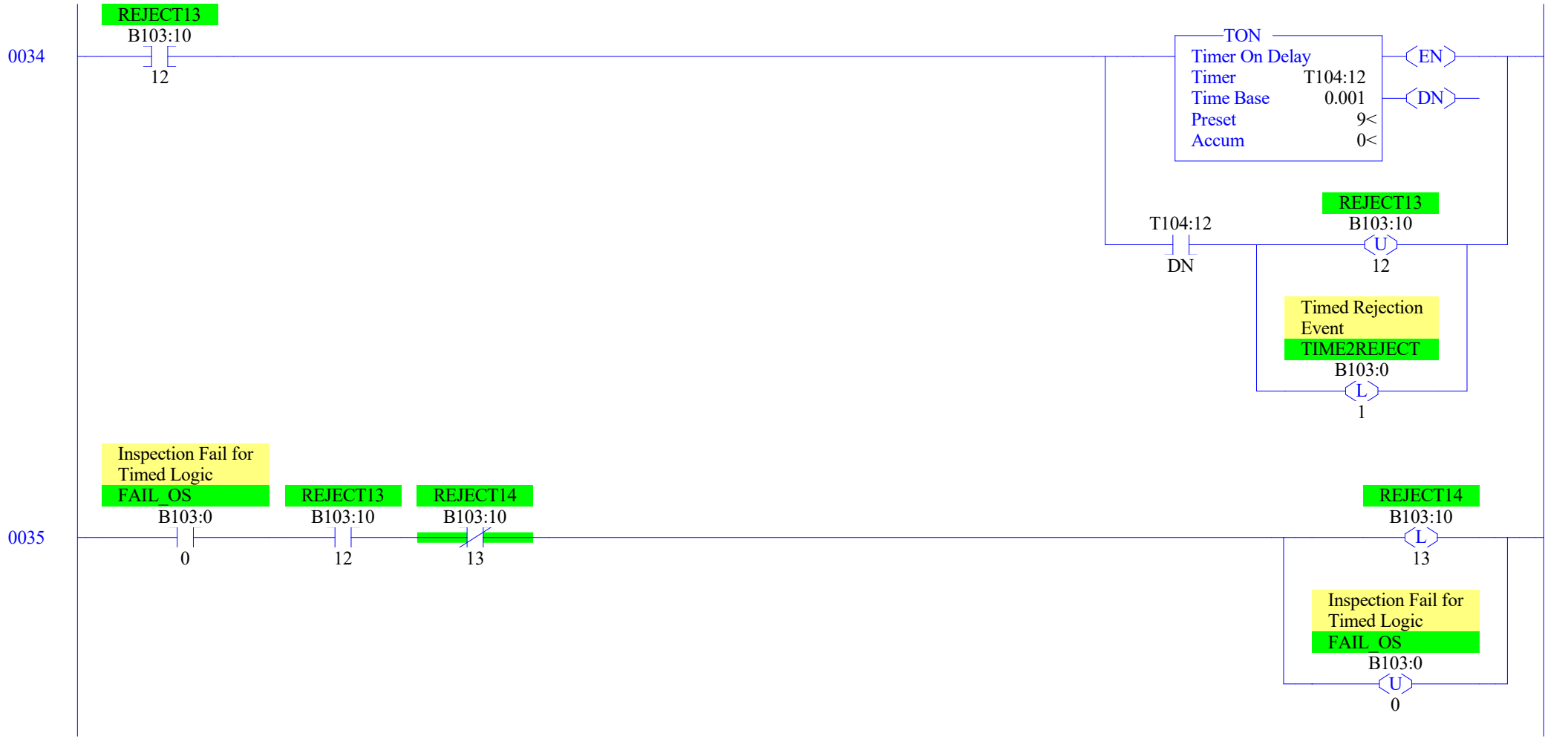

0024
REJECT8
B103:10
7
TON
Timer On Delay
Timer T104:7
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:7
DN
REJECT8
B103:10
U
7
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0025
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
REJECT8
B103:10
7
REJECT9
B103:10
8
REJECT9
B103:10
L
8
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

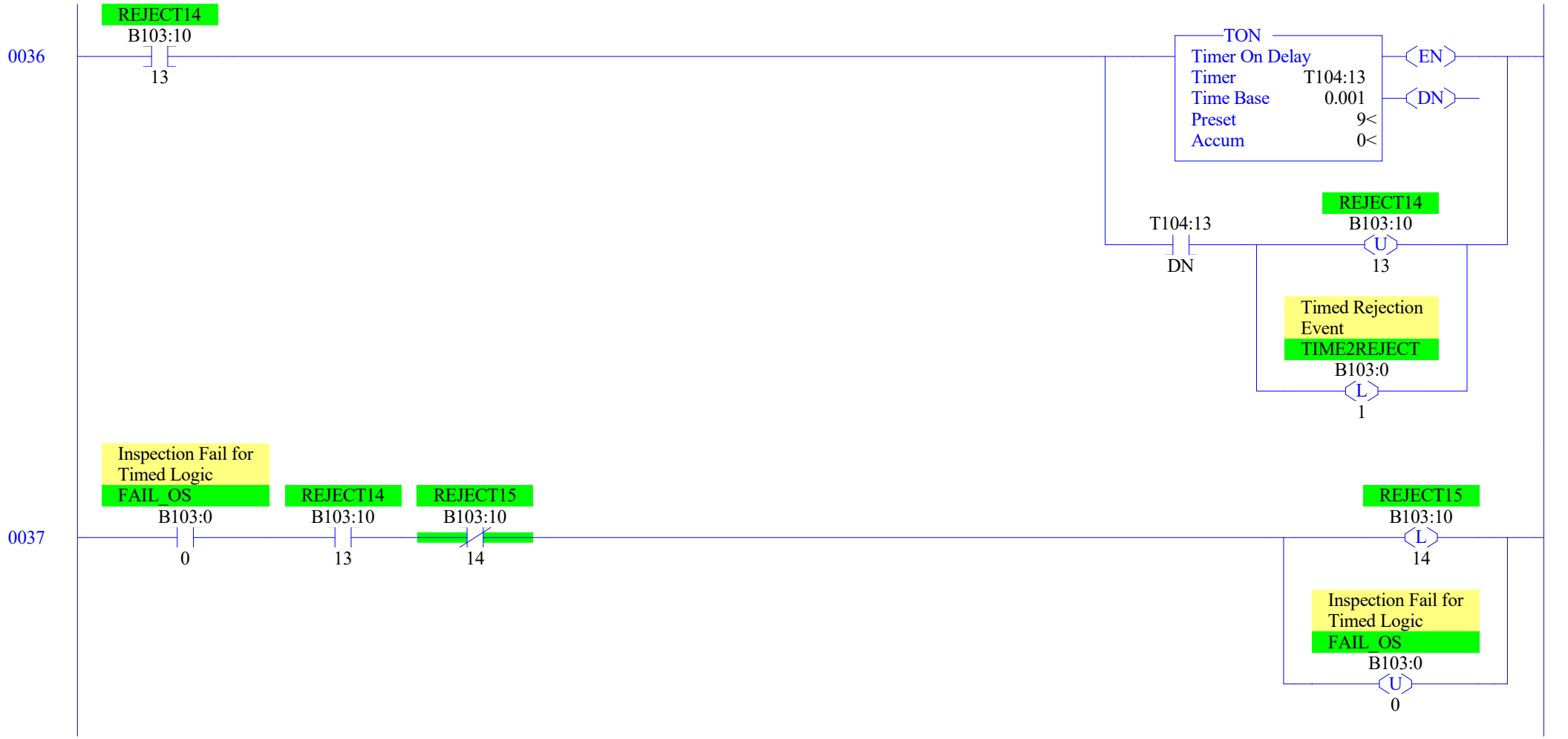

0026
REJECT9
B103:10
8
TON
Timer On Delay
Timer T104:8
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:8
DN
REJECT9
B103:10
U
8
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0027
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
REJECT9
B103:10
8
REJECT10
B103:10
9
REJECT10
B103:10
L
9
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

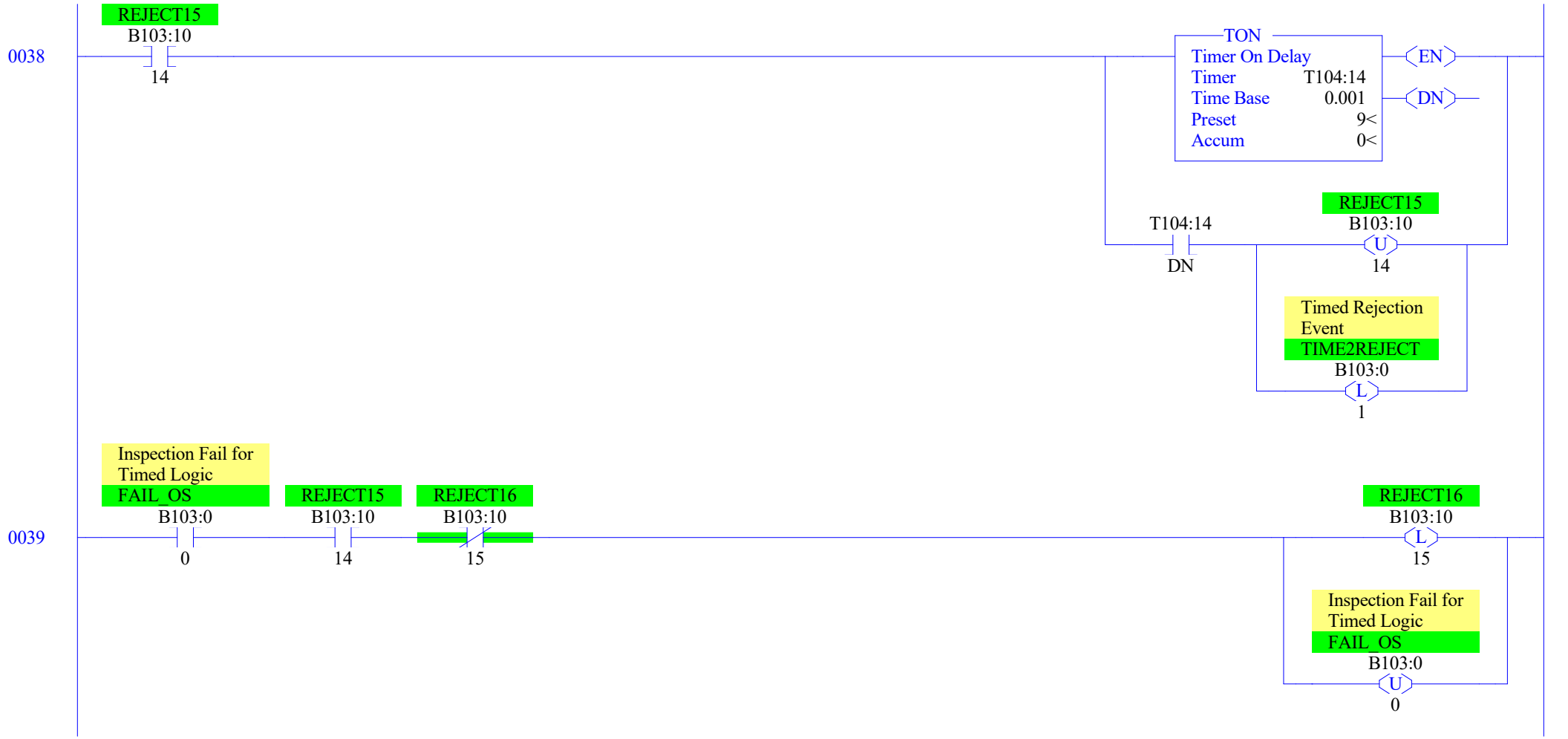

0028
REJECT10
B103:10
9
TON
Timer On Delay
Timer T104:9
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:9
DN
REJECT10
B103:10
U
9
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0029
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
REJECT10
B103:10
9
REJECT11
B103:10
10
REJECT11
B103:10
L
10
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

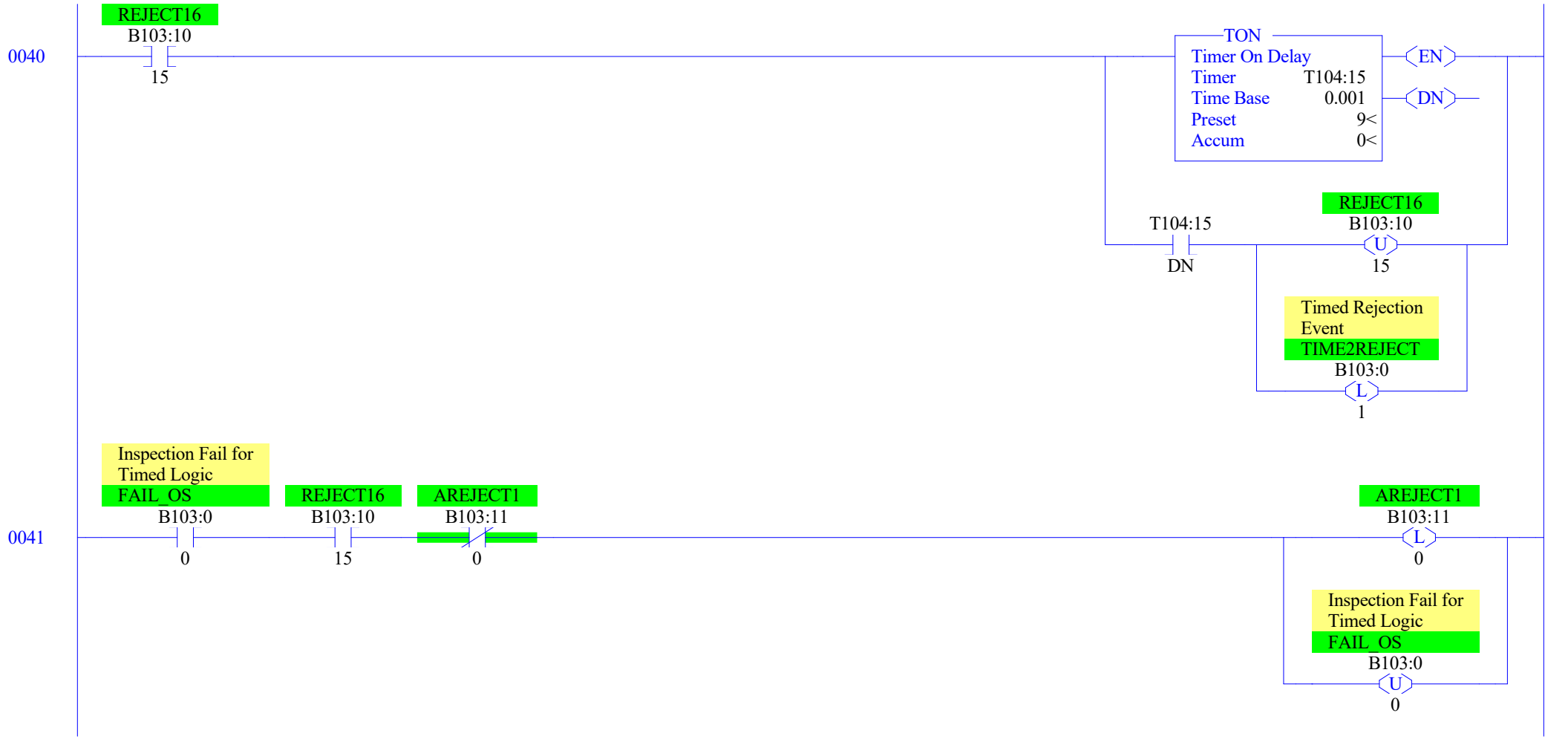

0030
REJECT11
B103:10
10
TON
Timer On Delay
Timer T104:10
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:10
DN
REJECT11
B103:10
U
10
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0031
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
REJECT11
B103:10
10
REJECT12
B103:10
11
REJECT12
B103:10
L
11
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

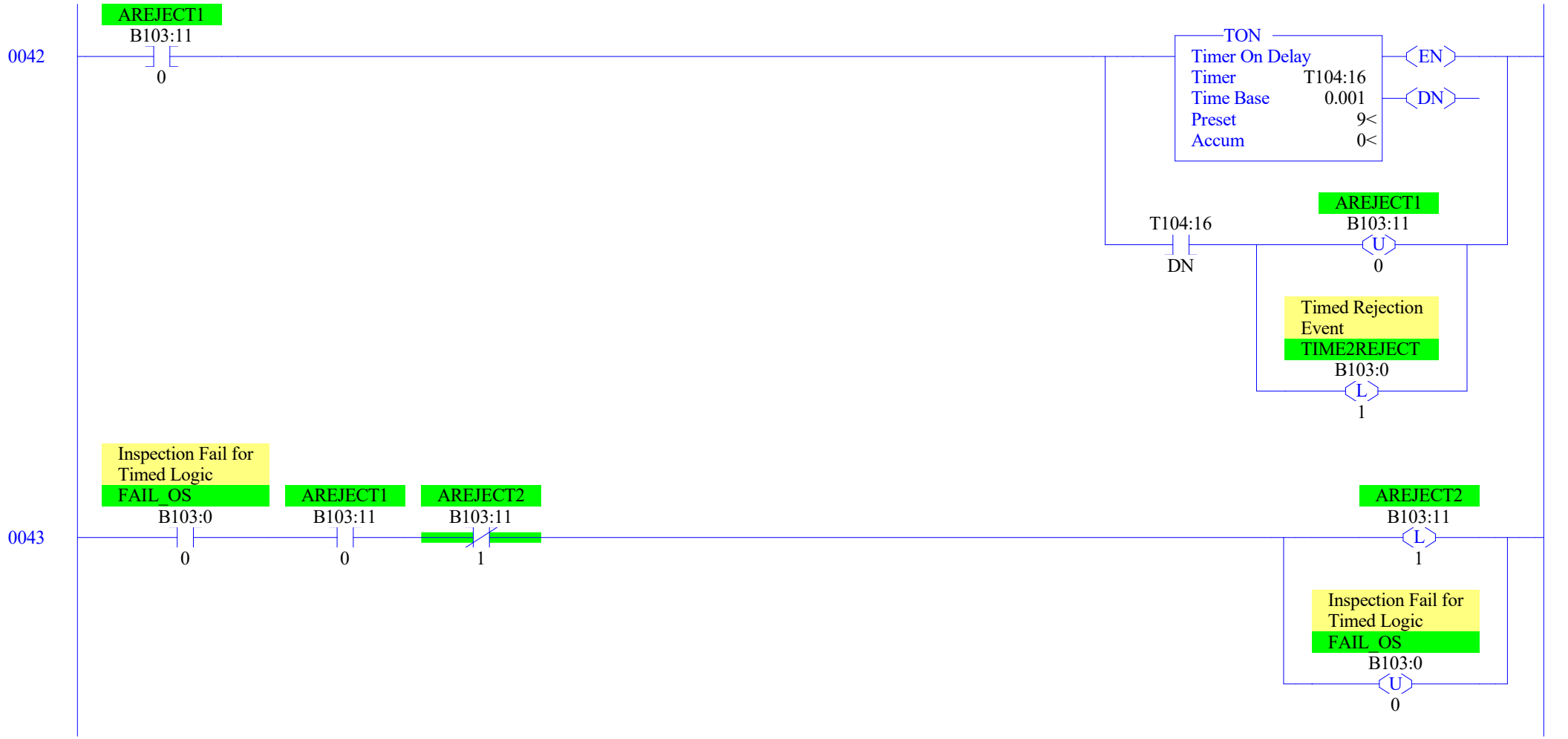

0032
REJECT12
B103:10
11
TON
Timer On Delay
Timer T104:11
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:11
DN
REJECT12
B103:10
U
11
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0033
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
REJECT12
B103:10
11
REJECT13
B103:10
12
REJECT13
B103:10
L
12
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

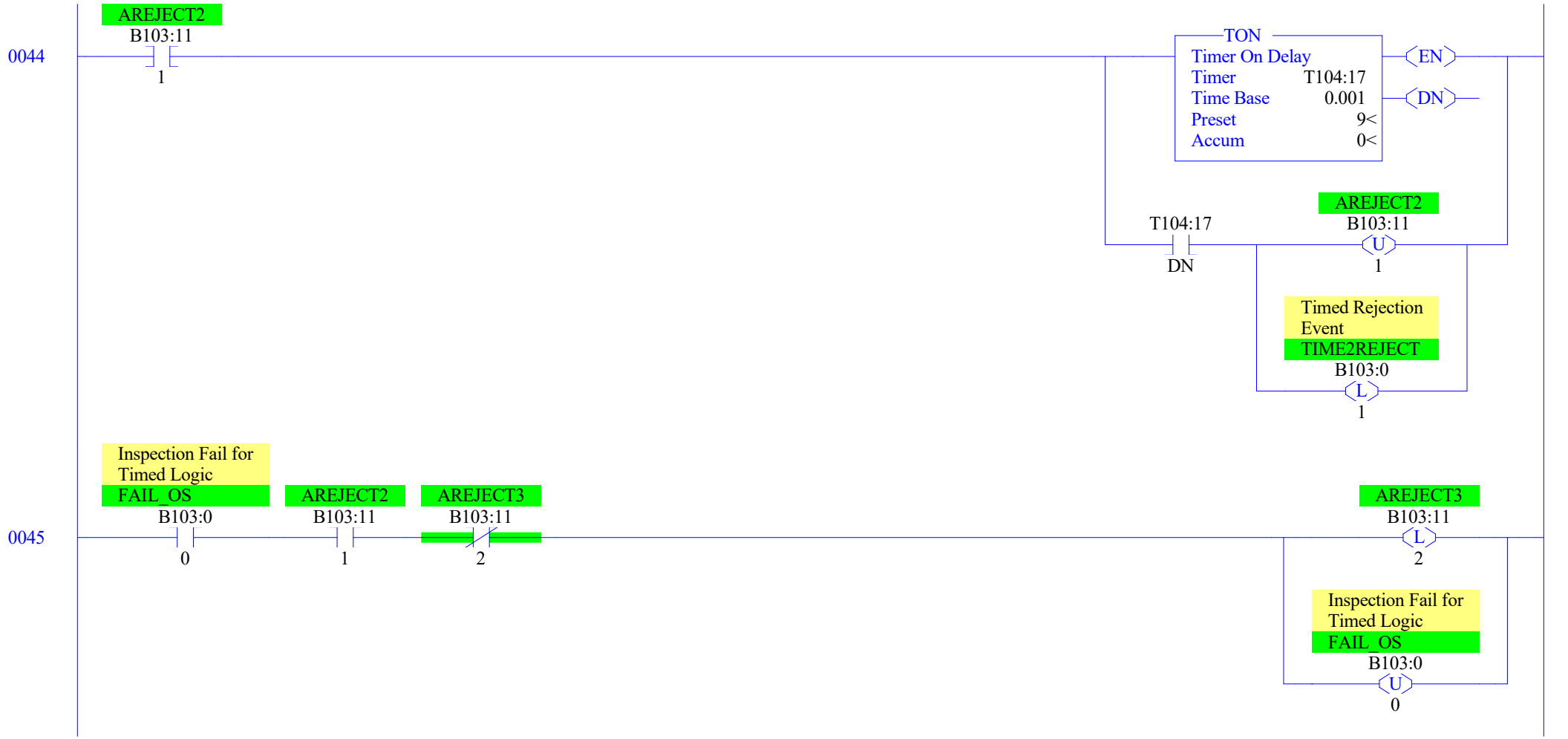

0034
REJECT13
B103:10
12
TON
Timer On Delay
Timer T104:12
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:12
DN
REJECT13
B103:10
U
12
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0035
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
REJECT13
B103:10
12
REJECT14
B103:10
13
REJECT14
B103:10
L
13
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

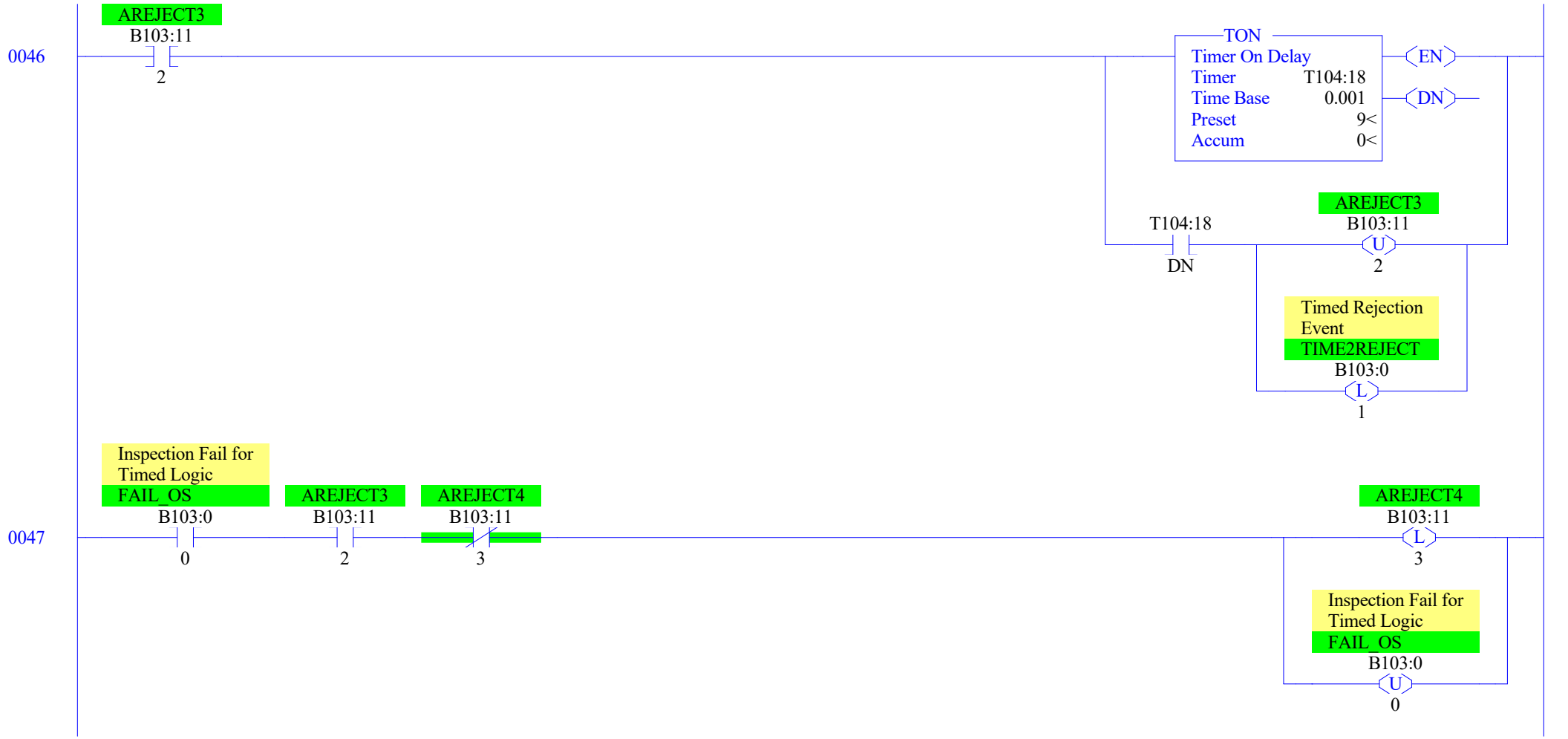

0036
REJECT14
B103:10
13
TON
Timer On Delay
Timer T104:13
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:13
DN
REJECT14
B103:10
U
13
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0037
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
REJECT14
B103:10
13
REJECT15
B103:10
14
REJECT15
B103:10
L
14
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

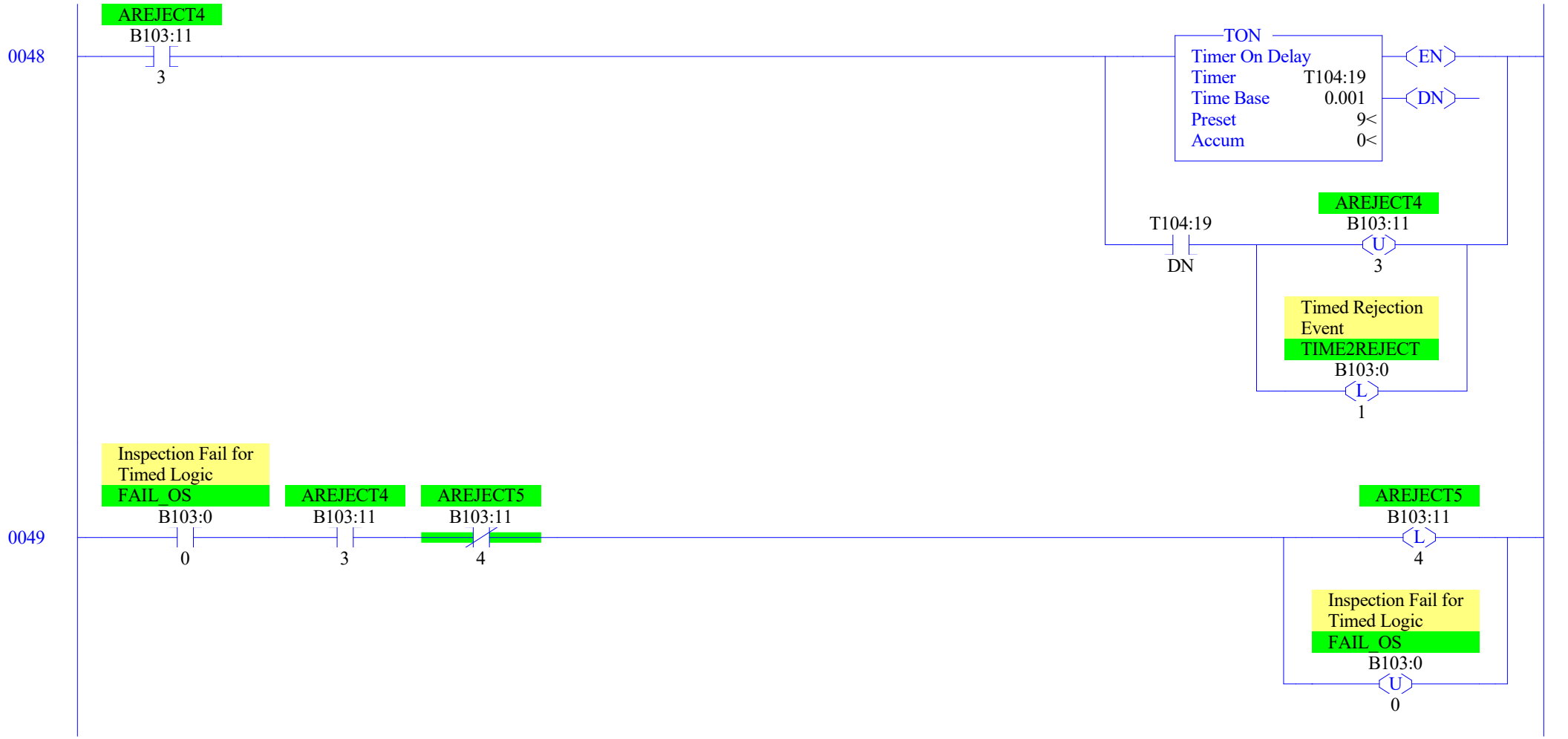

0038
REJECT15
B103:10
14
TON
Timer On Delay
Timer T104:14
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:14
DN
REJECT15
B103:10
U
14
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0039
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
REJECT15
B103:10
14
REJECT16
B103:10
15
REJECT16
B103:10
L
15
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

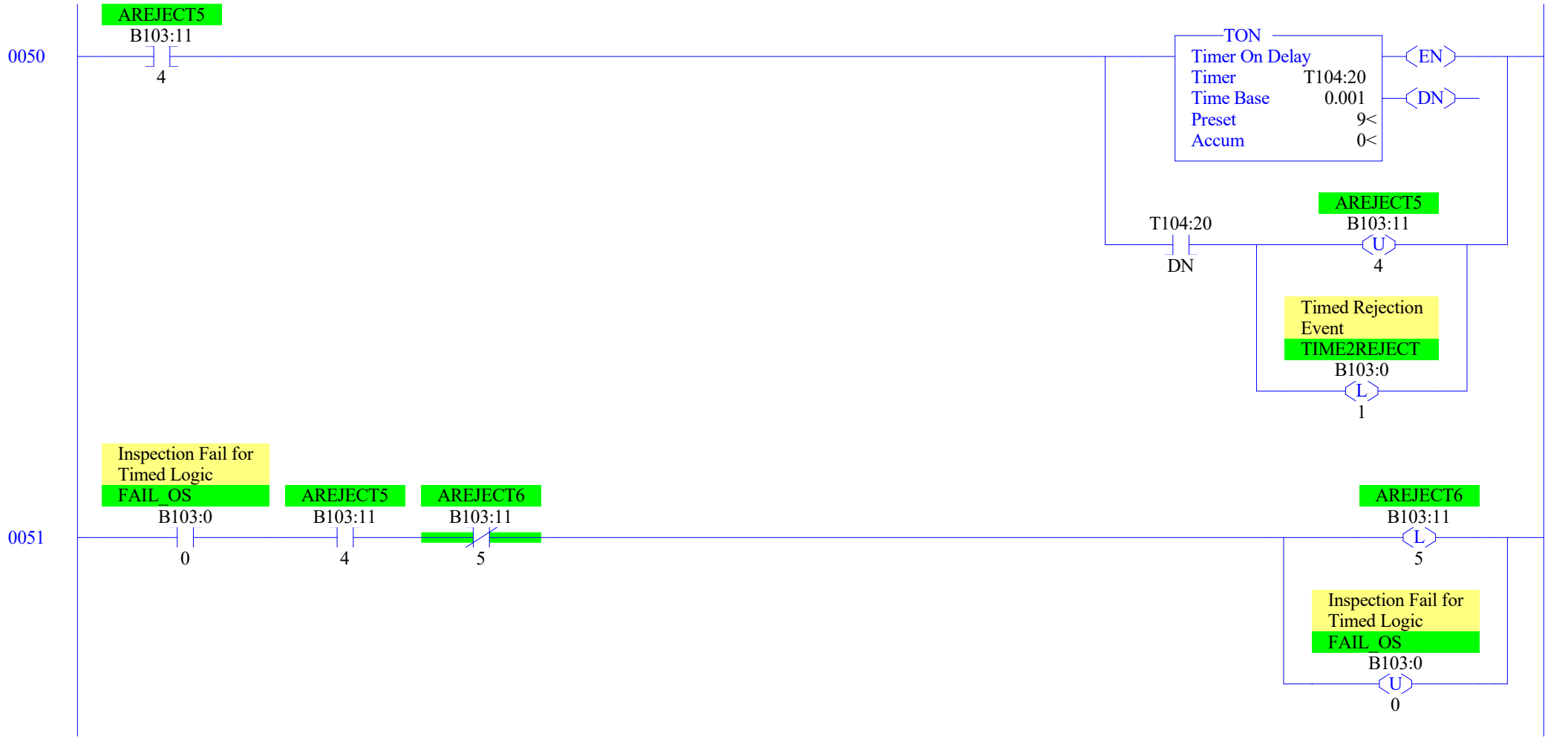

0040
REJECT16
B103:10
15
TON
Timer On Delay
Timer T104:15
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:15
DN
REJECT16
B103:10
U
15
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0041
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
REJECT16
B103:10
15
AREJECT1
B103:11
0
AREJECT1
B103:11
L
0
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

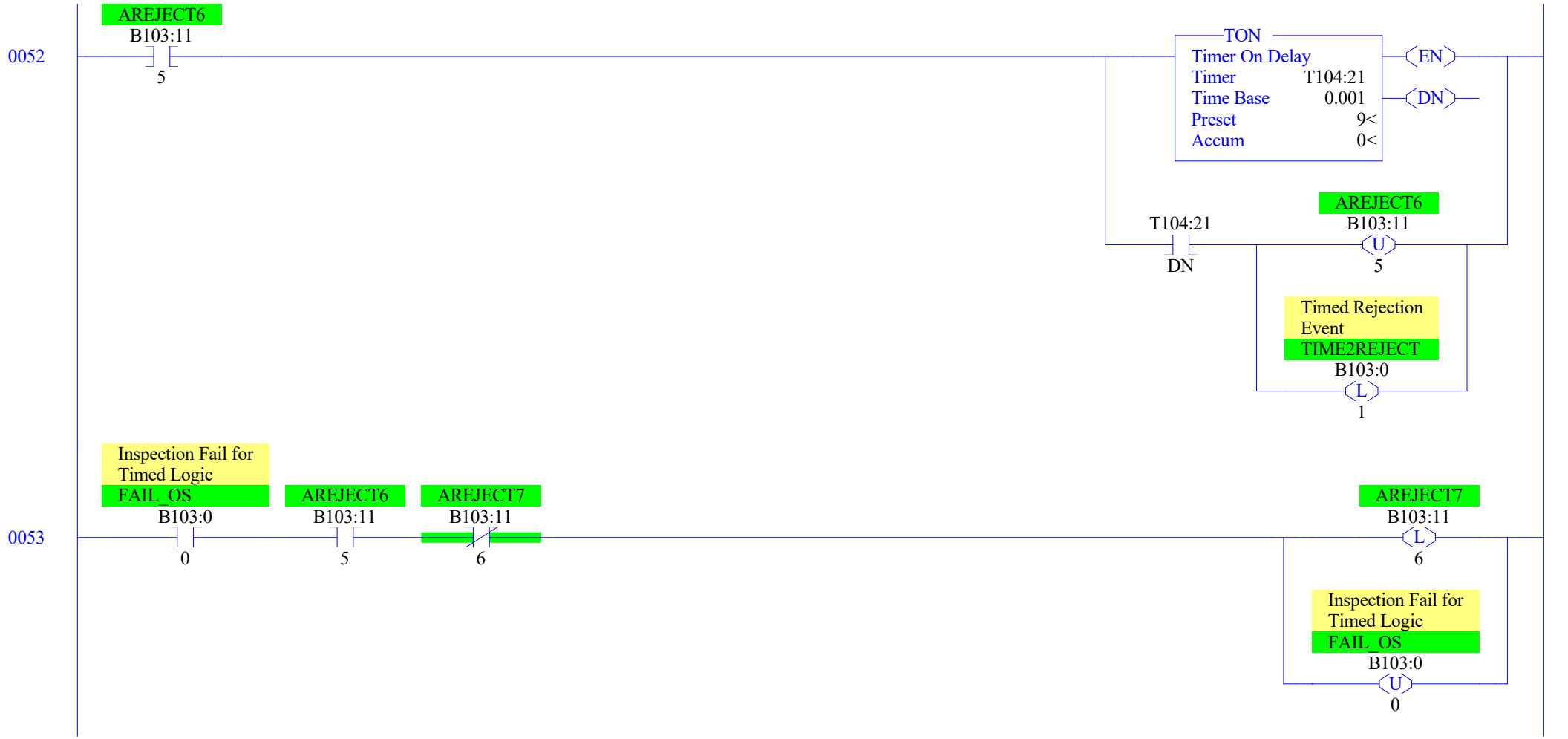

0042
AREJECT1
B103:11
0
TON
Timer On Delay
Timer T104:16
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:16
DN
AREJECT1
B103:11
U
0
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0043
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AREJECT1
B103:11
0
AREJECT2
B103:11
1
AREJECT2
B103:11
L
1
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

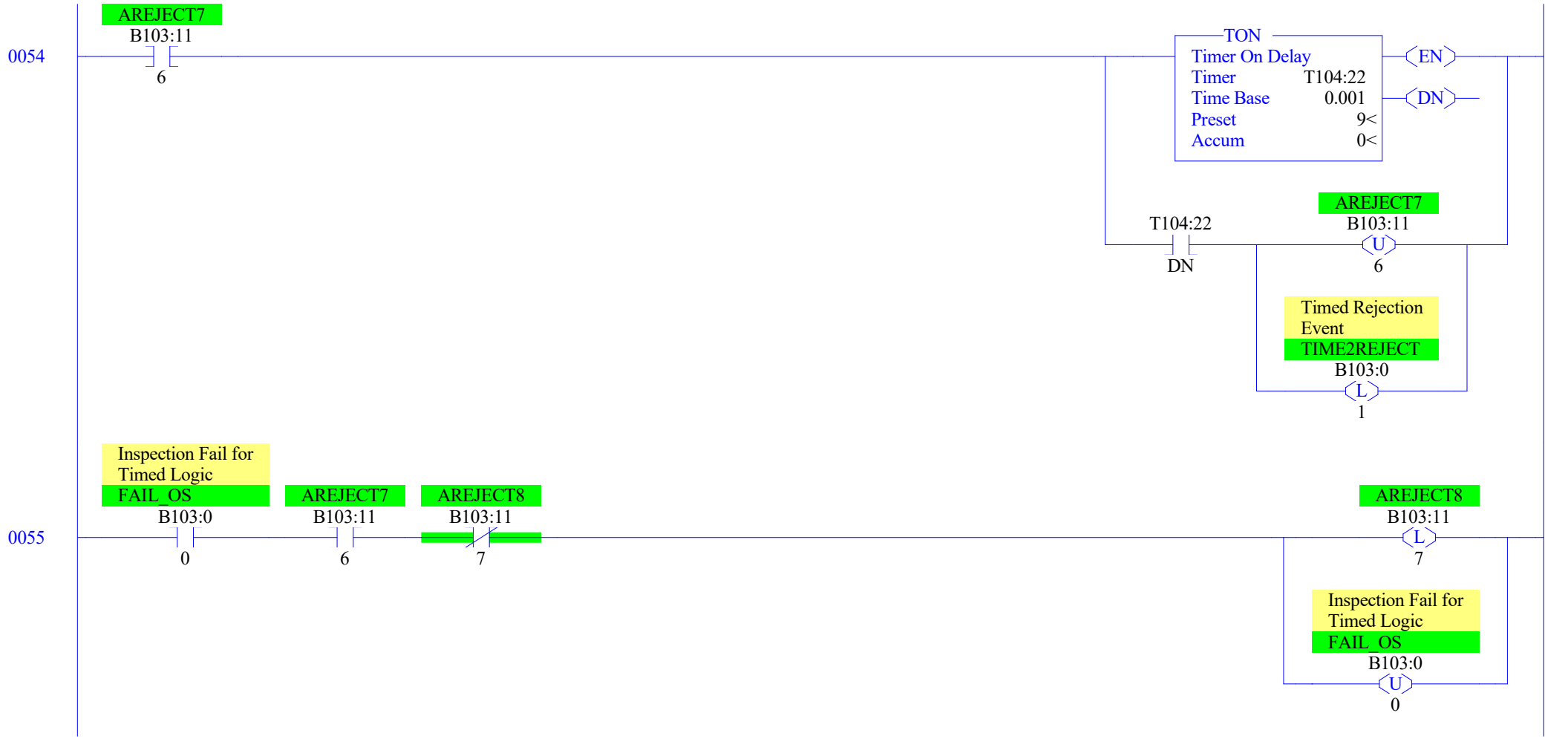

0044
AREJECT2
B103:11
1
TON
Timer On Delay
Timer T104:17
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:17
DN
AREJECT2
B103:11
U
1
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0045
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AREJECT2
B103:11
1
AREJECT3
B103:11
2
AREJECT3
B103:11
L
2
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

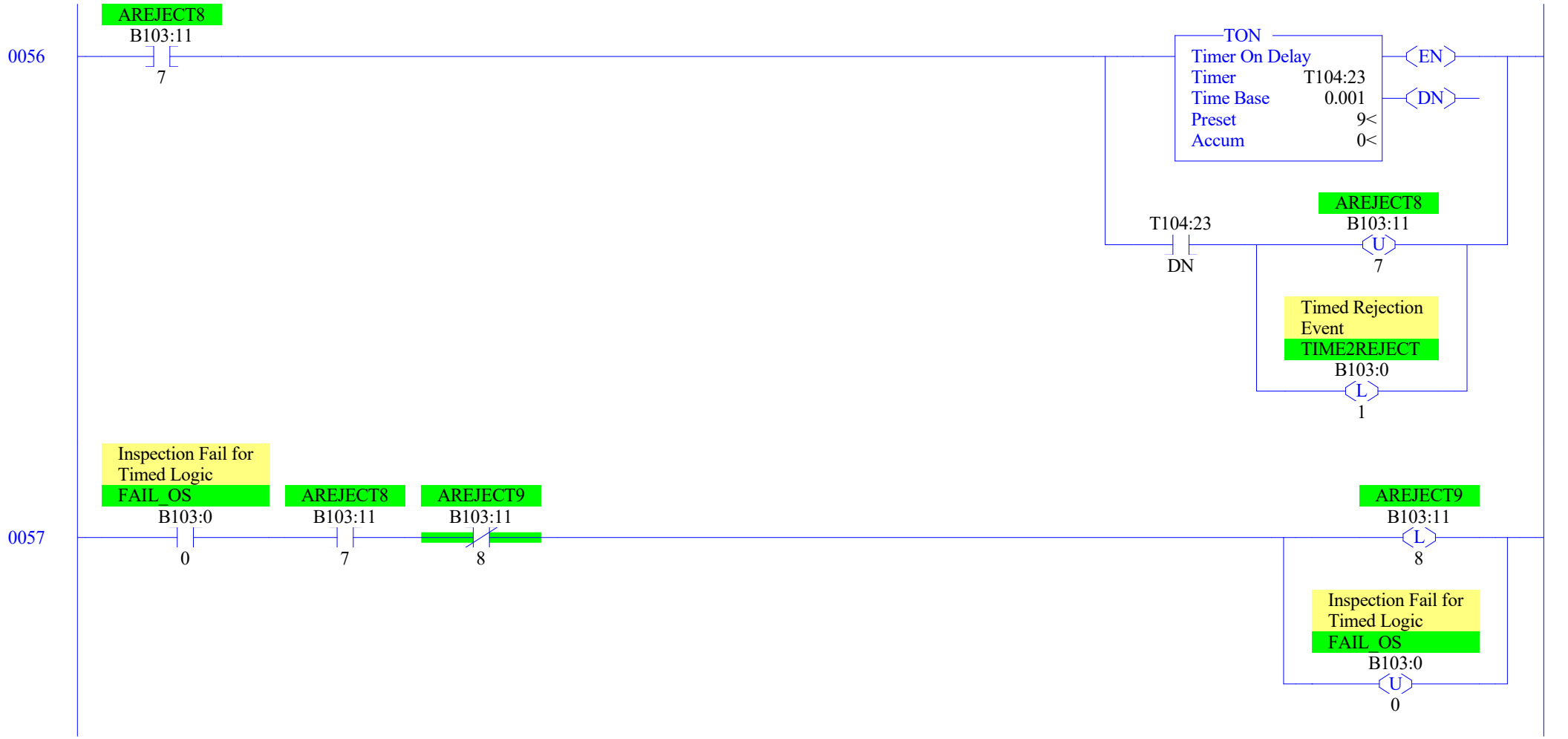

0046
AREJECT3
B103:11
2
TON
Timer On Delay
Timer T104:18
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:18
DN
AREJECT3
B103:11
U
2
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0047
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AREJECT3
B103:11
2
AREJECT4
B103:11
3
AREJECT4
B103:11
L
3
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

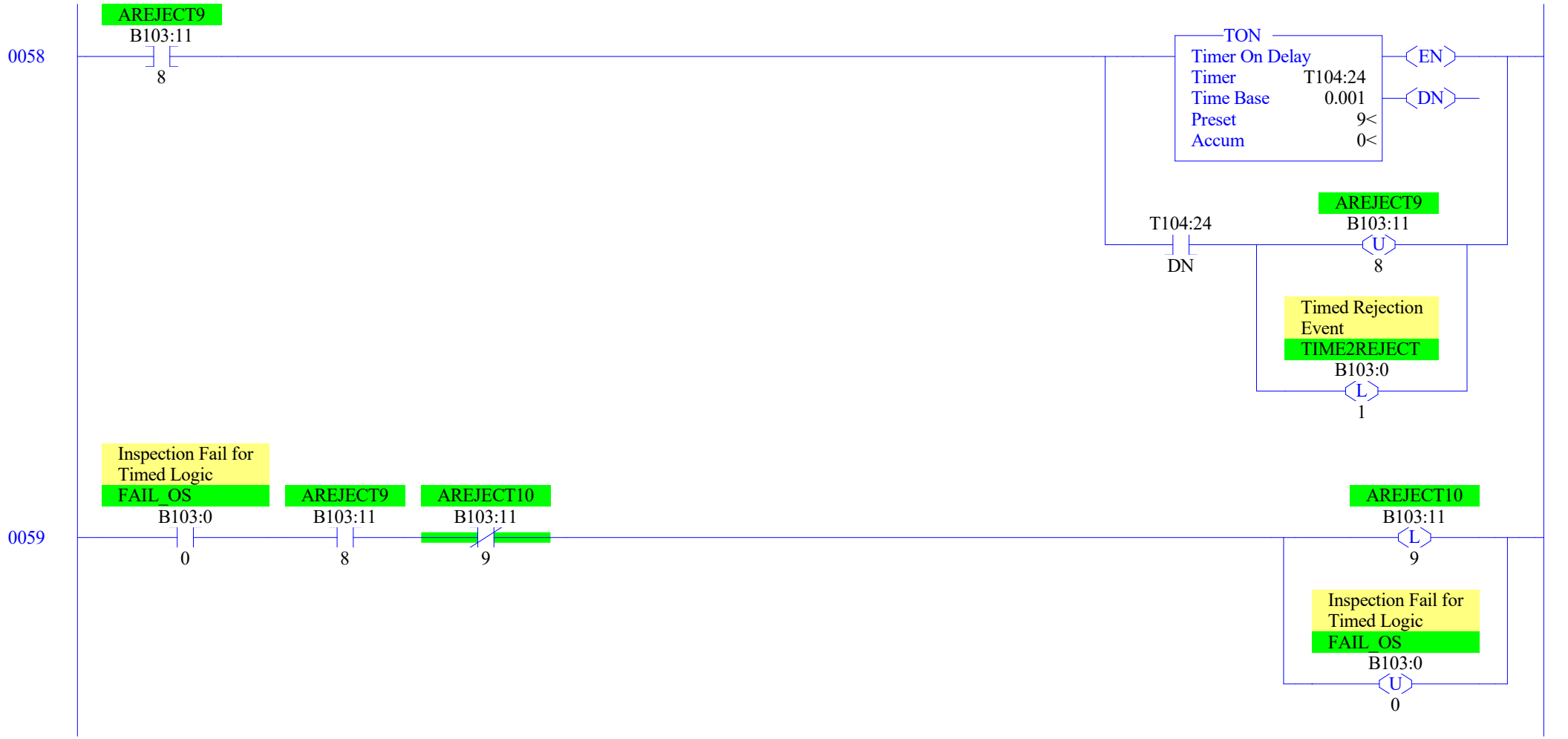

0048
AREJECT4
B103:11
3
TON
Timer On Delay
Timer T104:19
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:19
DN
AREJECT4
B103:11
U
3
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0049
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AREJECT4
B103:11
3
AREJECT5
B103:11
4
AREJECT5
B103:11
L
4
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

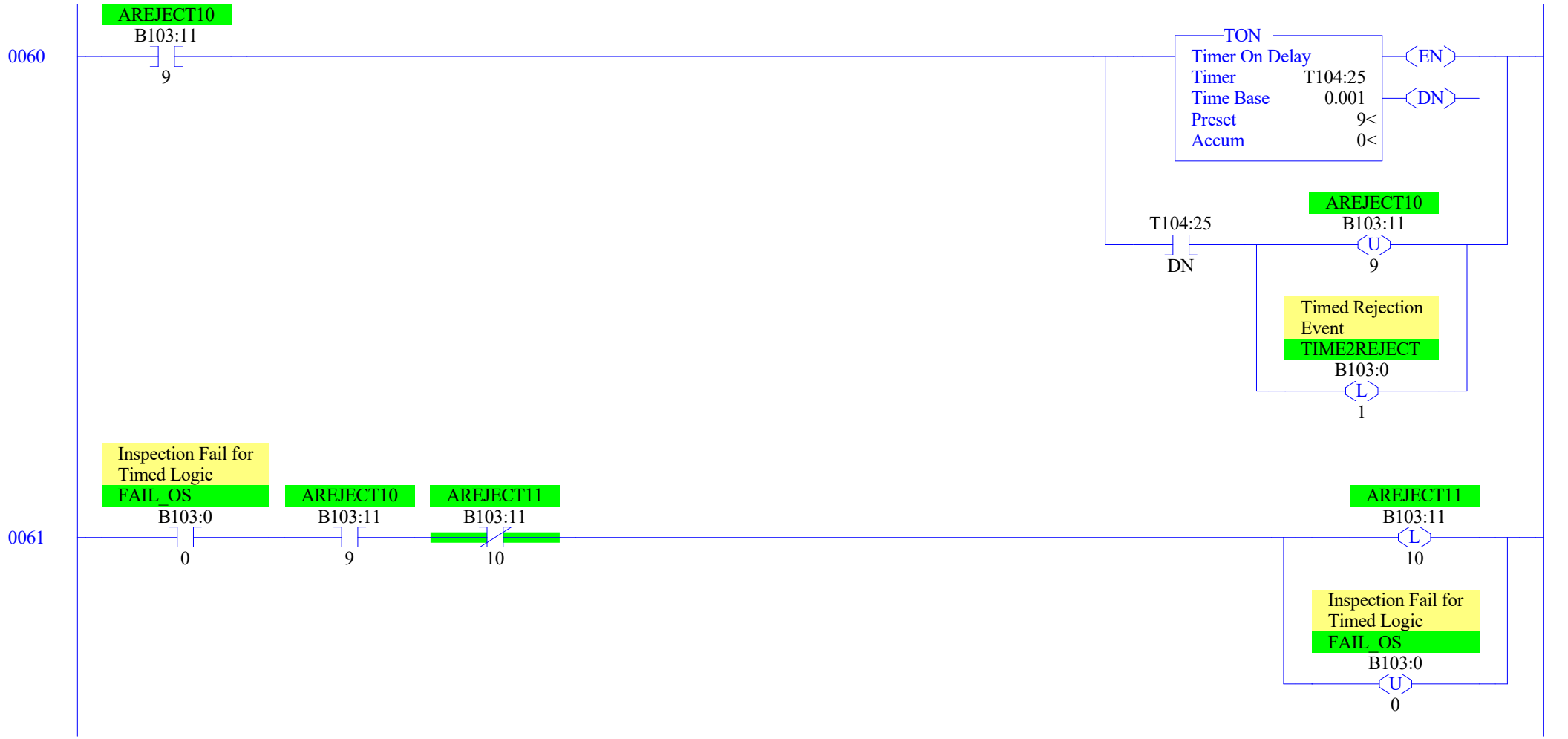

0050
AREJECT5
B103:11
4
TON
Timer On Delay
Timer T104:20
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:20
DN
AREJECT5
B103:11
U
4
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0051
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AREJECT5
B103:11
4
AREJECT6
B103:11
5
AREJECT6
B103:11
L
5
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

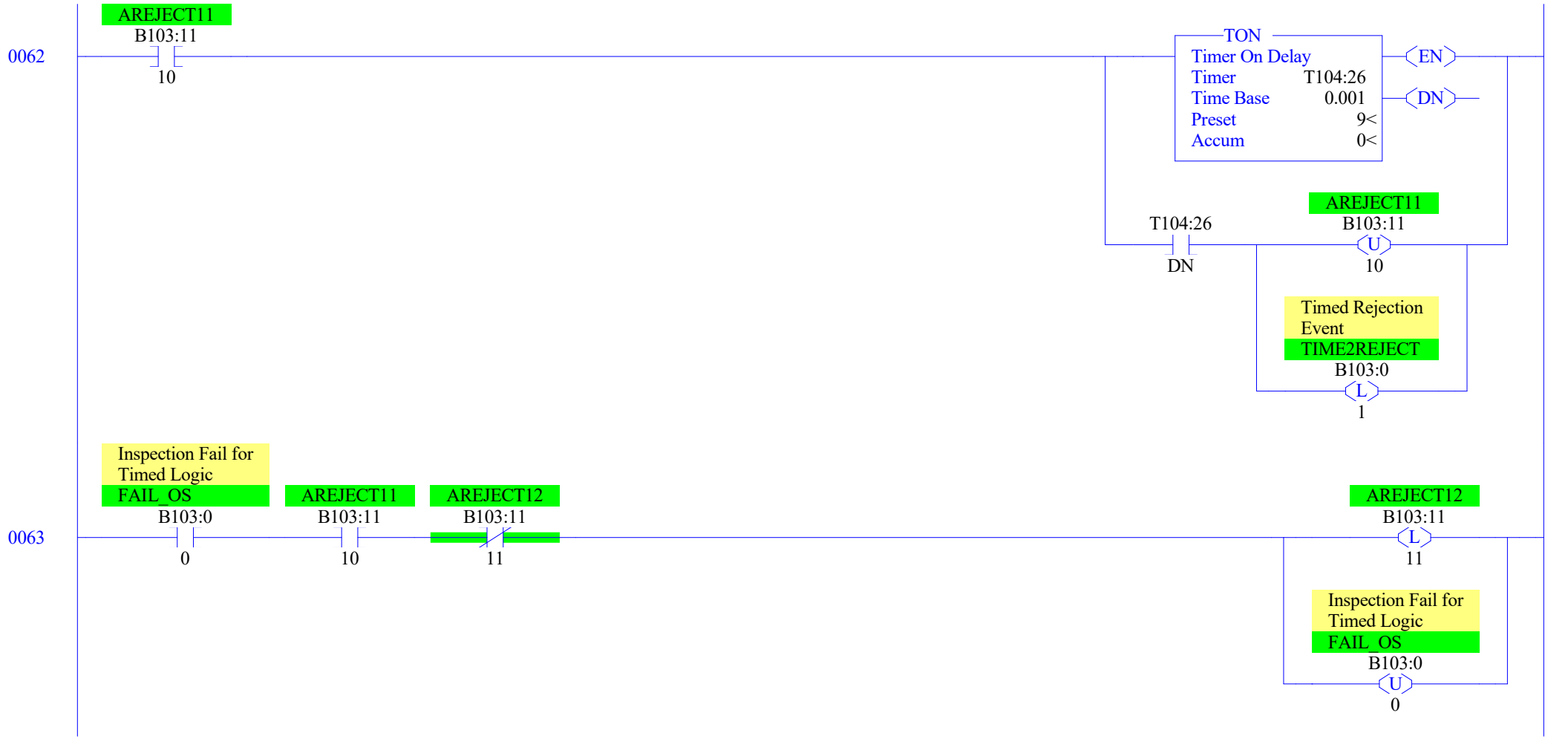

0052
AREJECT6
B103:11
5
TON
Timer On Delay
Timer T104:21
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:21
DN
AREJECT6
B103:11
U
5
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0053
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AREJECT6
B103:11
5
AREJECT7
B103:11
6
AREJECT7
B103:11
L
6
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

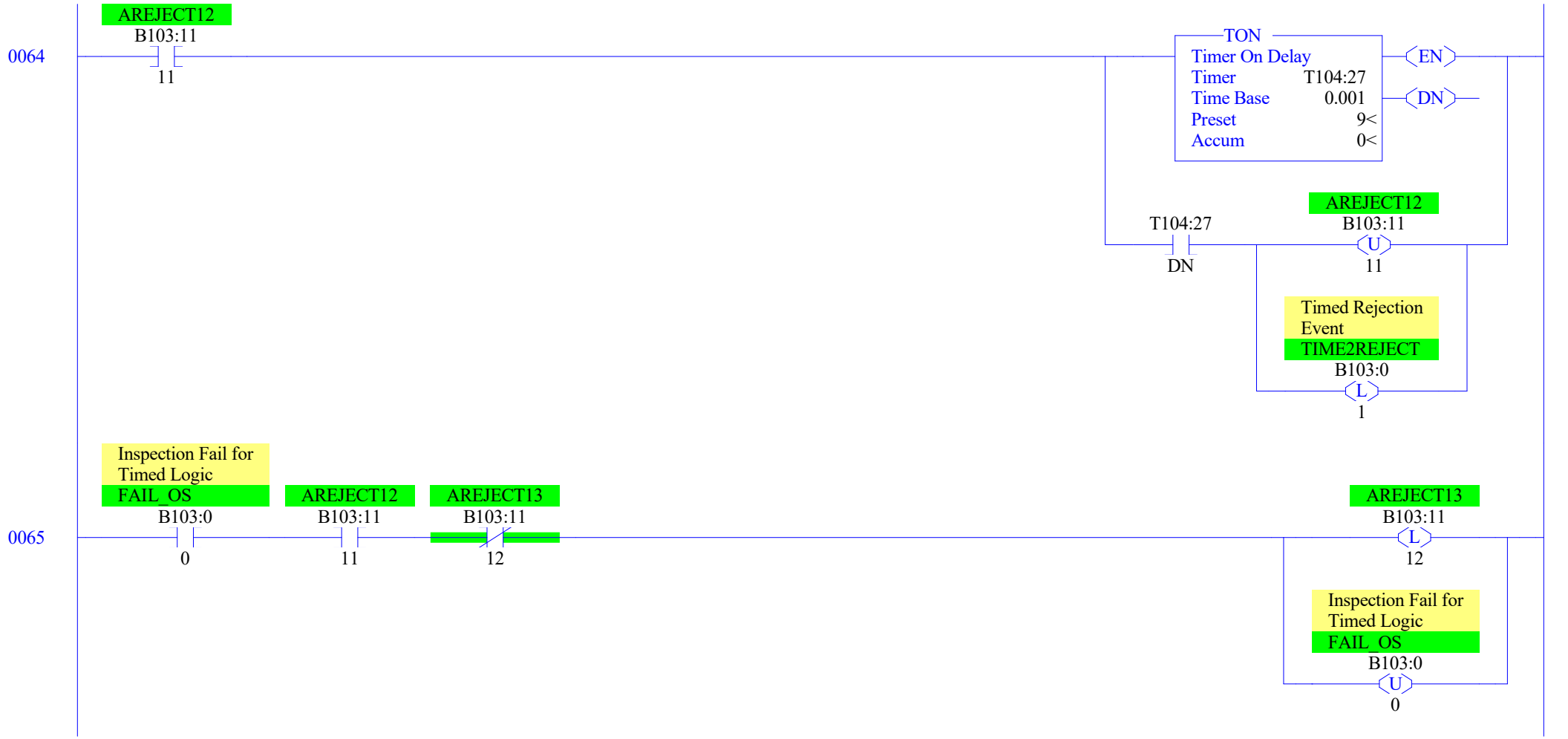

0054
AREJECT7
B103:11
6
TON
Timer On Delay
Timer T104:22
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:22
DN
AREJECT7
B103:11
U
6
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0055
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AREJECT7
B103:11
6
AREJECT8
B103:11
7
AREJECT8
B103:11
L
7
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

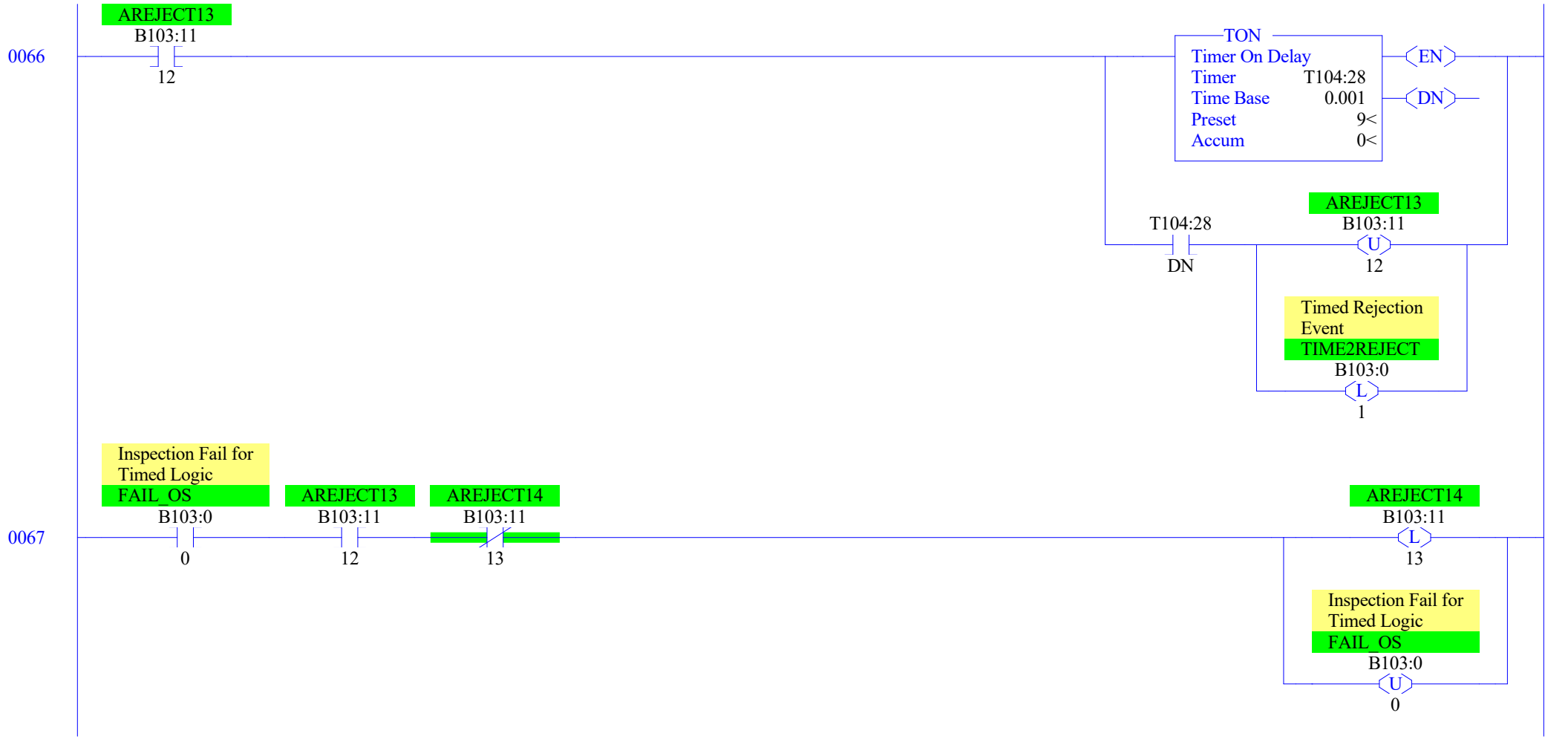

0056
AREJECT8
B103:11
7
TON
Timer On Delay
Timer T104:23
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:23
DN
AREJECT8
B103:11
U
7
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0057
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AREJECT8
B103:11
7
AREJECT9
B103:11
8
AREJECT9
B103:11
L
8
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

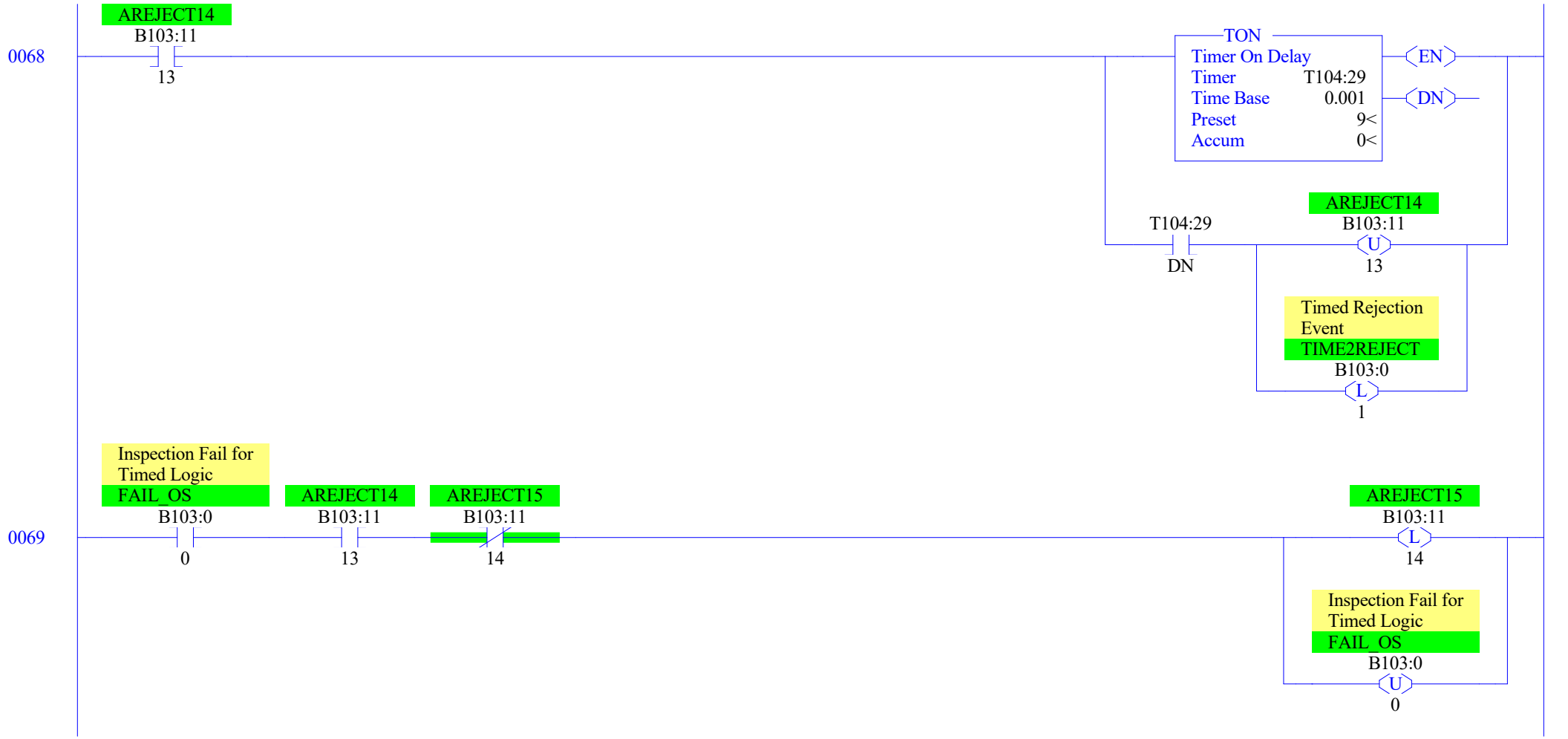

0058
AREJECT9
B103:11
8
TON
Timer On Delay
Timer T104:24
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:24
DN
AREJECT9
B103:11
U
8
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0059
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AREJECT9
B103:11
8
AREJECT10
B103:11
9
AREJECT10
B103:11
L
9
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

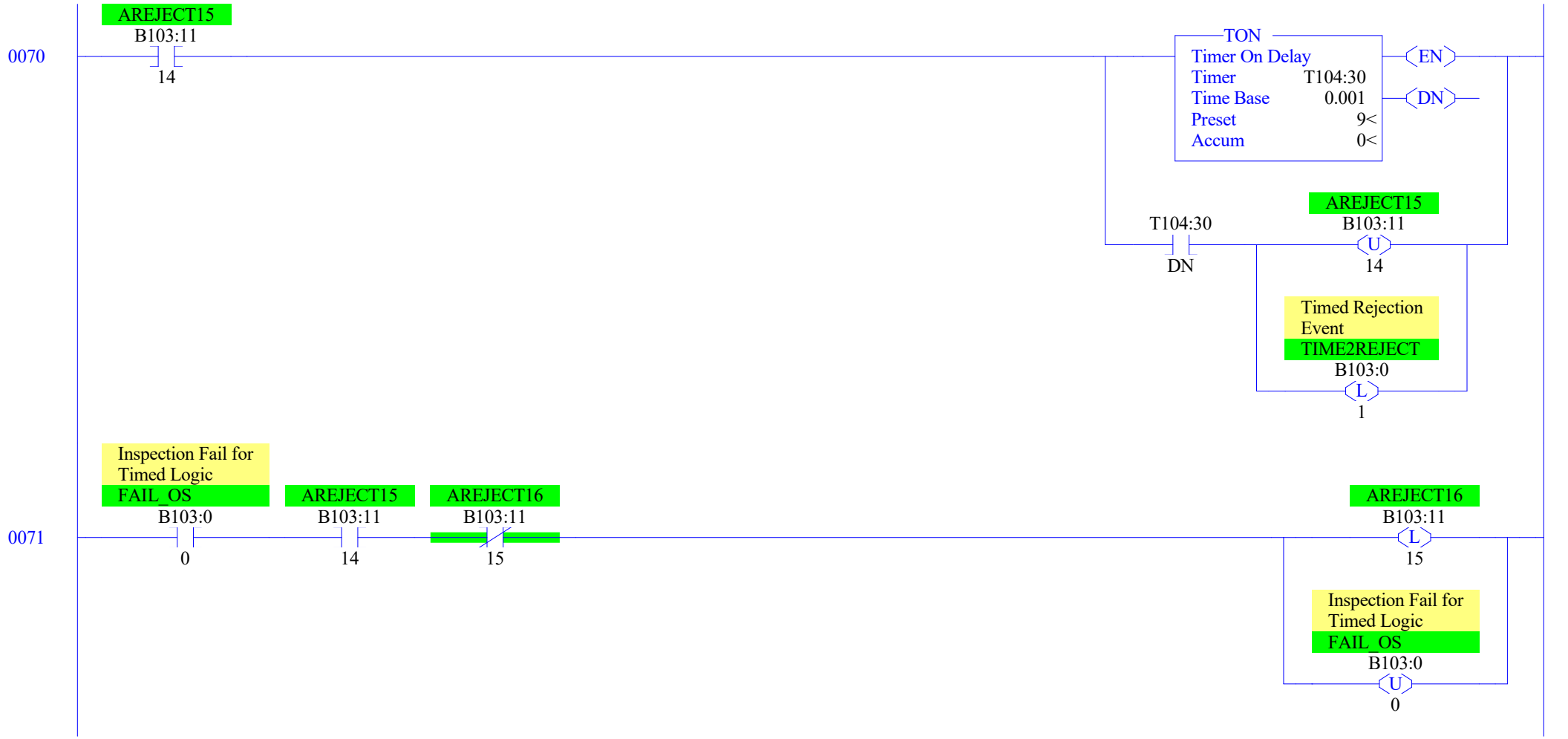

0060
AREJECT10
B103:11
9
TON
Timer On Delay
Timer T104:25
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:25
DN
AREJECT10
B103:11
U
9
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0061
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AREJECT10
B103:11
9
AREJECT11
B103:11
10
AREJECT11
B103:11
L
10
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

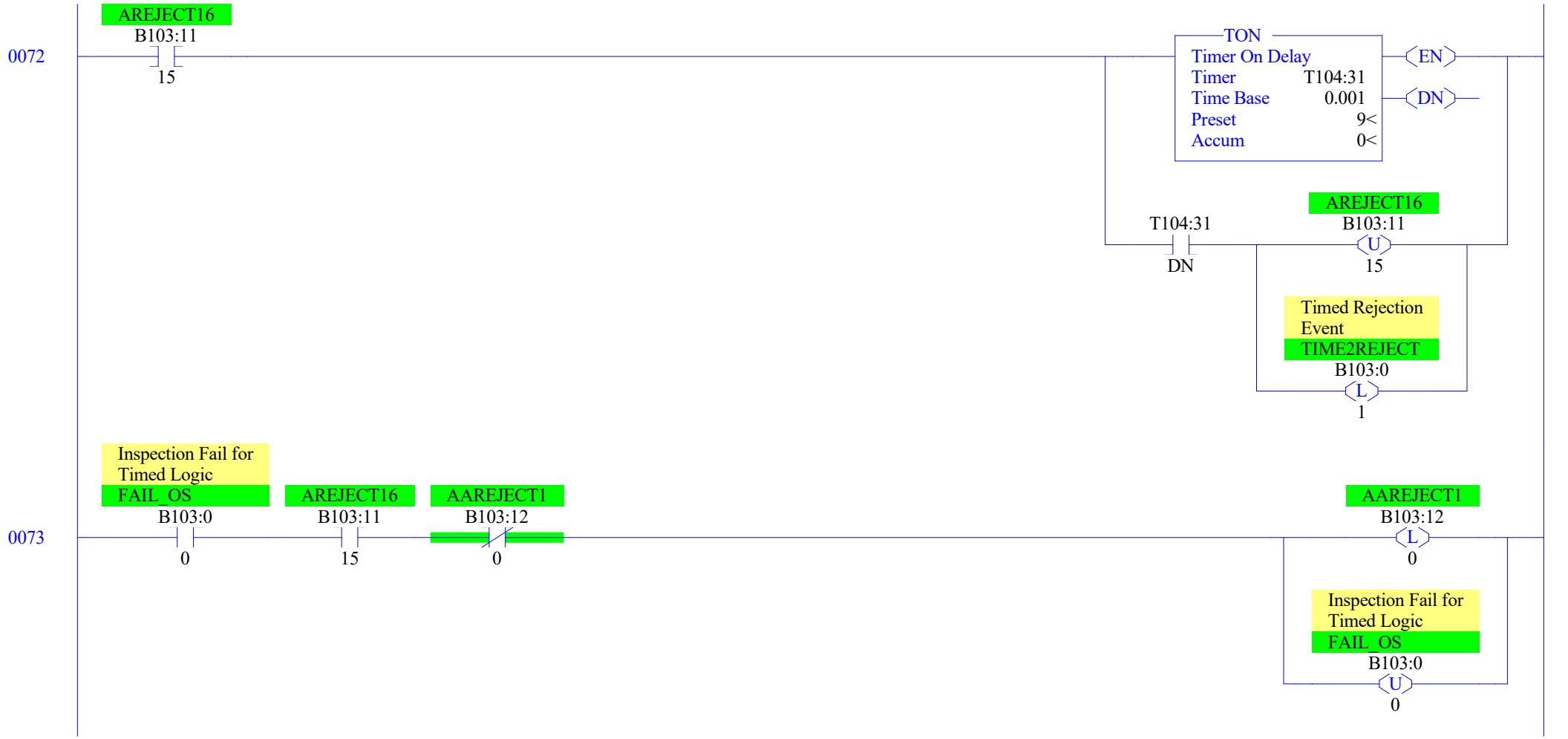

0062
AREJECT11
B103:11
10
TON
Timer On Delay
Timer T104:26
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:26
DN
AREJECT11
B103:11
U
10
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0063
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AREJECT11
B103:11
10
AREJECT12
B103:11
11
AREJECT12
B103:11
L
11
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

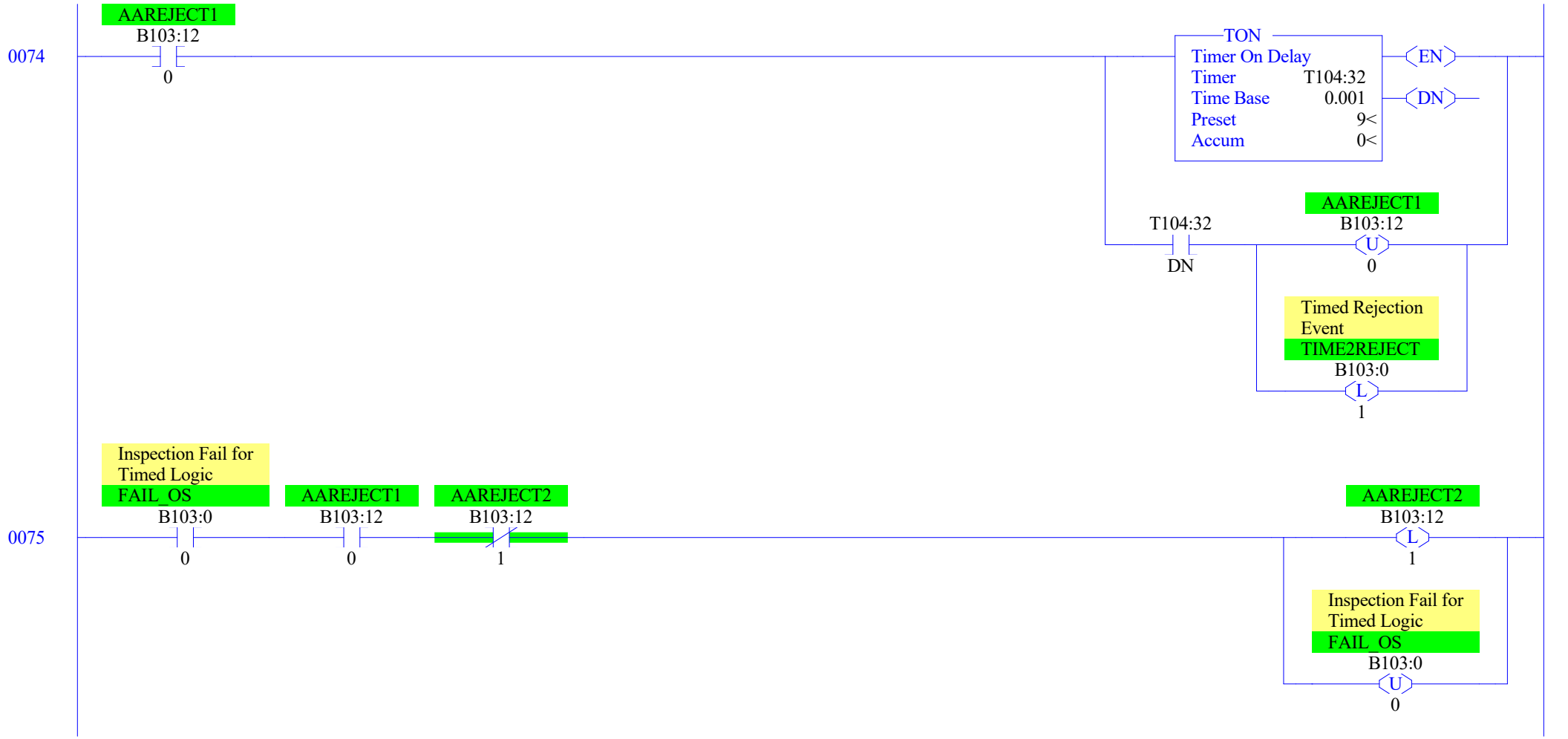

0064
AREJECT12
B103:11
11
TON
Timer On Delay
Timer T104:27
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:27
DN
AREJECT12
B103:11
U
11
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0065
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AREJECT12
B103:11
11
AREJECT13
B103:11
12
AREJECT13
B103:11
L
12
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

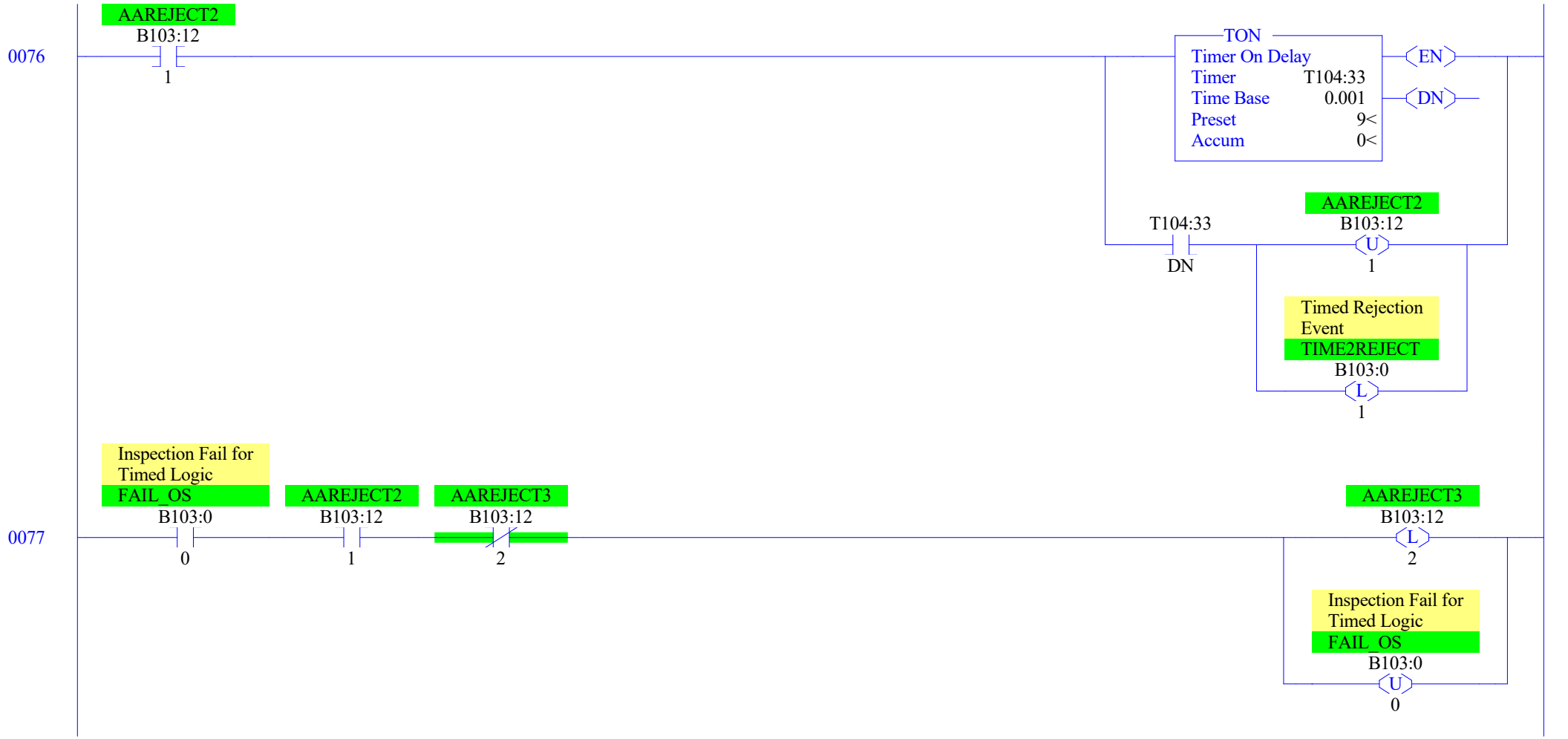

0066
AREJECT13
B103:11
12
TON
Timer On Delay
Timer T104:28
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:28
DN
AREJECT13
B103:11
U
12
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0067
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AREJECT13
B103:11
12
AREJECT14
B103:11
13
AREJECT14
B103:11
L
13
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

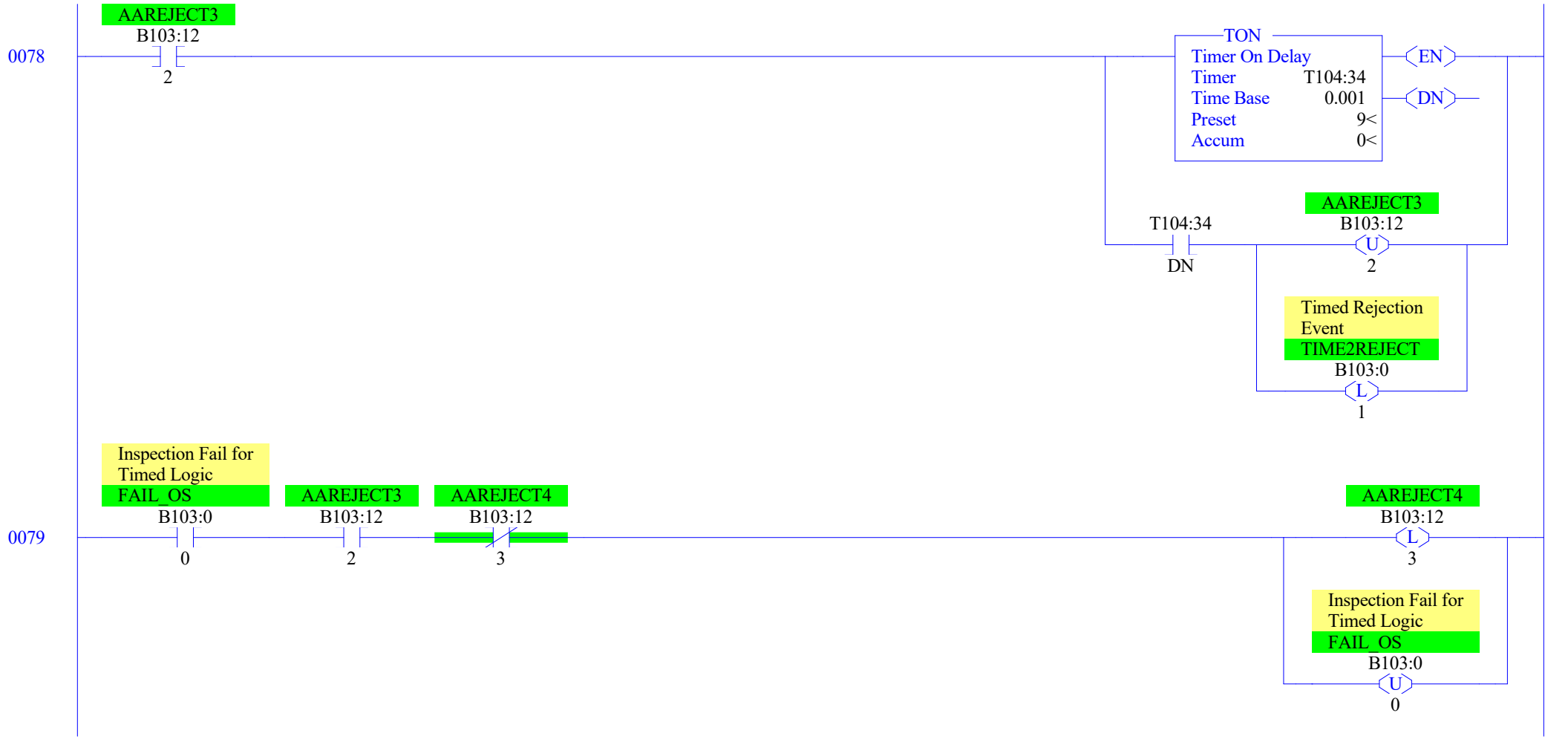

0068
AREJECT14
B103:11
13
TON
Timer On Delay
Timer T104:29
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:29
DN
AREJECT14
B103:11
U
13
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0069
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AREJECT14
B103:11
13
AREJECT15
B103:11
14
AREJECT15
B103:11
L
14
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

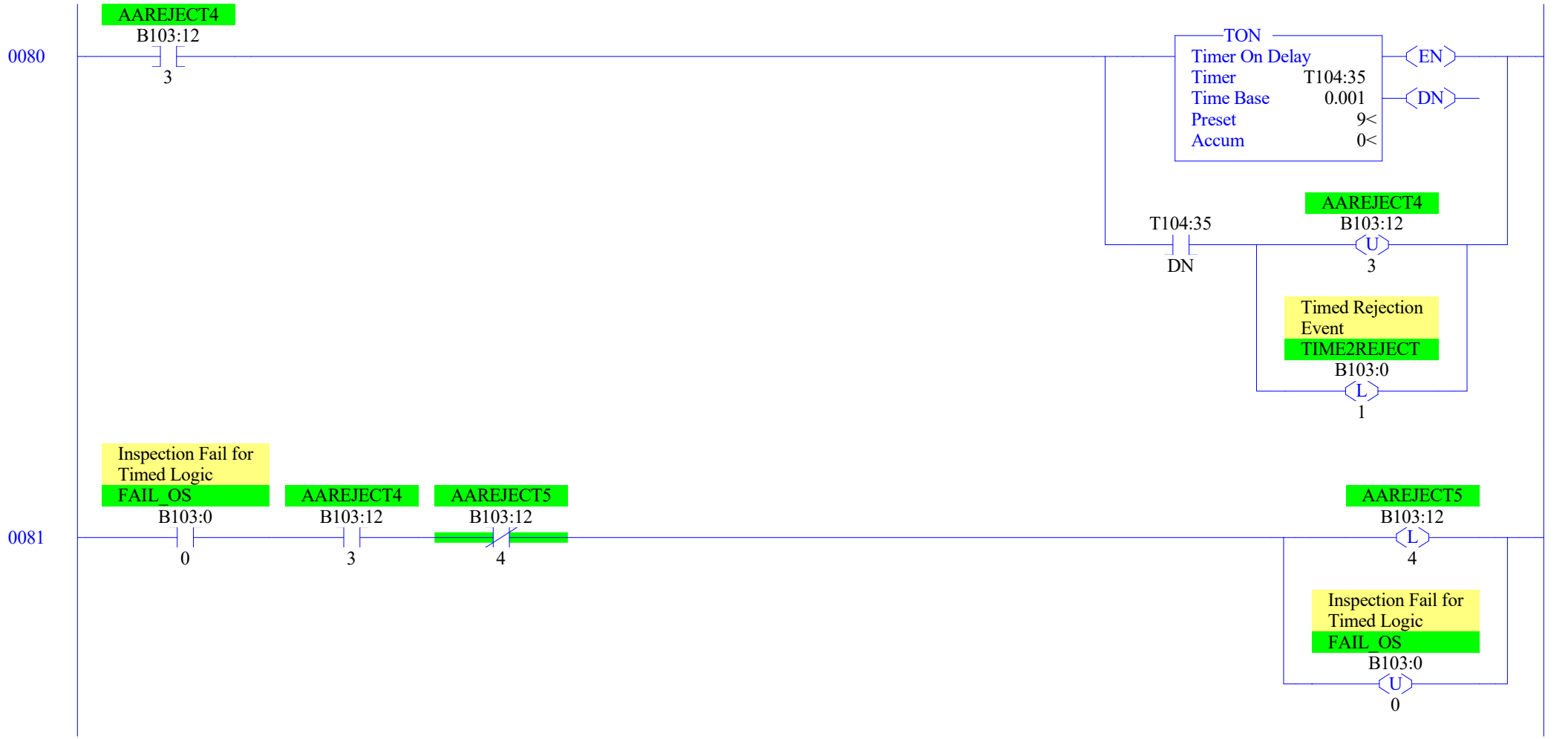

0070
AREJECT15
B103:11
14
TON
Timer On Delay
Timer T104:30
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:30
DN
AREJECT15
B103:11
U
14
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0071
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AREJECT15
B103:11
14
AREJECT16
B103:11
15
AREJECT16
B103:11
L
15
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

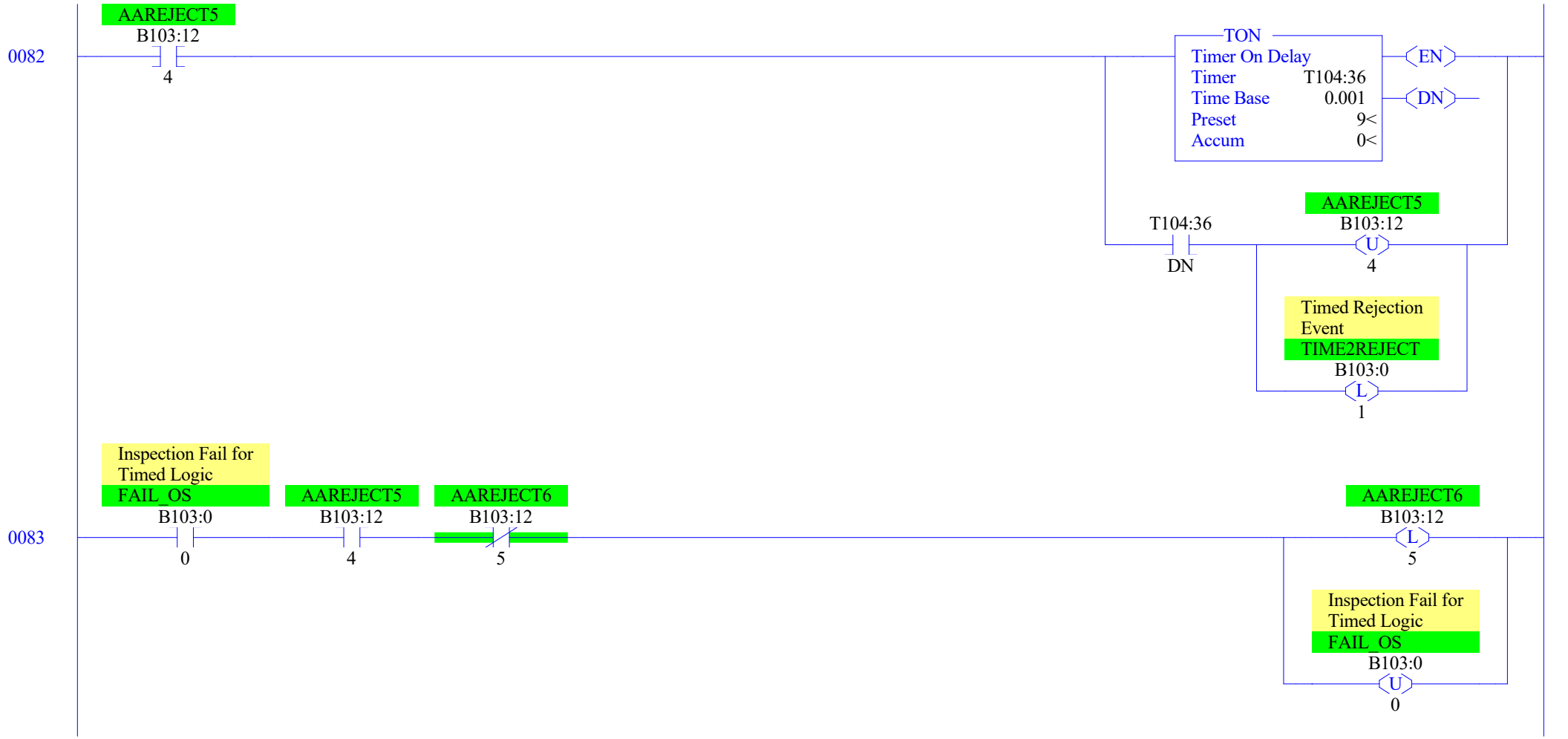

0072
AREJECT16
B103:11
15
TON
Timer On Delay
Timer T104:31
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:31
DN
AREJECT16
B103:11
U
15
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0073
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AREJECT16
B103:11
15
AAREJECT1
B103:12
0
AAREJECT1
B103:12
L
0
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

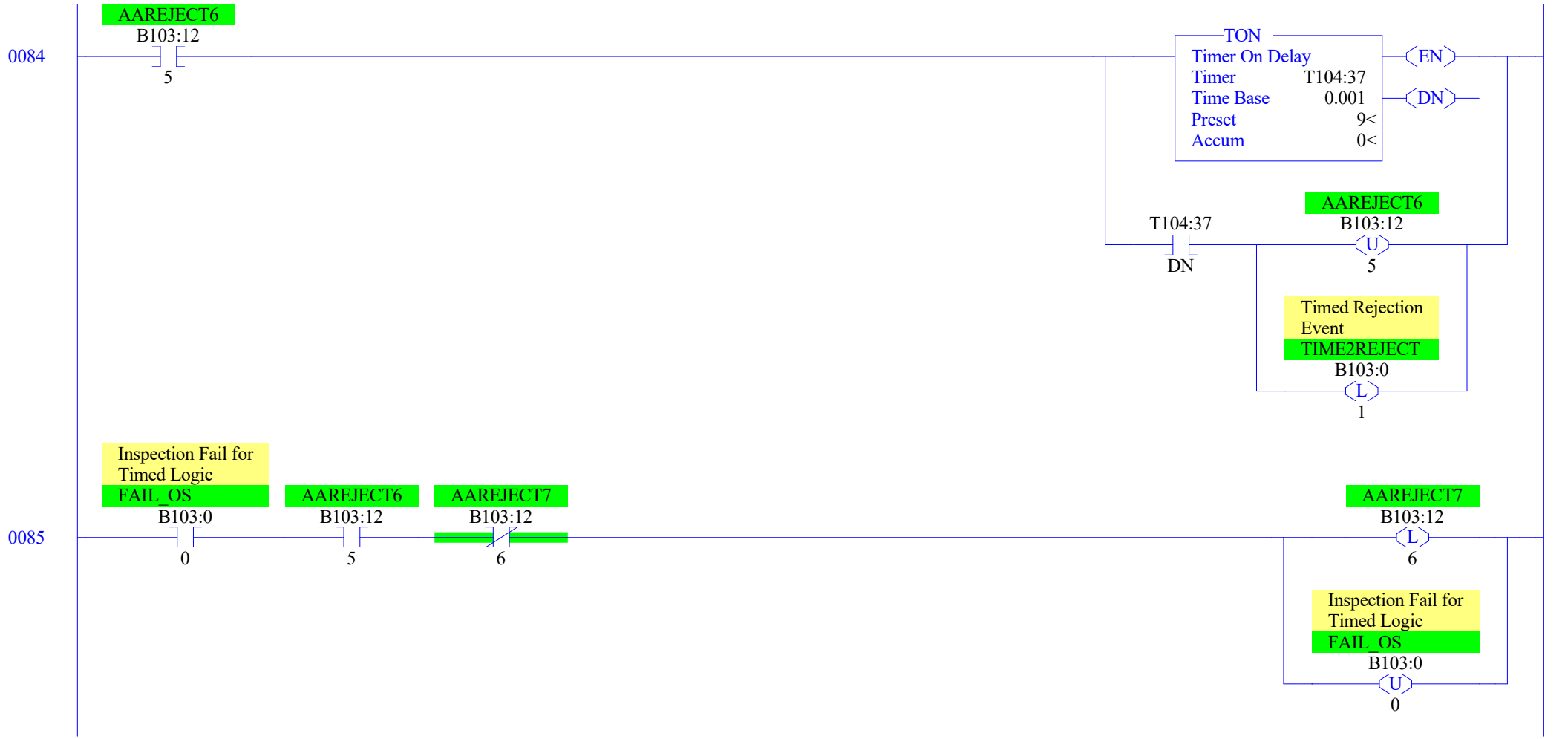

0074
AAREJECT1
B103:12
0
TON
Timer On Delay
Timer T104:32
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:32
DN
AAREJECT1
B103:12
U
0
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0075
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AAREJECT1
B103:12
0
AAREJECT2
B103:12
1
AAREJECT2
B103:12
L
1
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

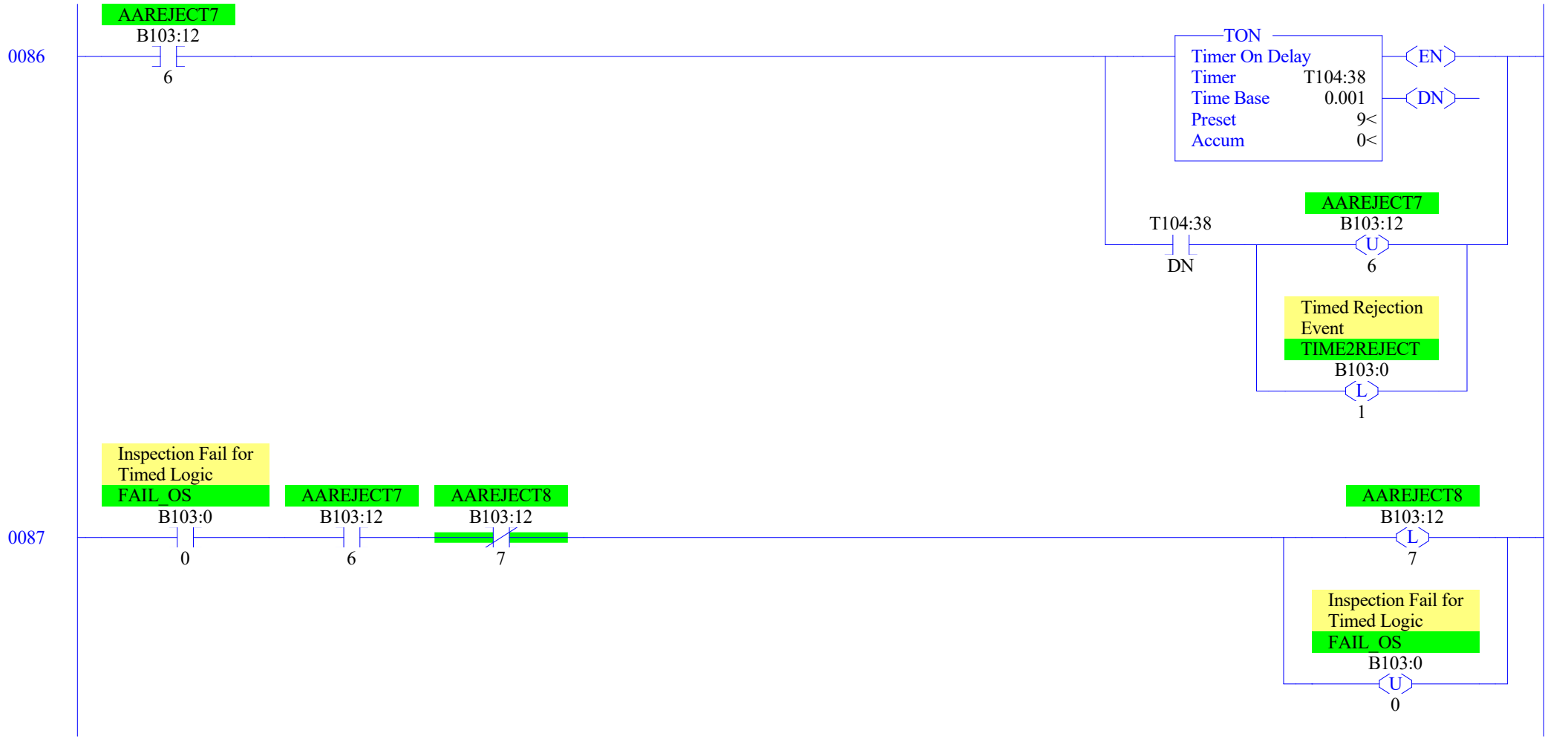

0076
AAREJECT2
B103:12
1
TON
Timer On Delay
Timer T104:33
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:33
DN
AAREJECT2
B103:12
U
1
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0077
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AAREJECT2
B103:12
1
AAREJECT3
B103:12
2
AAREJECT3
B103:12
L
2
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

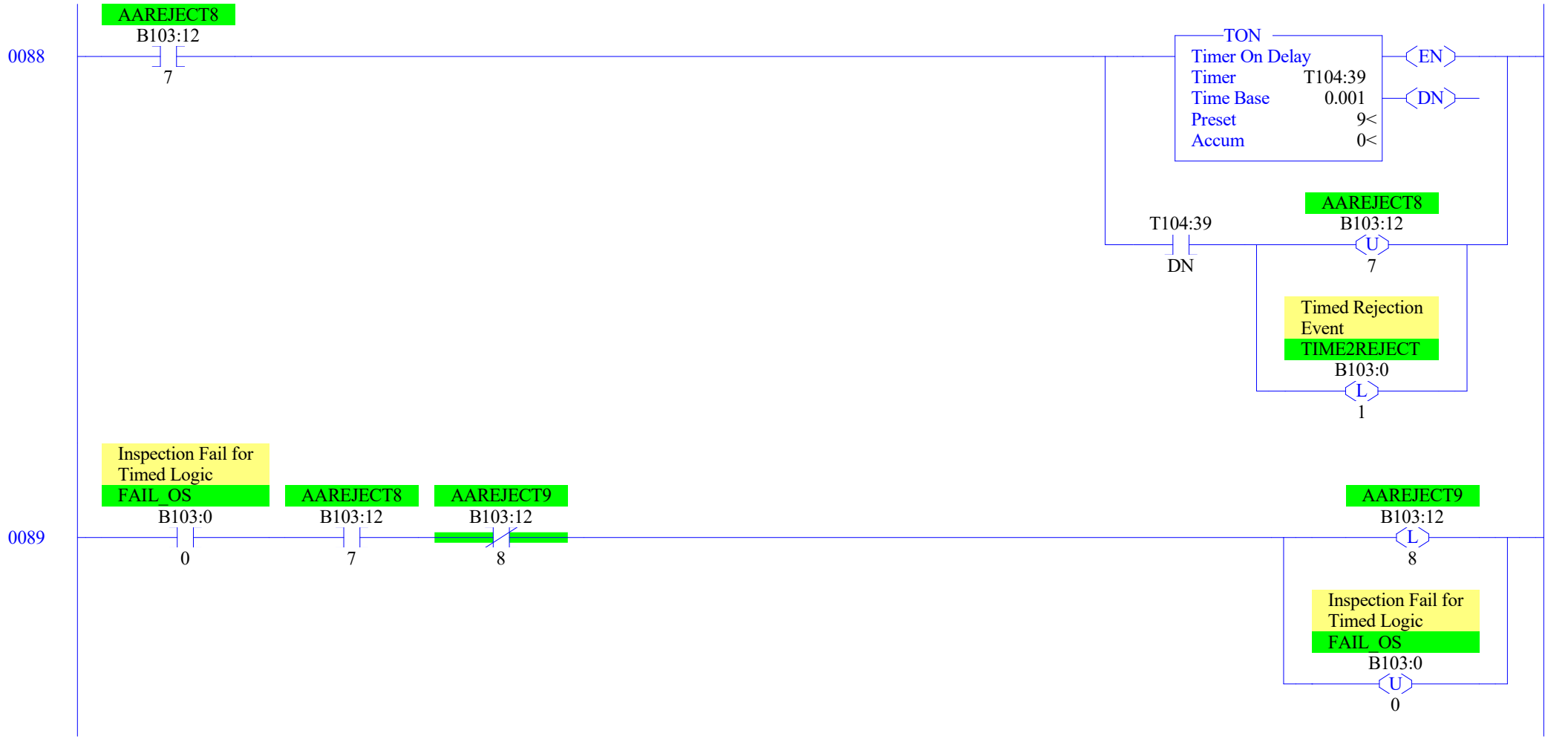

0078
AAREJECT3
B103:12
2
TON
Timer On Delay
Timer T104:34
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:34
DN
AAREJECT3
B103:12
U
2
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0079
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AAREJECT3
B103:12
2
AAREJECT4
B103:12
3
AAREJECT4
B103:12
L
3
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

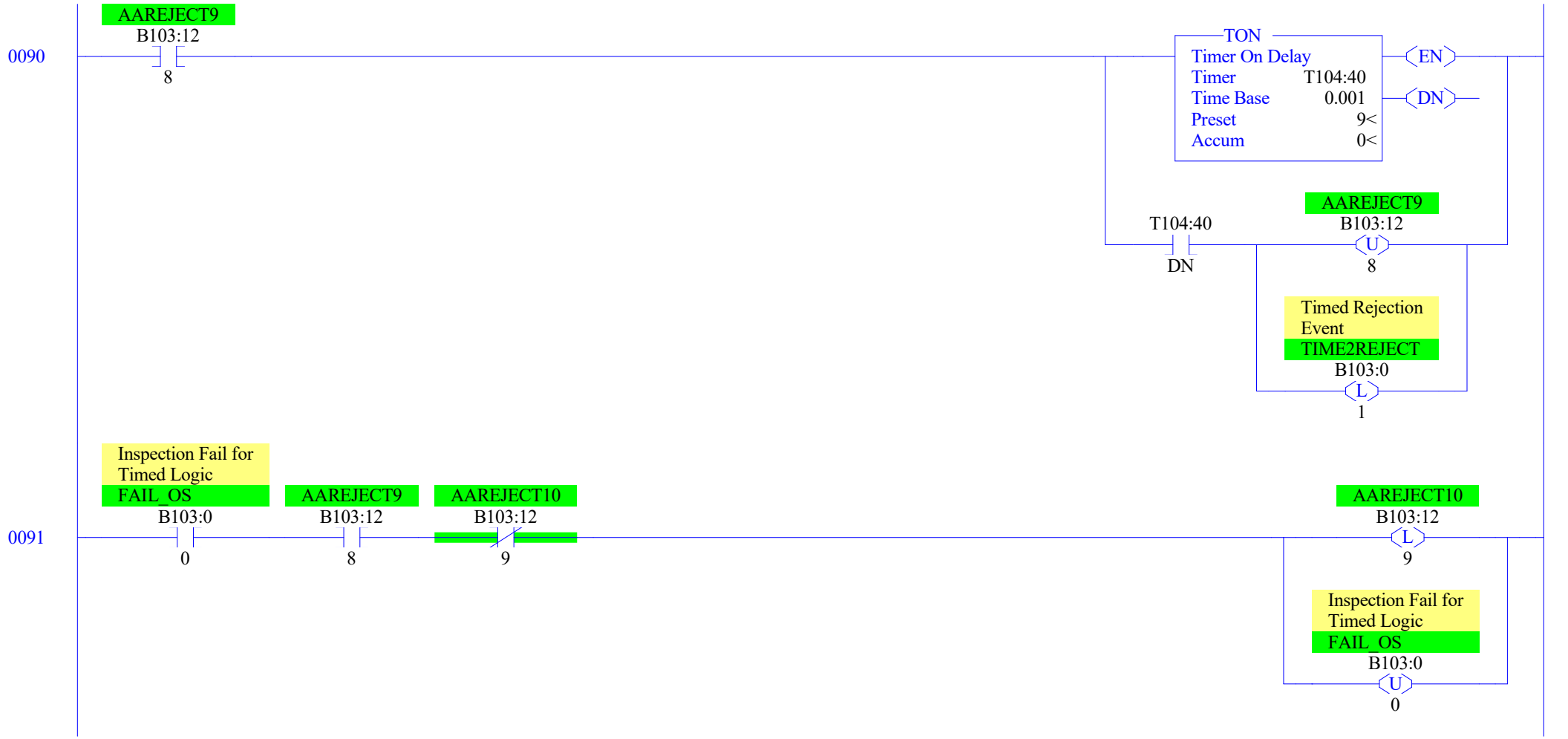

0080
AAREJECT4
B103:12
3
TON
Timer On Delay
Timer T104:35
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:35
DN
AAREJECT4
B103:12
U
3
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0081
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AAREJECT4
B103:12
3
AAREJECT5
B103:12
4
AAREJECT5
B103:12
L
4
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

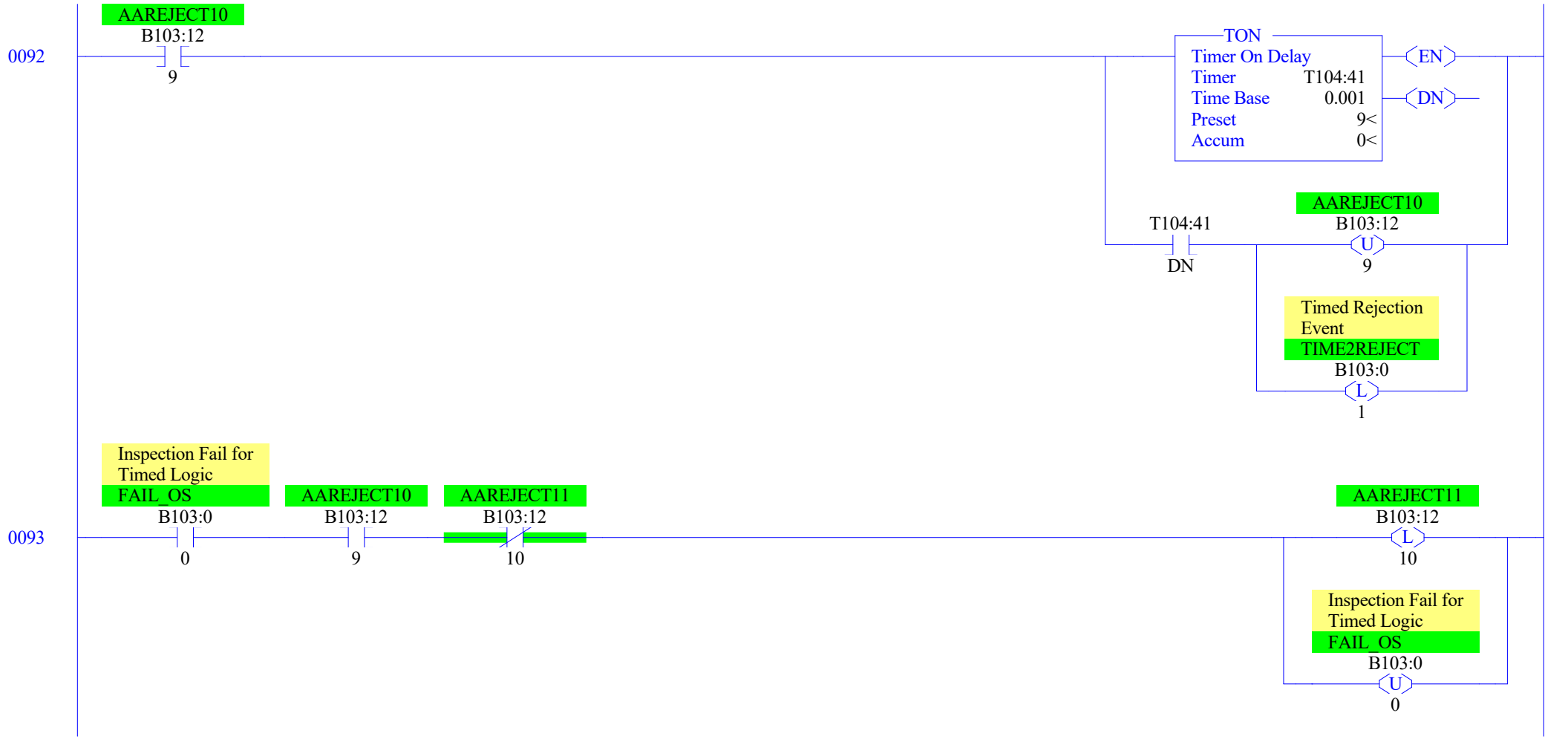

0082
AAREJECT5
B103:12
4
TON
Timer On Delay
Timer T104:36
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:36
DN
AAREJECT5
B103:12
U
4
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0083
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AAREJECT5
B103:12
4
AAREJECT6
B103:12
5
AAREJECT6
B103:12
L
5
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

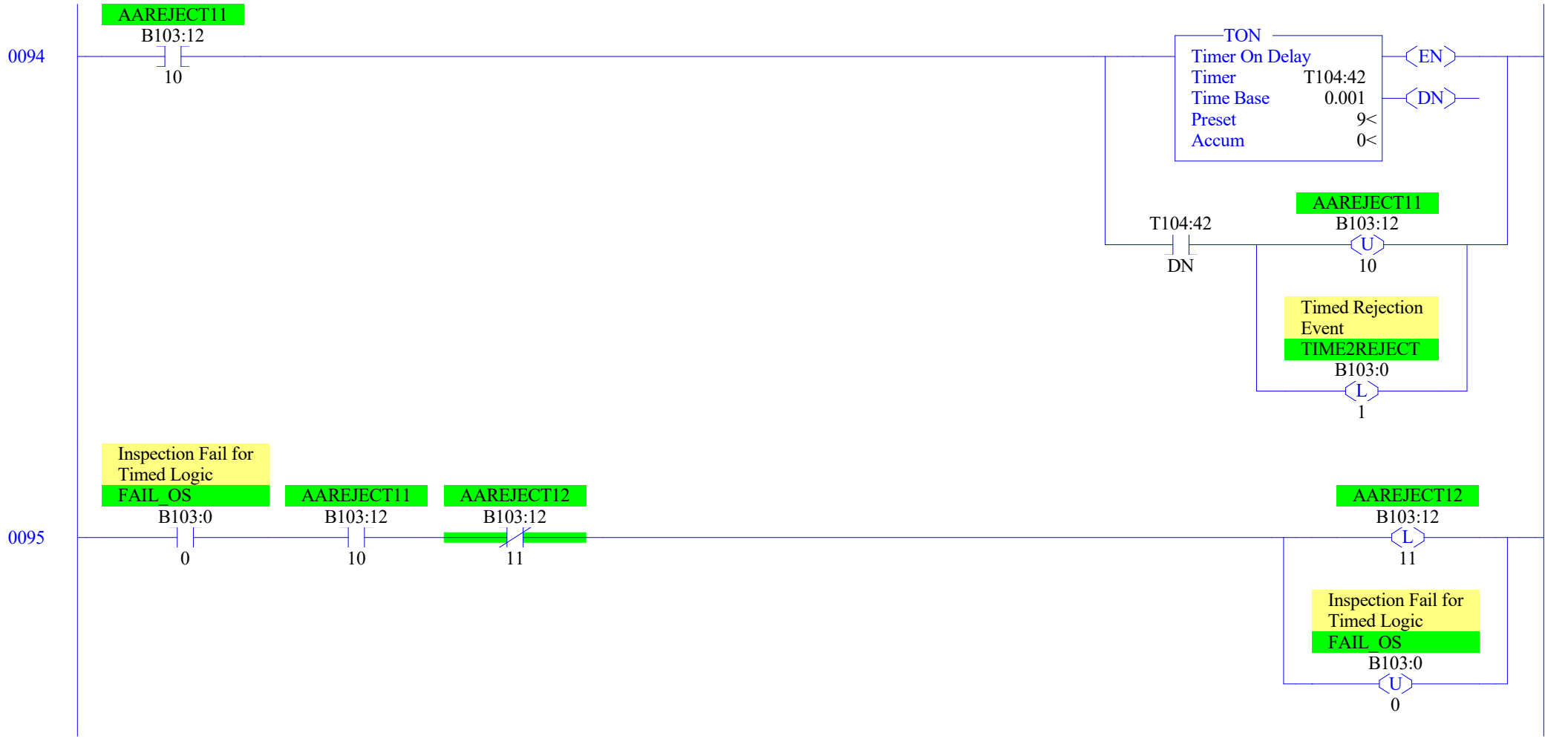

0084
AAREJECT6
B103:12
5
TON
Timer On Delay
Timer T104:37
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:37
DN
AAREJECT6
B103:12
U
5
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0085
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AAREJECT6
B103:12
5
AAREJECT7
B103:12
6
AAREJECT7
B103:12
L
6
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

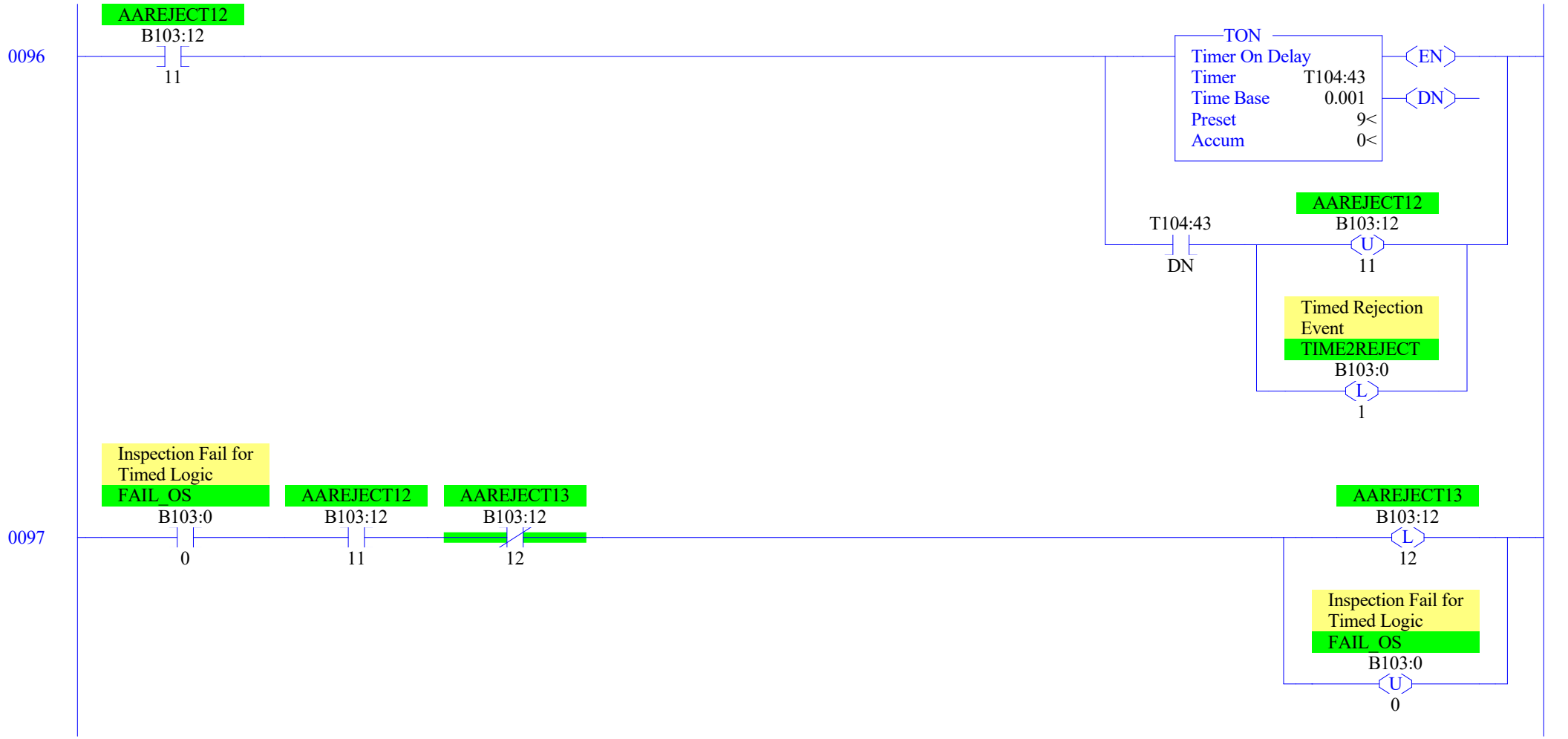

0086
AAREJECT7
B103:12
6
TON
Timer On Delay
Timer T104:38
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:38
DN
AAREJECT7
B103:12
U
6
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0087
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AAREJECT7
B103:12
6
AAREJECT8
B103:12
7
AAREJECT8
B103:12
L
7
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

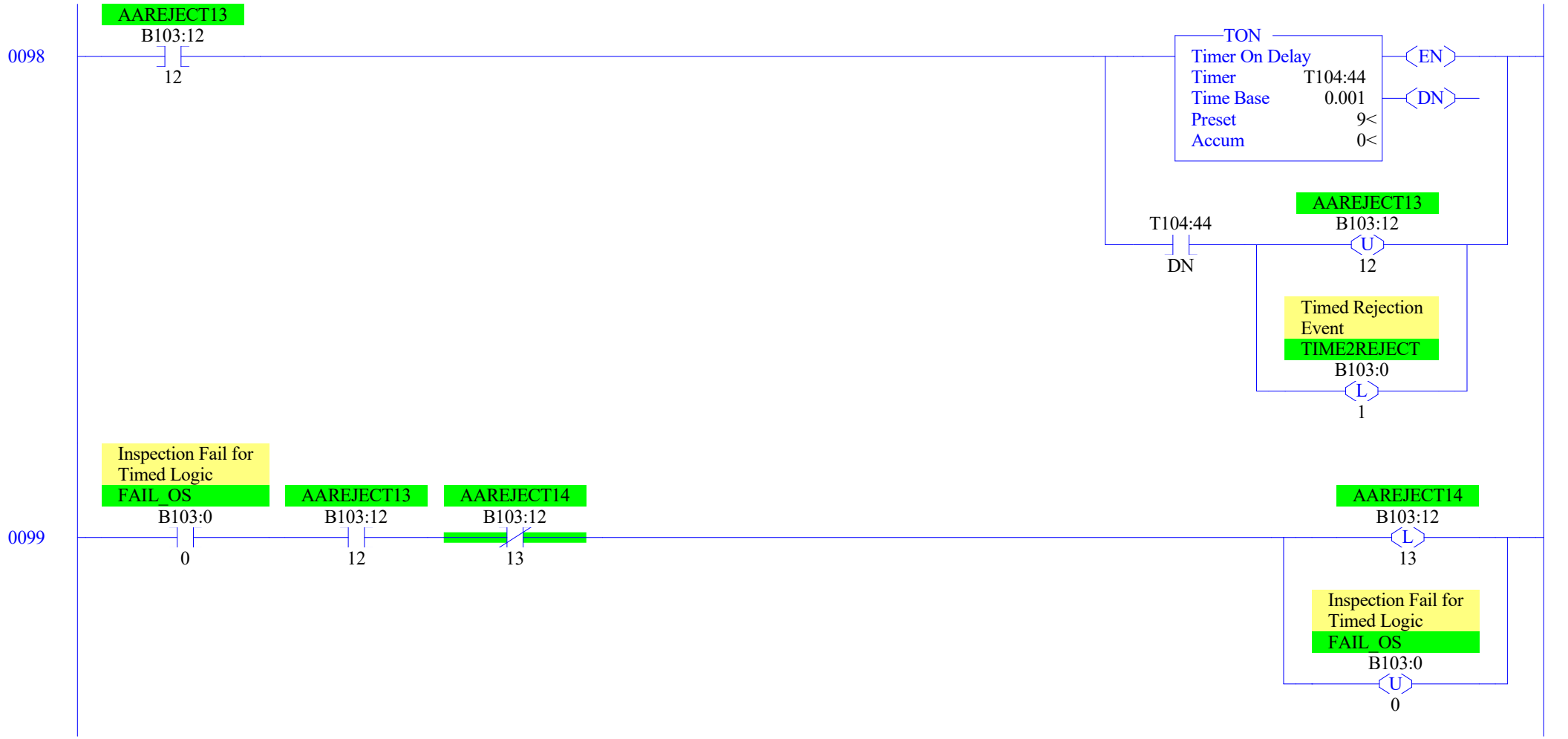

0088
AAREJECT8
B103:12
7
TON
Timer On Delay
Timer T104:39
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:39
DN
AAREJECT8
B103:12
U
7
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0089
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AAREJECT8
B103:12
7
AAREJECT9
B103:12
8
AAREJECT9
B103:12
L
8
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

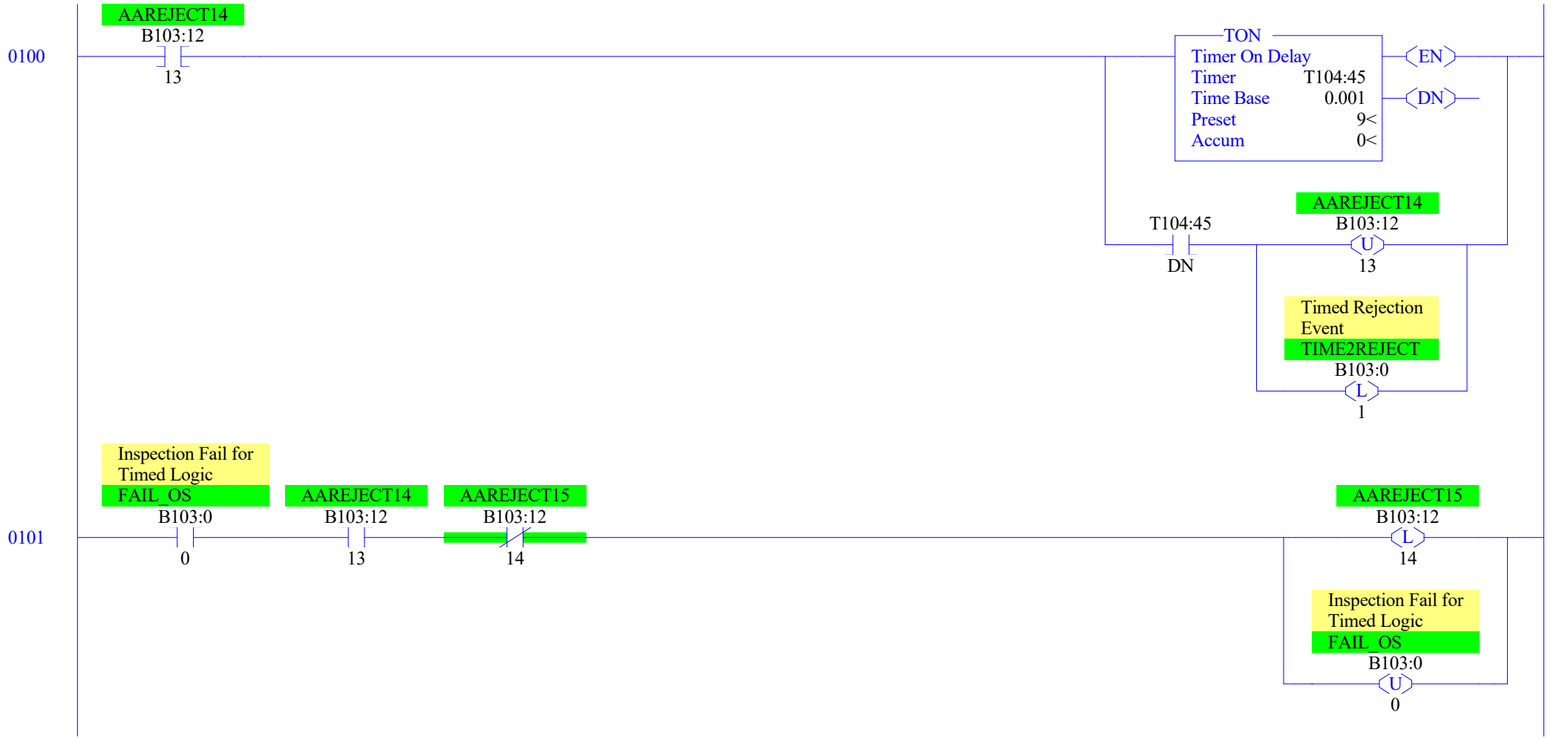

0090
AAREJECT9
B103:12
8
TON
Timer On Delay
Timer T104:40
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:40
DN
AAREJECT9
B103:12
U
8
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0091
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AAREJECT9
B103:12
8
AAREJECT10
B103:12
9
AAREJECT10
B103:12
L
9
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

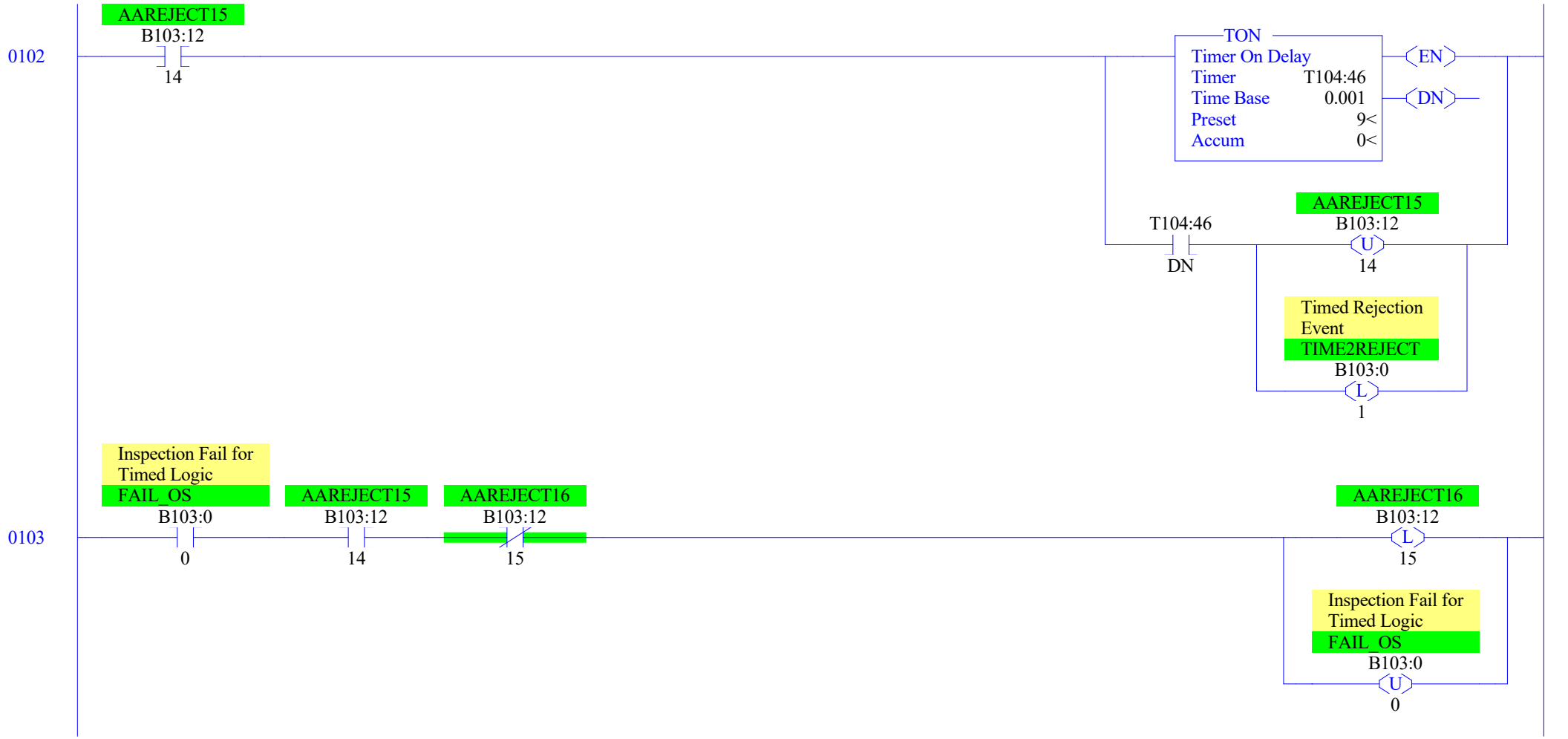

0092
AAREJECT10
B103:12
9
TON
Timer On Delay
Timer T104:41
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:41
DN
AAREJECT10
B103:12
U
9
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0093
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AAREJECT10
B103:12
9
AAREJECT11
B103:12
10
AAREJECT11
B103:12
L
10
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

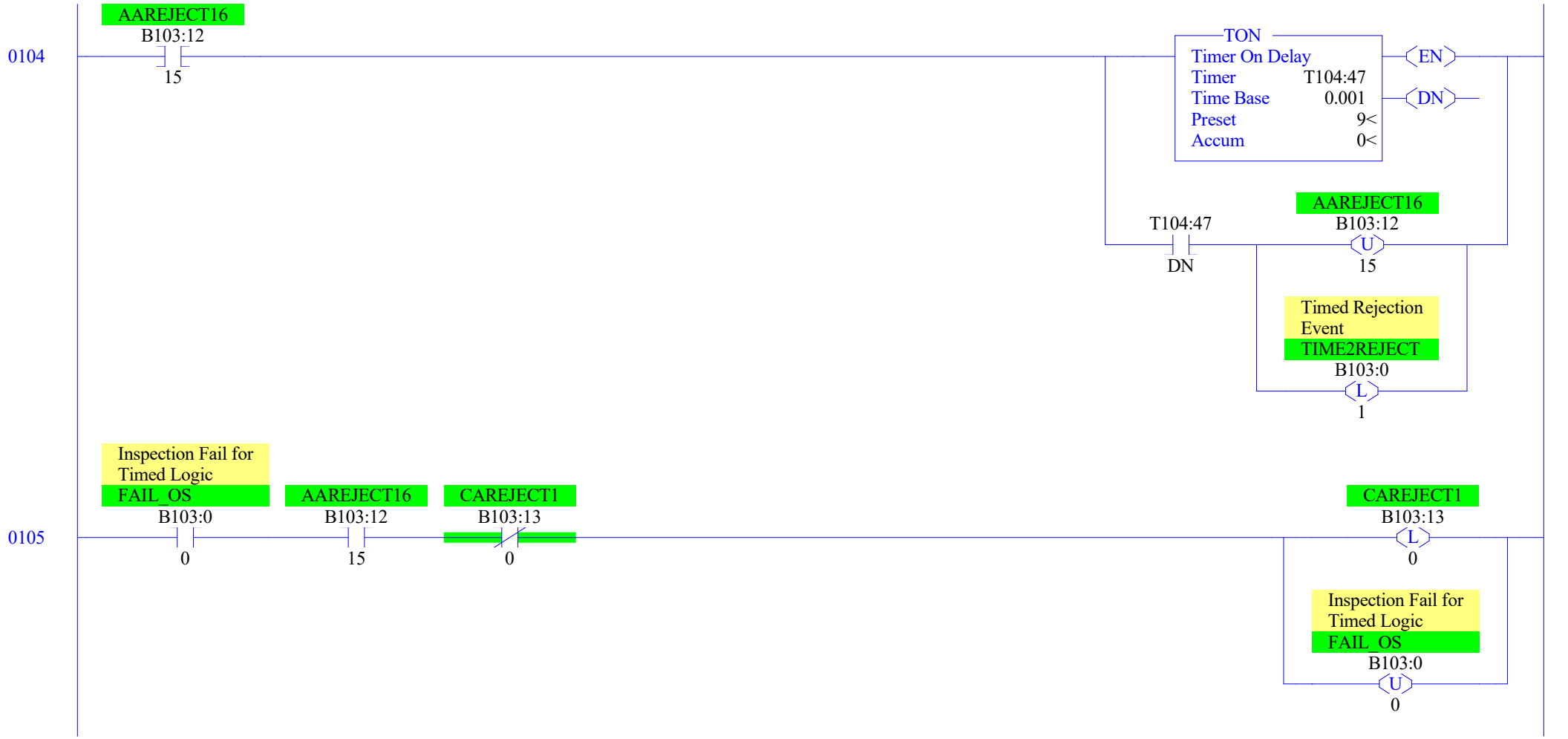

0094
AAREJECT11
B103:12
10
TON
Timer On Delay
Timer T104:42
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:42
DN
AAREJECT11
B103:12
U
10
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0095
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AAREJECT11
B103:12
10
AAREJECT12
B103:12
11
AAREJECT12
B103:12
L
11
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

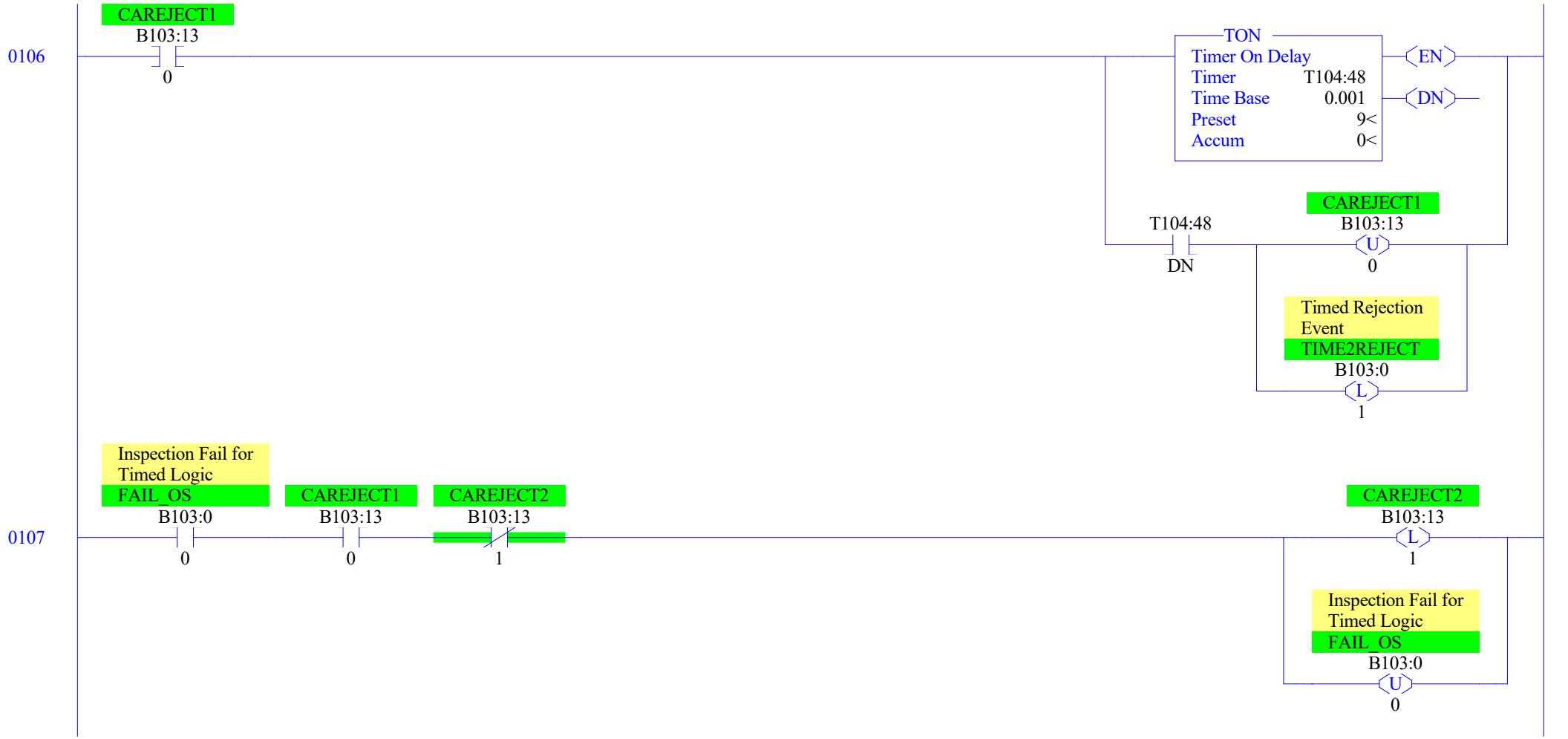

0096
AAREJECT12
B103:12
11
TON
Timer On Delay
Timer T104:43
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:43
DN
AAREJECT12
B103:12
U
11
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0097
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AAREJECT12
B103:12
11
AAREJECT13
B103:12
12
AAREJECT13
B103:12
L
12
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

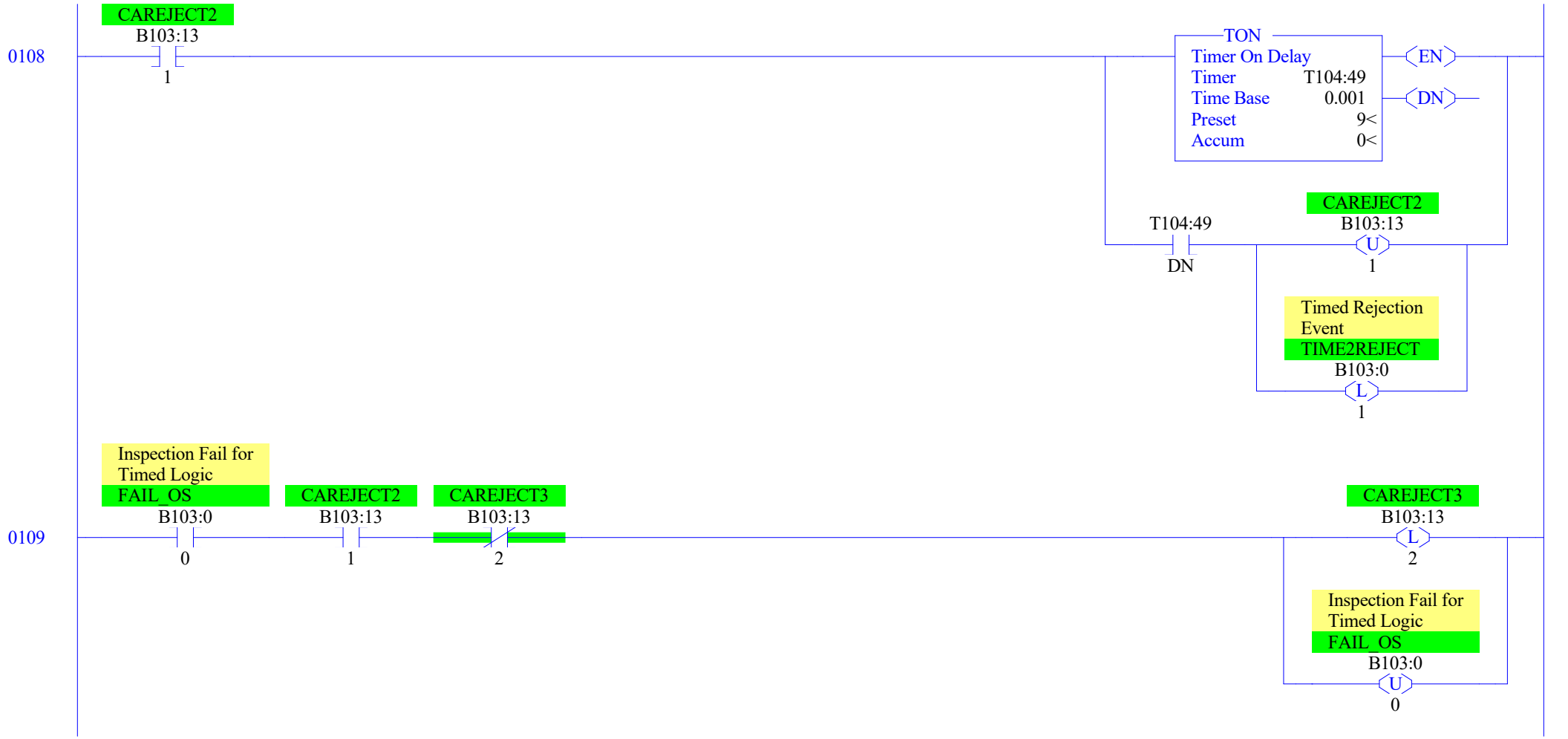

0098
AAREJECT13
B103:12
12
TON
Timer On Delay
Timer T104:44
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:44
DN
AAREJECT13
B103:12
U
12
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0099
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AAREJECT13
B103:12
12
AAREJECT14
B103:12
13
AAREJECT14
B103:12
L
13
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

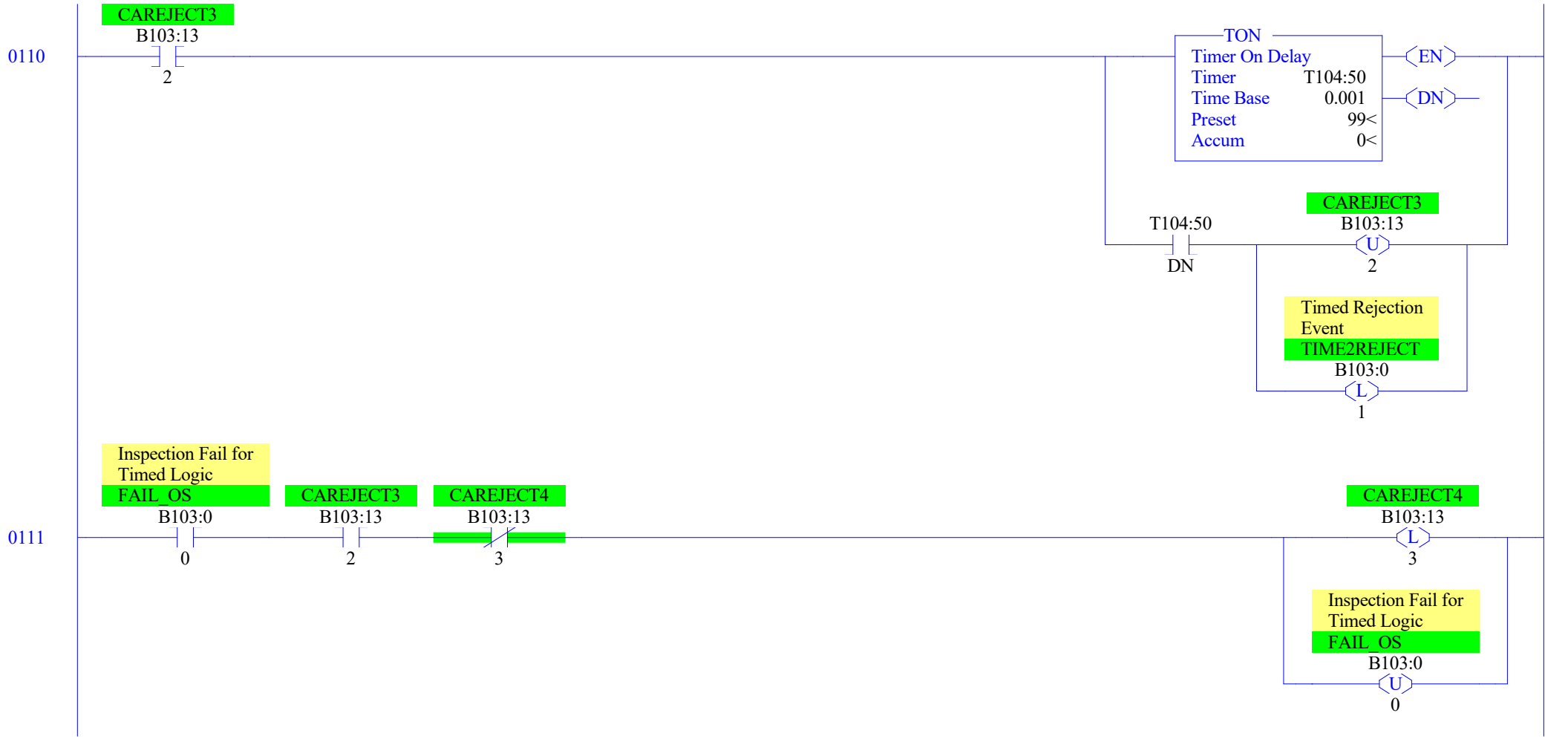

0100
AAREJECT14
B103:12
13
TON
Timer On Delay
Timer T104:45
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:45
DN
AAREJECT14
B103:12
U
13
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0101
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AAREJECT14
B103:12
13
AAREJECT15
B103:12
14
AAREJECT15
B103:12
L
14
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

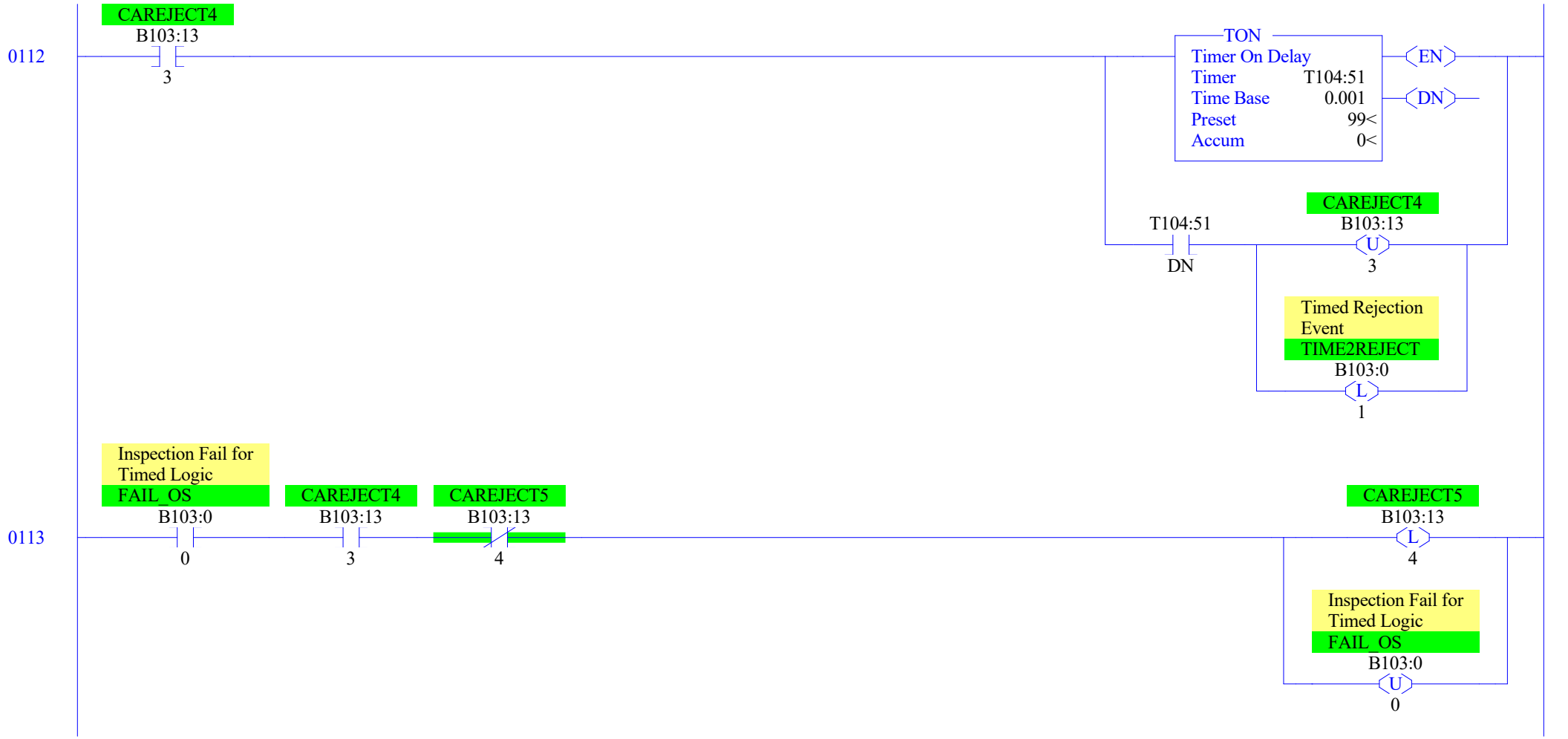

0102
AAREJECT15
B103:12
14
TON
Timer On Delay
Timer T104:46
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:46
DN
AAREJECT15
B103:12
U
14
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0103
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AAREJECT15
B103:12
14
AAREJECT16
B103:12
15
AAREJECT16
B103:12
L
15
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

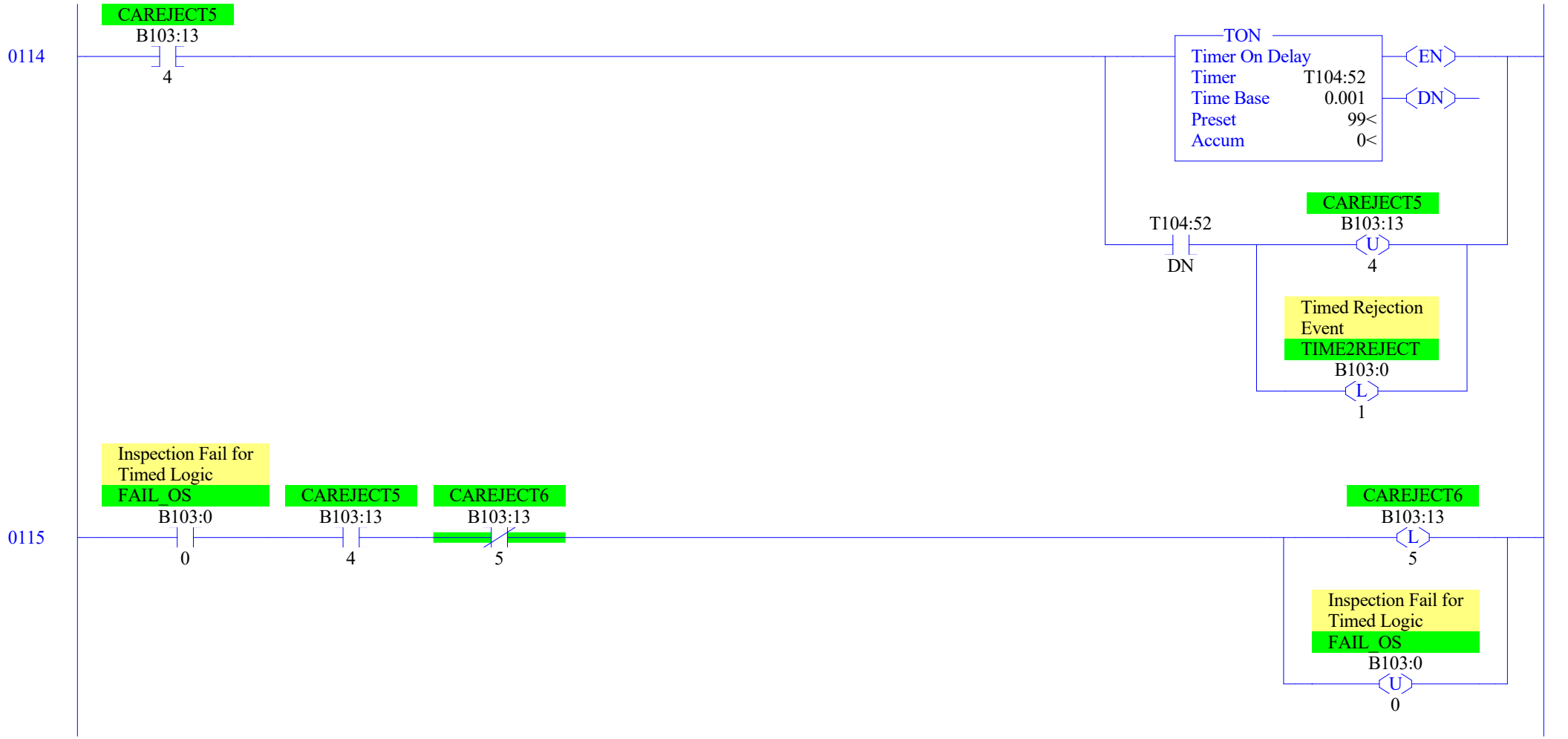

0104
AAREJECT16
B103:12
15
TON
Timer On Delay
Timer T104:47
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:47
DN
AAREJECT16
B103:12
U
15
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0105
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
AAREJECT16
B103:12
15
CAREJECT1
B103:13
0
CAREJECT1
B103:13
L
0
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0


0106
CAREJECT1
B103:13
0
TON
Timer On Delay
Timer T104:48
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:48
DN
CAREJECT1
B103:13
U
0
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0107
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
CAREJECT1
B103:13
0
CAREJECT2
B103:13
1
CAREJECT2
B103:13
L
1
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

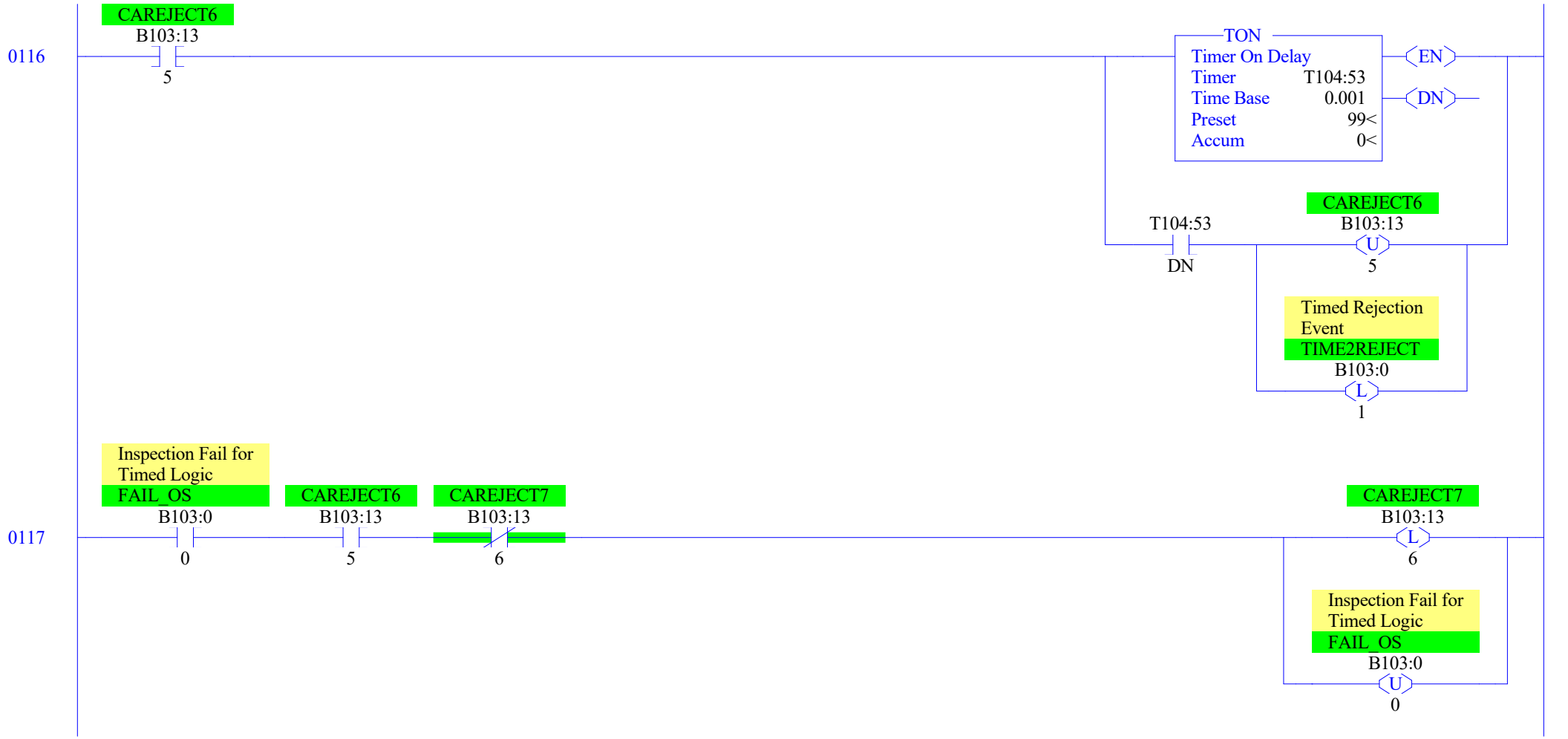

0108
CAREJECT2
B103:13
1
TON
Timer On Delay
Timer T104:49
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:49
DN
CAREJECT2
B103:13
U
1
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0109
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
CAREJECT2
B103:13
1
CAREJECT3
B103:13
2
CAREJECT3
B103:13
L
2
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

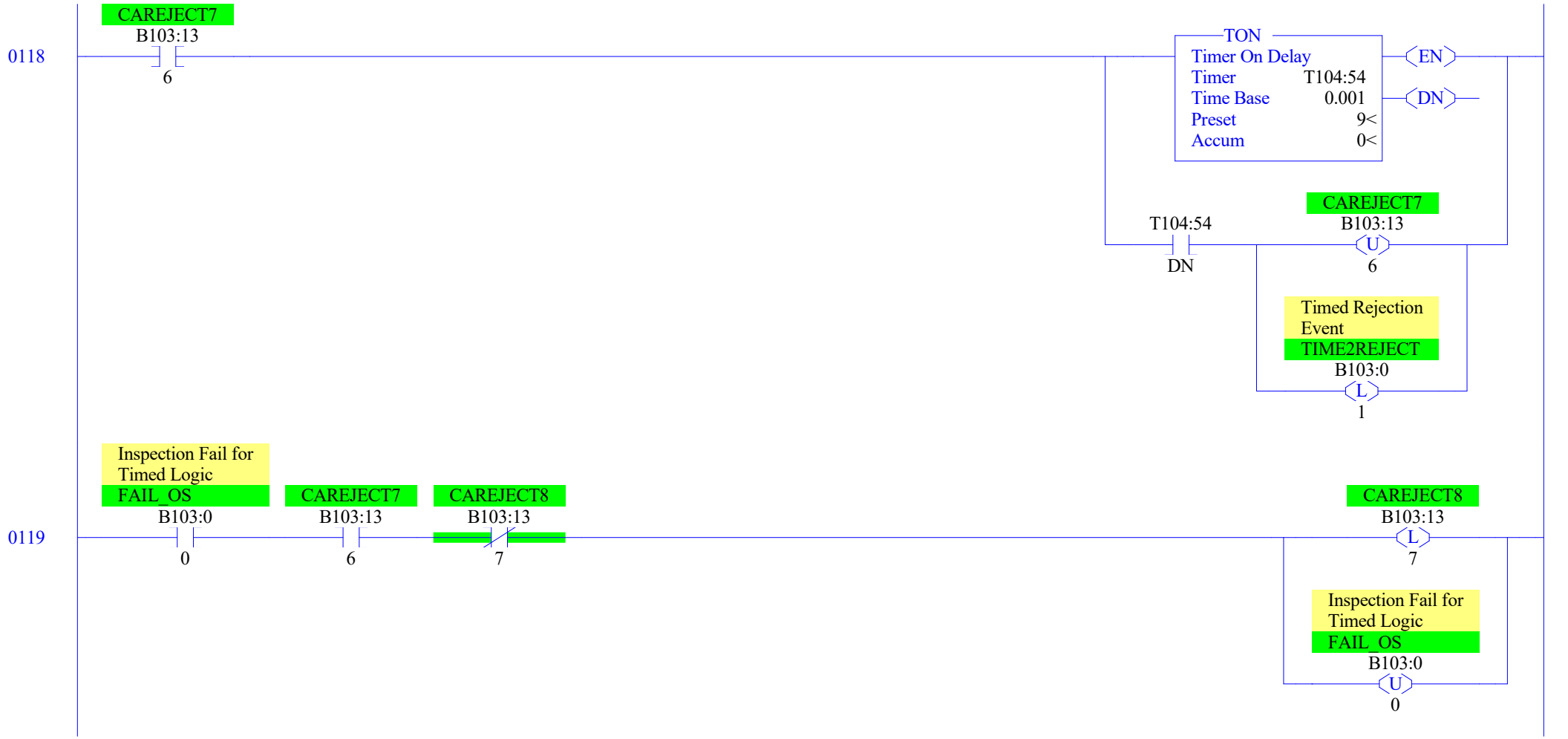

0110
CAREJECT3
B103:13
2
TON
Timer On Delay
Timer T104:50
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:50
DN
CAREJECT3
B103:13
U
2
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0111
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
CAREJECT3
B103:13
2
CAREJECT4
B103:13
3
CAREJECT4
B103:13
L
3
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

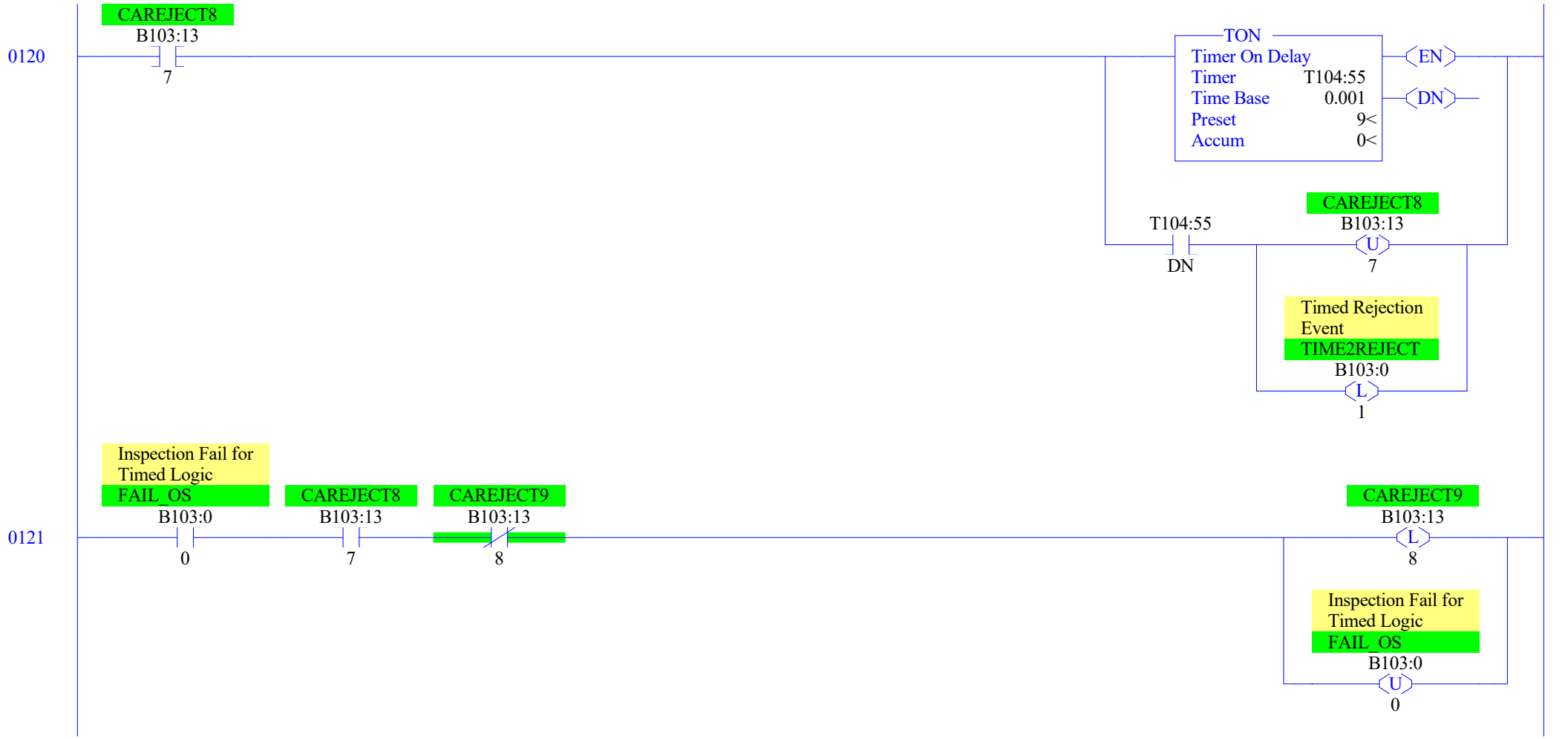

0112
CAREJECT4
B103:13
3
TON
Timer On Delay
Timer T104:51
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:51
DN
CAREJECT4
B103:13
U
3
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0113
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
CAREJECT4
B103:13
3
CAREJECT5
B103:13
4
CAREJECT5
B103:13
L
4
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

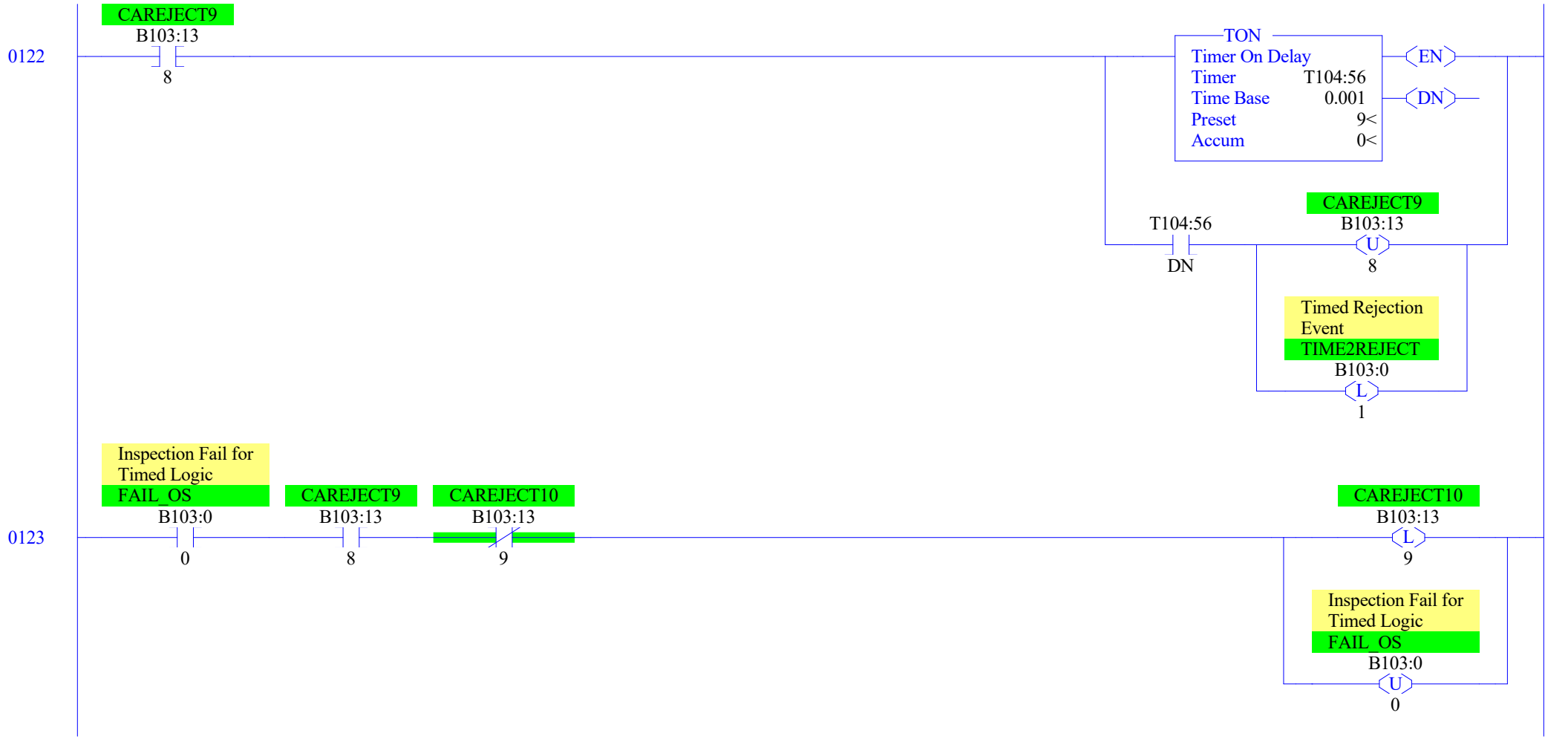

0114
CAREJECT5
B103:13
4
TON
Timer On Delay
Timer T104:52
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:52
DN
CAREJECT5
B103:13
U
4
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0115
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
CAREJECT5
B103:13
4
CAREJECT6
B103:13
5
CAREJECT6
B103:13
L
5
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

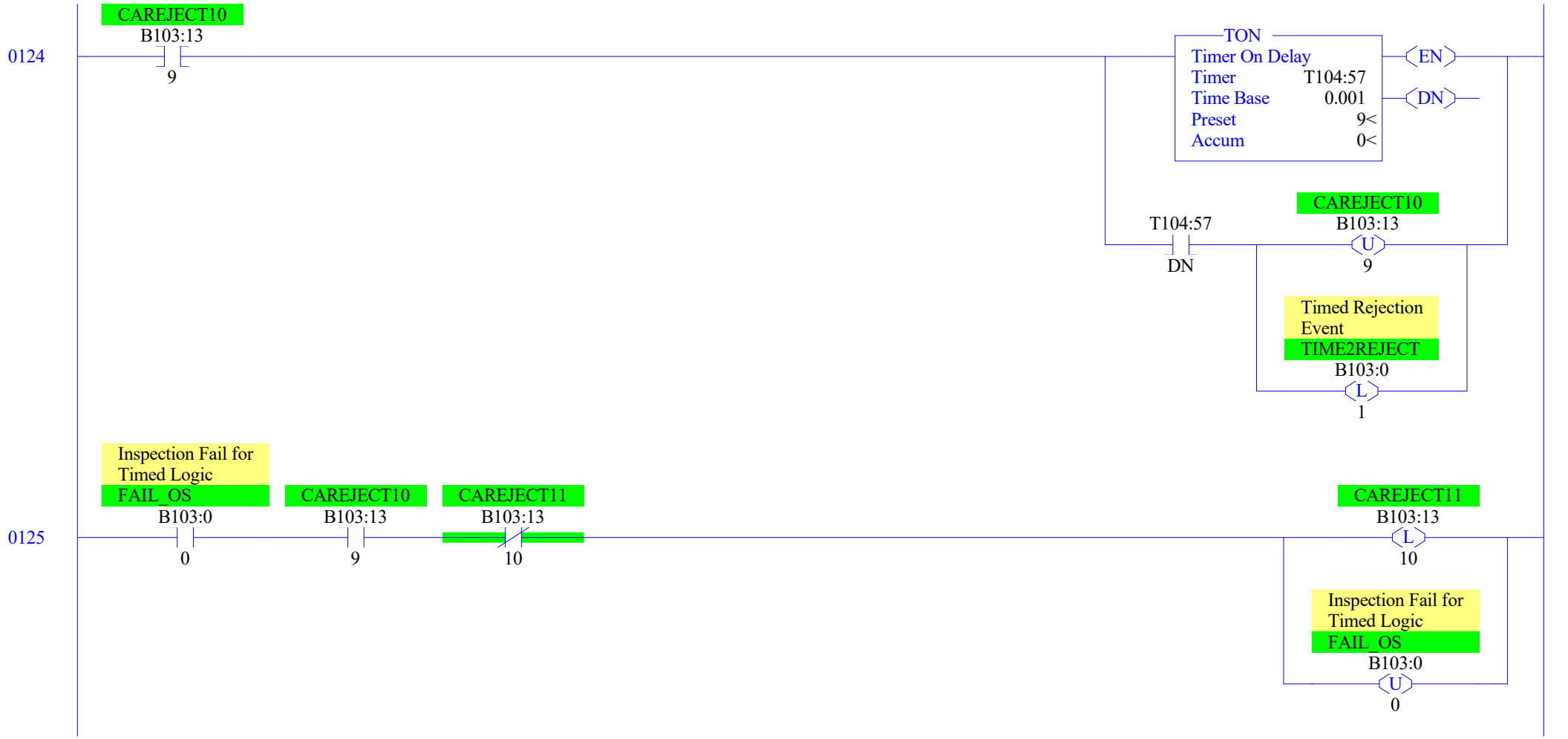
LAD 9 - REJ TIMERS --- Total Rungs in File = 235

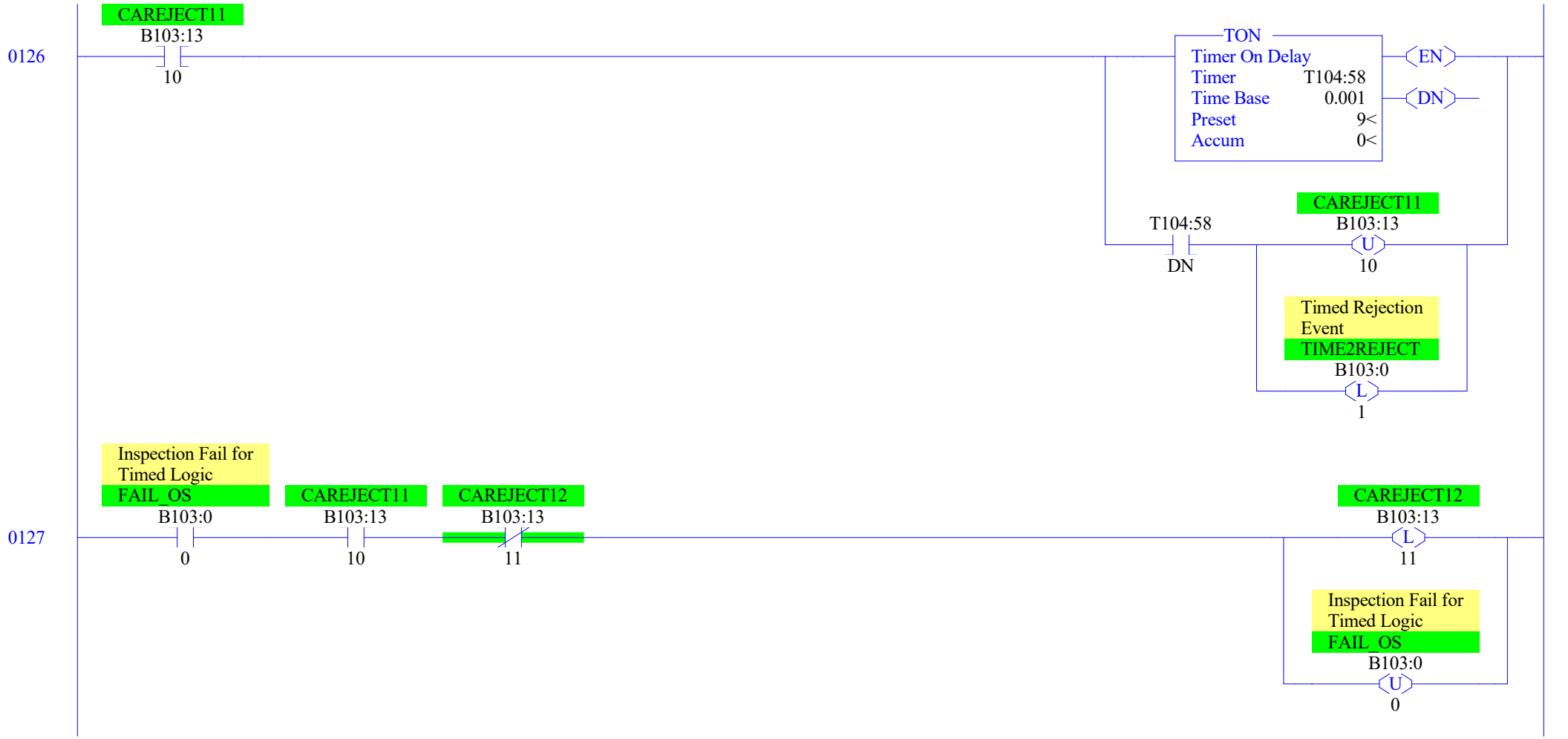


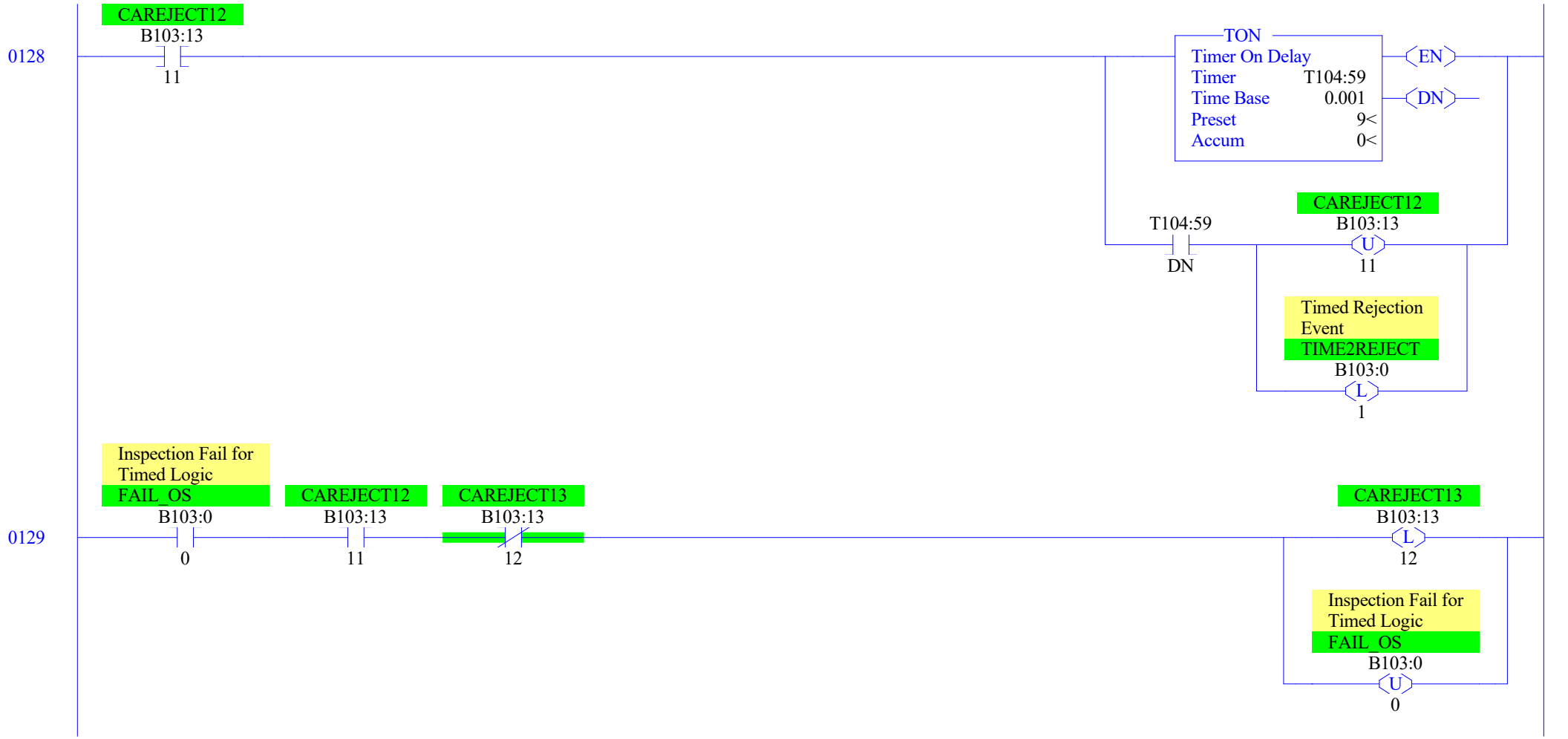

0118
CAREJECT7
B103:13
6
TON
Timer On Delay
Timer T104:54
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:54
DN
CAREJECT7
B103:13
U
6
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0119
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
CAREJECT7
B103:13
6
CAREJECT8
B103:13
7
CAREJECT8
B103:13
L
7
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

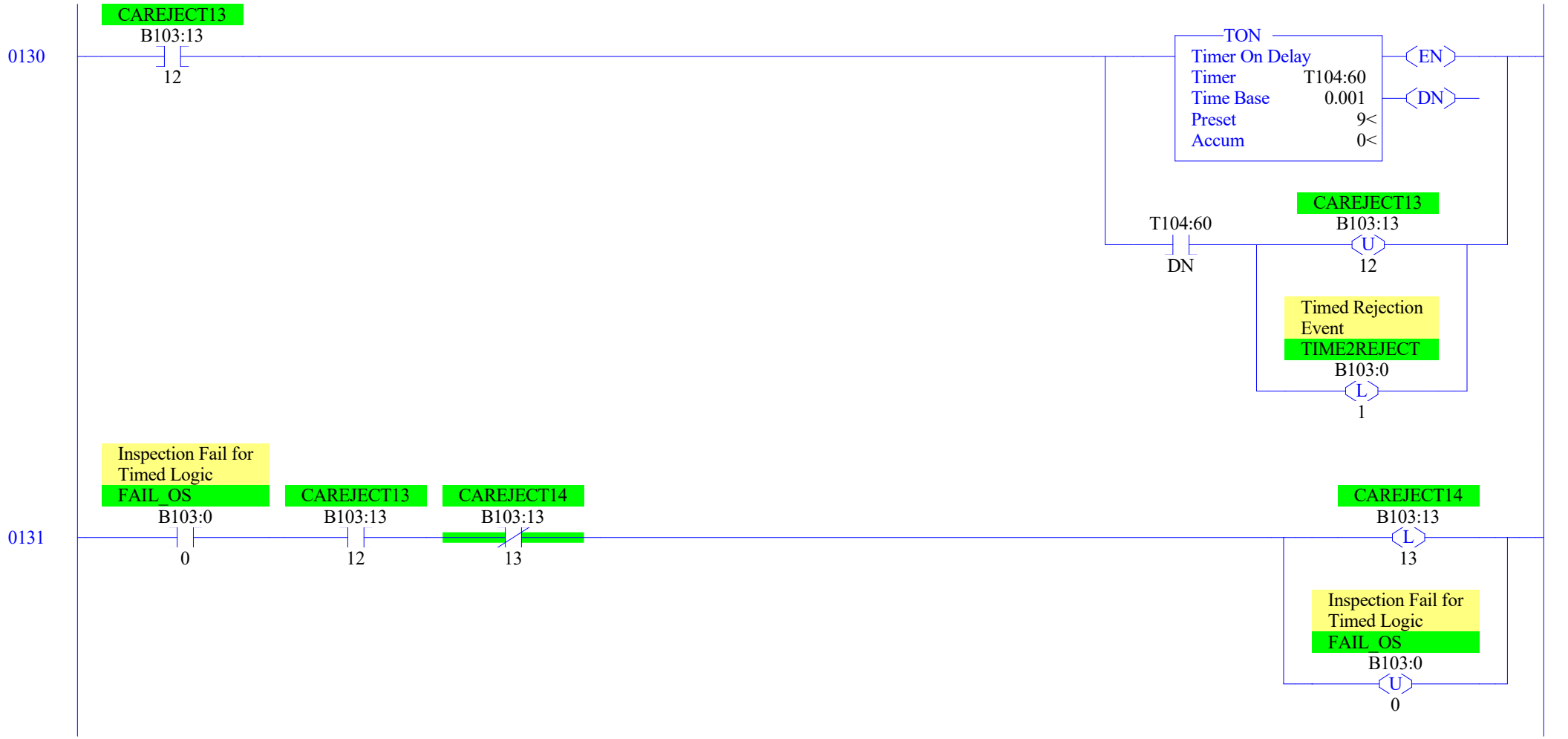

0120
CAREJECT8
B103:13
7
TON
Timer On Delay
Timer T104:55
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:55
DN
CAREJECT8
B103:13
U
7
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0121
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
CAREJECT8
B103:13
7
CAREJECT9
B103:13
8
CAREJECT9
B103:13
L
8
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

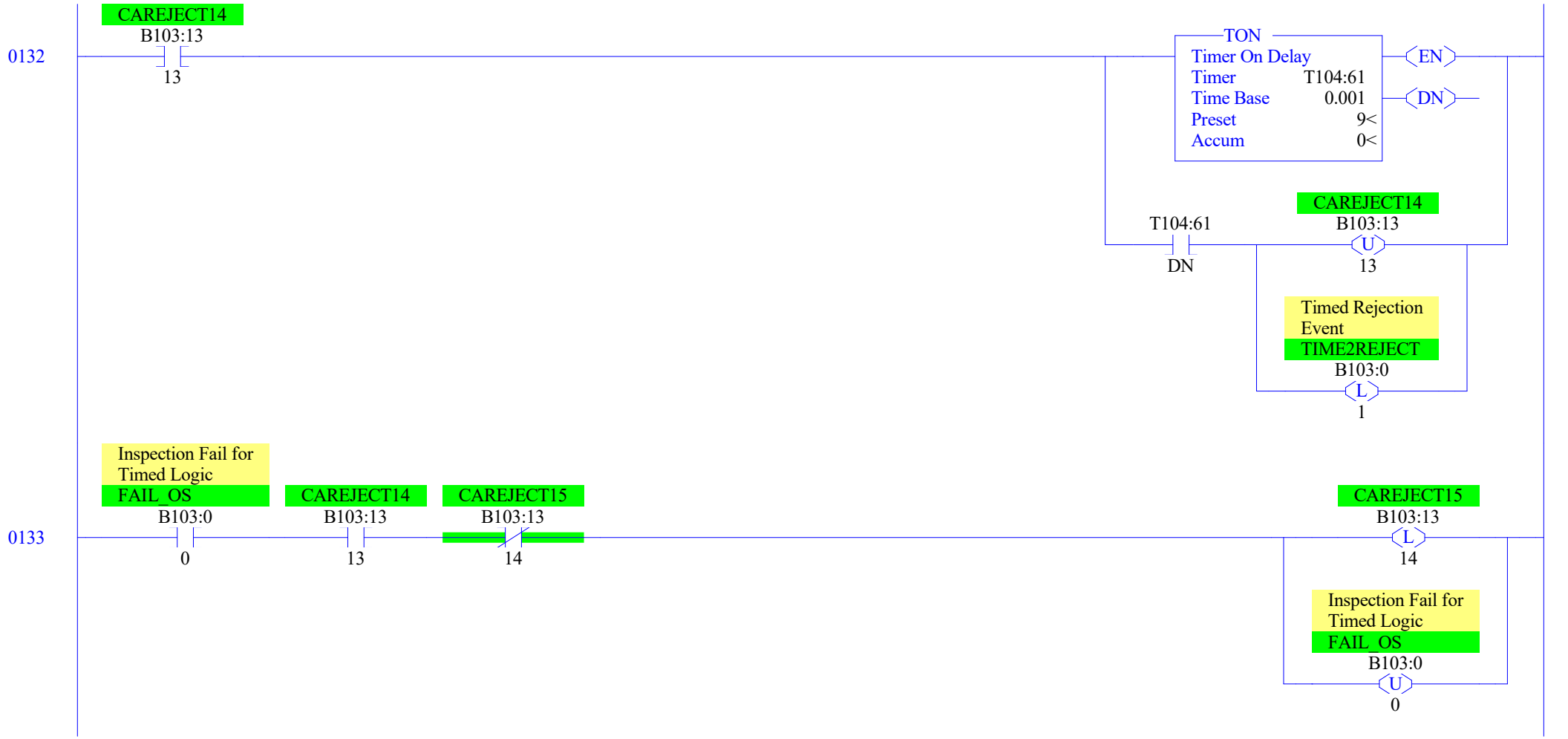

0122
CAREJECT9
B103:13
8
TON
Timer On Delay
Timer T104:56
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:56
DN
CAREJECT9
B103:13
U
8
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0123
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
CAREJECT9
B103:13
8
CAREJECT10
B103:13
9
CAREJECT10
B103:13
L
9
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

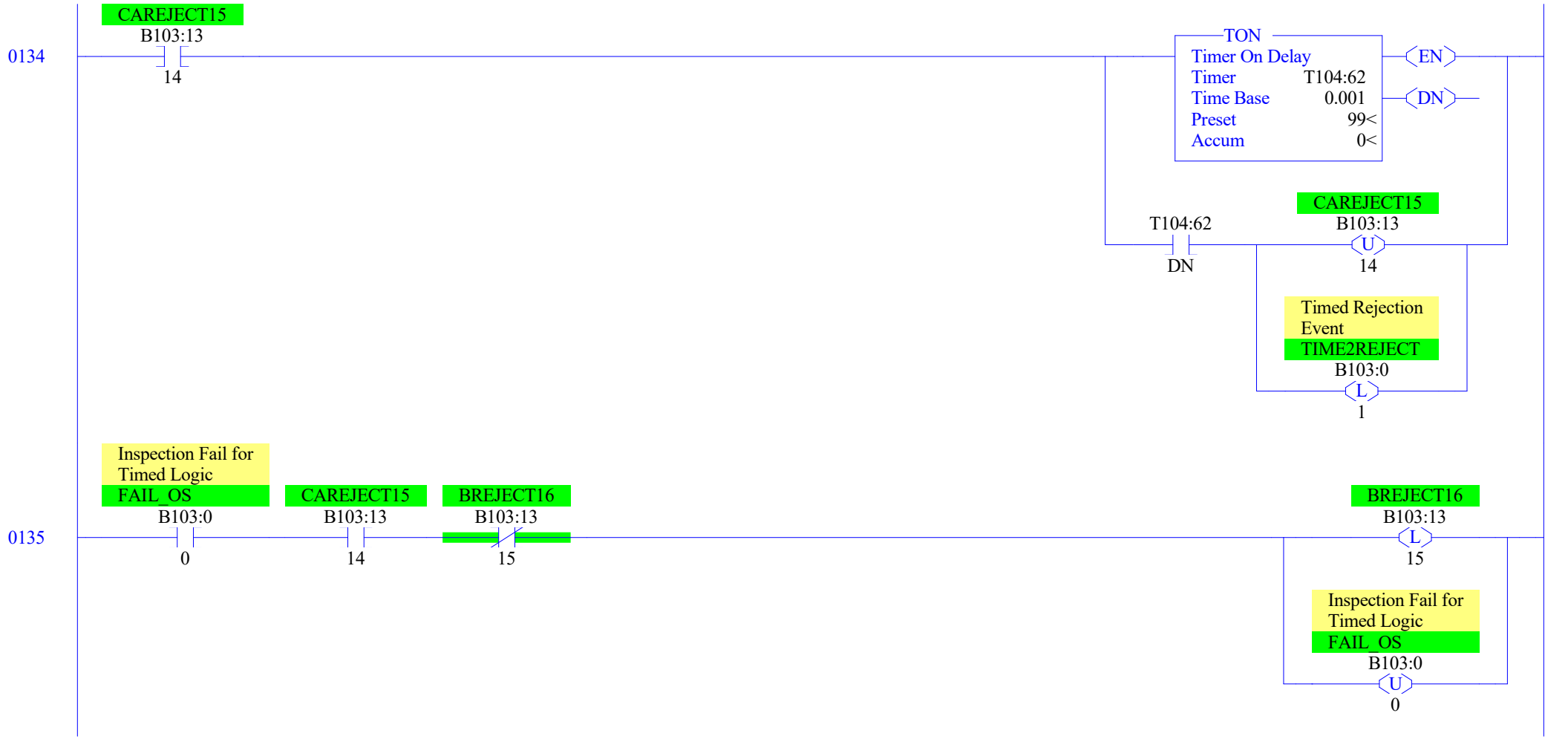

0124
CAREJECT10
B103:13
9
TON
Timer On Delay
Timer T104:57
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:57
DN
CAREJECT10
B103:13
U
9
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0125
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
CAREJECT10
B103:13
9
CAREJECT11
B103:13
10
CAREJECT11
B103:13
L
10
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0


0126
CAREJECT11
B103:13
10
TON
Timer On Delay
Timer T104:58
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:58
DN
CAREJECT11
B103:13
U
10
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0127
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
CAREJECT11
B103:13
10
CAREJECT12
B103:13
11
CAREJECT12
B103:13
L
11
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

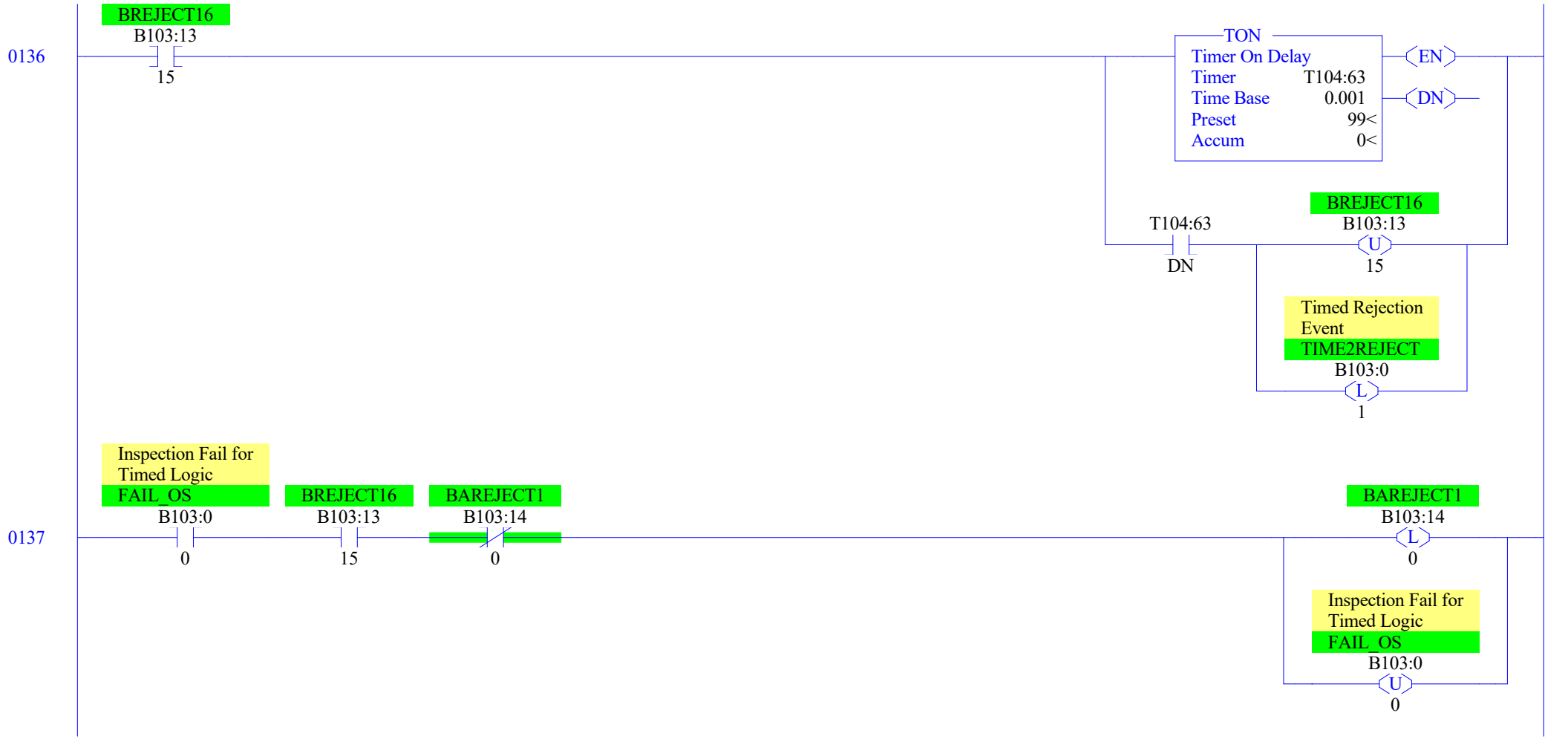

0128
CAREJECT12
B103:13
11
TON
Timer On Delay
Timer T104:59
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:59
DN
CAREJECT12
B103:13
U
11
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0129
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
CAREJECT12
B103:13
11
CAREJECT13
B103:13
12
CAREJECT13
B103:13
L
12
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

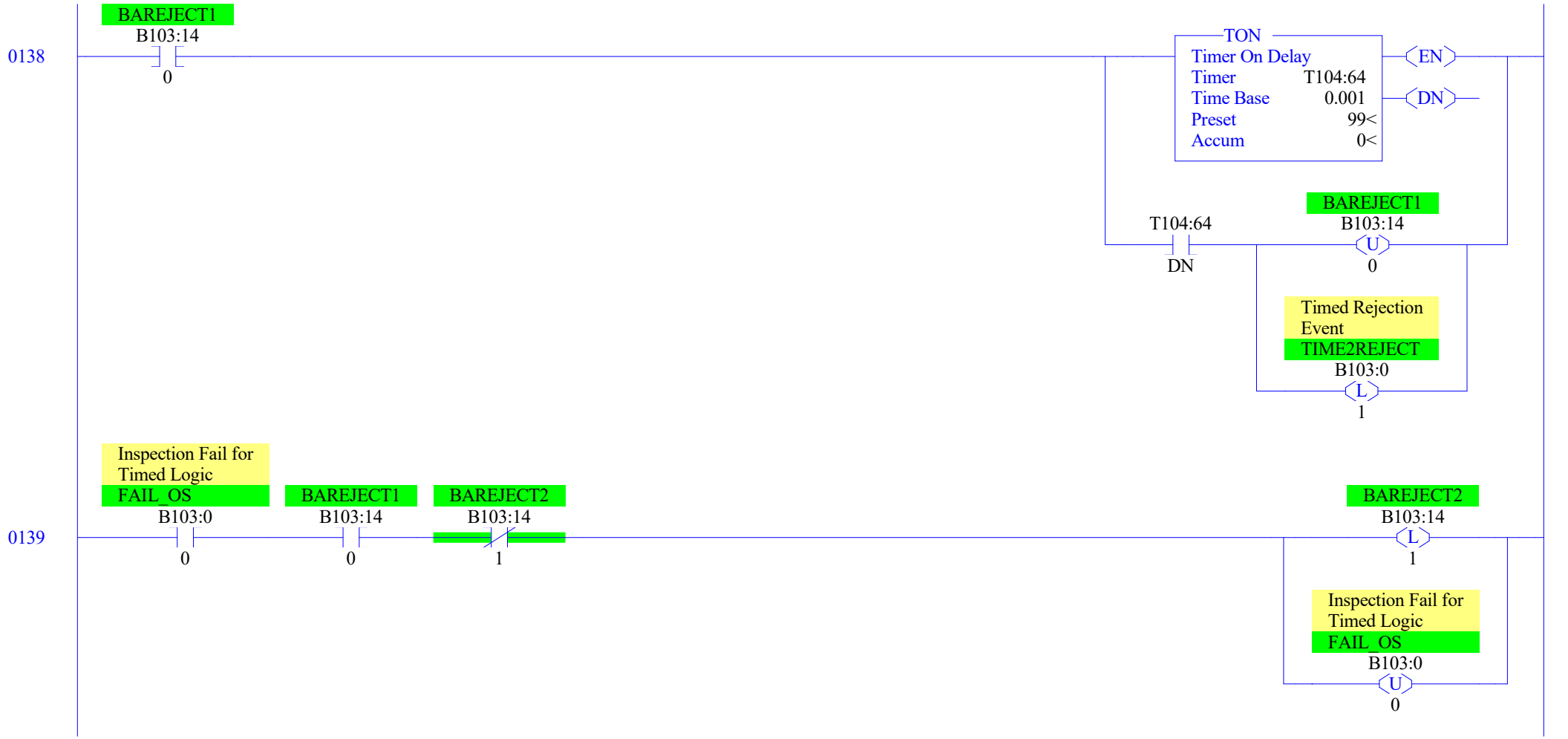

0130
CAREJECT13
B103:13
12
TON
Timer On Delay
Timer T104:60
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:60
DN
CAREJECT13
B103:13
U
12
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0131
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
CAREJECT13
B103:13
12
CAREJECT14
B103:13
13
CAREJECT14
B103:13
L
13
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

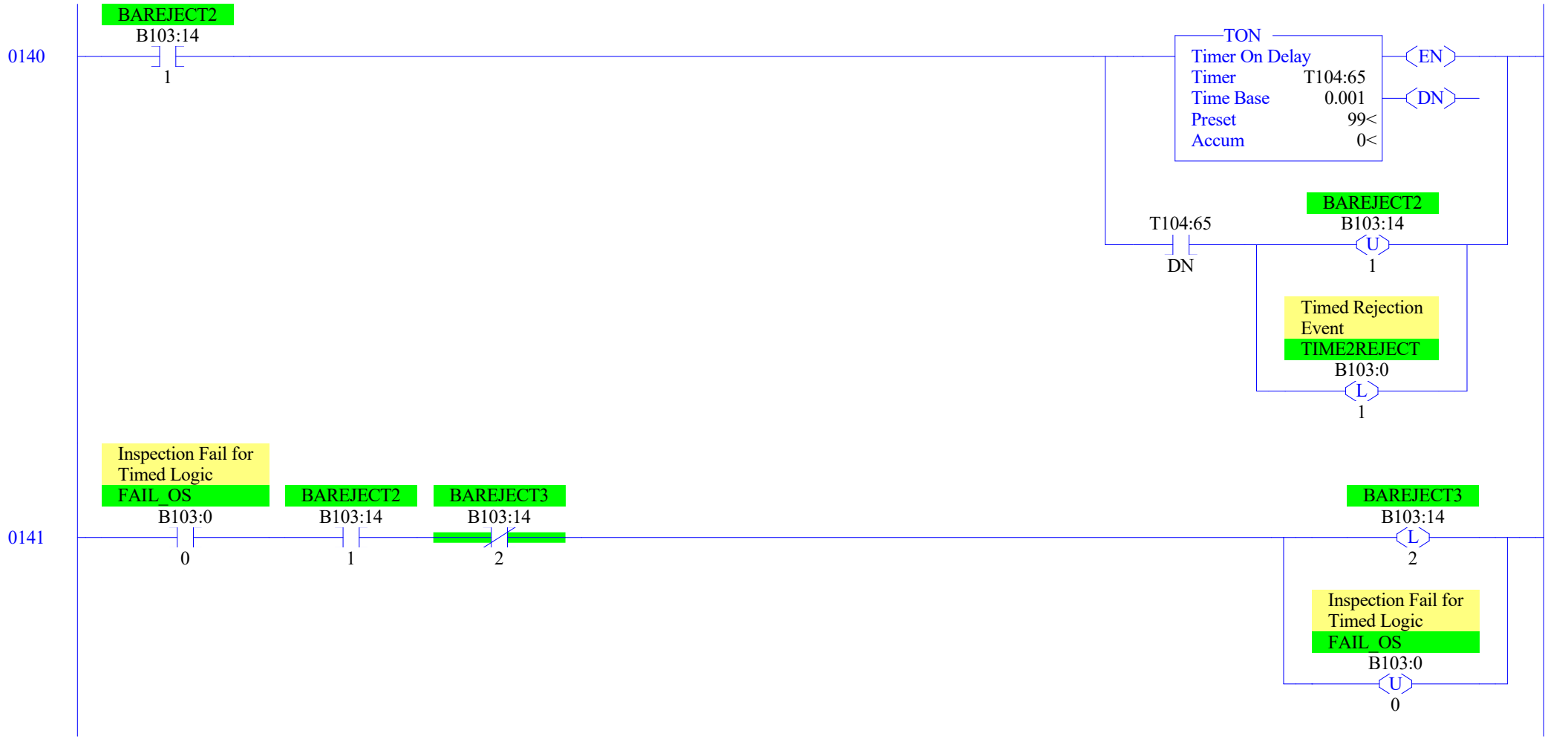

0132
CAREJECT14
B103:13
13
TON
Timer On Delay
Timer T104:61
Time Base 0.001
Preset 9<
Accum 0<
EN
DN
T104:61
DN
CAREJECT14
B103:13
U
13
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0133
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
CAREJECT14
B103:13
13
CAREJECT15
B103:13
14
CAREJECT15
B103:13
L
14
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

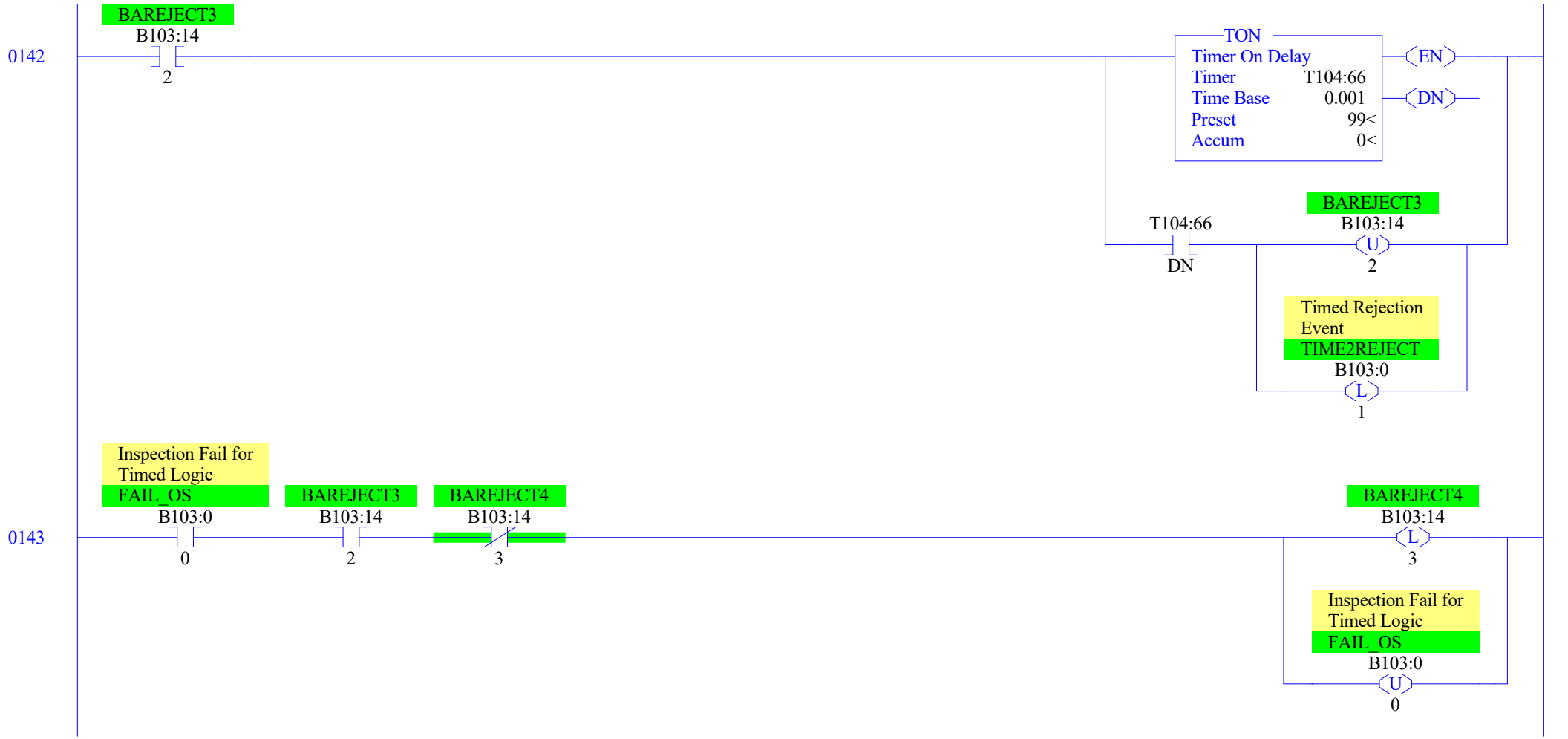

0134
CAREJECT15
B103:13
14
TON
Timer On Delay
Timer T104:62
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:62
DN
CAREJECT15
B103:13
U
14
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0135
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
CAREJECT15
B103:13
14
BREJECT16
B103:13
15
BREJECT16
B103:13
L
15
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

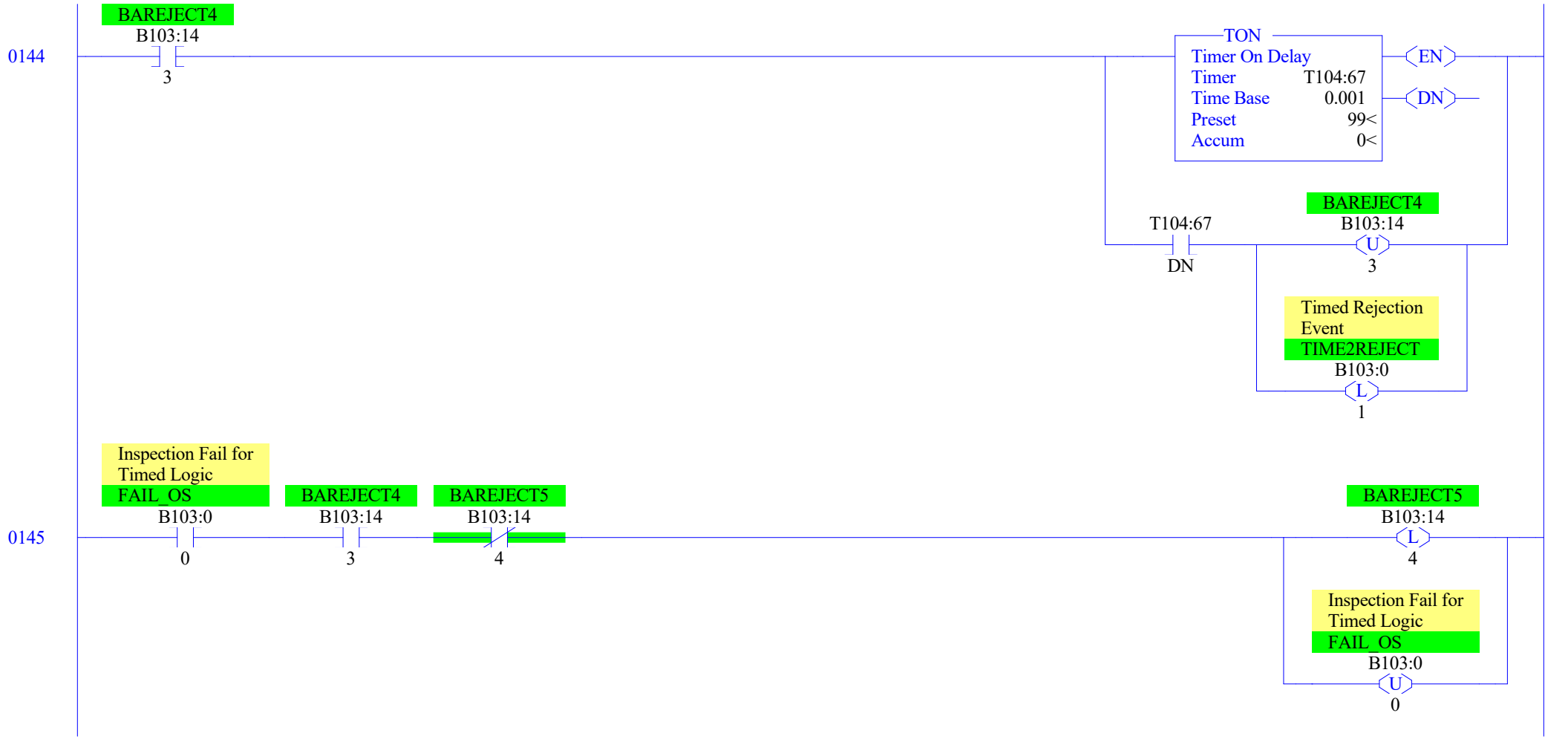
LAD 9 - REJ TIMERS --- Total Rungs in File = 235

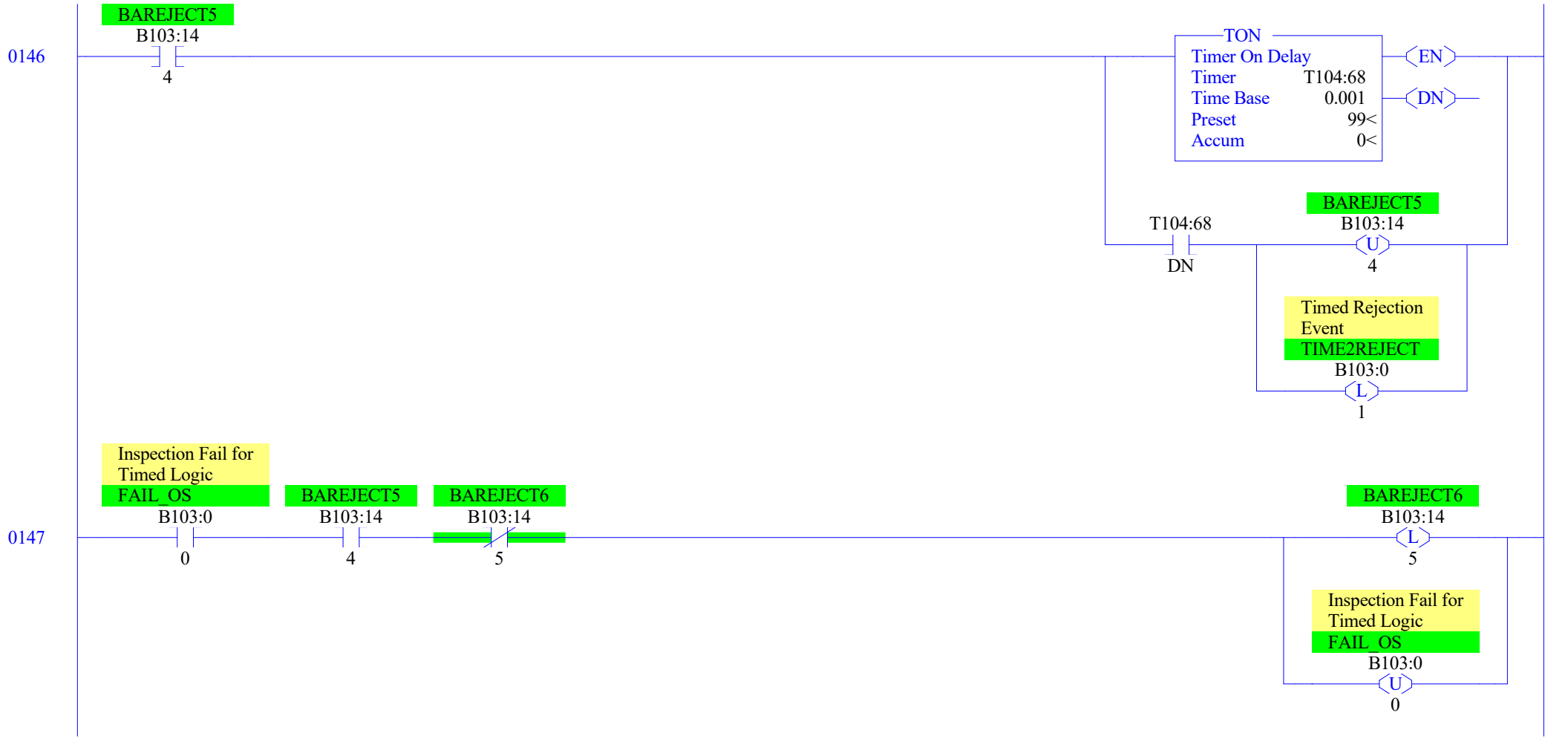


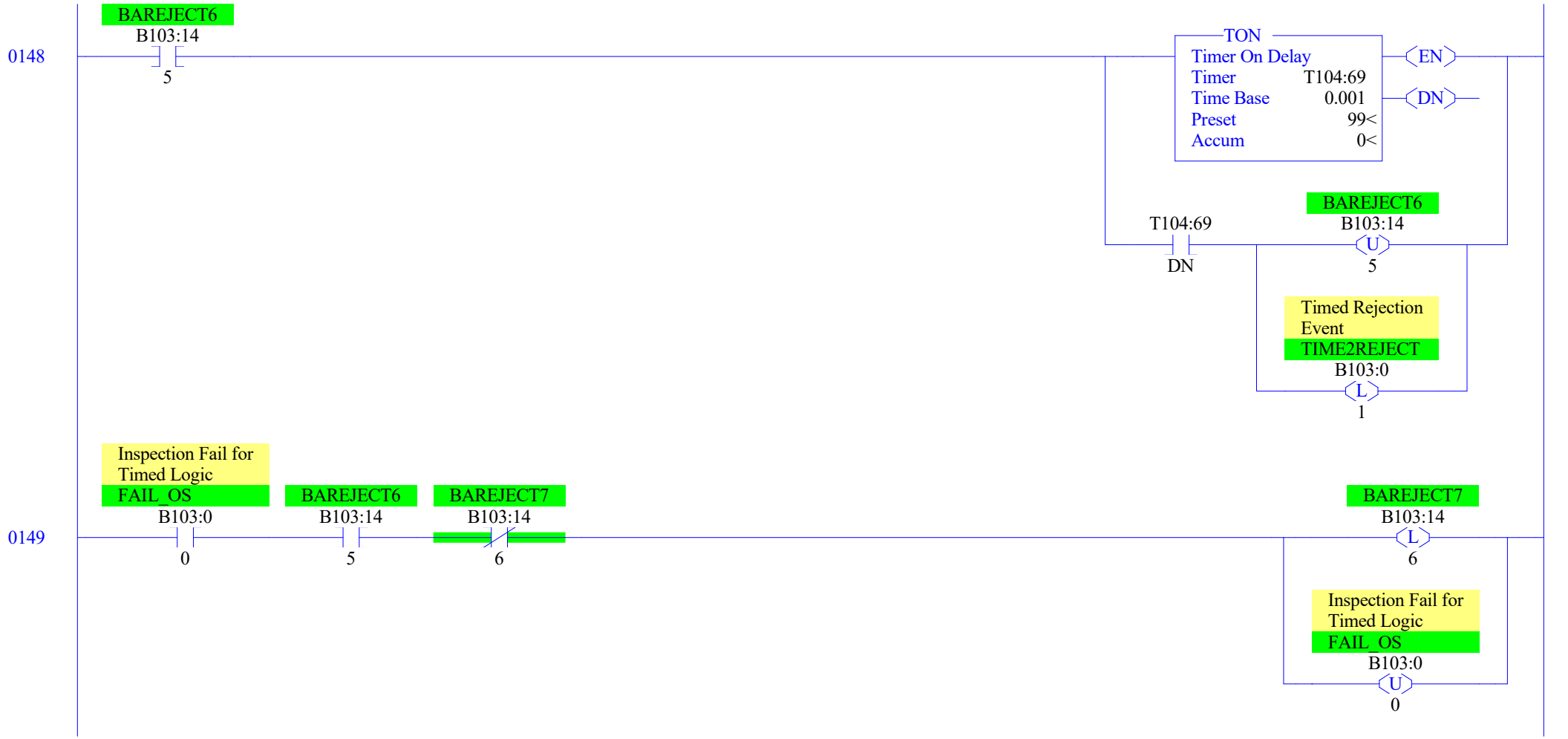

0138
BAREJECT1
B103:14
0
TON
Timer On Delay
Timer T104:64
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:64
DN
BAREJECT1
B103:14
U
0
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0139
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
BAREJECT1
B103:14
0
BAREJECT2
B103:14
1
BAREJECT2
B103:14
L
1
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0


0140
BAREJECT2
B103:14
1
TON
Timer On Delay
Timer T104:65
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:65
DN
BAREJECT2
B103:14
U
1
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0141
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
BAREJECT2
B103:14
1
BAREJECT3
B103:14
2
BAREJECT3
B103:14
L
2
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

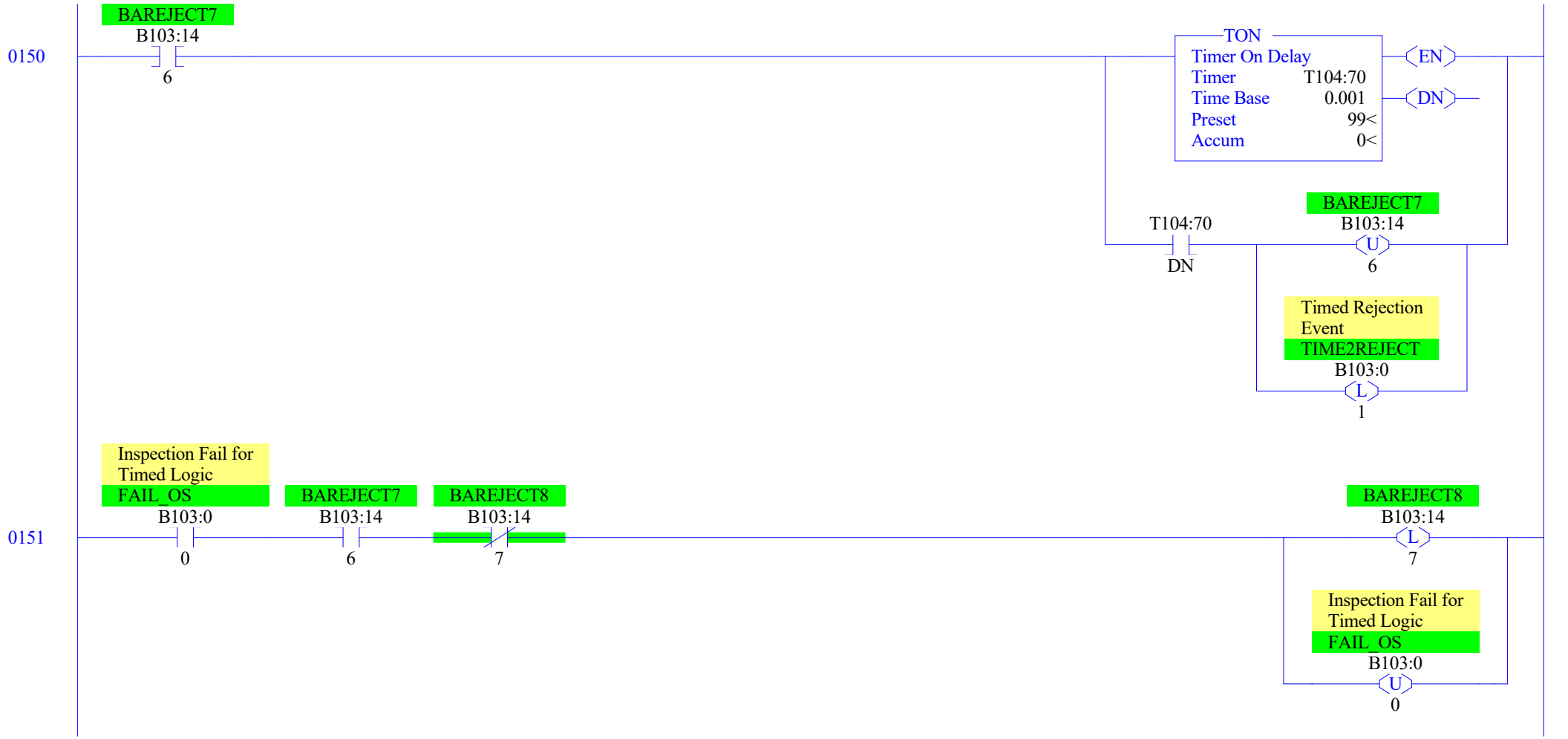

0142
BAREJECT3
B103:14
2
TON
Timer On Delay
Timer T104:66
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:66
DN
BAREJECT3
B103:14
U
2
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0143
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
BAREJECT3
B103:14
2
BAREJECT4
B103:14
3
BAREJECT4
B103:14
L
3
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

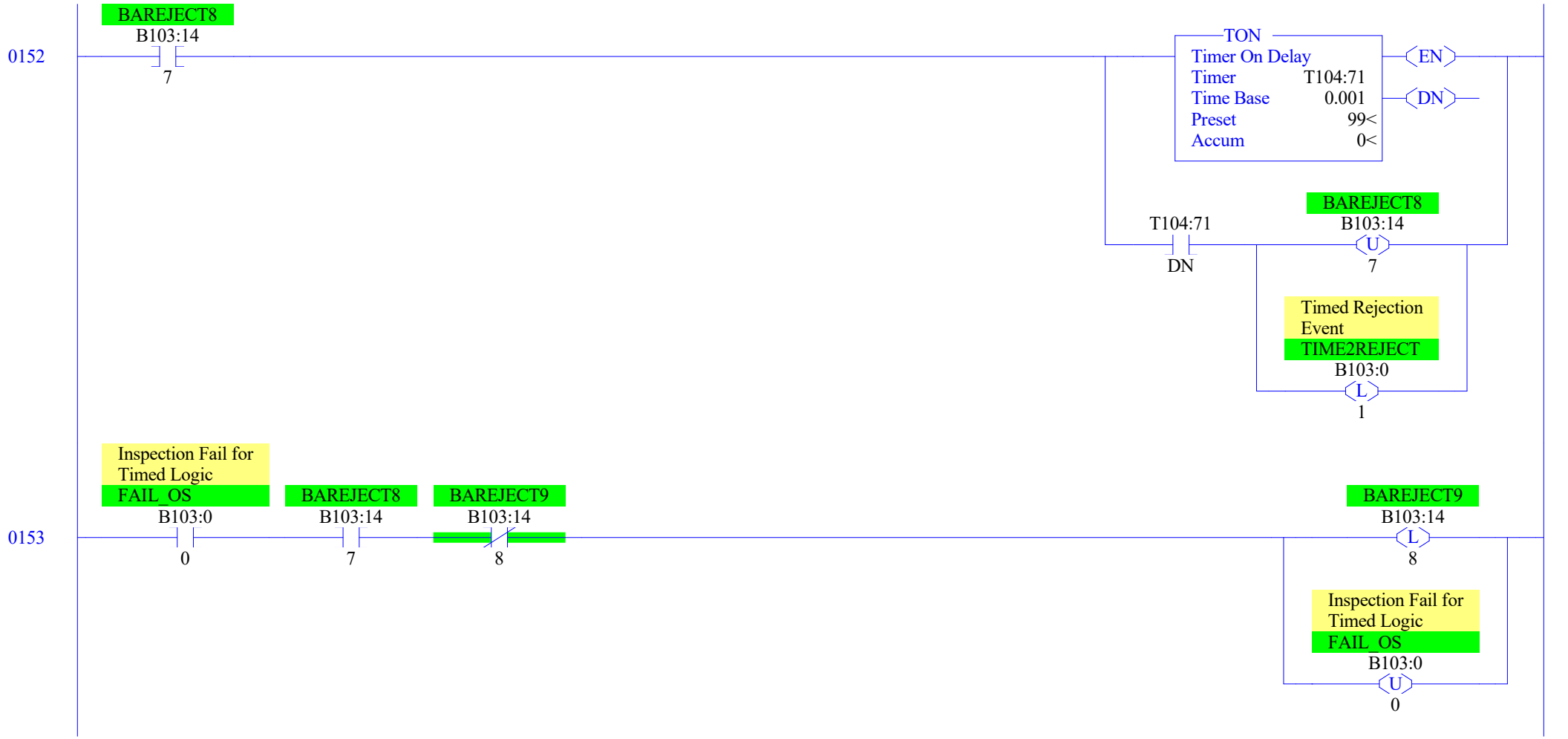

0144
BAREJECT4
B103:14
3
TON
Timer On Delay
Timer T104:67
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:67
DN
BAREJECT4
B103:14
U
3
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0145
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
BAREJECT4
B103:14
3
BAREJECT5
B103:14
4
BAREJECT5
B103:14
L
4
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0


0146
BAREJECT5
B103:14
4
TON
Timer On Delay
Timer T104:68
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:68
DN
BAREJECT5
B103:14
U
4
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0147
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
BAREJECT5
B103:14
4
BAREJECT6
B103:14
5
BAREJECT6
B103:14
L
5
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

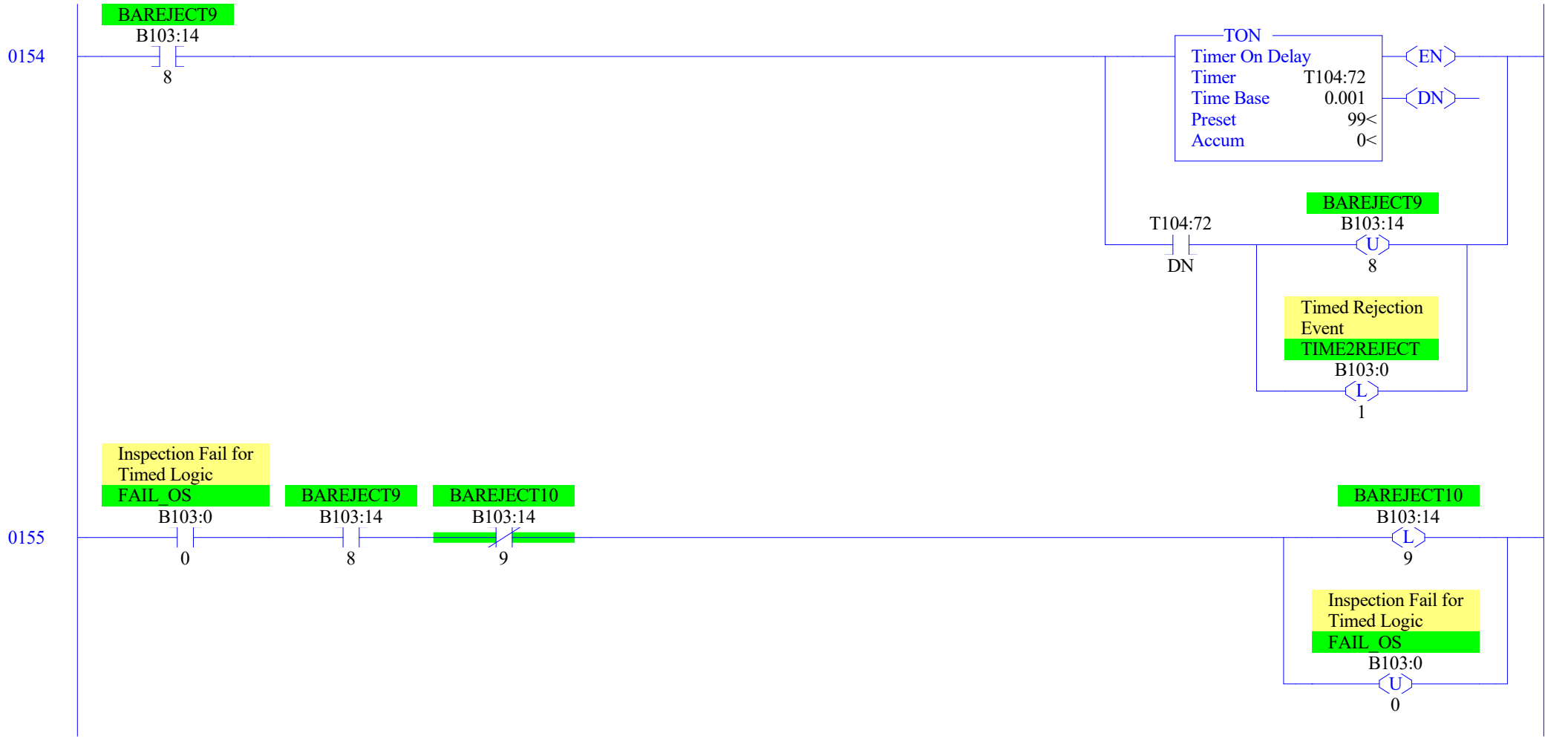

0148
BAREJECT6
B103:14
5
TON
Timer On Delay
Timer T104:69
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:69
DN
BAREJECT6
B103:14
U
5
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0149
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
BAREJECT6
B103:14
5
BAREJECT7
B103:14
6
BAREJECT7
B103:14
L
6
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

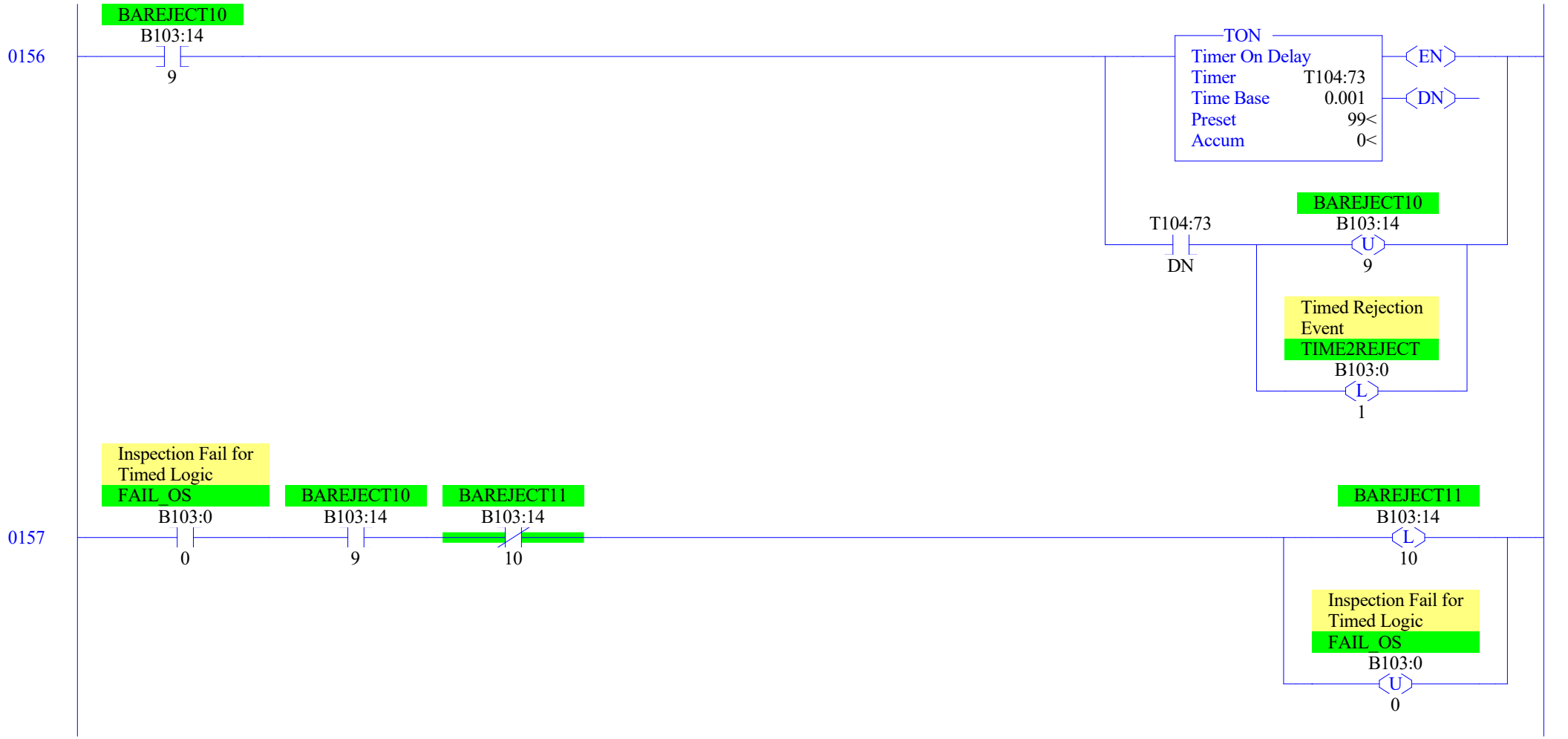
LAD 9 - REJ TIMERS --- Total Rungs in File = 235

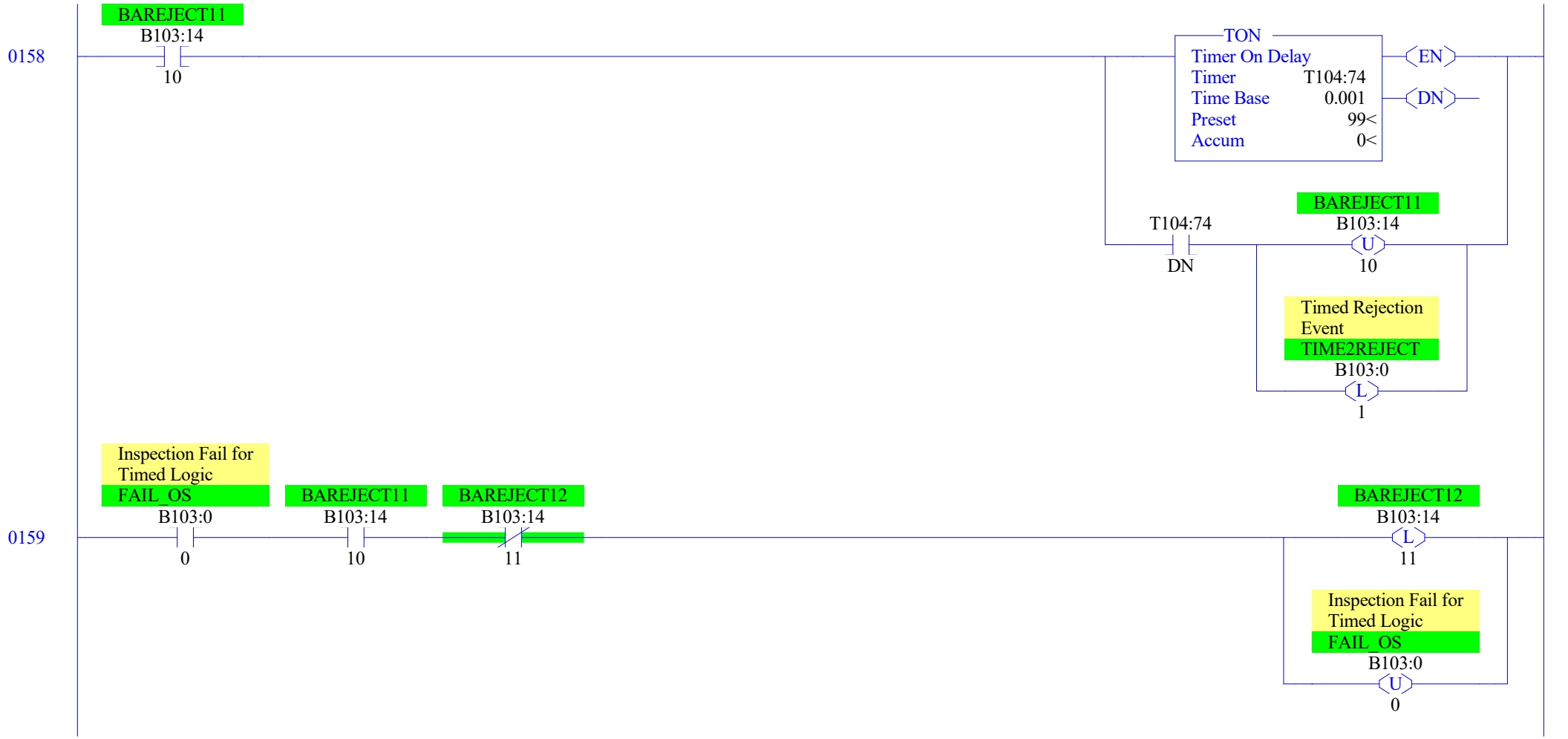


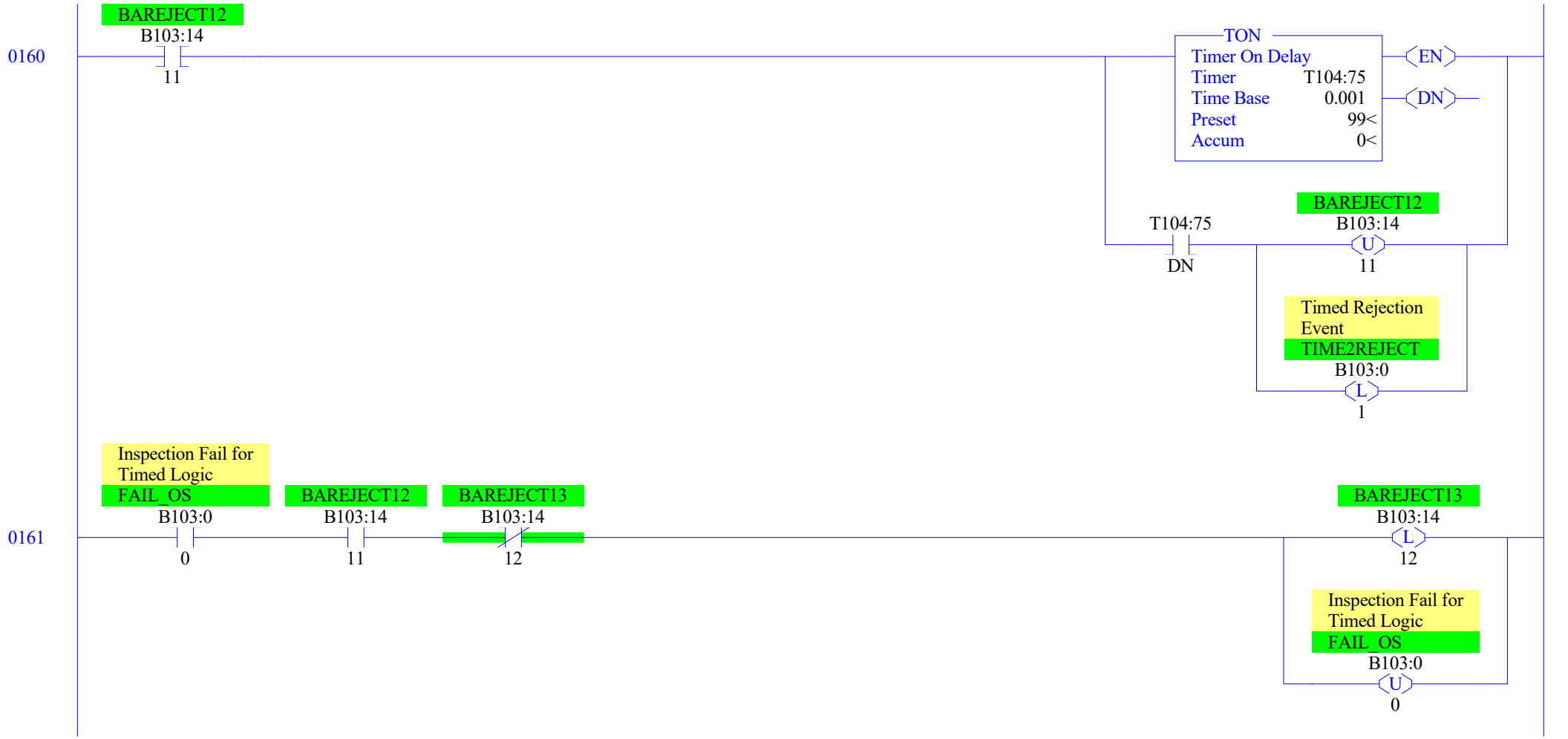

0152
BAREJECT8
B103:14
7
TON
Timer On Delay
Timer T104:71
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:71
DN
BAREJECT8
B103:14
U
7
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0153
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
BAREJECT8
B103:14
7
BAREJECT9
B103:14
8
BAREJECT9
B103:14
L
8
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

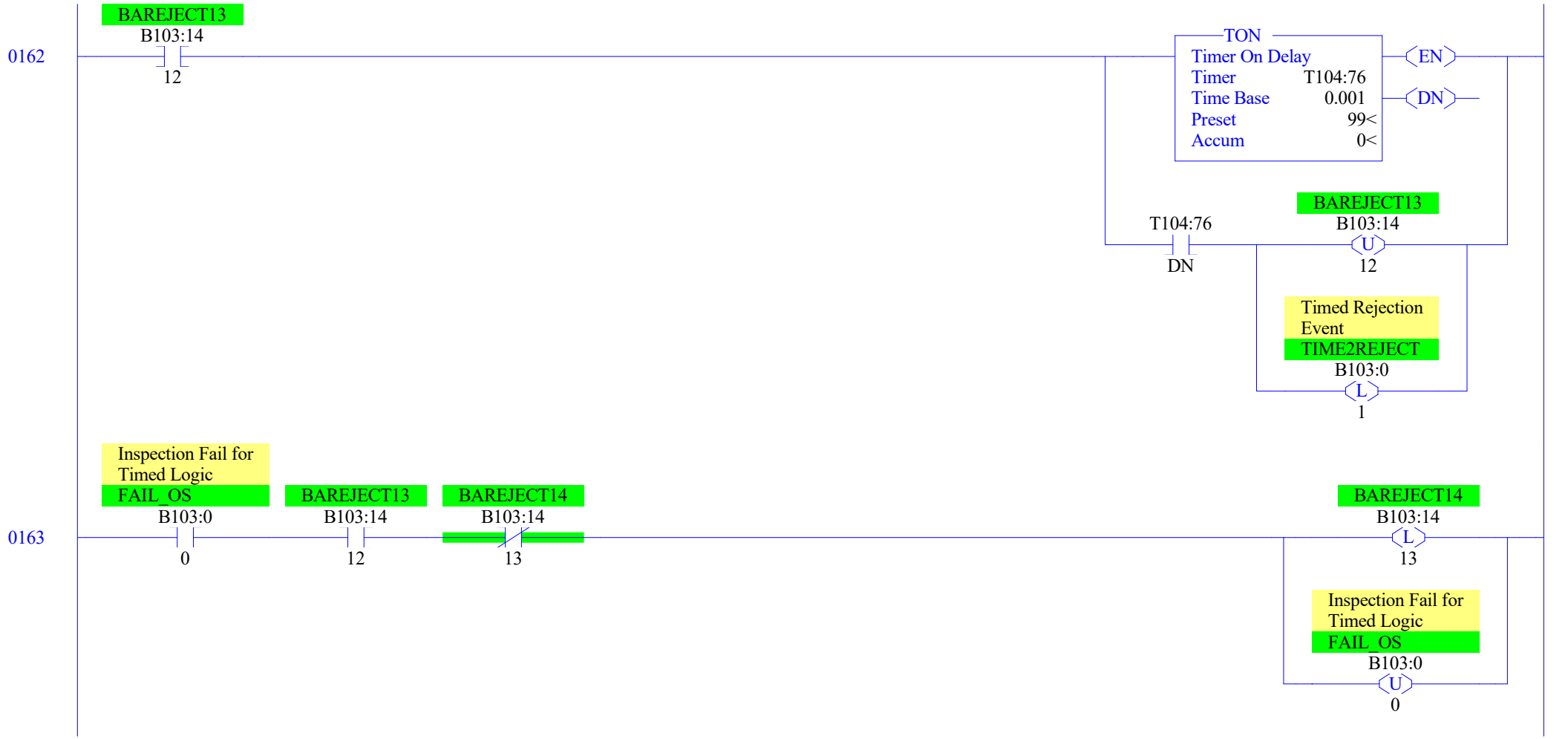
LAD 9 - REJ TIMERS --- Total Rungs in File = 235

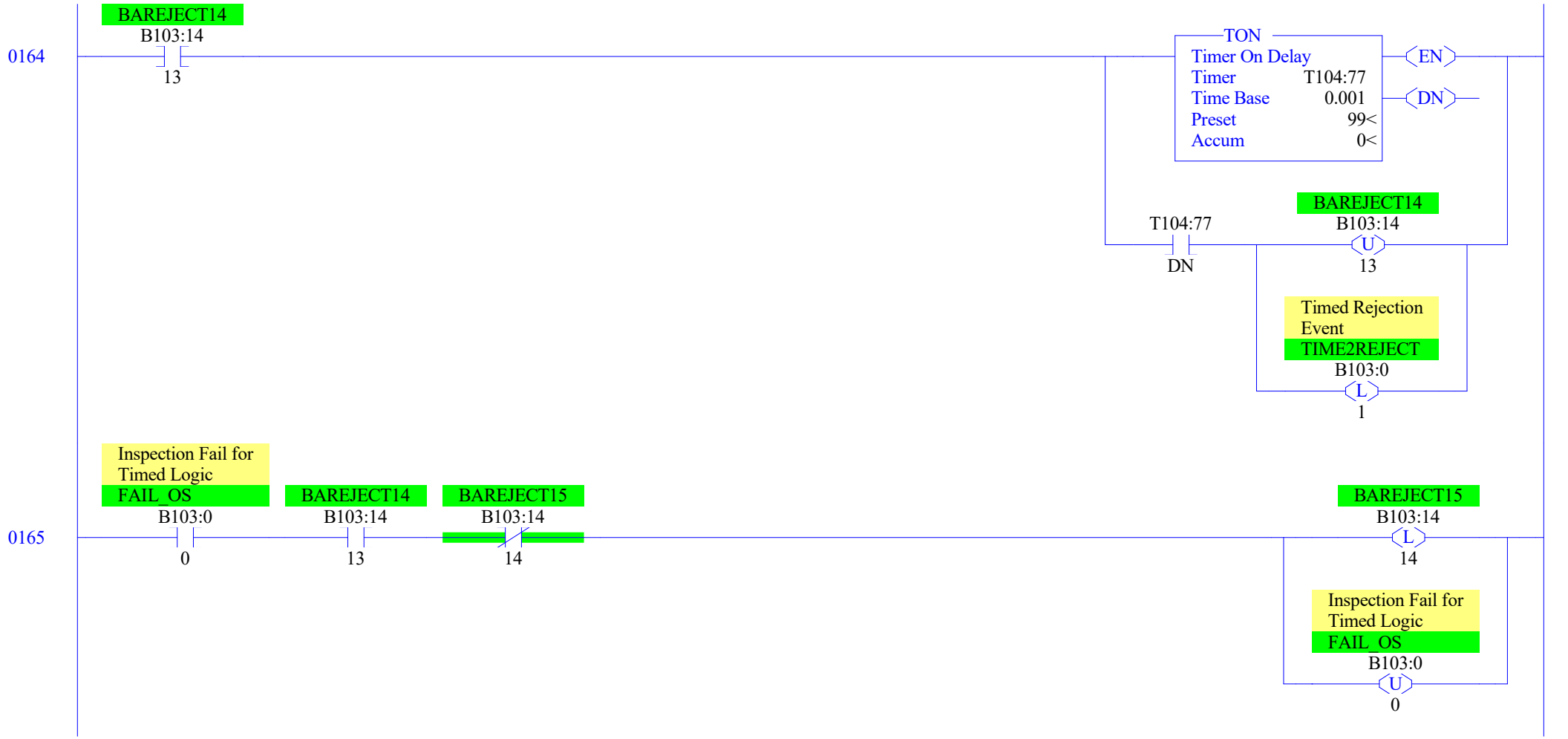


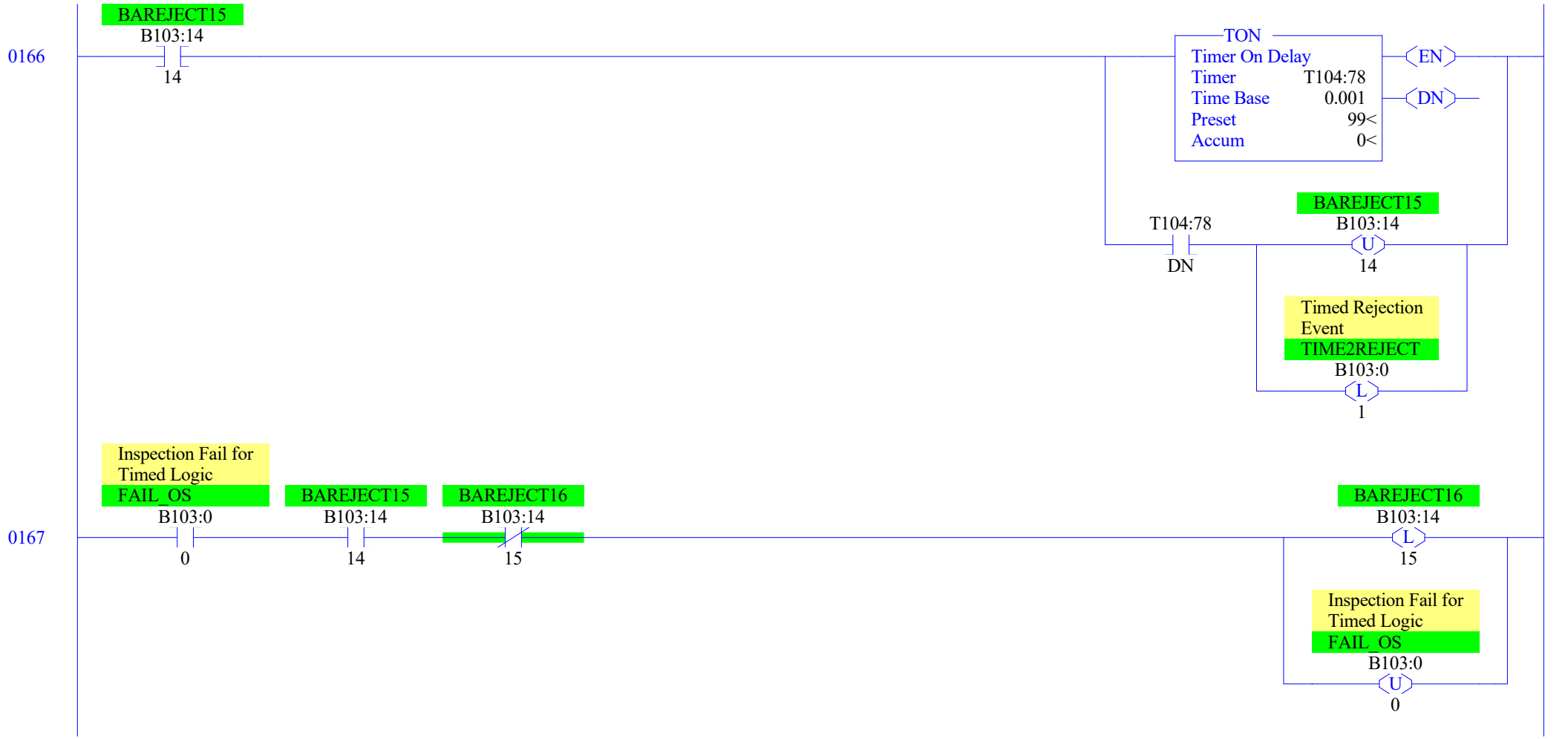

0156
BAREJECT10
B103:14
9
TON
Timer On Delay
Timer T104:73
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:73
DN
BAREJECT10
B103:14
U
9
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0157
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
BAREJECT10
B103:14
9
BAREJECT11
B103:14
10
BAREJECT11
B103:14
L
10
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

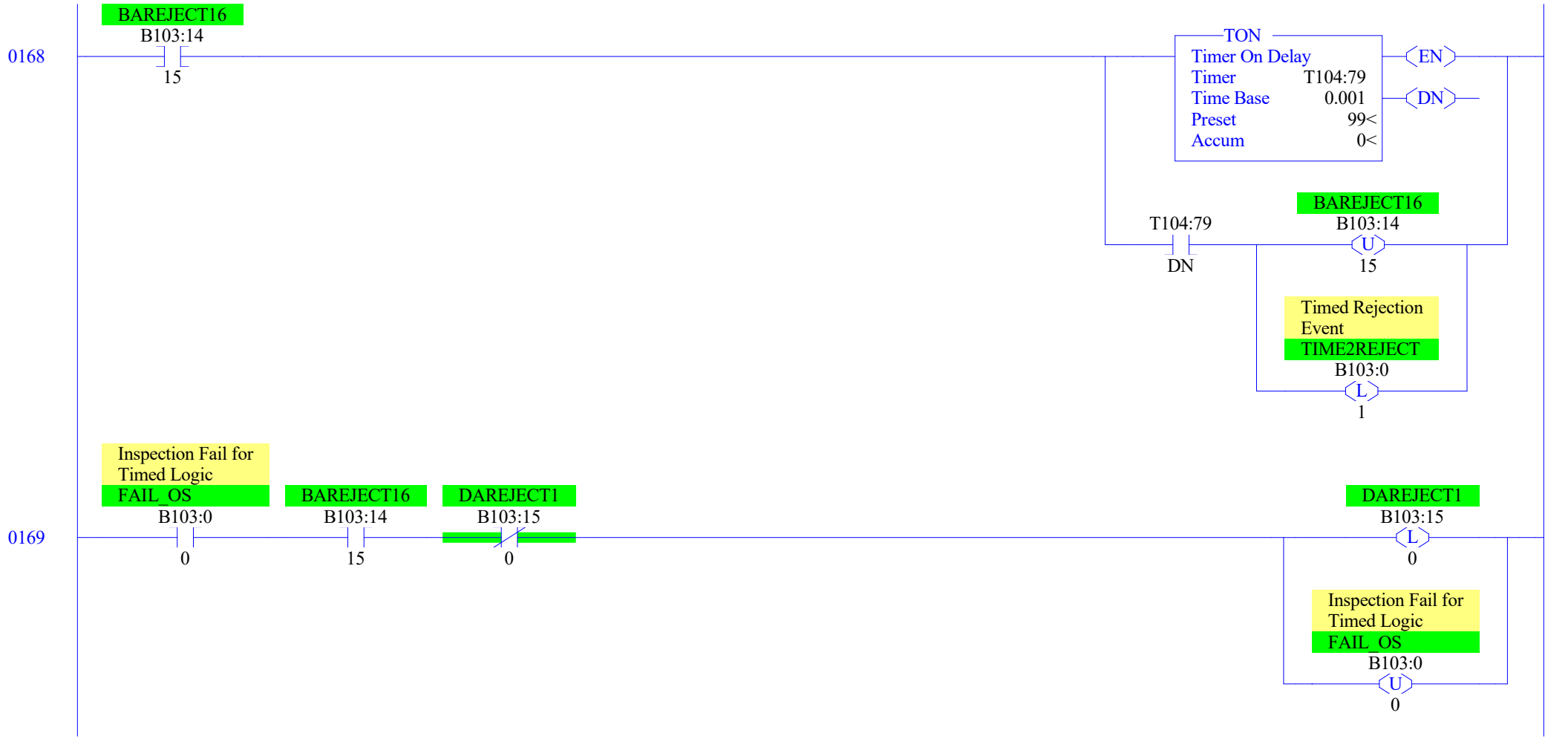

0158
BAREJECT11
B103:14
10
TON
Timer On Delay
Timer T104:74
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:74
DN
BAREJECT11
B103:14
U
10
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0159
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
BAREJECT11
B103:14
10
BAREJECT12
B103:14
11
BAREJECT12
B103:14
L
11
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

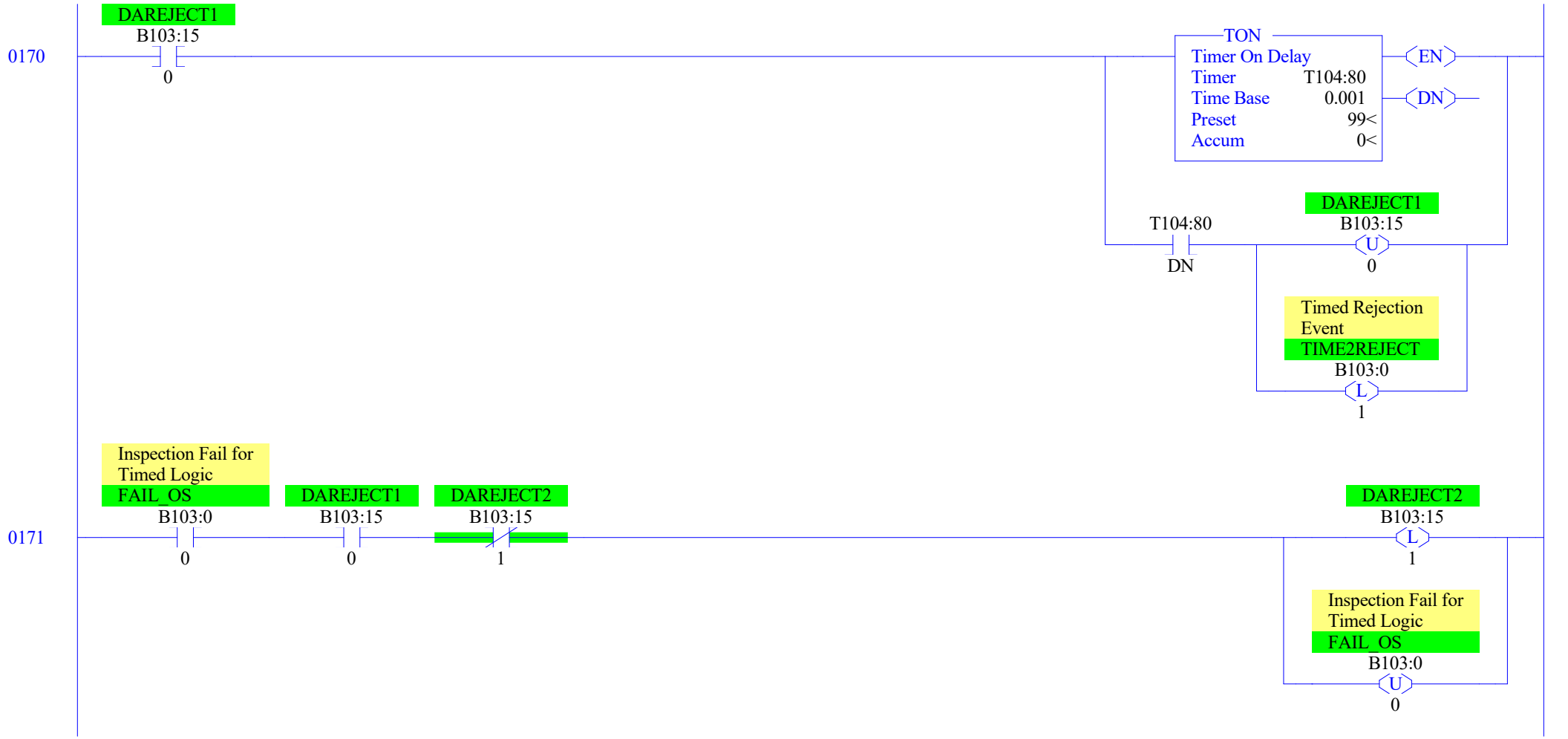

0160
BAREJECT12
B103:14
11
TON
Timer On Delay
Timer T104:75
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:75
DN
BAREJECT12
B103:14
U
11
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0161
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
BAREJECT12
B103:14
11
BAREJECT13
B103:14
12
BAREJECT13
B103:14
L
12
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

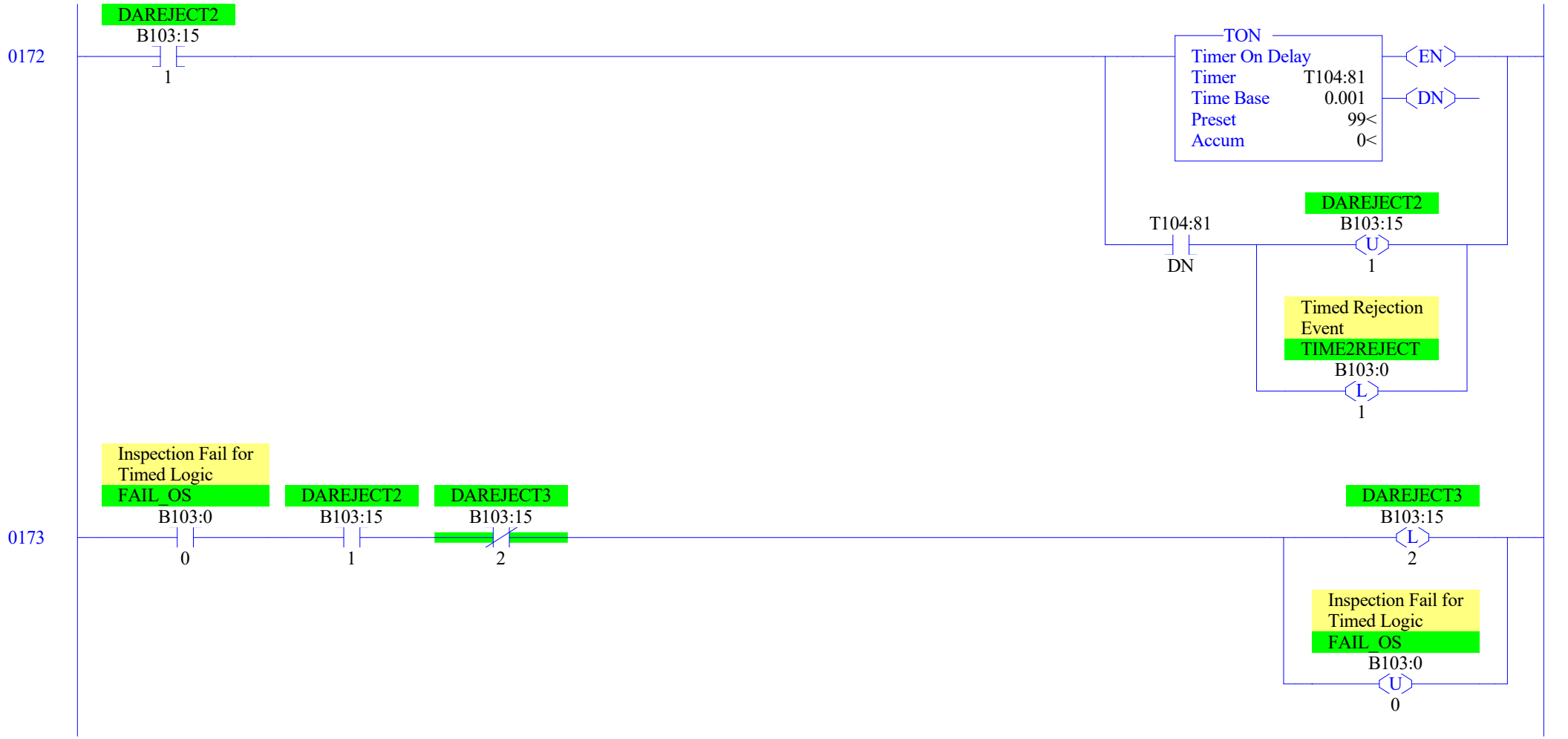

0162
BAREJECT13
B103:14
12
TON
Timer On Delay
Timer T104:76
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:76
DN
BAREJECT13
B103:14
U
12
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0163
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
BAREJECT13
B103:14
12
BAREJECT14
B103:14
13
BAREJECT14
B103:14
L
13
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

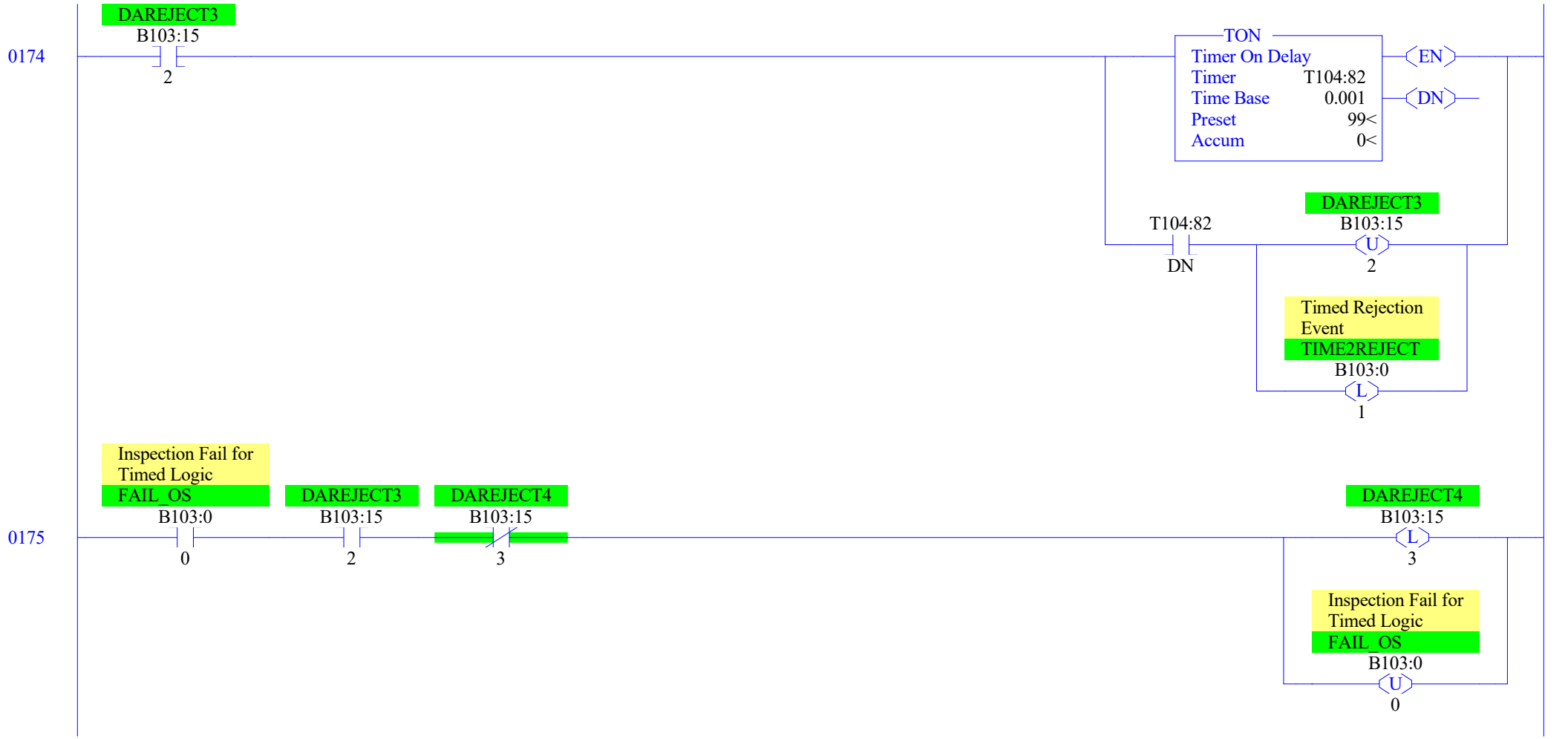

0164
BAREJECT14
B103:14
13
TON
Timer On Delay
Timer T104:77
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:77
DN
BAREJECT14
B103:14
U
13
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0165
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
BAREJECT14
B103:14
13
BAREJECT15
B103:14
14
BAREJECT15
B103:14
L
14
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

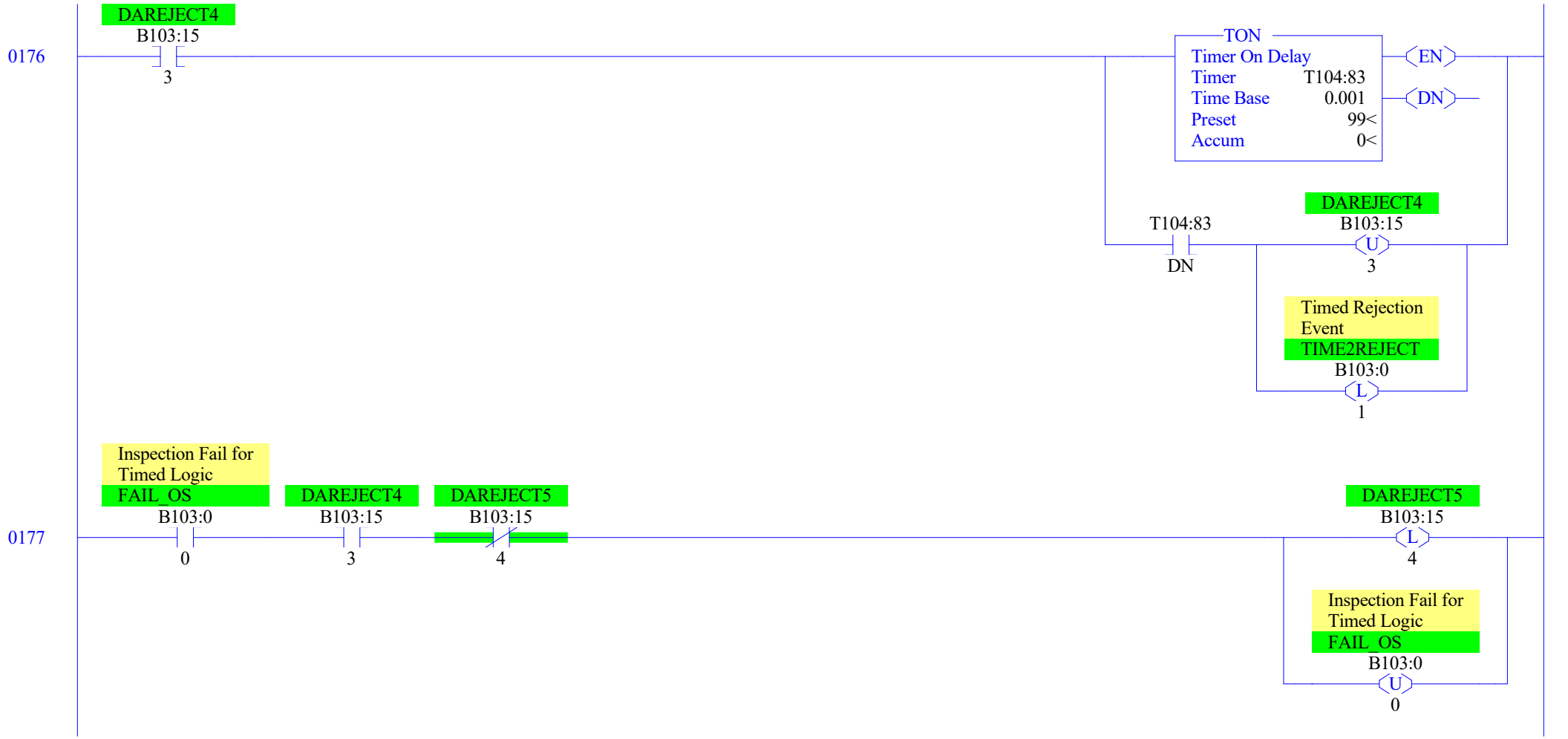

0166
BAREJECT15
B103:14
14
TON
Timer On Delay
Timer T104:78
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:78
DN
BAREJECT15
B103:14
U
14
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0167
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
BAREJECT15
B103:14
14
BAREJECT16
B103:14
15
BAREJECT16
B103:14
L
15
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0


0168
BAREJECT16
B103:14
15
TON
Timer On Delay
Timer T104:79
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:79
DN
BAREJECT16
B103:14
U
15
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0169
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
BAREJECT16
B103:14
15
DAREJECT1
B103:15
0
DAREJECT1
B103:15
L
0
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

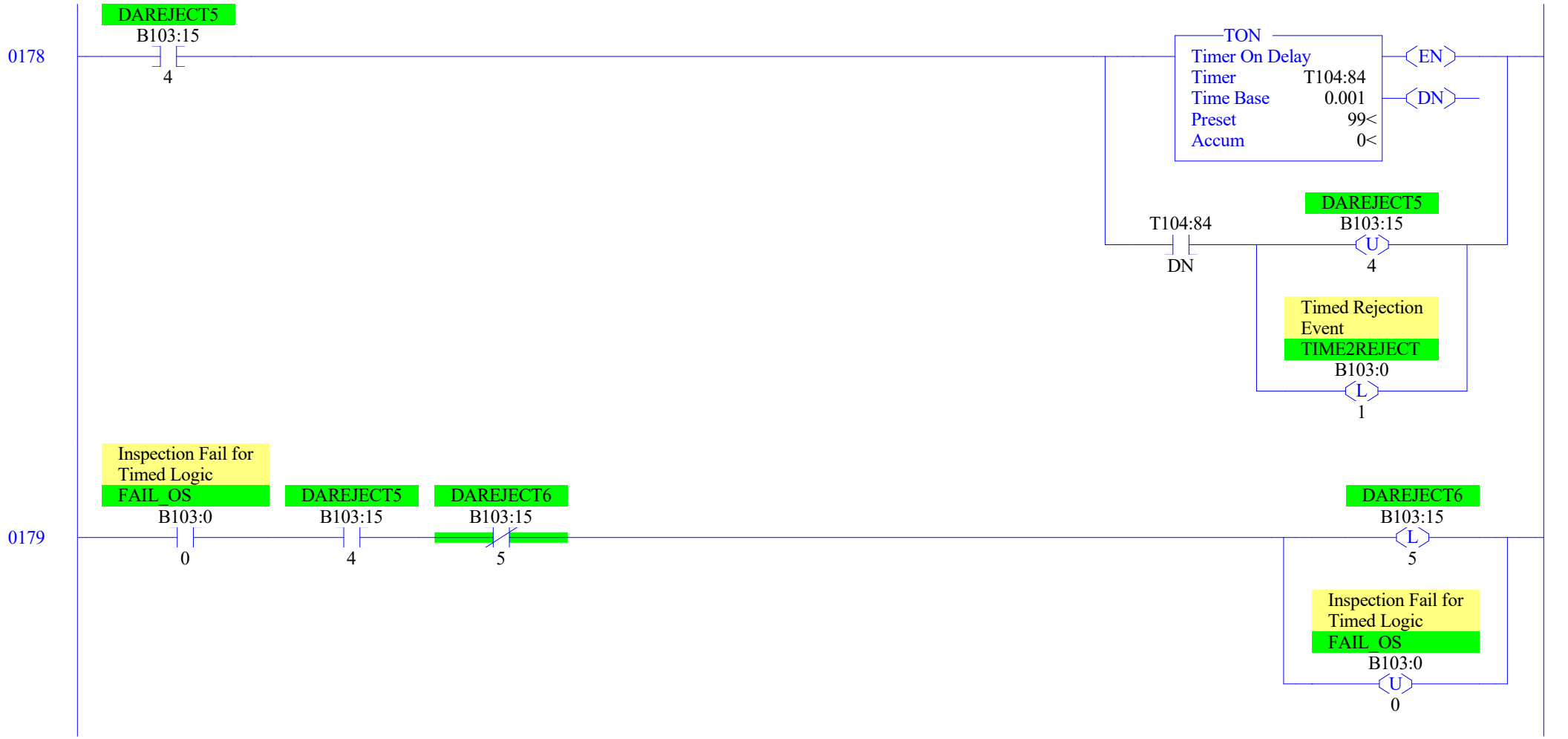

0170
DAREJECT1
B103:15
0
TON
Timer On Delay
Timer T104:80
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:80
DN
DAREJECT1
B103:15
U
0
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0171
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
DAREJECT1
B103:15
0
DAREJECT2
B103:15
1
DAREJECT2
B103:15
L
1
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0


0172
DAREJECT2
B103:15
1
TON
Timer On Delay
Timer T104:81
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:81
DN
DAREJECT2
B103:15
U
1
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0173
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
DAREJECT2
B103:15
1
DAREJECT3
B103:15
2
DAREJECT3
B103:15
L
2
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

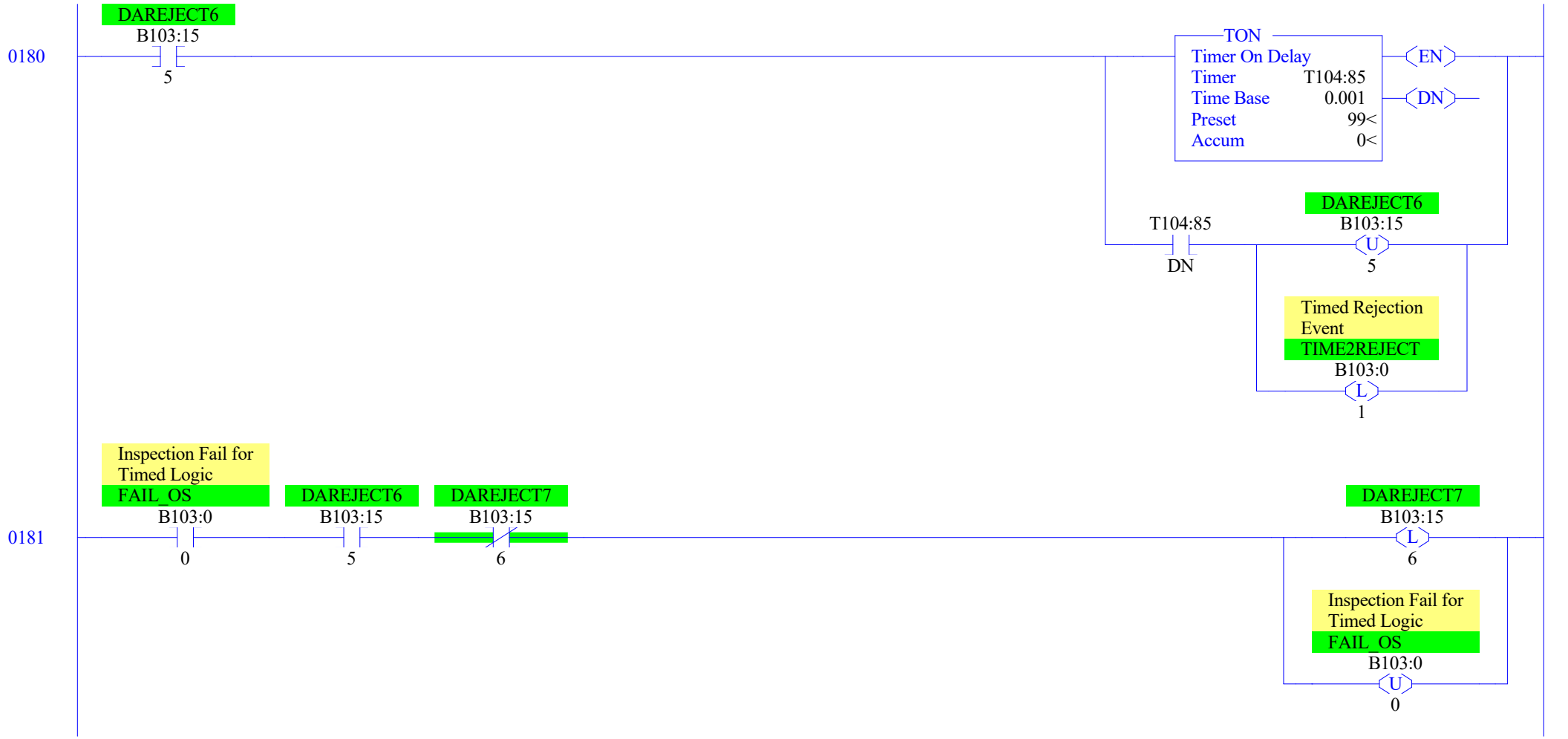

0174
DAREJECT3
B103:15
2
TON
Timer On Delay
Timer T104:82
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:82
DN
DAREJECT3
B103:15
U
2
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0175
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
DAREJECT3
B103:15
2
DAREJECT4
B103:15
3
DAREJECT4
B103:15
L
3
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0


0176
DAREJECT4
B103:15
3
TON
Timer On Delay
Timer T104:83
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:83
DN
DAREJECT4
B103:15
U
3
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0177
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
DAREJECT4
B103:15
3
DAREJECT5
B103:15
4
DAREJECT5
B103:15
L
4
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

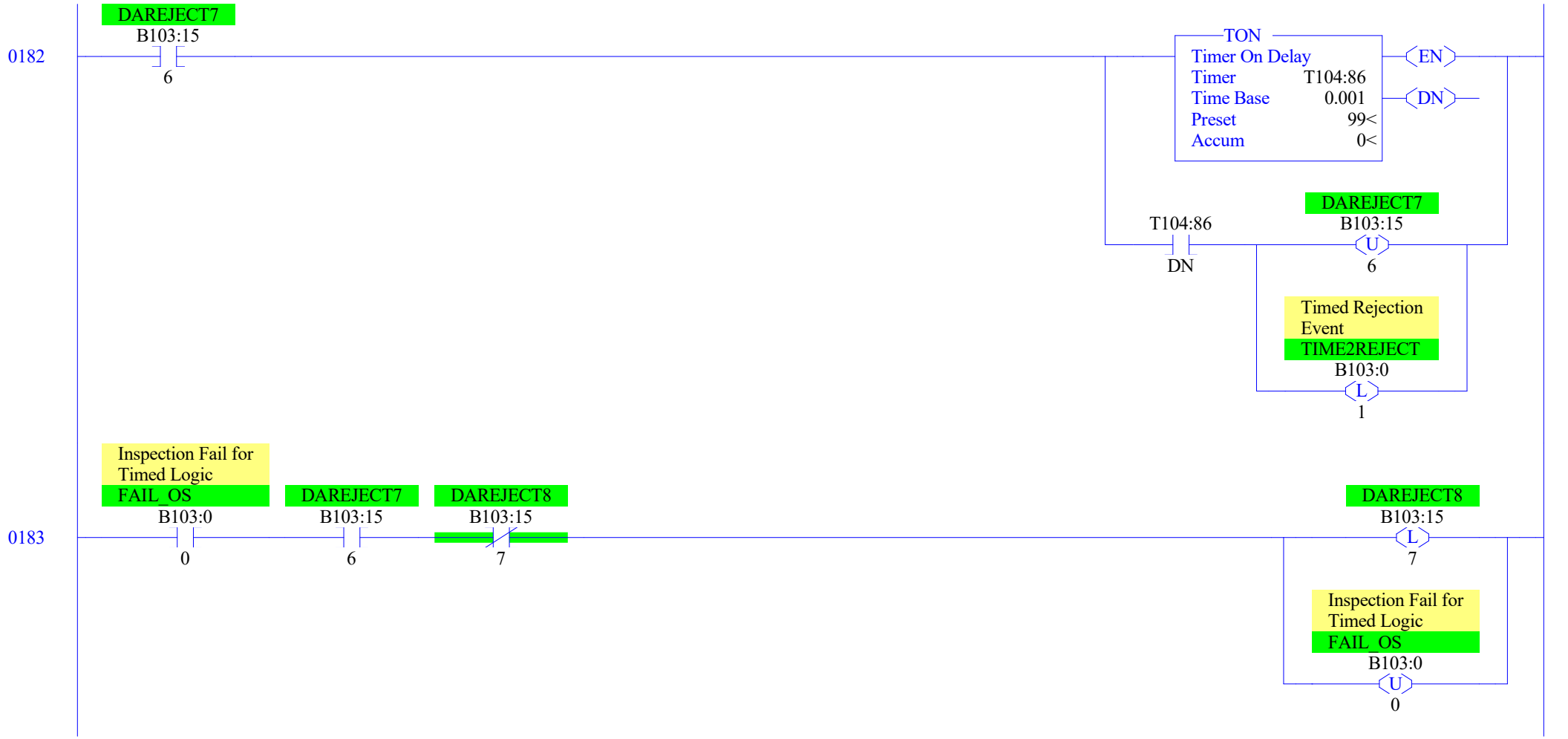
LAD 9 - REJ TIMERS --- Total Rungs in File = 235



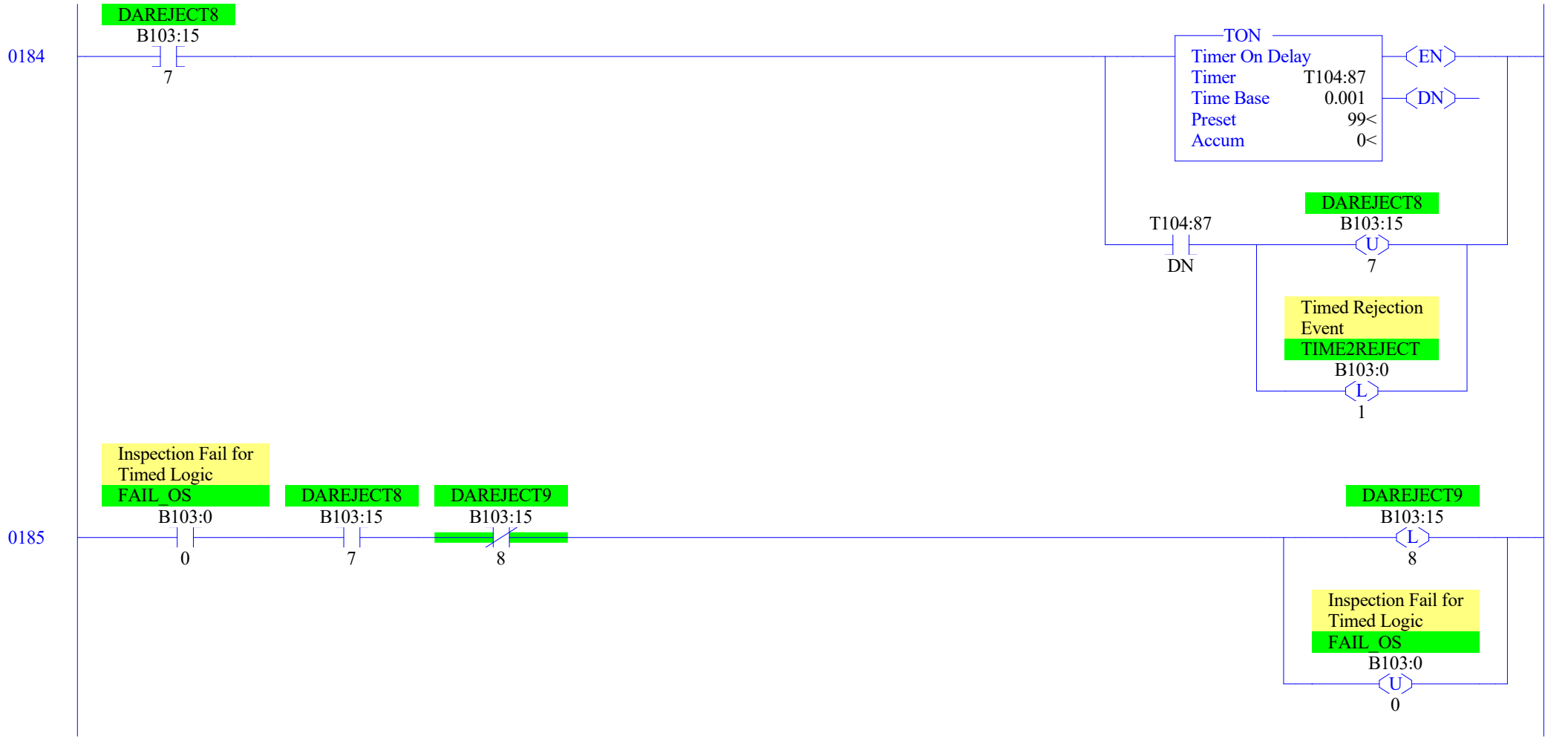
LAD 9 - REJ TIMERS --- Total Rungs in File = 235



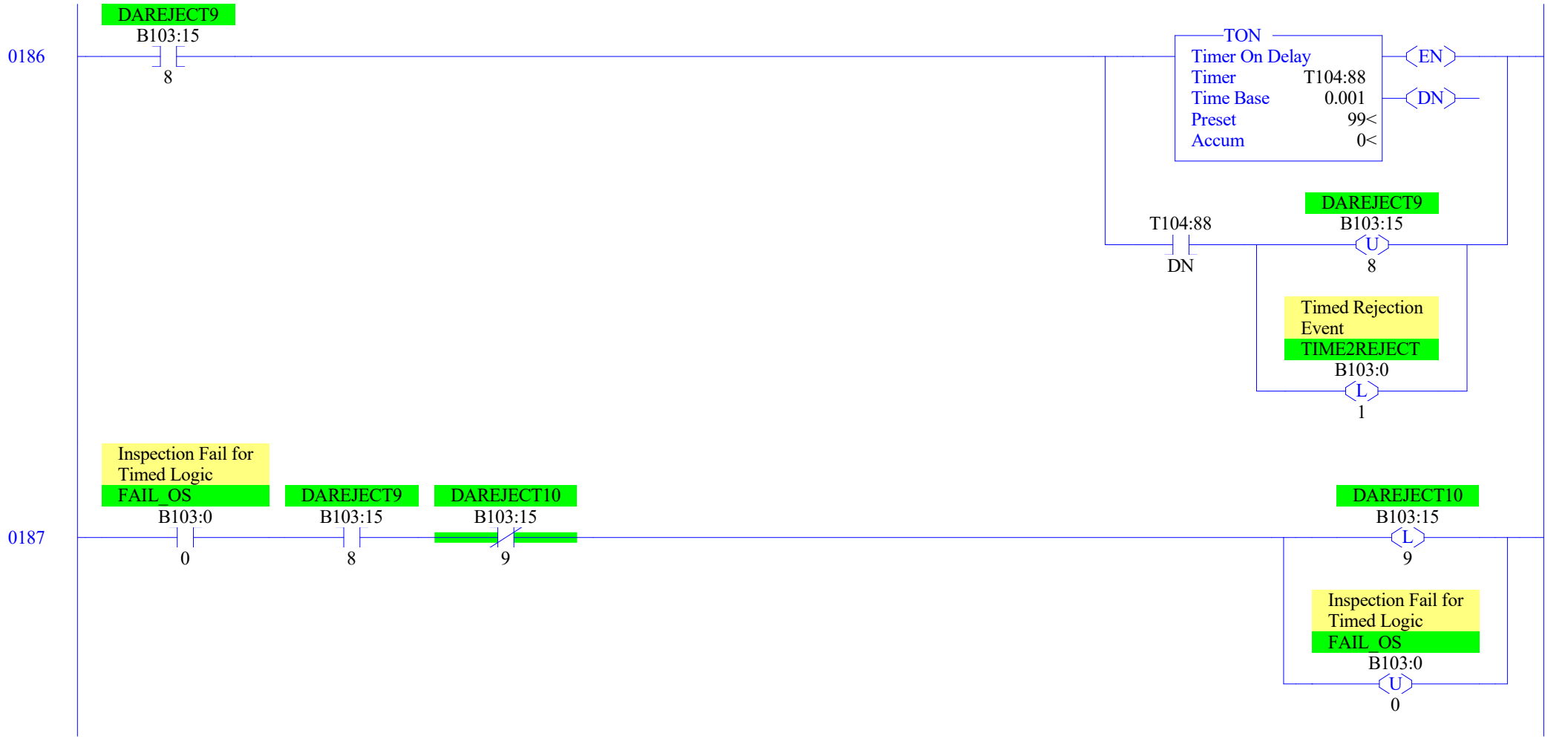
LAD 9 - REJ TIMERS --- Total Rungs in File = 235



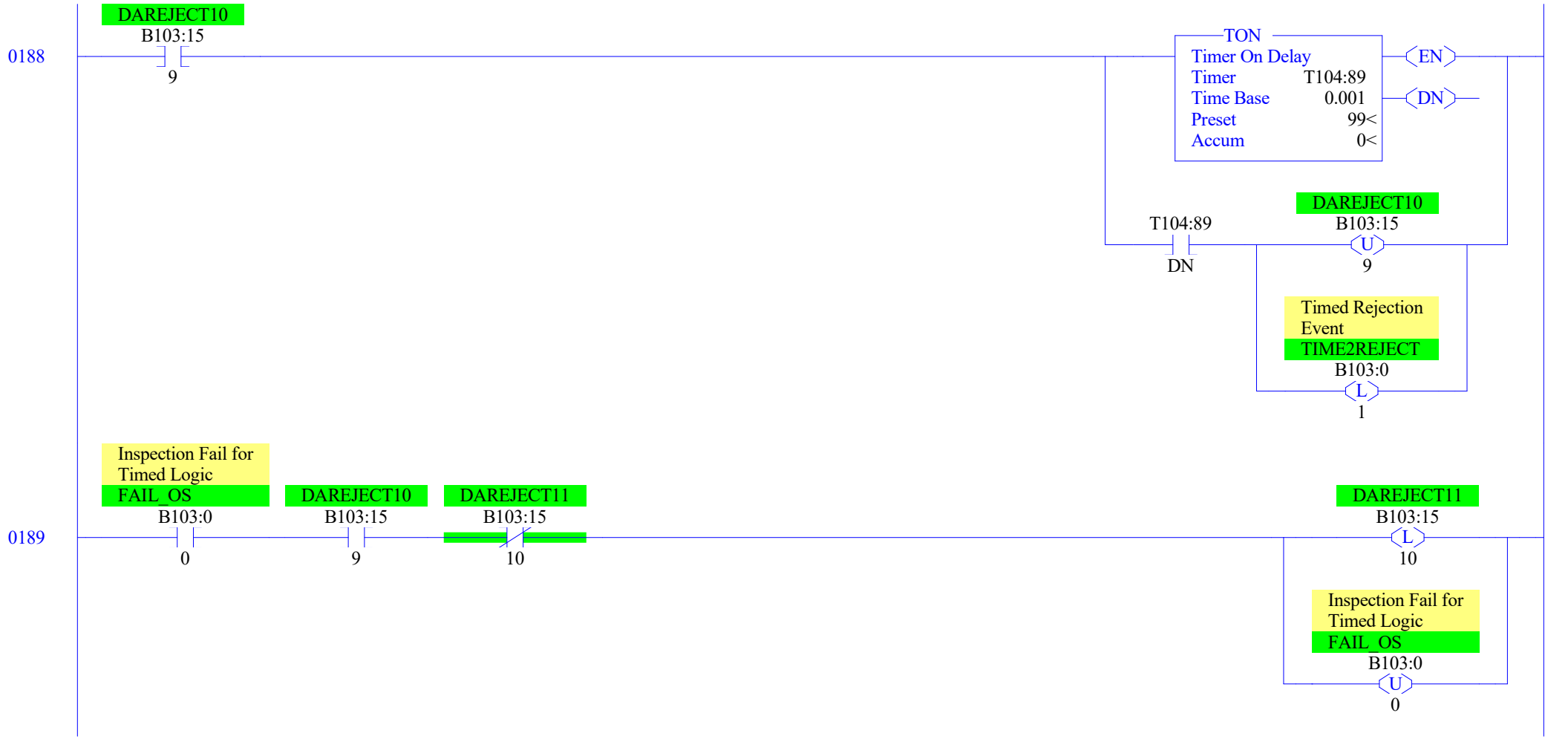
LAD 9 - REJ TIMERS --- Total Rungs in File = 235

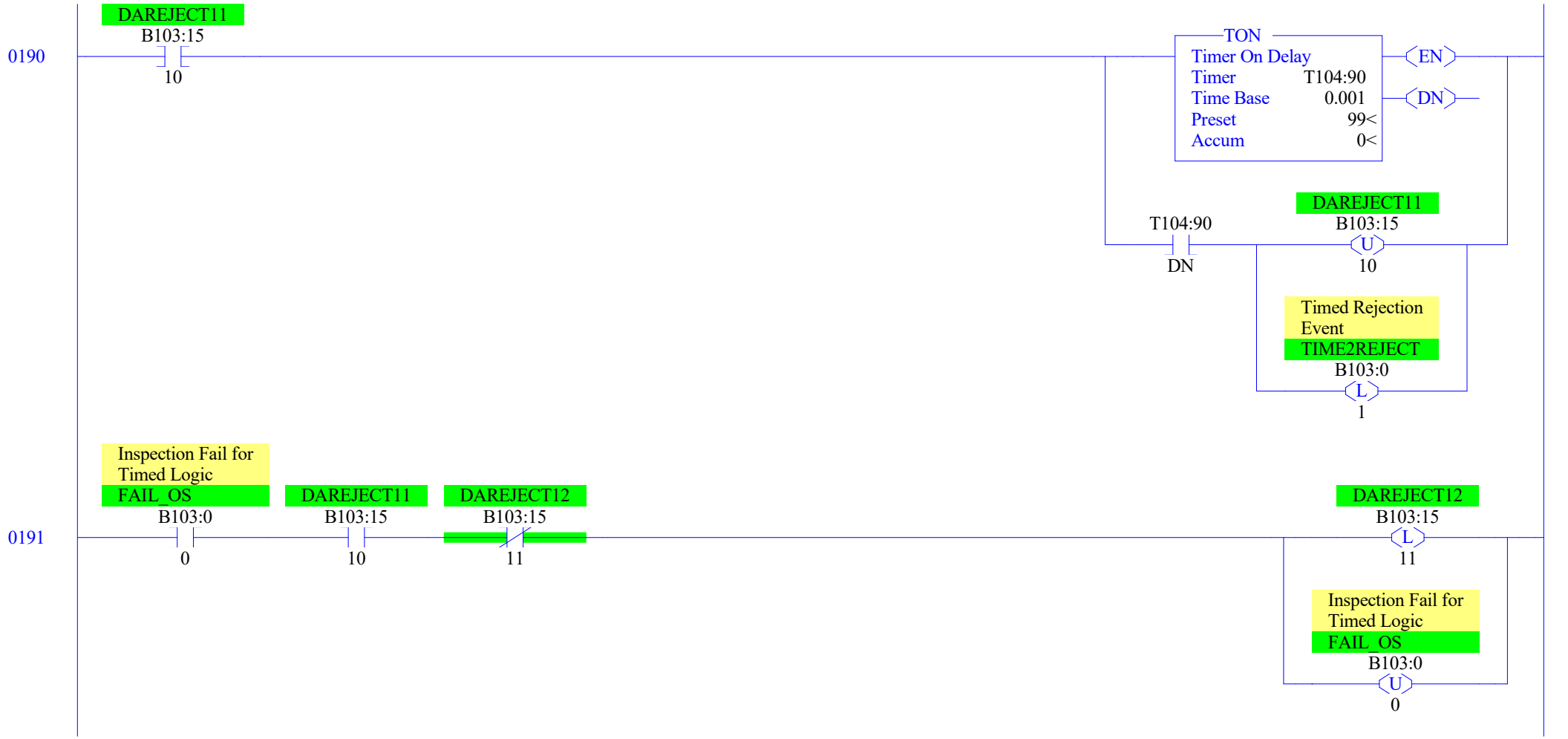


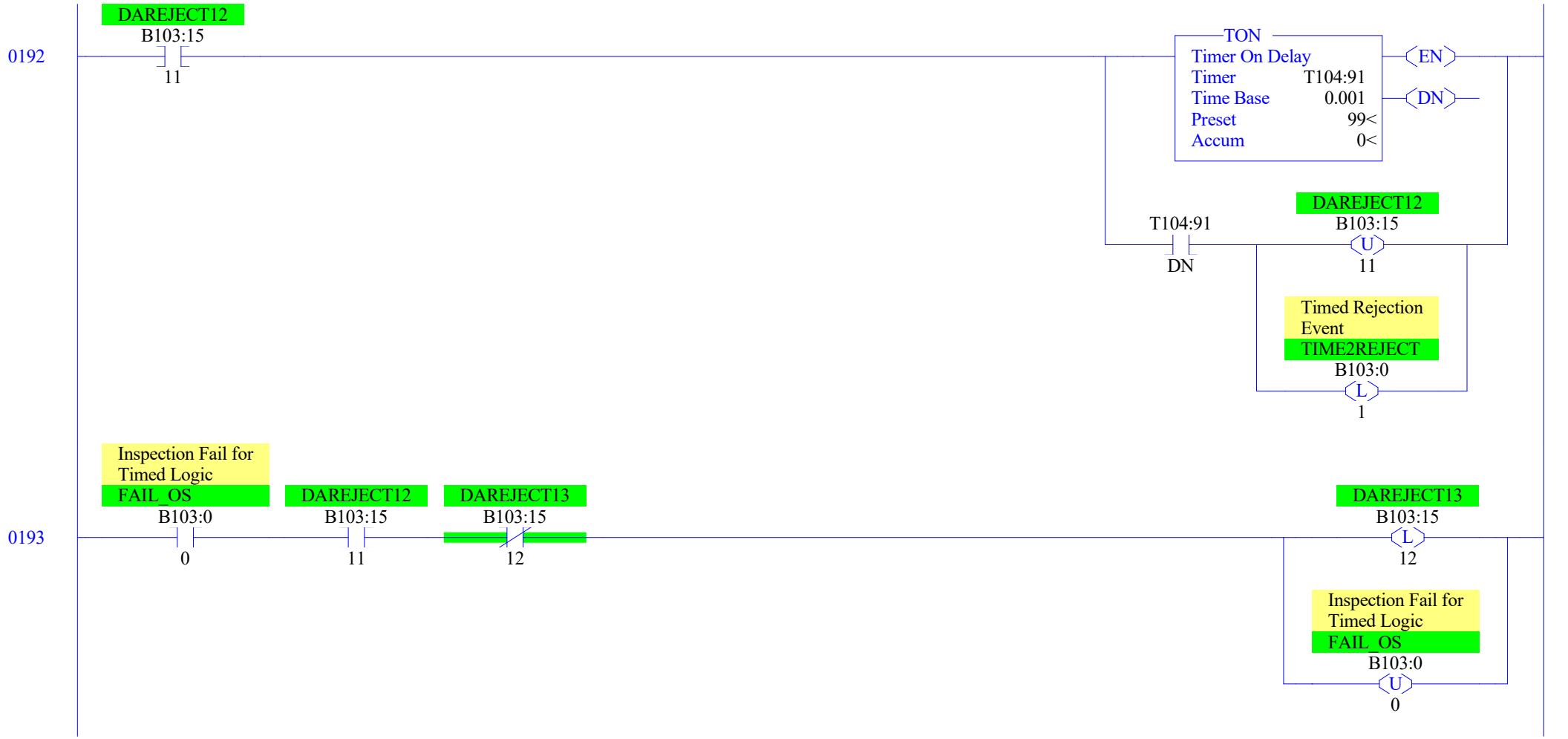
LAD 9 - REJ TIMERS --- Total Rungs in File = 235

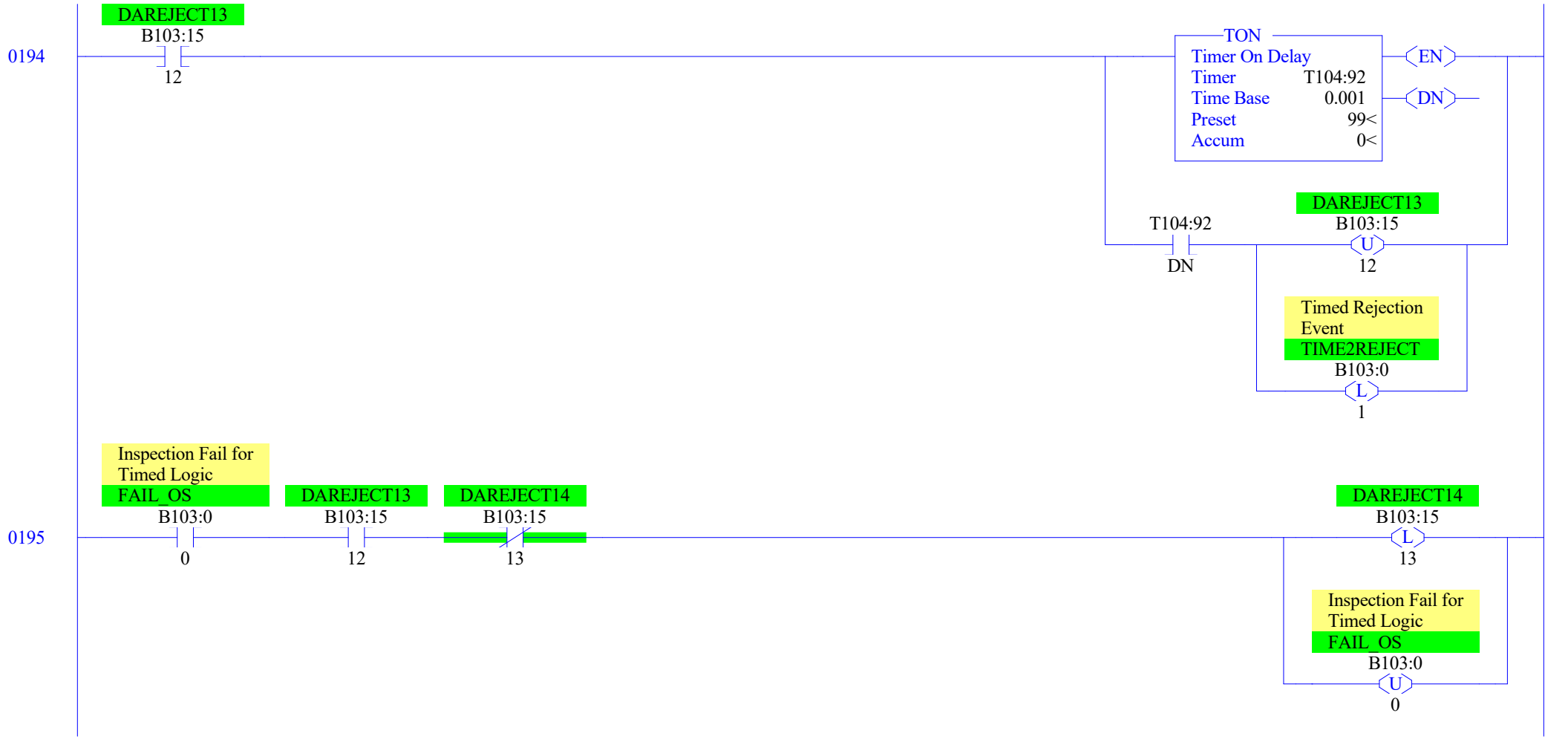


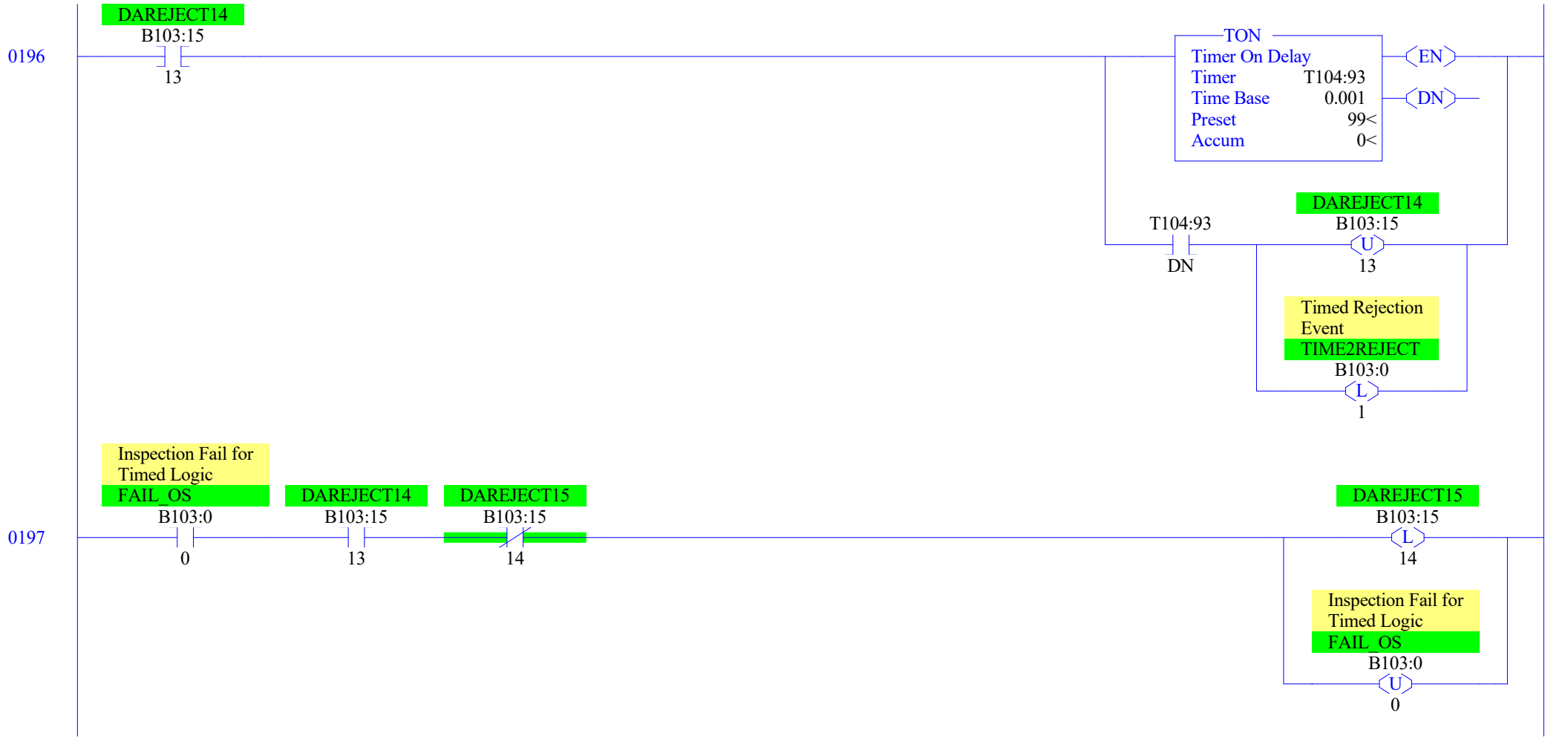
LAD 9 - REJ TIMERS --- Total Rungs in File = 235

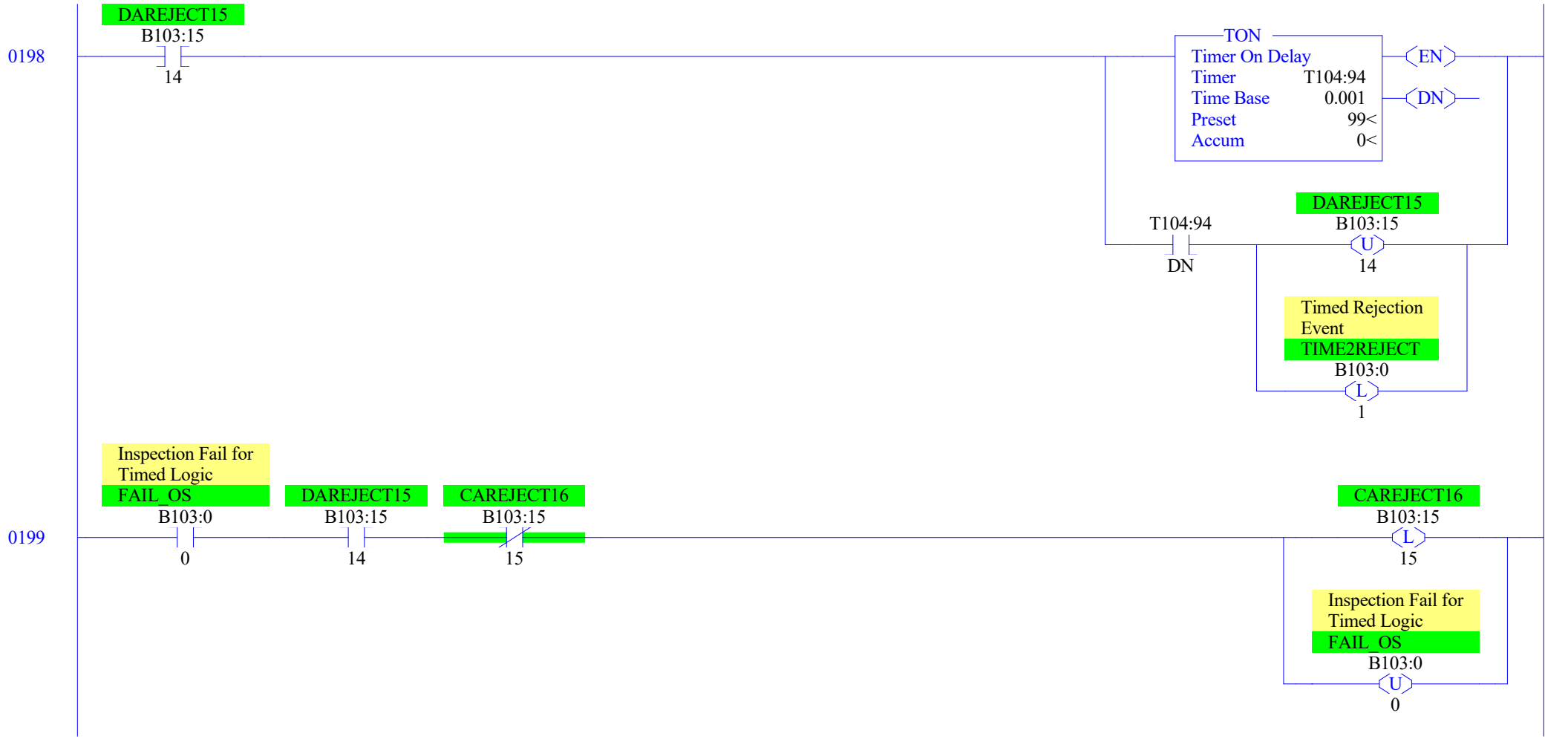


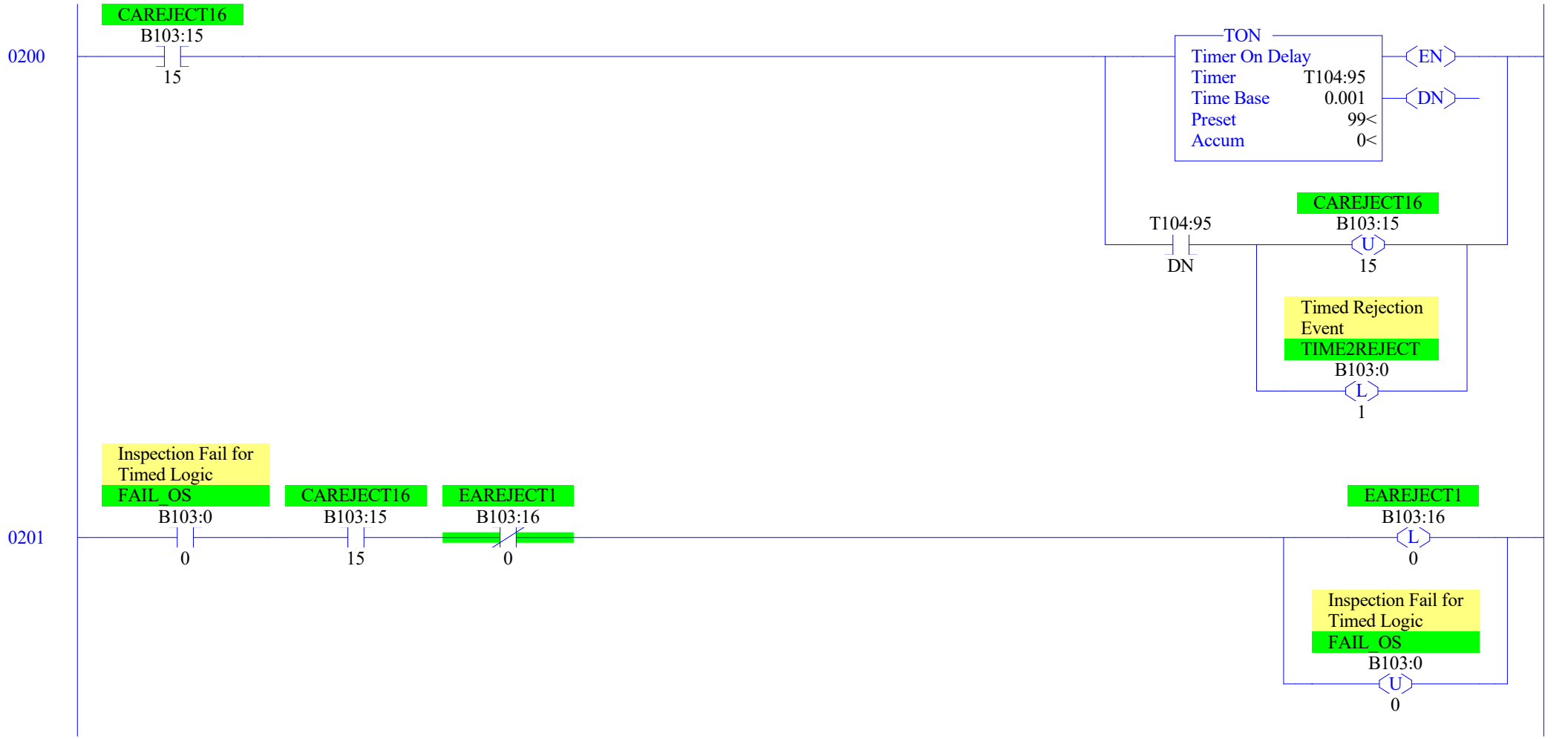

0190
DAREJECT11
B103:15
10
TON
Timer On Delay
Timer T104:90
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:90
DN
DAREJECT11
B103:15
U
10
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0191
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
DAREJECT11
B103:15
10
DAREJECT12
B103:15
11
DAREJECT12
B103:15
L
11
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

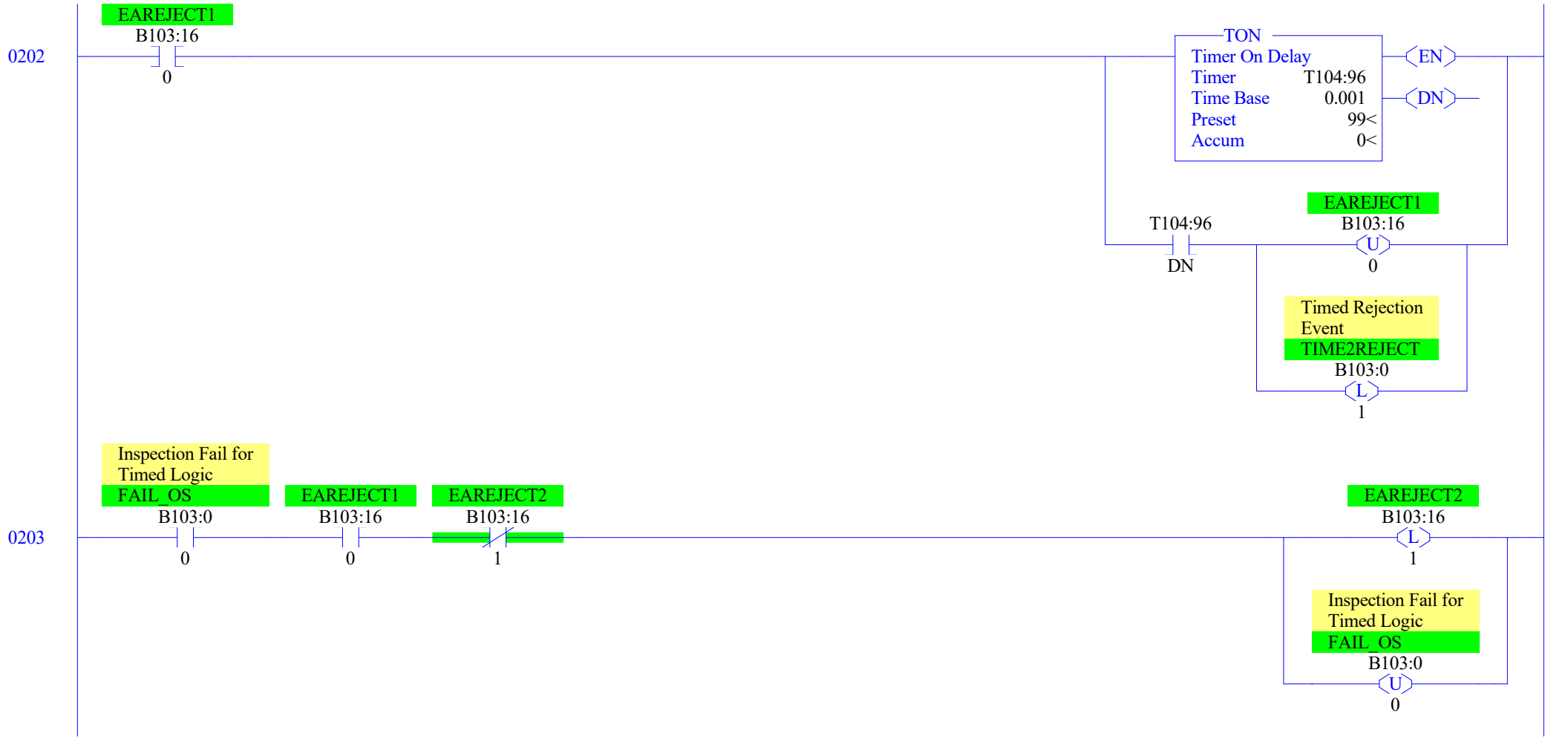

0192
DAREJECT12
B103:15
11
TON
Timer On Delay
Timer T104:91
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:91
DN
DAREJECT12
B103:15
U
11
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0193
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
DAREJECT12
B103:15
11
DAREJECT13
B103:15
12
DAREJECT13
B103:15
L
12
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

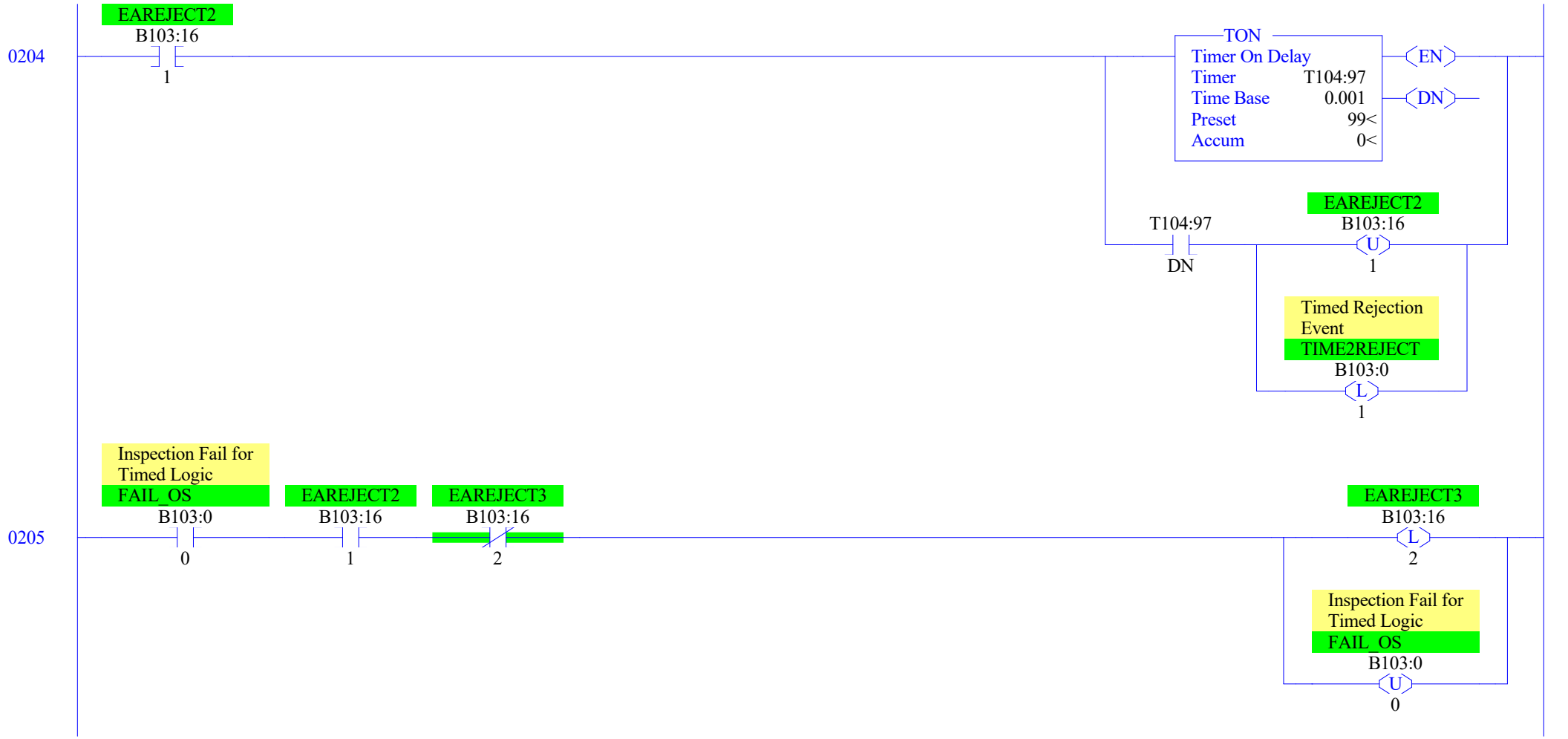

0194
DAREJECT13
B103:15
12
TON
Timer On Delay
Timer T104:92
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:92
DN
DAREJECT13
B103:15
U
12
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0195
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
DAREJECT13
B103:15
12
DAREJECT14
B103:15
13
DAREJECT14
B103:15
L
13
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

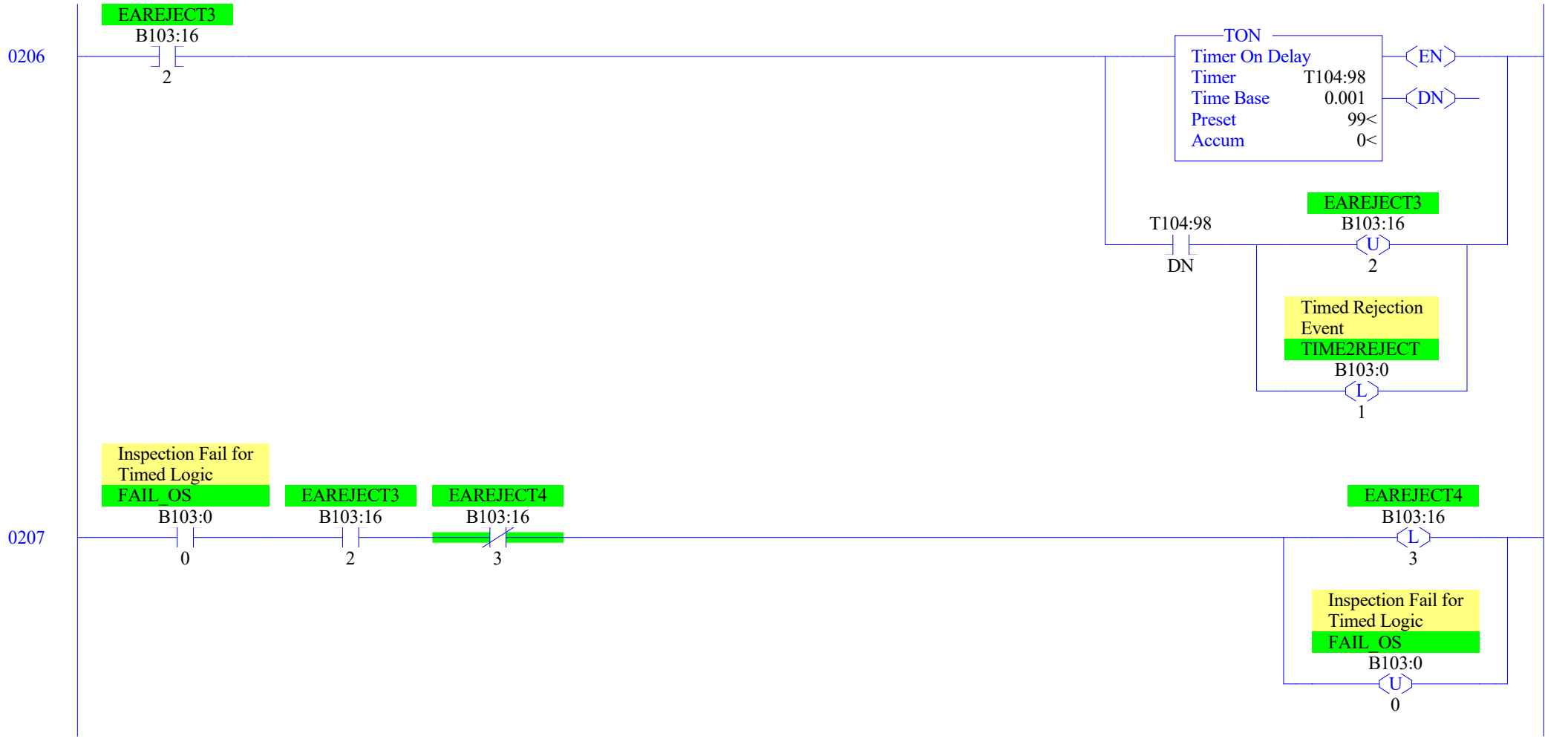

0196
DAREJECT14
B103:15
13
TON
Timer On Delay
Timer T104:93
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:93
DN
DAREJECT14
B103:15
U
13
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0197
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
DAREJECT14
B103:15
13
DAREJECT15
B103:15
14
DAREJECT15
B103:15
L
14
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

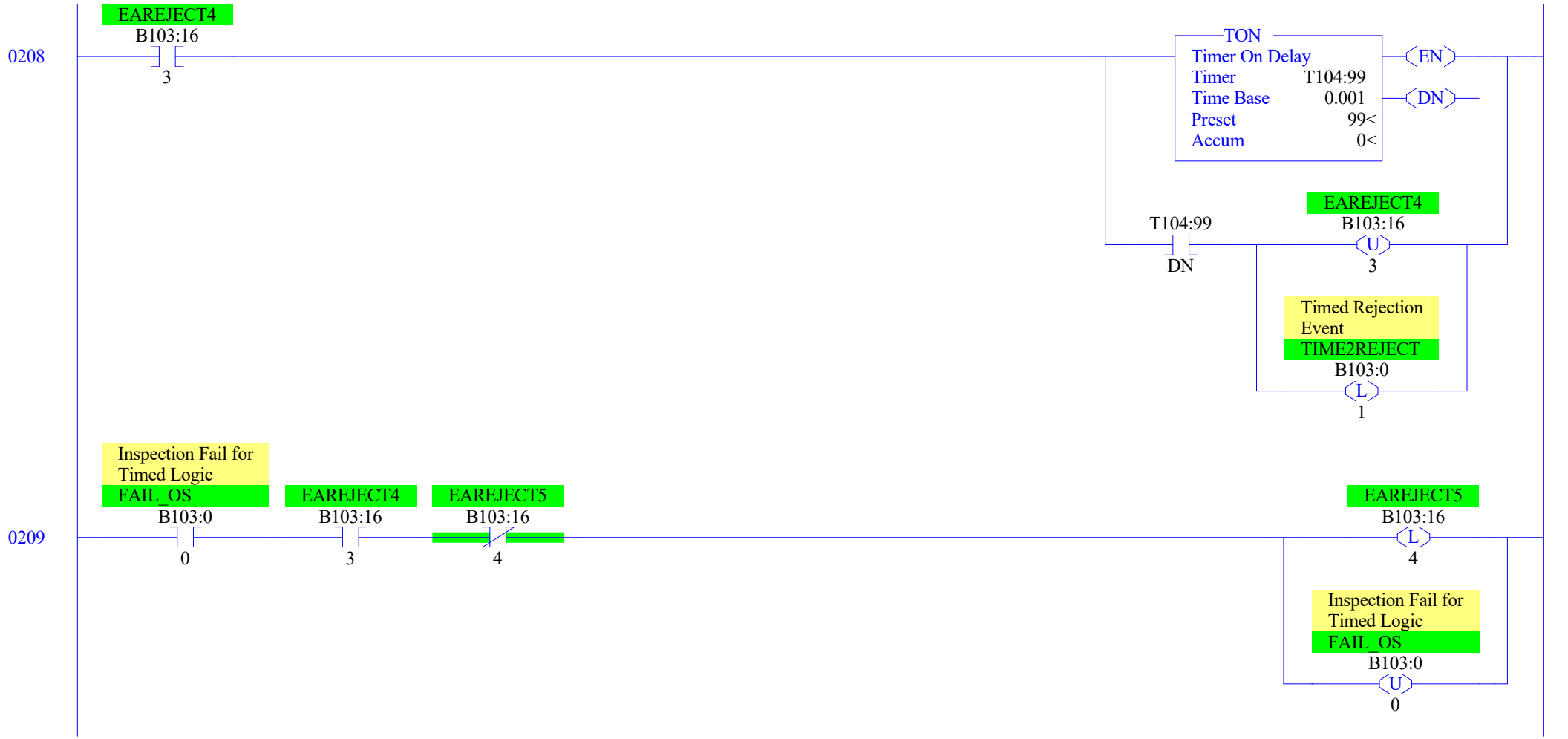

0198
DAREJECT15
B103:15
14
TON
Timer On Delay
Timer T104:94
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:94
DN
DAREJECT15
B103:15
U
14
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0199
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
DAREJECT15
B103:15
14
CAREJECT16
B103:15
15
CAREJECT16
B103:15
L
15
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

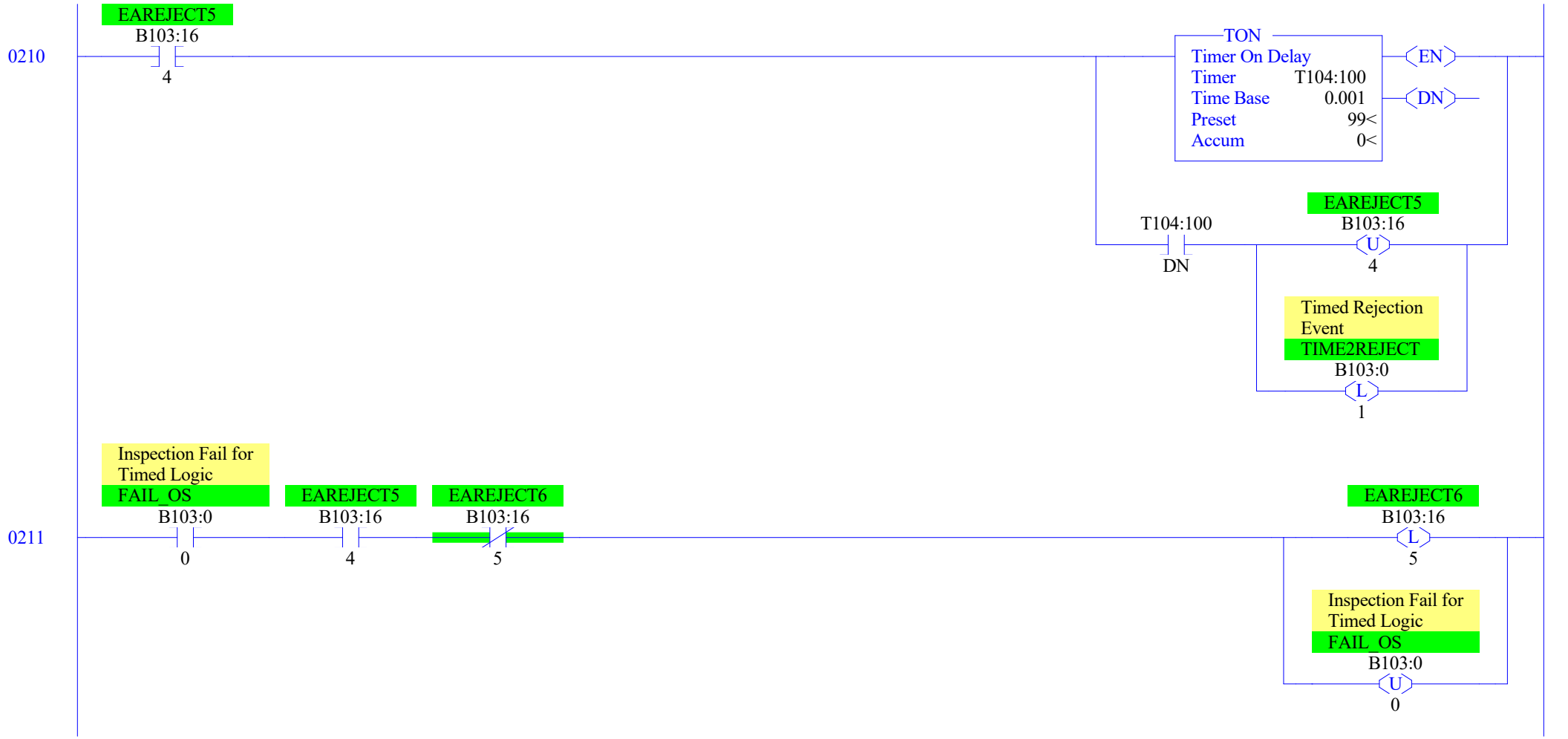

0200
CAREJECT16
B103:15
15
TON
Timer On Delay
Timer T104:95
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:95
DN
CAREJECT16
B103:15
U
15
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0201
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
CAREJECT16
B103:15
15
EAREJECT1
B103:16
0
EAREJECT1
B103:16
L
0
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

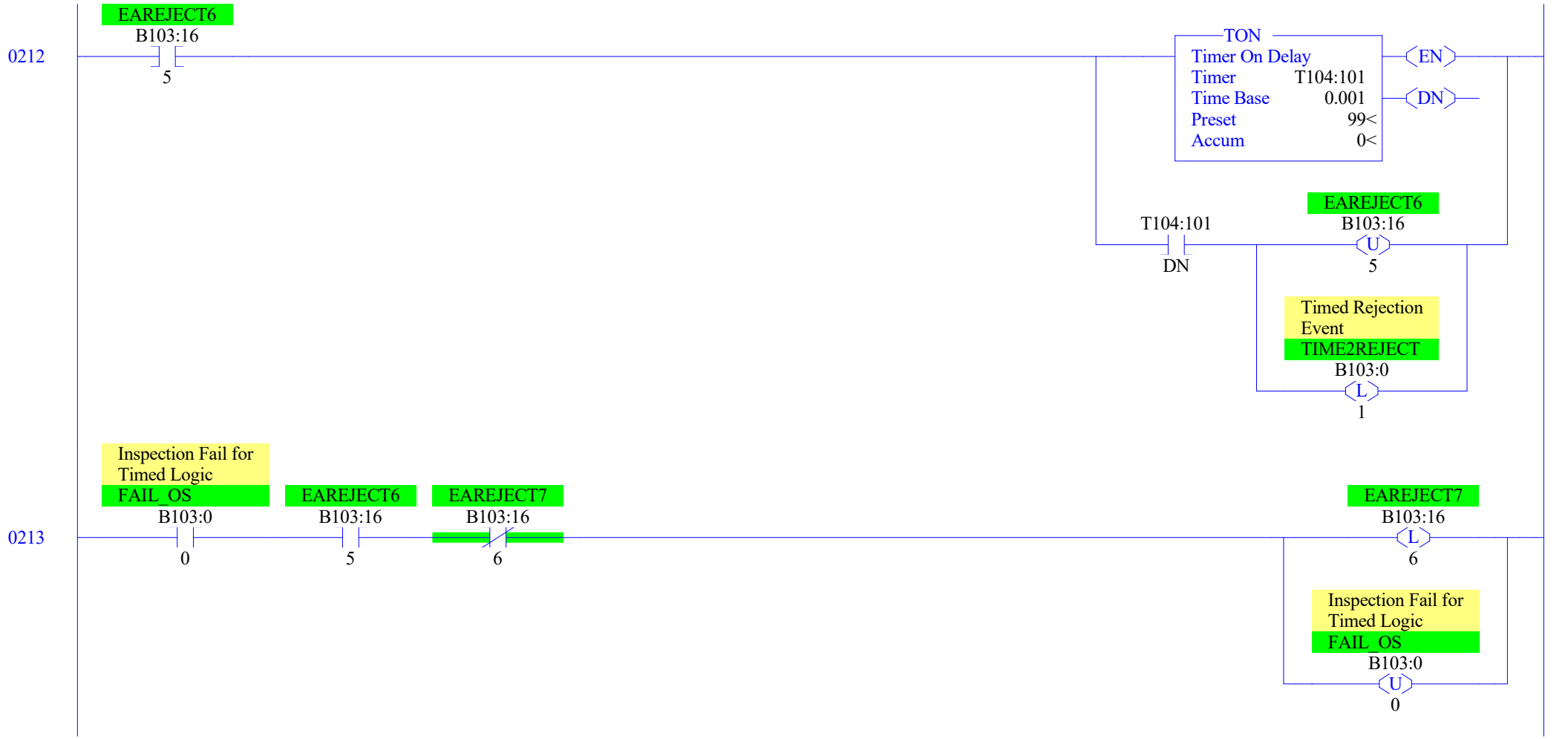

0202
EAREJECT1
B103:16
0
TON
Timer On Delay
Timer T104:96
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:96
DN
EAREJECT1
B103:16
U
0
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0203
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
EAREJECT1
B103:16
0
EAREJECT2
B103:16
1
EAREJECT2
B103:16
L
1
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

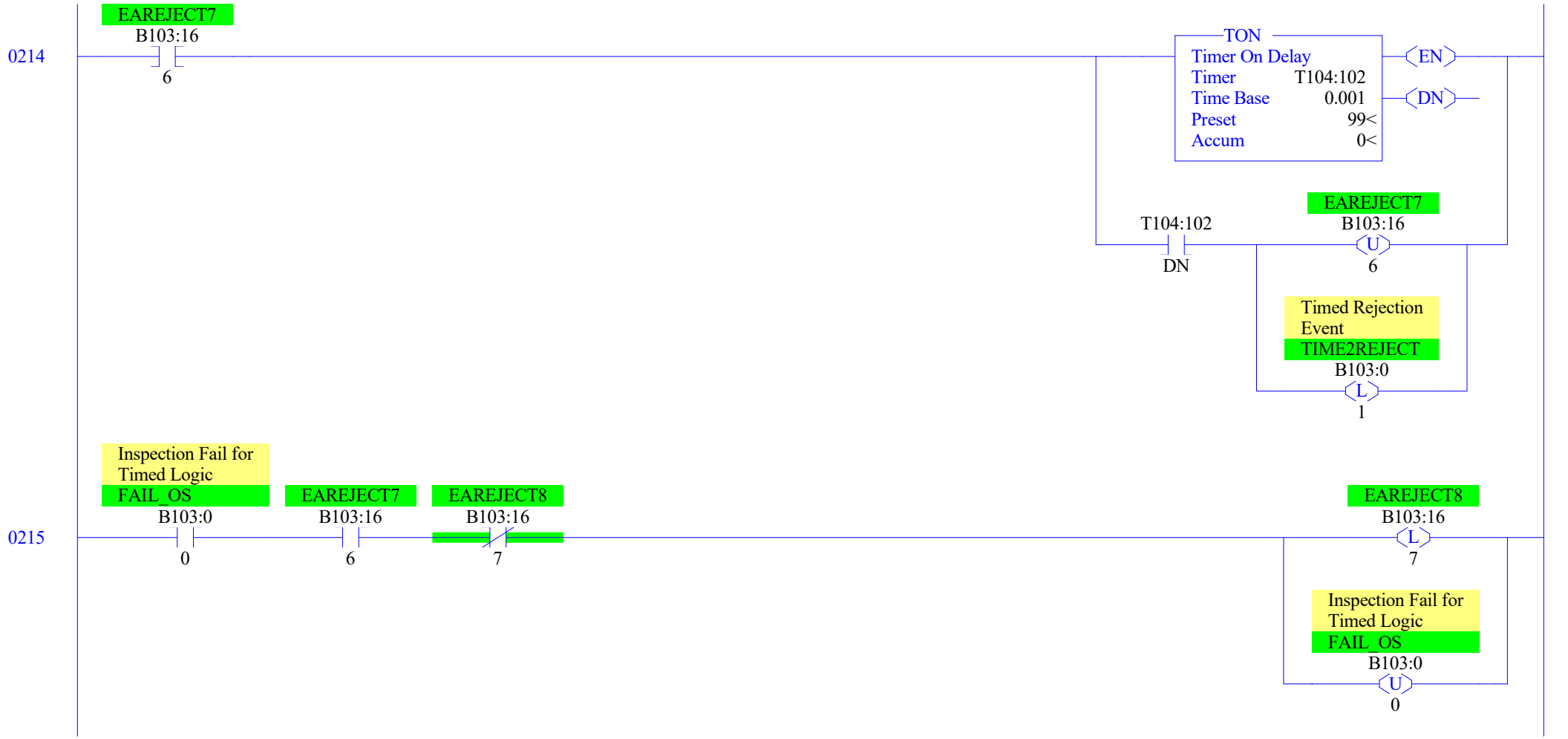

0204
EAREJECT2
B103:16
1
TON
Timer On Delay
Timer T104:97
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:97
DN
EAREJECT2
B103:16
U
1
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0205
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
EAREJECT2
B103:16
1
EAREJECT3
B103:16
2
EAREJECT3
B103:16
L
2
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

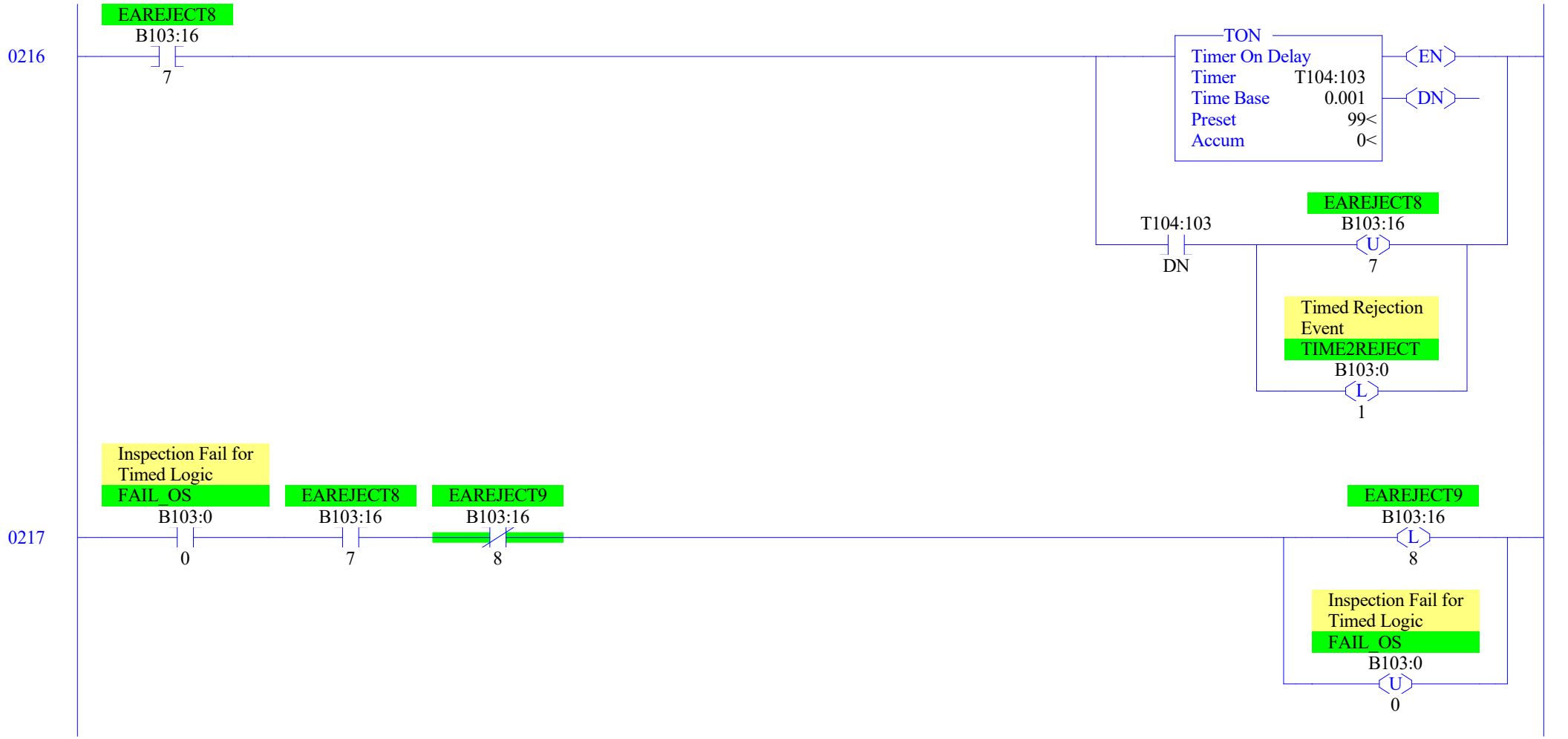

0206
EAREJECT3
B103:16
2
TON
Timer On Delay
Timer T104:98
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:98
DN
EAREJECT3
B103:16
U
2
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0207
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
EAREJECT3
B103:16
2
EAREJECT4
B103:16
3
EAREJECT4
B103:16
L
3
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

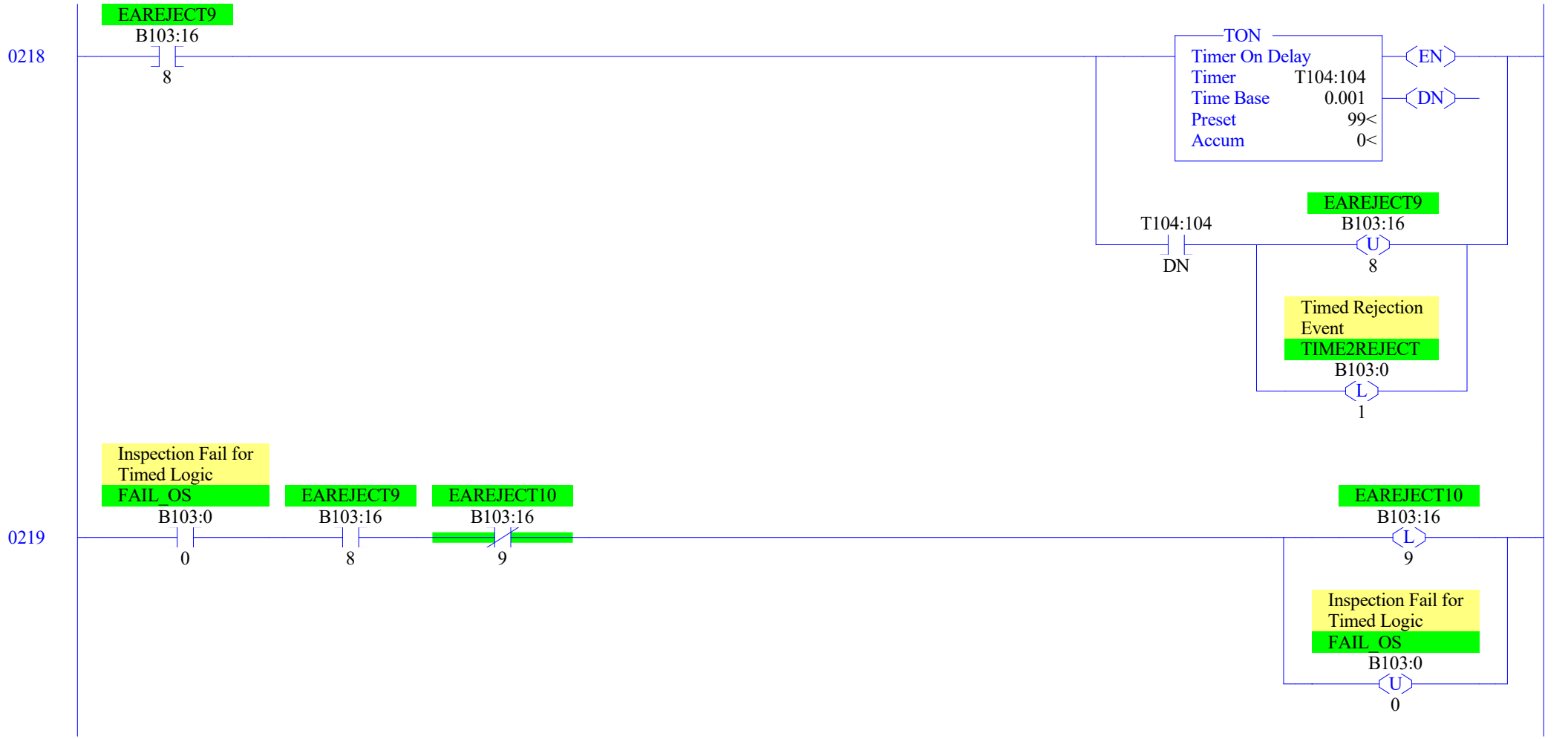

0208
EAREJECT4
B103:16
3
TON
Timer On Delay
Timer T104:99
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:99
DN
EAREJECT4
B103:16
U
3
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0209
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
EAREJECT4
B103:16
3
EAREJECT5
B103:16
4
EAREJECT5
B103:16
L
4
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

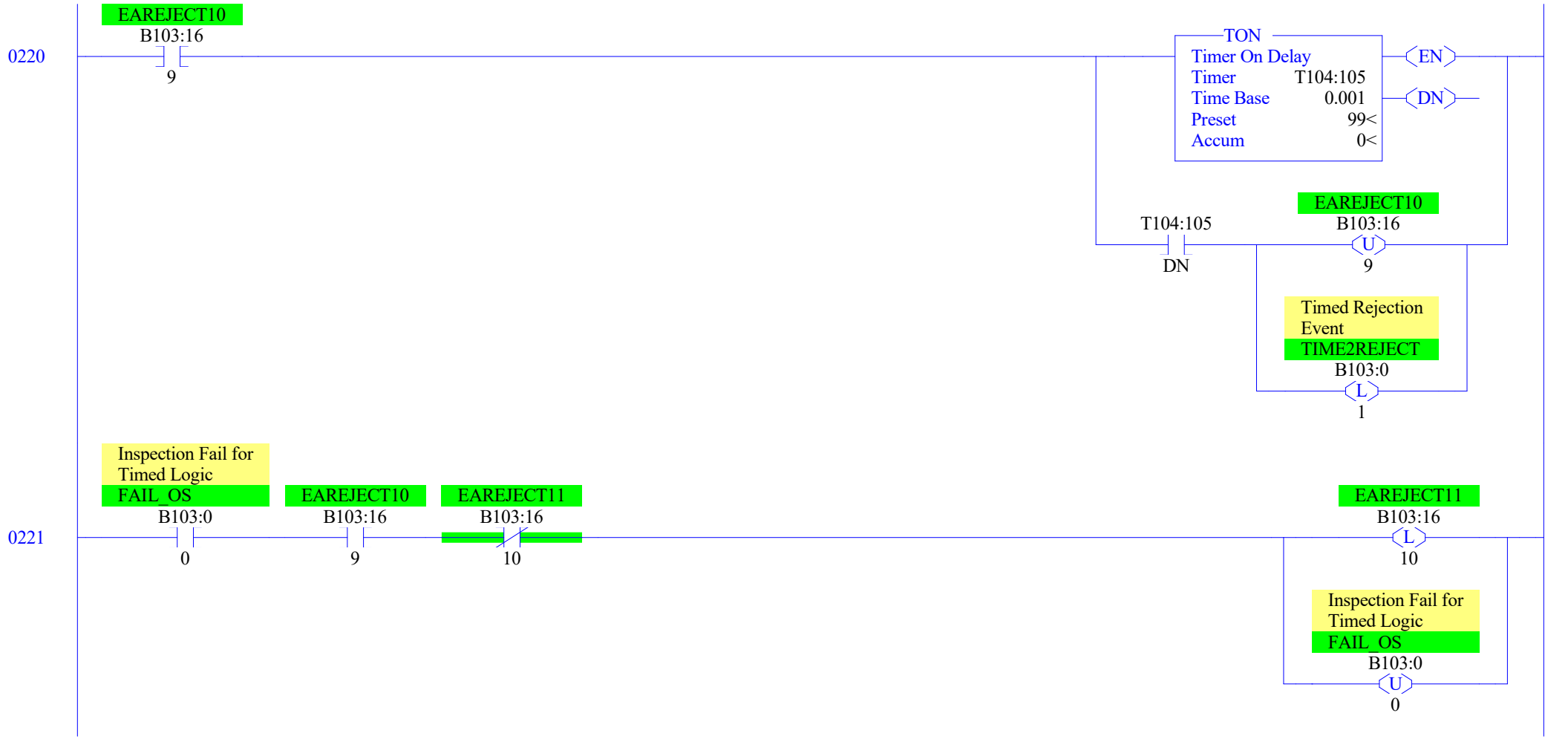

0210
EAREJECT5
B103:16
4
TON
Timer On Delay
Timer T104:100
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:100
DN
EAREJECT5
B103:16
U
4
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0211
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
EAREJECT5
B103:16
4
EAREJECT6
B103:16
5
EAREJECT6
B103:16
L
5
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

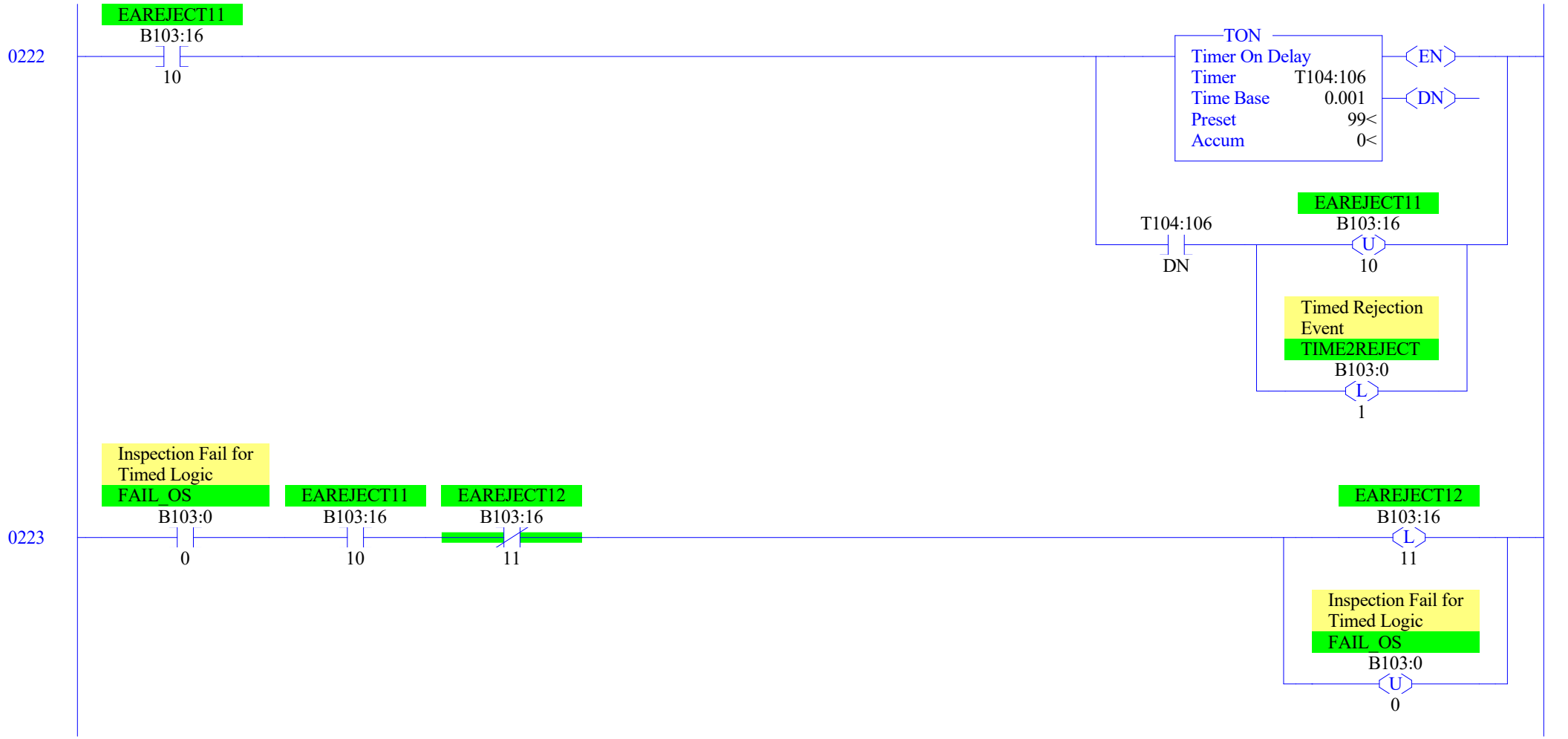

0212
EAREJECT6
B103:16
5
TON
Timer On Delay
Timer T104:101
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:101
DN
EAREJECT6
B103:16
U
5
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0213
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
EAREJECT6
B103:16
5
EAREJECT7
B103:16
6
EAREJECT7
B103:16
L
6
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

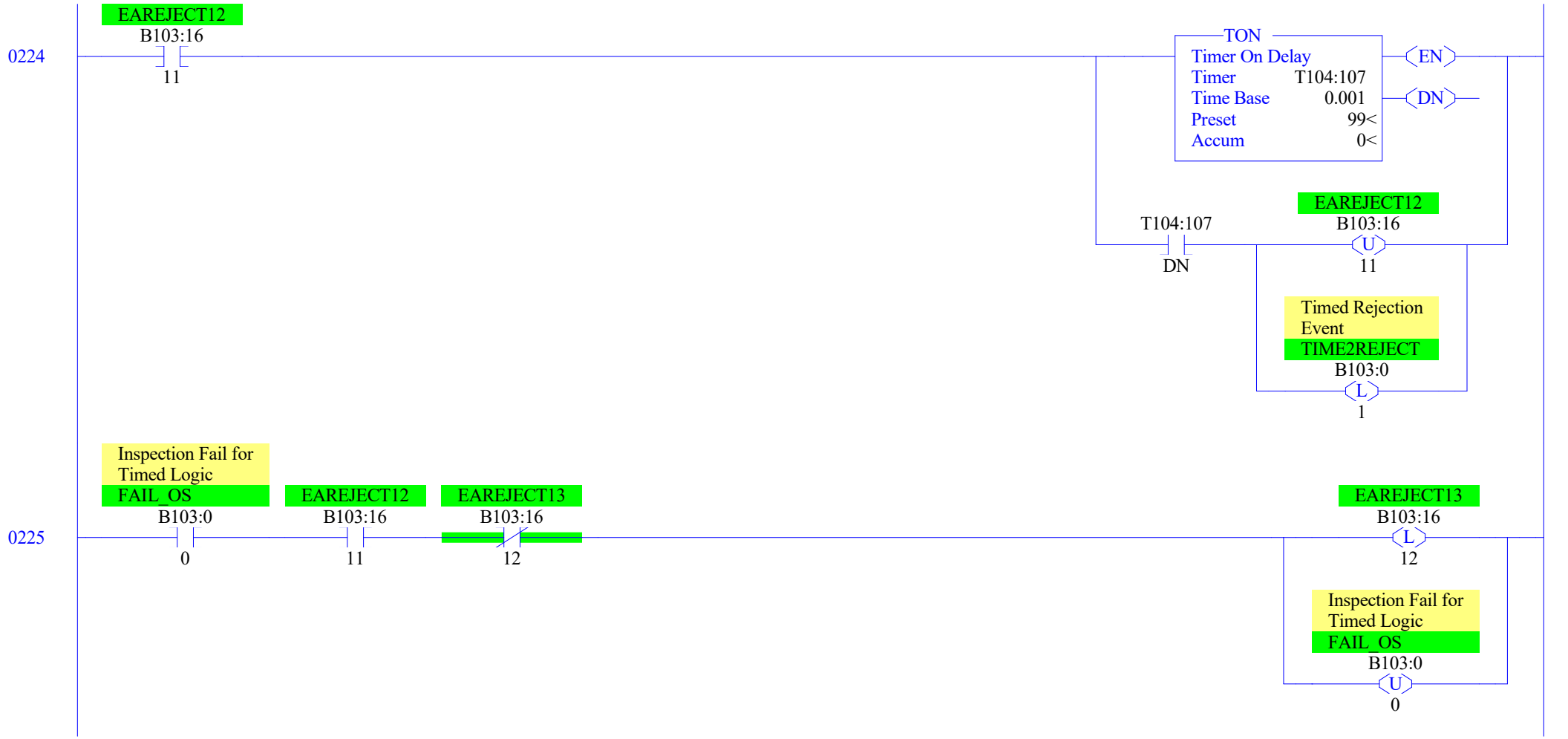

0214
EAREJECT7
B103:16
6
TON
Timer On Delay
Timer T104:102
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:102
DN
EAREJECT7
B103:16
U
6
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0215
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
EAREJECT7
B103:16
6
EAREJECT8
B103:16
7
EAREJECT8
B103:16
L
7
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

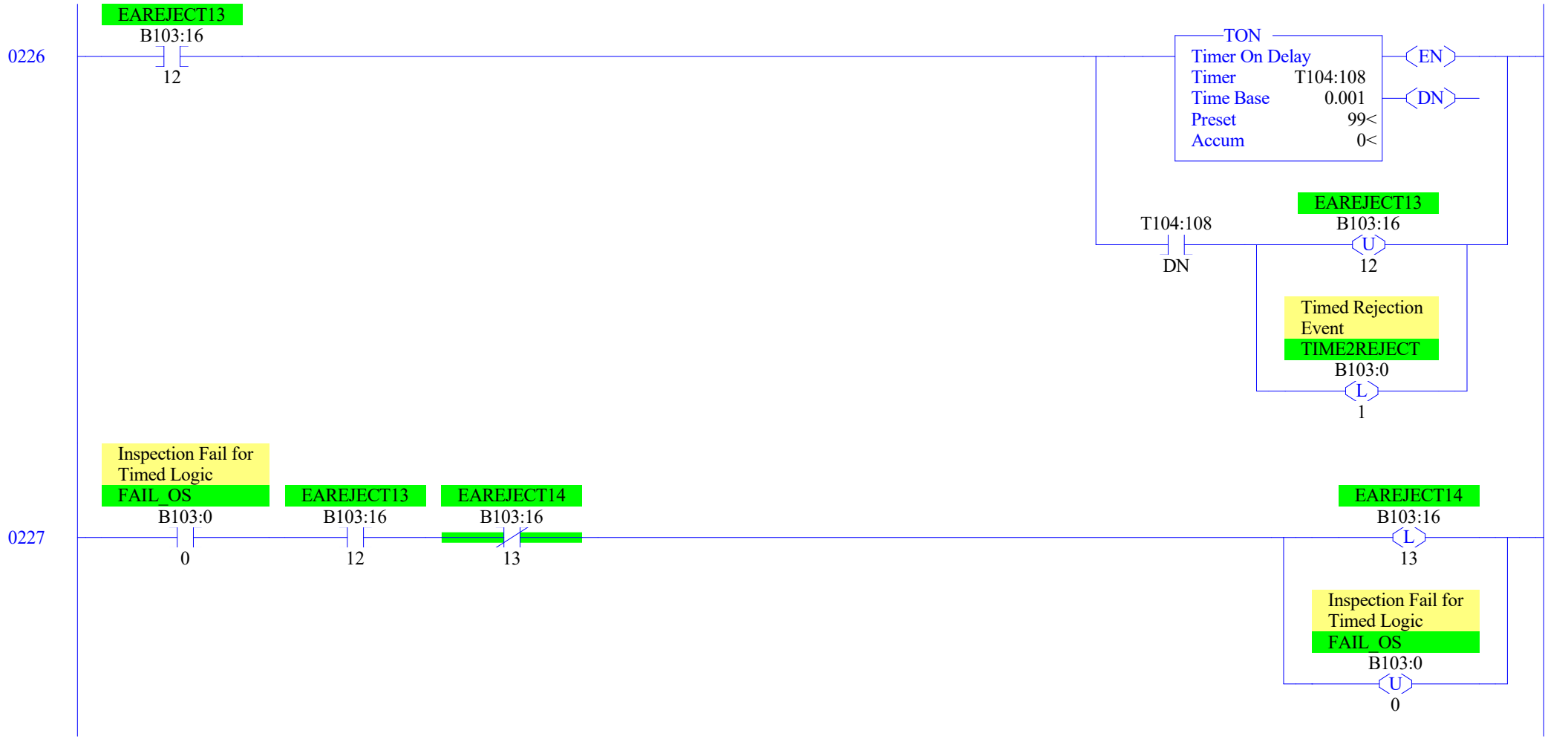

0216
EAREJECT8
B103:16
7
TON
Timer On Delay
Timer T104:103
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:103
DN
EAREJECT8
B103:16
U
7
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0217
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
EAREJECT8
B103:16
7
EAREJECT9
B103:16
8
EAREJECT9
B103:16
L
8
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

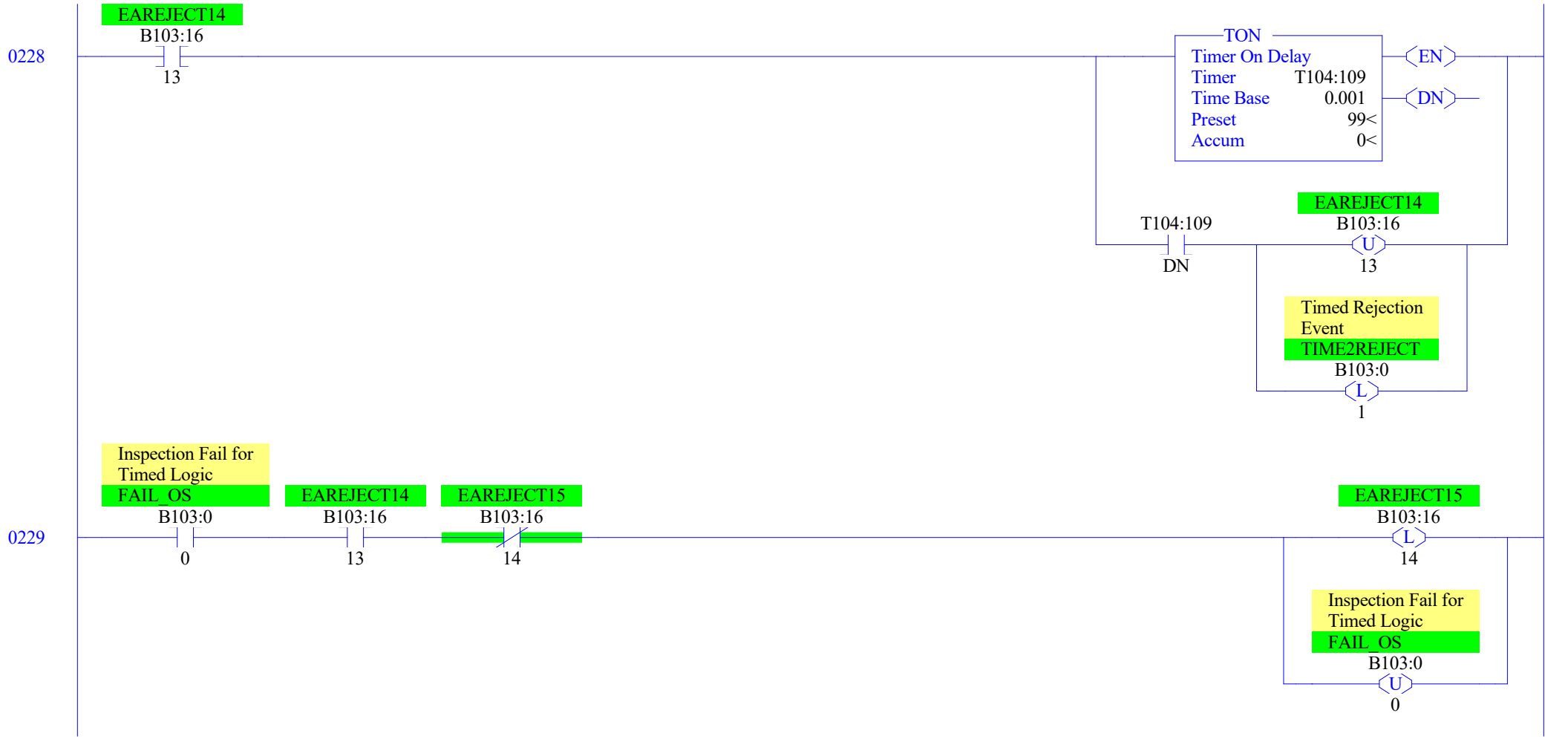

0218
EAREJECT9
B103:16
8
TON
Timer On Delay
Timer T104:104
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:104
DN
EAREJECT9
B103:16
U
8
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0219
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
EAREJECT9
B103:16
8
EAREJECT10
B103:16
9
EAREJECT10
B103:16
L
9
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0

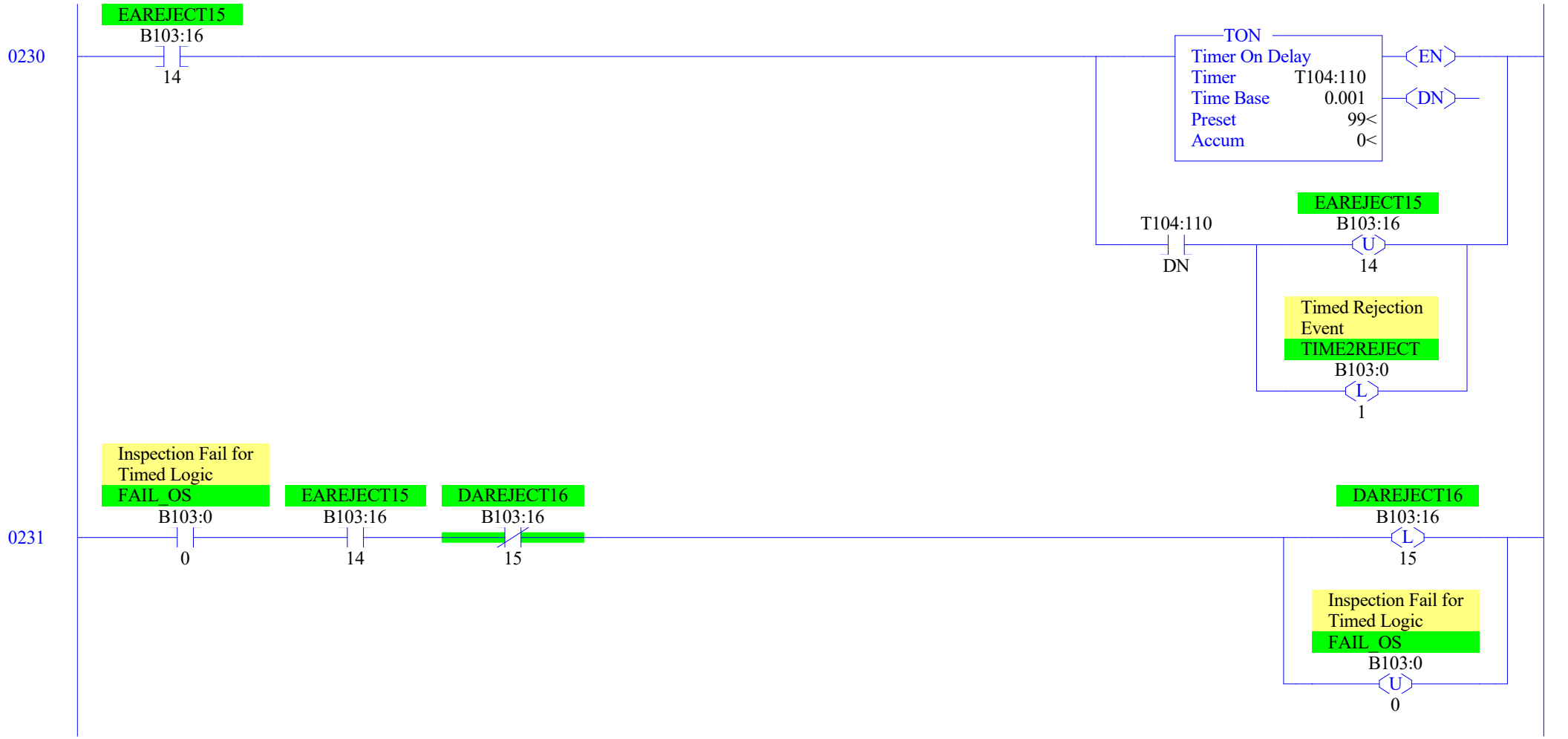

0220
EAREJECT10
B103:16
9
TON
Timer On Delay
Timer T104:105
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:105
DN
EAREJECT10
B103:16
U
9
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0221
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
EAREJECT10
B103:16
9
EAREJECT11
B103:16
10
EAREJECT11
B103:16
L
10
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0


0222
EAREJECT11
B103:16
10
TON
Timer On Delay
Timer T104:106
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:106
DN
EAREJECT11
B103:16
U
10
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0223
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
EAREJECT11
B103:16
10
EAREJECT12
B103:16
11
EAREJECT12
B103:16
L
11
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0


0224
EAREJECT12
B103:16
11
TON
Timer On Delay
Timer T104:107
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:107
DN
EAREJECT12
B103:16
U
11
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0225
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
EAREJECT12
B103:16
11
EAREJECT13
B103:16
12
EAREJECT13
B103:16
L
12
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0


0226
EAREJECT13
B103:16
12
TON
Timer On Delay
Timer T104:108
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:108
DN
EAREJECT13
B103:16
U
12
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0227
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
EAREJECT13
B103:16
12
EAREJECT14
B103:16
13
EAREJECT14
B103:16
L
13
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0


0228
EAREJECT14
B103:16
13
TON
Timer On Delay
Timer T104:109
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:109
DN
EAREJECT14
B103:16
U
13
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0229
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
EAREJECT14
B103:16
13
EAREJECT15
B103:16
14
EAREJECT15
B103:16
L
14
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0


0230
EAREJECT15
B103:16
14
TON
Timer On Delay
Timer T104:110
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:110
DN
EAREJECT15
B103:16
U
14
Timed Rejection Event
TIME2REJECT
B103:0
L
1
0231
Inspection Fail for Timed Logic
FAIL_OS
B103:0
0
EAREJECT15
B103:16
14
DAREJECT16
B103:16
15
DAREJECT16
B103:16
L
15
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0


0232
DAREJECT16
B103:16
15
TON
Timer On Delay
Timer T104:111
Time Base 0.001
Preset 99<
Accum 0<
EN
DN
T104:111
DN
DAREJECT16
B103:16
U
15
Timed Rejection Event
TIME2REJECT
B103:0
L
1
Inspection Fail for Timed Logic
FAIL_OS
B103:0
U
0
0233
0234
END

Obsolete Program File routine?

0000 END

HSC0 Interrupt Routine: accumulate encoder counts; shift accept/reject bits

This Program File is executed, once, on each event when the count of encoder pulses in the value of the High-Speed Counter accumulator (HSC:0.ACC) reaches the HSC High Preset value (HSC:0.HIP). The HSC will automatically reset the HSC accumulator to 0 on each such event, because the HSC Mode (HSC:0.MOD) is 0.

A typical value for HSC:0.HIP seems to be 30, but it is assigned from the value of the integer ENCODER_HIPRESET_SP (N7:11) in the INSPECTION routine (LAD 4) at Rung 0002. whenever

1) the bit USE_ENCODER (B3:0/11) is 1, and
2) ENCODER_HIPRESET_SP differs from HSC:0.HIP.

Both USE_ENCODER and ENCODER_HIPRESET_SP originate in the GUI HMI..

The HSC function is only enabled (HSC:0/FE) when USE_ENCODER is 1, per the assignment of HSC:0/FE in MAIN_PROG routine (LAD 2) Rung 0002.

==========

Rung 0000 adds the HSC High Preset value to the value of a working register, which register will, at regular intervals (300ms)*, be

1) Scaled to estimate the line speed, and
2) Cleared to 0.0 to initialize the estimate for the next interval

* Program File routine LAD 13 STI_SPEED, via Selectable Timed Interrupt

WORKING_REGISTER

0000

ADD

Add	
Source A	HSC:0.HIP
	30<
Source B	F18:11
	0.0<
Dest	F18:11
	0.0<

Shift bits left in the bitstream (B11) left by one bit per interrupt

The value of the new bit (B13:1/0) loaded here (B11:0/0) is 0 i.e. we assume the can at "location" B11:0/0, which location models that of the inspection cameras, is not a reject; once that 0 is in place, on the rising edge of a reject event from a camera between now and the next HSC0 interrupt, that bit's value is changed to 1 at Rung 0005 of Program File routine LAD 4 INSPECTION.

0001

BitShift Left 1
Control Register

BSL
Bit Shift Left
File #B11:0
Control R16:0
Bit Address B13:1/0
Length 2000<

EN
DN

Clear the /EN bit of the control register, so the BSL instruction above will "detect" a rising edge of its input rung when the next HSC0 interrupt executes this routine.

0002

BitShift Left 1
Control Register
R16:0
U
EN

BitShift Left 1
Control Register
R16:0
U
DN

0003

END

LAD 12 - EII_COUNTS - count events to determine speed --- Total Rungs in File = 1

Event Interrupt - obsolete Program File routine

See Function Files => EII:0 (Event Input Interrupt)

- EII:0.PFN (Program File Number) was probably 12 at one point
- EII:n.EIE (Event Interrupt Enable) is now 0 for all n (0-3) => all Event Input Interrupts are disabled

0000 END

Estimate motor speed in RPM

This Program File routine is executed at regular intervals (300ms) via Selectable Timed Interrupt (STI)

Pulses have been accumulating into the value of WORKING_REGISTER by the
High-Speed Counter Interrupt 0 routine (LAD11 HSC0).

==========

Determine number of pulses per minute.
This logic scans every 300 milliseconds so multiply the accumulated number of pulses by 200
to calculate the number of pulses per minute

CALCD_PPM

0000

MUL
Multiply
Source A F18:11 0.0<
Source B 200.0 200.0<
Dest F18:14 0.0<

Clear number of pulses in WORKING_REGISTER to start the accumulation for the next STI event

WORKING_REGISTER

0001

CLR
Clear
Dest F18:11 0.0<

Move the calculated linespeed from the last STI execution of this routine (F8:15; RPM) to the previous calculated linespeed (F8:16)

PREV_LINESPEED

0002

MOV
Move
Source F18:15 0.0<
Dest F18:16 0.0<

Divide pulses/minute by 100pulses/revolution to get current calculated linespeed (F8:15; RPM)

0003

CURR_LINESPEED

DIV

Divide	
Source A	F18:14
	0.0<
Source B	100.0
	100.0<
Dest	F18:15
	0.0<

Average the current and previous calculated linespeeds to use as the estimated linespeed (F8:10; RPM)

0004

AVE_LINESPEED

ADD

Add	
Source A	F18:15
	0.0<
Source B	F18:16
	0.0<
Dest	F18:10
	0.0<

AVE_LINESPEED

DIV

Divide	
Source A	F18:10
	0.0<
Source B	2.0
	2.0<
Dest	F18:10
	0.0<

0005

END