

1-1 General Description

1-1-1 Introduction

Based on a detailed analysis of device applications, the MN10200 Series Linear Address Edition has adopted a new architecture for C language program development. Under various user system requirements including miniaturization and energy conservation, the MN10200 Series Linear Address Edition makes it possible to develop a system with high speed and high function that surpass conventional standards.

The MN1020012 16-bit microcontroller, equipped with an abundance of peripheral function and a memory interface that supports DRAM and pseudo-SRAM, can realize exceptional real-time control performance in a wide variety of fields such as printers, electronic instruments, audiovisual equipment, household electric appliances, automobiles, robotics, cellular telephones, and computer peripheral devices.

The conventional memory-to-memory computing accumulator method used in this company's main series has been replaced by a register-to-register computing load/store architecture method. One-byte, one-machine cycle basic instructions are used to minimize code size and to improve the compiler efficiency. A circuit design method that utilizes half-micron technology is used to realize optimized hardware and low power consumption of the system.

1-1-2 Features

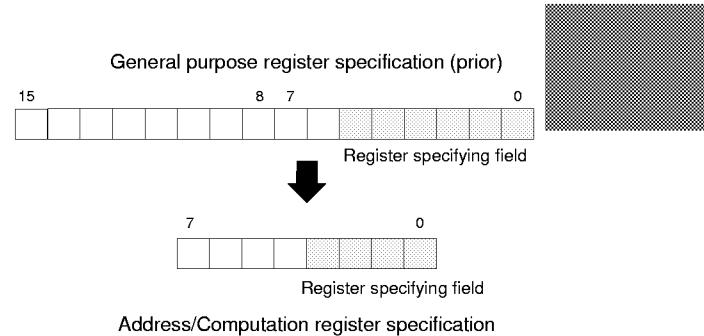
As a microcomputer for device applications, the MN10200 Series Linear Address Edition with its flexible, optimized hardware configuration and simple, highly efficient instructions realizes economy and high speed.

1. Linear Addressing Method for Large Scale Systems

A linear addressing method has been adopted that supports an address space - maximum 16 Mbyte. The hardware configuration has been optimized for large scale systems. There is no distinction between memory and instruction spaces, and operation is possible with common, shared instructions.

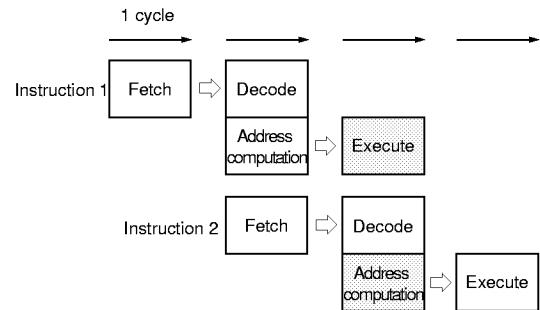
2. Basic Instruction Word Length of One Byte

Instead of conventional general purpose registers, 8 registers inside the CPU are separated by function into 4 address registers (A0~A3) and 4 data registers (D0~D3). The register specifying field is 4 bits or less, and the code size of frequently used basic instructions such as load/store as well as register-to-register computing is defined as one byte.



3. High Speed Pipelined Processing

In this series, high speed processing of instructions is performed by a three-stage pipeline (1. instruction fetch, 2. decode, 3. execute). Thus the shortest instruction execution time of one byte per machine cycle (100ns at 20MHz oscillation) is achieved.

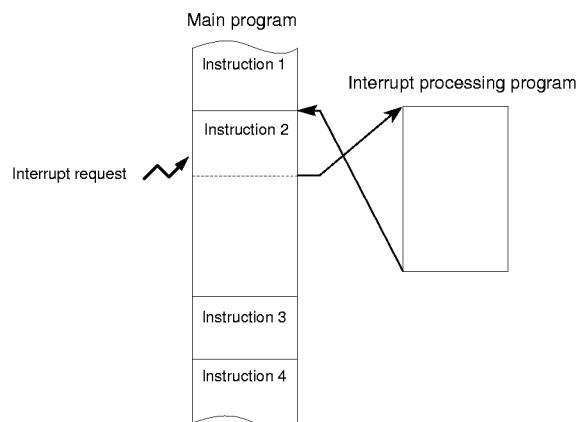


4. Simple Instruction Organization

Based on analysis of a programming model for device applications, the instruction set was carefully screened to comprise 36 simple instructions. In order to compress the code size, instructions have a variable word length of 1~5 bytes. Basic instructions frequently used in C compilers are one byte long.

5. High Speed Interrupt Response Mechanism

A quick response to interrupts is possible by halting the instructions, even during the execution of long cycle instructions. After an interrupt is generated, program control transfers to the interrupt processing routine within a maximum of 11 cycles. Since the interrupt handler processing is performed by software, interrupt processing can be tuned for higher speed depending upon user requirements. This will improve the real time control performance.



6. Flexible Interrupt Control Structure

The interrupt controller is layered into 11 groups of which Group 0 is reserved for NMI. Each group responds to a maximum of 4 interrupt conditions, up to a total of 38. Seven levels of interrupt priority can be set for each group, contributing to the design freedom and precise control by software. The software for previous Panasonic peripheral modules can also be used.

7. High Speed and Highly Functional External Interface

The MN1020012 is quipped with external interfaces such as DMA functions, handshaking functions, bus arbitration functions, etc.

8. C Language Development Environment

A simple, optimized hardware configuration for C language programs coupled with a C compiler that generates highly efficient code provides an environment to develop C language programs for device applications without increasing the program size. The **PanaXSeries** supports development tools.

9. Remarkably Low Power Consumption

Due to thoroughly optimized circuit design such as a divided internal bus to reduce or distribute the bus load capacity of the internal bus, miniaturization, and low power processes, power consumption is remarkably lower compared with previous products. Also, three types of energy conserving modes are supported: SLOW, HALT, and STOP modes. (Note that SLOW mode is not supported by the MN1020012.)

1-1-3 Overview

The basic configuration and functions of this series are described below.

■ Address Space

A linear addressing method has been adopted that supports a 16 Mbyte (max.) address space. There is no distinction between instruction space and data space. In the basic configuration, the internal RAM, control registers for internal peripheral functions, etc. are located in the first 64 Kbyte space. Corresponding to the product type and size of the user program, there are three memory modes shown in table 1-1-1.

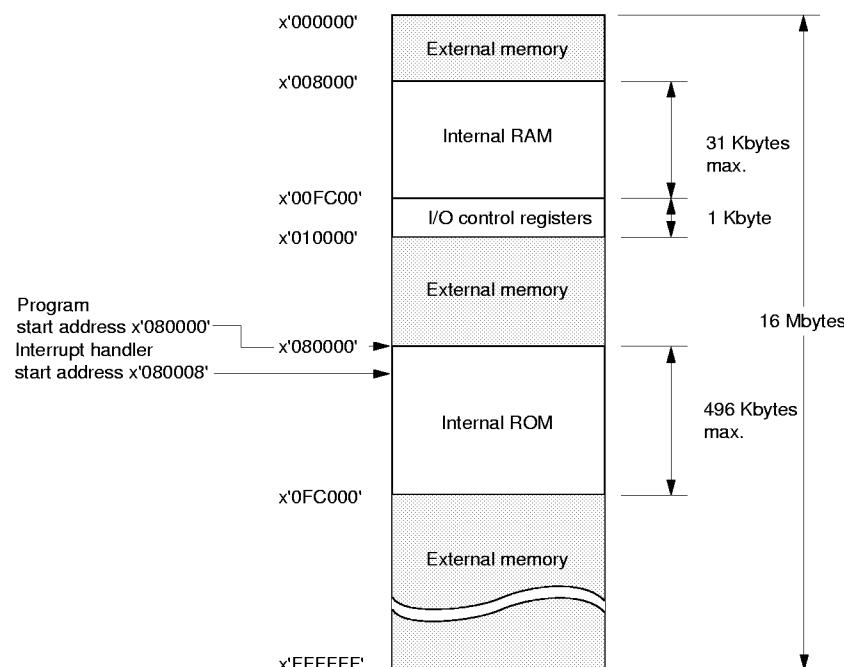


Figure 1-1-1 Address Space

This is a general example of the memory expansion mode.

The ending address of internal RAM is fixed (x'00FBFF'). The starting address will change depending upon the size. (A size of 31 Kbytes is shown in the figure.)

Since the MN1020012 has no internal RAM, access is prohibited in the area x'00F000'~x'00FBFF'.

The starting address of internal ROM is fixed (x'080000'). The ending address will change depending upon the size. (A size of 496 Kbytes is shown in the figure.)

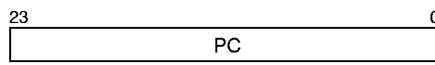
Table 1-1-1 Memory Modes

Mode	Address Bit Width	Internal ROM Capacity
Single step mode		16 Kbytes or greater
Memory expansion mode	24 bits maximum	
Processor mode		None

The MN1020012 only supports the processor mode.

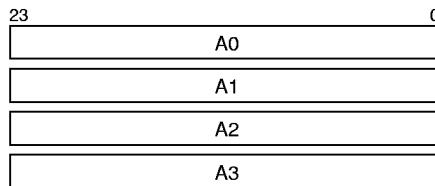
■ Configuration of Internal Registers, Memory, and Special Registers

Program Counter



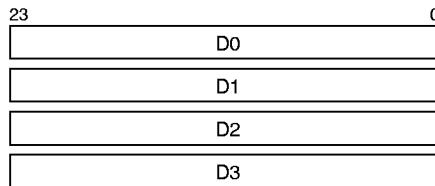
Specifies the program address (24 bits) during execution.

Address Registers

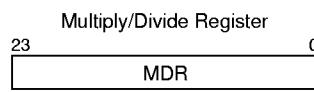


Address registers specify the location of data in memory. Of the 4 registers, A3 is allocated as the stack pointer.

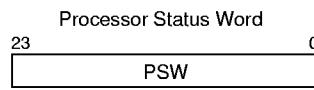
Data Registers



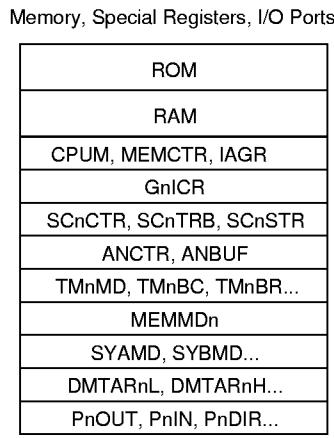
The data registers perform all arithmetic and logical operations. In the case of byte (8-bit) or word (16-bit) transfers between memory or another register, the contents are zero extended or sign extended, depending upon the instruction.



This register is used only for multiplication and division. When executing a multiply instruction, the upper 16 bits of the 32-bit result are stored. Before executing a divide instruction, the upper 16 bits of the 32-bit dividend are stored. After execution, the 16-bit remainder result is stored.



This register indicates the CPU status. The arithmetic result flags, interrupt mask levels, etc. are stored.



Memory (ROM, RAM), special registers for controlling peripheral functions, and I/O ports are assigned the same address space.

- Internal control registers
- Interrupt control registers
- Serial interfaces
- A/D converter
- Timers/Counters
- Memory control
- Stepping motor control
- DMA controller
- I/O ports

■ Interrupt Controller

With the exception of reset, non-maskable and maskable interrupts are controlled by an interrupt controller (groups 0~10) located outside the CPU core. A maximum of 4 interrupts are allocated to each group. Seven levels of interrupt priority (sequence of priority for receiving interrupts) can be specified for each group.

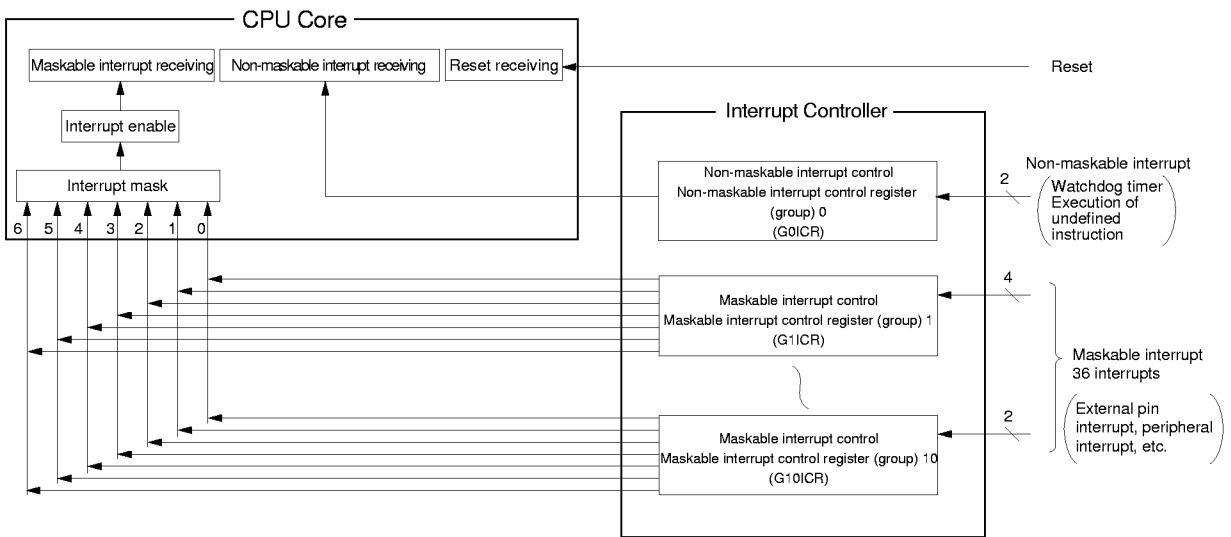


Figure 1-1-2 Configuration of Interrupt Controller

The state of processor status word determines whether an interrupt request is accepted. If accepted, the hardware will begin automatic processing and the program counter and other registers will be saved on the stack. Next, the starting address of the specific interrupt processing program corresponding to that interrupt is retrieved and branched to.

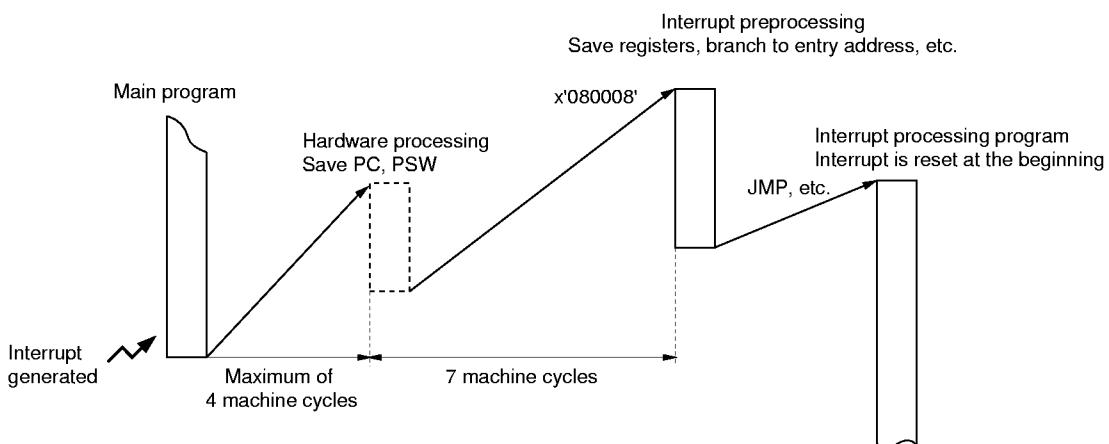


Figure 1-1-3 Interrupt Processing Sequence

1-2 Basic Specifications

The basic specifications of the MN1020012 are listed below. For further details, please refer to the product standards.

Table 1-2-1 Basic Specifications (1/3)

CPU structure	Load/store architecture Eight registers Data: four 24-bit registers Address: four 24-bit registers Other Program Counter: 24 bits Processor Status Word 16 bits Multiplication/division register: 16 bits
Instructions	Number of instructions: 36 Number of addressing modes: 6 Basic instruction length: 1 byte Operation-code assignment: 1~2 bytes (basic portion) + 0~3 bytes (extension)
Basic performance	Internal operating frequency: 10MHz (20MHz oscillator) Min. instruction execution clock: 1 clock cycle (100ns) Register-to-register execution clock: min. 1 clock cycle Load/store: min. 1 clock Conditional branch: 1~3 clock cycles
Pipeline	Three stages (instruction fetch, decode, execute)
Address space	16 Mbytes (linear addressing method)
External buses	Address: 24 bits four chip select (CS) lines (fixed addresses) Data: 8 or 16 bits Minimum bus cycle: 1 clock cycle (100ns with 20MHz oscillator) Bus timing can be configured for SRAM, ROM, DRAM, pseudo SRAM, and ASICs with 4-Mbyte increments DRAM high speed page mode support Fixed number of wait cycles inserted for SRAM, ROM, ASIC configurations Refresh control is available for DRAM and pseudo SRAM configurations CAS before RAS auto refresh

Table 1-2-1 Basic Specifications (2/3)

Energy-saving modes	STOP mode, HALT mode
Oscillator circuit	Max. 20MHz
Interrupts	<p>38 interrupts (Number of interrupt priority level settings: 7 levels)</p> <p>External interrupts: 4 interrupts (individual IRQ, edge specification) 1 interrupt (8 interrupts ORed together, sharing common IRQ)</p> <p>Internal interrupts: 33 (Timers: 18, Serial I/O: 4, DMA: 8, A/D: 1, Watchdog: 1, Undefined instruction interrupt: 1)</p>
Timer/Counter functions	<p>Ten 8-bit timers (count-down)</p> <p>Reload timers</p> <p>Cascadable (can be used as a timer 16~80 bits wide)</p> <p>Configurable for timer output (with 1:1 duty)</p> <p>Choice of internal or external clock source</p> <p>Serial interface clock generator</p> <p>Analog-to-digital converter start timing generator</p> <p>Three 16-bit timers (two configurable for counting up or down, one count-up timer)</p> <p>Two channel compare/capture register</p> <p>Choice of internal or external clock source</p> <p>Configurable for timer output (with 1:1 duty) (max. 6)</p> <p>PWM or one-shot pulse outputs (max. 3)</p> <p>Synchronous output port timing generator</p> <p>Two-phase encoder input (multiple of 1 or 4)</p> <p>17-bit watchdog timer</p>
Synchronous output	<p>Two 4-bit channels</p> <p>Stepping motor pattern generator</p> <p>4-phase single excitation, 4-phase double excitation, or 4-phase 1-2 excitation</p> <p>Forward or reverse operation</p> <p>Capable of generating arbitrary patterns using DMA function</p>
DMA functions	<p>8 channels</p> <p>Supports high-speed direct memory-to-memory or memory-to-I/O data transfers corresponding to each interrupt</p> <p>Max. transfer rate of 20 Mbytes/sec</p> <p>Transfer address space of 16 Mbytes</p> <p>1 byte/2 byte (1 word) transfer</p> <p>Choice of increment (INC), decrement (DEC), or fixed source and destination pointers</p> <p>Choice of single-word or burst mode transfers</p> <p>Max. continuous transfer cycles: 16,777,216</p> <p>2 channels per group for memory-to-memory transfers</p>

Table 1-2-1 Basic Specifications (3/3)

Serial interfaces	Two serial interfaces, supporting both UART and synchronous operation
Analog interface	Analog-to-digital converter 8-bits × 8 inputs Auto-scan function (1~8 channels can be set)
I/O ports	29 I/O ports (25 bidirectional, 4 input only, all shared)
Package	128-pin QFP with pin pitch of 0.5mm and 18mm square

1-3 Block Diagram

A block diagram of the CPU core for this series is shown in Figure 1-3-1.

The functions of each block are listed in Table 1-3-1.

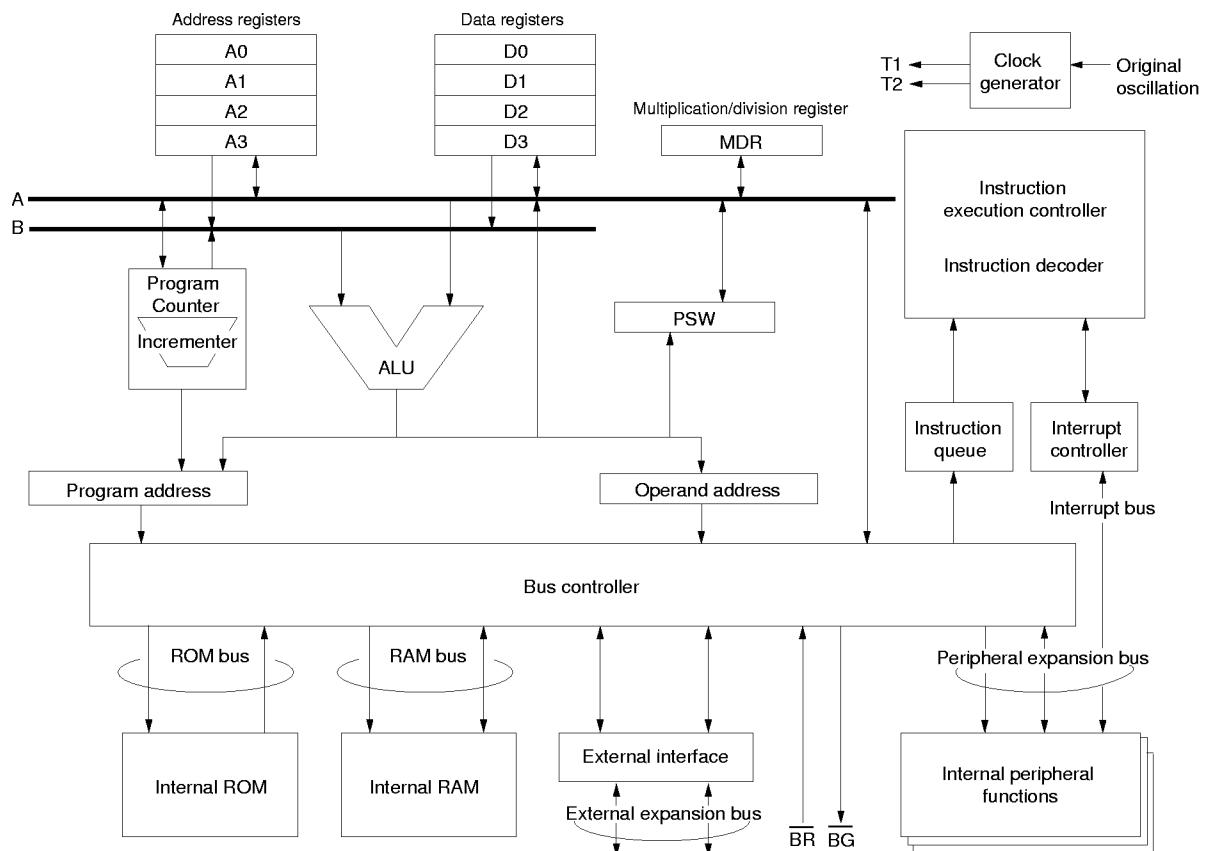


Figure 1-3-1 Block Diagram of Functions

Table 1-3-1 Summary of Block Functions

Block	Function
Clock Generator	Generates a clock signal from an external crystal and supplies the clock signal to each CPU section.
Program Counter	Generates the address of the instruction to be processed in the instruction queue. The program counter is usually incremented according to sequencer specifications, however branch addresses or ALU processing results are set when branch instruction executed or an interrupt is received.
Instruction Queue	Stores a maximum of 4 bytes of the prefetched instruction.
Instruction Decoder	The instruction decoder will decode the contents of the instruction queue. Control signals necessary to execute the instruction will be sequentially generated. Instructions are executed by controlling each block within the chip.
Instruction Execution Controller	Controls operation of each section of the CPU based on instruction decoding results, interrupt requests, etc.
ALU	Performs data arithmetic operations, logical operations, shift computations, and operand address computation during register-relative indirect, indexed addressing, or register indirect addressing modes.
Internal ROM, Internal RAM	Allocated as execute program, data, and stack areas.
Address Register (An)	Used to store addresses that specify memory locations for data transfers. Stores the base address for register-relative indirect, indexed addressing, and register indirect addressing modes.
Computation Register (Dn, MDR)	Dn is used for memory and data transfers, and to store computation results. Stores the offset address for indexed addressing and register indirect addressing modes. MDR is used to store multiplication and division data.
PSW	The various flags of the CPU interrupt control circuit status, computation results, etc. are stored in this register.
Interrupt Controller	Detects interrupt requests from peripheral functions and requests the CPU to transfer to interrupt processing.
Bus Controller	Controls the connection between the CPU internal bus and the CPU external bus. Contains an arbitration function for bus usage rights.
Internal Peripheral Functions	Contains peripheral functions (timer, serial, A/D converter, etc.)

1-4 Pin Functions

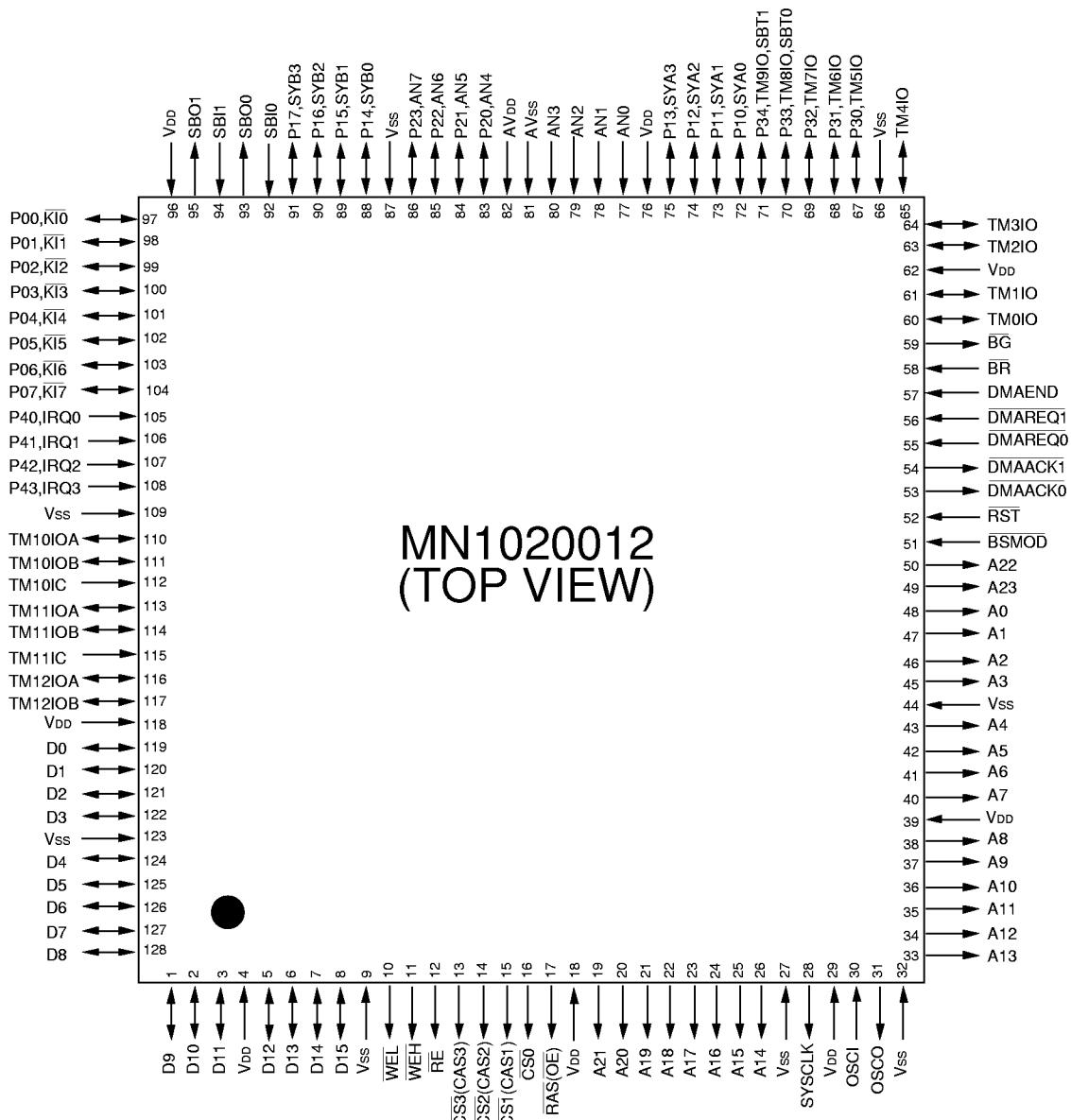


Figure 1-4-1 Pin Configuration

1-4-1 Summary of Pin Functions

This chapter describes pin functions.

Chapter 10 "Data Glossary" gives the pin's input level, whether it has a Schmitt trigger, and whether it has a pull-up. The TTL designation indicates that the pin judges input using TTL levels; the CMOS one, CMOS levels. Pins with Schmitt triggers have a Yes in the corresponding column; otherwise, the column is blank. Pins with pull-up resistors are all programmable. Programmable pins have their pull-up resistors controlled by the pull-up control register (PPLU). For further details, see Chapter 9 "Ports."

Table 1-4-1 List of Pin Functions (1/6)

Pin Name	I/O	Dual Purpose Pin	Name	Function
V _{DD}	—	—	Power Supply	There are eight of these pins. They must be connected to a power supply with a voltage of 4.5~5.5 V.
V _{ss}	—	—	Power Supply Grounding	There are eight of these pins. They must be connected to the 0-V side of the power supply.
AV _{DD}	—	—	Analog Power Supply Grounding	This is the power supply for the analog-to-digital converter. Connect this pin directly to one of the V _{DD} pins. The circuit board design must eliminate noise interference with the analog circuits--particularly, that due to noise from the digital power supply. If the pin is not used, make it the same level as V _{DD} . [Figure 1-4-2]
AV _{ss}	—	—	Analog Power Supply Grounding	This is the power supply for the analog-to-digital converter. Connect this pin directly to one of the V _{ss} pins. The circuit board design must eliminate noise interference with the analog circuits--particularly, that due to noise from the digital power supply. If the pin is not used, make it the same level as V _{ss} . [Figure 1-4-2]
OSCI	Input	—	Oscillator Input (4~20 MHz)	For a self-excited oscillator configuration, connect a crystal or ceramic oscillator across these two pins. The two pins have a built-in feedback resistor between them. For stability, insert capacitors of 20~33 pF between the pins and V _{ss} . [Figure 1-4-3] For the exact capacitance, consult the oscillator manufacturer.
OSCO	Output	—	Oscillator Output (4~20 MHz)	For an external oscillator configuration, connect OSCI to an oscillation with an amplitude swinging between V _{DD} and V _{ss} and a frequency of 4~20 MHz. Leave OSCO open.

Table 1-4-1 List of Pin Functions (2/6)

Pin Name	I/O	Dual Purpose Pin	Name	Function
<u>RST</u>	Input	—	Reset Input	This pin is for resetting the microcontroller. Pulling the pin LOW for at least 400ns (at 20 MHz) resets the chip. There may be cases where the chip is reset if noise is input even for less than 400nsec. Take precautions against noise in the reset circuit. When the input level returns to HIGH, the chip waits approximately 6~7 ms for the OSC1 signal to stabilize and then fetches and executes the instruction at address x'080000. [Figure 1-4-4]
SYSCLK	Output	—	System Clock Output	This pin provides the system clock. For a 20-MHz oscillator, the system clock is 10 MHz. After a reset, the chip waits for the OSC1 signal to stabilize. Note that it <u>keeps</u> the pin HIGH from the time that the RST pin goes LOW through to the end of this stabilization interval.
BSMOD	Input	—	Data Bus Width Input	This pin specifies the data bus width, 8 or 16 bits, for the first quarter of the 16-Mbyte address space, Block 0 (x'000000~x'3FFFFF). Pulling the pin LOW specifies a 16-bit data bus, enabling pins D15~D0; leaving it HIGH specifies an 8-bit data bus with only pins D15~D8 enabled. The data bus width cannot be changed during operation.
<u>BR</u> <u>BG</u>	Input Output	— —	Bus Request Input Bus Request Granted Output	These pins support bus arbitration. Pulling <u>BR</u> LOW causes the chip to suspend execution of the current instruction, release the bus, and pull <u>BG</u> LOW. After the MN1020012 accesses the bus, the bus is released and <u>BG</u> is pulled LOW. After a DMA transfer, the bus is released and <u>BG</u> is pulled LOW. BR is connected to a level detector. Returning it to HIGH restores the chip to bus master status. If bus arbitration is not used, fix <u>BR</u> at HIGH and leave <u>BG</u> open.

Table 1-4-1 List of Pin Functions (3/6)

Pin Name	I/O	Dual Purpose Pin	Name	Function
\overline{WE}	Output	—	Write Enable LOW Output	These provide control signals for memory read/write access.
\overline{WEH}	Output	—	Write Enable HIGH Output	For SRAM, ROM, and pseudo SRAM, connect \overline{RE} to the memory chips' \overline{OE} pins. The chip pulls the pin LOW when reading from memory.
\overline{RE}	Output	—	Read Enable Output	For SRAM, pseudo SRAM, and DRAM, connect WEH and \overline{WEL} to the memory chips' \overline{WE} pins. The chip pulls these pins LOW when writing to memory. \overline{WEH} controls pins D15~D8 for writing; \overline{WEL} , pins D7~D0. When the 8-bit data bus is in effect, \overline{WEL} is invalid and stays HIGH, so leave it open.
A23~A0	Output	—	Address Output	These normally provide the memory address. Connect them to the memory chips' address pins, address decoder circuits, etc. The pins states are indeterminate--that is, unspecified fixed values--when the chip is not accessing memory or is in the HALT or STOP modes. The output of fixed values is different for LSI and ICE systems. Therefore, during an external access, the address decode output and chip select (CS) are ANDed together off the chip. Addresses A23~A0 are in a high impedance state during bus requests (\overline{BG} is LOW).
D15~D0	I/O	—	Data I/O	These handle memory data I/O. Connect them to the memory chips' data pins, etc. When the chip is not accessing memory, the pins are configured for input.
\overline{RAS}	Output	\overline{OE}	RAS Output	If DRAM is connected, connect \overline{RAS} to the memory \overline{RAS} pin. If pseudo SRAM is connected, connect \overline{RAS} to the memory \overline{OE} pin. \overline{RAS} performs the read, write and refresh functions of DRAM or pseudo SRAM. Leave the pin open if not used.

Table 1-4-1 List of Pin Functions (4/6)

Pin Name	I/O	Dual Purpose Pin	Name	Function
$\overline{CS3} \sim \overline{CS0}$	Output Output	$\overline{CAS3} \sim \overline{CAS1}$	CS3~CS0 Output CAS3~CAS1 Output	These connect to the chip select (\overline{CS}) pins of SRAM, ROM, and pseudo SRAM chips. For DRAM, they also connect to the CAS pins for use in controlling read, write, and refresh cycles. Refer to "Chapter 2 Bus Interface" for the location of the $\overline{CS3} \sim \overline{CS0}$ address space.
AN3~AN0	Input	—	Analog-to-Digital Converter Inputs	These serve as inputs to the Analog-to-Digital Converter. [☞ Chapter 6, Analog Interface]
P13~P10	I/O Output	SYA3~ SYA0	General I/O Port 1, Synchronous A Outputs	When used as a general I/O port, these permit direction configuration at the bit level. [☞ Chapter 9, Port Functions] To use them as synchronous outputs, however, set the SYAEN flag in the synchronous output mode A register SYAMD to '1' and set the bits in the Port 1 direction register P1DIR for output ('1'). If these are not used, configure these pins for output and leave the pins open.
P17~P14	I/O Output	SYB3~ SYB0	General I/O Port 1, Synchronous B Outputs	When used as a general I/O port, these permit direction configuration at the bit level. [☞ Chapter 9, Port Functions] To use them as synchronous outputs, however, set the SYBEN flag in the synchronous output mode B register SYBMD to '1' and set the bits in the Port 1 direction register P1DIR for output ('1'). If these are not used, configure these pins for output and leave the pins open.
P23~P20	I/O Input	AN7~AN4	General I/O Port 2, Analog-to-Digital Converter Inputs	When used as a general I/O port, these permit direction configuration at the bit level. [☞ Chapter 9, Port Functions] To use them as analog-to-digital converter inputs, there is no need to switch them from general port operation. Just set the bits in the Port 2 direction register P2DIR for input ('0'). If these are not used, configure these pins for output and leave the pins open.

Table 1-4-1 List of Pin Functions (5/6)

Pin Name	I/O	Dual Purpose Pin	Name	Function
SBI1~SBI0 SBO1~SBO0	Input Output	— —	Serial Interface Inputs Serial Interface Outputs	These are serial interface I/O pins. If these are not used, fix the input pins at HIGH and leave the output pins open. [☞ Chapter 5, Serial Interfaces]
P43~P40	Input Input	IRQ3~IRQ0	General I/O Port 4, External Interrupt Inputs	These serve as a general input port. [☞ Chapter 9, Port Functions] If these are not used, fix them at HIGH.
P07~P00	I/O Input	KI7~KI0	General I/O Port 0, Keyboard Interrupt Inputs	When used as a general I/O port, these permit direction configuration at the bit level. [☞ Chapter 9, Port Functions] To use them as keyboard interrupt inputs, there is no need to switch them from general port operation. Just set the bits in the Port 0 direction register P0DIR for input ('0'). They support connection of up to eight keyboard matrix lines. Pulling any line LOW generates an interrupt. (HIGH triggers may also be used.) If these are not used, configure these pins for output and leave the pins open. Each bit can be selected as a general port or keyboard interrupt input.
P34~P30	I/O I/O I/O	TMIO9~ TMIO5, SBT1~ SBT0	General I/O Port 3, Timer 9~5 I/O Serial Interface Clock I/O	When used as a general I/O port, these permit direction configuration at the bit level. [☞ Chapter 9, Port Functions] To use them as timer outputs, set the Port 3 mode bits (P3MODE) to timer operation. To use them as timer inputs, set the Port 3 mode bits (P3MODE) to general port operation (0) and set the bits in the Port 3 direction register P3DIR for input ('0'). To use them as synchronous serial interface clock outputs, set the Port 3 mode bits (P3MODE) to serial operation. To use them as synchronous serial interface clock inputs, set the Port 3 mode bits (P3MODE) to general port operation (0) and set the bits in the Port 3 direction register P3DIR for input ('0'). If these are not used, configure these pins for output and leave the pins open.

Table 1-4-1 List of Pin Functions (6/6)

Pin Name	I/O	Dual Purpose Pin	Name	Function
TMIO4~TMIO0	I/O	—	Timer 4~0 I/O	These are I/O pins for 8-bit timers 0 through 4. [☞ Chapter 4, Timer/Counter Functions]
TMIO12A~ TMIO10A TMIO12B~ TMIO10B	I/O I/O	— —	Timer 12A, 11A, and 10A I/O Timer 12B, 11B, and 10B I/O	These serve as timer input capture or timer output compare pins.
TMI11C~ TMI10C	Input	—	Timer Count Clear Inputs	These clear the corresponding timer count to zero. [☞ Chapter 4, Timer/Counter Functions]
DMAACK1~ DMAACK0	Output	—	DMA Acknowledge Outputs	These provide acknowledge signals in response to external DMA requests.
DMAREQ1~ DMAREQ0	Input	—	DMA Request Inputs	These accept external DMA requests. If these are not used, fix them at HIGH.
DMAEND	Input	—	DMA I/O	This signal forces cancellation of all executing or pending DMA transfers. [☞ Chapter 8, DMA Functions] If these not used,fix them at LOW.

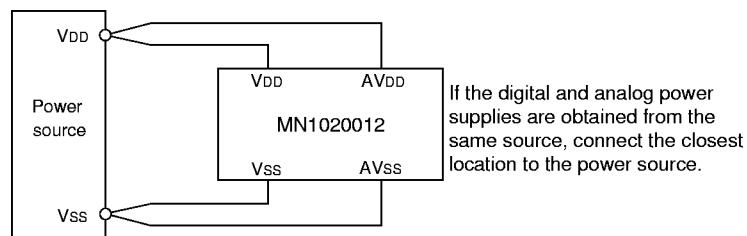
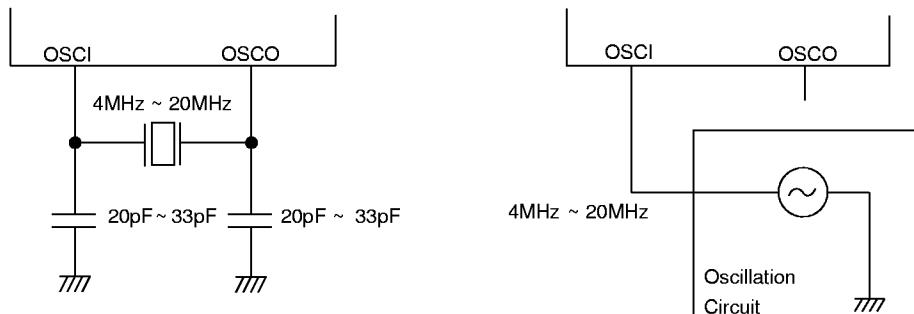


Figure 1-4-2 Power Source Wiring Precaution



Note: Capacitor values differ depending upon the crystal oscillator.

Figure 1-4-3 OSCI and OSCO Connections (Example)

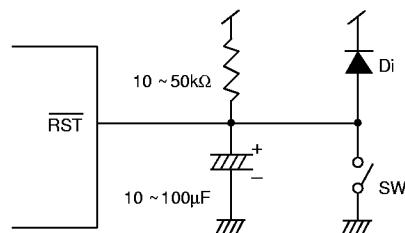
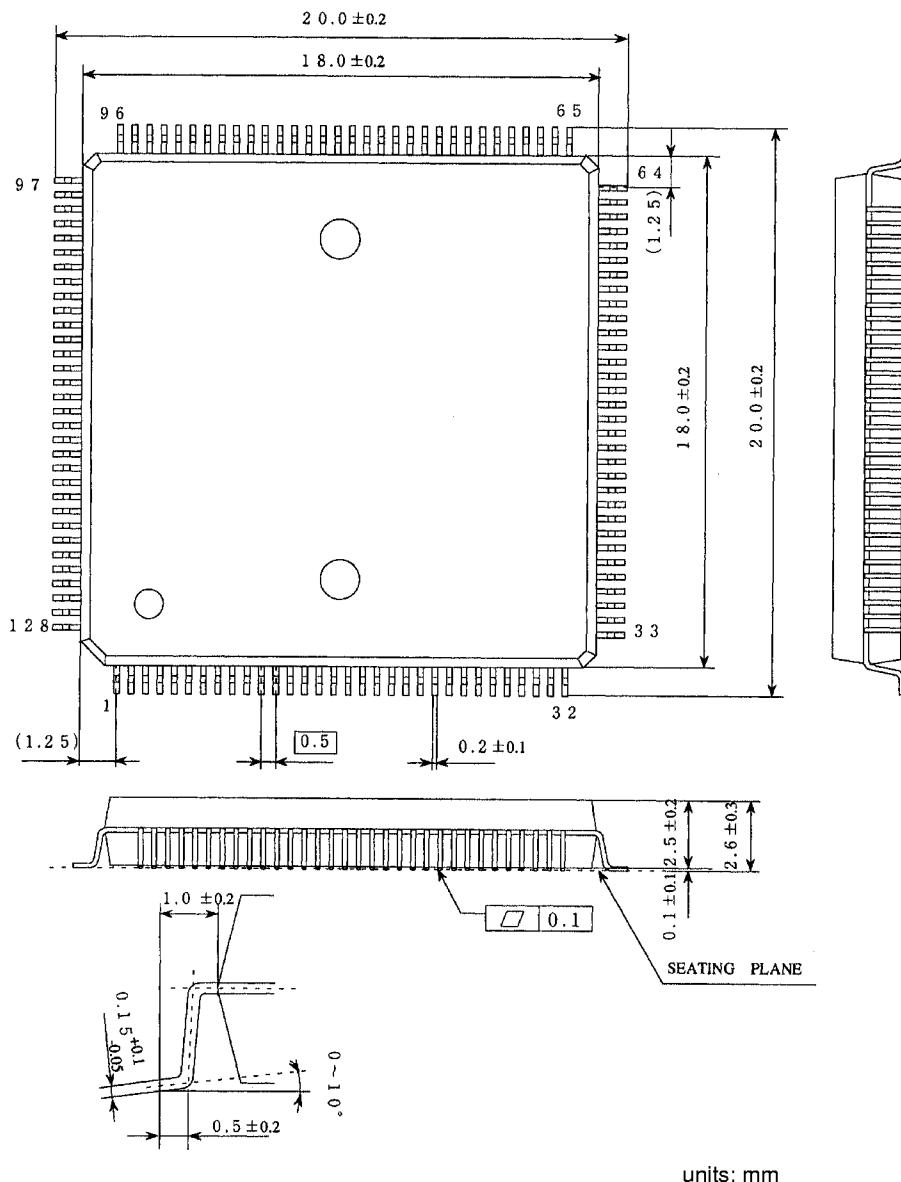


Figure 1-4-4 Example Reset Pin Connection

Package code: QFP128-P-1818



Sealing material: Epoxy resin, Lead material: Iron-nickel alloy 42,

Lead surface treatment: Solder plating

Figure 1-4-5 External Dimensions (MN1020012A): 128-pin QFP (18 mm square)

Package code: LQFP128-P-1818B



*Package external dimensions
are subject to change. Before
using the product, please
contact your nearest distributor
for the latest product
specifications.*

units: mm

Sealing material: Epoxy resin, Lead material: Copper,
Lead surface treatment: Solder plating

Figure 1-4-6 External Dimensions (MN1020012AFA): 128-pin LQFP (18 mm square)

Chapter 2 Bus Interface

2

2-1 Bus Interface Summary

2-1-1 Overview

The MN1020012 is operated connected to external ROM and RAM. An I/O gate array can also be connected. By using the MN1020012's internal chip select function, the address space is partitioned into 4 fixed areas (blocks 0~3), each area containing approximately 4 Mbytes. (Arbitrary partitioning is possible if an external chip select is used.)

A 16-bit or 8-bit bus width can be selected for each block. The BSMOD pin sets the bus width (either 16 bits or 8 bits) for block 0, that contains the reset handler. (Refer to section 1-4 "Pin Functions" for pin settings.) The MEMMDn register setting determines blocks 1~3.

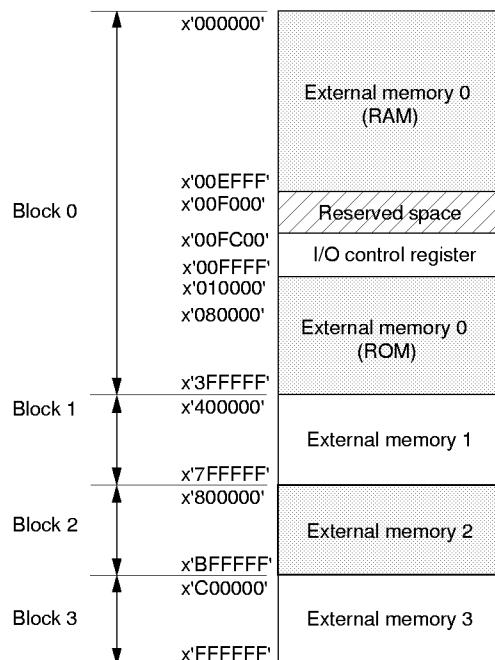


Figure 2-1-1 Address Space



The CS (chip select) pins for block 0, block 1, block 2, and block 3 are $\overline{\text{CS}0}$, $\overline{\text{CS}1}$, $\overline{\text{CS}2}$, and $\overline{\text{CS}3}$ respectively. They are pulled LOW when accessed.

If DRAM or pseudo SRAM is used, they must be located in blocks 1~3 (the exception is an 8 Mbyte DRAM area, which if selected uses blocks 2 and 3). Devices to be used are set in the MEMMDn register for that block. DRAM and pseudo SRAM cannot be mixed.

ROM is located in block 0. The MN1020012 executes instructions starting from address x'80000' after reset, or from x'80008' when there is an interrupt. The first instruction at the lowest address, either x'80000' or x'80008', must be in ROM.

Table 2-1-1 Memory Access Time Requirements (for 20 MHz oscillation)

Memory \ No. of Wait Cycles	No Wait	1 Wait
ROM	~45ns	~120ns
SRAM	~45ns	~120ns
DRAM	Not possible	~80ns
Pseudo SRAM	Not possible	~80ns

2-1-2 Control Registers

Control of the bus interface is performed by the memory control register (MEMCTR), the memory mode control registers n (MEMMDn), the DRAM control register (DRMCTR), and the refresh counter register (REFCNT).

Table 2-1-2 Summary of Bus Interface Control Registers

Register Abbreviation	Address	R/W	Register Name
MEMCTR	x'00FC02'	R/W	Memory control register
MEMMD0	x'00FC30'	R/W	Memory mode control register 0
MEMMD1	x'00FC32'	R/W	Memory mode control register 1
MEMMD2	x'00FC34'	R/W	Memory mode control register 2
MEMMD3	x'00FC36'	R/W	Memory mode control register 3
DRMCTR	x'00FD00'	R/W	DRAM control register
REFCNT	x'00FD02'	R/W	Refresh counter

The MEMCTR and MEMMDn register must be set in the initialization program to conform to the system configuration. [☞ 10-4 Initialization Program]



The MEMCTR of the MN1020012 is set to x'04n0' (n=0~3, the number of wait cycles for special registers is normally 1) by the initialization program.

MEMMD0 specifies the number of wait states corresponding to the device connected to block 0.

Since block 0 does not support DRAM (or pseudo SRAM) and uses a pin to specify the bus width, it differs from MEMMDn registers for other blocks in not having bits for enabling DRAM or specifying the bus mode.

When there is a reset, execution will start in the 7 wait state mode.

MEMMD0: x'00FC30'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	—	—	—	—	—	WAIT 2	WAIT 1	WAIT 0

Sets block 0 memory mode
Number of wait states to be inserted in block 0

- 000: no wait cycles
- 001: 1 wait cycle
- 010: 2 wait cycles
- 011: 3 wait cycles
- 100: 4 wait cycles
- 101: 5 wait cycles
- 110: 6 wait cycles
- 111: 7 wait cycles

MEMMD1 specifies the number of wait states and the bus width corresponding to the device connected to block 1. If block 1 is not used, bit 15 must be set to '0'.

When connecting DRAM or pseudo SRAM, the type of DRAM must be set in the DRMCTR register. If DRAM or SRAM is connected, set bit 15 of the MEMMD1 register to '1'. In this case, since the number of wait cycles is fixed at 1 wait cycle, it is not necessary to set WAIT2~0. (They are ignored.)

MEMMD1: x'00FC32'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRAM	—	—	—	—	—	—	BSMOD	—	—	—	—	—	WAIT2	WAIT1	WAIT0

DRAM/PSRAM Selection
0: disable
1: enable

Number of Wait Cycles to Insert in Block 1
000: no wait cycles
001: 1 wait cycle
010: 2 wait cycles
011: 3 wait cycles
100: 4 wait cycles
101: 5 wait cycles
110: 6 wait cycles
111: 7 wait cycles

Block 1 Bus Mode
0: 16-bit bus mode
1: 8-bit bus mode

MEMMD2 specifies the number of wait states and the bus width corresponding to the device connected to block 2. If block 2 is not used, bit 15 must be set to '0'.

When connecting DRAM or pseudo SRAM, the type of DRAM must be set in the DRMCTR register. If DRAM or SRAM is connected, set bit 15 of the MEMMD2 register to '1'. In this case, since the number of wait cycles is fixed at 1 wait cycle, it is not necessary to set WAIT2~0. (They are ignored.)

MEMMD2: x'00FC34'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRAM	—	—	—	—	—	—	BSMOD	—	—	—	—	—	WAIT2	WAIT1	WAIT0

DRAM/PSRAM Selection
0: disable
1: enable

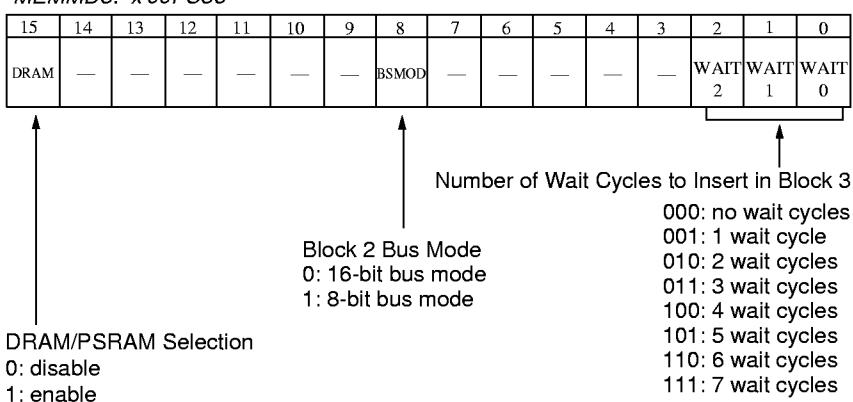
Number of Wait Cycles to Insert in Block 2
000: no wait cycles
001: 1 wait cycle
010: 2 wait cycles
011: 3 wait cycles
100: 4 wait cycles
101: 5 wait cycles
110: 6 wait cycles
111: 7 wait cycles

Block 2 Bus Mode
0: 16-bit bus mode
1: 8-bit bus mode

MEMMD3 specifies the number of wait states and the bus width corresponding to the device connected to block 3. If block 3 is not used, bit 15 must be set to '0'.

When connecting DRAM or pseudo SRAM, the type of DRAM must be set in the DRMCTR register. If DRAM or SRAM is connected, set bit 15 of the MEMMD3 register to '1'. In this case, since the number of wait cycles is fixed at 1 wait cycle, it is not necessary to set WAIT2~0. (They are ignored.)

MEMMD3: x'00FC36'

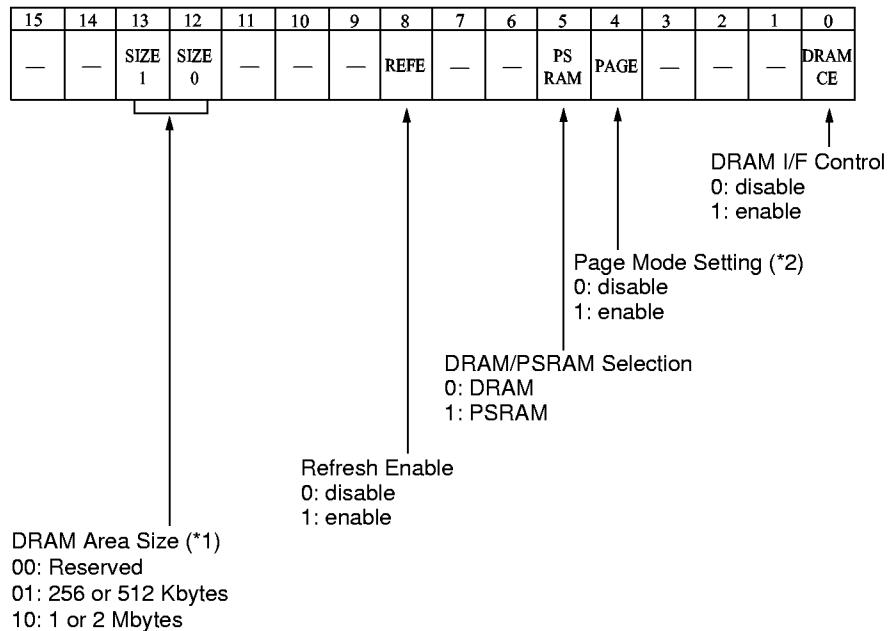


DRMCTR is the DRAM control register. It specifies the DRAM or pseudo SRAM memory mode.

If DRAM or pseudo SRAM is selected by any of one of the registers MEMMD3~MEMMD1, the normal setting for the DRMCE bit is '1'. Bit 5, the PSRAM bit, is used to select DRAM or pseudo SRAM. Set bit 8, the REFE bit, to '1' if refresh cycles are to be inserted in synchronization with the internal refresh counter.

DRAM address multiplexing is performed according to the values of the SIZE1~0 bits. The software does not have to manage page hits and misses for the page mode since addresses for comparison are determined from the value of the SIZE0~1 bits.

DRMCTR: x'00FD00'



2 Page mode cannot be used for DRAMS with different row and column address widths.

1 The size value is the size of the DRAM in which row and column address widths agree. If a DRAM is used in which the address widths do not agree, select the number of address bits that are right-shifted to form the row address.

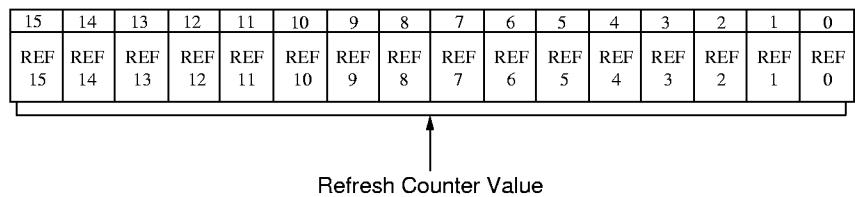
Table 2-1-3 DRAM Size and Address Multiplexer

DRAM	SIZE1, SIZE0					
	11		10		01	
	An	Row	Column	Row	Column	Row
A0	A11	A0	A10	A0	A9	A0
A1	A12	A1	A11	A1	A10	A1
A2	A13	A2	A12	A2	A11	A2
A3	A14	A3	A13	A3	A12	A3
A4	A15	A4	A14	A4	A13	A4
A5	A16	A5	A15	A5	A14	A5
A6	A17	A6	A16	A6	A15	A6
A7	A18	A7	A17	A7	A16	A7
A8	A19	A8	A18	A8	A17	A8
A9	A20	A9	A19	A9	(A18)	(A9)
A10	A21	A10	(A20)	(A10)	(A20)	(A10)

The refresh counter sets the refresh interval for the DRAM or pseudo SRAM.

The refresh counter is a countdown register synchronized with the SYSCLK. The refresh interval is thus this value times the SYSCLK interval.

REFCNT: x'00FD02'



2-1-3 Refresh Timing

The refresh timing is CAS before RAS. CAS before RAS refresh uses the internal counter of the DRAM or pseudo SRAM. One row address is refreshed in each refresh cycle. For example, if a device rating is listed as 256 addresses within 8 ms, one auto-refresh every $8\text{ms}/256=31.25\mu\text{s}$ is necessary.

This $31.25\mu\text{s}$ is set by REFCNT. Since REFCNT is a down-counter synchronized with the SYSLCK (10 MHz for a 20 MHz oscillation), for example, setting 256 for a 20 MHz oscillation will cause a refresh signal to be generated every $25.6\mu\text{s}$.

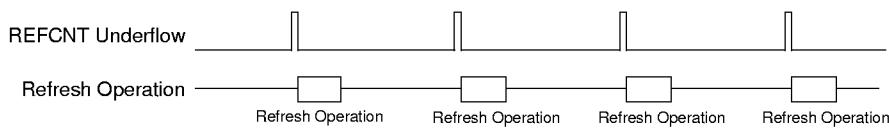


Figure 2-1-2 Refresh Timing Generation

Even during the refresh operation, the CPU will not halt DRAM access or access of blocks other than the DRAM with the exception of write access.

If the bus request function from the external bus master is utilized, the use of DRAM refresh control in the MN1020012 is prohibited.

Using the bus request function from the external bus master, and with the MN1020012 refresh control set to be invalid when DRAM is used (bit 8 of the DRAMCTR is set to '0'), the DRAM refresh operation is performed entirely by the external bus master which generates NBR to acquire the bus.



If DRAM page mode has been set, the bus request function cannot be used. Do not set DRAM page mode if using a microcomputer that is connected to a system that uses DRAM and requires the bus request function.

2-2 External Memory Connection Example

2-2-1 External Memory Connection Example

An example of the connection between this LSI chip and external memory is shown below.

■ ROM connection example for 16-bit bus width

The following example shows two 256-Kbyte ROMs assigned to Block 0.

Since the MN1020012 jumps to address x'080000' after a reset, the valid addresses consist of the range x'080000'~x'0FFFFF'. False images are also available at x'000000'~x'00EFFF', x'010000'~x'08FFFF', x'100000'~x'17FFFF', x'180000'~x'1FFFFFF', x'200000'~x'27FFFF', x'280000'~x'2FFFFFF', x'300000'~x'37FFFF', and x'380000'~x'3FFFFFF'.

A 16-bit word access of these two 256-Kbyte ROMs involves shifting the address bus connections by one bit. Line A1 of the MN1020012 is connected to line A0 of the ROM.

MEMMD0: x'00FC30'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	—	—	—	—	—	WAIT2	WAIT1	WAIT0
—	—	—	—	—	—	—	—	—	—	—	—	—	0	0	0

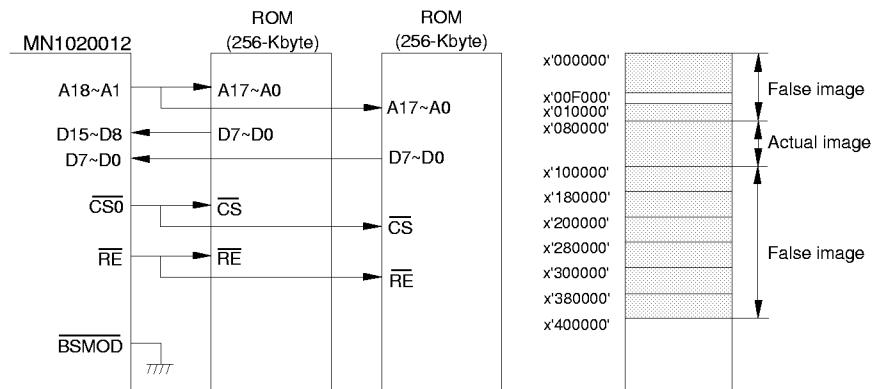


Figure 2-2-1 ROM Connection Example for 16-bit Bus Width

■ ROM Connection Example for 8-bit Bus Width

The following example shows a 512-Kbyte ROM assigned to Block 0 with an 8-bit bus width.

The memory map is exactly the same as for the 16-bit bus width, but the wiring connections are slightly different. The data bus is limited to D15~D8.

MEMMD0: x'00FC30'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	—	—	—	—	—	WAIT2	WAIT1	WAIT0
—	—	—	—	—	—	—	—	—	—	—	—	—	0	0	1

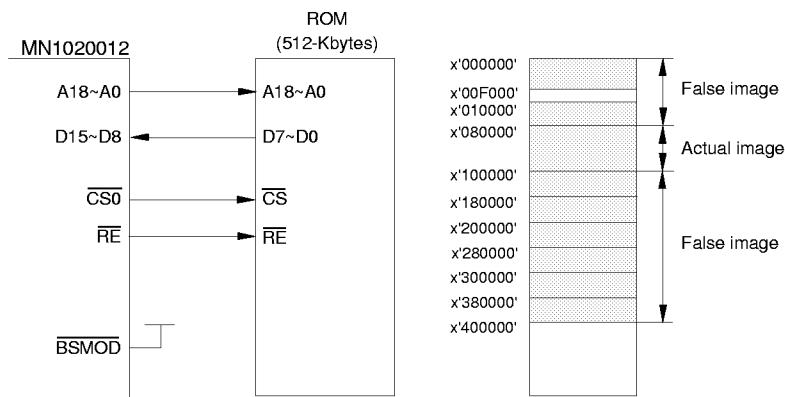


Figure 2-2-2 ROM Connection Example for 8-bit Bus Width

■ SRAM Connection Example for 16-bit Bus Width

The following example shows two 32-Kbyte SRAMs assigned to Block 1.

The actual ROM area is x'400000'~x'40FFFF' (containing the actual image). However, since there is no address decoder, false images are also available at regions x'410000'~x'41FFFF' through x'7F0000'~x'7FFFFFF'.

Since access is by word, the address bus connections are shifted by one bit. Line A1 of the MN1020012 is connected to line A0 of the SRAM.

MEMMD1: x'00FC32'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRAM	—	—	—	—	—	—	BMOD	—	—	—	—	—	WAIT2	WAIT1	WAIT0
0	—	—	—	—	—	—	0	—	—	—	—	—	0	0	1

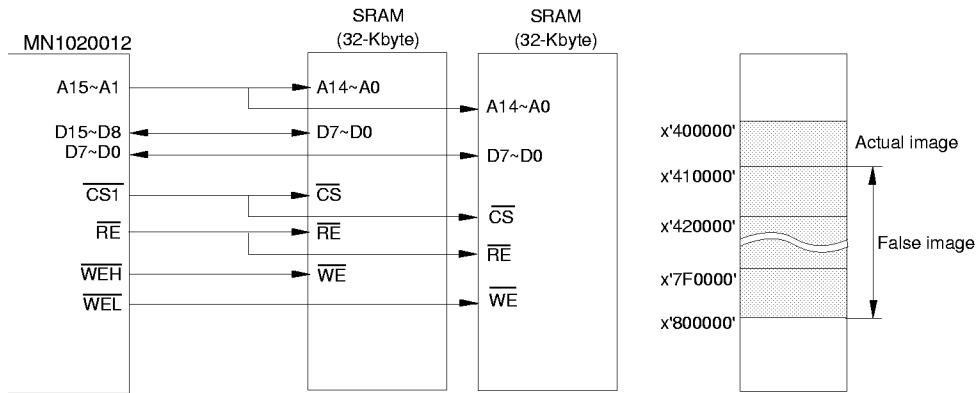


Figure 2-2-3 RAM Connection Example for 16-bit Bus Width

■ SRAM Connection Example for 8-bit Bus Width

The following example shows a 64-Kbyte SRAM with 8-bit access in Block 1.

The actual ROM area is x'400000'~x'40FFFF' (containing the actual image).

However, since there is no address decoder, false images are also available at regions x'410000'~x'41FFFF' through x'7F0000'~x'7FFFFFF'.

Since access is by an 8-bit bus, only D15~8 of the MN1020012 is connected.

MEMMD1: x'00FC32'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRAM	—	—	—	—	—	—	BMOD	—	—	—	—	—	WAIT2	WAIT1	WAIT0
0	—	—	—	—	—	—	1	—	—	—	—	—	0	0	0

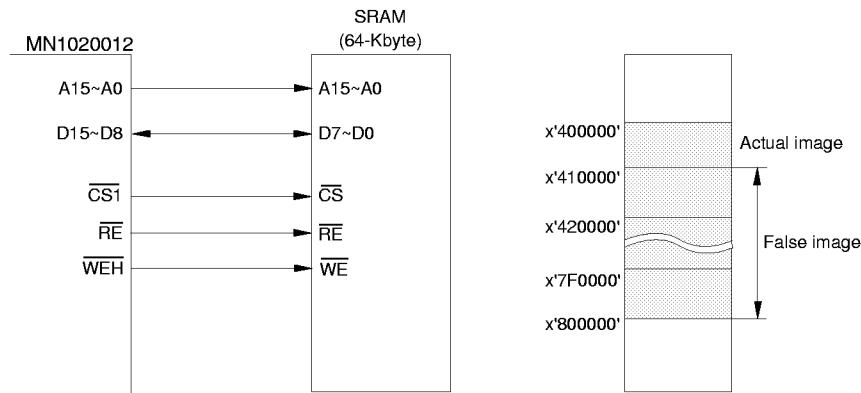


Figure 2-2-4 RAM Connection Example for 8-bit Bus Width

■ DRAM Connection Example for 16-bit Bus Width

This example shows two 256-Kbyte DRAMs with 16-bit access assigned to the region x'800000'~x'87FFFF' in Block 2. There are false images in the region x'880000'~x'BFFFFFF'. There is no need for an external address multiplexer as the MN1020012 provides one onboard.

MEMMD2: x'00FC34'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRAM	—	—	—	—	—	—	BMOD	—	—	—	—	—	WAIT2	WAIT1	WAIT0
1	—	—	—	—	—	—	0	—	—	—	—	—	—	—	—

DRAMCTR: x'00FD00'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	SIZE1	SIZE0	—	—	—	REFE	—	—	PS RAM	PAGE	—	—	—	DRAM CE
—	—	0	1	—	—	—	1	—	—	0	*	—	—	—	1

* Set to '1' if page mode is used, '0' otherwise.

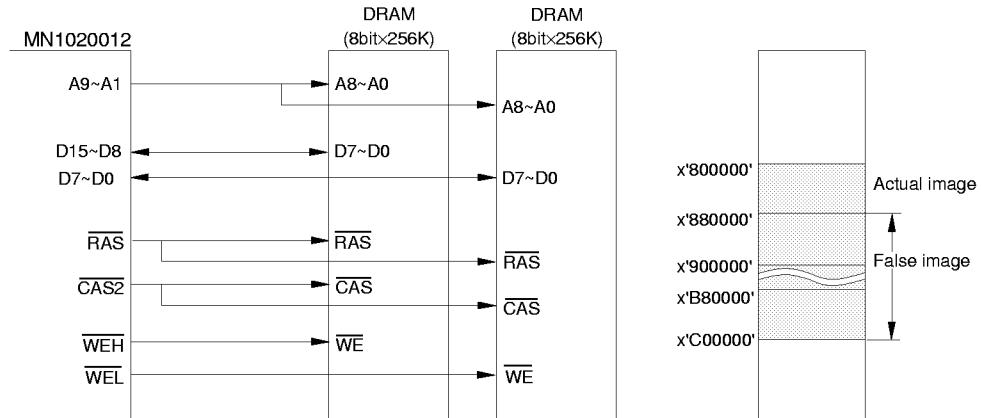


Figure 2-2-5 DRAM Connection Example for 16-bit Bus Width

■ DRAM Connection Example for 8-bit Bus Width

This example shows 256-Kbyte DRAMs with 8-bit access assigned to the region x'800000'~x'87FFFF' in Block 2. There are false images in the region x'840000'~x'BFFFFFF'. There is no need for an external address multiplexer as the MN1020012 provides one onboard.

MEMMD2: x'00FC34'

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRAM	—	—	—	—	—	—	—	BMOD	—	—	—	—	—	WAIT2	WAIT1	WAIT0
1	—	—	—	—	—	—	—	1	—	—	—	—	—	—	—	—

DRAMCTR: x'00FD00'

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	SIZE1	SIZE0	—	—	—	REFE	—	—	—	PS RAM	PAGE	—	—	—	DRAM CE
—	—	0	1	—	—	—	1	—	—	0	*	—	—	—	—	1

* Set to '1' if page mode is used, '0' otherwise.

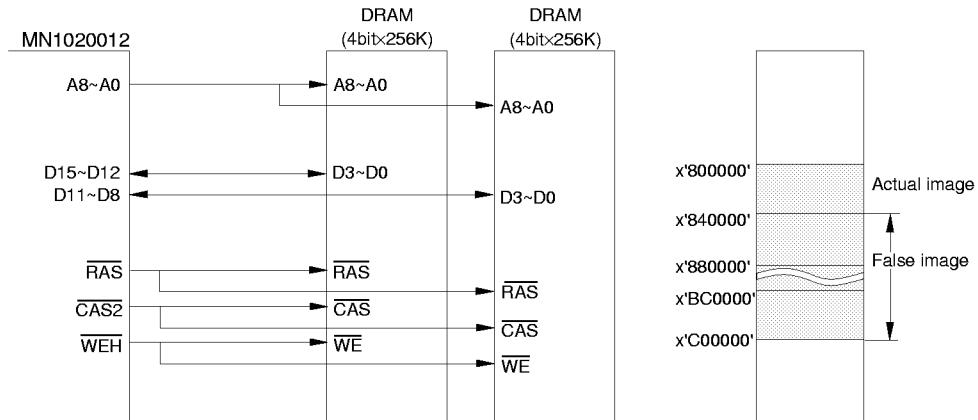


Figure 2-2-6 DRAM Connection Example for 8-bit Bus Width

■ DRAM Connection Example for Row and Column Addresses of Different Widths

This example shows a 512-Kbyte DRAM (10-bit row address and 8-bit column address) with 16-bit access assigned to the region x'800000'~x'87FFFF' in Block 2. There are false images in the region x'880000'~x'BFFFFFF'. There is no need for an external address multiplexer as the MN1020012 provides one onboard.

MEMMD2: x'00FC34'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRAM	—	—	—	—	—	—	BMOD	—	—	—	—	—	WAIT2	WAIT1	WAIT0
1	—	—	—	—	—	—	0	—	—	—	—	—	—	—	—

DRAMCTR: x'00FD00'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	SIZE1	SIZE0	—	—	—	REFE	—	—	PS RAM	PAGE	—	—	—	DRAM CE
—	—	0	1	—	—	—	1	—	—	0	0	—	—	—	1

(*1)

(*2)

* Selects the number of address bits that are right-shifted to form the ROW address.

2 Must be set to '0' since the page mode cannot be used.



The connection of a 16-bit bus to DRAM can differ depending upon the DRAM. Verify the row and address column address widths.

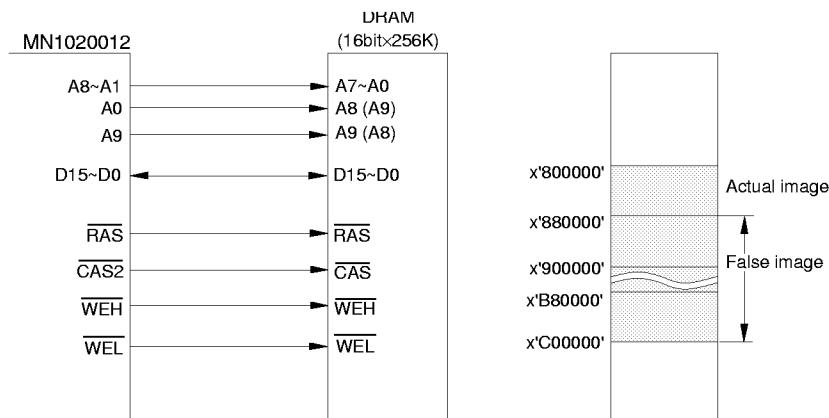


Figure 2-2-7 DRAM Connection Example for Row and Column Addresses of Different Widths

■ Pseudo SRAM Connection Example for 16-bit Bus Width

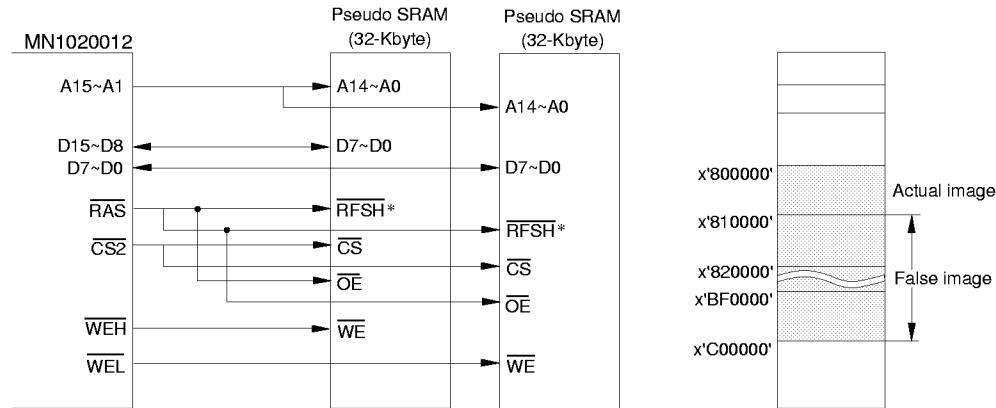
This example shows a 32-Kbyte pseudo SRAM with 16-bit access assigned to the region x'800000'~x'80FFFF' in Block 2. There are false images in the region x'810000'~x'BFFFFFF'.

MEMMD2: x'00FC34'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRAM	—	—	—	—	—	—	BMOD	—	—	—	—	—	WAIT2	WAIT1	WAIT0
1	—	—	—	—	—	—	0	—	—	—	—	—	—	—	—

DRAMCTR: x'00FD00'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	SIZE1	SIZE0	—	—	—	REFE	—	—	PS RAM	PAGE	—	—	—	DRAM CE
—	—	0	0	—	—	—	1	—	—	1	0	—	—	—	1



* indicates connection to a device that has RFSH.

* indicates connection to a device that has RFSH.

Figure 2-2-8 Pseudo SRAM Connection Example for 16-bit Bus Width

■ Access Timing for ROM and RAM with 16-bit Bus

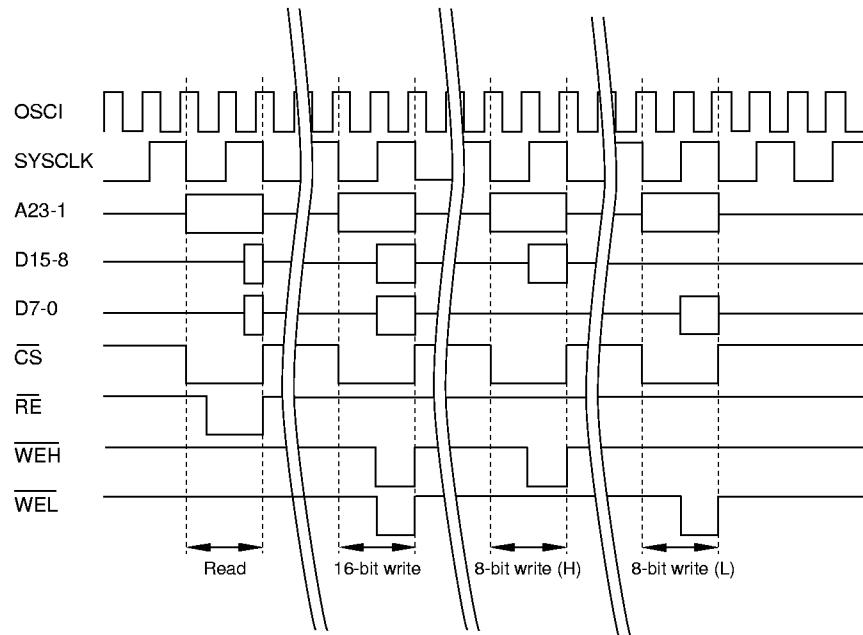


Figure 2-2-9 Access Timing of a 16-bit Bus with No Wait States

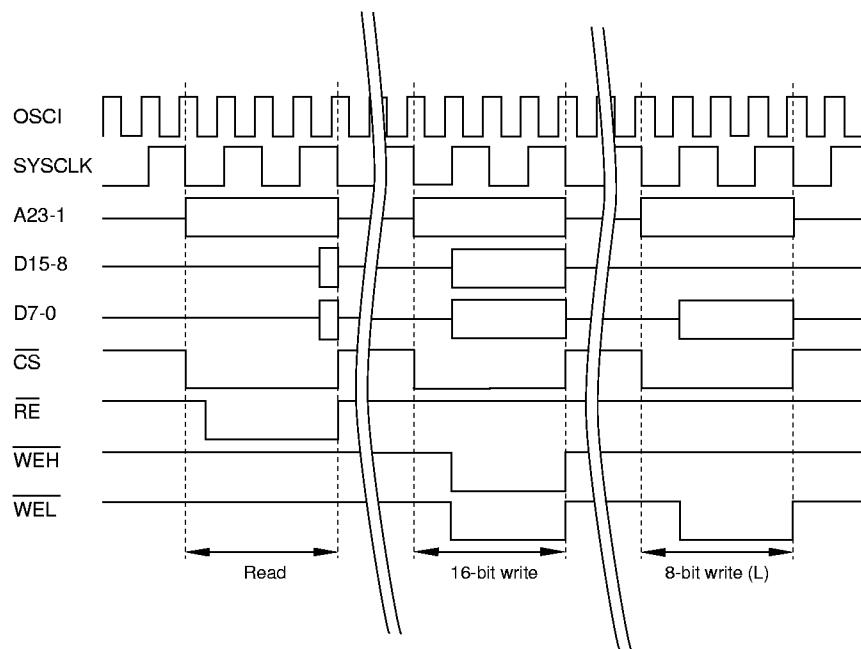


Figure 2-2-10 Access Timing of a 16-bit Bus with One Wait State

■ Access Timing for ROM and RAM with 8-bit Bus

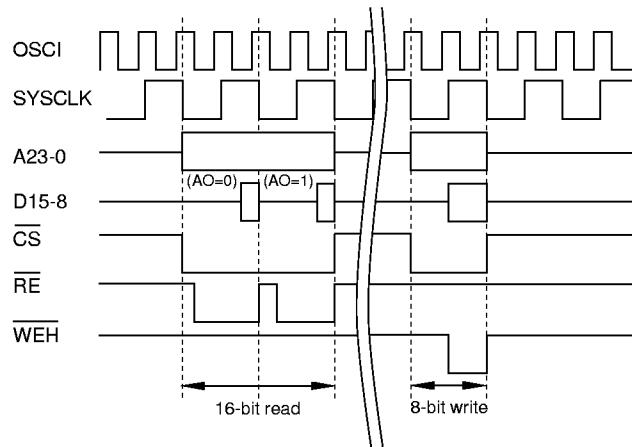


Figure 2-2-11 Access Timing of an 8-bit Bus with No Wait States

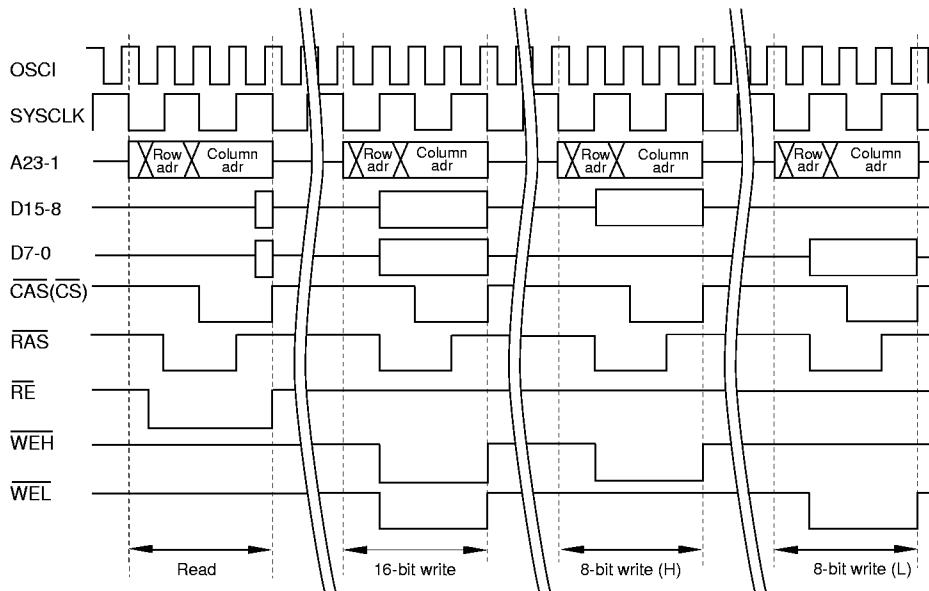


Figure 2-2-12 Access Timing for DRAM with a 16-bit Bus

(without page mode)

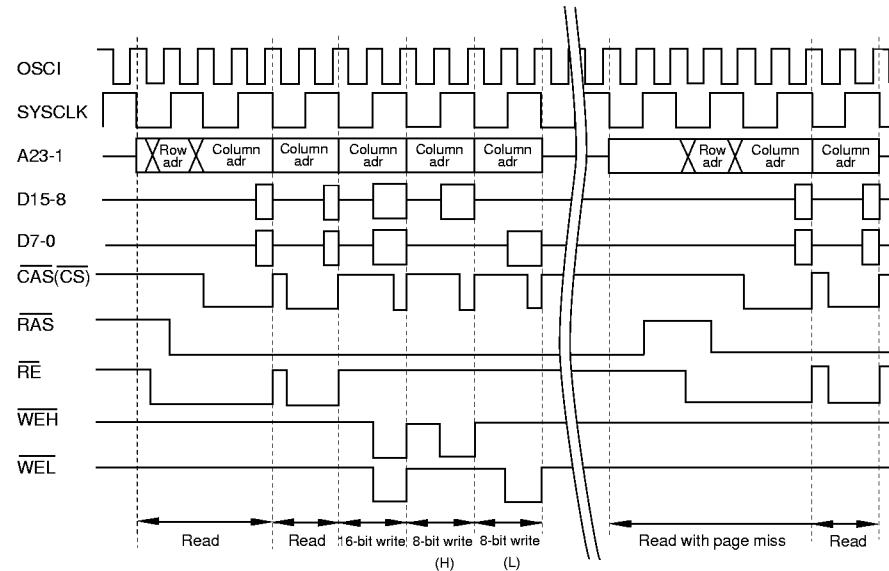


Figure 2-2-13 Access Timing for DRAM with a 16-bit Bus (with page mode)

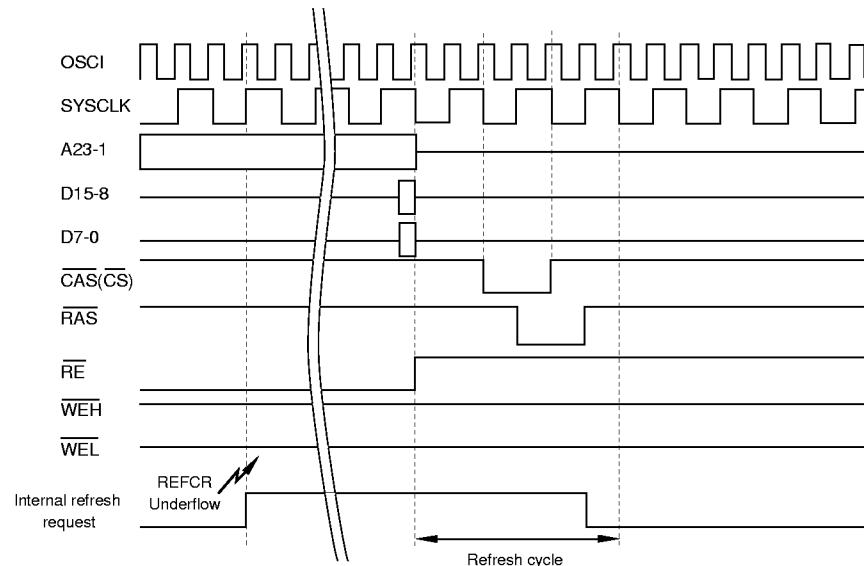


Figure 2-2-14 Access Timing for DRAM Refresh

■ Access Timing for Pseudo SRAM with 16-bit Bus

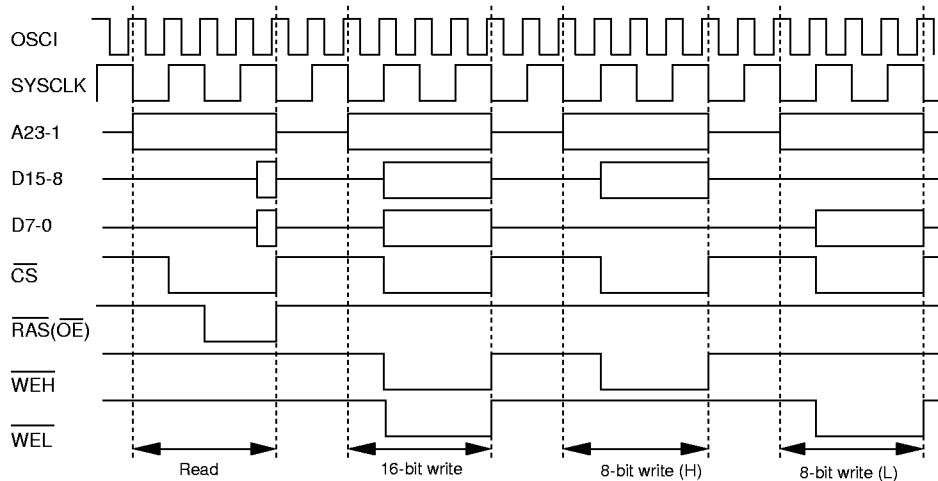


Figure 2-2-15 Access Timing for Pseudo SRAM with 16-bit Bus

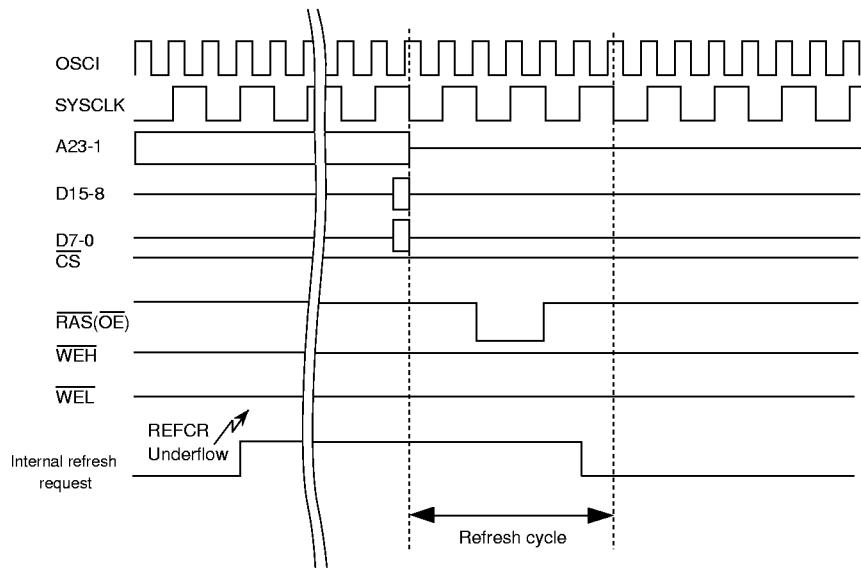


Figure 2-2-16 Access Timing for Pseudo SRAM Refresh (using \overline{OE} pin)

Chapter 2 Bus Interface

Chapter 3 Interrupt Control

3

3-1 Interrupt Groups

3-1-1 Overview

The interrupt controller on this LSI chip is configured into 11 groups. Several interrupts are allocated to each group. When an interrupt occurs, the CPU receives an interrupt request.

[MN10200 Series LSI Manual Linear Address Edition]

Table 3-1-1 Summary of Interrupt Control Registers (1/2)

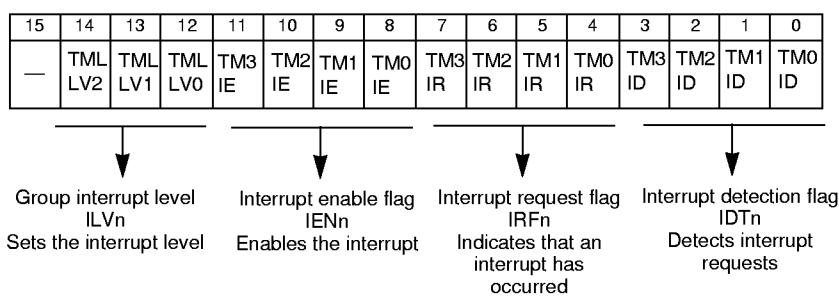
Interrupt Group Name	Interrupt Cause (numbers represent the IDTn bit position)	Control Register (Group) Name
Group 0	2 Undefined instruction interrupt 1 Watchdog timer interrupt	Non-maskable interrupt control register (group) 0 G0ICR: x'00FC40'
Group 1	3 timer-counter 3 underflow 2 timer-counter 2 underflow 1 timer-counter 1 underflow 0 timer-counter 0 underflow	Maskable interrupt control register (group) 1 G1ICR: x'00FC42'
Group 2	3 timer-counter 7 underflow 2 timer-counter 6 underflow 1 timer-counter 5 underflow 0 timer-counter 4 underflow	Maskable interrupt control register (group) 2 G2ICR: x'00FC44'
Group 3	3 timer-counter 12 compare/capture B 2 timer-counter 12 compare/capture A 1 timer-counter 9 underflow 0 timer-counter 8 underflow	Maskable interrupt control register (group) 3 G3ICR: x'00FC46'
Group 4	3 — 2 timer-counter 10 compare/capture B 1 timer-counter 10 compare/capture A 0 timer-counter 10 underflow	Maskable interrupt control register (group) 4 G4ICR: x'00FC48'
Group 5	3 — 2 timer-counter 11 compare/capture B 1 timer-counter 11 compare/capture A 0 timer-counter 11 underflow	Maskable interrupt control register (group) 5 G5ICR: x'00FC4A'
Group 6	3 DMA ch3 end of transfer 2 DMA ch2 end of transfer 1 DMA ch1 end of transfer 0 DMA ch0 end of transfer	Maskable interrupt control register (group) 6 G6ICR: x'00FC4C'
Group 7	3 DMA ch7 end of transfer 2 DMA ch6 end of transfer 1 DMA ch5 end of transfer 0 DMA ch4 end of transfer	Maskable interrupt control register (group) 7 G7ICR: x'00FC4E'

Table 3-1-1 Summary of Interrupt Control Registers (2/2)

Group 8	3 External interrupt IRQ3 2 External interrupt IRQ2 1 External interrupt IRQ1 0 External interrupt IRQ0	Maskable interrupt control register (group) 8 G8ICR: x'00FC50'
Group 9	3 Serial ch1 receive interrupt 2 Serial ch1 transmit interrupt 1 Serial ch0 receive interrupt 0 Serial ch0 transmit interrupt	Maskable interrupt control register (group) 9 G9ICR: x'00FC52'
Group 10	1 End of A/D conversion interrupt 0 Key pin ORed interrupts	Maskable interrupt control register (group) 10 G10ICR: x'00FC54'

With the exception of Group 0, a control register for each group controls the interrupts allocated to that group. For example, if underflow of timer 0 occurs in the MN1020012, the interrupt request flag (IRF0=TM0IR) of the maskable interrupt control register (group) 1 (G1ICR) will be set to '1'. If the corresponding interrupt enable flag (IEN0=TM0IE) has been set to '1', the interrupt request will be transmitted to the CPU core. Whether or not the interrupt will be accepted is determined by the PSW interrupt enable flag (IE) and a comparison between the interrupt mask level (IM2~0) set in the processor status word (PSW) and the G1ICR group interrupt level (ILVn=TMLLV2~0).

G1ICR: x'00FC42'



For further details on the content and operation, refer to section 2-5 "Interrupt Controller" of the "MN10200 Series LSI Manual, Linear Address Edition". Refer to the "MN10200 Series Command Manual, Linear Address Edition". Next, the specifications (external interrupt) of this LSI chip will be described.

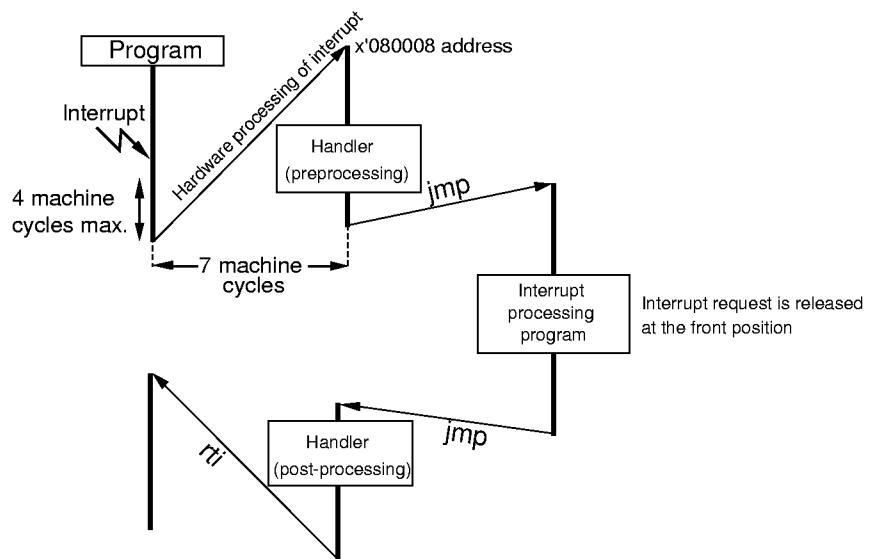


Figure 3-1-1 Interrupt Processing Execution Time (number of cycles)

3-2 External Interrupts

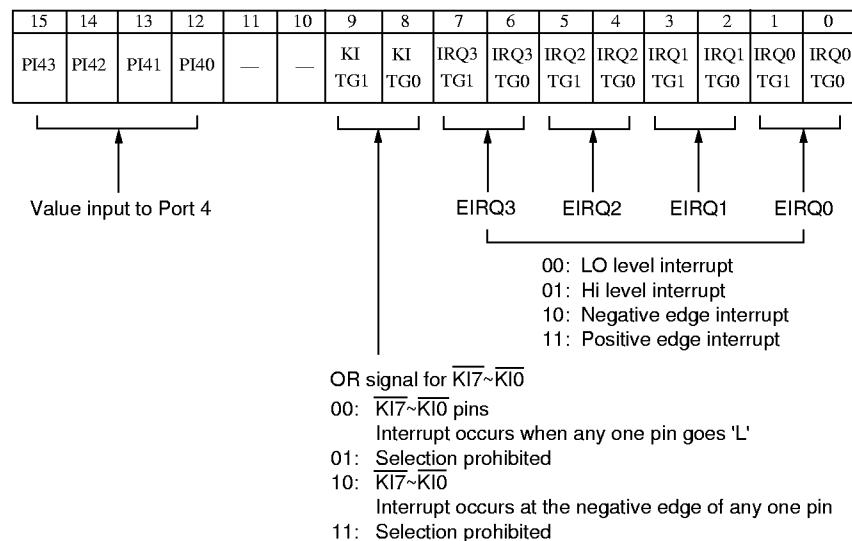
3-2-1 External Pin Interrupts

The external pin interrupts of this LSI chip are controlled by Group 8.

The external pin interrupt condition control register (EXTMD) sets the interrupt conditions.

EXTMD sets the interrupt level and timing of the external interrupt. Arbitrary levels or edges can be set for each pin.

EXTMD: x'00FC56'



3-2-2 Key Input Interrupts

The Key input interrupts of this LSI chip are controlled by Group 10 and correspond to the pins of port 0 (P07~P00).

The external pin interrupt condition control register (EXTMD) sets the interrupt conditions.

When either EXTMD9 or EXTMD8 are set for an interrupt if any one pin be at a 'LO' level, an interrupt will occur if at least one pin of $\overline{KI7} \sim \overline{KI0}$ goes to a 'LO' level.

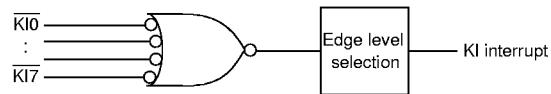


Figure 3-2-1 Key Input Interrupt

Individual bits of P07~P00 ($\overline{KI7} \sim \overline{KI0}$) cannot be selected for either a general purpose port or a key input interrupt. Therefore, all the pins will be set as general purpose ports or key input interrupts. If used as general purpose ports, disable the G10ICR key input interrupt.

3-3 Example Interrupt Setting

3-3-1 Example of External Pin Interrupt Setting

A negative (falling) edge at external interrupt pin IRQ0 (P40) generates an interrupt.

After reset is released, the external interrupt condition control register (EXTMD) is set to generate interrupt requests for 'L' level signals. IRQ0IR of maskable interrupt control register (group) 8 (G8ICR) is set to '0'.

■ Interrupt Enable Setting

- (1) Interrupt pin IRQ0 (P40) sets the interrupt condition. In this case, IRQ0TG of EXTMD is set with the value '2' (bit string 10: negative edge).

EXTMD: x'00FC56'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI43	PI42	PI41	PI40	—	—	KI TG1	KI TG0	IRQ3 TG1	IRQ3 TG0	IRQ2 TG1	IRQ2 TG0	IRQ1 TG1	IRQ1 TG0	IRQ0 TG1	IRQ0 TG0
—	—	—	—	—	—	0	0	0	0	0	0	0	0	1	0

Interrupt level 4 has been set in this example.

- (2) Interrupts are enabled. At this time, all prior interrupt requests are cleared. In other words, in maskable interrupt control register (group) 8 (G8ICR), the interrupt level is set in IRQLV2~0, IRQ0IR is set to '0' and IRQ0IE to '1'.

G8IRC: x'00FC50'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	IRQ	IRQ	IRQ	IRQ3	IRQ2	IRQ1	IRQ0	IRQ3	IRQ2	IRQ1	IRQ0	IRQ3	IRQ2	IRQ1	IRQ0
—	LV2	LV1	LV0	IE	IE	IE	IE	IR	IR	IR	IR	ID	ID	ID	ID
—	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0

- (3) The interrupt enable flag (IE) and the interrupt mask level (IMn) of the processor status word (PSW) are set to '1' and '7' (bit string 111) respectively to enable the interrupts.

Thereafter, an interrupt will be generated whenever there is a negative (falling) edge at interrupt pin IRQ0 (P40).

■ Interrupt Processing

- (4) During interrupt preprocessing, the interrupt accept group number register (IAGR) is read and the interrupt group specified.
- (5) G8ICR is read and the cause of the interrupt within a group is specified. IRQ0ID is checked with a bit test (BTST) instruction. If it is '1', the interrupt is processed.
- (6) IRQ0IR of G8ICR is cleared.
- (7) After interrupt processing is complete, an interrupt return (RTI) instruction will return program control to the original program.

Normally the program generates the leading address for the interrupt and then branches to that address.

During interrupt processing, the IM level in the PSW is the interrupt level. Also, since IE is '0', multiple interrupts are disabled. As long as the PSW is not manipulated, with the exception of non-maskable interrupts, other interrupts will not be accepted during interrupt processing.

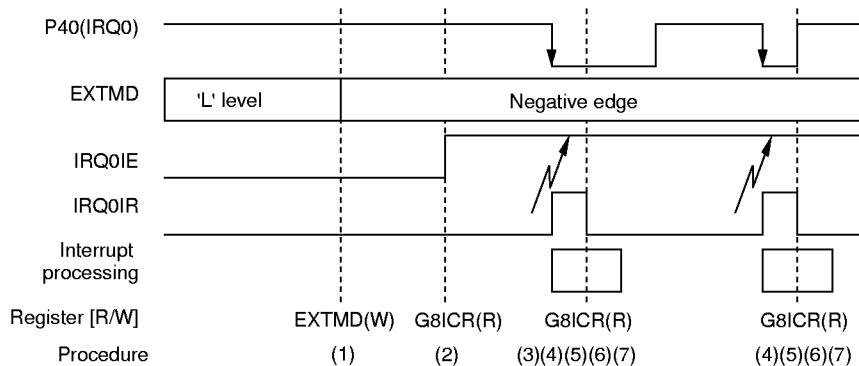


Figure 3-3-1 Timing Chart of Example External Pin Interrupt Setting

3-3-2 Example Key Input Interrupt Setting

When stopped, an interrupt is generated by a 'L' level at key input interrupt pins P07~P00 ($\overline{K17} \sim \overline{K0}$).

After reset is released, the external interrupt condition control register (EXTMD) is set to generate interrupt requests for 'L' levels. KIIR of maskable interrupt control register (group) 10 (G10ICR) is set to '0'.

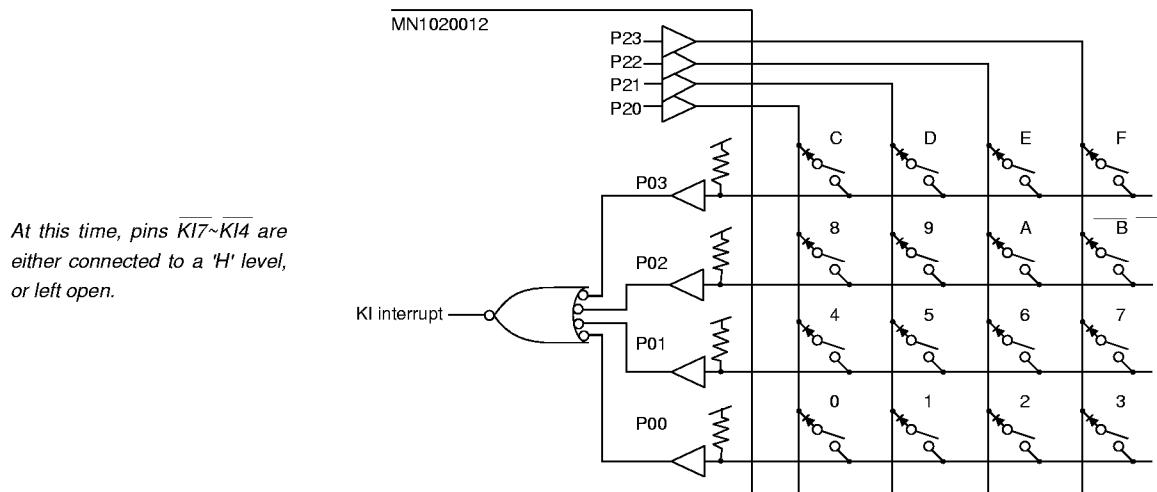


Figure 3-3-2 Example KI Input Circuit

■ Interrupt Enable Setting

- (1) The port 0 I/O control register (P0DIR) and port 2 I/O control register (P2DIR) set the port direction for either input or output. By setting pins P03~P00 for input and pins P23~P20 for output, a low level will be output from all pins P23~P20.

$P0DIR: x'00FFE0'$

7	6	5	4	3	2	1	0
P0DIR7	P0DIR6	P0DIR5	P0DIR4	P0DIR3	P0DIR2	P0DIR1	P0DIR0
0	0	0	0	0	0	0	0

$P2DIR: x'00FFE2'$

7	6	5	4	3	2	1	0
—	—	—	—	P2DIR3	P2DIR2	P2DIR1	P2DIR0
0	0	0	0	0	1	1	1

P2OUT: x'00FFC2'

7	6	5	4	3	2	1	0
—	—	—	—	P2OUT3	P2OUT2	P2OUT1	P2OUT0
0	0	0	0	1	1	1	1

- (2) P07~P00 are set in port pull-up control register (PPLU) to be pulled up so that interrupts will not be generated when keys are not pressed. When one key is pressed, any one of P07~P00 will become '0' and a key interrupt signal will be generated.

PPLU: x'00FFB0'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	SBT 1P	SBO 1P	SBI 1P	SBT 0P	SBO 0P	SBI 0P	—	PKIP	P43P	P42P	P41P	P40P	DHP	DLP
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

- (3) The external interrupt condition control register (EXTMD) sets the key input pins to a 'L' level.

EXTMD: x'00FC56'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI43	PI42	PI41	PI40	—	—	KI TG1	KI TG0	IRQ3 TG1	IRQ3 TG0	IRQ2 TG1	IRQ2 TG0	IRQ1 TG1	IRQ1 TG0	IRQ0 TG1	IRQ0 TG0
—	—	—	—	—	—	0	0	0	0	0	0	0	0	0	0

- (4) Interrupts are enabled. At this time, all prior interrupt requests are cleared. In other words, in maskable interrupt control register (group) 10 (G10ICR), the interrupt level is set, KIIR is set to '0' and KYIE to '1'.

G10ICR: x'00FC54'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	GP8 LV2	GP8 LV1	GP8 LV0	—	—	AN IE	KI IE	—	—	AN IR	KI IR	—	—	AN ID	KI ID
—	1	0	0	—	—	0	1	—	—	0	0	—	—	0	0

Interrupt level 4 has been set in this example.

- (5) The interrupt enable flag (IE) and the interrupt mask level (IMn) of the processor status word (PSW) are set to '1' and '7' (bit string 111) respectively to enable the interrupts.

Thereafter, interrupts will be generated when even one key is pressed.

Normally the program generates the leading address for the interrupt and then branches to that address.

During interrupt processing, the IM level in the PSW is the interrupt level. Also, since IE is '0', multiple interrupts are disabled. As long as the PSW is not manipulated, with the exception of non-maskable interrupts, other interrupts will not be accepted during interrupt processing.

Key assessment is performed based on results of reading the port 0 input register (P0IN).

■ Interrupt Processing

- (6) During interrupt preprocessing, the interrupt accept group number register (IAGR) is read and the interrupt group specified.
- (7) G10ICR is read and the cause of the interrupt within a group is specified. KIID is checked with a bit test (BTST) instruction. If it is '1', the interrupt is processed.
- (8) KIIR of G10ICR is cleared.
- (9) Processing is performed to assess the key.
- (10) After interrupt processing is complete, an interrupt return (RTI) instruction will return program control to the original program.

■ Key Assessment Processing

- (11) Port 2 output register (P2OUT) is set to x'E' (bit string 1110: only P20 is '0').

P2OUT: x'00FFC2'

7	6	5	4	3	2	1	0
—	—	—	—	P2OUT3	P2OUT2	P2OUT1	P2OUT0
0	0	0	0	1	1	1	0

- (12) If any of keys 0, 4, 8, or C are pressed, the bit corresponding to port 0 input register (P0IN) will become '0'. This is checked by the bit test instruction (BTST).

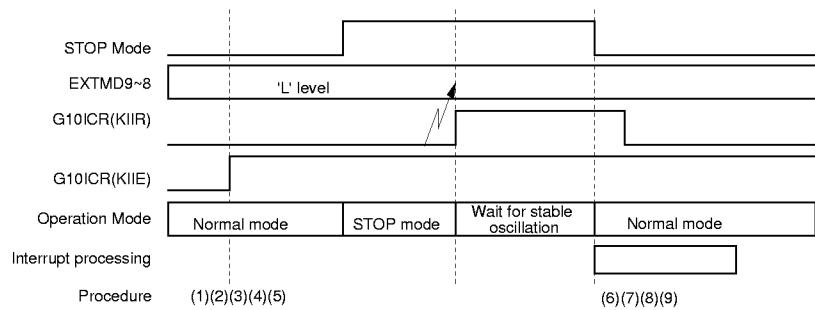
P0IN: x'00FFD0'

7	6	5	4	3	2	1	0
P0IN7	P0IN6	P0IN5	P0IN4	P0IN3	P0IN2	P0IN1	P0IN0

- (13) P2OUT is set to x'D' (bit string 1101: only P21 is '0').

- (14) If any of keys 1, 5, 9, or D are pressed, the bit corresponding to P0IN will become '0'. This is checked by the bit test instruction (BTST).

- (15) P2OUT is set to x'B' (bit string 1011: only P22 is '0').
- (16) If any of keys 2, 6, A, or E are pressed, the bit corresponding to P0IN will become '0'. This is checked by the bit test instruction (BTST).
- (17) P2OUT is set to x'7' (bit string 0111: only P23 is '0').
- (18) If any of keys 3, 7, B, or F are pressed, the bit corresponding to P0IN will become '0'. This is checked by the bit test instruction (BTST).



If used in a remote control application, the STOP mode is transferred to and low power consumption is achieved. If an interrupt is initiated during a STOP, oscillation stabilization is waited for. At 20MHz, the wait will be for 6.5536 msec. Afterwards, program control branches to address x'080008'.

Figure 3-3-3 Timing Chart of Example Key Input Interrupt Setting

3-3-3 Example Watch Dog Timer Interrupt Setting

The watchdog timer generates interrupts.

When using the watchdog function, operation will begin if the WDRST flag of the CPU mode control register (CPUM) is enabled (set to '0') after reset. Since a non-maskable interrupt will be generated if the watchdog counter overflows, it is necessary for the main program to clear the watchdog timer.

A watchdog interrupt is generated when the watchdog timer counts the SYSCLK 65,536 times (6.5536 msec for a 20MHz oscillation).

■ Interrupt Enable Setting

- (1) The interrupt enable flag (IE) and the interrupt mask level (IMn) of the processor status word (PSW) are set to '1' and '7' (bit string 111) respectively to enable the interrupts.
- (2) WDRST of the CPUM is cleared and the watchdog timer is operated.

CPUM: X'00FC00'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WD RST	—	—	—	—	—	—	—	—	—	—	OSC ID	STOP	HALT	OSC1	OSC2
0	—	—	—	—	—	—	—	—	—	—	0	0	0	0	0

■ Watchdog Timer Clear

- (3) By setting WDRST of the CPUM to '1', and then immediately clearing it to '0', the watchdog time is cleared. The watchdog timer is cleared to '0' when WDRST is set to '1'.

■ Interrupt Processing

When an interrupt is generated and accepted, program control will branch to address x'080008'.

- (4) During interrupt preprocessing, the interrupt accept group number register (IAGR) is read and the interrupt group specified.
- (5) The non-maskable interrupt control register (group) 0 (G0ICR) is read and the watchdog timer interrupt is verified. WDIF is checked with a bit test (BTST) instruction. If it is '1', the interrupt is processed.

During interrupt processing, IM of the PSW is at a high level and other interrupts are not accepted.

- (6) WDIF of the G0ICR is cleared to '0'.
- (7) After interrupt processing is complete, an interrupt return (RTI) instruction will return program control to the original program.

The watchdog counter also functions as an oscillation stabilization wait counter. WDIF is cleared to '0' when transferring to the stop state so that it may operate as an oscillation stabilization wait counter upon return from the stop state. Also, after transfer to the normal state, it is cleared to '0' again.

[¹² MN10200 Series LSI Manual, Linear Address Edition
section 2-6, "Standby Function"]

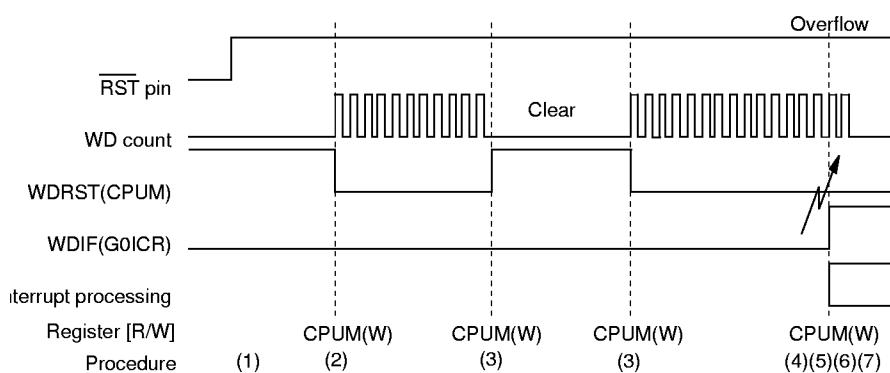


Figure 3-3-4 Timing Chart of Example Watchdog Timer Interrupt Setting

Chapter 3 Interrupt Control

Chapter 4 Timer/Counter Functions

4

4-1 Summary of Timer Functions

4-1-1 Overview

This LSI chip has ten 8-bit timers (timer 0~9) and three 16-bit timers (timer 10~12) on-chip, for a total of 13 timer/counters.

Table 4-1-1 Timer Functions (1/3)

Function \ Timer	8-bit Timer			
	Timer 0	Timer 1	Timer 2	Timer 3
Interrupt outputs	Group1 (G1ICR) • TM0IR	Group1 (G1ICR) • TM1IR	Group1 (G1ICR) • TM2IR	Group1 (G1ICR) • TM3IR
Interrupt sources	Timer 0 underflow	Timer 1 underflow	Timer 2 underflow	Timer 3 underflow
Clock sources	• TM0IO pin • Prescaler 0 • Prescaler 1	• TM1IO pin • Timer 0 • Prescaler 0 • Prescaler 1	• TM2IO pin • Timer 1 • Prescaler 0 • Prescaler 1	• TM3IO pin • Timer 2 • Prescaler 0 • Prescaler 1
Counter method	Count down	Count down	Count down	Count down
Interval timer	✓	✓	✓	✓
Event counter	✓	✓	✓	✓
Timer output	✓	✓	✓	✓
PWM	—	—	—	—
2-phase timer output	—	—	—	—
One-shot pulse generator	—	—	—	—
Single-phase capture input	—	—	—	—
Two-phase capture input	—	—	—	—
Two-phase encoder	—	—	—	—
External count direction control	—	—	—	—
External count reset control	—	—	—	—
Serial interface transfer clock generator	—	—	—	—
Synchronous output timing generator	—	✓	—	—
A/D conversion timing generator	—	—	—	—

Table 4-1-1 Timer Functions (2/3)

8-bit Timer				
Timer 4	Timer 5	Timer 6	Timer 7	Timer 8
Group2 (G2ICR) • TM4IR	Group2 (G2ICR) • TM5IR	Group2 (G2ICR) • TM6IR	Group2 (G2ICR) • TM7IR	Group3 (G3ICR) • TM8IR
Timer 4 underflow	Timer 5 underflow	Timer 6 underflow	Timer 7 underflow	Timer 8 underflow
• TM4IO pin • Timer 3 • Prescaler 0 • Prescaler 1	• TM5IO pin • Timer 4 • Prescaler 0 • Prescaler 1	• TM6IO pin • Timer 5 • Prescaler 0 • Prescaler 1	• TM7IO pin • Timer 6 • Prescaler 0 • Prescaler 1	• TM8IO pin • Timer 7 • Prescaler 0 • Prescaler 1
Count down				
✓	✓	✓	✓	✓
✓	✓	✓	✓	✓
✓	✓	✓	✓	✓
—	—	—	—	—
—	—	—	—	—
—	—	—	—	—
—	—	—	—	—
—	—	—	—	—
—	—	—	—	—
—	—	—	—	✓
—	—	—	—	—
—	—	—	✓	—



Table 4-1-1 Timer Functions (3/3)

Function \ Timer	8-bit Timer	16-bit Timer		
Function	Timer 9	Timer 10	Timer 11	Timer 12
Interrupt outputs	Group3 (G3ICR) • TM9IR	Group4 (G4ICR) • TM10UIR • TM10AIR • TM10BIR	Group5 (G5ICR) • TM11UIR • TM11AIR • TM11BIR	Group3 (G3ICR) • TM12AIR • TM12BIR
Interrupt sources	Timer 9 underflow	• TM10 underflow • TM10 compare A match, TM10 capture A • TM10 compare B match, TM10 capture B	• TM11 underflow • TM11 compare A match, TM11 capture A • TM11 compare B match, TM11 capture B	• TM12 compare A match, TM12 capture A • TM12 compare B match, TM12 capture B
Clock sources	• TM9IO pin • Timer 8 • Prescaler 0 • Prescaler 1	• SYSCLK • Prescaler 0 • Prescaler 1 • TM10IOB pin • Two-phase encoder	• SYSCLK • Prescaler 0 • Prescaler 1 • TM11IOB pin • Two-phase encoder	• SYSCLK • Prescaler 0 • Prescaler 1 • TM12IOB pin
Counter method	Count down	Up/down counter	Up/down counter	Up/down counter
Interval timer	✓	✓	✓	✓
Event counter	✓	✓	✓	✓
Timer output	✓	✓	✓	✓
PWM	—	Arbitrary duty	Arbitrary duty	Arbitrary duty
2-phase timer output	—	✓	✓	✓
One-shot pulse generator	—	✓	✓	✓
Single-phase capture input	—	✓	✓	✓
Two-phase capture input	—	✓	✓	✓
Two-phase encoder	—	Multiple of 4, multiple of 1	Multiple of 4, multiple of 1	—
External count direction control	—	✓	✓	—
External count reset control	—	✓	✓	—
Serial interface transfer clock generator	✓	—	—	—
Synchronous output timing generator	—	—	—	✓
A/D conversion timing generator	—	—	—	—

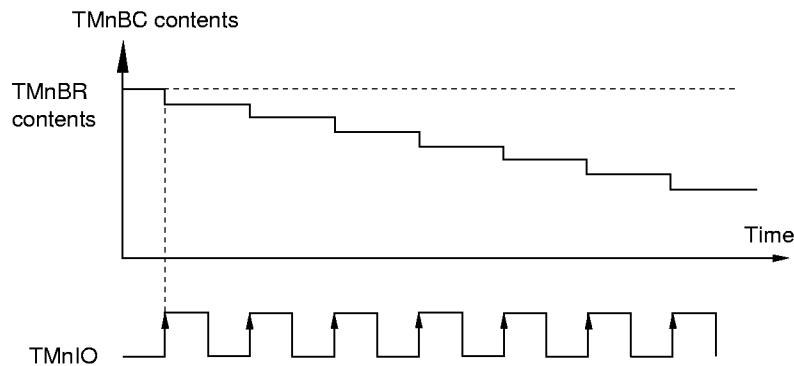


Figure 4-1-1 Timing Chart of Event Counter (TM0~9)

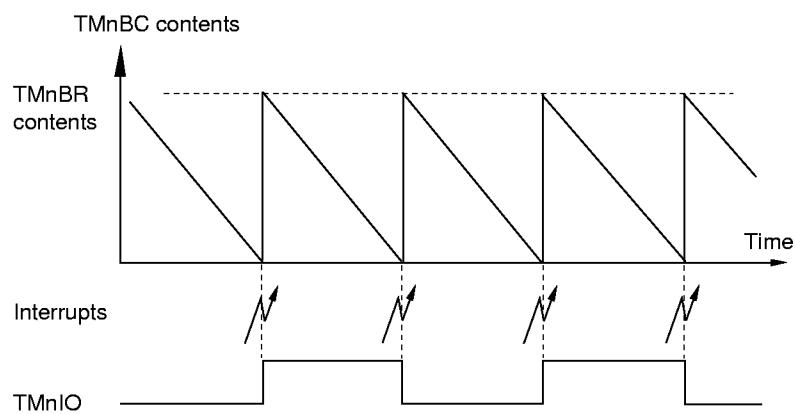


Figure 4-1-2 Timing Chart of Timer Output, Interval Timer (TM0~9)

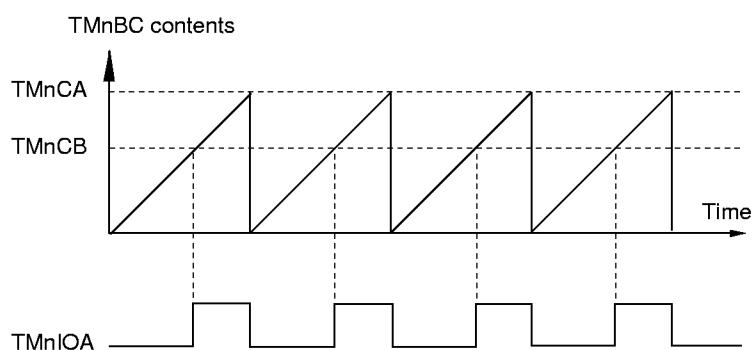


Figure 4-1-3 Timing Chart of PWM Output (TM10~12)

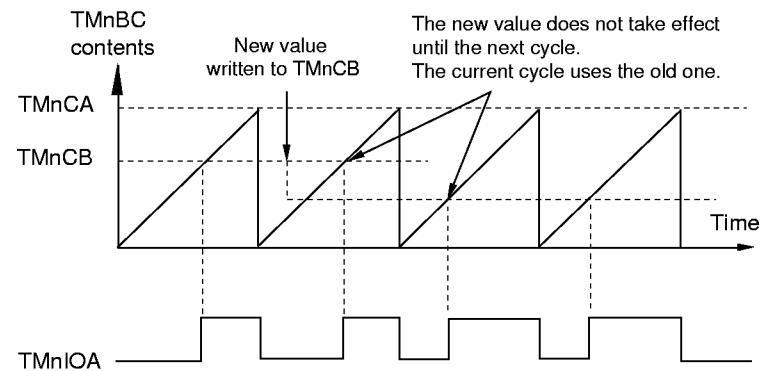


Figure 4-1-4 Timing Chart of PWM Output with Data Change (TM10~12)

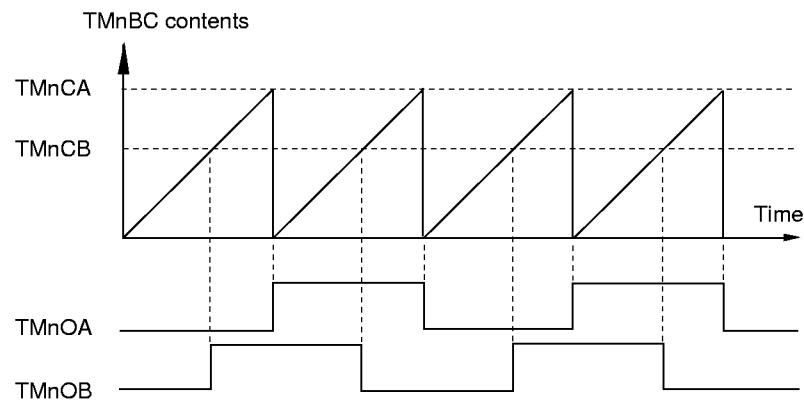


Figure 4-1-5 Timing Chart of Two-phase Timer Output (TM10~12)

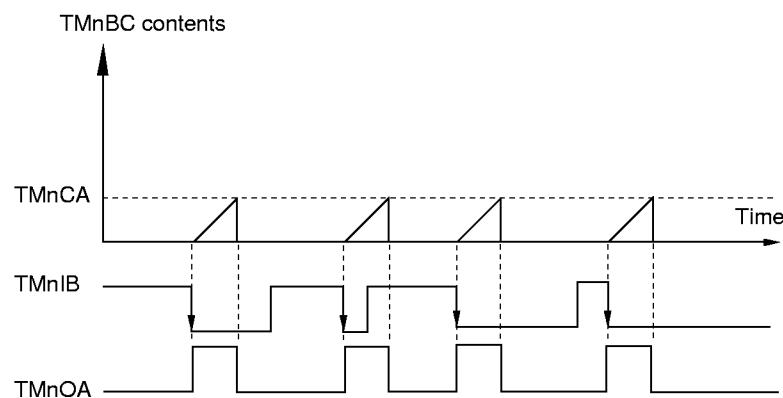


Figure 4-1-6 Timing Chart of One-shot Pulse Output (TM10~12)

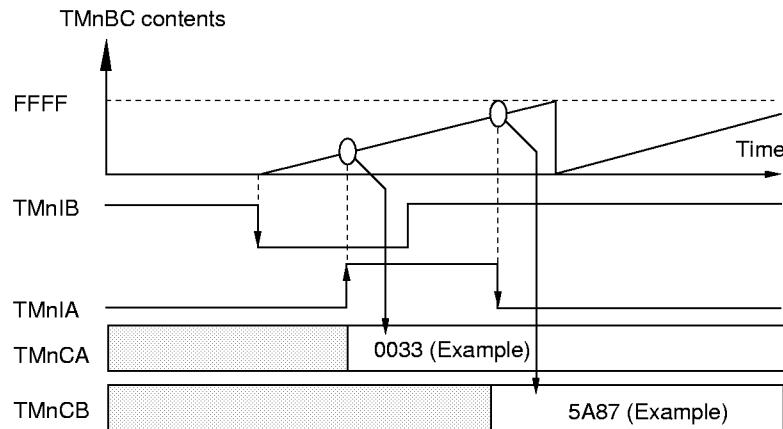


Figure 4-1-7 Timing Chart of Single-phase Capture Input (TM10~12)

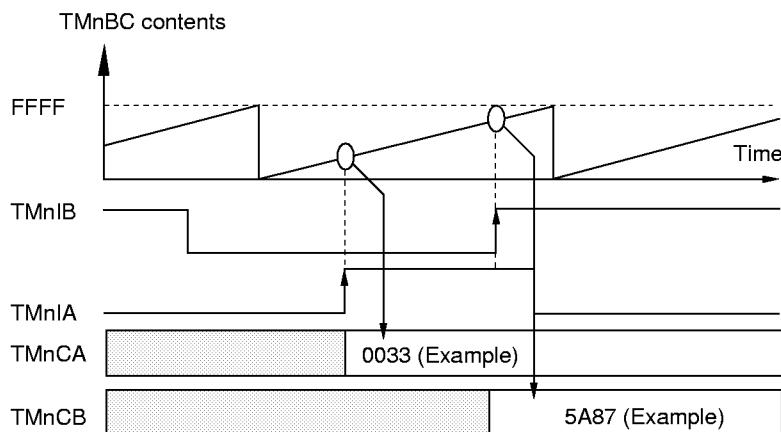


Figure 4-1-8 Timing Chart of Two-phase Capture Input (TM10~12)

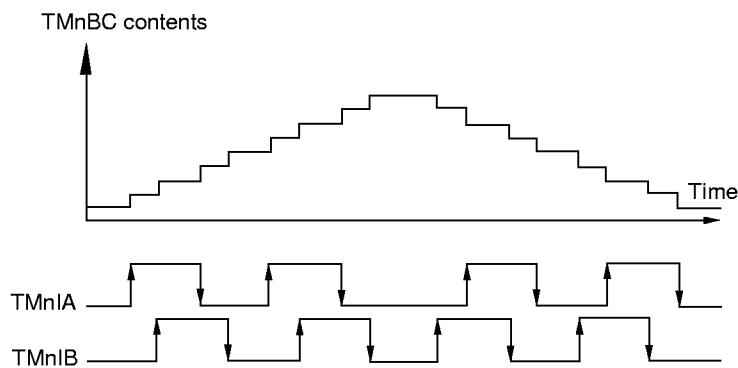


Figure 4-1-9 Timing Chart of Two-phase Encoder (multiple of 4) (TM10, 11)

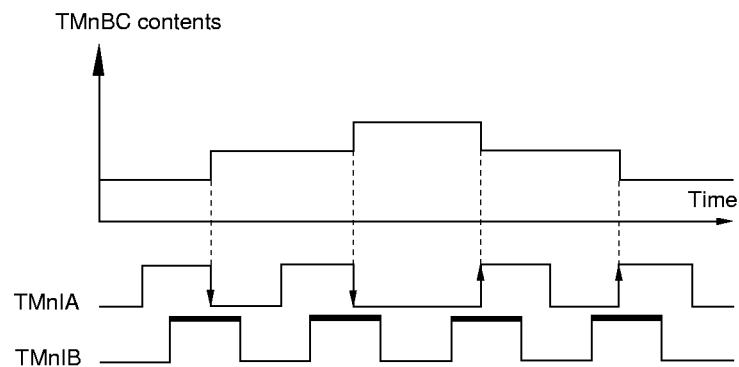


Figure 4-1-10 Timing Chart of Two-phase Encoder
(multiple of 1) (TM10, 11)

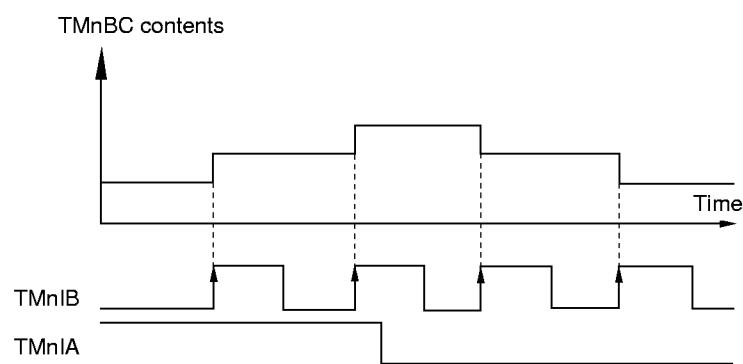


Figure 4-1-11 Timing Chart of External Count Direction Control (TM10, 11)

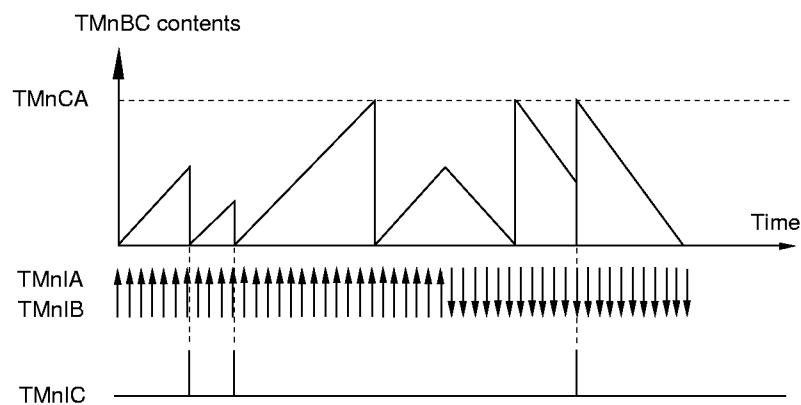


Figure 4-1-12 Timing Chart of External Count Reset Control
(for two-phase Encoder) (TM10, 11)

■ Timers 0~9

Timers 0~9 are 8-bit timers. These countdown timers use the 8-bit value in the base registers (TMnBR) plus one as their frequency dividers. (It is prohibited to set TMnDR to '0'.) The interrupt source is underflow of the corresponding timer (when the binary counter contents change from x'00' to an 8-bit set value). Applications include interval timers, event counters, clock output, serial interface reference clocks, synchronous output timing, and A/D conversion start timing.

*Timers 0~9 can be cascaded.
For example, timer 0 + timer 1
form a 16-bit timer, timer 2 +
timer 3 + timer 4 form a 24-bit
timer. Cascading all ten yields
an 80-bit timer.*

*(Use a 5MHz or lower
frequency clock source when 6
or more channels are
cascaded.)*

■ Timers 10 and 11

Timers 10 and 11 are 16-bit timers. These up/down counters each have two compare/capture registers (TMnCA, TMnCB) for capturing or comparing the contents of the up/down counter and then generating PWM output or an interrupt. A double buffer mode is provided to delay changes in the PWM frequency or transition points until the next cycle, so as to avoid glitches in the PWM waveform or disrupted transition timings. Applications include interval timers, event counters (when generating clock signals), single-phase PWM, two-phase PWM, two types of capture circuits, two types of two-phase encoders, one-shot pulse generators, and external count direction control.



*Underflow interrupts only occur
when counting down.*

■ Timer 12

Timer 12 is a 16-bit timer. This up-counter has two compare/capture registers (TM12CA, TM12CB) for capturing or comparing the contents of the up-counter and then generating PWM output or an interrupt. A double buffer mode is provided to delay changes in the PWM frequency or transition points until the next cycle, so as to avoid glitches in the PWM waveform or disrupted transition timings. Applications include interval timers, event counters (when generating clock signals), single-phase PWM, two-phase PWM, two types of capture circuits, and one-shot pulse generators.

■ Prescalers 0 and 1

Prescalers 0 and 1 are 8-bit prescalers that may be used as frequency divider circuits for the system clock and supplied as count clocks to timers 0~12, enabling an easy means to generate low-frequency signals or synchronize the timers.

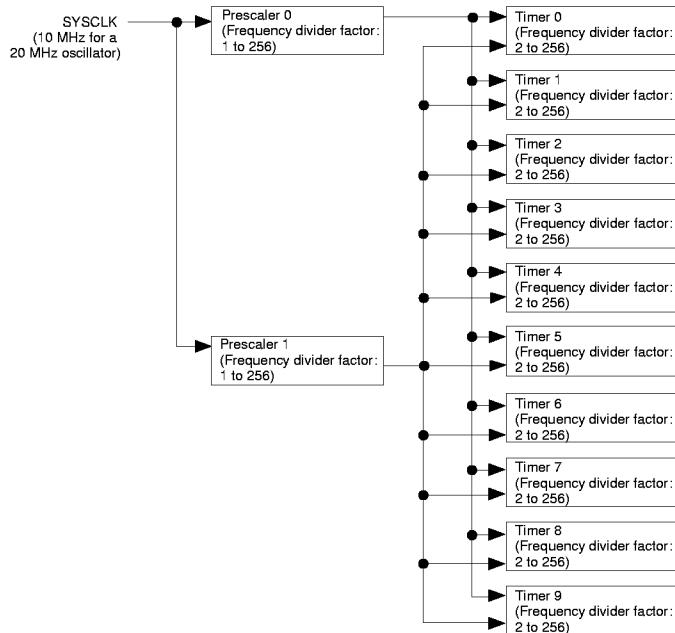


Figure 4-1-13 Relationships between Prescalers and Timers TC0 to TC9

Figure 4-1-14 gives an example of timer configuration. Combining timers into 16-bit timers and with prescalers permits the creation of a wide variety of interval timers.

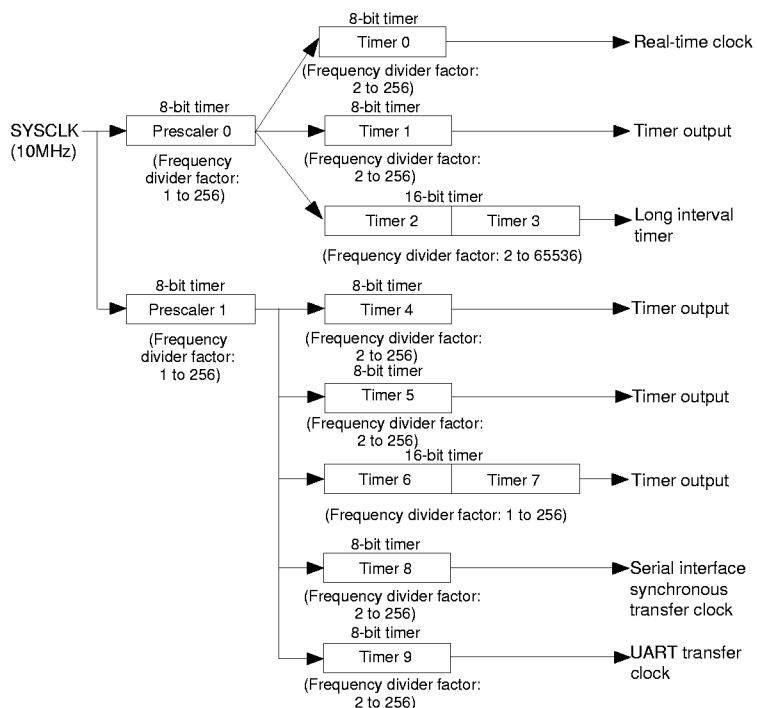


Figure 4-1-14 Example of Timer Configuration

In the cascade connection for timers 1~9, the output of timer n-1 (where n=1~9) is the input to timer n. Therefore, instead of an 8-bit frequency divider followed by another 8-bit frequency divider, two 8-bit counters will operate as a 16-bit frequency divider (16-bit counter). Also, the output from prescaler 0 or 1 can be used as the input to timers 0~12. During the normal and halt modes, SYSCLK is the frequency of the clock signal from the OSCI pin divided by 2 (10MHz for 20MHz oscillation). SYSCLK will cease during a STOP. SYSCLK is output to the external SYSCLK pin.

4-1-2 Timer Control Registers

The timer control registers for this LSI chip are listed below.

Table 4-1-2 Timer Control Register List (1/2)

	Register Abbreviation	Address	R/W	Register Name
Timer 0	TM0MD	x'00FE20'	R/W	Timer 0 mode register
	TM0BC	x'00FE00'	R	Timer 0 binary counter
	TM0BR	x'00FE10'	R/W	Timer 0 base register
Timer 1	TM1MD	x'00FE21'	R/W	Timer 1 mode register
	TM1BC	x'00FE01'	R	Timer 1 binary counter
	TM1BR	x'00FE11'	R/W	Timer 1 base register
Timer 2	TM2MD	x'00FE22'	R/W	Timer 2 mode register
	TM2BC	x'00FE02'	R	Timer 2 binary counter
	TM2BR	x'00FE12'	R/W	Timer 2 base register
Timer 3	TM3MD	x'00FE23'	R/W	Timer 3 mode register
	TM3BC	x'00FE03'	R	Timer 3 binary counter
	TM3BR	x'00FE13'	R/W	Timer 3 base register
Timer 4	TM4MD	x'00FE24'	R/W	Timer 4 mode register
	TM4BC	x'00FE04'	R	Timer 4 binary counter
	TM4BR	x'00FE14'	R/W	Timer 4 base register
Timer 5	TM5MD	x'00FE25'	R/W	Timer 5 mode register
	TM5BC	x'00FE05'	R	Timer 5 binary counter
	TM5BR	x'00FE15'	R/W	Timer 5 base register
Timer 6	TM6MD	x'00FE26'	R/W	Timer 6 mode register
	TM6BC	x'00FE06'	R	Timer 6 binary counter
	TM6BR	x'00FE16'	R/W	Timer 6 base register
Timer 7	TM7MD	x'00FE27'	R/W	Timer 7 mode register
	TM7BC	x'00FE07'	R	Timer 7 binary counter
	TM7BR	x'00FE17'	R/W	Timer 7 base register
Timer 8	TM8MD	x'00FE28'	R/W	Timer 8 mode register
	TM8BC	x'00FE08'	R	Timer 8 binary counter
	TM8BR	x'00FE18'	R/W	Timer 8 base register
Timer 9	TM9MD	x'00FE29'	R/W	Timer 9 mode register
	TM9BC	x'00FE09'	R	Timer 9 binary counter
	TM9BR	x'00FE19'	R/W	Timer 9 base register
Prescaler 0	PS0MD	x'00FE2A'	R/W	Prescaler 0 mode register
	PS0BC	x'00FE0A'	R	Prescaler 0 binary counter
	PS0BR	x'00FE1A'	R/W	Prescaler 0 base register
Prescaler 1	PS1MD	x'00FE2B	R/W	Prescaler 1 mode register
	PS1BC	x'00FE0B	R	Prescaler 1 binary counter
	PS1BR	x'00FE1B	R/W	Prescaler 1 base register

Table 4-1-2 Timer Control Register List (2/2)

Register Abbreviation	Address	R/W	Register Name
Timer 10	TM10MD	x'00FE30'	Timer 10 mode register
	TM10BC	x'00FE32'	Timer 10 binary counter
	TM10CA	x'00FE34'	Timer 10 compare/capture register A
	TM10CAX	x'00FE36'	Timer 10 compare/capture register set A
	TM10CB	x'00FE38'	Timer 10 compare/capture register B
	TM10CBX	x'00FE3A'	Timer 10 compare/capture register set B
Timer 11	TM11MD	x'00FE40'	Timer 11 mode register
	TM11BC	x'00FE42'	Timer 11 binary counter
	TM11CA	x'00FE44'	Timer 11 compare/capture register A
	TM11CAX	x'00FE46'	Timer 11 compare/capture register set A
	TM11CB	x'00FE48'	Timer 11 compare/capture register B
	TM11CBX	x'00FE4A'	Timer 11 compare/capture register set B
Timer 12	TM12MD	x'00FE50'	Timer 12 mode register
	TM12BC	x'00FE52'	Timer 12 binary counter
	TM12CA	x'00FE54'	Timer 12 compare/capture register A
	TM12CAX	x'00FE56'	Timer 12 compare/capture register set A
	TM12CB	x'00FE58'	Timer 12 compare/capture register B
	TM12CBX	x'00FE5A'	Timer 12 compare/capture register set B

TM10CAX, TM10CBX, TM11CAX, TM11CBX, TM12CAX, and TM12CBX, are dummy registers used when the double buffer mode is specified during PWM output, and do not actually exist.

4-1-3 Timer Block

Block diagrams of the MN1020012's timers 0~12 are shown below.

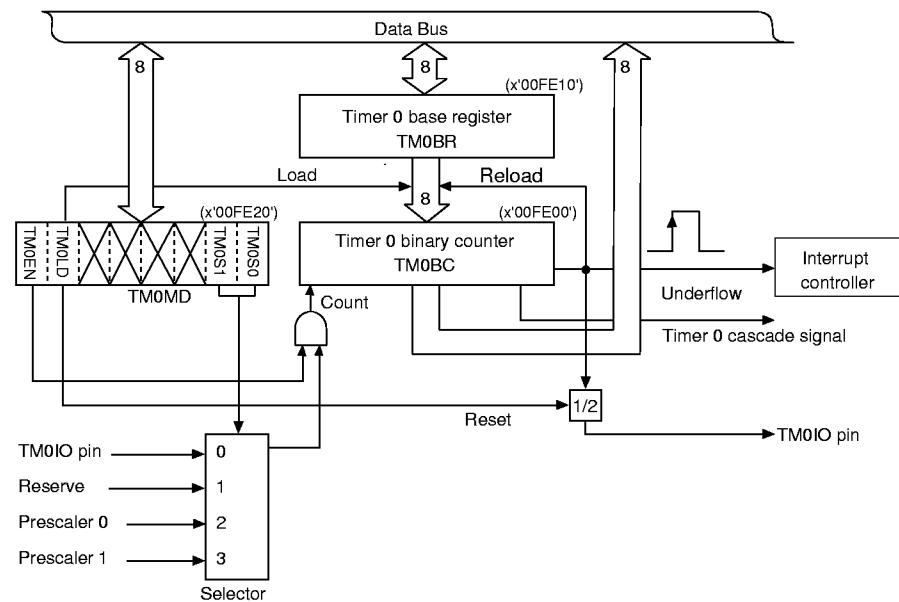


Figure 4-1-15 Timer 0 Block Diagram

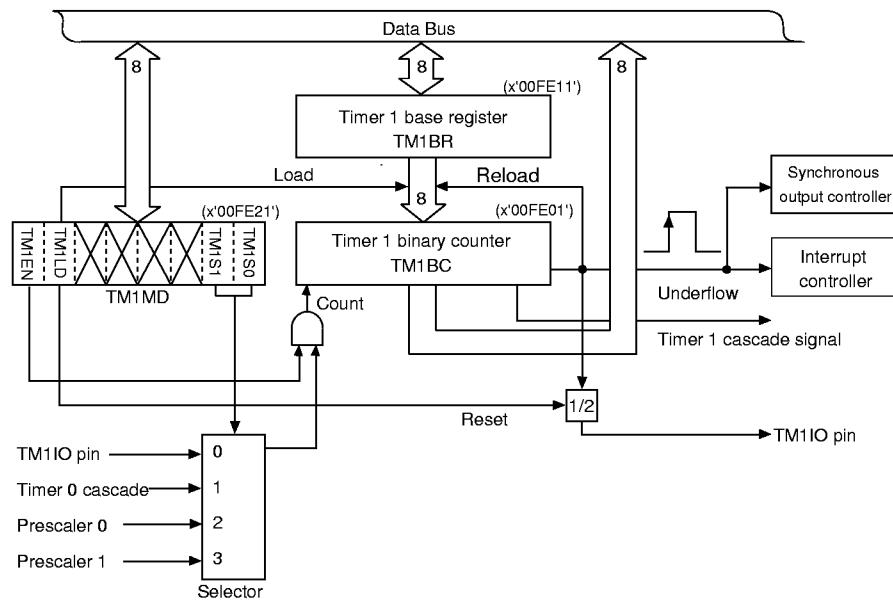


Figure 4-1-16 Timer 1 Block Diagram

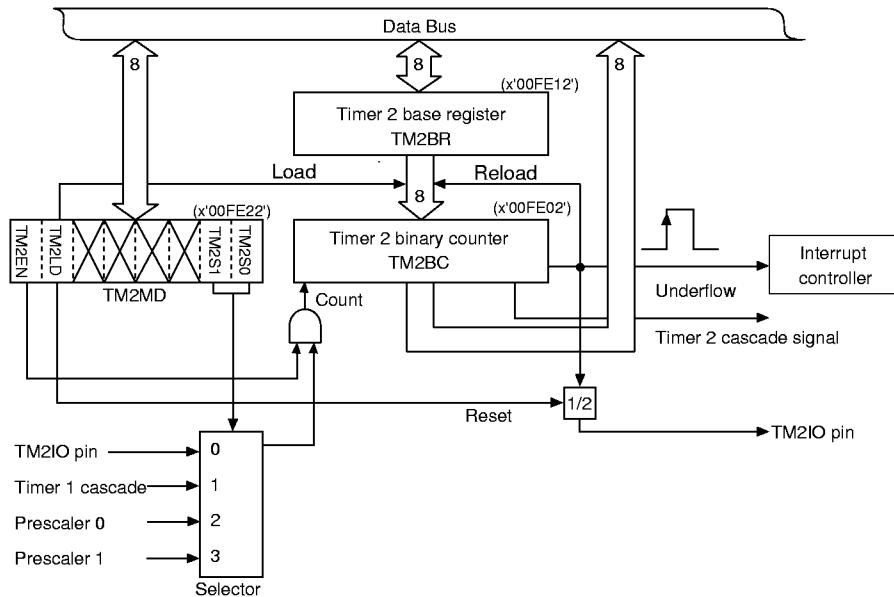


Figure 4-1-17 Timer 2 Block Diagram

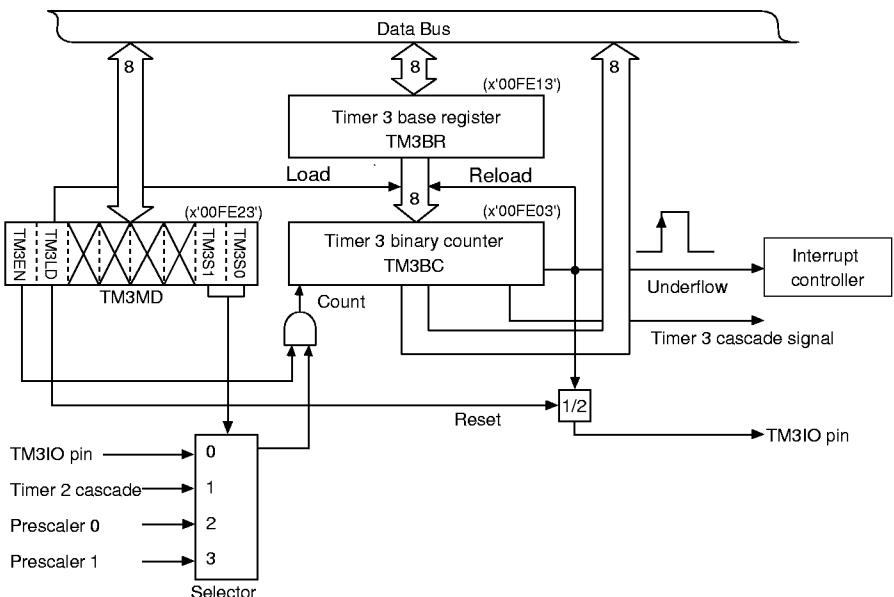


Figure 4-1-18 Timer 3 Block Diagram

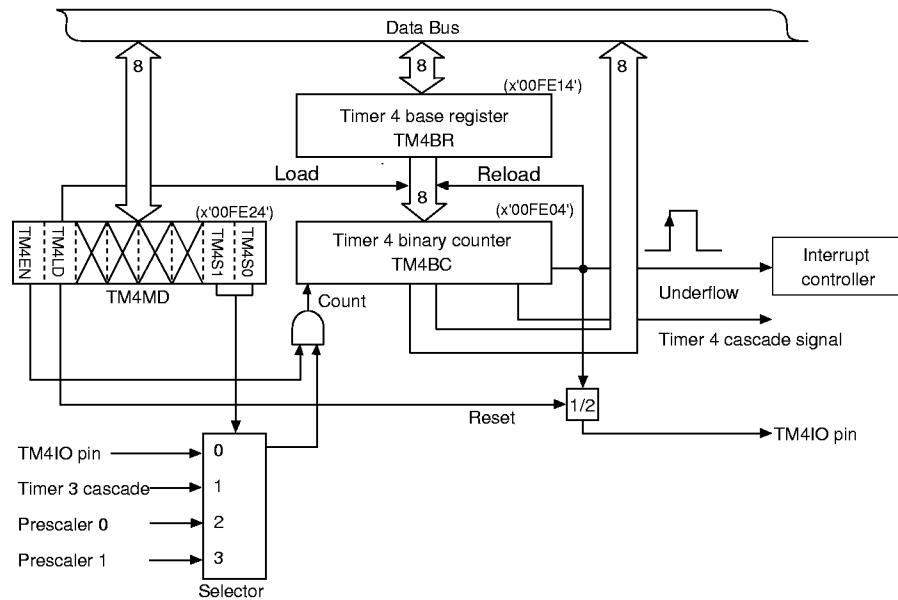


Figure 4-1-19 Timer 4 Block Diagram

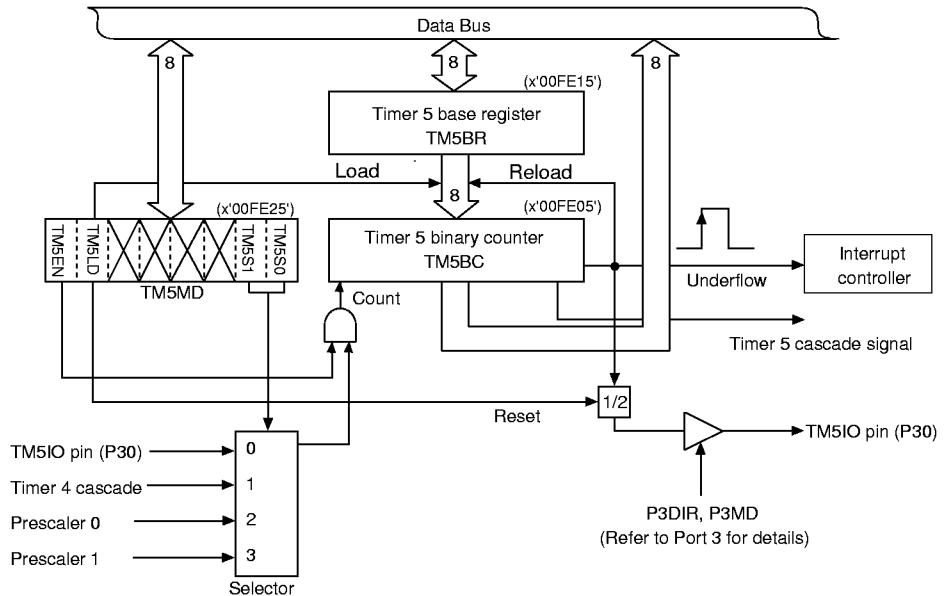


Figure 4-1-20 Timer 5 Block Diagram

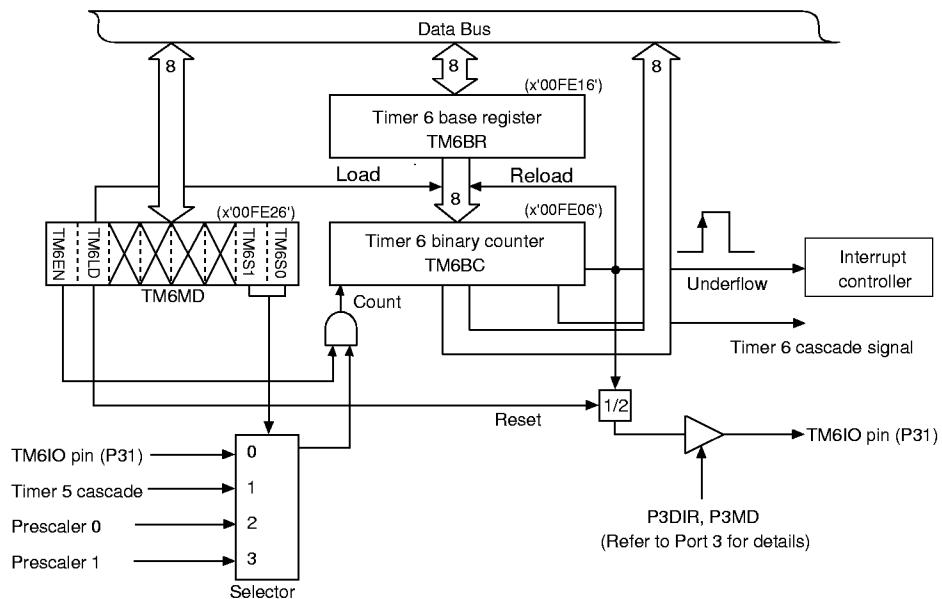


Figure 4-1-21 Timer 6 Block Diagram

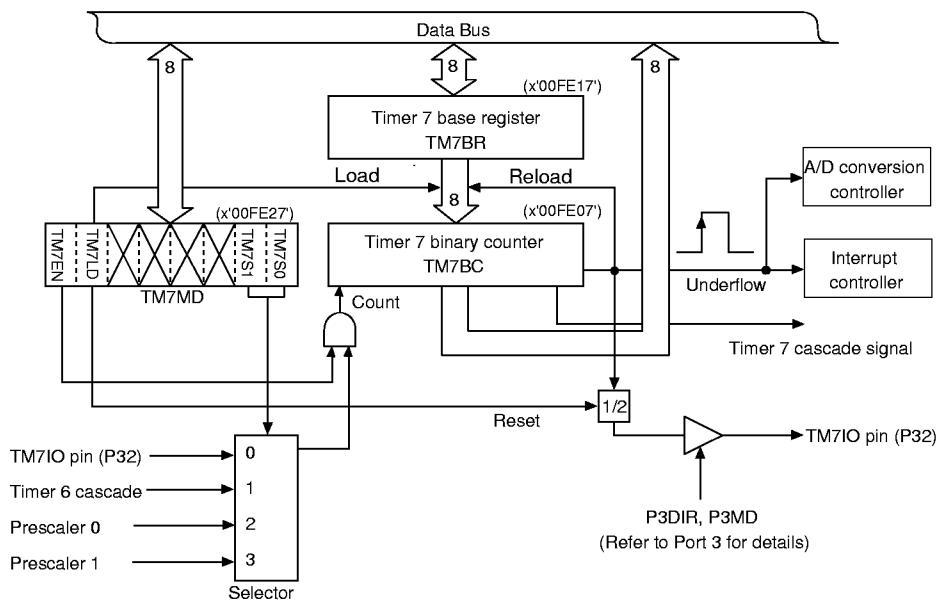


Figure 4-1-22 Timer 7 Block Diagram

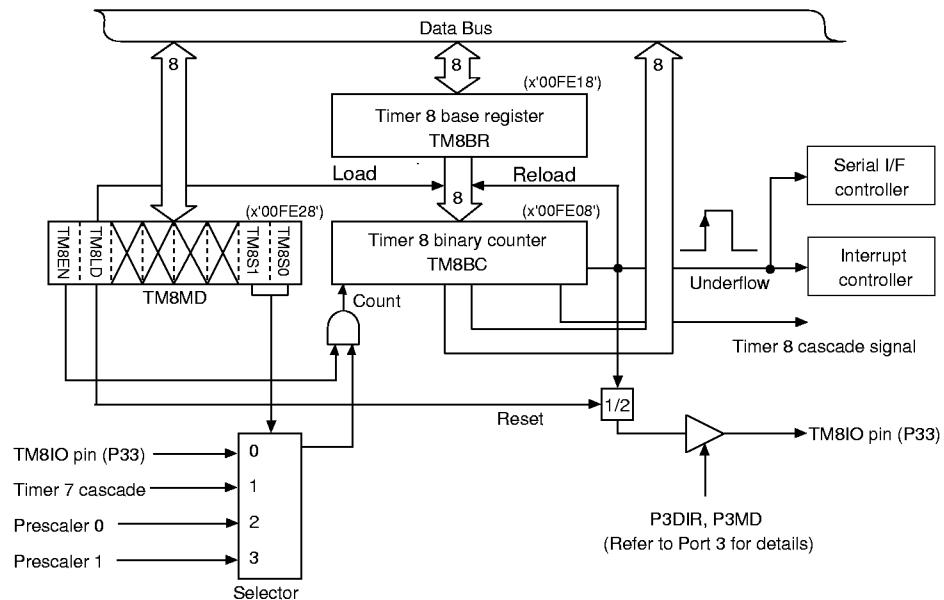


Figure 4-1-23 Timer 8 Block Diagram

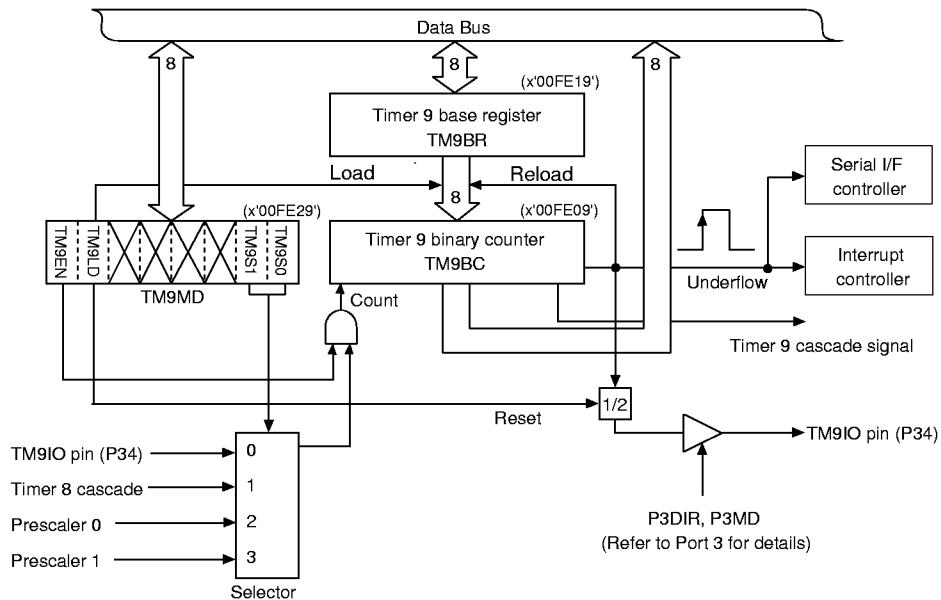


Figure 4-1-24 Timer 9 Block Diagram

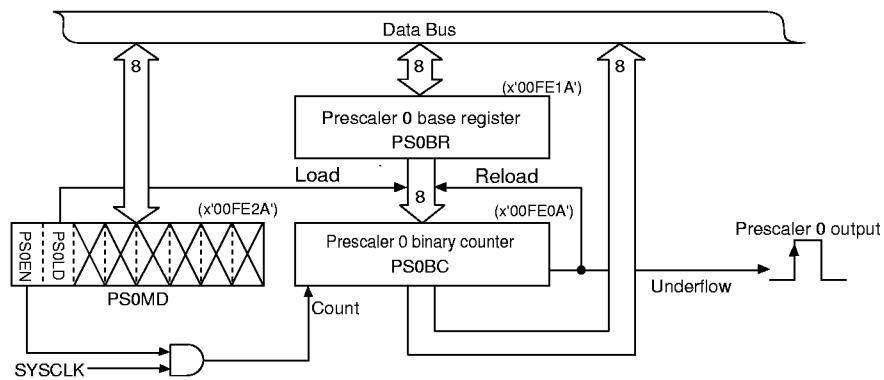


Figure 4-1-25 Prescaler 0 Block Diagram

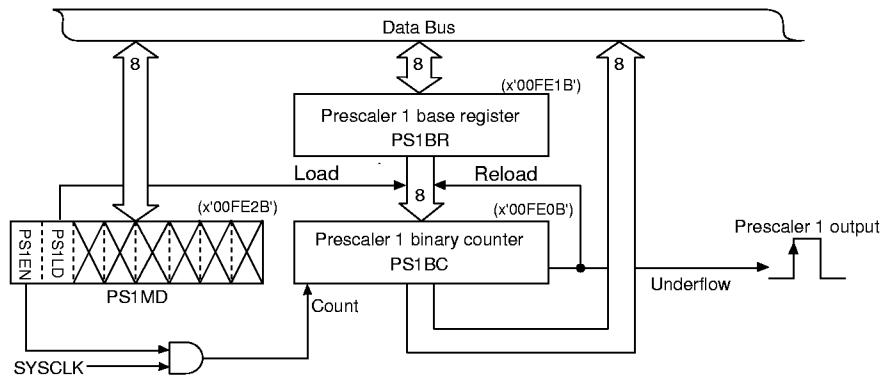


Figure 4-1-26 Prescaler 1 Block Diagram

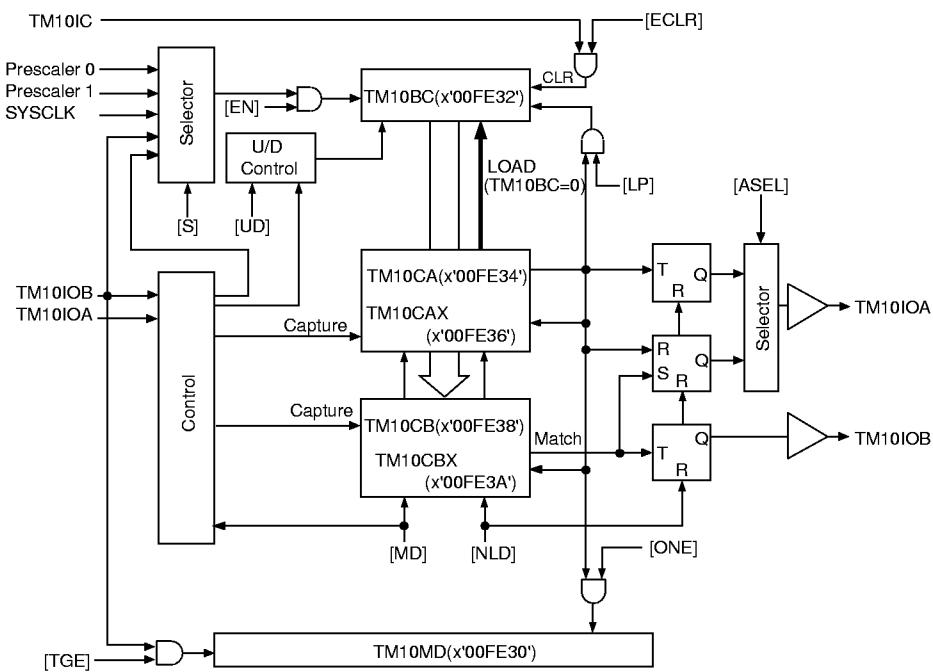


Figure 4-1-27 Timer 10 Block Diagram

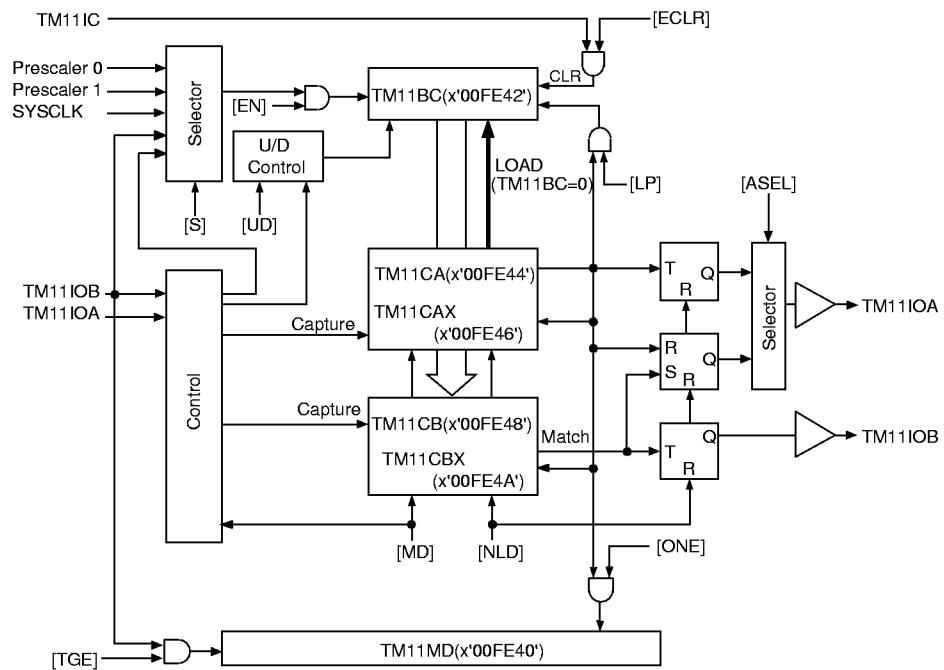


Figure 4-1-28 Timer 11 Block Diagram

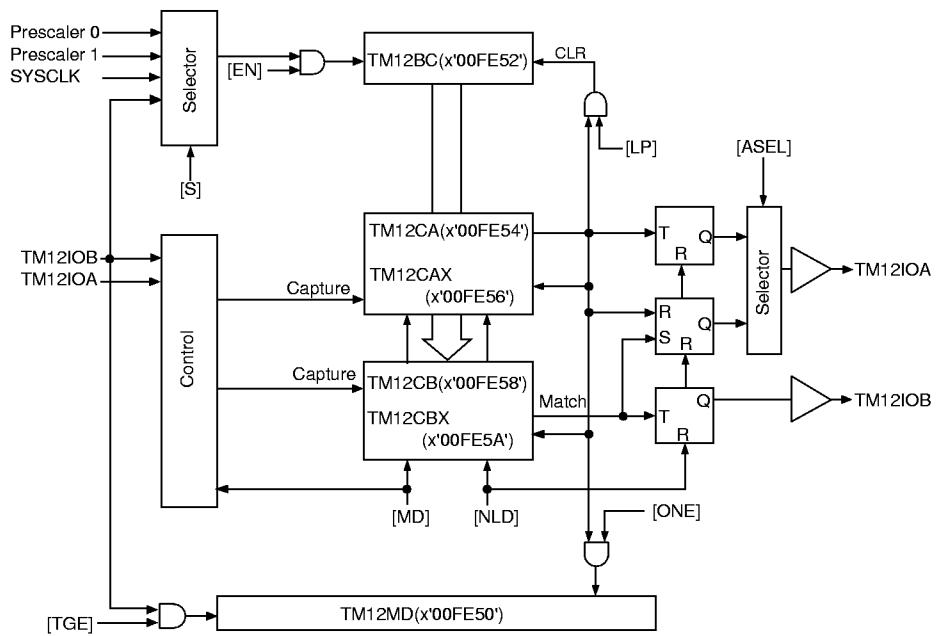


Figure 4-1-29 Timer 12 Block Diagram

4-2 Examples of 8-bit Timer Settings

4-2-1 8-bit Timer as an Event Counter

The event counter setting procedure is the same for timers 0~9. This example uses timer 0. The TM0IO pin input is divided by 4, and the procedure for generating interrupts when underflow occurs will be described.

- (1) The interrupt enable flag (IE) of the processor status word (PSW) is set to '1'.
- (2) The timer 0 mode register (TM0MD) verifies that the count operation has stopped.

Verification is not necessary immediately after a reset.

TM0MD: x'00FE20'

7	6	5	4	3	2	1	0
TM0 EN	TM0 LD	—	—	—	—	TM0 S1	TM0 S0
0	0	—	—	—	—	0	0

- (3) Interrupts are enabled, and at the same time, all prior interrupt requests are cleared. In other words, in maskable interrupt control register (group) 1 (G1ICR), the interrupt level (6~0) is set in TMLLV2~0, TM0IR is set to '0' and TM0IE to '1'. For example, x'4100' is written to G1ICR. Thereafter, an interrupt will be generated whenever underflow of timer 0 occurs.

G1ICR: x'00FC42'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	TML LV2	TML LV1	TML LV0	TM3 IE	TM2 IE	TM1 IE	TM0 IE	TM3 IR	TM2 IR	TM1 IR	TM0 IR	TM3 ID	TM2 ID	TM1 ID	TM0 ID
—	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0

- (4) The frequency divider factor for the timer is set. Since the TM0IO pin divides by 4, the timer 0 base register (TM0BR) is set to '3' (values in the range 1~255 can be set).

TM0BR: x'00FE10'

7	6	5	4	3	2	1	0
TM0 BR7	TM0 BR6	TM0 BR5	TM0 BR4	TM0 BR3	TM0 BR2	TM0 BR1	TM0 BR0
0	0	0	0	0	0	1	1

- (5) TM0LD and TM0EN of TM0MD are set to '1' and '0' respectively (the value of TM0BR is read into TM0BC). At the same time, the clock source is selected (TM0S is set to '00').
- (6) TM0LD and TM0EN are both set to '0'. If these settings are not made, the binary counter may not be counted during the first count and will be unstable.
- (7) TM0LD is set to '0' and TM0EN is set to '1'. The operation of the timer begins. The counter begins operation at the start of the cycle following the setting cycle.

If the binary counter (TM0BC) reaches '0', and if the value of the base register (TM0BR) read at the next count is '3', then timer 0 underflow (interrupt request) will occur.



If the clock source selection is changed at the same time as the count operation control, the value the binary counter will be corrupted.

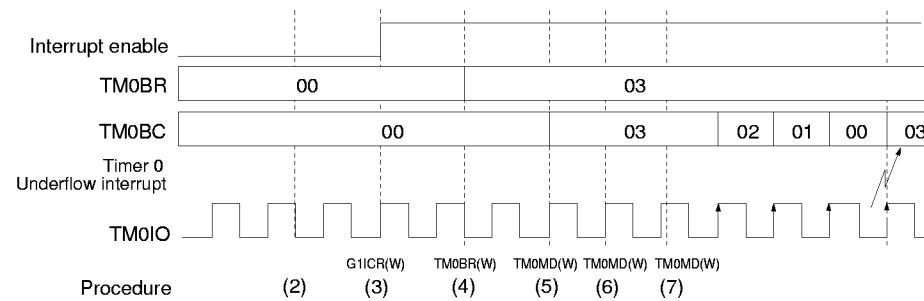


Figure 4-2-1 Event Counter Timing Chart

4-2-2 8-bit Timer as Clock Output

Timers 0~9 contain a clock output function and share the same setting procedure. In this example, timer 1 and prescaler 0 are used for a 12-cycle (SYSCLK divided by 6) clock output.

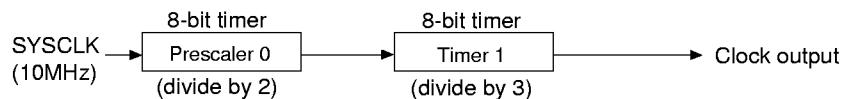


Figure 4-2-2 Example Clock Output Configuration (1)

■ Prescaler 0 Setting

Verification is not necessary immediately after a reset.

- (1) The prescaler 0 mode register (PS0MD) verifies that the counting operation has stopped.

PS0MD: x'00FE2A'

7	6	5	4	3	2	1	0
PS0	PS0	—	—	—	—	—	—
EN	LD	0	0	—	—	—	—

If the frequency divider factor is '1', a dummy value (x'0F' for example) is written once.

- (2) The frequency divider factor for the prescaler is set. Since the SYSCLK will be divided by 2, the prescaler 0 base register (PS0BR) is set to '1' (values in the range 1~255 can be set).

PS0BR: x'00FE1A'

7	6	5	4	3	2	1	0
PS0							
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0

- (3) PS0LD is set to '1' and PS0EN is set to '0' (the value of PS0BR is read into PS0BC).

PS0MD: x'00FE2A'

7	6	5	4	3	2	1	0
PS0	PS0	—	—	—	—	—	—
EN	LD	0	0	—	—	—	—

- (4) PSOLD and PS0EN are both set to '0'. If these settings are not made, the binary counter may not be counted during the first count and will be unstable.
 - (5) PS0LD is set to '0' and PS0EN is set to '1'. The operation of the prescaler begins. The counter begins operation at the start of the cycle following the setting cycle. If the prescaler 0 binary counter (PS0BC) reaches '0', and if the value of the base register (PS0BR) read at the next count is '1', then prescaler 0 underflow will occur.

■ Pin Settings

- (6) The timer output control register (TMDIR) sets the TM1IO pin for output (a value of '2' is set).

TMDIR: x'00FFB2'

■ Timer 1 Settings

- (7) The timer 1 mode register (TM1MD) verifies that the count operation has stopped.

If the frequency divider factor is '1', after procedure (5), the prescaler 0 base register (*PS0BR*) is reset with a prescaler frequency divider value of '0'. The first count uses the value settings of procedure (2). However, for the second count on, frequency division by '1' is used. If '0' is set in procedure (2), the first count will divide the frequency by 257. From the second count on, division will be by '1'.

Since the port control register sets the pins of timers 5~9, refer to "Chapter 9, Port Functions".

Verification is not necessary immediately after reset.

TM1MD: x'00FE21'

7	6	5	4	3	2	1	0
TM1 EN	TM1 LD	—	—	—	—	TM1 S1	TM1 S0
0	0					1	0

- (8) The frequency divider factor for the timer is set. Since the prescaler output will be divided by 3, the timer 1 base register (TM1BR) is set to '2' (values in the range 1~255 can be set).

TM1BR: x'00FE11'

- (9) TM1LD is set to '1' and TM1EN is set to '0' (the value of TM1BR is read into TM1BC). At the same time, the clock source is selected.

If the clock source selection is changed at the same time as the count operation control, the value the binary counter will be corrupted.

(10) TM1LD and TM1EN are both set to '0'. If these settings are not made, the binary counter may not be counted during the first count and will be unstable.

(11) TM1LD is set to '0' and TM1EN is set to '1'. The operation of the timer begins. Counting will start at the beginning of the cycle that follows the setting cycle.

If the binary counter (TM1BC) reaches '0', and if the value of the base register (TM1BR) read at the next count is '2', the TM1IO output will be inverted. '0' is output immediately after starting. If the binary counter reaches '0', output is inverted to '1' at the beginning of the next count. Then if the binary counter reaches '0', output is inverted to '0' at the beginning of the next count. This operation is repeated to realize a 12-cycle clock output.

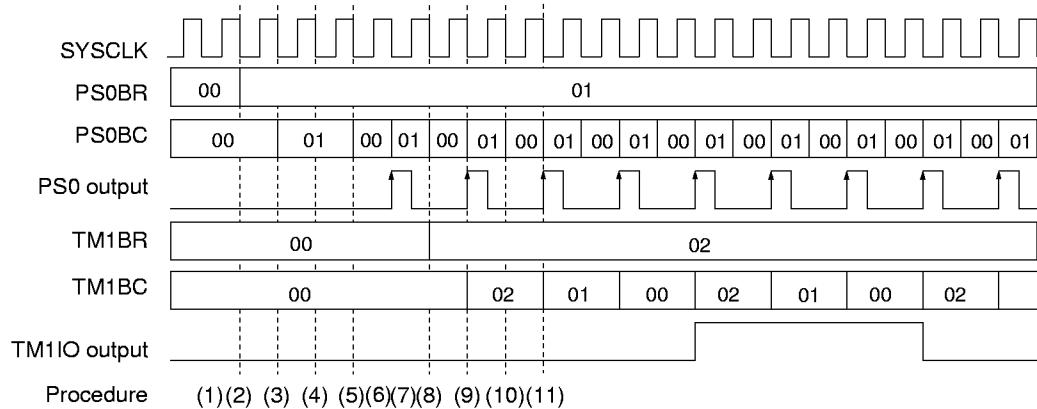


Figure 4-2-3 Clock Output Timing Chart

4-2-3 8-bit Timer as an Interval Timer

The interval timer setting procedure is the same for timers 0~9. Here, timer 2, timer 3 and prescaler 0 are used to generate interrupts at fixed timer intervals (1 sec). (To divide SYSCLK by 10,000,000, the prescaler, timer 2, timer 3 divide by 250, 200, and 200 respectively.)

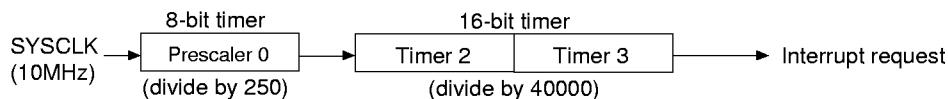


Figure 4-2-4 Example Clock Output Configuration (2)

- (1) The interrupt enable flag (IE) of the processor status word (PSW) is set to '1'.
- (2) Interrupts are enabled, and at the same time, all prior interrupt requests are cleared. In other words, in maskable interrupt control register (group) 1 (G1ICR), the interrupt level (6~0) is set in TM1LV2~0, TM3IR is set to '0' and TM3IE to '1'. For example, x'4800' is written to G1ICR. Thereafter, an interrupt will be generated whenever underflow of timer 3 occurs.

G1ICR: x'00FC42'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	TML LV2	TML LV1	TML LV0	TM3	TM2	TM1	TM0	TM3	TM2	TM1	TM0	TM3	TM2	TM1	TM0
—	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0

■ Prescaler 0 Setting

- (3) The prescaler 0 mode register (PS0MD) verifies that the count operation is stopped.

Verification is not necessary immediately after reset.

PS0MD: x'00FE2A'

7	6	5	4	3	2	1	0
PS0 EN	PS0 LD	—	—	—	—	—	—
0	0						

- (4) The frequency divider factor for the prescaler is set. Since the SYSCLK will be divided by 250, the prescaler 0 base register (PS0BR) is set to '249' (values in the range 1~255 can be set).

If the frequency divider factor is '1', a dummy value (x'0F' for example) is written once.

PS0BR: x'00FE1A'

7	6	5	4	3	2	1	0
PS0 BR7	PS0 BR6	PS0 BR5	PS0 BR4	PS0 BR3	PS0 BR2	PS0 BR1	PS0 BR0
1	1	1	1	1	0	0	1

- (5) PS0LD is set to '1' and PS0EN is set to '0' (the value of PS0BR is read into PS0BC).

PS0MD: x'00FE2A'

7	6	5	4	3	2	1	0
PS0 EN	PS0 LD	—	—	—	—	—	—
0	1	—	—	—	—	—	—



If the frequency divider factor is '1', after procedure (7), the prescaler 0 base register (PS0BR) is reset with a prescaler frequency divider value of '0'. The first count uses the value settings of procedure (4). However, for the second count on, frequency division by '1' is used. If '0' is set in procedure (4), the first count will divide the frequency by 257. From the second count on, division will be by '1'.

Verification is not necessary immediately after reset.

- (6) PS0LD and PS0EN are both set to '0'. If these settings are not made, the binary counter may not be counted during the first count and will be unstable.

- (7) PS0LD is set to '0' and PS0EN is set to '1'. The operation of the prescaler begins. The counter begins operation at the start of the cycle following the setting cycle. If the prescaler 0 binary counter (PS0BC) reaches '0', and if the value of the base register (PS0BR) read at the next count is '249', then prescaler 0 underflow will occur.

■ Settings for Timers 2 and 3

- (8) The timer 2 mode register (TM2MD) and timer 3 mode register (TM3MD) verify that the count operation has stopped.

TM2MD: x'00FE22'

7	6	5	4	3	2	1	0
TM2 EN	TM2 LD	—	—	—	—	TM2 S1	TM2 S0
0	0	—	—	—	—	1	0

TM3MD: x'00FE23'

7	6	5	4	3	2	1	0
TM3 EN	TM3 LD	—	—	—	—	TM3 S1	TM3 S0
0	0	—	—	—	—	0	1

- (9) The frequency divider factor for the timer is set. Since the frequency divider factor is 40000 (x'9C40), the timer 2 base register (TM2BR) is set to x'3F' and the timer 3 base register (TM3BR) is set to x'9C'. (Values in the range 1~255 can be set).

TM2BR: x'00FE12'

7	6	5	4	3	2	1	0
TM2 BR7	TM2 BR6	TM2 BR5	TM2 BR4	TM2 BR3	TM2 BR2	TM2 BR1	TM2 BR0
0	0	1	1	1	1	1	1

TM3BR: x'00FE13'

7	6	5	4	3	2	1	0
TM3 BR7	TM3 BR6	TM3 BR5	TM3 BR4	TM3 BR3	TM3 BR2	TM3 BR1	TM3 BR0
1	0	0	1	1	1	0	0

If the clock source selection is changed at the same time as the count operation control, the value the binary counter will be corrupted.

- (10) TM2LD and TM3LD are set to '1'. TM2EN and TM3EN are set to '0'. (The value of TM2BR is read into TM2BC and the value of TM3BR is read into TM3BC). At the same time, the clock source (prescaler 0 for timer 2, timer 2 cascade for timer 3) is selected.

(11) TM2LD and TM3LD are both set to '0'. TM2EN and TM3EN are both set to '0'. If these settings are not made, the binary counter may not be counted during the first count and will be unstable.

(12) TM2LD and TM3LD are both set to '0'. TM2EN and TM3EN are both set to '1'. The operation of the timer begins. Counting will start at the beginning of the cycle that follows the setting cycle.

If the timer 2 binary counter (TM2BC) and the timer 3 binary counter (TM3BC) reach '0', and if the value of the timer 2 base register (TM2BR) and the timer 3 base register (TM3BR) read at the next count are x'3F' and x'9C' respectively, timer 3 underflow (interrupt request) will occur.

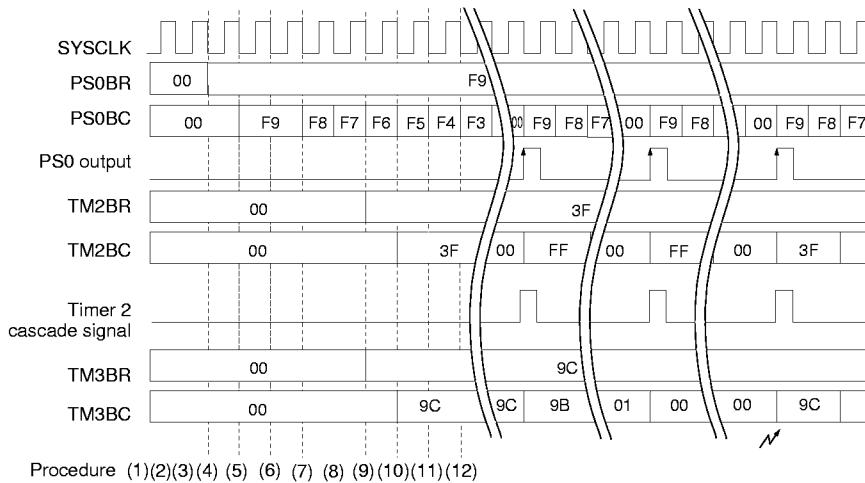


Figure 4-2-5 Interval Timer Timing Chart

4-3 Examples of 16-bit Timer Settings

4-3-1 16-bit Timer as an Event Counter

With the exception of up/down counter selection, the event counter setting procedure is the same for timers 10~12. In this example, timer 10 is used to count the input (at a frequency 1/2 or less of the SYSCLK, 5MHz or below for 20MHz oscillation) at the TM10IOB pin, and generate an interrupt every 2nd and 5th cycle.

■ Interrupt Enable Settings



Data settings use the MOV instruction and must be written as 16 bits.

*TM10BC counting is stopped.
TM10BC and RS.F.F. are initialized (cleared to '0').*

- (1) Interrupts are enabled, and at this time, all prior interrupt requests are cleared. In other words, in G4ICR, the interrupt level (6~0) is set in TM10LV2~0, TM10AIR and TM10BIR are set to '0', and TM10AIE and TM10BIE are set to '1'. For example, G4ICR is set to x'4600'. Thereafter, an interrupt will be generated whenever capture A and capture B of timer 10 occur.

■ Timer 10 Settings

- (2) The timer 10 mode register (TM10MD) is set to the operation mode. It is verified that counting has stopped and that interrupts are disabled. Either up or down operation is selected. TM10IOB is selected as the clock source.

TM10MD: x'00FE30'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 EN	TM10 NLD	—	—	TM10 UD1	TM10 UDO	TM10 TGE	TM10 ONE	TM10 MD1	TM10 MD0	TM10 ECLR	TM10 LP	TM10 ASEL	TM10 S2	TM10 S1	TM10 S0
0	0	—	—	0	0	0	0	0	0	0	1	0	0	1	0

- (3) The frequency divider factor for timer 10 is set. Since the TM10IOB pin input will be divided by 5, the timer 10 compare/capture register A (TM10CA) is set to '4'. (Values in the range 1~x'FFFE' can be set.)

TM10CA: x'00FE34'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 CA15	TM10 CA14	TM10 CA13	TM10 CA12	TM10 CA11	TM10 CA10	TM10 CA9	TM10 CA8	TM10 CA7	TM10 CA6	TM10 CA5	TM10 CA4	TM10 CA3	TM10 CA2	TM10 CA1	TM10 CA0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

- (4) The phase difference for timer 10 is set. For 2 cycles, the timer 10 compare/capture register B (TM10CB) is set to '1'. (Values in the range of $-1 \leq TM10CB < TM10CA$ may be set.)

In the single buffer mode, comparison is made to TM10CA and TM10CB. -1 is x'FFFF. Set the TM10CB to -1 if it is not used.

TM10CB: x'00FE38'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 CB15	TM10 CB14	TM10 CB13	TM10 CB12	TM10 CB11	TM10 CB10	TM10 CB9	TM10 CB8	TM10 CB7	TM10 CB6	TM10 CB5	TM10 CB4	TM10 CB3	TM10 CB2	TM10 CB1	TM10 CB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

- (5) TM10NLD and TM10EN of the mode register are set to '1' and '0' respectively. TM10BC, T.F.F., and RS.F.F. are in operating states.

- (6) TM10NLD and TM10EN are both set to '1'. Timer 10 operation is started. Counting starts at the beginning of the cycle that follows the setting cycle.

If these settings are not made, the binary counter may not be counted during the first count and will be unstable. Other operating modes are not to be altered.

When SYSCLK is operating (normal and halt modes), external inputs at TM10IOB are sampled at the SYSCLK. If the SYSCLK is stopped (stop mode), the TM10IOB input causes timer 10 to count. The clock for the event counter is 1/4 of the clock source or less (5MHz or below for 20MHz oscillation).

The timing chart below shows an example of interrupts being generated by counting-up.

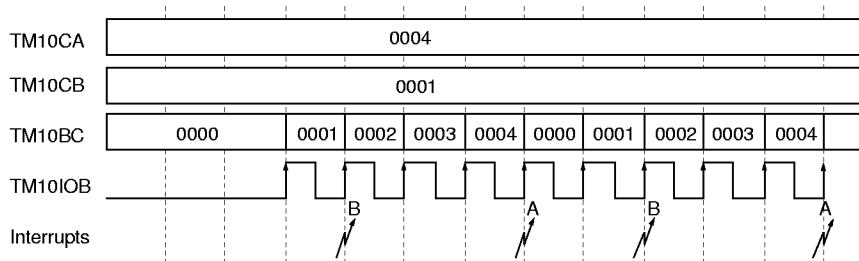


Figure 4-3-1 Event Counter Timing Chart

4-3-2 PWM Output from a 16-bit Timer

With the exception of up/down counter selection, the PWM output setting procedure is the same for timers 10~12. In this example, timer 10 divides SYSCLK by 5, and after 5 cycles, outputs PWM with a duty of 2:3 cycles. Therefore, compare/capture register A is set to divide by 5 (value of 4 is set) and compare/capture register B is set to 2 cycles (value of 1 is set).

■ Pin Settings

- (1) The timer I/O control register (TMDIR) sets the TM10IOA pin for output (the value '0100' is set).

TMDIR: x'00FFB2'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	TM12 BO	TM12 AO	TM11 BO	TM11 AO	TM10 BO	TM10 AO	—	—	—	TM4O	TM3O	TM2O	TM1O	TM0O

0 0 0 0 0 0 0 1 — — — 0 0 0 0 0

■ Timer 10 Settings

- (2) The timer 10 mode register (TM10MD) is set to the operation mode. It is verified that counting has stopped and that interrupts are disabled. Either up or down operation is selected. SYSCLK is selected as the clock source. Here, the double operation mode is selected.

TM10MD: x'00FE30'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 EN	TM10 NLD	—	—	TM10 UD1	TM10 UD0	TM10 TGE	TM10 ONE	TM10 MD1	TM10 MD0	TM10 ECLR	TM10 LP	TM10 ASEL	TM10 S2	TM10 S1	TM10 S0

0 0 — — 0 0 0 0 0 0 1 0 1 0 0 1 1

- (3) The frequency divider factor for timer 10 is set. Since SYSCLK will be divided by 5, the timer 10 compare/capture register A (TM10CA) is set to '4'. (Values in the range 1~x'FFFF' can be set.)

TM10CA: x'00FE34'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 CA15	TM10 CA14	TM10 CA13	TM10 CA12	TM10 CA11	TM10 CA10	TM10 CA9	TM10 CA8	TM10 CA7	TM10 CA6	TM10 CA5	TM10 CA4	TM10 CA3	TM10 CA2	TM10 CA1	TM10 CA0

0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0



Data settings use the MOV instruction and must be written as 16 bits.

*TM10BC counting is stopped.
TM10BC and RS.F.F. are initialized (cleared to '0').*

- (4) The duty cycle for timer 10 is set. Since the duty is 2/5 of the SYSCLK, the timer 10 compare/capture register B (TM10CB) is set to '1'. (Values in the range of $-1 \leq TM10CB < TM10CA$ may be set.)

-1 is x'FFFF'. Set the TM10CB to -1 if it is not used.

TM10CB: x'00FE38'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 CB15	TM10 CB14	TM10 CB13	TM10 CB12	TM10 CB11	TM10 CB10	TM10 CB9	TM10 CB8	TM10 CB7	TM10 CB6	TM10 CB5	TM10 CB4	TM10 CB3	TM10 CB2	TM10 CB1	TM10 CB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

- (5) TM10CAX is compared during the double buffer mode. However, since TM6CAX will be modified when TM10CAX=TM10BC, it is reset to x'0000' before operation. Therefore, in order for the contents of TM10CA to be read into TM10CAX, dummy data is written to TM10CAX. (The value of the dummy data does not matter).

TM10CAX and TM10CBX are only valid when the compare registers are set to double buffer.

TM10CAX: x'00FE36'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 CAX15	TM10 CAX14	TM10 CAX13	TM10 CAX12	TM10 CAX11	TM10 CAX10	TM10 CAX9	TM10 CAX8	TM10 CAX7	TM10 CAX6	TM10 CAX5	TM10 CAX4	TM10 CAX3	TM10 CAX2	TM10 CAX1	TM10 CAX0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- (6) TM10CBX is compared during the double buffer mode. However, since TM6CBX will be modified when TM10CBX=TM10BC, it is reset to x'0000' before operation. Therefore, in order for the contents of TM10CA to be read into TM10CBX, dummy data is written to TM10CBX. (The value of the dummy data does not matter).

TM10CBX: x'00FE3A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 CBX15	TM10 CBX14	TM10 CBX13	TM10 CBX12	TM10 CBX11	TM10 CBX10	TM10 CBX9	TM10 CBX8	TM10 CBX7	TM10 CBX6	TM10 CBX5	TM10 CBX4	TM10 CBX3	TM10 CBX2	TM10 CBX1	TM10 CBX0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Settings that follow are the same as (5) and (6) of section 4-3-1 "16-bit Timer as an Event Counter".

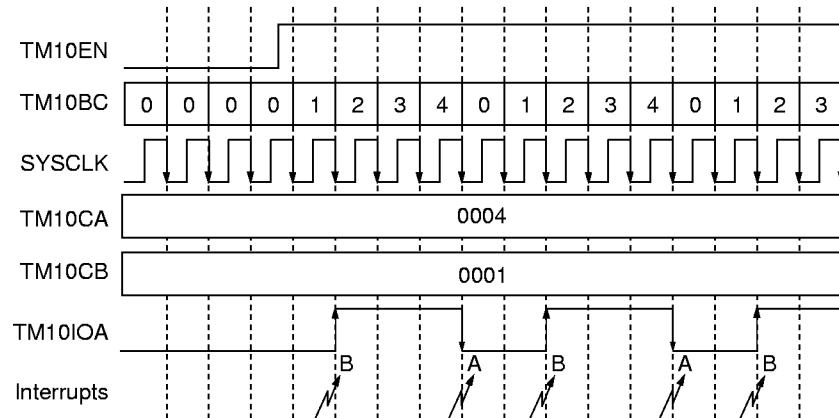


Figure 4-3-2 PWM Timing Chart

When the duty of the output PWM waveform is dynamically changed, in single buffer mode, there may be glitches in the synchronized output waveform or interrupts caused by timing that changes the value of TMnCB. In the double buffer mode, with an arbitrary timing, even if the value of TMnCB is changed, there will be no glitches in the output waveform or interrupts. The output waveform will be maintained even if it is consecutive 1's or 0's.

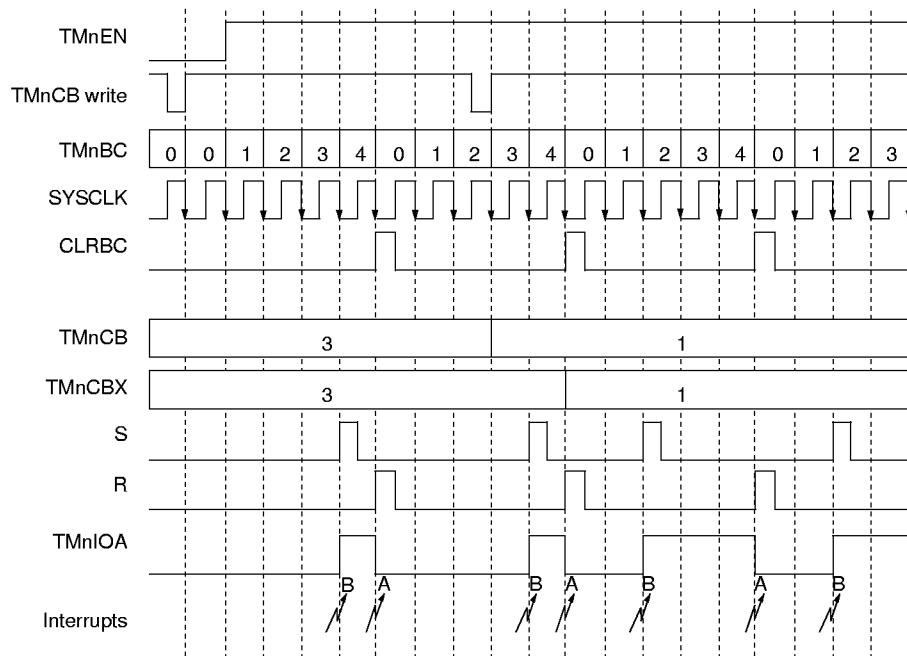


Figure 4-3-3 PWM Double Buffer Mode Timing Chart

4-3-3 Two-phase Clock Output from a 16-bit Timer

With the exception of up/down counter selection, the 2-phase clock output setting procedure is the same for timers 10~12. In this example, timer 10 divides the output of prescaler 0 (SYSCLK divided by 2) by 5, and after 5 cycles, outputs 2-phase clock with a phase difference of 2 cycles. Therefore, compare/capture register A is set to divide by 5 (value of 4 is set) and compare/capture register B is set to 2 cycles (value of 1 is set).

■ Pin Settings

- (1) The timer I/O control register (TMDIR) sets the TM10IOA pin and the TM10IOB pin for output (the value '0100' is set).

Verification is not necessary immediately after reset.

TMDIR: x'00FFB2'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	TM12 BO	TM12 AO	TM11 BO	TM11 AO	TM10 BO	TM10 AO	—	—	—	TM4O	TM3O	TM2O	TM1O	TM0O

0 0 0 0 0 1 1 0 0 0 0 0 0 0 0

■ Prescaler 0 Settings

- (2) The prescaler 0 mode register (PS0MD) verifies that counting has stopped.

PS0MD: x'00FE2A'

7	6	5	4	3	2	1	0
PS0 EN	PS0 LD	—	—	—	—	—	—

0 0 — — — — — —

- (3) The frequency divider factor for the prescaler is set. Since the SYSCLK will be divided by 2, the prescaler 0 base register (PS0BR) is set to '1' (values in the range 1~255 can be set).

If the frequency divider factor is '1', a dummy value (x'0F' for example) is written once.

PS0BR: x'00FE1A'

7	6	5	4	3	2	1	0
PS0 BR7	PS0 BR6	PS0 BR5	PS0 BR4	PS0 BR3	PS0 BR2	PS0 BR1	PS0 BR0

0 0 0 0 0 0 0 1

- (4) PS0LD is set to '1' and PS0EN is set to '0' (the value of PS0BR is read into PS0BC).

PS0MD: x'00FE2A'

7	6	5	4	3	2	1	0
PS0 EN	PS0 LD	—	—	—	—	—	—

0 1

If the frequency divider factor is '1', after procedure (6), the prescaler 0 base register (PS0BR) is reset with a prescaler frequency divider value of '0'. The first count uses the value settings of procedure (3). However, for the second count on, frequency division by '1' is used. If '0' is set in procedure (3), the first count will divide the frequency by 257. From the second count on, division will be by '1'.



Data settings use the MOV instruction and must be written as 16 bits.

TM10BC counting is stopped.
TM10BC and RS.F.F. are initialized (cleared to '0').

- (5) PSOLD and PSOEN are both set to '0'. If these settings are not made, the binary counter may not be counted during the first count and will be unstable.

- (6) PSOLD is set to '0' and PSOEN is set to '1'. The operation of the prescaler begins. The counter begins operation at the start of the cycle following the setting cycle. If the prescaler 0 binary counter (PS0BC) reaches '0', and if the value of the base register (PS0BR) read at the next count is '1', then prescaler 0 underflow will occur.

■ Timer 10 Settings

- (7) The timer 10 mode register (TM10MD) is set to the operation mode. It is verified that counting has stopped and that interrupts are disabled. Either up or down operation is selected. Prescaler 0 is selected as the clock source. Here, the double buffer operation mode is selected.

TM10MD: x'00FE30'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 EN	TM10 NLD	—	—	TM10 UD1	TM10 UD0	TM10 TGE	TM10 ONE	TM10 MD1	TM10 MD0	TM10 ECLR	TM10 LP	TM10 ASEL	TM10 S2	TM10 S1	TM10 S0
0	0	—	—	0	0	0	0	0	1	0	1	0	0	1	1

- (8) The frequency divider factor for timer 10 is set. Since prescaler 0 will be divided by 5, the timer 10 compare/capture register A (TM10CA) is set to '4'. (Values in the range 1~x'FFFE' can be set.)

TM10CA: x'00FE34'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 CA15	TM10 CA14	TM10 CA13	TM10 CA12	TM10 CA11	TM10 CA10	TM10 CA9	TM10 CA8	TM10 CA7	TM10 CA6	TM10 CA5	TM10 CA4	TM10 CA3	TM10 CA2	TM10 CA1	TM10 CA0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

- (9) The phase difference for timer 10 is set. For 2 cycles of prescaler 0, the timer 10 compare/capture register B (TM10CB) is set to '1'. (Values in the range of -1<TM10CB<TM10CA may be set.)

TM10CB: x'00FE38'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 CB15	TM10 CB14	TM10 CB13	TM10 CB12	TM10 CB11	TM10 CB10	TM10 CB9	TM10 CB8	TM10 CB7	TM10 CB6	TM10 CB5	TM10 CB4	TM10 CB3	TM10 CB2	TM10 CB1	TM10 CB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

- (10) TM10CAX is compared during the double buffer mode. However, since TM10CAX will be modified when TM10CAX=TM10BC, it is reset to x'0000' before operation. Therefore, in order for the contents of TM10CA to be read into TM10CAX, dummy data is written to TM10CAX. (The value of the dummy data does not matter).

TM10CAX and TM10CBX are only valid when the compare registers are set to double buffer.

TM10CAX: x'00FE36'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 CAX15	TM10 CAX14	TM10 CAX13	TM10 CAX12	TM10 CAX11	TM10 CAX10	TM10 CAX9	TM10 CAX8	TM10 CAX7	TM10 CAX6	TM10 CAX5	TM10 CAX4	TM10 CAX3	TM10 CAX2	TM10 CAX1	TM10 CAX0

- (11) TM10CBX is compared during the double buffer mode. However, since TM10CBX will be modified when TM10CBX=TM10BC, it is reset to x'0000' before operation. Therefore, in order for the contents of TM10CB to be read into TM10CBX, dummy data is written to TM10CBX. (The value of the dummy data does not matter).

TM10CBX: x'00FE3A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 CBX15	TM10 CBX14	TM10 CBX13	TM10 CBX12	TM10 CBX11	TM10 CBX10	TM10 CBX9	TM10 CBX8	TM10 CBX7	TM10 CBX6	TM10 CBX5	TM10 CBX4	TM10 CBX3	TM10 CBX2	TM10 CBX1	TM10 CBX0

Settings that follow are the same as (5) and (6) of section 4-3-1 "16-bit Timer as an Event Counter".

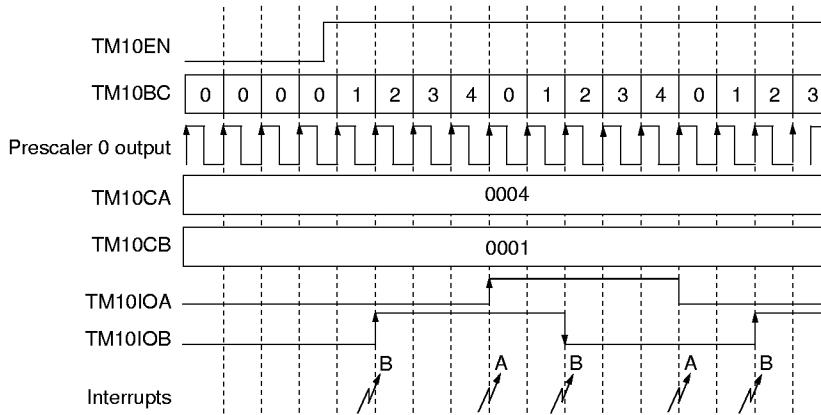


Figure 4-3-4 Two-phase Clock Timing Chart

Clock waveform is dynamically changed, in single buffer mode, there may be glitches in the synchronized output waveform or interrupts caused by timing that changes the value of TMnCB. In the double buffer mode, with an arbitrary timing, even if the value of TMnCB is changed, there will be no glitches in the output waveform or interrupts. The output waveform will be maintained even if it is consecutive 1's or 0's.

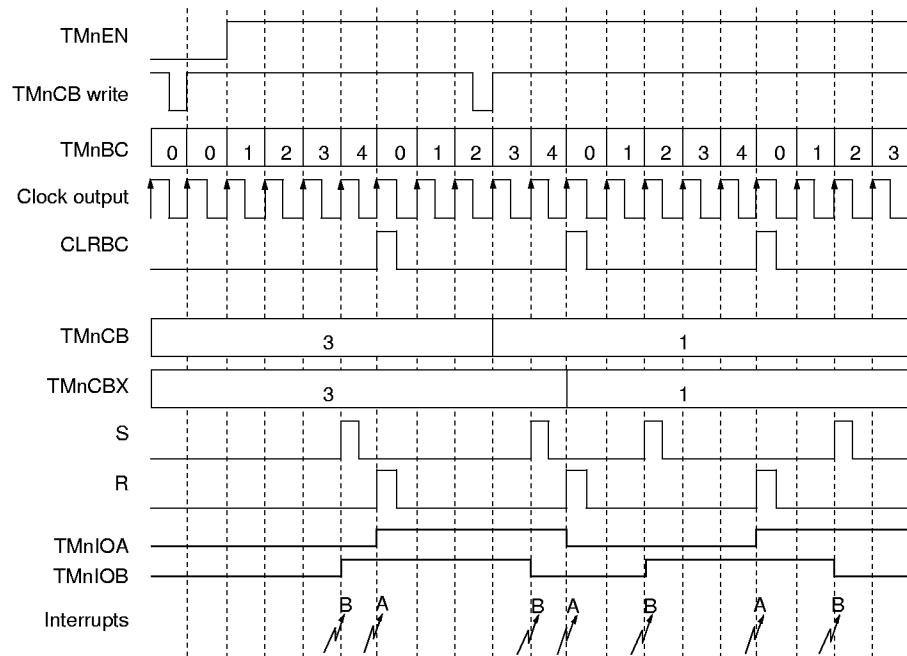


Figure 4-3-5 Two-phase Double Buffer Mode Timing Chart

4-3-4 Single-phase Capture Input with a 16-bit Timer

With the exception of up/down counter selection, the single-phase capture input setting procedure is the same for timers 10~12. In this example, timer 11 is used to divide the SYSCLK by 65536, and to measure the width of the interval between 1's input to the TM11IOA pin. Capture B causes an interrupt to be generated and the width (TMnCB-TMnCA) is computed by the software.



Data settings use the MOV instruction and must be written as 16 bits.

*TM11BC counting is stopped.
TM11BC and RS.F.F. are initialized (cleared to '0').*

■ Interrupt Enable Settings

- (1) Interrupts are enabled, and at this time, all prior interrupt requests are cleared. In other words, in G5ICR, the interrupt level (6~0) is set in TM11LV2~0, TM11BIR is set to '0', and TM11BIE is set to '1'. For example, G5ICR is set to x'4400'. Thereafter, an interrupt will be generated whenever capture B of timer 11 occurs.

■ Timer 11 Settings

- (2) The timer 11 mode register (TM11MD) is set to the operation mode. It is verified that counting has stopped and that interrupts are disabled. Either up or down operation is selected. TM11LP is set to '0' and counting is repeated from 0~x'FFFF'. SYSCLK is selected as the clock source.

TM11MD: x'00FE40'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 EN	TM11 NLD	—	—	TM11 UD1	TM11 UD0	TM11 TGE	TM11 ONE	TM11 MD1	TM11 MD0	TM11 ECLR	TM11 LP	TM11 ASEL	TM11 S2	TM11 S1	TM11 S0
0	0	—	—	0	0	0	0	1	0	0	0	0	0	1	1

If these settings are not made, the binary counter may not be counted during the first count and will be unstable.

- (3) TM11NLD is set to '1' and TM11EN is set to '0'. TM11BC and RS.F.F. are in operating states. Other operating modes are not to be altered.
- (4) TM11NLD and TM11EN are both set to '1'. Timer 11 begins operation. Counting starts at the beginning of the cycle that follows the setting cycle.

■ Compare/Capture Register Settings

- (5) When TM11MD='10' (during capture), TM11CA and TM11CB are read-only.

If it is necessary to set TM11CA and TM11CB, they are set after TM11MD is made equal to '00'.

TM11CA: x'00FE44'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 CA15	TM11 CA14	TM11 CA13	TM11 CA12	TM11 CA11	TM11 CA10	TM11 CA9	TM11 CA8	TM11 CA7	TM11 CA6	TM11 CA5	TM11 CA4	TM11 CA3	TM11 CA2	TM11 CA1	TM11 CA0

TM11CB: x'00FE48'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 CB15	TM11 CB14	TM11 CB13	TM11 CB12	TM11 CB11	TM11 CB10	TM11 CB9	TM11 CB8	TM11 CB7	TM11 CB6	TM11 CB5	TM11 CB4	TM11 CB3	TM11 CB2	TM11 CB1	TM11 CB0



In single-phase capture, TM11CA is captured at the falling edge of TM11IOA, and TM11CB is captured at the falling edge of TM11IOA.

■ Interrupt Processing and width Computation

- (6) The interrupt processing is performed. The interrupt processing determines the group, specifies the cause, and clears IRFn.

- (7) Width computation is performed. The values of TM11CA and TM11CB are stored in data registers and the subtraction of TM11CB-TM11CA is computed. The C and V flags are ignored. With TM11LP=0, the width can be properly measured even when the value of TMCA is larger than that of TMCB. In the example below, detection is after 3 cycles (000A-0007=0003).

The values of TM11CA and TM11CB are read during interrupt processing.

Even if the value of TMCA is large, the width can be obtained by ignoring the flags.

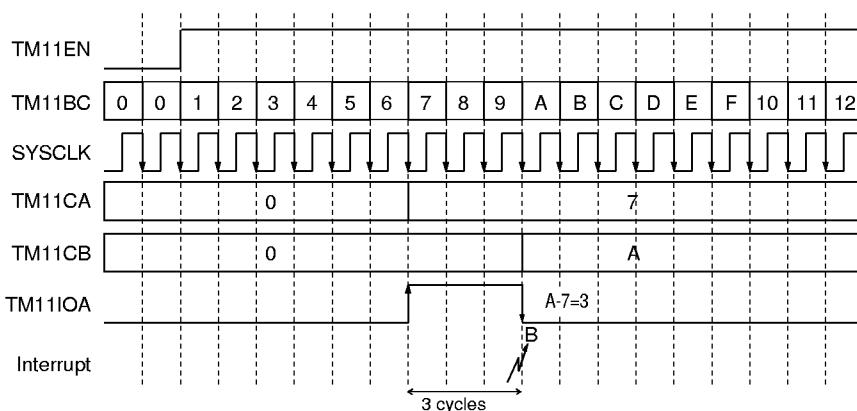


Figure 4-3-6 Single-phase Capture Timing Chart

4-3-5 Two-phase Capture Input with a 16-bit Timer

With the exception of up/down counter selection, the two-phase capture input setting procedure is the same for timers 10~12. In this example, prescaler 0 divides the SYSCLK by 2, then divides that signal by 65536, and measures the width from the rising edge of TM11IOA pin input to the rising edge of TM11IOB pin input. Capture B causes an interrupt to be generated and the width (TMnCB-TMnCA) is computed by the software.



Data settings use the MOV instruction and must be written as 16 bits.

*Verification is not necessary immediately after reset.
If the frequency divider factor is '1', a dummy value (x'0F' for example) is written once.*

If these settings are not made, the PS0BC may not be counted during the first count and will be unstable.

If the frequency divider factor is '1', the prescaler 0 base register (PS0BR) is reset with a prescaler frequency divider value of '0'. The first count uses the value settings of procedure (2). However, for the second count on, frequency division by '1' is used. If '0' is set in procedure (2), the first count will divide the frequency by 257. From the second count on, division will be by '1'.

■ Interrupt Enable Settings

- (1) Interrupts are enabled. At this time, all prior interrupt requests are cleared. In other words, in G5ICR, the interrupt level (6~0) is set in TM11LV2~0, TM11BIR is set to '0', and TM11BIE is set to '1'. For example, G5ICR is set to x'4400'. Thereafter, an interrupt will be generated whenever capture B of timer 11 occurs.

■ Prescaler 0 Settings (Set to divide SYSCLK frequency by 2)

- (2) The prescaler 0 mode register (PS0MD) verifies that counting has stopped. The frequency divider factor for the prescaler is set. Since the SYSCLK is to be divided by 2, the prescaler 0 base register (PS0BR) is set to '1' (values in the range 0~255 can be set).
- (3) PS0LD is set to '1' and PS0EN is set to '0' (the value of PS0BR is read into PS0BC).

PS0MD: x'00FE2A'

7	6	5	4	3	2	1	0
PS0 EN	PS0 LD	—	—	—	—	—	—
0	1	—	—	—	—	—	—

- (4) PS0LD and PS0EN are both set to '0'.
- (5) PS0LD is set to '0' and PS0EN is set to '1'. The operation of the prescaler begins. The counter begins operation at the start of the cycle following the setting cycle. If the binary counter (PS0BC) reaches '0', and if the value of the base register (PS0BR) read at the next count is '1', then prescaler 0 underflow will occur.

■ Timer 11 Settings

- (6) The timer 11 mode register (TM11MD) is set to the operation mode. It is verified that counting has stopped and that interrupts are disabled. Either up or down operation is selected. TM11LP is set to '0' and counting is repeated from 0~xxFFFF'. Prescaler 0 is selected as the clock source.

TM11MD: x'00FE40'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 EN	TM11 NLD	—	—	TM11 UD1	TM11 UD0	TM11 TGE	TM11 ONE	TM11 MD1	TM11 MD0	TM11 ECLR	TM11 LP	TM11 ASEL	TM11 S2	TM11 S1	TM11 S0
0	0	—	—	0	0	0	0	1	1	0	0	0	0	0	0



Data settings use the MOV instruction and must be written as 16 bits.

*TM11BC counting is stopped.
TM11BC and RS.F.F. are initialized (cleared to '0').*



In two-phase capture, TM11CA is captured at the rising edge of TM11IOA, and TM11CB is captured at the rising edge of TM11IOB.

Settings that follow are the same as (3)~(7) of section 4-3-4 "Single-phase Capture Input with a 16-bit Timer". In the example below, detection is after 3 cycles (000A-0007=0003).

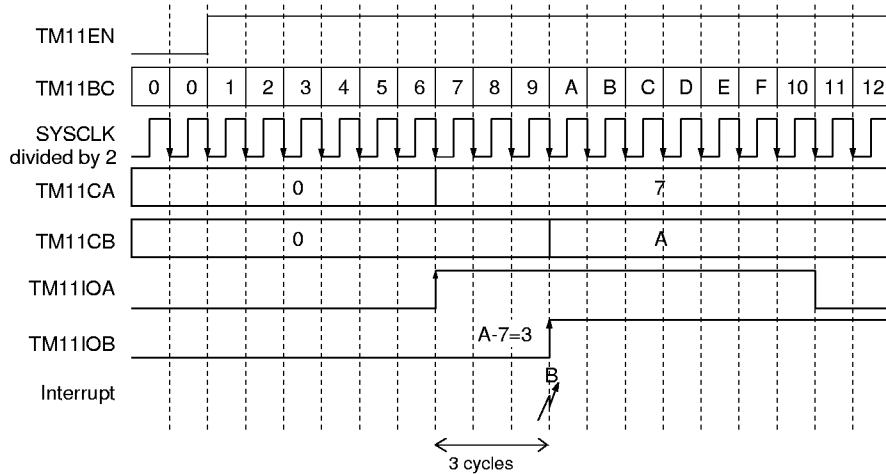


Figure 4-3-7 Two-phase Capture Timing Chart

4-3-6 Two-phase Encoder Input with a 16-bit Timer (multiply by 4)

The two-phase encoder input setting procedure is the same for timers 10 and 11. Here, with timer 11, a two-phase encoded (multiply by 4) signal is input and up/down counting is performed. Interrupts are generated when the counter reaches a previously set value.



Data settings use the MOV instruction and must be written as 16 bits.

*TM11BC counting is stopped.
TM11BC and RS.F.F. are initialized (cleared to '0').*

■ Interrupt Enable Settings

- (1) Interrupts are enabled. At this time, all prior interrupt requests are cleared. In other words, in G5ICR, the interrupt level (6~0) is set in TM11LV2~0, TM11BIR is set to '0', and TM11BIE is set to '1'. For example, G5ICR is set to x'4400'. Thereafter, an interrupt will be generated whenever capture B of timer 11 occurs.

■ Timer 11 Settings

- (2) The timer 11 mode register (TM11MD) is set to the operation mode. It is verified that counting has stopped and that interrupts are disabled. If counting is to be performed in a loop of value TM11CA, TM11LP is set to '1'. If counting is to be performed from 0~x'FFFF', TM11LP is set to '0'. The two-phase encoder (multiply by 4) is selected as the clock source.

TM11MD: x'00FE40'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 EN	TM11 NLD	—	—	TM11 UD1	TM11 UDO	TM11 TGE	TM11 ONE	TM11 MD1	TM11 MD0	TM11 ECLR	TM11 LP	TM11 ASEL	TM11 S2	TM11 S1	TM11 S0
0	0	—	—	0	0	0	0	0	0	0	1	0	1	0	0

- (3) If counting is to be performed in a loop of value TMCA, the timer 11 loop value is set (values from 1~x'FFFF' can be set). If x'1FFF' is set in TM11CA, counter TM11BC will count from 0~'1FFF'.

TM11CA: x'00FE44'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 CA15	TM11 CA14	TM11 CA13	TM11 CA12	TM11 CA11	TM11 CA10	TM11 CA9	TM11 CA8	TM11 CA7	TM11 CA6	TM11 CA5	TM11 CA4	TM11 CA3	TM11 CA2	TM11 CA1	TM11 CA0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

If the TM11CA value is reached by either up or down counting, a compare/capture A interrupt will be generated at the beginning of the next cycle.

(4) If an interrupt is to be generated at the value of TM11CB, the timer 11 interrupt value is set. (Values from 0~TM11CA can be set.) If this value is reached by either up or down counting, interrupt B will be generated at the beginning of the next cycle. If counting is to be performed from 0~x'FFFF', the timer 11 interrupt value is set (values from 0~x'FFFF' can be set).

(5) TM11NLD is set to '1' and TM11EN is set to '0'. TM11BC and RS.F.F. are in operating states. Other operating modes are not to be altered.

(6) TM11NLD and TM11EN are both set to '1'. Timer 11 begins operation. Counting starts at the beginning of the cycle that follows the setting cycle.

If these settings are not made, the binary counter may not be counted during the first count and will be unstable.

■ Interrupt Processing

(7) The interrupt processing is performed. The interrupt processing determines the group, specifies the cause, and clears IRFn.

The timing chart below shows count direction.

	Count-up				Count-down			
TM11IOA	↑	1	↓	0	↑	0	↓	1
TM11IOB	0	↑	1	↓	1	↑	0	↓

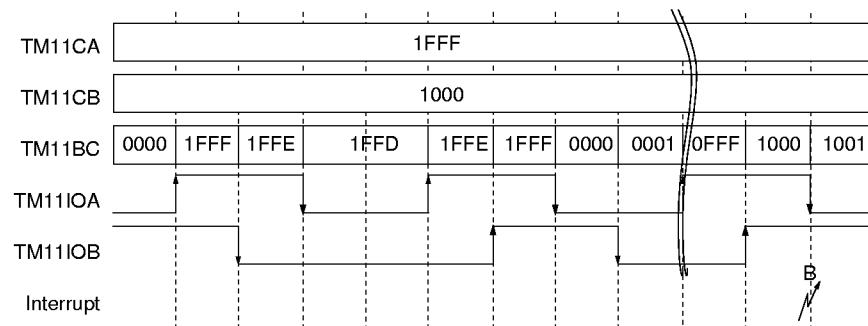


Figure 4-3-8 Two-phase Encoder Input Timing Chart

4-3-7 One-shot Pulse Output with a 16-bit Timer

The one-shot pulse output setting procedure is the same for timers 10~12. Here, with timer 11 is used to generate a one-shot pulse. The pulse width is set to 2 cycles of the SYSCLK.



Data settings use the MOV instruction and must be written as 16 bits.

*TM11BC counting is stopped.
TM11BC and RS.F.F. are initialized (cleared to '0').*

■ Timer 11 Settings

- (1) The timer 11 mode register (TM11MD) is set to the operation mode. It is verified that counting has stopped and that interrupts are disabled. The up/down counting is set to count-up. SYSCLK is selected as the clock source.

TM11MD: x'00FE40'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 EN	TM11 NLD	—	—	TM11 UD1	TM11 UD0	TM11 TGE	TM11 ONE	TM11 MD1	TM11 MD0	TM11 ECLR	TM11 LP	TM11 ASEL	TM11 S2	TM11 S1	TM11 S0
0	0	—	—	0	0	0	1	0	0	0	1	0	0	1	1

- (2) TM11CA is set to the pulse width of timer 11. (Values from 1~x'FFFF' can be set.) Since the pulse width is 2 cycles of SYSCLK, the value '3' is set. TM11BC counts from 0 to 3. During the interval from 2 to 3, '1' is output to TM11IOA.

TM11CA: x'00FE44'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 CA15	TM11 CA14	TM11 CA13	TM11 CA12	TM11 CA11	TM11 CA10	TM11 CA9	TM11 CA8	TM11 CA7	TM11 CA6	TM11 CA5	TM11 CA4	TM11 CA3	TM11 CA2	TM11 CA1	TM11 CA0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

- (3) TM11CB is set to '1'.

TM11CB: x'00FE48'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 CB15	TM11 CB14	TM11 CB13	TM11 CB12	TM11 CB11	TM11 CB10	TM11 CB9	TM11 CB8	TM11 CB7	TM11 CB6	TM11 CB5	TM11 CB4	TM11 CB3	TM11 CB2	TM11 CB1	TM11 CB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

- (4) TM11NLD is set to '1' and TM11EN is set to '0'. TM11BC and RS.F.F are in operating states.
- (5) At the rising edge of TM11IOB, TM11EN is set to '1' by the hardware. Therefore, counting starts at the beginning of the cycle after TM11IOB rises.

If TM11CB is set to '0', only the first one-shot pulse is output.

If these settings are not made, the binary counter may not be counted during the first count and will be unstable.

TM11EN can be used as a substitute for the one-shot busy flag.

A timing chart is shown below. TM11EN is set at the falling edge of TM11IOB. Counting begins at the next cycle. Before counting begins, TM11BC is 0, an initial value of 0 is output to TM11IOA, and the R (reset) and S (set) signals are not output. When counting begins, the count changes from '0' to '1' and the S signal is output. TM11IOA is set to '1' and a pulse is output. If the count reaches 3, TM11BC is reset from 3 to 0. At the same time, the R signal is output and TM11IOA outputs '0'. Since TM11ONE is set to '1', the TM11EN flag is also reset, and the count suspended. The status will be the same as that before the falling edge of TM11IOB. When the falling edge of TM11IOB is input again, TM11EN will be set, the same operation repeated, and a one-shot pulse output.

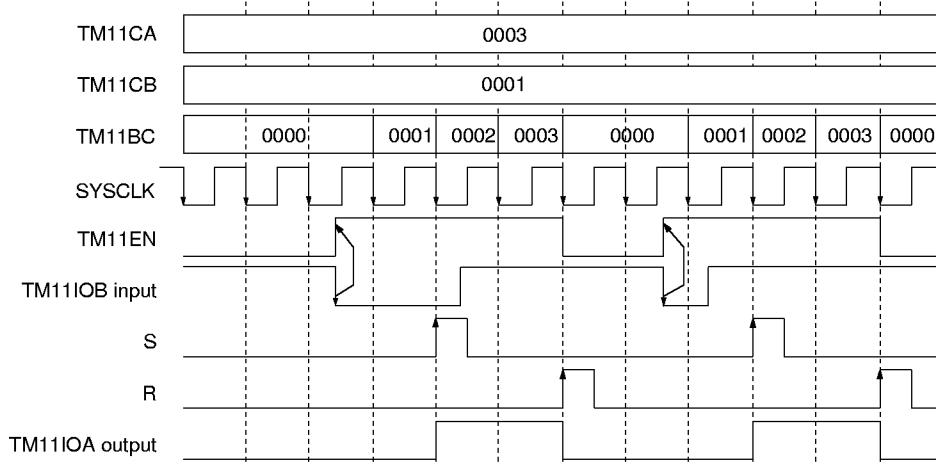


Figure 4-3-9 One-shot Pulse Output Timing Chart

4-3-8 External Count Direction Control with 16-bit Timer

The external count direction control setting procedure is the same for timers 10 and 11. Here, timer 11 counts SYSCLK. The count direction (up or down) is controlled by TM11IOA. An interrupt is generated when the counter reaches a previously set value.



Data settings use the MOV instruction and must be written as 16 bits.

*TM11BC counting is stopped.
TM11BC and RS.F.F. are initialized (cleared to '0').*

■ Interrupt Enable Settings

- (1) Interrupts are enabled, and at this time, all prior interrupt requests are cleared. In other words, in G5ICR, the interrupt level (6~0) is set in TM11LV2~0, TM11BIR is set to '0', and TM11BIE is set to '1'. For example, G5ICR is set to x'4400'. Thereafter, an interrupt will be generated whenever capture B of timer 11 occurs.

■ Timer 11 Settings

- (2) The timer 11 mode register (TM11MD) is set to the operation mode. It is verified that counting has stopped and that interrupts are disabled. The up/down operation is set such that when the TM11IOA pin is '1', up-counting is performed, and when '0', down-counting is performed. SYSCLK is selected as the clock source.

TM11MD: x'00FE40'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 EN	TM11 NLD	—	—	TM11 UD1	TM11 UD0	TM11 TGE	TM11 ONE	TM11 MD1	TM11 MD0	TM11 ECLR	TM11 LP	TM11 ASEL	TM11 S2	TM11 S1	TM11 S0
0	0	—	—	1	0	0	0	0	0	0	1	0	0	1	1

- (3) If the counting is to be performed in a loop of value TM11CA, the timer 11 loop value is set. (Values from 1~x'FFFF' can be set.) If TM11CA is set to x'1FFF', the counter TM11BC will count from 0 to x'1FFF'. If the TM11CA value is reached by either up or down counting, interrupt A will be generated at the beginning of the next cycle.

TM11CA: x'00FE44'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 CA15	TM11 CA14	TM11 CA13	TM11 CA12	TM11 CA11	TM11 CA10	TM11 CA9	TM11 CA8	TM11 CA7	TM11 CA6	TM11 CA5	TM11 CA4	TM11 CA3	TM11 CA2	TM11 CA1	TM11 CA0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

- (4) If an interrupt is to be generated at the value of TM11CB, the timer 11 interrupt value is set. (Values from 0~TM11CA can be set.) If this value is reached by either up or down counting, interrupt B will be generated at the beginning of the next cycle. If counting is to be performed from 0~x'FFFF', the timer 11 interrupt value is set (values from 0~x'FFFF' can be set). In this example, a value of x'1000' is set.
- (5) TM11NLD is set to '1' and TM11EN is set to '0'. TM11BC and RS.F.F. are in operating states. Other operating modes are not to be altered.
- (6) TM11NLD and TM11EN are both set to '1'. Timer 11 begins operation. Counting starts at the beginning of the cycle that follows the setting cycle.

If these settings are not made, the binary counter may not be counted during the first count and will be unstable.

■ Interrupt Processing

- (7) The interrupt processing is performed. The interrupt processing determines the group, specifies the cause, and clears IRFn. The timing chart below shows the count direction.

With TM11IOA or TM11IOB, timer 11 can control the direction of up/down counting. The count direction is determined by the edge opposite the count edge (indicated by O in the chart below). Timing is shown below. In this example, the count direction is changed from down to up, and an interrupt is generated.

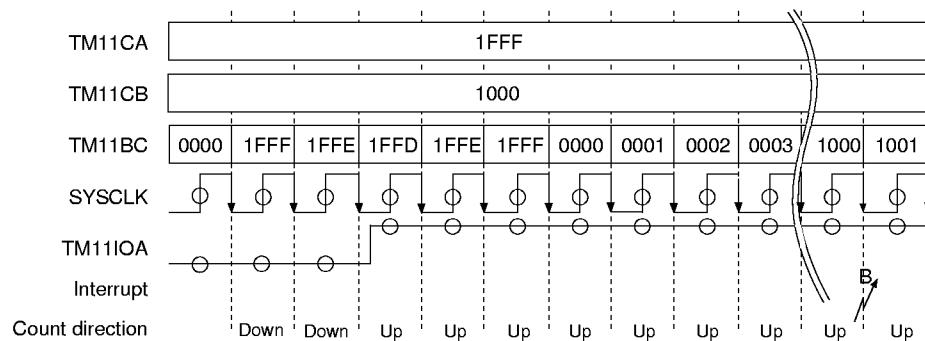


Figure 4-3-10 External Count Direction Control Timing Chart

4-3-9 External Reset Control with 16-bit Timer

The external reset control setting procedure is the same for timers 10 and 11. In this example, an external reset occurs while timer 11 is counting-up.



Data settings use the MOV instruction and must be written as 16 bits.

*TM11BC counting is stopped.
TM11BC and RS.F.F. are initialized (cleared to '0').*

■ Timer 11 Settings

- (1) Operation mode is set in the timer 11 mode register (TM11MD). It is verified that counting has stopped and that interrupts are disabled. The up/down operation is set to count-up. Since the counter is reset asynchronously by TM11IC, TM11ECLR is set to '1'. SYSCLK is selected as the clock source.

TM11MD: x'00FE40'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 EN	TM11 NLD	—	—	TM11 UD1	TM11 UD0	TM11 TGE	TM11 ONE	TM11 MD1	TM11 MD0	TM11 ECLR	TM11 LP	TM11 ASEL	TM11 S2	TM11 S1	TM11 SO
0	0	—	—	0	0	0	0	0	0	1	1	0	0	1	1

- (2) The loop value of timer 11 is set. (Values from 1~x'FFFF' can be set.) If TM11CA is set to x'1FFF', the counter TM11BC will count from 0~x'1FFF'.

TM11CA: x'00FE44'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 CA15	TM11 CA14	TM11 CA13	TM11 CA12	TM11 CA11	TM11 CA10	TM11 CA9	TM11 CA8	TM11 CA7	TM11 CA6	TM11 CA5	TM11 CA4	TM11 CA3	TM11 CA2	TM11 CA1	TM11 CA0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

If these settings are not made, the binary counter may not be counted during the first count and will be unstable.

- (3) TM11NLD is set to '1' and TM11EN is set to '0'. TMBC and RS.F.F. are in operating states.
- (4) TM11NLD and TM11EN are both set to '1'. Timer 11 begins operation. Counting starts at the beginning of the cycle that follows the setting cycle.

Thereafter, when TM11IC is '1', since timer 11 can initiate an asynchronous reset, synchronization to external signals is simple. This can be used to adjust the number of motor rotations, or to for the initialization of timer hardware. The timing chart is shown below.

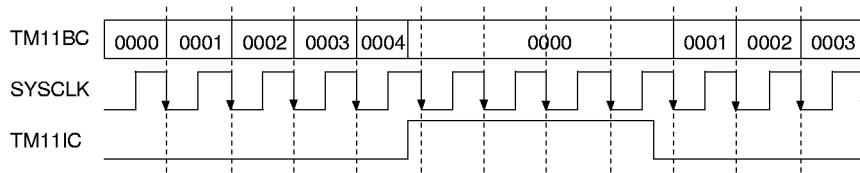


Figure 4-3-11 External Reset Control Timing Chart

Chapter 4 Timer/Counter Functions

Chapter 5 Serial Interface



5-1 Overview of Serial Interface

5-1-1 Overview

This LSI chip includes two serial interfaces, serial interface 0 and 1, each offering a choice of synchronous or asynchronous operation. The maximum transfer rate for synchronous operation is one-eighth of SYSCLK. For a 20MHz oscillator, a top speed of 19,200 bps can be achieved for asynchronous transmission.

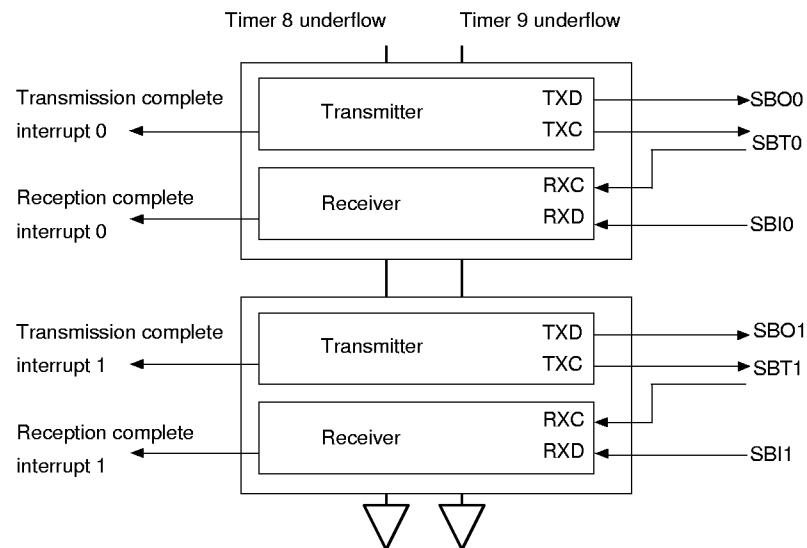


Figure 5-1-1 Serial Interface Configuration

Table 5-1-1 Serial Interface Overview

	Synchronous Serial Interface	Asynchronous Serial Interface
Parity	None, zero, one, even, odd	
Character length	7 or 8 bits	
Bit order	LSB or MSB first	
Source clock	One-eighth output from timer 8 or 9 and SBTn	
Maximum transfer speed	1,250,000 bps (for 20-MHz oscillator)	19,200 bps (for 20-MHz oscillator)
Error detection	Parity errors, overrun errors	Parity errors, overrun errors, framing errors
Buffers	Independent buffers for transmitting (single buffer) and receiving (doublebuffer)	
Interrupts	Transmission complete interrupt, reception complete interrupt	

5-1-2 Control Register

The serial interface control register contains a control register (SCnCTR), transmit/receive register (SCnTRB), and status register (SCnSTR) each for serial interface 0 and 1.

Table 5-1-2 Serial Interface Control Register List

	Serial Interface 0	Serial Interface 1
Control register	Serial 0 control register (SC0CTR), x'00FD80'	Serial 1 control register (SC1CTR), x'00FD90'
Transmit/receive register	Serial 0 transmit/receive register (SC0TRB), x'00FD82'	Serial 1 transmit/receive register (SC1TRB), x'00FD92'
Status register	Serial 0 status register (SC0STR), x'00FD83'	Serial 1 status register (SC1STR), x'00FD93'

The control register (SCnCTR) sets the serial interface control conditions and controls clock source selection, parity bit selection, protocol selection, transmit/receive enable, etc.

The transmit/receive register (SCnTRB) writes to transmit data and reads to receive data. Data is written during transmission. Data transmission begins when data is written to SCnTRB. Data is read during reception. Once the data is written, the transfer begins 1 to 2 transfer clock (underflow of timer 8 or 9) cycles later.

During serial reception, the received data is retrieved by reading data from SCnTRB. When an interrupt is generated or the SCnRXA flag of SCnSTR is '1', the received data can be retrieved.

The MSB (bit 7) is ignored for 7-bit transfers.

The MSB (bit 7) is '0' for 7-bit transfers.

The status register (SCnSTR) reads the status of such things as serial interface error detection. An overrun error occurs when the reception of new data is completed before the previous data is read from the SCnTRB. By reading SCnTRB, an error will not be generated at the next cycle. Overrun error information is updated when the last bit (the 7th or 8th bit) has been received. A parity error occurs if '1' is received when the parity was fixed at 0, '0' is received when the parity bit was fixed at 1, odd parity is received when set for even parity, or even parity is received when set for odd parity. Parity error information is updated when the parity bits are received. A framing error occurs if '0' is received during a stop bit transfer. Framing error information is updated when the stopbit is received.

5-1-3 Serial Interface Connection Methods

The four types of serial interface connections are shown below.

■ Asynchronous connections

The asynchronous connections may be unidirectional or bidirectional.

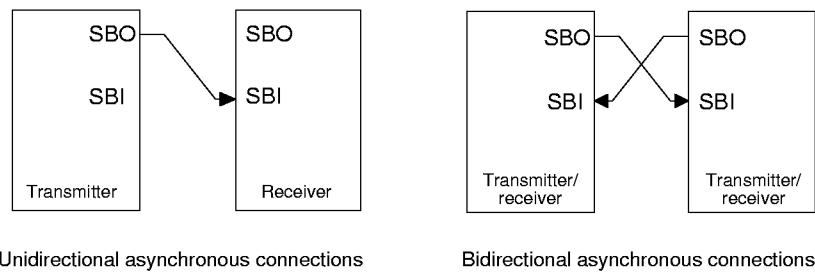


Figure 5-1-2 Asynchronous Connections

■ Synchronous connections

The synchronous connections may be unidirectional or bidirectional.

Refer to Chapter 9 for SBT port settings.

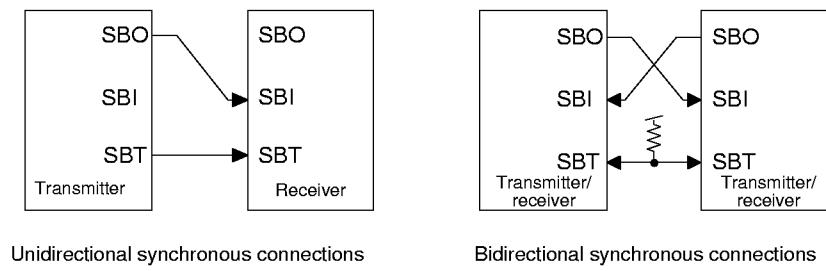


Figure 5-1-3 Synchronous Connections

In the bidirectional configuration, the SBT pins default to input when neither side is transmitting, so a pull-up resistor becomes necessary. This pull-up resistor may be external or may use the one built into the chip.

The transfer clock for both synchronous and asynchronous serial interfaces is set at 8 times the transfer baud rate clock.

Table 5-1-3 Transfer Clock Settings

Transfer clock setting (bps)	Frequency division at 20MHz	Example frequency divider settings
19200	65	Divide timer 8 by 65
9600	130	Divide timer 8 by 130, or prescaler 1 by 65 and timer 8 by 2
4800	260	Divide timer 8 by 260, or prescaler 1 by 65 and timer 8 by 4

$$\text{baud rate (bps)} = (\text{oscillation source OSCI, OSCO}) \times 1/16 \times 1/\text{freq. divider factor of timer}$$

The above example is for 20MHz oscillation. By using 9.8304MHz or 19.6608MHz crystal oscillators, baud rates of 38400 bps and above can be achieved.

5-2 Example Serial Interface Settings

5-2-1 Serial Interface Asynchronous Transmission with Timer 8

The following example illustrates the case where serial interface 0 is used for asynchronous transmission. The settings are for a transfer rate of 9,600 bps (timer 8 and prescaler 1 divide SYSCLK by 130), a bit order of LSB first, 8-bit data transfer, 2 stop bits and odd parity. After an interrupt signals that the transmission is complete, the next data is transmit.

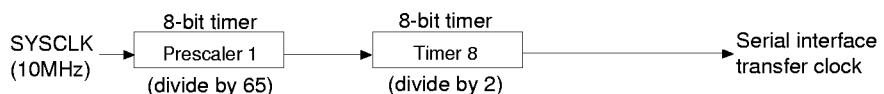


Figure 5-2-1 Example of Asynchronous Transmission

Data transmission begins when data is written to the SCTR0 register. The start of data transmission is synchronized to the underflow of timer 8 (at the 2nd occurrence of timer 8 underflow). An interrupt is generated to signal that the transmission is complete. The interrupt processing routine writes new data for transmission. If interrupts are not used, the SC0TBSY flag of SCSTR is polled to determine when processing should be performed.



In the case of asynchronous reception, the timer must also be set.

The transfer baud rate of the serial interface is determined by 8 times (divided by 8 at the serial interface) the underflow of timer 8 or timer 9. At 20MHz (SYSCLK = 10MHz), a baud rate of 9600 bps is determined by the following computation:

$$10\text{MHz}/8/9600=130.21 \text{ bps}$$

The underflow of timer 8 or timer 9 is set to 130. In this example, prescaler 1 divides by 65 and timer 8 divides by 2.

■ Prescaler 1 Settings

Verification is not necessary immediately after reset.

- (1) The prescaler 1 mode register (PS1MD) verifies that the counting operation has been halted. The above settings are made immediately after reset.

PS1MD: x'00FE2B'

7	6	5	4	3	2	1	0
PS1 EN	PS1 LD	—	—	—	—	—	—
0	0						

- (2) The prescaler frequency divider factor is set. Since SYSCLK is divided by 65, the prescaler 1 base register (PS1BR) is set to 64 (values in the range 1 to 255 can be set).

PS1BR: x'00FE1B'

7	6	5	4	3	2	1	0
PS1 BR7	PS1 BR6	PS1 BR5	PS1 BR4	PS1 BR3	PS1 BR2	PS1 BR1	PS1 BR0
0	1	0	0	0	0	0	0

- (3) PS1LD is set to 1 and PS1EN is set to 0 (the contents of PS1BR are read into PS1BC).

- (4) Both PS1LD and PS1EN are set to 0.

- (5) PS1LD is set to 0 and PS1EN is set to 1. The prescaler begins operation. Counting begins at the cycle following the setting cycle.

■ Timer 8 Settings

- (6) The timer 8 mode register (TM8MD) verifies that the counting operation has been halted.

Verification is not necessary immediately after reset.

TM8MD: x'00FE28'

7	6	5	4	3	2	1	0
TM8 EN	TM8 LD	—	—	—	—	TM8 S1	TM8 S0
0	0				1	1	

- (7) The frequency divider factor for the timer is set. Since the prescaler output will be divided by 2, the timer 8 base register (TM8BR) is set to 1 (values in the range of 1 to 255 can be set).

TM8BR: x'00FE18'

7	6	5	4	3	2	1	0
TM8 BR7	TM8 BR6	TM8 BR5	TM8 BR4	TM8 BR3	TM8 BR2	TM8 BR1	TM8 BR0
0	0	0	0	0	0	0	1


If the frequency divider factor is 1, a dummy value (x'0F' for example) is written once in procedure (2). Then, after procedure (5), the prescaler 1 base register (PS1BR) is reset with a prescaler frequency divider value of '0'. The first count uses the value settings of procedure (2). However, for the second count on, frequency division by 1 is used. If '0' is set in procedure (2), the first count will divide the frequency by 257. From the second count on, division will be by 1.

If these settings are not made, the binary counter (PS1BC) may not be counted during the first count and will be unstable.



Be sure not to change the selected clock source. If the clock source selection is changed at the same time as the count operation control, the value the binary counter will be corrupted.

If this setting is not made, TM8BC may not be counted during the first count and will be unstable.

Counting begins at the cycle following the setting cycle.

- (8) TM8LD is set to '1' and TM8EN is set to '0' (the value of TM8BR is read into TM8BC). At the same time, the clock source is selected.

- (9) Both TM8LD and TM8EN are set to '0'.

- (10) TM8LD is set to '0' and TM8EN is set to '1'. The timer begins operation.

■ Serial Interface 0 Settings

- (11) Interrupts are enabled, and at this time, all prior interrupt requests are cleared.

In other words, in maskable interrupt control register (group 9) (G9ICR), the interrupt level (6~0) is set, SC0TIR is set to '0', and SC0TIE is set to '1'. For example, G9ICR is set to x'4100'. Thereafter, a serial transfer complete interrupt will be generated when the transfer of data that was written to the serial transfer/receive register is complete.

G9ICR: x'00FC52'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	SC LV2	SC LV1	SC LVO	SC1R IE	SC1T IE	SC0R IE	SC0T IE	SC1R IR	SC1T IR	SC0R IR	SC0T IR	SC1R ID	SC1T ID	SC0R ID	SC0T ID
0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0

- (12) The serial 0 control register (SC0CTR) is set to the operation control conditions. The settings are for asynchronous transmission, a bit order of LSB first, 2 stop bits and odd parity.

SC0CTR: x'00FD80'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SC0 TEN	SC0 REN	SC0 BRE	—	SC0 PTL	—	SC0 OD	—	SC0 LN	SC0 PTY2	SC0 PTY1	SC0 PTY0	SC0 SB	—	SC0 S1	SC0 S0
1	1	0	—	0	—	0	—	1	1	1	1	1	—	0	1

- (13) The serial 0 transfer/receive register (SC0TRB) is set with the initial data to be transferred. Once the data for transfer is set, transmission begins in synchronization with timer 8. If an interrupt is generated, the interrupt is processed and the next data is transferred.

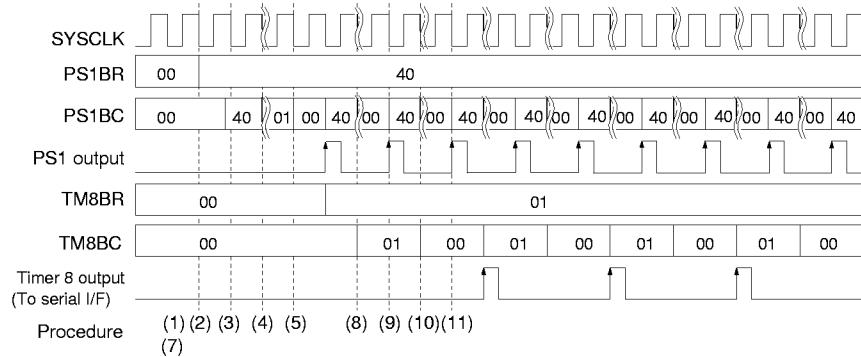


Figure 5-2-2 Asynchronous Transmission Timing of Serial Interface 0

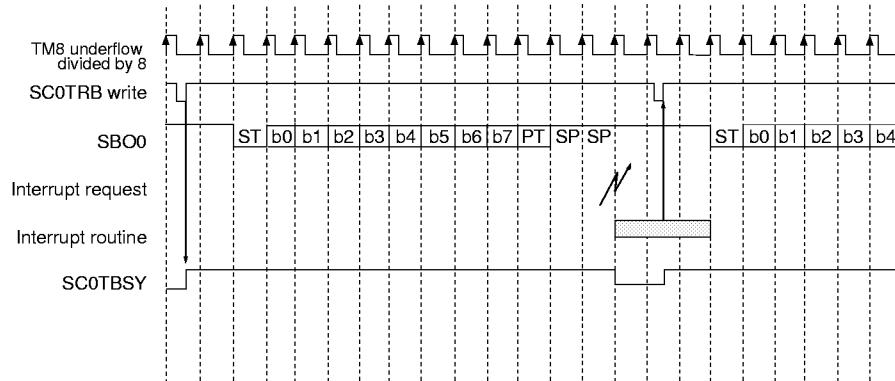


Figure 5-2-3 Bit Transmission Timing for Asynchronous Transmission

5-2-2 Serial Interface Synchronous Reception with Timer 8

The following example illustrates the case where a serial interface is used for synchronous reception. Settings are for a bit order of LSB first, 8-bit data transfer and odd parity. After a receive complete interrupt, data is retrieved.

■ Port 3 Settings

The port 3 I/O control (P3DIR) is set to SBT 0 input for the serial interface (P3DIR4='0').

■ Serial Interface 0 Settings

- (1) The serial 0 control register (SC0CTR) is set with the operating control conditions. Settings are for synchronous transmission, a bit order of LSB first, 1/8 of the timer 8 underflow, 8-bit data transfer and odd parity.

SC0CTR: x'00FD80'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SC0 TEN	SC0 REN	SC0 BRE	—	SC0 PTL	—	SC0 OD	—	SC0 LN	SC0 PTY2	SC0 PTY1	SC0 PTY0	SC0 SB	—	SC0 S1	SC0 S0
1	1	0	—	1	—	0	—	1	1	1	1	0	—	0	1

- (2) Interrupts are enabled, and at this time, all prior interrupt requests are cleared.

In other words, in maskable interrupt control register (group) 9 (G9ICR), the interrupt level (6~0) is set, SC0RIR is set to '0', and SC0RIE is set to '1'. For example, G9ICR is set to x'4200'. Thereafter, a serial receive complete interrupt will be generated when the data write to the serial transfer/receive register is complete.

G9ICR: x'00FC52'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	SC LV2	SC LV1	SC LV0	SC1R IE	SC1T IE	SC0R IE	SC0T IE	SC1R IR	SC1T IR	SC0R IR	SC0T IR	SC1R ID	SC1T ID	SC0R ID	SC0T ID
0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Thereafter, an interrupt will be generated when serial data is received.

After the interrupt processing determines the group, specifies the cause, and clears IRFn, the interrupt processing routine is specified.

Chapter 6 Analog Interface

6

6-1 Analog Interface Summary

6-1-1 Overview

The analog interface is an 8-bit charge redistribution analog-to-digital converter that supports digital signal processing in the voice and audio ranges with a resolution of 8 bits, a maximum conversion frequency of 250KHz (4 μ s at 20MHz), and a low current.

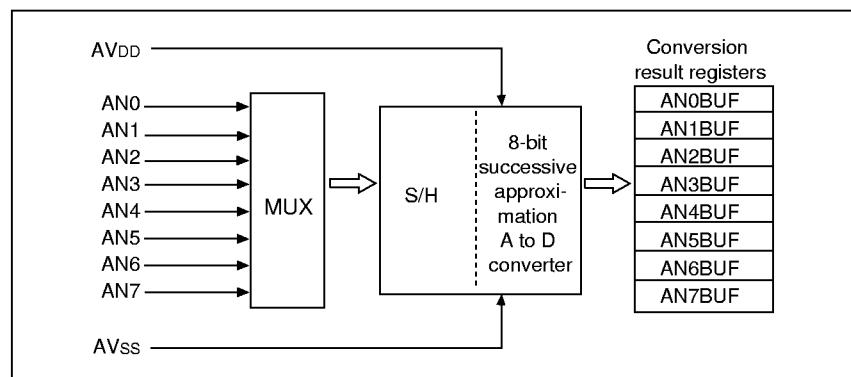


Figure 6-1-1 Analog Interface Configuration

Table 6-1-1 Analog Interface Summary

Sample and hold circuit	Built in
Conversion precision	8 bits \pm 3 LSB The interval between AVDD and AVss is divided into 256 levels and these values are stored in registers AN7BUF~AN0BUF.
Conversion time	4.0 μ s or greater per channel (sampling interval of 400ns at 20MHz)
Clock selection	1/1, 1/2, 1/4, and 1/8th of internal system clock SYSCLK
Operating modes	30 modes: Single-shot conversion on ch0 Continuous conversion on ch0 Single-shot conversion on ch1, Continuous conversion on ch1, Single-shot conversion on ch0~1 Continuous conversion on ch0~1 Single-shot conversion on ch2, Continuous conversion on ch2, Single-shot conversion on ch0~2 Continuous conversion on ch0~2 Single-shot conversion on ch3, Continuous conversion on ch3, Single-shot conversion on ch0~3 Continuous conversion on ch0~3 Single-shot conversion on ch4, Continuous conversion on ch4, Single-shot conversion on ch0~4 Continuous conversion on ch0~4 Single-shot conversion on ch5, Continuous conversion on ch5, Single-shot conversion on ch0~5 Continuous conversion on ch0~5 Single-shot conversion on ch6, Continuous conversion on ch6, Single-shot conversion on ch0~6 Continuous conversion on ch0~6 Single-shot conversion on ch7, Continuous conversion on ch7, Single-shot conversion on ch0~7 Continuous conversion on ch0~7
Conversion start	TM7 underflow or software modification of register
Interrupts	Issued at the end of each set of channel operations

■ Clock Selection for A/D Converter

The A/D converter clock is selected as SYSCLK divided by 1, 2, 4, or 8. Select the converter clock such that the conversion time will be 4 μ s or greater (ie. SYSCLK frequency/divider value 5MHz). For example, with 20MHz oscillation, the A/D converter clock is set to SYSCLK divided by 4 (conversion speed of 4 μ s) or SYSCLK divided by 8 (conversion speed of 8 μ s). Similarly, for 10MHz, the converter clock is set to SYSCLK divided by 2, 4, or 8. If the oscillation clock is 5MHz or less, SYSCLK divided by 1, 2, 4, or 8 can be selected for the converter clock.

As shown below, the conversion time is 10 cycles of the A/D converter clock. For example, when the SYSCLK is divided by 4, the conversion time in units of seconds is [SYSCLK period (s) \times 4 (frequency divider) \times 40 (cycles)].

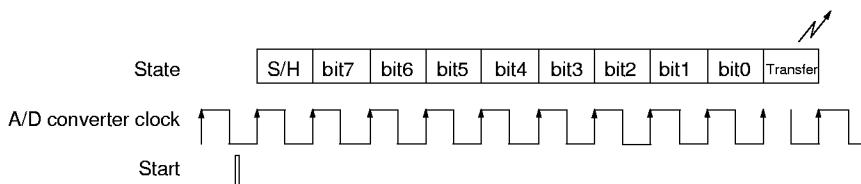


Figure 6-1-2 A/D Conversion Timing

■ Single-shot Conversion on Arbitrary One Channel

These modes sample a single A/D input just once, and when conversion is finished, issue an A/D interrupt. Set AN1CH (the arbitrary one channel for conversion) to the number of the conversion channel.

To start the conversion with ANEN (conversion start and execute flag bit), ANTC7 (timer 7 conversion start flag) is set to '0' and ANEN to '1'. ANEN remains at a '1' during the conversion and changes to '0' upon completion.

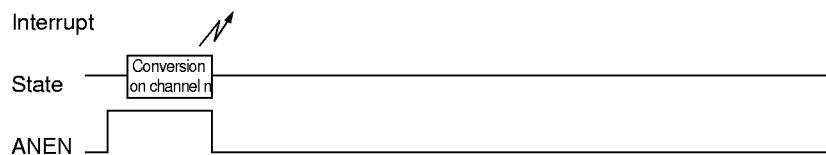


Figure 6-1-3 Timing of Single-shot Conversion on Arbitrary One Channel

■ Single-shot Conversion on Multiple Channels

These modes sample A/D inputs just once at pin AN0 (channel 0) through the specified channel. When the channels have all been converted, an interrupt is generated. Set AN1CH (arbitrary one channel for conversion) to channel 0 and ANNCH (conversion channel) to the number of the last channel. (The conversion begins from channel 0).

To start the conversion with ANEN (conversion start and execute flag bit), ANTC7 (timer 7 conversion start flag) is set to '0' and ANEN to '1'. ANEN remains at a '1' during the conversion and changes to '0' after conversion is complete for all the channels. Also, AN1CH contains the number of the channel currently being converted. After all channels have been converted, it is reset to '0'.

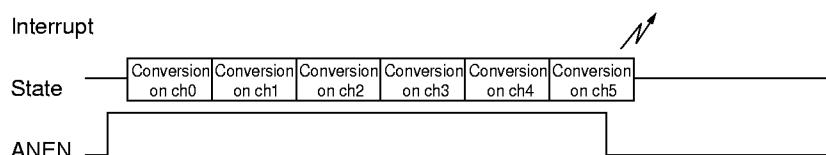


Figure 6-1-4 Timing of Single-shot Conversion on Multiple Channels

■ Continuous Conversion on Arbitrary One Channel

These modes continuously sample a single A/D input and issue an A/D interrupt after each conversion. Set AN1CH (the arbitrary one channel for conversion) to the number of the conversion channel.

To start the conversion with ANEN (conversion start and execute flag bit), ANTC7 (timer 7 conversion start flag) is set to '0' and ANEN to '1'. Forcibly setting ANEN to '0' causes the conversion to stop.

ANNCH is ignored.

AN1CH, ANNCH, ANEN, and ANTC7 are the names of flags in the A/D conversion control register (ANCTR).

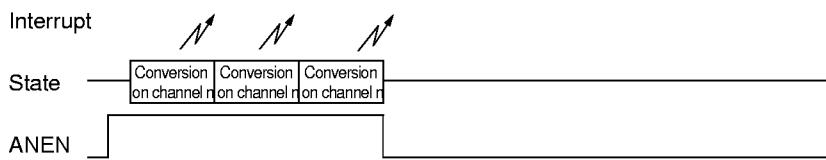


Figure 6-1-5 Timing of Continuous Conversion on Arbitrary One Channel

■ Continuous Conversion on Multiple Channels

These modes continuously sample A/D inputs at pin AN0 (channel 0) through the specified channel and issue an A/D interrupt each time after all the channels have all been converted. Set AN1CH (the arbitrary one channel for conversion) to channel 0, and ANNCH (conversion channel) to the number of the last channel. (The conversion begins from channel 0).

To start the conversion with ANEN (conversion start and execute flag bit), ANTC7 (timer 7 conversion start flag) is set to '0' and ANEN to '1'. Forcibly setting ANEN to '0' causes the conversion to stop. ANEN remains at a '1' during the conversion and changes to '0' after conversion is complete for all the channels. Also, AN1CH contains the number of the channel currently being converted. After all channels have been converted, it is reset to '0'.

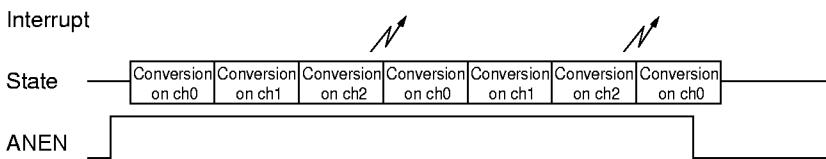


Figure 6-1-6 Timing of Continuous Conversion on Multiple Channels

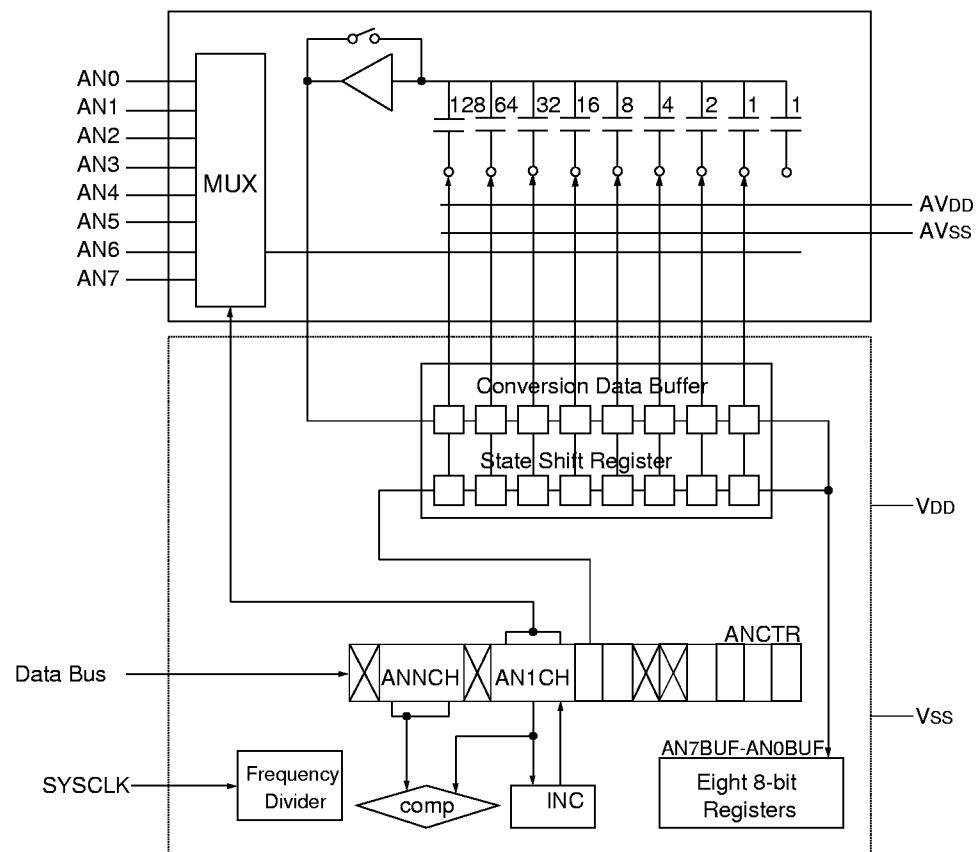


Figure 6-1-7 Analog Interface Block Diagram

6-1-2 Control Registers

The analog interface control registers include the A/D conversion control register (ANCTR) and A/D conversion data registers (ANnBUF) that correspond to channels 7~0 (pins AN7~0).

Table 6-1-2 List of Analog Interface Control Registers

Control Register	A/D Control Register (ANCTR), x'00FDA0'	
Data Registers	A/D0 Conversion Data Buffer (AN0BUF), x'00FDA8'	A/D4 Conversion Data Buffer (AN4BUF), x'00FDAC'
	A/D1 Conversion Data Buffer (AN1BUF), x'00FDA9'	A/D5 Conversion Data Buffer (AN5BUF), x'00FDAD'
	A/D2 Conversion Data Buffer (AN2BUF), x'00FDAA'	A/D6 Conversion Data Buffer (AN6BUF), x'00FDAE'
	A/D3 Conversion Data Buffer (AN3BUF), x'00FDAB'	A/D7 Conversion Data Buffer (AN7BUF), x'00FDAD'

Control register (ANCTR) sets the A/D converter control conditions.

The A/D conversion results from channels 7~0 (pins AN7~0) are input to the data registers (ANnBUF). Therefore, these registers cannot be written to. Initial values are undefined.

6-2 Analog Interface Setting Examples

6-2-1 Software Initiated Single Channel A/D Conversion Using Pin AN6

The following example illustrates the case where single channel A/D conversion is initiated through software. An analog voltage (0~5V) is input to pin AN6. A/D conversion results are obtained.

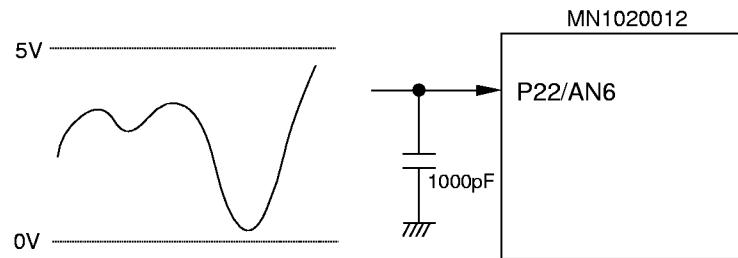


Figure 6-2-1 Single Channel A/D Conversion

■ Port 2 Setting

- (1) The AN6 pin (P22) of port 2 is set as a general purpose input (P22DIR='0').

■ A/D Conversion Control Register Settings

- (2) The A/D conversion control register (ANCTR) is set to operation mode. Operation mode ANMD is set for single-shot conversion of any one channel, and the clock is set to SYSCLK/4 (10MHz/4 for 20MHz oscillation). The ANEN conversion start flag is set to '0' and AN1CH is set to the conversion channel (ch6).
- ANNCH is ignored.*

ANCTR: x'00FDA0'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	AN NCH2	AN NCH1	AN NCHO	—	AN 1CH2	AN 1CH1	AN 1CH0	AN EN	AN TC7	—	—	AN CK1	AN CK0	AN MD1	AN MDO
—	0	0	0	—	1	1	0	0	0	—	—	1	0	0	0

- (3) The ANEN conversion start flag is set to '1' in order to begin the conversion. With ANEN set to '1', the conversion begins at the rising edge of the clock for the initial A/D conversion. The conversion lasts for 10 cycles of the A/D conversion clock (4 μ sec, 4~4.4 μ sec after setting ANEN).

- (4) Conversion completion is waited for. The ANEN flag is '1' during conversion and cleared to '0' upon completion.

- (5) The AN6 conversion data buffer (AN6BUF) is read.

The conversion divides the range from 0~5V into 256 levels. The converted result is returned with a value of 0~255.

If software will initiate the A/D conversion, the ANEN flag is set to '1'.

The conversion results can also be read by generating an interrupt. In this case, since an interrupt is generated after the converted result has been stored in AN6BUF, it is not necessary to wait for the ANEN flag.

AN6BUF: x'00FDAE'

7	6	5	4	3	2	1	0
AN6 BUF7	AN6 BUF6	AN6 BUF5	AN6 BUF4	AN6 BUF3	AN6 BUF2	AN6 BUF1	AN6 BUF0

6-2-2 Timer Initiated Multiple Channel A/D Conversion Using Pins AN2~0

Analog voltages (0~5V) are input to pins AN2, AN1, and AN0. A/D conversion results are obtained. Conversion is periodically initiated by timer 7.

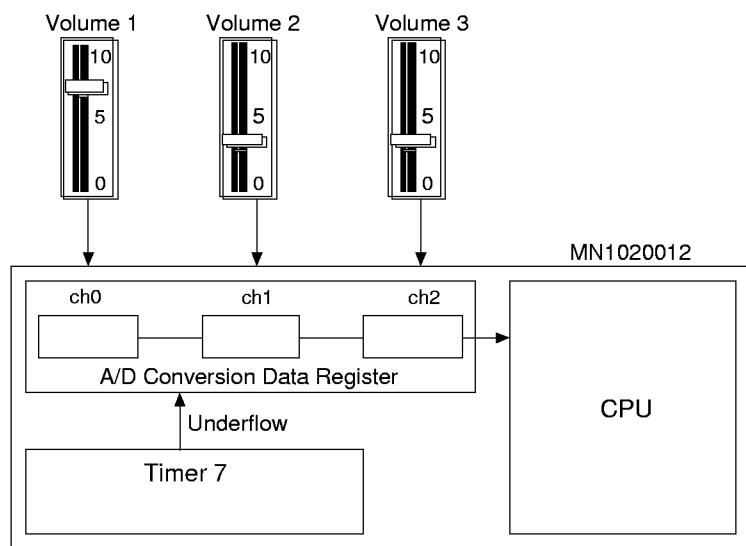


Figure 6-2-2 Multiple Channel A/D Conversion

■ A/D Conversion Control Register Settings

- (1) The A/D conversion control register (ANCTR) is set to operation mode. Operation mode ANMD is set for single-shot conversion of multiple channels, and the clock is set to SYSCLK/4 (10MHz/4 for 20MHz oscillation). The ANEN conversion start flag is set to '0', ANCT7 to '1', AN1CH to channel 0, and ANNCH to the number of the last channel for conversion, channel 2.

ANCTR: x'00FDA0'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	AN NCH2	AN NCH1	AN NCH0	—	AN 1CH2	AN 1CH1	AN 1CH0	AN EN	AN TC7	—	—	AN CK1	AN CK0	AN MD1	AN MD0

— 0 1 0 — 0 0 0 0 1 — — 1 0 0 1

■ Timer 7 Settings (Setting the Conversion Period)

- (2) The timer 7 frequency divider factor is set. If SYSCLK is to be divided by 256, the timer 7 base register (TM7BR) is set to 255. (Values from 1~255 may be set).

TM7BR: x'00FE17'

7	6	5	4	3	2	1	0
TM7 BR7	TM7 BR6	TM7 BR5	TM7 BR4	TM7 BR3	TM7 BR2	TM7 BR1	TM7 BR0
1	1	1	1	1	1	1	1

- (3) TM7LD of the timer 7 mode register (TM7MD) is set to '1' and TM7EN is set to '0'. (The value of TM7BR is read into TM7BC). At the same time, the clock source is selected.

TM7MD: x'00FE27'

7	6	5	4	3	2	1	0
TM7 EN	TM7 LD	—	—	—	—	TM7 S1	TM7 S0
1	1	—	—	—	—	1	0

- (4) TM7LD and TM7EN are both set to '0'.

- (5) TM7LD is set to '0' and TM7EN is set to '1'. The timer begins operation. Counting begins at the start of the cycle following the setting cycle.

If the binary counter (TM7BC) reaches 0, and at the next count, the contents of the base register (TM7BR) are read to be 255, then timer 7 underflow (interrupt) will occur. Upon underflow of timer 7, single-shot conversion will be performed on each pin AN2~AN0.

Hereafter, be sure not to change the selected clock source. If the clock source selection is changed at the same time as the count operation control, the value the binary counter will be corrupted.

If this setting is not made, the binary counter (TM7BC) may not be counted during the first count and will be unstable.

Compared to continuous A/D conversion, periodic conversion reduces the consumption of electric power.

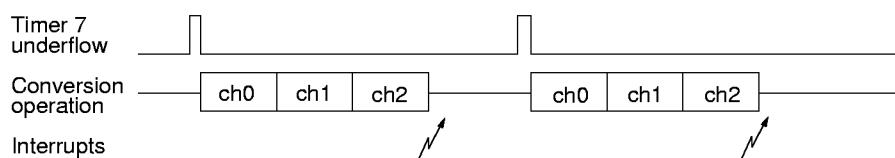


Figure 6-2-3 A/D Conversion Timing
(single-shot conversion on channels 0~2)

Chapter 6 Analog Interface

Chapter 7 Synchronous Output Functions

7

7-1 Synchronous Output Function Summary

7-1-1 Overview

The synchronous output function consists of two 4-bit channels that realize a driving circuit for a 4-phase stepping motor. 4-phase single excitation, 4-phase double excitation, or 4-phase 1-2 excitation waveforms can be generated for both forward and reverse rotation. When forward rotation of the motor is to be stopped or changed to reverse rotation, the software need only manage the timer and rotation direction. The synchronization circuit is configured from a 4-bit shift register and can also be used in LED dynamic circuit applications.

Stepping motors having 5 to 8 phases can be used with arbitrary patterns. The output timing uses a timer. The next pattern to be output is set by an interrupt program or DMA. [☞ 7-2-3 Synchronous Output of Arbitrary Pattern]
The output timing has a choice of timers: timer 1 (TC1) underflow or timer 12 (TC12) compare capture A.

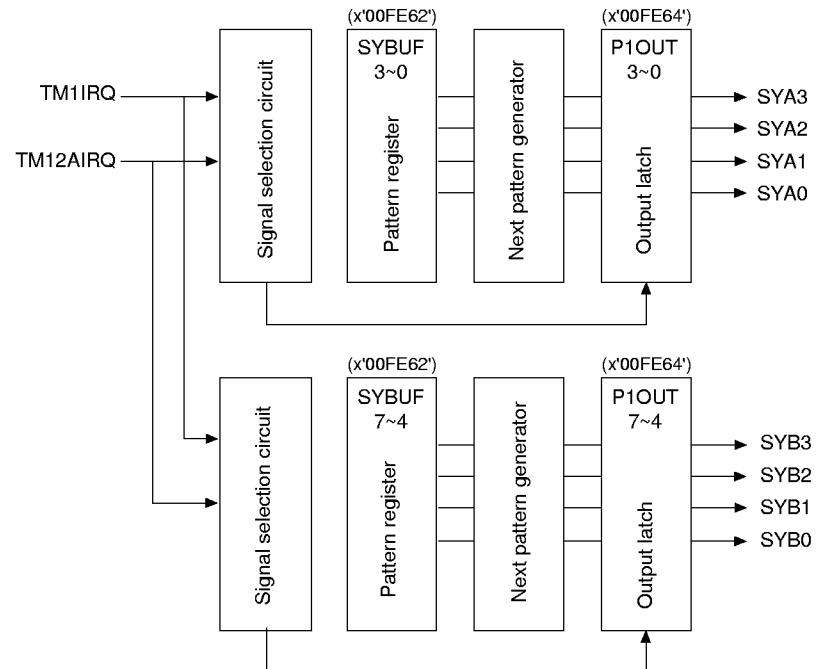


Figure 7-1-1 Synchronous Output Block Diagram

Table 7-1-1 Overview of Synchronous Output Function

Configuration	Two 4-bit channels (A, B) (2 channels can be used asynchronously)
Rotation Direction Control	Forward or reverse
Operating Modes	Four modes: arbitrary pattern output 4-phase single excitation 4-phase double excitation 4-phase 1-2 excitation
Output Timing	Timer 1 underflow or timer 12 compare/capture A interrupt

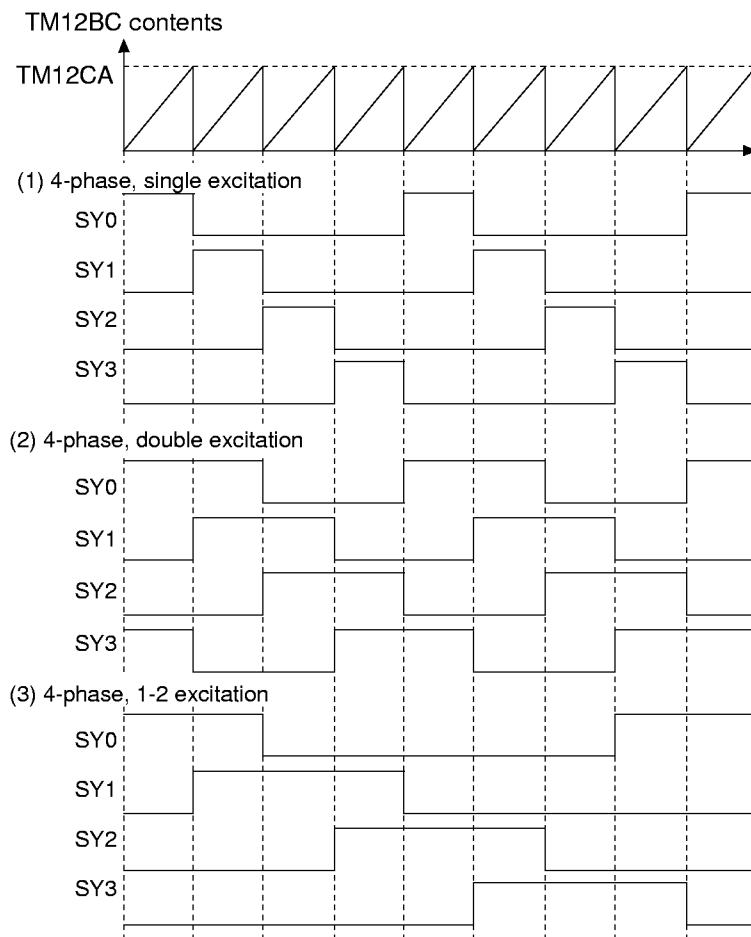


Figure 7-1-2 4-phase Motor Drive Patterns

7-1-2 Control Registers

Synchronous output control registers include synchronous output A and B mode registers (SYAMD, SYBMD), synchronous output buffer (SYBUF) that sets the output pattern, and the port 1 output latch (P1OUT).

Table 7-1-2 List of Synchronous Output Control Registers

Mode Registers	Synchronous Output A Mode Register (SYAMD), x'00FE60'	Synchronous Output B Mode Register (SYBMD), x'00FE61'
Pattern Registers	Synchronous Output Buffer (SYBUF), x'00FE62'	Port 1 Output Latch (P1OUT), x'00FE64'

Synchronous output A and B mode registers (SYAMD, SYBMD) set the individual control conditions (operating mode, rotation direction, transition timing selection, enable/disable) for synchronous outputs A and B.

During output of an arbitrary pattern from synchronous outputs A and B, the synchronous output buffer (SYBUF) sets the output pattern with the initial synchronous output transition timing. The port 1 output latch (P1OUT) sets the initial output pattern for synchronous outputs A and B.

7-2 Synchronous Output Function Setting Example

7-2-1 Synchronous Output Example: 4-phase, Single Excitation (4-phase, Double Excitation)

In this example, underflow of timer 1 initiates forward rotation at a constant speed of a 4-phase motor.

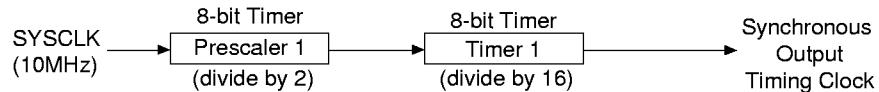


Figure 7-2-1 Synchronous Output Configuration Example (1)

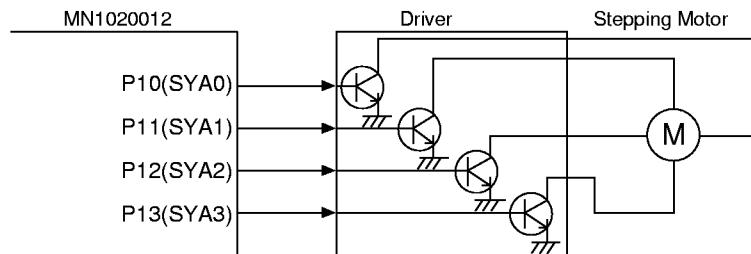


Figure 7-2-2 4-phase Stepping Motor Connection Example

■ Port Output Setting

- (1) Port 1 (P13 to P10) is configured for general purpose output (P1DIR3 to P1DIR0=1).

■ Synchronous Output Setting

- (2) The synchronous output A mode register (SYAMD) is set with the operating mode. The operating mode is 4-phase, single excitation (SYAMD=01), the rotation direction is forward (SYADIR=0), synchronous output A is selected for the output (SYAEN=1), and the synchronous output transition timing is set to the underflow of timer 1 (SYAIRQ=0).

SYAMD: x'00FE60'

7	6	5	4	3	2	1	0
—	—	—	SYA IRQ	SYA EN	SYA DIR	SYA MD1	SYA MD0
—	—	—	0	1	0	0	1

- (3) The initial output pattern is set. When the output mode is for 4-phase and single-excitation, the port 1 output latch is set with any of one the following bit strings: 0001, 0010, 0100, or 1000. For 4-phase double-excitation, any one of the following bit strings is set: 0011, 0110, 1100, 1001.

In the case of negative logic output, any one of the following bit strings is set: 1110, 1101, 1011, or 0111.

P1OUT: x'00FE64'

7	6	5	4	3	2	1	0
P1OUT7	P1OUT6	P1OUT5	P1OUT4	P1OUT3	P1OUT2	P1OUT1	P1OUT0
0	0	0	0	0	0	0	1

- (4) Timer 1 is activated.

[☞ Chapter 4, Timing Counter Functions]

The pattern changes every time timer 1 underflow occurs. Set values and modified values are listed below. Forward rotation shifts left and reverse rotation shifts right.

4-phase Single-excitation Forward Rotation

Initial Setting	0001	0010	0100	1000
1st	0010	0100	1000	0001
2nd	0100	1000	0001	0010
3rd	1000	0001	0010	0100
4th	0001	0010	0100	1000
5th	0010	0100	1000	0001

4-phase Single-excitation Reverse Rotation

Initial Setting	0001	0010	0100	1000
1st	1000	0001	0010	0100
2nd	0100	1000	0001	0010
3rd	0010	0100	1000	0001
4th	0001	0010	0100	1000
5th	1000	0001	0010	0100

4-phase Double-excitation Forward Rotation

Initial Setting	0011	0110	1100	1001
1st	0110	1100	1001	0011
2nd	1100	1001	0011	0110
3rd	1001	0011	0110	1100
4th	0011	0110	1100	1001
5th	0110	1100	1001	0011

7-2-2 Synchronous Output Example: 4-phase, 1-2 Excitation

The compare/capture A interrupt of timer 12 causes a 4-phase motor to rotate in the reverse direction at a constant speed.



Figure 7-2-3 Synchronous Output Configuration Example (2)

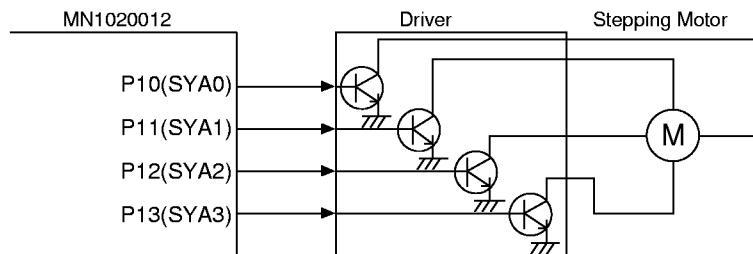


Figure 7-2-4 4-phase Stepping Motor Connection Example (2)

■ Port Output Setting

- (1) Port 1 (P13 to P10) is configured for general purpose output (P1DIR3 to P1DIR0=1).

■ Synchronous Output Setting

- (2) The synchronous output A mode register (SYAMD) is set with the operating mode. The operating mode is 4-phase, 1-2 excitation (SYAMD=01), the rotation direction is forward (SYADIR=0), synchronous output A is selected for the output (SYAEN=1), and the synchronous output transition timing is set to the compare/capture A interrupt of timer 12 (SYAIRQ=1).

SYAMD: x'00FE60'

7	6	5	4	3	2	1	0
—	—	—	SYA IRQ	SYA EN	SYA DIR	SYA MD1	SYA MD0
—	—	—	1	1	0	1	0

- (3) The initial output pattern is set. When the output mode is for 4-phase and single-excitation, the port 1 output latch is set with any of one the following bit strings: 0001, 0011, 0010, 0110, 0100, 1100, 1000, or 1001.

Negative logic output cannot be set.

P1OUT: x'00FE64'

7	6	5	4	3	2	1	0
P1OUT7	P1OUT6	P1OUT5	P1OUT4	P1OUT3	P1OUT2	P1OUT1	P1OUT0
0	0	0	0	0	0	0	1

- (4) Timer 1 is activated.

[☞ Chapter 4, Timing Counter Functions]

The pattern changes every time timer 12 compare/capture A interrupt occurs. Set values and modified values are listed below. Forward rotation shifts left and reverse rotation shifts right.

4-phase, 1-2 Excitation Forward Rotation

Initial Setting	0001	0011	0010	0110	0100	1100	1000	1001
1st	0011	0010	0110	0100	1100	1000	1001	0001
2nd	0010	0110	0100	1100	1000	1001	0001	0011
3rd	0110	0100	1100	1000	1001	0001	0011	0010
4th	0100	1100	1000	1001	0001	0011	0010	0110
5th	1100	1000	1001	0001	0011	0010	0110	0100
6th	1000	1001	0001	0011	0010	0110	0100	1100
7th	1001	0001	0011	0010	0110	0100	1100	1000
8th	0001	0011	0010	0110	0100	1100	1000	1001
9th	0011	0010	0110	0100	1100	1000	1001	0001

4-phase, 1-2 Excitation Reverse Rotation Initial Setting

Initial Setting	0001	0011	0010	0110	0100	1100	1000	1001
1st	1001	0001	0011	0010	0110	0100	1100	1000
2nd	1000	1001	0001	0011	0010	0110	0100	1100
3rd	1100	1000	1001	0001	0011	0010	0110	0100
4th	0100	1100	1000	1001	0001	0011	0010	0110
5th	0110	0100	1100	1000	1001	0001	0011	0010
6th	0010	0110	0100	1100	1000	1001	0001	0011
7th	0011	0010	0110	0100	1100	1000	1001	0001
8th	0001	0011	0010	0110	0100	1100	1000	1001
9th	1001	0001	0011	0010	0010	0110	0100	1100

7-2-3 Synchronous Output of Arbitrary Pattern

7-segment LEDs are configured for display upon underflow of timer 1.

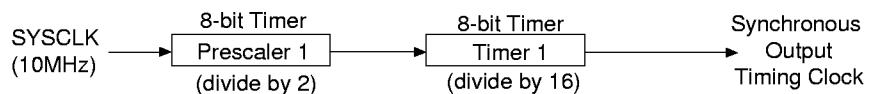


Figure 7-2-5 Synchronous Output Configuration Example (3)

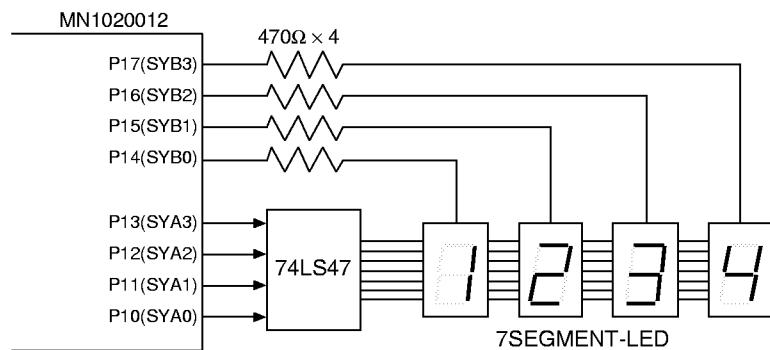


Figure 7-2-6 Seven Segment LED Connection Example

■ Port Output Setting

- (1) Port 1 (P17 to P10) is configured for general purpose output (P1DIR7 to P1DIR0=1).

■ Synchronous Output Setting

- (2) The synchronous output B mode register (SYBMD) is set to the operating mode. Since the dynamic LED display turns on only one of the 7-segment LEDs, the operating mode is set for 4-phase single-excitation (SYAMD=01), rotation in the forward direction (SYADIR=0), synchronous output A is selected (SYAEN=1), and timer 1 underflow is set for synchronous output modified timing (SYAIRQ=0).

SYBMD: x'00FE61'

7	6	5	4	3	2	1	0
—	—	—	SYB IRQ	SYB EN	SYB DIR	SYB MD1	SYB MD0
—	—	—	0	1	0	0	1

- (3) The synchronous output A mode register (SYAMD) is set to the operating mode. The operating mode is set for arbitrary output (SYAMD=00), rotation in the forward direction (SYADIR=0, setting is ignored), port 1 synchronous output is selected (SYAEN=1), and timer 1 underflow is set for synchronous output timing changes (SYAIRQ=0).

SYAMD: x'00FE60'

7	6	5	4	3	2	1	0
—	—	—	SYA IRQ	SYA EN	SYA DIR	SYA MD1	SYA MD0
—	—	—	0	1	0	0	0

- (4) The initial output pattern is set. The port 1 output latch (P1OUT7~4) that displays the seven segment LED1 is set to '0001'. Also, the display data ('1') is set in the port 1 output latch (P1OUT3~0).

P1OUT: x'00FE64'

7	6	5	4	3	2	1	0
P1OUT7	P1OUT6	P1OUT5	P1OUT4	P1OUT3	P1OUT2	P1OUT1	P1OUT0
0	0	0	0	0	0	0	1

- (5) Display data ('2'), to be output at the initial synchronous output transition timing, is set.

SYBUF: x'00FE62'

7	6	5	4	3	2	1	0
SYB BF3	SYB BF2	SYB BF1	SYB BF0	SYA BF3	SYA BF2	SYA BF1	SYA BF0
0	0	0	0	0	0	1	0

- (6) The timer 1 interrupt is enabled and timer 1 is activated. Every time that underflow of timer 1 occurs, the selected pattern for the seven segment LED will change. At the same time, a timer 1 interrupt is generated.
- (7) After the interrupt is determined and processed, the next data ('3') to be displayed by the seven segment LED is set in SYSBUF. Thereafter, whenever an interrupt is processed, display data is reset in the order of '4', '1', '2', '3', etc.



The contents of SYBBF3~0 are ignored.

7-Segment LED Display

Registe/ Output	SYB	P1OUT 7~4	P1OUT 3~0	SYBBF 3~0	SYABF 3~0	Display
Initial Setting	0001	0001	0001	0010	0010	1
1st	0010				0011	2
2nd	0100				0100	3
3rd	1000				0001	4
4th	0001				0010	1
5th	0010				0011	2

Blank areas must be set by the software.

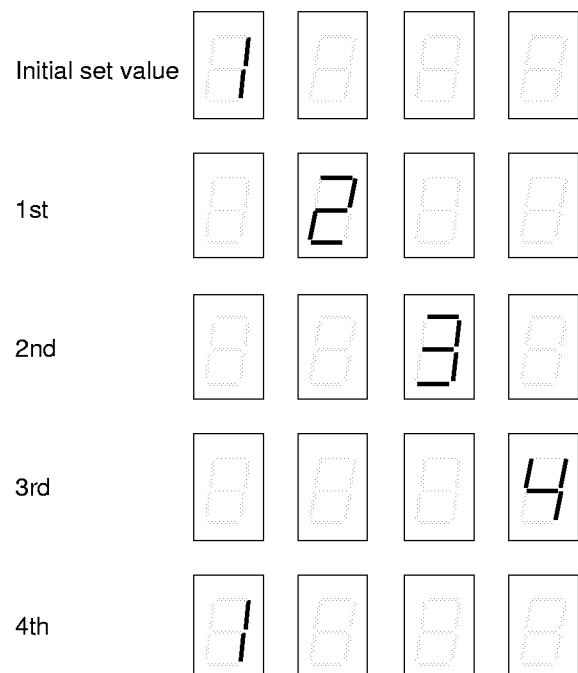


Figure 7-2-7 Seven Segment LED Display

Chapter 8 DMA Functions

8

8-1 DMA Function Summary

8-1-1 Overview

DMA (Direct Memory Access) functions bypass the CPU to enable high speed data transfers between memory and memory, memory and internal I/O, or memory and external devices.

There are 8 channels for DMA data transfer. Each channel can individually perform data transfers between memory and I/O. Two channels used as a pair can perform memory-to-memory transfers. Transfer of an 8-bit byte or 16-bit word with no wait states takes, depending on the source-destination combination, either one bus/machine cycle (100 ns for a 20-MHz oscillator) or two. The chip boosts system response by accepting interrupts during burst mode transfers.

8-1-2 Starting Factors

There are four ways to initiate a DMA transfer: internal interrupt, external interrupt from a pin, external request, and software. Each channel can have only one starting factor.

Table 8-1-1 DMA Starting Factors

Internal Interrupt	Interrupts that may be used include the end of analog-to-digital conversion interrupt, serial interface interrupts, and timer interrupts.
External Interrupt	These are the external interrupts from the pins $\overline{\text{IRQ}0}$ ~ $\overline{\text{IRQ}3}$.
External Request	This type of transfer starts with a DMA request ($\overline{\text{DMAREQ}}$) signal from the external device. There are request pins for two such devices.
Software	Setting a bit in the control registers initiates the transfer. The transfer continues until the value of the transfer word count register reaches 0.

8-1-3 Transfer Types

There are four transfer types based on the source-destination combination: between memory and an onboard I/O device, between memory and memory, between memory and an external device (type 1), and between memory and an external device (type 2).

Either pulse output or level output can be selected for the DMAACKn signal.

- Edge operation

This mode features handshaking using the DMAREQ and DMAACK lines.

[☞ 8-2-5]

- Level Operation

The transfer is performed while the DMAREQn signal is at a 'L' level. [☞ 8-2-4]

1. Between Memory and Onboard I/O Device (2 bus cycles)

This type transfers data between memory and an onboard I/O device. Settings are for individual channels. [☞ 8-2-1]

2. Between Memory and Memory (2 bus cycles)

This type transfers data between two memory locations. Two channels are used together as a pair. The transfer uses one of the following channel pairs: 0-1, 2-3, 4-5, or 6-7. [☞ 8-2-3]

3. Between Memory and External Device (Type 1)

This type transfers data between memory and an external device in a single bus cycle.

- From memory to external device [☞ 8-2-4]

The chip simultaneously accesses the source address, reading the data onto the bus, issues a DMAACK to the destination device, and writes the bus data to the destination.

- From external device to memory [☞ 8-2-5]

An external device at the source is accessed by the DMAACKn signal. At the same time as data is output on the bus, the destination address is accessed and the bus data is stored in memory.

4. Between Memory and External Device (Type 2)

This type transfers data between memory and an external device in two bus cycles. [☞ 8-2-6]



In a 2-bus-cycle DMA transfer, data is read from the source during a read cycle, and data is written to the destination during a write cycle.



For level operation, do not terminate without verifying whether a DMA transfer has been initiated.



The destination cannot include the DMAC registers (x'00FE80~x'00FEFF).



The two sides must, however, use the same bus mode.





For transfers between memory and external device 1, both sides must use the same bus mode.

8-1-4 Addressing and Bus Modes

There are three addressing modes for transfers: fixed, with increment, and with decrement. There are separate specifications for source and destination. There are two bus modes: 8- and 16-bit. It is also possible to transfer data between memory using different bus modes.

For word transfers the memory using the 8-bit bus mode must have an even address if the addressing mode is with increment and an odd one if the addressing mode is with decrement.

Table 8-1-2 Relation between Addressing Mode and the Leading Address for Memory Word Transfers during 8-bit Bus Mode

Addressing Mode	Leading Address
Increment	Even
Decrement	Odd
Fixed	—

8-1-5 Transfer Methods

There are two transfer methods : normal and continue.

- Normal method

This mode performs the number of transfers set in the DMAn transfer count register (DMnCNT). DMnCNT is decremented every transfer. The transfer terminates when DMnCNT reaches 0.

- Continue method

This is for repeating a data transfer between memory and an onboard I/O device. Although this mode involves transfers between memory and I/O, two channels are used together as a pair. The single-word transfer mode is used. The DMnCNT for the even channel is decremented every transfer. When the number of transfers set in DMnCNT reaches 0, the first transfer address and number of transfers set for the odd channel are read into the even channel, and the transfer is continued. Transfer is terminated by setting the execution enable flag of the DMAn control register to 0.

[☞ 8-2-2]

8-1-6 Transfer Direction

The transfer direction can be arbitrarily specified for any of the devices, the source, or destination.

8-1-7 Transfer Modes

There are two transfer modes: single-word and burst.

- Single-word mode

This mode releases the bus after each unit transfer. As a result, the controller transfers only one unit per DMA request and does not regain the bus until the next $\overline{\text{DMAREQ}}$ signal. [8-2-1]

- Burst mode

This mode does not release the bus after each unit transfer. Interrupts with priority levels higher than that for the burst interrupt are, however, accepted, and the burst mode transfer continues once they have been processed. [8-2-5, 8-2-6]

8-1-8 Transfer Units

Transfers offer a choice of two unit sizes: 8 (bytes) or 16 (words) bits.

8-1-9 Interrupts

An interrupt can be generated when the DMA transfer is complete. Whether or not an interrupt is issued is set by the DMA_n control register.

8-1-10 Channel Priority

Priority decreases with channel number.

During a burst DMA transfer, transfer requests for another channel will not be accepted until the transfer is completed (until the transfer count reaches 0). During a single-word DMA transfer, transfer requests with higher priority can be received every time a single-word is transferred and the execution channel will be switched.

8-1-11 Forcing Termination

Pull the DMAEND pin to a 'H' level to force termination of the currently executing DMA transfer and pending DMA transfers. By pulling the DMAEND pin to a high level, all currently executing and pending DMA transfers can be terminated.

This pin should normally be kept LOW.

Termination with this procedure invalidates the contents of all DMA registers. They must be reset.



Do not pull the DMAEND pin to a 'H' level during execution of a transfer between memory and I/O.

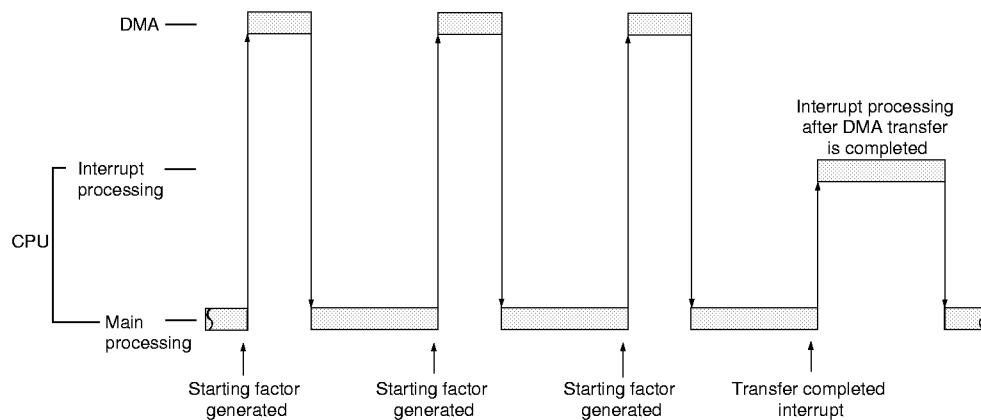


Figure 8-1-1 Single-word Transfer Mode

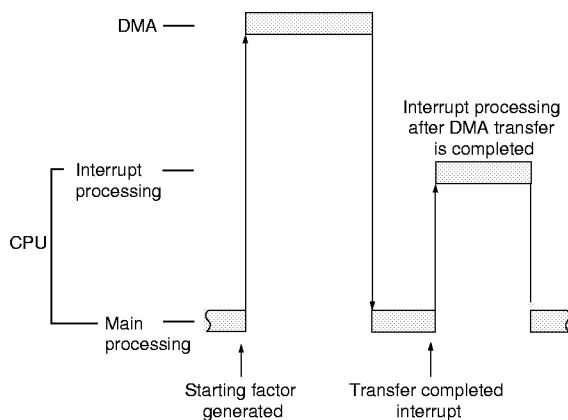


Figure 8-1-2 Burst Transfer Mode (when not terminated by an interrupt)

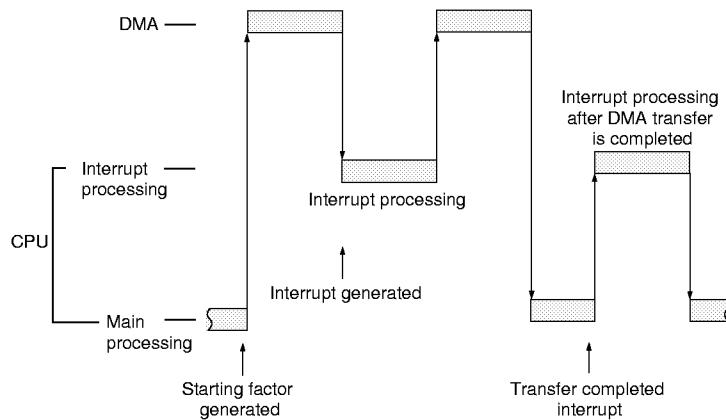


Figure 8-1-3 Burst Transfer Mode (when terminated by an interrupt)

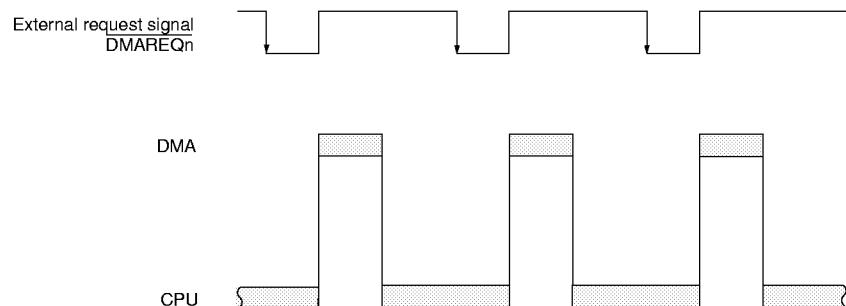


Figure 8-1-4 External Request Edge Factor (single-word transfer mode)

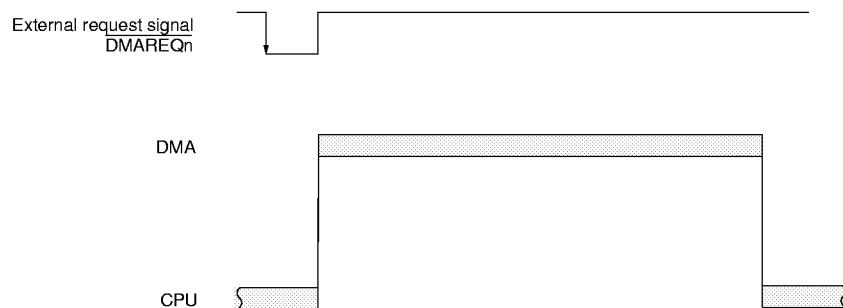


Figure 8-1-5 External Request Edge Factor (burst mode)



Before terminating a DMA transfer that was requested by an external request level factor, verify whether the transfer has been initiated. Each external request level factor can initiate one DMA transfer per channel.

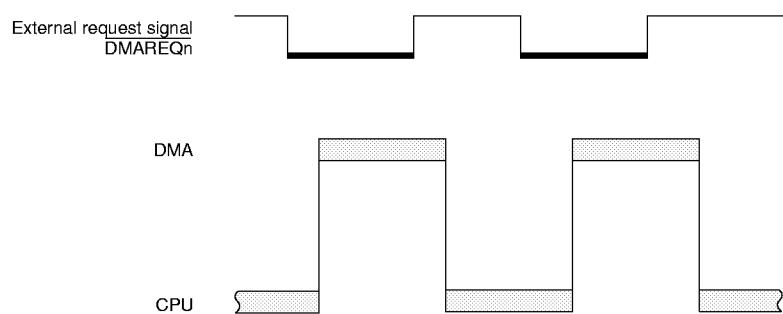


Figure 8-1-6 External Request Level Factor

8-1-12 Control Registers

Each channel contains the following DMA control registers.

- DMA_n Control Registers (DM_nCTR)
- DMA_n Transfer Count Registers (DM_nCNTL, DM_nCNH)
- DMA_n Transfer Address Pointers (DM_nTAPL, DM_nTAPH)
- DMA_n Internal Address Pointers (DM_nIAPR)
- DMA_n Burst Interrupt Registers (DM_nBIR)

Table 8-1-3 DMA Function Control Register List (1/2)

	Register Name	Register Symbol: Address
DMA channel 0 register	DMA0 transfer address pointer (lower 16 bits) DMA0 transfer address pointer (upper 8 bits) DMA0 transfer count register (lower 16 bits) DMA0 transfer count register (upper 8 bits) DMA0 internal address pointer DMA0 control register DMA0 burst interrupt register	DM0TAPL: x'00FE80' DM0TAPH: x'00FE82' DM0CNTL: x'00FE84' DM0CNTH: x'00FE86' DM0IAPR: x'00FE88' DM0CTR: x'00FE8A' DM0BIR: x'00FE8C'
DMA channel 1 register	DMA1 transfer address pointer (lower 16 bits) DMA1 transfer address pointer (upper 8 bits) DMA1 transfer count register (lower 16 bits) DMA1 transfer count register (upper 8 bits) DMA1 internal address pointer DMA1 control register DMA1 burst interrupt register	DM1TAPL: x'00FE90' DM1TAPH: x'00FE92' DM1CNTL: x'00FE94' DM1CNTH: x'00FE96' DM1IAPR: x'00FE98' DM1CTR: x'00FE9A' DM1BIR: x'00FE9C'
DMA channel 2 register	DMA2 transfer address pointer (lower 16 bits) DMA2 transfer address pointer (upper 8 bits) DMA2 transfer count register (lower 16 bits) DMA2 transfer count register (upper 8 bits) DMA2 internal address pointer DMA2 control register DMA2 burst interrupt register	DM2TAPL: x'00FEA0' DM2TAPH: x'00FEA2' DM2CNTL: x'00FEA4' DM2CNTH: x'00FEA6' DM2IAPR: x'00FEA8' DM2CTR: x'00FEAA' DM2BIR: x'00FEAC'
DMA channel 3 register	DMA3 transfer address pointer (lower 16 bits) DMA3 transfer address pointer (upper 8 bits) DMA3 transfer count register (lower 16 bits) DMA3 transfer count register (upper 8 bits) DMA3 internal address pointer DMA3 control register DMA3 burst interrupt register	DM3TAPL: x'00FEB0' DM3TAPH: x'00FEB2' DM3CNTL: x'00FEB4' DM3CNTH: x'00FEB6' DM3IAPR: x'00FEB8' DM3CTR: x'00FEBA' DM3BIR: x'00FEBC'

Table 8-1-3 DMA Function Control Register List (2/2)

DMA channel 4 register	DMA4 transfer address pointer (lower 16 bits) DMA4 transfer address pointer (upper 8 bits) DMA4 transfer count register (lower 16 bits) DMA4 transfer count register (upper 8 bits) DMA4 internal address pointer DMA4 control register DMA4 burst interrupt register	DM4TAPL: x'00FEC0' DM4TAPH: x'00FEC2' DM4CNTL: x'00FEC4' DM4CNTH: x'00FEC6' DM4IAPR: x'00FEC8' DM4CTR: x'00FECA' DM4BIR: x'00FECC'
DMA channel 5 register	DMA5 transfer address pointer (lower 16 bits) DMA5 transfer address pointer (upper 8 bits) DMA5 transfer count register (lower 16 bits) DMA5 transfer count register (upper 8 bits) DMA5 internal address pointer DMA5 control register DMA5 burst interrupt register	DM5TAPL: x'00FED0' DM5TAPH: x'00FED2' DM5CNTL: x'00FED4' DM5CNTH: x'00FED6' DM5IAPR: x'00FED8' DM5CTR: x'00FEDA' DM5BIR: x'00FEDC'
DMA channel 6 register	DMA6 transfer address pointer (lower 16 bits) DMA6 transfer address pointer (upper 8 bits) DMA6 transfer count register (lower 16 bits) DMA6 transfer count register (upper 8 bits) DMA6 internal address pointer DMA6 control register DMA6 burst interrupt register	DM6TAPL: x'00FEE0' DM6TAPH: x'00FEE2' DM6CNTL: x'00FEE4' DM6CNTH: x'00FEE6' DM6IAPR: x'00FEE8' DM6CTR: x'00FEFA' DM6BIR: x'00FEFC'
DMA channel 7 register	DMA7 transfer address pointer (lower 16 bits) DMA7 transfer address pointer (upper 8 bits) DMA7 transfer count register (lower 16 bits) DMA7 transfer count register (upper 8 bits) DMA7 internal address pointer DMA7 control register DMA7 burst interrupt register	DM7TAPL: x'00FEF0' DM7TAPH: x'00FEF2' DM7CNTL: x'00FEF4' DM7CNTH: x'00FEF6' DM7IAPR: x'00FEF8' DM7CTR: x'00FEFA' DM7BIR: x'00FEFC'

The DMA_n control registers (DM_nCTR) select the operation control conditions (starting factor, transfer configuration, transfer method, transfer mode, transfer units, etc.) for DMA.

The DMA_n transfer count registers (DM_nCNTL, DM_nCNTH) set the number of transfers. Every time there is a transfer, the contents of these registers are decremented by one. The transfer is complete when the value 0 is reached.

The DMA_n transfer address pointers (DM_nTAPL, DM_nTAPH) set the transfer address.

The DMA_n internal address pointers (DM_nIAPR) set the internal I/O address.

The DMA_n burst interrupt registers (DM_nBIR) set the interrupt level during burst transfers.

8-2 DMA Function Setting Example

8-2-1 A/D Reception

After completion of A/D conversion (ch0), the contents of the conversion data buffer are automatically transferred to memory. After 5 transfers, a transfer complete interrupt is generated and the interrupt routine is processed by the software. The transfer destination address is x'AAAAAA0'.

■ Analog Interface Settings

If the A/D interrupt is enabled, an A/D transfer interrupt will be generated after each DMA transfer.

- (1) The A/D conversion interrupt is disabled. ADIE of G10ICR (x'00FC54') is set to '0'.
- (2) The A/D conversion mode is set. Refer to section 6-2, "Analog Interface Setting Examples" for further details.

■ DMA Settings

- (3) The DMA0 internal address pointer (DM0IAPR) is set to the lower 10 bits (x'3A8') of the AN0BUF address (x'00FDA8').

DM0IAPR: x'00FE8A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	DMA0 IO9	DMA0 IO8	DMA0 IO7	DMA0 IO6	DMA0 IO5	DMA0 IO4	DMA0 IO3	DMA0 IO2	DMA0 IO1	DMA0 IO0
1	1	1	1	0	1	0	1	1	0	1	0	1	0	0	0

- (4) The DMA0 transfer address pointer (DM0TAP) is set to the first memory address (x'AAAAAA0') where A/D conversion result data will be transferred.

DM0TAPL, DM0TAPH: x'00FE80', x'00FE82'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0 AR15	DMA0 AR14	DMA0 AR13	DMA0 AR12	DMA0 AR11	DMA0 AR10	DMA0 AR9	DMA0 AR8	DMA0 AR7	DMA0 AR6	DMA0 AR5	DMA0 AR4	DMA0 AR3	DMA0 AR2	DMA0 AR1	DMA0 AR0
1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	DMA0 AR23	DMA0 AR22	DMA0 AR21	DMA0 AR20	DMA0 AR19	DMA0 AR18	DMA0 AR17	DMA0 AR16
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

- (5) The DMA0 transfer count register (DM0CNT) is set to the number of transfers for automatic transmission. In this example, a value of 5 is set for 5 transfers.

DM0CNTL, DM0CNTH: x'00FE84', x'00FE86'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0															
CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	DMA0							
								CT23	CT22	CT21	CT20	CT19	CT18	CT17	CT16
								0	0	0	0	0	0	0	0

- (6) The DMA0 control register (DM0CTR) is set to the transfer parameters. A/D conversion completion is selected as the starting factor. Transfer between memory and internal I/O (M-I/O) is selected as the transfer configuration. INC is selected for transfer addressing so that the destination pointer will be incremented. The transfer method is normal. Since the destination is memory, destination is selected as the transfer direction. The transfer mode is set to single-word transfers. The unit for transfers is set to one-byte units. Interrupt generation selection is set to generate. Execute enable is set to disabled. Other parameters do not affect operation.

DM0CTR: x'00FE8A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0															
EN	IT	UT	MD	SD	MT	AD1	AD0	ACK	ST1	ST0	BG4	BG3	BG2	BG1	BG0
0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1

- (7) Execute enable of the DM0CTR is set to enable. Other parameters are set with the same values as in procedure (6).

DM0CTR: x'00FE8A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0															
EN	IT	UT	MD	SD	MT	AD1	AD0	ACK	ST1	ST0	BG4	BG3	BG2	BG1	BG0
1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1

- (8) DMA channel 0 interrupts are enabled.

G6ICR: x'00FC4C'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	DMA														
	LV2	LV1	LV0	3IE	2IE	1IE	0IE	3IR	2IR	1IR	0IR	3ID	2ID	1ID	0ID
—	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

With the above settings, when A/D conversion is completed, the results will automatically be transferred to memory. When the set number of transfers are performed, a DMA transfer complete interrupt will be generated and processed.

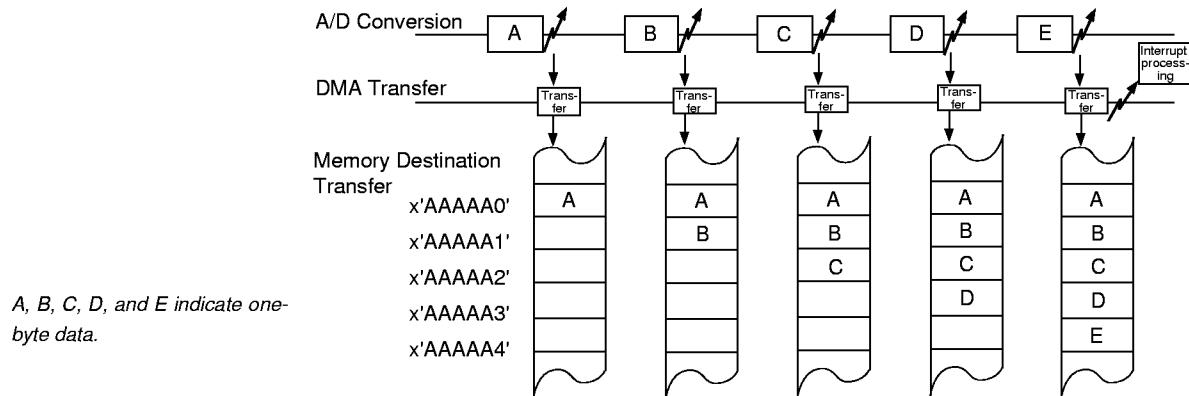


Figure 8-2-1 Transfer of Data Received from A/D Converter

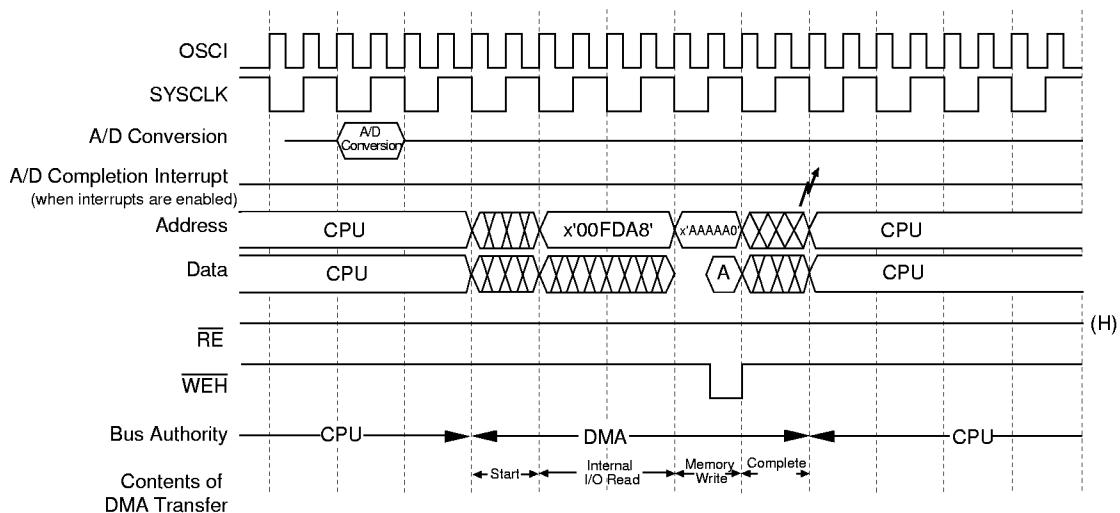


Figure 8-2-2 Timing Chart of Bus Cycle during Single-word Transfer
(internal I/O → 8-bit bus mode memory, no wait)

8-2-2 Serial Reception

Using the continue mode, every 5 bytes of data received by the serial interface is transferred to the same memory address. After 5 bytes has been transferred, a transfer completion interrupt is generated and processed by the software. The continue mode is used to repeat single-word transfers from an arbitrary address for an arbitrary number of transfers. Even though an even channel is used, it is necessary to also set the transfer address and number of transfers for the odd channel that makes up the pair (0-1, 2-3, 4-5, 6-7). If the transfer count for the channel in use reaches zero, initialization values are read from the odd channel and the transfer is continued.



Two channels are used as pair in the continue mode.

If the serial reception interrupt is enabled, a serial reception interrupt will be generated after each DMA transfer.

■ Serial Interface Settings

- (1) The serial reception interrupt is disabled. SIR0IE of G9ICR (x'00FC52') is set to '0'.
- (2) The serial interface reception mode is set. Refer to section 5-2, "Example Serial Interface Settings" for further details.

■ DMA Settings

- (3) The DMA0 internal address pointer (DM0IAPR) is set to the lower 10 bits (x'382') of the serial 0 transmit/receive buffer address (x'00FD82').

DM0IAPR: x'00FE8A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	DMA0 IO9	DMA0 IO8	DMA0 IO7	DMA0 IO6	DMA0 IO5	DMA0 IO4	DMA0 IO3	DMA0 IO2	DMA0 IO1	DMA0 IO0

1 1 1 0 0 0 0 0 0 0 0 0 0 1 0

- (4) The first memory address (x'007000') that will receive serial data is set. The DMA transfer address pointers for both execution channel 0 (DMA0TAP) and its pair, odd channel 1 (DM1TAP) are set.

DM1TAPL and DM1TAPH are both set to the same value.

DM0TAPL, DM0TAPH: x'00FE80', x'00FE82'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0 AR15	DMA0 AR14	DMA0 AR13	DMA0 AR12	DMA0 AR11	DMA0 AR10	DMA0 AR9	DMA0 AR8	DMA0 AR7	DMA0 AR6	DMA0 AR5	DMA0 AR4	DMA0 AR3	DMA0 AR2	DMA0 AR1	DMA0 AR0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	DMA0 AR23	DMA0 AR22	DMA0 AR21	DMA0 AR20	DMA0 AR19	DMA0 AR18	DMA0 AR17	DMA0 AR16

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

- (5) The DMA0 transfer count register (DM0CNT) and the DMA1 transfer count register (DM1CNT) are set to the number of transfers for automatic transmission. In this example, a value of 5 is set for 5 transfers.

DM0CNTL, DM0CNTH: x'00FE84', x'00FE86'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0															
CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	DMA0							
								CT23	CT22	CT21	CT20	CT19	CT18	CT17	CT16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- (6) The DMA0 control register (DM0CTR) is set to the transfer parameters. Serial 0 reception is selected as the starting factor. Transfer between memory and internal I/O (M-I/O) is selected as the transfer configuration. Since the destination pointer will be incremented, INC is selected for transfer addressing. The transfer method is continue. Since the destination is memory, destination is selected as the transfer direction. The transfer mode is set to single-word transfers. The unit for transfers is set to one-byte units. Interrupt generation selection is set to generate. Execute enable is set to disabled. Other parameters do not affect operation.

DM0CTR: x'00FE8A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0															
EN	IT	UT	MD	SD	MT	AD1	AD0	ACK	ST1	ST0	BG4	BG3	BG2	BG1	BG0
0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1

- (7) Execute enable of the DM0CTR is set to enable. Other parameters are set with the same values as in procedure (6).

DM0CTR: x'00FE8A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0															
EN	IT	UT	MD	SD	MT	AD1	AD0	ACK	ST1	ST0	BG4	BG3	BG2	BG1	BG0
1	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1

- (8) DMA channel 0 interrupts are enabled.

G6ICR: x'00FC4C'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	DMA														
	LV2	LV1	LV0	3IE	2IE	1IE	0IE	3IR	2IR	1IR	0IR	3ID	2ID	1ID	0ID
—	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0

In the same manner as for the transfer address, a two channel pair is also set for the number of transfers. DM1CNTL and DM1CNTH are both set to the same value.

With the above settings, when serial reception occurs, the received data will automatically be transferred to memory.

With the continue mode, when the set number of transfers are completed (when DM0CNT becomes 0), DM0TAP and DM0CNT are reset with the values of DM1TAP and DM1CNT.

In this example, errors cannot be detected during transfer. If error detection is necessary, SC0TRB and SC0STR are transmit. DMAOUT of DM0CTR is set to 0 to achieve word transfers. In this case, a memory area of 5 words (10 bytes) is required. During an interrupt processing routine, by checking the contents of SC0STR, that was transferred to memory, the status of each reception can be verified.

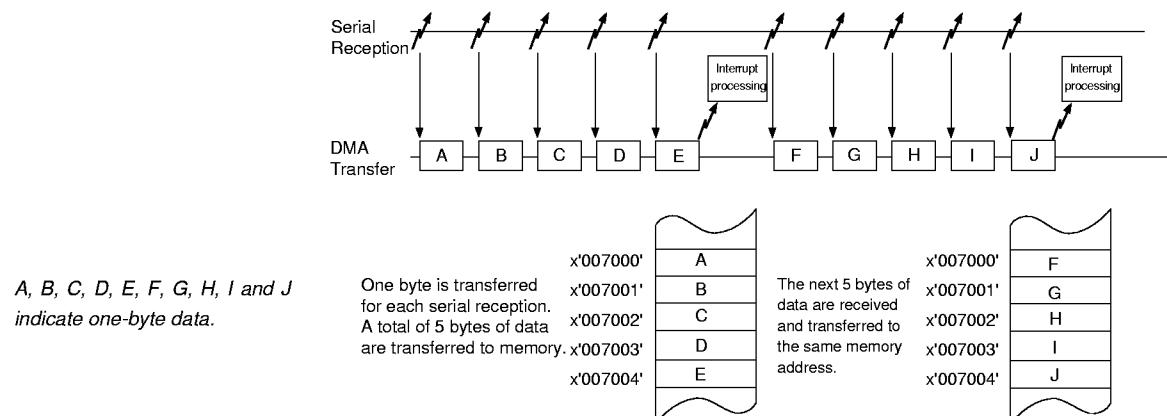


Figure 8-2-3 Transfer of Received Serial Data

8-2-3 Memory-Memory Transfer

8-bit bus mode memory data is transferred to 16-bit bus mode memory in a burst transfer. In this example, 3 words from memory address x'500000' are transferred to memory address x'A00000'.



Two channels are used as a pair in a memory-mem transfer.



If 8-bit bus mode memory data is used in word transfers, set the first address to an even address.

■ DMA Settings

- The DMA0 transfer address pointer (DM0TAP) is set to the first address x'500000' of the transfer source.

DM0TAPL, DM0TAPH: x'00FE80', x'00FE82'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0															
AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	DMA0							
—	—	—	—	—	—	—	—	AR23	AR22	AR21	AR20	AR19	AR18	AR17	AR16
0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0

- The DMA1 transfer address pointer (DM1TAP) is set to the first address x'A00000' of the transfer destination.

DM1TAPL, DM1TAPH: x'00FE90', x'00FE92'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA1															
AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	DMA1							
—	—	—	—	—	—	—	—	AR23	AR22	AR21	AR20	AR19	AR18	AR17	AR16
1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0

- The number of transfers is set. Since 3 words are to be transferred, the DMA0 transfer count register (DM0CNT) is set to '3'.

DM0CNTL, DM0CNTH: x'00FE84', x'00FE86'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0															
CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	DMA0							
—	—	—	—	—	—	—	—	CT23	CT22	CT21	CT20	CT19	CT18	CT17	CT16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- (4) The DMA1 control register (DM1CTR) is set to the transfer destination parameters. Since the destination pointer will be incremented, INC is selected for transfer addressing. Destination is selected as the transfer direction. Execute enable is set to disabled. Other parameters do not affect operation.

DM1CTR: x'00FE9A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA1 EN	DMA1 IT	DMA1 UT	DMA1 MD	DMA1 SD	DMA1 MT	DMA1 AD1	DMA1 AD0	DMA1 ACK	DMA1 ST1	DMA1 ST0	DMA1 BG4	DMA1 BG3	DMA1 BG2	DMA1 BG1	DMA1 BG0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

- (5) The DMA0 control register (DM0CTR) is set to the transfer source parameters. Software is selected as the starting factor. M-M is selected as the transfer configuration. Since the source pointer will be incremented, INC is selected for transfer addressing. The transfer method is normal. Source is selected as the transfer direction. The transfer mode is set to burst transfers. The unit for transfers is set to one word units. Interrupt generation selection is selected as not generated. Execute enable is set to disabled. Other parameters do not affect operation.

DM0CTR: x'00FE8A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0 EN	DMA0 IT	DMA0 UT	DMA0 MD	DMA0 SD	DMA0 MT	DMA0 AD1	DMA0 AD0	DMA0 ACK	DMA0 ST1	DMA0 ST0	DMA0 BG4	DMA0 BG3	DMA0 BG2	DMA0 BG1	DMA0 BG0
0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0

- (6) Execute enable of the DM0CTR is set to enable. Other parameters are set with the same values as in procedure (5).

DM0CTR: x'00FE8A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0 EN	DMA0 IT	DMA0 UT	DMA0 MD	DMA0 SD	DMA0 MT	DMA0 AD1	DMA0 AD0	DMA0 ACK	DMA0 ST1	DMA0 ST0	DMA0 BG4	DMA0 BG3	DMA0 BG2	DMA0 BG1	DMA0 BG0
1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Since activated by the software, the transfer begins automatically after the registers are set.

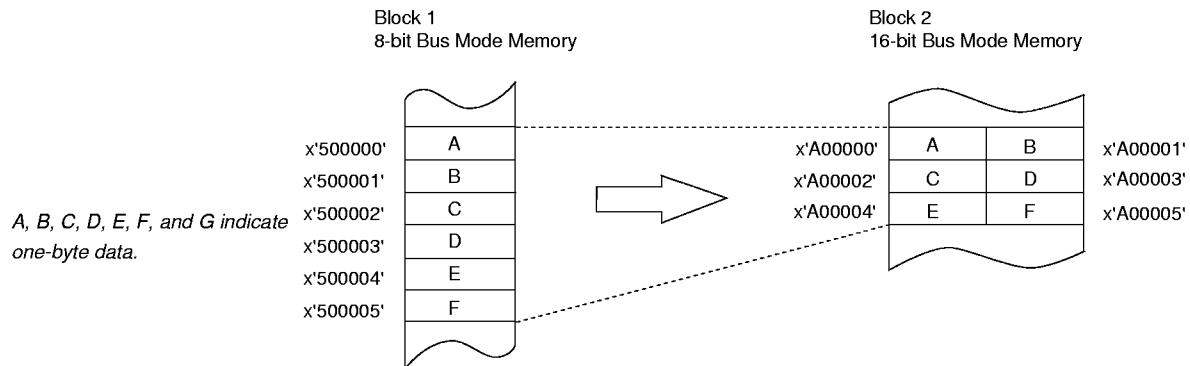


Figure 8-2-4 Memory-Memory Data Transfer

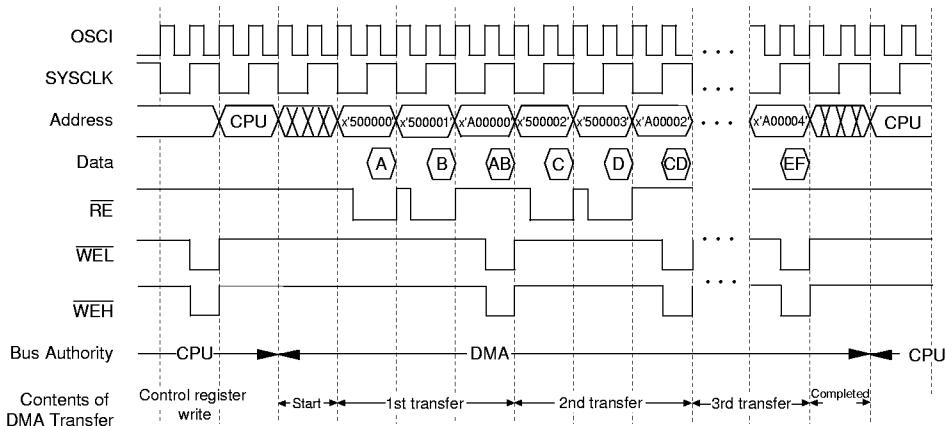


Figure 8-2-5 Timing Chart of DMA Transfer Bus Cycle (8-bit bus mode memory, no wait → 16-bit bus mode memory, no wait)

8-2-4 Transfer from Memory to External Device

8 bytes of memory data are written to an external device. In response to the external request signal DMAREQ0, a burst transfer is performed in one bus cycle. Interrupts of level 2 or higher are accepted and processed during the burst transfer.

■ DMA Settings

- (1) The DMA0 transfer address pointer (DM0TAP) is set to the first address x'C00000' of the transfer source.

DM0TAPL, DM0TAPH: x'00FE80', x'00FE82'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0 AR15	DMA0 AR14	DMA0 AR13	DMA0 AR12	DMA0 AR11	DMA0 AR10	DMA0 AR9	DMA0 AR8	DMA0 AR7	DMA0 AR6	DMA0 AR5	DMA0 AR4	DMA0 AR3	DMA0 AR2	DMA0 AR1	DMA0 AR0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	DMA0 AR23	DMA0 AR22	DMA0 AR21	DMA0 AR20	DMA0 AR19	DMA0 AR18	DMA0 AR17	DMA0 AR16
0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

- (2) The number of transfers is set. Since 8 bytes are to be transferred, the DMA0 transfer count register (DM0CNT) is set to '8'.

DM0CNTL, DM0CNTH: x'00FE84', x'00FE86'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0 CT15	DMA0 CT14	DMA0 CT13	DMA0 CT12	DMA0 CT11	DMA0 CT10	DMA0 CT9	DMA0 CT8	DMA0 CT7	DMA0 CT6	DMA0 CT5	DMA0 CT4	DMA0 CT3	DMA0 CT2	DMA0 CT1	DMA0 CT0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	DMA0 CT23	DMA0 CT22	DMA0 CT21	DMA0 CT20	DMA0 CT19	DMA0 CT18	DMA0 CT17	DMA0 CT16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- (3) The DMA0 burst interrupt register (DM0BIR) is set to the interrupt level to terminate a burst transfer. In this example a value of '3' is set. If a higher level interrupt (0~2) is generated, the burst transfer will be terminated and the interrupt processed.

DM0BIR: x'00FE8C'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	—	—	—	—	—	DMA0 BR2	DMA0 BR1	DMA0 BR0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

(4) The interrupt level is set for those interrupts that are necessary to accept even during a burst transfer. In this example, the interrupt level for external interrupts is set to '2'. [☞ 3-3-1]

(5) The DMA0 control register (DM0CTR) is set to the transfer source parameters. External request 0 level is selected as the starting factor. Transfer between memory and external device 1 is selected as the transfer configuration. Level is selected as the ACK output. Since "level" is selected, the DMAACK0 output will be at the 'L' level while valid addresses are being output during a DMA transfer. INC is selected for transfer addressing so that the source pointer will be incremented. The transfer method is normal and source is selected as the transfer direction. The transfer mode is set to burst. The unit for transfers is set to one-byte units. Interrupt generation selection is set as not generated. Execute enable is set to disabled. Other parameters do not affect operation.

DM0CTR: x'00FE8A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0 EN	DMA0 IT	DMA0 UT	DMA0 MD	DMA0 SD	DMA0 MT	DMA0 AD1	DMA0 AD0	DMA0 ACK	DMA0 ST1	DMA0 ST0	DMA0 BG4	DMA0 BG3	DMA0 BG2	DMA0 BG1	DMA0 BG0
0	1	1	0	0	0	0	0	1	1	0	1	1	1	1	0

(6) Execute enable of the DM0CTR is set to enable. Other parameters are set with the same values as in procedure (5).

DM0CTR: x'00FE8A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0 EN	DMA0 IT	DMA0 UT	DMA0 MD	DMA0 SD	DMA0 MT	DMA0 AD1	DMA0 AD0	DMA0 ACK	DMA0 ST1	DMA0 ST0	DMA0 BG4	DMA0 BG3	DMA0 BG2	DMA0 BG1	DMA0 BG0
1	1	1	0	0	0	0	0	1	1	0	1	1	1	1	0

Since activated by the external request level, the transfer begins after register setting, when the external request signal DMAREQ0 goes to a 'L' level.

(7) When an external interrupt is generated, the DMA transfer is terminated and the interrupt processed.

Upon completion of the interrupt processing, the remaining DMA transfer is executed. After performing the set number of transfers, control of the bus is returned to the CPU and the transfer is complete.

A, B, C, D, E, F, G, and H indicate one-byte data.

If an interrupt with a higher level than DM0BIR is generated during a burst transfer of 8 bytes of data to an external device, the transfer is terminated and the interrupt processed. The DMA transfer resumes after interrupt processing is complete.

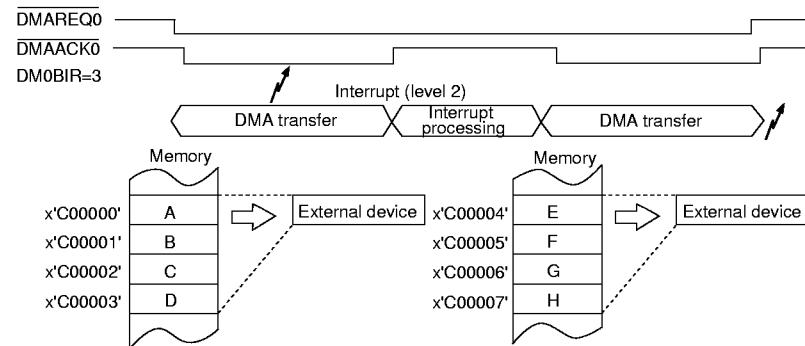


Figure 8-2-6 Burst Transfer from Memory to External Device

and Interrupt Processing

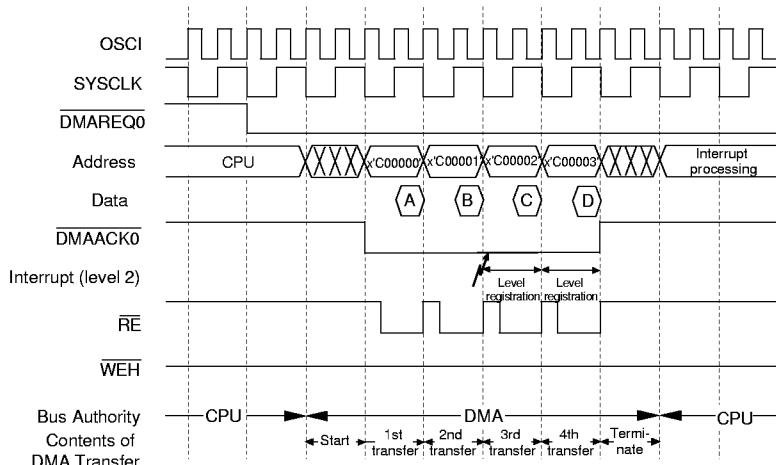


Figure 8-2-7 Timing Chart of DMA Transfer Bus Cycle

(8-bit bus mode memory → 8-bit bus mode external device)

8-2-5 Transfer from External Device to Memory

Three bytes of data from an external device are written to memory (x'C00000'~). The burst transfer, initiated by the external request signal DMAREQ0, is performed in one bus cycle.

■ DMA Settings

- (1) The DMA0 transfer address pointer (DM0TAP) is set to the first address in memory x'C00000' of the transfer destination.

DM0TAPL, DM0TAPH: x'00FE80', x'00FE82'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0															
AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	DMA0							
—	—	—	—	—	—	—	—	AR23	AR22	AR21	AR20	AR19	AR18	AR17	AR16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- (2) The number of transfers is set. Since 3 bytes are to be transferred, the DMA0 transfer count register (DM0CNT) is set to '3'.

DM0CNTL, DM0CNTH: x'00FE84', x'00FE86'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0															
CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	DMA0							
—	—	—	—	—	—	—	—	CT23	CT22	CT21	CT20	CT19	CT18	CT17	CT16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- (3) The DMA0 control register (DM0CTR) is set to the transfer destination parameters. External request 0 edge is selected as the starting factor. Transfer between memory and external device 1 is selected as the transfer configuration. Pulse is selected as the ACK output. INC is selected for transfer addressing so that the destination pointer will be incremented. The transfer method is normal and destination is selected as the transfer direction. The transfer mode is set to burst. The unit for transfers is set to one-byte units. Interrupt generation selection is set as not generated. Execute enable is set to disabled. Other parameters do not affect operation.

DM0CTR: x'00FE8A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0 EN	DMA0 IT	DMA0 UT	DMA0 MD	DMA0 SD	DMA0 MT	DMA0 AD1	DMA0 AD0	DMA0 ACK	DMA0 ST1	DMA0 ST0	DMA0 BG4	DMA0 BG3	DMA0 BG2	DMA0 BG1	DMA0 BG0
0	1	1	0	1	0	0	0	0	1	0	1	1	1	0	0

- (4) Execute enable of the DM0CTR is set to enable. Other parameters are set with the same values as in procedure (3).

DM0CTR: x'00FE8A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0 EN	DMA0 IT	DMA0 UT	DMA0 MD	DMA0 SD	DMA0 MT	DMA0 AD1	DMA0 AD0	DMA0 ACK	DMA0 ST1	DMA0 ST0	DMA0 BG4	DMA0 BG3	DMA0 BG2	DMA0 BG1	DMA0 BG0
1	1	1	0	1	0	0	0	0	1	0	1	1	1	0	0

After register setting, the transfer begins when a negative edge is input to external request signal DMAREQ0. After the set number of transfers are repeated, control of the bus is returned to the CPU and the transfer is complete.

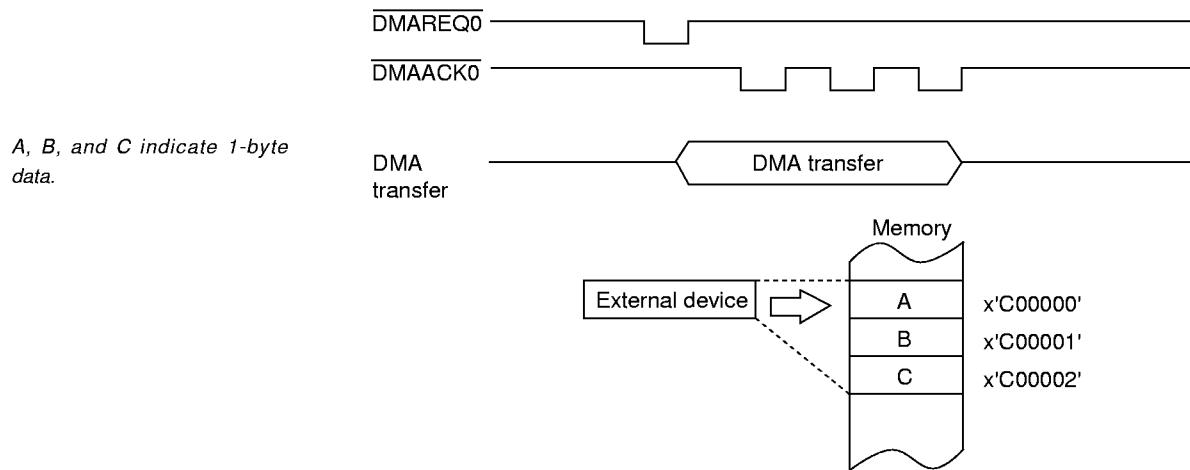


Figure 8-2-8 Data Transfer from External Device to Memory

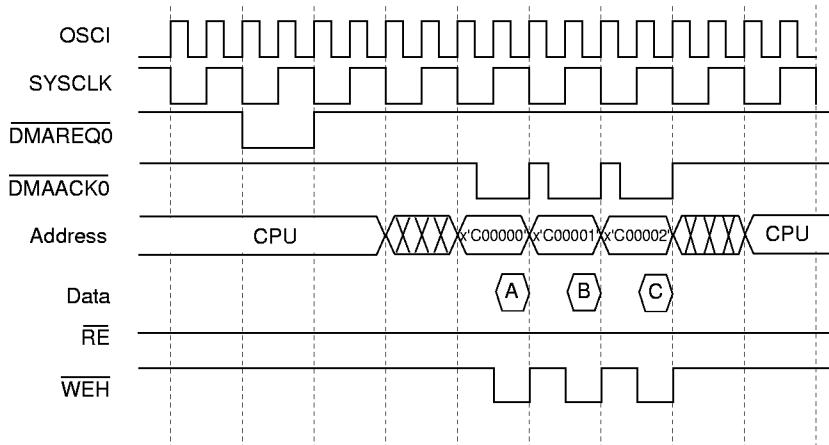


Figure 8-2-9 Timing Chart of DMA Transfer Bus Cycle (8-bit bus mode
external device → 8-bit bus mode memory, edge mode, burst)

8-2-6 Transfer from 16-bit Memory to 8-bit External Device

Five words of 16-bit bus mode memory data are written to an 8-bit bus mode external device. The burst transfer, initiated by the external request signal $\overline{\text{DMAREQ}1}$, is performed in two bus cycles. The first address of the data to be transferred is x'A00000'. The address of the external device is x'500000'.

■ DMA Settings

- (1) The DMA0 transfer address pointer (DM0TAP) is set to the first address in memory x'A00000' of the transfer source.

DM0TAPL, DM0TAPH: x'00FE80', x'00FE82'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0 AR15	DMA0 AR14	DMA0 AR13	DMA0 AR12	DMA0 AR11	DMA0 AR10	DMA0 AR9	DMA0 AR8	DMA0 AR7	DMA0 AR6	DMA0 AR5	DMA0 AR4	DMA0 AR3	DMA0 AR2	DMA0 AR1	DMA0 AR0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	DMA0 AR23	DMA0 AR22	DMA0 AR21	DMA0 AR20	DMA0 AR19	DMA0 AR18	DMA0 AR17	DMA0 AR16
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0

- (2) The DMA1 transfer address pointer (DM1TAP) is set to the first address in memory x'500000' of the transfer destination.

DM1TAPL, DM1TAPH: x'00FE90', x'00FE92'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA1 AR15	DMA1 AR14	DMA1 AR13	DMA1 AR12	DMA1 AR11	DMA1 AR10	DMA1 AR9	DMA1 AR8	DMA1 AR7	DMA1 AR6	DMA1 AR5	DMA1 AR4	DMA1 AR3	DMA1 AR2	DMA1 AR1	DMA1 AR0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	DMA1 AR23	DMA1 AR22	DMA1 AR21	DMA1 AR20	DMA1 AR19	DMA1 AR18	DMA1 AR17	DMA1 AR16
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0

- (3) The number of transfers is set. Since 5 words are to be transferred, the DMA0 transfer count register (DM0CNT) is set to '5'.

DM0CNTL, DM0CNTH: x'00FE84', x'00FE86'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0 CT15	DMA0 CT14	DMA0 CT13	DMA0 CT12	DMA0 CT11	DMA0 CT10	DMA0 CT9	DMA0 CT8	DMA0 CT7	DMA0 CT6	DMA0 CT5	DMA0 CT4	DMA0 CT3	DMA0 CT2	DMA0 CT1	DMA0 CT0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	DMA0 CT23	DMA0 CT22	DMA0 CT21	DMA0 CT20	DMA0 CT19	DMA0 CT18	DMA0 CT17	DMA0 CT16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- (4) The transfer parameters are set. External request 1 level is selected as the starting factor. Transfer between memory and external device 2 is selected as the transfer configuration. Pulse is selected as the ACK output. INC is selected for transfer addressing so that the source pointer will be incremented. The transfer method is normal and source is selected as the transfer direction. The transfer mode is set to burst. The unit for transfers is set to one-word units. Interrupt generation selection is set to generate. Execute enable is set to disabled. Other parameters do not affect operation.

DM0CTR: x'00FE8A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0 EN	DMA0 IT	DMA0 UT	DMA0 MD	DMA0 SD	DMA0 MT	DMA0 AD1	DMA0 AD0	DMA0 ACK	DMA0 ST1	DMA0 ST0	DMA0 BG4	DMA0 BG3	DMA0 BG2	DMA0 BG1	DMA0 BG0
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

- (5) Execute enable of the DM0CTR is set to enable. Other parameters are set with the same values as in procedure (4).

DM0CTR: x'00FE8A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0 EN	DMA0 IT	DMA0 UT	DMA0 MD	DMA0 SD	DMA0 MT	DMA0 AD1	DMA0 AD0	DMA0 ACK	DMA0 ST1	DMA0 ST0	DMA0 BG4	DMA0 BG3	DMA0 BG2	DMA0 BG1	DMA0 BG0
1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

After register setting, the transfer begins when external request signal DMAREQ1 goes to a 'L' level. After the set number of transfers are repeated, control of the bus is returned to the CPU and the transfer is complete.

A, B, C, D, E, F, G, H, I and J indicate 1-byte data.

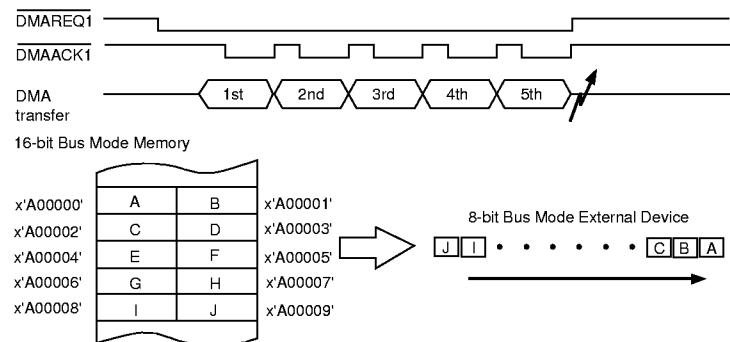


Figure 8-2-10 Data Transfer from Memory to External Device

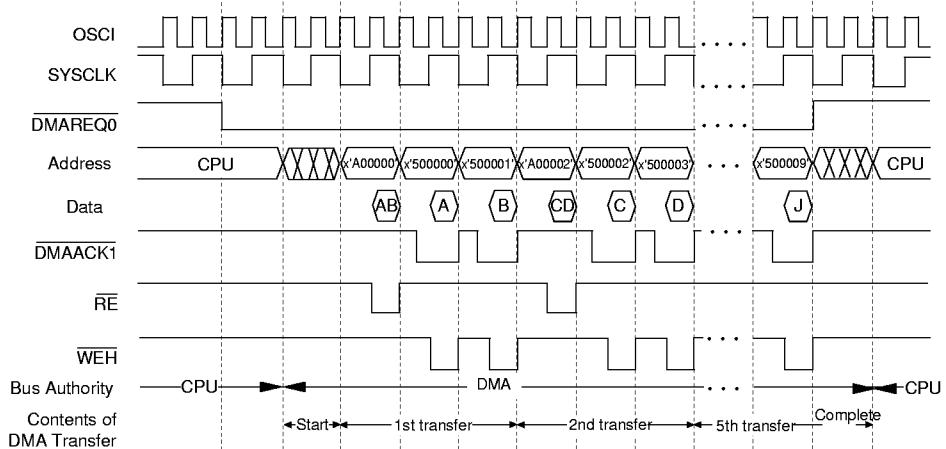


Figure 8-2-11 Timing Chart of DMA Transfer Bus Cycle

(16-bit bus mode memory → 8-bit bus mode external device)

Chapter 9 Port Functions

9

9-1 Port Function Summary

9-1-1 Overview

The MN1020012 has a total of five I/O ports: 8-bit Ports 0 and 1, 4-bit Port 2, 5-bit Port 3, and 4-bit Port 4. The first four are bidirectional. The last is for input only.

Table 9-1-1 List of Port Functions (1/3)

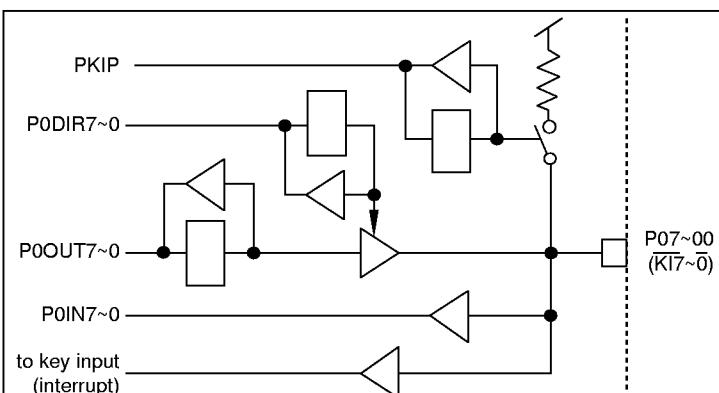
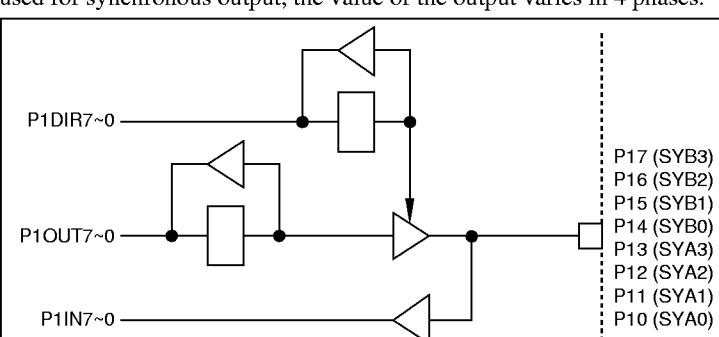
Port Name	Pin Name (Dual Purpose Pin Name)	Summary
Port0	P07~P00 (KI7~KI0)	<p>Port 0 is used both as a general purpose port and for key input. During reset, it is operated as a general purpose port input. If even one pin is to be used as a general purpose port, set KIIE of G10ICR to '0'.</p>  <p>The diagram illustrates the internal logic for Port 0. It shows a bidirectional bus with P0OUT7~0 and P0IN7~0. A key input line, labeled 'to key input (interrupt)', connects to an inverter. The output of this inverter is connected to a switch. The switch connects the key input line to ground or to the bidirectional bus. The bus also includes a direction register P0DIR7~0 and a pull-up/pull-down logic section controlled by PKIP.</p>
Port1	P17~P10 (SYB3~SYB0, SYA3~SYA0)	<p>Port 1 is used both as a general purpose port and for synchronous output. During reset, it is operated as a general purpose port input. When being used for synchronous output, the value of the output varies in 4 phases.</p>  <p>The diagram illustrates the internal logic for Port 1. It shows a bidirectional bus with P1OUT7~0 and P1IN7~0. A synchronous output line, labeled 'P1OUT7~0', connects to an inverter. The output of this inverter is connected to a switch. The switch connects the output line to ground or to the bidirectional bus. The bus also includes a direction register P1DIR7~0 and a pull-up/pull-down logic section.</p>

Table 9-1-1 List of Port Functions (2/3)

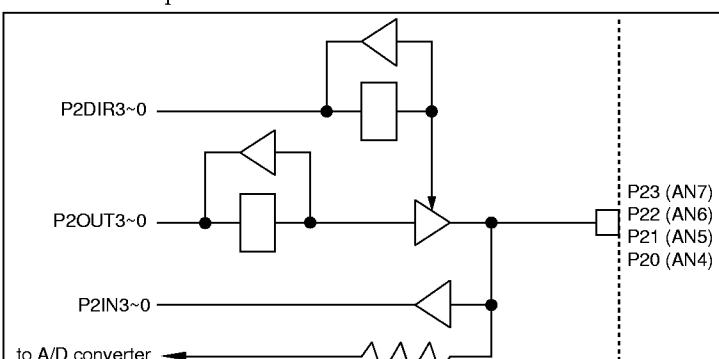
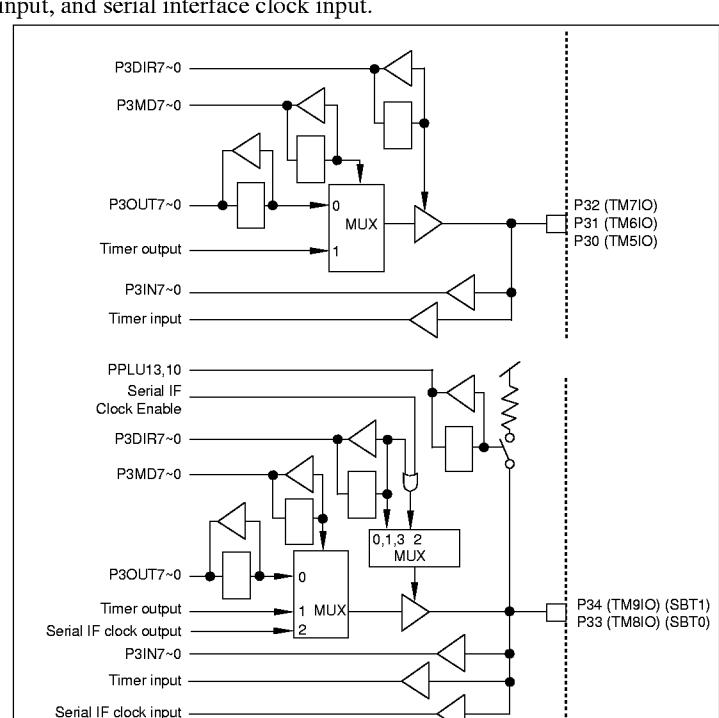
Port Name	Pin Name (Dual Purpose Pin Name)	Summary
Port2	P23~P20 (AN7~AN4)	<p>Port 2 is used both as a general purpose port and as an A/D converter input pin. During reset, it is operated as a general purpose port input and A/D converter input.</p> 
Port3	P34~P30 (TM9IO~TM5IO, SBT1~SBT0)	<p>Port 3 is used as a general purpose port or timer and serial interface clock. During reset, it is operated as a general purpose port input, timer input, and serial interface clock input.</p> 

Table 9-1-1 List of Port Functions (3/3)

Port Name	Pin Name (Dual Purpose Pin Name)	Summary
Port4	P43~P40 (IRQ3~IRQ0)	<p>Port 4 is used as both a general purpose port and an interrupt port. Port 4 is only used for inputs. It is assigned to bits 15~12 of the external pin interrupt condition control register, EXTMD.</p> <p>PPLU5~2</p> <p>EXTMD15~12</p> <p>External interrupt signal</p> <p>P43 (IRQ3) P42 (IRQ2) P41 (IRQ1) P40 (IRQ0)</p>

9-1-2 Control Registers

The port control registers consist of the following.

Table 9-1-2 List of Port Control Registers

Port 0	Port 0 Output Register Port 0 Input Register Port 0 I/O Control Register	(P0OUT) (P0IN) (P0DIR)	x'00FFC0' x'00FFD0' x'00FFE0'
Port 1	Port 1 Output Register Port 1 Input Register Port 1 I/O Control Register	(P1OUT) (P1IN) (P1DIR)	x'00FE64'* x'00FFD1' x'00FE1'
Port 2	Port 2 Output Register Port 2 Input Register Port 2 I/O Control Register	(P2OUT) (P2IN) (P2DIR)	x'00FFC2' x'00FFD2' x'00FE2'
Port 3	Port 3 Output Register Port 3 Input Register Port 3 I/O Control Register Port 3 Output Mode Register	(P3OUT) (P3IN) (P3DIR) (P3MD)	x'00FFC3' x'00FFD3' x'00FE3' x'00FFF3'
Port 4	External Interrupt Condition Control Register	(EXTMD15~12)	x'00FC56'
Other	Port Pull-up Control Register Timer Output Control Register	(PPLU) (TMDIR)	x'00FFB0' x'00FFB2'

* The port 1 output register is located in the register area related to synchronous output functions.

The port output registers (PnOUT) set the data for output. The port input registers (PnIN) are read only, and read the pin value. The port I/O control registers (PnDIR) set I/O direction for each bit. The output mode registers (PnMD) set the port output data. The port pull-up control register (PPLU) specifies whether each pin is pulled up.

The pull-up resistor is approximately 30 kΩ. Refer to the product standards for specific values.

Two systems exist for writing to the port 1 output register (P1OUT): writing from the CPU core and synchronous output. Read and write from the CPU core is possible with a MOV or similar instruction. Also, by synchronizing a timer for synchronous output, an automatic write operation can be performed for the operating pattern of a stepping motor, etc.

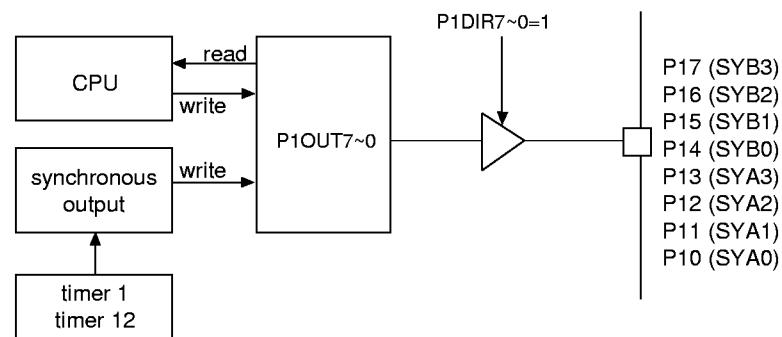


Figure 9-1-1 Write to Port 1

Table 9-1-3 Port 0

Item	P0DIR	Comments
Port input Key interrupt input	0	When KIIE of G10ICR is set to '1', P00~P07 operate as $\bar{K}I$ pins. (At this time, clear all the bits of P0DIR to '0').
Port output	1	

Table 9-1-4 Port 1

Item	P1DIR	Comments
Port input	0	
Port output Synchronous output	1	When SYAEN of SYAMD or SYBEN of SYBMD is set to '1', P10~P13 or P14~P17 operate as synchronous outputs.

Table 9-1-5 Port 2

Item	P2DIR	Comments
Port input Analog input	0	When ANEN of ANCTR is set to '1', P20~P23 operate as analog inputs.
Port output	1	

Table 9-1-6 Port 3 (P32~P30)

Item	P3DIR	P3MD	Comments
Port input Timer input	0	*	When the clock selection for the corresponding timer (TMnS1 and TMnS0 of TMnMD) is set to the TMnIO pin, P30~P32 operate as timer inputs. (n=5~7)
Port output Timer output	1 1	0 1	

Table 9-1-7 Port 3 (P34~P33)

Item	P3DIR [4] [3]	P3MD [6] [5]	P3MD	Comments
Port input Timer input Serial interface clock input (synchronous unidirectional transfer)	0	*	*	When the clock selection for the corresponding timer (TMnS1 and TMnS0 of TMnMD) is set to the TMnIO pin, P33~P34 operate as timer inputs. (n=8, 9) When the clock selection for the corresponding serial interface (SCnS1 and SCnS0 of SCnCTR) is set to the SBTn pin, P33~P34 operate as serial interface clock inputs. (n=0, 1)
Serial interface clock I/O (synchronous bidirectional transfer)	0	1	1	
Port output	1	0	*	
Timer output	1	1	0	
Serial interface clock output (synchronous unidirectional transfer)	1	1	1	

9-2 Port Function Setting Example

9-2-1 General Purpose Port Setting Example

A light emitting diode, LED, is either lit or turned off depending upon the state of a switch input. A switch is connected to port P01 and an LED is connected to port P00. With this configuration, the LED will be lit when the switch at port P01 is closed, and the LED will be off when the switch is open.

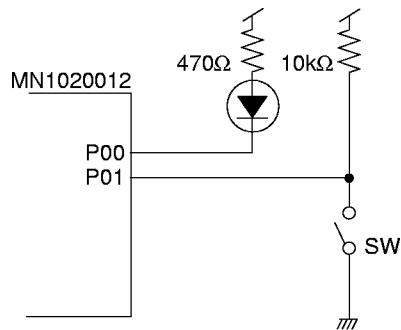


Figure 9-2-1 Example General Purpose Port Connection

- (1) After reset is released, the initial register values configure P01 and P00 as inputs. The LED is off.
- (2) The state of P01 (P0IN) is read by a MOV instruction. If bit 1 is '0' (switch is closed), P0OUT is set to x'00'.

P0OUT: x'00FFC0'

7	6	5	4	3	2	1	0
P0OUT7	P0OUT6	P0OUT5	P0OUT4	P0OUT3	P0OUT2	P0OUT1	P0OUT0
0	0	0	0	0	0	0	0

However, if bit 1 is '1' (switch is open), P0OUT is set to x'01'.

P0OUT: x'00FFC0'

7	6	5	4	3	2	1	0
P0OUT7	P0OUT6	P0OUT5	P0OUT4	P0OUT3	P0OUT2	P0OUT1	P0OUT0
0	0	0	0	0	0	0	1

- (3) P0DIR is set to x'01' and P00 is set to output for a general purpose port. Under these conditions, if the switch is closed, a 'L' level signal will output to P00. A 'H' level signal will be output to P00 if the switch is open.

P0DIR: x'00FFE0'

7	6	5	4	3	2	1	0
P0DIR7	P0DIR6	P0DIR5	P0DIR4	P0DIR3	P0DIR2	P0DIR1	P0DIR0
0	0	0	0	0	0	0	1

Chapter 9 Port Functions

Chapter 10 Appendix

10

10-1 Electrical Characteristics



This LSI instruction manual describes standard specifications. When using this LSI chip, please obtain the product standards from this company's business office.

Classification	CMOS integrated circuit
Use	General purpose
Function	16-bit microcomputer
Pin diagram	Figure 1-4-1
External dimensions	Figure 1-4-5

A. Absolute Maximum Ratings

$V_{SS}=0V$				
Item		Symbol	Rating	Units
A1	Power source voltage	V_{DD}	-0.3~+7.0	V
A2	Input pin voltage	V_I	-0.3~ $V_{DD}+0.3$	V
A3	Output pin voltage	V_O	-0.3~ $V_{DD}+0.3$	V
A4	I/O pin voltage	V_{IO}	-0.3~ $V_{DD}+0.3$	V
A5	Temperature of operating environment	T_{opr}	-30~+85	°C
A6	Storage temperature	T_{stg}	-55~+125	°C

Notes:

- (1) The absolute maximum ratings are allowable values that when applied, will not damage the chip. They do not guarantee operation.
- (2) Connect all V_{DD} pins directly to the external power source and all V_{SS} pins directly to the external ground.
- (3) To prevent latch up, insert one or more $0.1\mu F$ or larger bypass capacitors between the power source pin and GND.

B. Operating Conditions

$V_{SS}=0V \ Ta=-30\sim+85^{\circ}C$							
Item	Symbol	Conditions	Allowable values			Units	
			Min	Typ	Max		
B1	Power source voltage	V_{DD}		4.5	5	5.5	V
Crystal oscillation 1 (OSCI)							
B2	Oscillation frequency	F_{osc1}				20	MHz



C. Electrical Characteristics

(1) DC Characteristics

$V_{DD}=5.0V$ $V_{SS}=0V$ $T_a=-30\sim+85^{\circ}C$

Item	Symbol	Conditions	Allowable values			Units
			Min	Typ	Max	
C1	Power source current during operation	I_{DD1}	$V_t=V_{DD}$ or V_{SS} $Fosc1=20MHz$ Output open			75 mA
C2	Standstill power source current 1(STOP mode)	I_{DD2}	Oscillation stopped			50 μA
C3	Standstill power source current 2 (HALT mode)	I_{DD3}	$Fosc1=20MHz$			30 mA

■ I/O Pins

Output push-pull/input CMOS level schmitt trigger 1: TM7IO~TM0IO,
 TM12IOA~TM10IOA,
 TM12IOB~TM10IOB,
 SYA3~0, SYB3~0

$V_{DD}=4.5\sim5.5V$ $V_{SS}=0V$ $T_a=-30\sim+85^{\circ}C$

Item	Symbol	Conditions	Standard			Units
			Min	Typ	Max	
C4	'H' level input voltage	V_{IH1}		$V_{DD}\times 0.8$		V
C5	'L' level input voltage	V_{IL1}			$V_{DD}\times 0.2$	V
C6	'H' level output voltage	V_{OH1}	$V_{DD}=5V$ $I_{OH}=-4.0mA$	$V_{DD}-0.6$		V
C7	'L' level output voltage	V_{OL1}	$V_{DD}=5V$ $I_{OL}=4.0mA$			0.4 V
C8	Output leakage current	I_{OL1}	During high impedance output			$\pm 10 \mu A$

■ I/O Pins

Output push-pull/input CMOS level schmitt trigger 1/with pull-up: TM9IO,
TM8IO,
K17~K10

$V_{DD}=4.5\sim 5.5V$ $V_{SS}=0V$ $T_a=-30\sim +85^{\circ}C$

Item	Symbol	Conditions	Standard			Units
			Min	Typ	Max	
C9	'H' level input voltage	V_{IH1}		$V_{DD}\times 0.8$		V
C10	'L' level input voltage	V_{IL1}			$V_{DD}\times 0.2$	V
C11	'H' level output voltage	V_{OH1}	$V_{DD}=5V$ $I_{OH}=-4.0mA$	$V_{DD}-0.6$		V
C12	'L' level output voltage	V_{OL1}	$V_{DD}=5V$ $I_{OL}=4.0mA$		0.4	V
C13	Output leakage current	I_{OL1}	During high impedance output		± 10	μA
C14	Pull-up resistor value	R_{PUL}	$V_I=1.5V$	17.5	30	50
						k Ω

■ Output Pins

Output push-pull: SYSCLK, CS3~CS0, RAS, RE, WEH, WEL,
DMAACK1~DMAACK0, BG, A23~00, SBO1~0

$V_{DD}=4.5\sim 5.5V$ $V_{SS}=0V$ $T_a=-30\sim +85^{\circ}C$

Item	Symbol	Conditions	Standard			Units
			Min	Typ	Max	
C15	'H' level output voltage	V_{OH2}	$V_{DD}=5V$ $I_{OH}=-4.0mA$	$V_{DD}-0.6$		V
C16	'L' level output voltage	V_{OL2}	$V_{DD}=5V$ $I_{OL}=4.0mA$		0.4	V
C17	Output leakage current	I_{OL2}	During high impedance output		± 10	μA

■ Input Pins 1

Input CMOS level schmitt trigger: $\overline{\text{BSMOD}}$, $\overline{\text{RST}}$, $\overline{\text{DMAREQ1}}\sim\overline{\text{DMAREQ0}}$,
 $\overline{\text{DMAEND}}$, $\overline{\text{BR}}$, $\overline{\text{IRQ3}}\sim\overline{\text{IRQ0}}$,
 $\overline{\text{SBI1}}\sim\overline{\text{SBI0}}$, TM11IC, TM10IC

$V_{DD}=4.5\sim5.5V$ $V_{SS}=0V$ $T_a=-30\sim+85^{\circ}C$

Item	Symbol	Conditions	Standard			Units
			Min	Typ	Max	
C18	V_{IH3}		$V_{DD}\times0.8$			V
C19	V_{IL3}				$V_{DD}\times0.2$	V
C20	I_{L11}	$V_{DD}=5.5V$ $V_t=V_{SS}\sim V_{DD}$			±10	μA
C21	R_{PU2}	$V_t=1.5V$	17.5	30	50	k Ω

■ I/O Pins

Output push-pull/input TTL level/with pull-up: D15~00,

$V_{DD}=4.5\sim5.5V$ $V_{SS}=0V$ $T_a=-30\sim+85^{\circ}C$

Item	Symbol	Conditions	Standard			Units
			Min	Typ	Max	
C22	V_{IH4}		2.4			V
C23	V_{IL4}				0.8	V
C24	V_{OH4}	$V_{DD}=5V$ $I_{OH}=-4.0mA$	$V_{DD}-0.6$			V
C25	V_{OL4}	$V_{DD}=5V$ $I_{OL}=4.0mA$			0.4	V
C26	I_{LO4}	During high impedance output			±10	μA
C27	R_{PU4}	$V_t=1.5V$	17.5	30	50	k Ω

■ OSC pins (during external clock input)

$V_{DD}=4.5\sim 5.5V$ $V_{SS}=0V$ $T_a=-30\sim +85^{\circ}C$

Item	Symbol	Conditions	Standard			Units
			Min	Typ	Max	
C28	V_{IH4}		$V_{DD}\times 0.8$		V_{DD}	V
C29	V_{IL4}		V_{SS}		$V_{DD}\times 0.2$	V

Refer to Figure 10-1-1 for a self-excited oscillator configuration with a crystal or ceramic oscillator.

■ Analog I/O Pins: AN7~4

$V_{DD}=4.5\sim 5.5V$ $V_{SS}=0V$ $T_a=-30\sim +85^{\circ}C$

Item	Symbol	Conditions	Standard			Units
			Min	Typ	Max	
C30	V_{OH1}	$V_{DD}=5V$ $I_{OH}=-4.0mA$	$V_{DD}-0.6$			V
C31	V_{OL1}	$V_{DD}=5V$ $I_{OL}=4.0mA$			0.4	V
C32	I_{OL1}	During high impedance output			± 10	μA

■ Analog Input Pins: AN3~0

$V_{DD}=4.5\sim 5.5V$ $V_{SS}=0V$ $T_a=-30\sim +85^{\circ}C$

Item	Symbol	Conditions	Standard			Units
			Min	Typ	Max	
C33	I_{LI2}	$V_{DD}=5V$ $V_I=V_{SS}\sim V_{DD}$			± 10	μA

■ Pin Capacitance

$V_{DD}=4.5\sim 5.5V$ $V_{SS}=0V$ $T_a=-30\sim +85^{\circ}C$

Item	Symbol	Conditions	Standard			Units
			Min	Typ	Max	
C34	C_{IN}	$V_{IN}=0V$ $T_a=25^{\circ}C$		7	15	pF
C35	C_{OUT}			7	15	pF
C36	C_{IO}			7	15	pF

(2) A/D Converter Characteristics

$V_{DD}=5.0V \ V_{SS}=0V \ Ta=25^{\circ}C$							
Item		Symbol	Conditions	Standard			Units
				Min	Typ	Max	
D1	Resolution					8	Bits
D2	A/D conversion relative precision		$AV_{DD}=5V$ $AV_{SS}=0V$			± 3	LSB
D3	A/D conversion time		$F_{osc}=20MHz$	4.0			μs
D4	A/D conversion period		$F_{osc}=20MHz$	4.0			μs
D5	Analog input voltage	V_{LA}		V_{SS}		V_{DD}	V

(3) AC Characteristics

Input Timing Conditions

■ External Clock Input Timing ($F_{osc1}=20MHz$)

$V_{DD}=4.5\sim 5.5V \ V_{SS}=0V \ Ta=-30\sim +85^{\circ}C$							
Item		Symbol	Conditions	Standard			Units
				Min	Typ	Max	
E1	External clock input cycle time	t_{EXCyc}	Figure 10-1-3	50			ns
E2	External clock input HIGH pulse width	t_{EXCH}		$\frac{t_{EXCyc}}{2}-5$			ns
E3	External clock input LOW pulse width	t_{EXCL}		$\frac{t_{EXCyc}}{2}-5$			ns
E4	External clock input rise time	t_{EXCR}				5	ns
E5	External clock input fall time	t_{EXCF}				5	ns

■ Reset Input Timing

$V_{DD}=4.5\sim 5.5V$ $V_{SS}=0V$ $T_a=-30\sim +85^{\circ}C$

Item	Symbol	Conditions	Standard			Units	
			Min	Typ	Max		
E6	Reset signal setup time (\overline{RST})	t_{RSTS}	Figure 10-1-4	60			ns
E7	Reset signal pulse width (\overline{RST})	t_{RSTW}		4			t_{EXCyc}

■ Data Transfer Signal Input Timing

$V_{DD}=4.5\sim 5.5V$ $V_{SS}=0V$ $T_a=-30\sim +85^{\circ}C$

Item	Symbol	Conditions	Standard			Units	
			Min	Typ	Max		
E8	Read data setup time (D15~00)	t_{RDs}	Figure 10-1-5 Figure 10-1-6	20			ns
E9	Read data hold time 1 (D15~00)	t_{RDH1}		0			ns

■ Interrupt Signal Input Timing

$V_{DD}=4.5\sim 5.5V$ $V_{SS}=0V$ $T_a=-30\sim +85^{\circ}C$

Item	Symbol	Conditions	Standard			Units
			Min	Typ	Max	
E10	External interrupt signal pulse width (IRQ3~0, \overline{KI} : when $t_{cyc}=100ns$)	t_{IRQW}	Figure 10-1-10	$t_{cyc}\times 2$		ns

■ Serial Interface Related Signal Input Timing 2
(during synchronous serial reception)

$V_{DD}=4.5\sim 5.5V$ $V_{SS}=0V$ $T_a=-30\sim +85^{\circ}C$							
Item		Symbol	Conditions	Standard			Units
Min	Typ			Max			
E11	Received data setup time (SBII~0)	t_{RXDS2}	Figure 10-1-12	50			ns
E12	Received data hold time (SBII~0)	t_{RXDH2}		50			ns

■ Timer/Counter Signal Input Timing

$V_{DD}=4.5\sim 5.5V$ $V_{SS}=0V$ $T_a=-30\sim +85^{\circ}C$							
Item		Symbol	Conditions	Standard			Units
Min	Typ			Max			
E13	Timer external input clock LOW pulse width (TM12IO~TM0IO)	$t_{TCCCLKL}$	Figure 10-1-13	$t_{cyc}\times 2$			ns
E14	Timer external input clock HIGH pulse width (TM12IO~TM0IO)	$t_{TCCCLKH}$		$t_{cyc}\times 2$			ns
E15	Timer control signal LOW input pulse width (TM12IO~TM0IO)	t_{TCCNTL}	Figure 10-1-14	$t_{cyc}\times 2$			ns
E16	Timer control signal HIGH input pulse width (TM12IO~TM0IO)	t_{TCCNTH}		$t_{cyc}\times 2$			ns

■ DMA Signal Input Timing

Item		Symbol	Conditions	Standard			Units
				Min	Typ	Max	
E17	Setup time for DMA edge transfer (DMAREQ: when $t_{cyc}=100\text{ns}$)	t_{DRQEBS}	Figure 10-1-15	30			ns
E18	Hold time for DMA edge transfer (DMAREQ)	t_{DRQEBH}		30			ns
E19	Setup time for DMA level transfer startup (DMAREQ: when $t_{cyc}=100\text{ns}$)	t_{DRQLBS}	Figure 10-1-16	$\frac{t_{cyc}}{4} + 30$			ns
E20	Hold time for DMA level transfer termination (DMAREQ)	t_{DRQLEH}		0			ns
E21	Setup time for DMA level transfer termination (DMAREQ)	t_{DRQLES}		50			ns
E22	Width of HIGH level DMA forced termination signal (DMAEND)	t_{DENDHW}	Figure 10-1-17	$t_{cyc} \times 3$			ns

Output Signal Characteristics

■ System Clock Output Timing

Item		Symbol	Conditions	Standard			Units
				Min	Typ	Max	
F1	System clock output cycle time (SYSCLK)	t_{cyc}	Figure 10-1-3	100			ns
F2	System clock output LOW pulse width (SYSCLK)	t_{CL}		45			ns
F3	System clock output HIGH pulse width (SYSCLK)	t_{CH}		35			ns
F4	System clock output rise time (SYSCLK)	t_{CR}				10	ns
F5	System clock output fall time (SYSCLK)	t_{CF}				10	ns

■ Data Transfer Signal Output Timing 1

$V_{DD}=4.5\sim 5.5V$ $V_{SS}=0V$ $T_a=-30\sim +85^{\circ}C$ $C_L=70pF$

Item		Symbol	Conditions	Standard			Units
				Min	Typ	Max	
F6	Address delay time 1 (A23~00)	t_{AD1}	Figure 10-1-5 Figure 10-1-6 Figure 10-1-7			30	ns
F7	Address delay time 2 (A23~00)	t_{AD2}	Figure 10-1-6			$\frac{t_{CYC}}{4} + 25$	ns
F8	Address delay time 3 (A23~00)	t_{AD3}				$\frac{t_{CYC}}{4} + 25$	ns
F9	Address hold time 1 (A23~00)	t_{AH1}	Figure 10-1-5 Figure 10-1-6 Figure 10-1-7	5			ns
F10	Address hold time 2 (A23~00)	t_{AH2}	Figure 10-1-6	$\frac{t_{CYC}}{4} - 10$			ns
F11	Chip select signal fall delay time ($\overline{CS3}$ - $\overline{CS0}$)	t_{CSDF}	Figure 10-1-5 Figure 10-1-7			30	ns
F12	Chip select signal rise delay time ($\overline{CS3}$ - $\overline{CS0}$)	t_{CSDR}				30	ns
F13	Chip select signal hold time 1 ($\overline{CS3}$ - $\overline{CS0}$)	t_{CSH1}		0			ns
F14	Chip select signal hold time 2 ($\overline{CS3}$ - $\overline{CS0}$)	t_{CSH2}		0			ns

■ Data Transfer Signal Output Timing 2

$V_{DD}=4.5\sim 5.5V$ $V_{SS}=0V$ $T_a=-30\sim +85^{\circ}C$ $C_L=70pF$

Item	Symbol	Conditions	Standard			Units
			Min	Typ	Max	
F15	Column Address Strobe signal fall delay time 1 (CAS)	t _{CASDF1}	Figure 10-1-6 Figure 10-1-9		20	ns
F16	Column Address Strobe signal fall delay time 2 (CAS)	t _{CASDF2}	Figure 10-1-7		$\frac{t_{Cyc}}{4} + 20$	ns
F17	Column Address Strobe signal rise delay time (CAS)	t _{CASDR}	Figure 10-1-6		20	ns
F18	Row Address Strobe signal fall delay time (RAS)	t _{RASDF}	Figure 10-1-6 Figure 10-1-7		20	ns
F19	Row Address Strobe signal rise delay time (\overline{RAS})	t _{RASDR}			20	ns
F20	Chip Enable signal fall delay time (CE)	t _{CEDF}	Figure 10-1-8 Figure 10-1-9		20	ns
F21	Chip Enable signal rise delay time (\overline{CE})	t _{CEDR}			20	ns
F22	Output Enable signal fall delay time (\overline{OE})	t _{OEDF}			20	ns
F23	Output Enable signal rise delay time (\overline{OE})	t _{OEDR}			20	ns

■ Data Transfer Signal Output Timing 3

Item		Symbol	Conditions	Standard			Units
				Min	Typ	Max	
F24	Read data enable signal fall delay time (\overline{RE})	t _{REDF}	Figure 10-1-5 Figure 10-1-6 Figure 10-1-7 Figure 10-1-8			$\frac{t_{cyc}}{4} + 20$	ns
F25	Read data enable signal rise delay time (\overline{RE})	t _{REDR}				15	ns
F26	Write data enable signal fall delay time (\overline{WEL} , \overline{WEH})	t _{WEWF}				25	ns
F27	Write data enable signal rise delay time (\overline{WEL} , \overline{WEH})	t _{WEFR}				20	ns
F28	Write data delay time (D15~00)	t _{WD}				20	ns
F29	Write data hold time 1 (D15~00)	t _{WDH1}		5			ns
F30	Write data hold time 2 (D15~00)	t _{WDH2}		5			ns

■ Serial Interface Signal Output Timing 1 (during synchronous serial transfer)

Item		Symbol	Conditions	Standard			Units
				Min	Typ	Max	
F32	Transfer data setup time (SBO1~0)	t _{RXDOS}	Figure 10-1-11	$t_{cyc} \times 2$			ns
F33	Transfer data hold time* (SBO1~0)	t _{RXDOH}		$\frac{t_{cyc}}{2}$			ns

Note: During 20MHz oscillation, $t_{cyc}=100\text{ns}$; during 10MHz oscillation, $t_{cyc}=200\text{ns}$

■ DMA Interface Signal Output Timing

Item		Symbol	Conditions	Standard			Units
				Min	Typ	Max	
F34	DMA acknowledge signal delay time (falling edge) ($\overline{\text{DMAACK1}} \sim \overline{\text{DMAACK0}}$)	t _{DACKDD}	Figure 10-1-15			$\frac{t_{cyc}}{4} + 25$	ns
F35	DMA acknowledge signal delay time (rising edge) ($\overline{\text{DMAACK1}} \sim \overline{\text{DMAACK0}}$)	t _{DACKUD}				15	ns



Figure 10-1-1 Self-exciting Circuit Connection Example

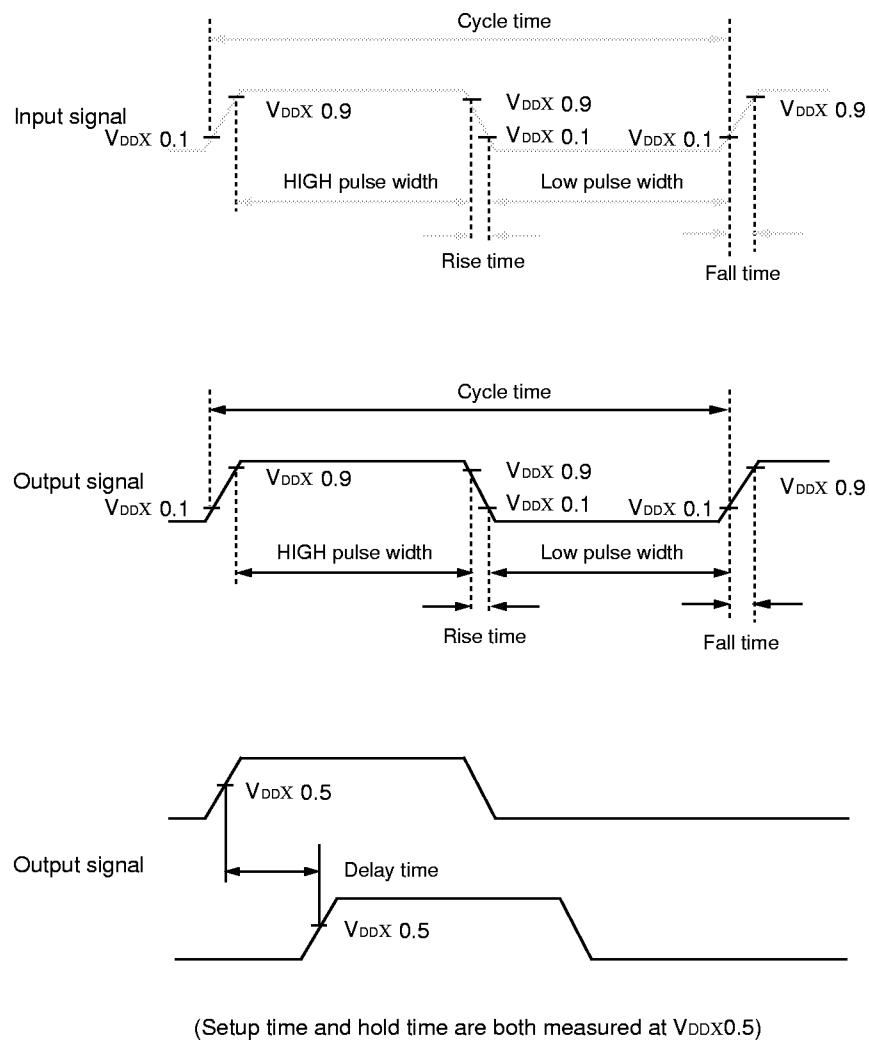


Figure 10-1-2 Voltage Level Conditions for Measuring AC Timing

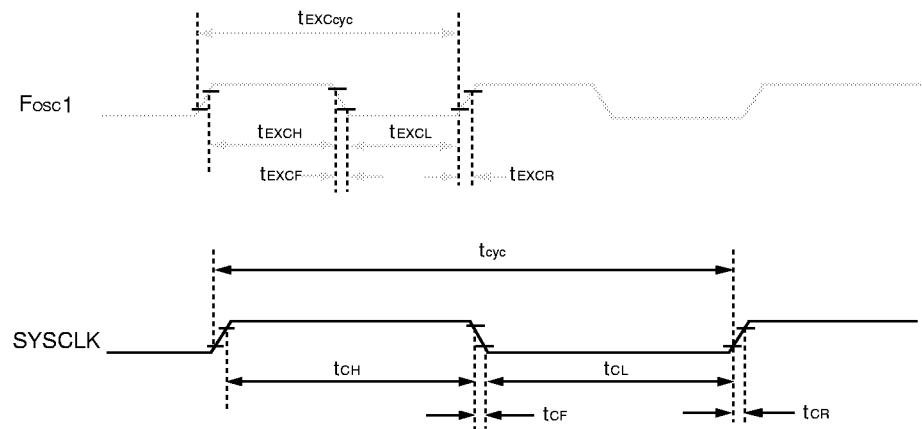


Figure 10-1-3 System Clock Timing

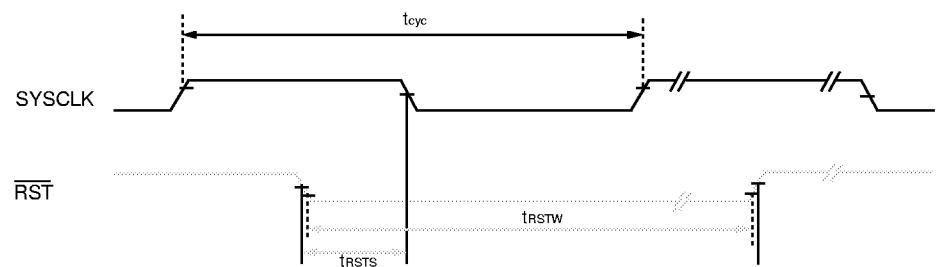


Figure 10-1-4 Reset Timing

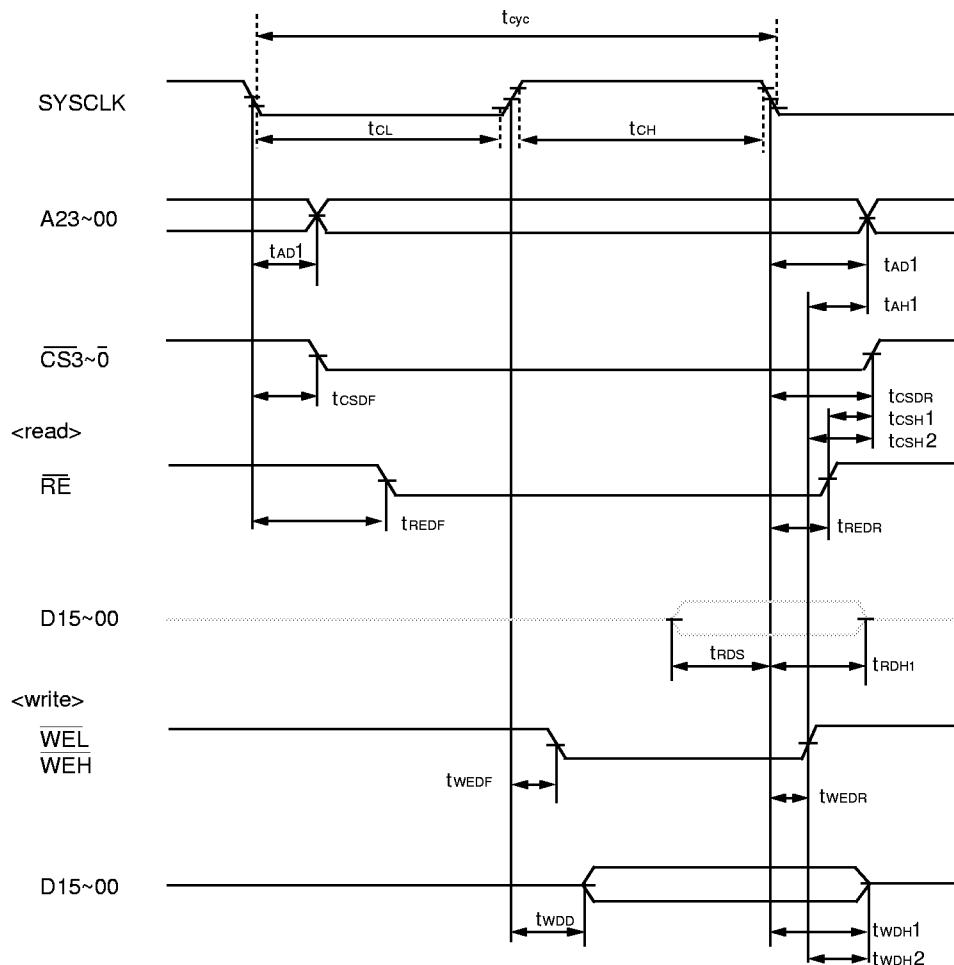


Figure 10-1-5 Timing of Data Transfer Signals (SRAM interface)

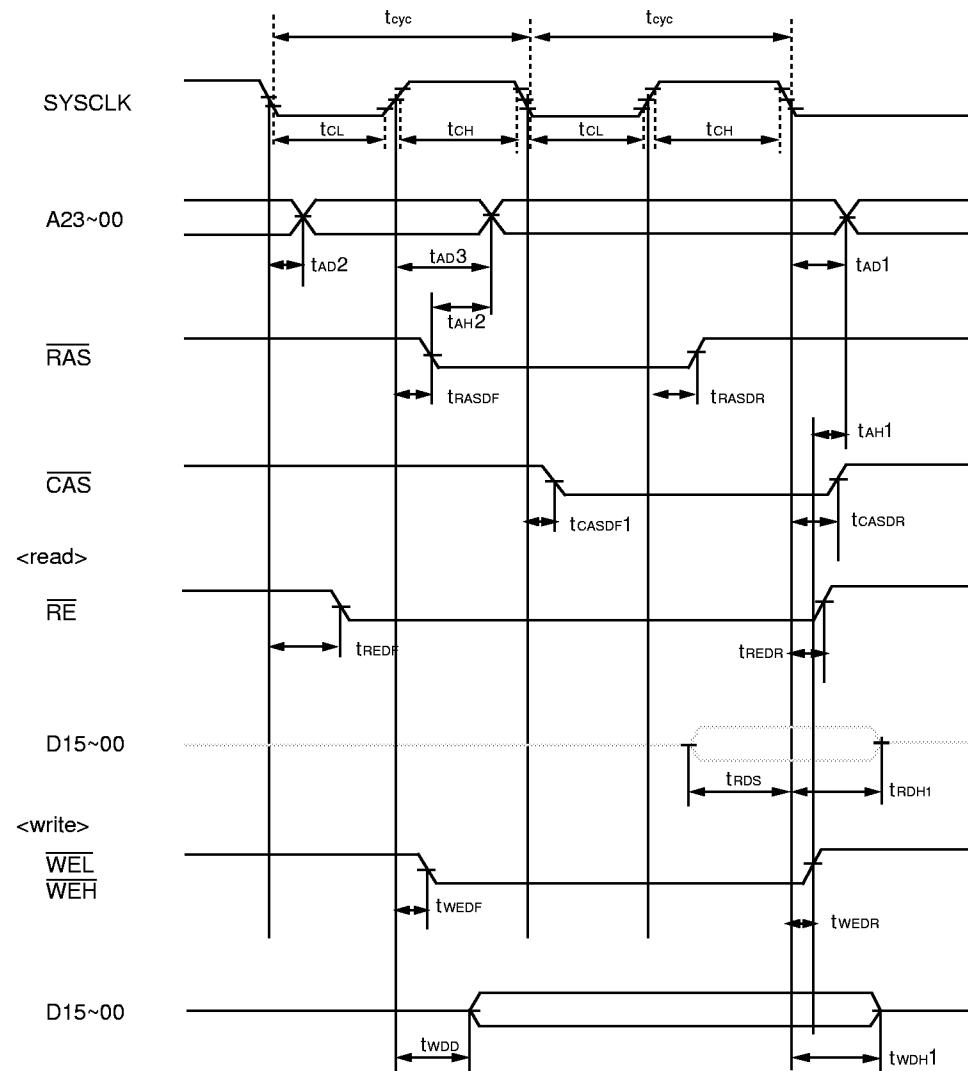


Figure 10-1-6 Timing of Data Transfer Signals (DRAM normal interface)

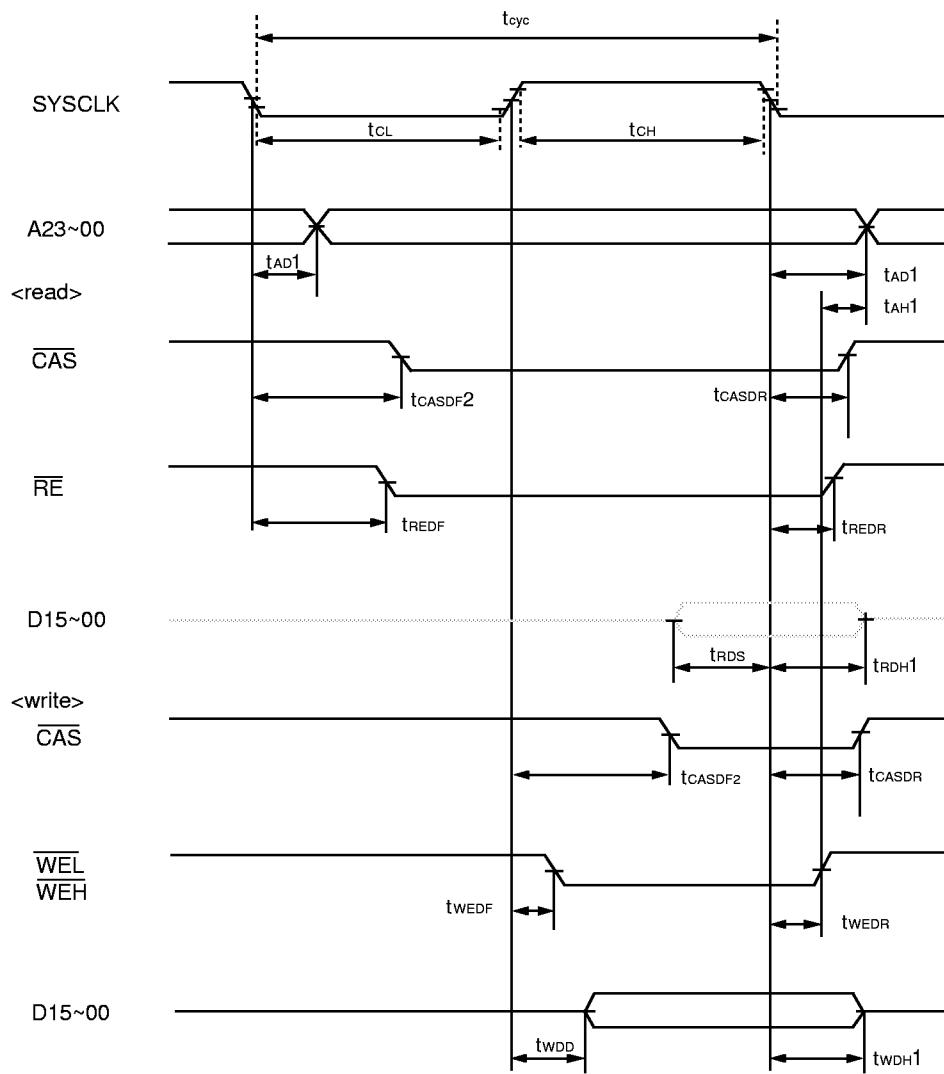


Figure 10-1-7 Timing of Data Transfer Signals (DRAM page mode interface)

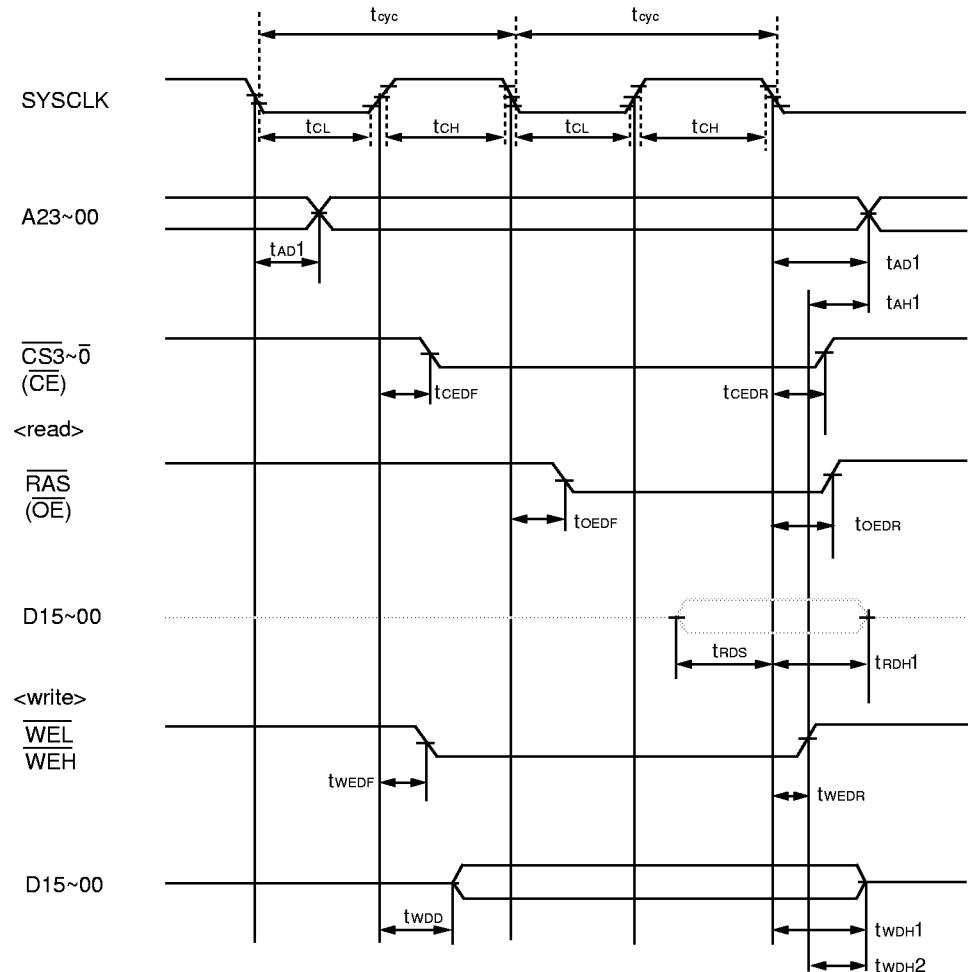


Figure 10-1-8 Timing of Data Transfer Signals (pseudo SRAM interface)

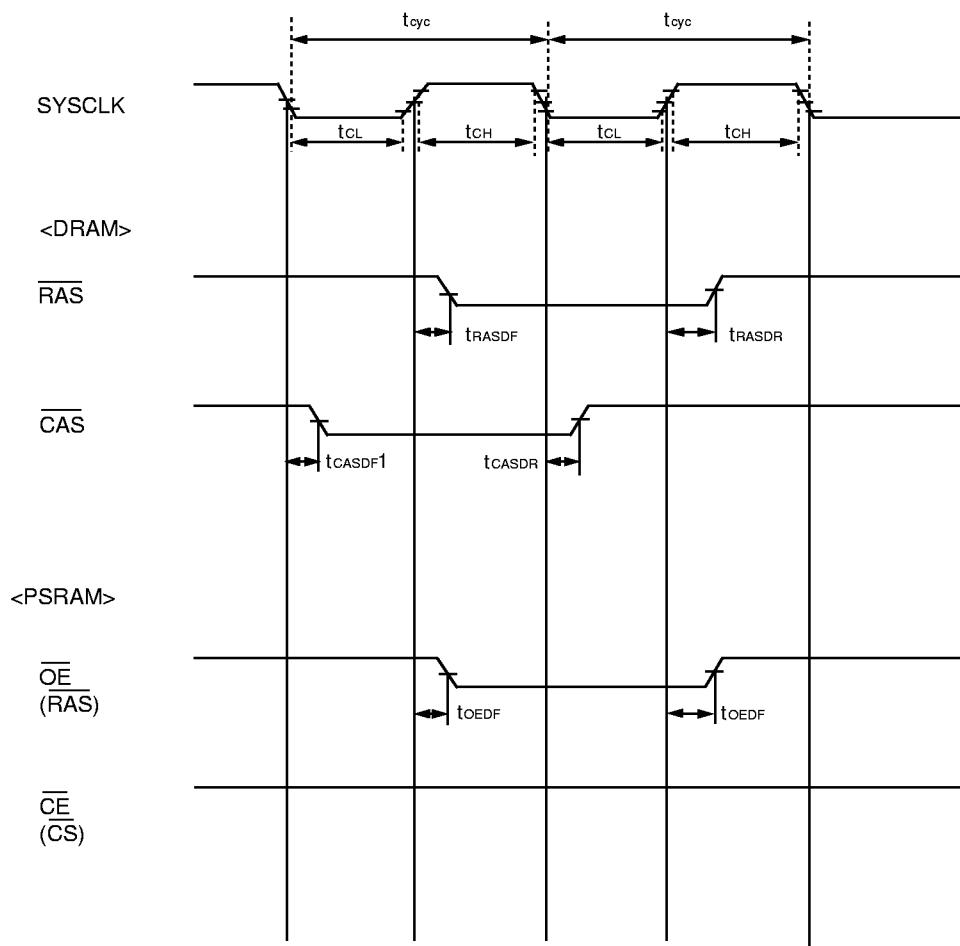


Figure 10-1-9 Timing of Refresh Signals (DRAM, pseudo SRAM)



Figure 10-1-10 Interrupt Signal Timing

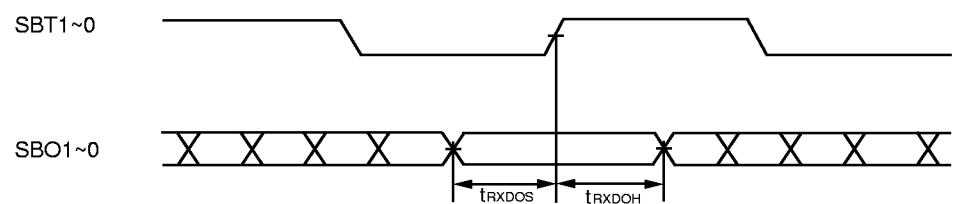


Figure 10-1-11 Serial Interface Signal Timing 1
(during synchronous serial transmission)

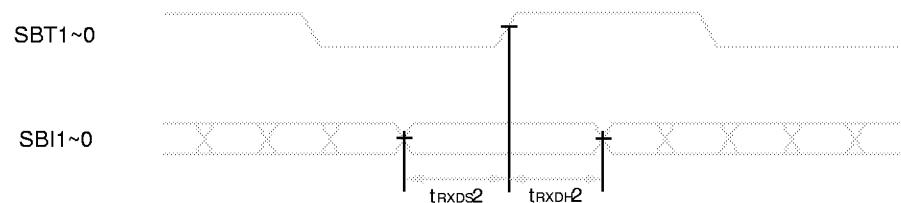


Figure 10-1-12 Serial Interface Signal Timing 2
(during synchronous serial reception)



Figure 10-1-13 Timer/Counter Signal Timing 1



Figure 10-1-14 Timer/Counter Signal Timing 2

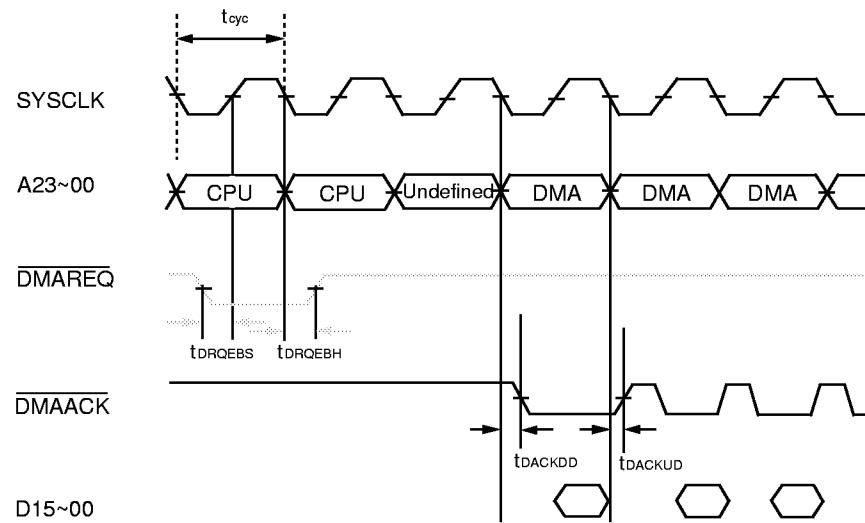


Figure 10-1-15 DMA Signal Timing (edge operation)

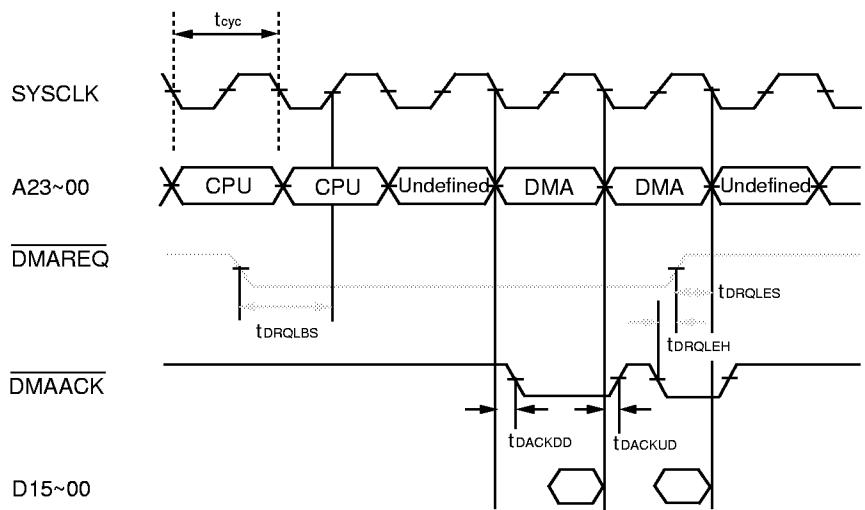


Figure 10-1-16 DMA Signal Timing (level operation)

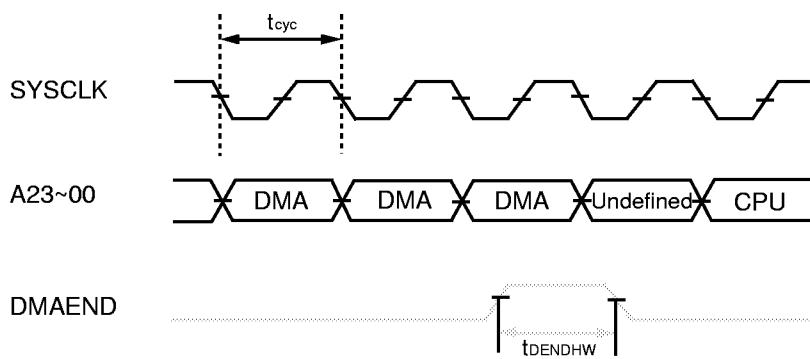


Figure 10-1-17 DMA Signal Timing (when terminated)

Chapter 10 Appendix

A**B****C****D****E****F****G****H****I****J****K****L****M****N****O****P****Q****R****S****T****U****V****W****X****Y****Z**

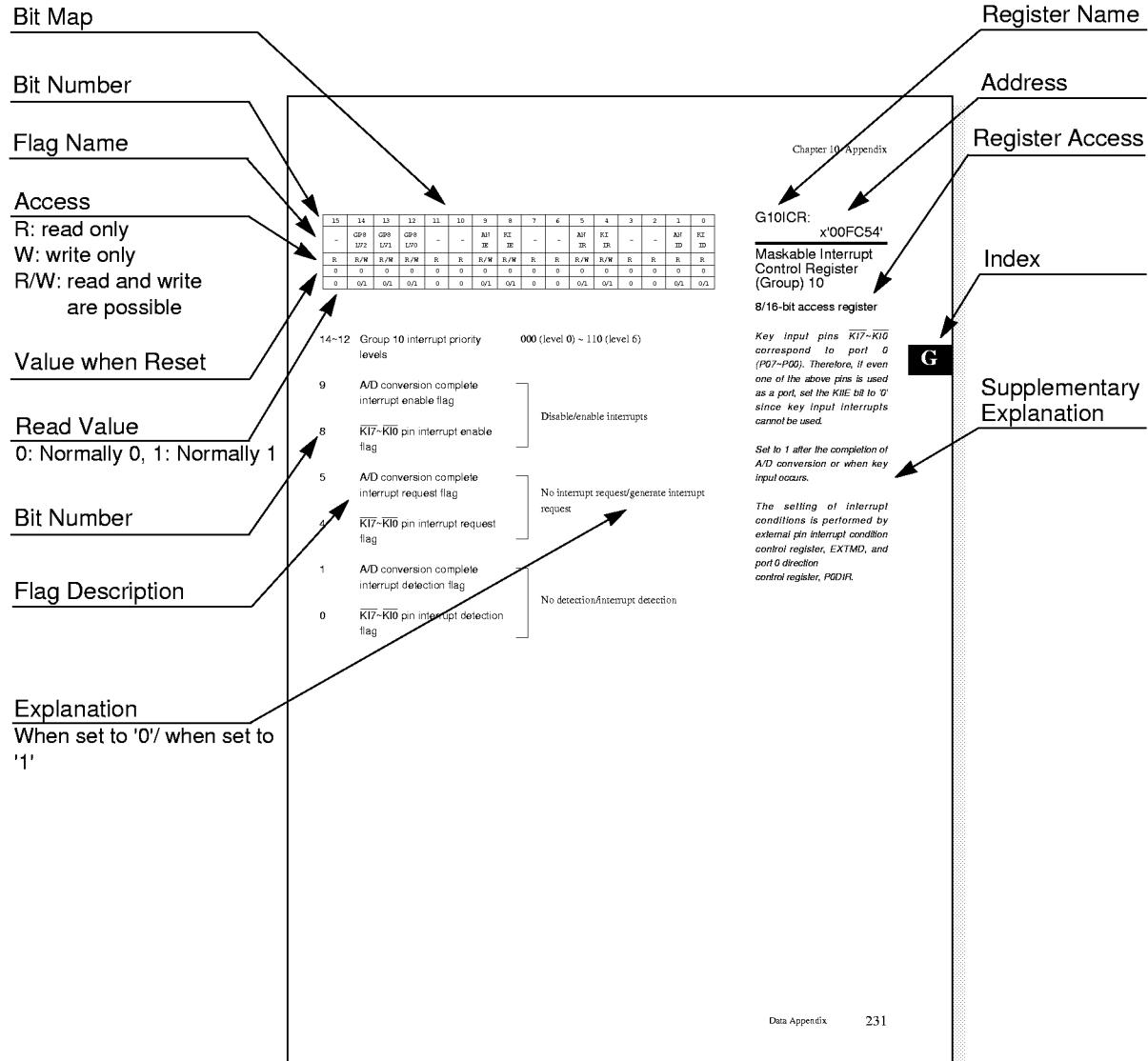
10-2 Data Appendix

10-2-1 List of Special Registers

How to Read Each Page

■ Configuration of each page

Each page of this chapter lists one or more registers. Each page is organized to contain a description of the register name, address, register access, bit map, and flags for each bit, as well as supplementary explanations. The layout and definitions of each section are shown below.



15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WD RST	-	-	-	-	-	-	-	-	-	-	OSC ID	STOP	HALT	OSC1	OSC0
R/W											R	R/W	R/W	R/W	R/W
1											0	0	0	0	0
0/1	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1

15	Watchdog timer enable flag	Enables/disables the watchdog function and clears the counter (during reset)
4	System clock monitor	High speed/low speed (normally 0 for the MN1020012)
3	CPU operating status control (STOP request)	
2	CPU operating status control (HALT request)	0000: NORMAL mode 0100: HALT mode 1000: STOP mode
1~0	Oscillation control	(If the MN1020012 is set to other than the above, operation is not guaranteed.)

CPUM:
x'00FC00'

CPU Mode Control Register

16-bit access register

If '0' is set after '1' had been set, the count value of the watchdog timer will be cleared and the count will restart.

The watchdog timer is formed from a 17-bit binary counter that runs on the CPU clock. Therefore, it is necessary for the user program to clear the count value of the watchdog timer within an interval of 2^{16} (65,536) machine cycles.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	HSWT IOE	NWAIT IOE	WAIT SET	ARBSZ	-	WAIT IO1	WAIT IO0	-	WAIT2	WAIT1	WAIT0
R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
0	0	0	0	0	1	1	0	0	0	1	1	0	1	1	1
0	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	0/1	0	0/1	0/1	0/1

- 10 Flag enable for independent setting of number of fixed wait cycles for peripheral devices during handshake mode No wait/number of peripheral fixed wait cycles
- 9 Flag enable for independent setting of number of fixed wait cycles for peripheral devices Enable independent setting of peripheral fixed wait number/disable
- 8 Switching between fixed wait mode/handshake mode Handshake mode/fixed wait mode
- 7 Bus width setting flag for fixed area (x'040000'~x'07FFFF') Conform to BSMOD pin setting/8-bit width access regardless of the BSMOD pin setting
- 5,4 Independent setting of number of peripheral fixed wait cycles 00: No wait cycles
01: 1 wait cycle
10: 2 wait cycles
11: 3 wait cycles
- 2~0 Setting of number of fixed wait cycles 000: No wait cycles
001: 1 wait cycle
010: 2 wait cycles
011: 3 wait cycles
100: 4 wait cycles
101: 5 wait cycles
110: 6 wait cycles
111: 7 wait cycles

MEMCTR:
x'00FC02'

Memory Control Register

16-bit access register

*When setting initial values, be sure that WAITSET is set to '0'. During initial setting of the MN1020012, set this register to x'04*0' (*= number of peripheral fixed wait cycles, 1 is recommended).*

If the value of the flag within MEMCTR for setting the number of fixed wait cycles is rewritten, the number of wait cycles will change immediately after the write instruction.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	GN4	GN3	GN2	GN1	GN0	-
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0

5~1 Group number of accepted interrupt

IAGR:
x'00FC0E'

Interrupt Accept Group Number Register

8 or 16-bit access register

This register is read only, and therefore cannot be written to.

I

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	WAIT2	WAIT1	WAIT0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1

2~0 Block 0 wait cycles

- 000: no wait cycles
- 001: 1 wait cycle
- 010: 2 wait cycles
- 011: 3 wait cycles
- 100: 4 wait cycles
- 101: 5 wait cycles
- 110: 6 wait cycles
- 111: 7 wait cycles

MEMMD0:
x'00FC30'

External Memory Mode Register 0

16-bit access register

Unused blocks (BLOCKn) may be set to any value.

M

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRAM	-	-	-	-	-	-	BMOD	-	-	-	-	-	WAIT2	WAIT1	WAIT0
R/W	R	R	R	R	R	R	R/W	R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0	0	0	0	0	0	0/1	0	0	0	0	0	0/1	0/1	0/1

15 DRAM or pseudo SRAM interface select Not selected/select

MEMMD1: x'00FC32'

External Memory Mode Register 1

16-bit access register

If there are any unused blocks (BLOCKn), set them to '0'.

8 Block 1 bus mode 16-bit bus mode/8-bit bus mode

2~0 Block 1 wait cycles
 000: No wait cycles
 001: 1 wait cycle
 010: 2 wait cycles
 011: 3 wait cycles
 100: 4 wait cycles
 101: 5 wait cycles
 110: 6 wait cycles
 111: 7 wait cycles

Unused blocks (BLOCKn) may be set to any value.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRAM	-	-	-	-	-	-	BMOD	-	-	-	-	-	WAIT2	WAIT1	WAIT0
R/W	R	R	R	R	R	R	R/W	R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0	0	0	0	0	0	0/1	0	0	0	0	0	0/1	0/1	0/1

15 DRAM or pseudo SRAM interface select Not selected/select

MEMMD2: x'00FC34'

External Memory Mode Register 2

16-bit access register

If there are any unused blocks (BLOCKn), set them to '0'.

8 Block 2 bus mode 16-bit bus mode/8-bit bus mode

2~0 Block 2 wait cycles
 000: No wait cycles
 001: 1 wait cycle
 010: 2 wait cycles
 011: 3 wait cycles
 100: 4 wait cycles
 101: 5 wait cycles
 110: 6 wait cycles
 111: 7 wait cycles

Unused blocks (BLOCKn) may be set to any value.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRAM	-	-	-	-	-	-	BMOD	-	-	-	-	WAIT2	WAIT1	WAIT0	
R/W	R	R	R	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0	0	0	0	0	0	0/1	0	0	0	0	0/1	0/1	0/1	0/1

15 DRAM or pseudo SRAM interface select Not selected/select

8 Block 3 bus mode 16-bit bus mode/8-bit bus mode

2~0 Block 3 wait cycles
 000: No wait cycles
 001: 1 wait cycle
 010: 2 wait cycles
 011: 3 wait cycles
 100: 4 wait cycles
 101: 5 wait cycles
 110: 6 wait cycles
 111: 7 wait cycles

MEMMD3: x'00FC36'

External Memory Mode Register 3

16-bit access register

If there are any unused blocks (BLOCKn), set them to '0'.

G

Unused blocks (BLOCKn) may be set to any value.

M

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	UNIF	WDIF	-
R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0

2 Non-maskable interrupt request flag in response to execution of an undefined instruction No interrupt request/interrupt request generated

1 Non-maskable interrupt request flag in response to overflow of watchdog timer No interrupt request/interrupt request generated

G0ICR: x'00FC40'

Non-Maskable Interrupt Control Register (Group) 0

8/16-bit access register
 Bit 0 must be set to '0'.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	TMLA LV2	TML LV1	TML LV0	IE	TM2 IE	TM1 IE	TM0 IE	TM3 IR	TM2 IR	TM1 IR	TM0 ID	TM3 ID	TM2 ID	TM1 ID	TM0 ID
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

G1ICR:
x'00FC42'

Maskable Interrupt Control Register (Group) 1

8/16-bit access register

14~12 TM3~0 interrupt priority levels 000 (level 0)~110 (level 6)

11~8 TM3~0 underflow interrupt enable flags Disable/enable interrupt

7~4 TM3~0 underflow interrupt request flags No interrupt request/generate interrupt request

Set to 1 when timer underflow occurs.

3~0 TM3~0 underflow interrupt detection flags No detection/interrupt detection

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	TMM LV2	TMM LV1	TMM LV0	IE	TM7 IE	TM6 IE	TM5 IE	TM4 IR	TM7 IR	TM6 IR	TM5 IR	TM4 ID	TM7 ID	TM6 ID	TM5 ID
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

G2ICR:
x'00FC44'

Maskable Interrupt Control Register (Group) 2

8/16-bit access register

14~12 TM7~4 interrupt priority levels 000 (level 0)~110 (level 6)

11~8 TM7~4 underflow interrupt enable flags Disable/enable interrupt

7~4 TM7~4 underflow interrupt request flags No interrupt request/generate interrupt request

Set to 1 when timer underflow occurs.

3~0 TM7~4 underflow interrupt detection flags No detection/interrupt detection

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	TMH LV2	TMH LV1	TMH LVO	TM12 BIE	TM12 AIE	TM9 IE	TM8 IE	TM12 BIR	TM12 AIR	TM9 IR	TM8 IR	TM12 BID	TM12 AID	TM9 ID	TM8 ID
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

14~12 TM8, 9, 12 interrupt priority levels 000 (level 0)~110 (level 6)

11, 10 TM12 compare/capture B, A interrupt enable flags

9, 8 TM9, 8 underflow interrupt enable flags

7, 6 TM12 compare/capture B, A interrupt request flags

5, 4 TM9, 8 underflow interrupt request flags

3, 2 TM12 compare/capture B, A interrupt detection flags

1, 0 TM9, 8 underflow interrupt detection flags

Disable/enable interrupts

No interrupt request/generate interrupt request

No detection/interrupt detection

G3ICR:
x'00FC46'

Maskable Interrupt Control Register (Group) 3

8/16-bit access register

G

Set to 1 when timer underflow or compare/capture occurs.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	TM10 LV2	TM10 LV1	TM10 LV0	-	TM10 BIE	TM10 AIE	TM10 UIE	-	TM10 BIR	TM10 AIR	TM10 UIR	-	TM10 BID	TM10 AID	TM10 UID
R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

G4ICR:
x'00FC48'

Maskable Interrupt
Control Register
(Group) 4

8/16-bit access register

14~12 TM10 interrupt priority level 000 (level 0)~110 (level 6)

10, 9 TM10 compare/capture B,
A interrupt enable flags

Disable/enable interrupts

8 TM10 underflow interrupt
enable flag

*Set to 1 when timer underflow
or compare/capture occurs.*

6, 5 TM10 compare/capture B,
A interrupt request flags

No interrupt request/generate interrupt
request

4 TM10 underflow interrupt
request flag

No detection/interrupt detection

2, 1 TM10 compare/capture B,
A interrupt detection flags

0 TM10 underflow interrupt
detection flag

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	TM11 LV2	TM11 LV1	TM11 LV0	-	TM11 BIE	TM11 AIE	TM11 UIE	-	TM11 BIR	TM11 AIR	TM11 UIR	-	TM11 BID	TM11 AID	TM11 UID
R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0	0/1	0/1	0/1	0	0/1	0/1	0/1	0	0/1	0/1	0/1

14~12 TM11 interrupt priority levels 000 (level 0)~110 (level 6)

10, 9 TM11 compare/capture B,
A interrupt enable flags

Disable/enable interrupts

8 TM11 underflow interrupt
enable flag6, 5 TM11 compare/capture B,
A interrupt request flagsNo interrupt request/generate interrupt
request*Set to 1 when timer underflow
or compare/capture occurs.*4 TM11 underflow interrupt
request flag

No detection/interrupt detection

2, 1 TM11 compare/capture B,
A interrupt detection flags0 TM11 underflow interrupt
detection flag

G

G5ICR:
x'00FC4A'Maskable Interrupt
Control Register
(Group) 5

8/16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
-	DMA LV2	DMA LV1	DMA LV0	IE	IE	IE	IE	IR	IR	IR	IR	DMA0 ID	DMA3 ID	DMA2 ID	DMA1 ID	DMA0 ID
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	

G6ICR:
x'00FC4C'

Maskable Interrupt Control Register (Group) 6

8/16-bit access register

14~12 DMA interrupt priority levels 000 (level 0)~110 (level 6)

11~8 DMA3~0 transfer complete interrupt enable flags Disable/enable interrupts

7~4 DMA3~0 transfer complete interrupt request flags No interrupt request/generate interrupt request

Set to 1 when the DMA transfer is complete.

3~0 DMA3~0 transfer complete interrupt detection flags No detection/interrupt detection

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
-	DMA LV2	DMA LV1	DMA LV0	IE	IE	IE	IE	IR	IR	IR	IR	DMA4 ID	DMA7 ID	DMA6 ID	DMA5 ID	DMA4 ID
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	

G7ICR:
x'00FC4E'

Maskable Interrupt Control Register (Group) 7

8/16-bit access register

14~12 DMA interrupt priority levels 000 (level 0)~110 (level 6)

11~8 DMA7~4 transfer complete interrupt enable flags Disable/enable interrupts

7~4 DMA7~4 transfer complete interrupt request flags No interrupt request/generate interrupt request

Set to 1 when the DMA transfer is complete.

3~0 DMA7~4 transfer complete interrupt detection flags No detection/interrupt detection

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	IRQ LV2	IRQ LV1	IRQ LV0	IRQ3	IRQ2	IRQ1	IRQ0	IRQ3	IRQ2	IRQ1	IRQ0	IRQ3	IRQ2	IRQ1	IRQ0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

14~12 IRQ pin interrupt priority levels 000 (level 0)~110 (level 6)

11~8 IRQ3~0 pin interrupt enable flags Disable/enable interrupts

7~4 IRQ3~0 pin interrupt request flags No interrupt request/generate interrupt request

3~0 IRQ3~0 pin interrupt detection flags No detection/interrupt detection

G8ICR: x'00FC50'

Maskable Interrupt Control Register (Group) 8

8/16-bit access register

Interrupt pins IRQ3~IRQ0 correspond to port 4 (P43~P40).

G

The external pin interrupt condition control register, EXTMD, sets the interrupt conditions.

Set to 1 when an external interrupt occurs.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	SC LV2	SC LV1	SC LV0	SC1R IE	SC1T IE	SC0R IE	SC0T IE	SC1R IR	SC1T IR	SC0R IR	SC0T IR	SC1R ID	SC1T ID	SC0R ID	SC0T ID
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

G9ICR:
x'00FC52'

Maskable Interrupt
Control Register
(Group) 9

8/16-bit access register

14~12 Serial interface interrupt priority levels 000 (level 0)~110 (level 6)

11 Serial interface 1 reception complete interrupt enable flag

Disable/enable interrupt

10 Serial interface 1 transmission complete interrupt enable flag

9 Serial interface 0 reception complete interrupt enable flag

8 Serial interface 0 transmission complete interrupt enable flag

Set to 1 when the serial transfer is complete.

7 Serial interface 1 reception complete interrupt request flag

No interrupt request/generate interrupt request

6 Serial interface 1 transmission complete interrupt request flag

5 Serial interface 0 reception complete interrupt request flag

4 Serial interface 0 transmission complete interrupt request flag

3 Serial interface 1 reception complete interrupt detection flag

No detection/interrupt detection

2 Serial interface 1 transmission complete interrupt detection flag

1 Serial interface 0 reception complete interrupt detection flag

0 Serial interface 0 transmission complete interrupt detection flag

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	GP8 LV2	GP8 LV1	GP8 LV0	-	-	AN IE	KI IE	-	-	AN IR	KI IR	-	-	AN ID	KI ID
R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0	0	0/1	0/1	0	0	0/1	0/1	0	0	0/1	0/1

14~12 Group 10 interrupt priority levels 000 (level 0) ~ 110 (level 6)

9 A/D conversion complete interrupt enable flag

Disable/enable interrupts

8 $\overline{KI7} \sim \overline{KI0}$ pin interrupt enable flag

No interrupt request/generate interrupt request

5 A/D conversion complete interrupt request flag

No detection/interrupt detection

4 $\overline{KI7} \sim \overline{KI0}$ pin interrupt request flag

Set to 1 after the completion of A/D conversion or when key input occurs.

1 A/D conversion complete interrupt detection flag

The setting of interrupt conditions is performed by external pin interrupt condition control register, EXTMD, and port 0 direction control register, P0DIR.

0 $\overline{KI7} \sim \overline{KI0}$ pin interrupt detection flag

8/16-bit access register

Key input pins $\overline{KI7} \sim \overline{KI0}$ correspond to port 0 (P07~P00). Therefore, if even one of the above pins is used as a port, set the KIIE bit to '0' since key input interrupts cannot be used.

G

G10ICR: x'00FC54'

Maskable Interrupt Control Register (Group) 10

14~12 Group 10 interrupt priority levels

Key input pins $\overline{KI7} \sim \overline{KI0}$ correspond to port 0 (P07~P00). Therefore, if even one of the above pins is used as a port, set the KIIE bit to '0' since key input interrupts cannot be used.

Set to 1 after the completion of A/D conversion or when key input occurs.

The setting of interrupt conditions is performed by external pin interrupt condition control register, EXTMD, and port 0 direction control register, P0DIR.

EXTMD:
x'00FC56'

External Interrupt Condition Control Register

8/16-bit access register

15	Port 43 input value
14	Port 42 input value
13	Port 41 input value
12	Port 40 input value

9, 8	$\overline{K1}$ pin interrupt conditions	00: 'L' level at one of the $\overline{K1}$ pins 01: reserved 10: negative (falling) edge at one of the $\overline{K1}$ pins 11: reserved
------	--	--

7, 6	IRQ3 pin interrupt conditions	00: 'L' level 01: 'H' level 10: negative (falling) edge 11: positive (rising) edge
------	-------------------------------	---

5, 4	IRQ2 pin interrupt conditions	00: 'L' level 01: 'H' level 10: negative (falling) edge 11: positive (rising) edge
------	-------------------------------	---

3, 2	IRQ1 pin interrupt conditions	00: 'L' level 01: 'H' level 10: negative (falling) edge 11: positive (rising) edge
------	-------------------------------	---

1, 0	IRQ0 pin interrupt conditions	00: 'L' level 01: 'H' level 10: negative (falling) edge 11: positive (rising) edge
------	-------------------------------	---

'L' level is normally set when a key input interrupt is used. If any one of the key input setting pins for K17~K10 goes to a 'L' level, an interrupt request signal will be activated. 'L' level is set if used during a STOP. Edge interrupts cannot be initiated during a STOP.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	SIZE1	SIZE0	-	-	-	REFE	-	-	PS RAM	PAGE	-	-	-	DRAM CE
R	R	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W	R	R	R	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0/1	0/1	0	0	0	0/1	0	0	0/1	0/1	0	0	0	0/1

DRMCTR:
x'00FD00'

DRAM Control
Register

8/16-bit access register

D

E

13, 12 DRAM area size	00: reserved 01: 256 KB or 512 KB 10: 1 MB or 2 MB 11: 4 MB or 8 MB
-----------------------	--

8 Refresh enable disable/enable

5 DRAM/Pseudo SRAM selection DRAM/pseudo SRAM

4 Page mode setting disable/enable

0 DRAM interface control disable/enable

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REF															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

REFCNT:
x'00FD02'

Refresh Counter

8/16-bit access register

R

15~0 Refresh counter refresh interval setting

Since the refresh counter is a countdown register synchronized with SYSCLK, the refresh interval is the set value multiplied by the SYSCLK interval.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SC0 TEN	SC0 REN	SC0 BRE	-	SC0 PTL	-	SC0 OD	-	SC0 LN	SC0 PTY2	SC0 PTY1	SC0 PTY0	SC0 SB	-	SC0 S1	SC0 S0
R/W	R/W	R/W	R	R/W	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0	0/1	0	0/1	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0/1

SC0CTR:
x'00FD80'

**Serial 0 Control
Register**

8/16-bit access register

15	Transmit enable	disable/enable	
14	Receive enable	disable/enable	
13	Break transmit	do not break/break (SBO is 0)	
11	Protocol	asynchronous/synchronous	
9	Bit transmission order	LSB first/MSB first	"LSB first" is the only setting for 7-bit transfers.
7	Character length	7 bits/8 bits	
6~4	Parity bit	000: no parity 001: [] 010: [] prohibited (reserved) 011: [] 100: fixed 0 ('L' output) 101: fixed 1 ('H' output) 110: even (number of 1's are even) 111:odd (number of 1's are odd)	
3	Stop bit	1 bit/ 2 bits	
1, 0	Clock source	00: SBT0 pin 01: 1/8th of timer 8 underflow 10: prohibited (reserved) 11: 1/8th of timer 9 underflow	Stop bit selection is only valid when in the asynchronous mode.

7	6	5	4	3	2	1	0
SC0							
TRB7	TRB6	TRB5	TRB4	TRB3	TRB2	TRB1	TRB0
R/W							
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

SC0TRB:
x'00FD82'

**Serial 0 Transmit/
Receive Buffer**

8/16-bit access register

7~0 Serial transit/receive data

During serial transmission, data transmission begins when data is written to the SC0TRB register. Once the data has been written, the transmission begins 1 to 2 clock (underflow of timer 8 or 9) cycles later. For 7-bit transmission, the MSB (bit 7) is ignored.

During serial reception, data is taken in by reading the SC0TRB register. When an interrupt occurs or the SC0RXA flag of SC0STR is 1, the received data can be read. For 7-bit transmission, the MSB (bit 7) is 0.

S

7	6	5	4	3	2	1	0
SC0 TBSY	SC0 RBSY	-	SC0 RXA	-	SC0 FE	SC0 PE	SC0 OE
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0	0/1	0	0/1	0/1	0/1

SC0STR:
x'00FD83'

**Serial 0 Status
Register**

8-bit access register
(16-bit access is possible from
an even address)

7	Transmit status flag	ready to transmit/transmitting	
6	Receive status flag	waiting/receiving	
4	Received data flag	not present/present	
2	Framing error	no error/error	<i>Framing errors occur when 0 is received during a stop bit transmission. Error information is updated when the stop bit is received.</i>
1	Parity error	no error/error	<i>Parity errors occur if the parity bit was fixed at 0 and 1 was received, if fixed at 1 and 0 is was received, if set for even and odd was received, or if set for odd and even was received. Error information is updated when the parity bits are received.</i>
0	Overrun error	no error/error	<i>Overrun errors occur when new data is received in the serial transmit/receive register (SC0TRB) before the old data can be read. Error information is updated when the last data bit has been received.</i>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SC1 TEN	SC1 REN	SC1 BRE	-	SC1 PTL	-	SC1 OD	-	SC1 LN	SC1 PTY2	SC1 PTY1	SC1 PTY0	SC1 SB	-	SC1 S1	SC1 S0
R/W	R/W	R/W	R	R/W	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0	0/1	0	0/1	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0/1

SC1CTR:
x'00FD90'

Serial 1 Control Register

8/16-bit access register

15	Transmit enable	disable/enable	
14	Receive enable	disable/enable	
13	Break transmit	do not break/break (SBO is 0)	
11	Protocol	asynchronous/synchronous	
9	Bit transmission order	LSB first/MSB first	"LSB first" is the only setting for 7-bit transfers.
7	Character length	7 bits/8 bits	
6~4	Parity bit	000: no parity 001: 010: [] prohibited (reserved) 011: 100: fixed 0 ('L' output) 101: fixed 1 ('H' output) 110: even (number of 1's are even) 111: odd (number of 1's are odd)	
3	Stop bit	1 bit/ 2 bits	
1, 0	Clock source	00: SBT1 pin 01: 1/8th of timer 8 underflow 10: prohibited (reserved) 11: 1/8th of timer 9 underflow	Stop bit selection is only valid when in the asynchronous mode.

S

7	6	5	4	3	2	1	0
SC1							
TRB7	TRB6	TRB5	TRB4	TRB3	TRB2	TRB1	TRB0
R/W							
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

SC1TRB:
x'00FD92'

**Serial 1 Transmit/
Receive Buffer**

8/16-bit access register

7~0 Serial transit/receive data

During serial transmission, data transmission begins when data is written to the SC1TRB register. Once the data has been written, the transmission begins 1 to 2 clock (underflow of timer 8 or 9) cycles later. For 7-bit transmission, the MSB (bit 7) is ignored.

During serial reception, data is taken in by reading the SC1TRB register. When an interrupt occurs or the SC1RXA flag of SC1STR is 1, the received data can be read. For 7-bit transmission, the MSB (bit 7) is 0.

7	6	5	4	3	2	1	0
SC1 TBSY	SC1 RBSY	-	SC1 RXA	-	SC1 FE	SC1 PE	SC1 OE
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0	0/1	0	0/1	0/1	0/1

SC1STR:
x'00FD93'

Serial 1 Status Register

8-bit access register

(16-bit access is possible from
an even address)

- | | | | |
|---|----------------------|--------------------------------|---|
| 7 | Transmit status flag | ready to transmit/transmitting | an even address) |
| 6 | Receive status flag | waiting/receiving | |
| 4 | Received data flag | not present/present | |
| 2 | Framing error | no error/error | <p><i>Framing errors occur when 0 is received during a stop bit transmission.</i></p> <p><i>Error information is updated when the stop bit is received.</i></p> |
| 1 | Parity error | no error/error | <p><i>Parity errors occur if the parity bit was fixed at 0 and 1 was received, if fixed at 1 and 0 was received, if set for even and odd was received, or if set for odd and even was received.</i></p> <p><i>Error information is updated when the parity bits are received.</i></p> |
| 0 | Overrun error | no error/error | <p><i>Overrun errors occur when new data is received in the serial transmit/receive register (SC1TRB) before the old data can be read.</i></p> <p><i>Error information is updated when the last data bit has been received.</i></p> |

S

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	AN NCH2	AN NCH1	AN NCHO	-	AN 1CH2	AN 1CH1	AN 1CH0	AN EN	AN ST	-	-	AN CK1	AN CK0	AN MD1	AN MD0
R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0	0/1	0/1	0/1	0/1	0/1	0	0	0/1	0/1	0/1	0/1

ANCTR:
x'00FDA0'

AN Conversion Control Register

8/16-bit access register

14~12	Channel numbers during conversion of multiple channels	000: AN0 001: AN0, 1 010: AN0, 1, 2 011: AN0, 1, 2, 3 100: AN0, 1, 2, 3, 4 101: AN0, 1, 2, 3, 4, 5 110: AN0, 1, 2, 3, 4, 5, 6 111: AN0, 1, 2, 3, 4, 5, 6, 7
10~8	Channel number during conversion of arbitrary one channel	000 (AN0)~111 (AN7)
7	Conversion start and execute enable flag	prohibited/start conversion or conversion in progress
6	Perform A/D conversion based on timer 7	stop/execute
3, 2	Clock	00: SYSCLK 01: SYSCLK divided by 2 10: SYSCLK divided by 4 11: SYSCLK divided by 8
1, 0	Operating mode	00: single-shot conversion on arbitrary one channel 01: single-shot conversion on multiple channels 10: continuous conversion on arbitrary one channel 11: continuous conversion on multiple channels

For 10~20MHz oscillation, 10 and 11 are possible. For oscillations of 5~10MHz, 01, 10, and 11 are possible. For oscillation of 5MHz and below, all choices are possible.

7	6	5	4	3	2	1	0
AN0							
BUF7	BUF6	BUF5	BUF4	BUF3	BUF2	BUF1	BUF0
R	R	R	R	R	R	R	R
Undefined							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Channel 0 (AN0 pin)
A/D conversion results

AN0BUF:
x'00FDA8'

**AN0 Conversion
Data Buffer**

8/16-bit access register

This register is read only.

7	6	5	4	3	2	1	0
AN1							
BUF7	BUF6	BUF5	BUF4	BUF3	BUF2	BUF1	BUF0
R	R	R	R	R	R	R	R
Undefined							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Channel 1 (AN1 pin)
A/D conversion results

AN1BUF:
x'00FDA9'

**AN1 Conversion
Data Buffer**

8-bit access register

(16-bit access is possible from
an even address)

This register is read only.

7	6	5	4	3	2	1	0
AN2							
BUF7	BUF6	BUF5	BUF4	BUF3	BUF2	BUF1	BUF0
R	R	R	R	R	R	R	R
Undefined							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Channel 2 (AN2 pin)
A/D conversion results

AN2BUF:
x'00FDAA'

**AN2 Conversion
Data Buffer**

8/16-bit access register

This register is read only.

7	6	5	4	3	2	1	0
AN3 BUF7	AN3 BUF6	AN3 BUF5	AN3 BUF4	AN3 BUF3	AN3 BUF2	AN3 BUF1	AN3 BUF0
R	R	R	R	R	R	R	R
Undefined							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Channel 3 (AN3 pin)
A/D conversion results

AN3BUF:
x'00FDAB'

**AN3 Conversion
Data Buffer**

8-bit access register
(16-bit access is possible from
an even address)
This register is read only.

7	6	5	4	3	2	1	0
AN4 BUF7	AN4 BUF6	AN4 BUF5	AN4 BUF4	AN4 BUF3	AN4 BUF2	AN4 BUF1	AN4 BUF0
R	R	R	R	R	R	R	R
Undefined							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Channel 4 (AN4 pin)
A/D conversion results

AN4BUF:
x'00FDAC'

**AN4 Conversion
Data Buffer**

8/16-bit access register
This register is read only.

7	6	5	4	3	2	1	0
AN5 BUF7	AN5 BUF6	AN5 BUF5	AN5 BUF4	AN5 BUF3	AN5 BUF2	AN5 BUF1	AN5 BUF0
R	R	R	R	R	R	R	R
Undefined							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Channel 5 (AN5 pin)
A/D conversion results

AN5BUF:
x'00FDAD'

**AN5 Conversion
Data Buffer**

8-bit access register
(16-bit access is possible from
an even address)

This register is read only.

7	6	5	4	3	2	1	0
AN6							
BUF7	BUF6	BUF5	BUF4	BUF3	BUF2	BUF1	BUF0
R	R	R	R	R	R	R	R
Undefined							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

AN6BUF:
x'00FDAE'

**AN6 Conversion
Data Buffer**

8/16-bit access register

7~0 Channel 6 (AN6 pin)
A/D conversion results

This register is read only.

7	6	5	4	3	2	1	0
AN7							
BUF7	BUF6	BUF5	BUF4	BUF3	BUF2	BUF1	BUF0
R	R	R	R	R	R	R	R
Undefined							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

AN7BUF:
x'00FDAD'

**AN7 Conversion
Data Buffer**

8-bit access register

(16-bit access is possible from
an even address)

This register is read only.

7~0 Channel 7 (AN7 pin)
A/D conversion results

Chapter 10 Appendix

7	6	5	4	3	2	1	0
TM0 BC7	TM0 BC6	TM0 BC5	TM0 BC4	TM0 BC3	TM0 BC2	TM0 BC1	TM0 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 0 count value

TM0BC:
x'00FE00'

Timer 0 Binary Counter

8/16-bit access register

This register is read only.

7	6	5	4	3	2	1	0
TM1 BC7	TM1 BC6	TM1 BC5	TM1 BC4	TM1 BC3	TM1 BC2	TM1 BC1	TM1 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 1 count value

TM1BC:
x'00FE01'

Timer 1 Binary Counter

8-bit access register

(16-bit access is possible from an even address)

This register is read only.

7	6	5	4	3	2	1	0
TM2 BC7	TM2 BC6	TM2 BC5	TM2 BC4	TM2 BC3	TM2 BC2	TM2 BC1	TM2 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 2 count value

TM2BC:
x'00FE02'

Timer 2 Binary Counter

8/16-bit access register

This register is read only.

7	6	5	4	3	2	1	0
TM3 BC7	TM3 BC6	TM3 BC5	TM3 BC4	TM3 BC3	TM3 BC2	TM3 BC1	TM3 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 3 count value

TM3BC:
x'00FE03'

Timer 3 Binary Counter

8-bit access register

(16-bit access is possible from an even address)

This register is read only.

7	6	5	4	3	2	1	0
TM4 BC7	TM4 BC6	TM4 BC5	TM4 BC4	TM4 BC3	TM4 BC2	TM4 BC1	TM4 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 4 count value

TM4BC:
x'00FE04'

Timer 4 Binary Counter

8/16-bit access register

This register is read only.

7	6	5	4	3	2	1	0
TM5 BC7	TM5 BC6	TM5 BC5	TM5 BC4	TM5 BC3	TM5 BC2	TM5 BC1	TM5 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 5 count value

TM5BC:
x'00FE05'

Timer 5 Binary Counter

8-bit access register

(16-bit access is possible from an even address)

This register is read only.

T

7	6	5	4	3	2	1	0
TM6 BC7	TM6 BC6	TM6 BC5	TM6 BC4	TM6 BC3	TM6 BC2	TM6 BC1	TM6 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 6 count value

TM6BC:
x'00FE06'

Timer 6 Binary Counter

8/16-bit access register

This register is read only.

7	6	5	4	3	2	1	0
TM7 BC7	TM7 BC6	TM7 BC5	TM7 BC4	TM7 BC3	TM7 BC2	TM7 BC1	TM7 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 7 count value

TM7BC:
x'00FE07'

Timer 7 Binary Counter

8-bit access register

(16-bit access is possible from an even address)

This register is read only.

7	6	5	4	3	2	1	0
TM8 BC7	TM8 BC6	TM8 BC5	TM8 BC4	TM8 BC3	TM8 BC2	TM8 BC1	TM8 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 8 count value

TM8BC:
x'00FE08'

Timer 8 Binary Counter

8/16-bit access register

This register is read only.

7	6	5	4	3	2	1	0
TM9 BC7	TM9 BC6	TM9 BC5	TM9 BC4	TM9 BC3	TM9 BC2	TM9 BC1	TM9 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 9 count value

TM9BC:
x'00FE09'

Timer 9 Binary Counter

8-bit access register

(16-bit access is possible from an even address)

This register is read only.

7	6	5	4	3	2	1	0
PS0 BC7	PS0 BC6	PS0 BC5	PS0 BC4	PS0 BC3	PS0 BC2	PS0 BC1	PS0 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Prescaler 0 count value

PS0BC:
x'00FE0A'

Prescaler 0 Binary Counter

8/16-bit access register

The register is read only.

P

7	6	5	4	3	2	1	0
PS1 BC7	PS1 BC6	PS1 BC5	PS1 BC4	PS1 BC3	PS1 BC2	PS1 BC1	PS1 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Prescaler 1 count value

PS1BC:
x'00FE0B'

Prescaler 1 Binary Counter

8-bit access register

(16-bit access is possible from an even address)

This register is read only.

T

7	6	5	4	3	2	1	0
TM0							
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
R/W							
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 0 count cycle

Sets the count cycle (2~256). Since the set value + 1 are counted, set the count cycle to a value between 1 and 255.

TM0BR:
x'00FE10'

Timer 0 Base Register
8/16-bit access register

A value of 0 may be set after startup. Refer to section 4-2, "Examples of 8-bit Timer Settings" for further details.

7	6	5	4	3	2	1	0
TM1							
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
R/W							
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 1 count cycle

Sets the count cycle (2~256). Since the set value + 1 are counted, set the count cycle to a value between 1 and 255.

TM1BR:
x'00FE11'

Timer 1 Base Register
8-bit access register
(16-bit access is possible from an even address)

A value of 0 may be set after startup. Refer to section 4-2, "Examples of 8-bit Timer Settings" for further details.

7	6	5	4	3	2	1	0
TM2							
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
R/W							
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 2 count cycle

Sets the count cycle (2~256). Since the set value + 1 are counted, set the count cycle to a value between 1 and 255.

TM2BR:
x'00FE12'

Timer 2 Base Register
8/16-bit access register

A value of 0 may be set after startup. Refer to section 4-2, "Examples of 8-bit Timer Settings" for further details.

7	6	5	4	3	2	1	0
TM3 BR7	TM3 BR6	TM3 BR5	TM3 BR4	TM3 BR3	TM3 BR2	TM3 BR1	TM3 BR0
R/W							
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 3 count cycle

Sets the count cycle (2~256). Since the set value + 1 are counted, set the count cycle to a value between 1 and 255.

TM3BR:
x'00FE13'

Timer 3 Base Register

8-bit access register

(16-bit access is possible from an even address)

A value of 0 may be set after startup. Refer to section 4-2, "Examples of 8-bit Timer Settings" for further details.

7	6	5	4	3	2	1	0
TM4 BR7	TM4 BR6	TM4 BR5	TM4 BR4	TM4 BR3	TM4 BR2	TM4 BR1	TM4 BR0
R/W							
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 4 count cycle

Sets the count cycle (2~256). Since the set value + 1 are counted, set the count cycle to a value between 1 and 255.

TM4BR:
x'00FE14'

Timer 4 Base Register

8/16-bit access register

A value of 0 may be set after startup. Refer to section 4-2, "Examples of 8-bit Timer Settings" for further details.

7	6	5	4	3	2	1	0
TM5 BR7	TM5 BR6	TM5 BR5	TM5 BR4	TM5 BR3	TM5 BR2	TM5 BR1	TM5 BR0
R/W							
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 5 count cycle

Sets the count cycle (2~256). Since the set value + 1 are counted, set the count cycle to a value between 1 and 255.

TM5BR:
x'00FE15'

Timer 5 Base Register

8-bit access register

(16-bit access is possible from an even address)

A value of 0 may be set after startup. Refer to section 4-2, "Examples of 8-bit Timer Settings" for further details.

T

7	6	5	4	3	2	1	0
TM6							
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
R/W							
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 6 count cycle

Sets the count cycle (2~256). Since the set value + 1 are counted, set the count cycle to a value between 1 and 255.

TM6BR:
x'00FE16'

Timer 6 Base Register
8/16-bit access register

A value of 0 may be set after startup. Refer to section 4-2, "Examples of 8-bit Timer Settings" for further details.

7	6	5	4	3	2	1	0
TM7							
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
R/W							
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 7 count cycle

Sets the count cycle (2~256). Since the set value + 1 are counted, set the count cycle to a value between 1 and 255.

TM7BR:
x'00FE17'

Timer 7 Base Register
8-bit access register
(16-bit access is possible from an even address)

A value of 0 may be set after startup. Refer to section 4-2, "Examples of 8-bit Timer Settings" for further details.

7	6	5	4	3	2	1	0
TM8							
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
R/W							
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Timer 8 count cycle

Sets the count cycle (2~256). Since the set value + 1 are counted, set the count cycle to a value between 1 and 255.

TM8BR:
x'00FE18'

Timer 8 Base Register
8/16-bit access register

A value of 0 may be set after startup. Refer to section 4-2, "Examples of 8-bit Timer Settings" for further details.

7	6	5	4	3	2	1	0
TM9 BR7	TM9 BR6	TM9 BR5	TM9 BR4	TM9 BR3	TM9 BR2	TM9 BR1	TM9 BR0
R/W							
0 0/1							

7~0 Timer 9 count cycle

Sets the count cycle (2~256). Since the set value + 1 are counted, set the count cycle to a value between 1 and 255.

TM9BR:
x'00FE19'

Timer 9 Base Register

8-bit access register

(16-bit access is possible from an even address)

A value of 0 may be set after startup. Refer to section 4-2, "Examples of 8-bit Timer Settings" for further details.

7	6	5	4	3	2	1	0
PS0 BR7	PS0 BR6	PS0 BR5	PS0 BR4	PS0 BR3	PS0 BR2	PS0 BR1	PS0 BR0
R/W							
0 0/1							

7~0 Prescaler 0 count cycle

Sets the count cycle (1~256). Since the set value + 1 are counted, set the count cycle to a value between 0 and 255.

PS0BR:
x'00FE1A'

Prescaler 0 Base Register

8/16-bit access register

A value of 0 may be set after startup. Refer to section 4-2, "Examples of 8-bit Timer Settings" for further details.

P

7	6	5	4	3	2	1	0
PS1 BR7	PS1 BR6	PS1 BR5	PS1 BR4	PS1 BR3	PS1 BR2	PS1 BR1	PS1 BR0
R/W							
0 0/1							

7~0 Prescaler 1 count cycle

Sets the count cycle (1~256). Since the set value + 1 are counted, set the count cycle to a value between 0 and 255.

PS1BR:
x'00FE1B'

Prescaler 1 Base Register

8-bit access register

(16-bit access is possible from an even address)

A value of 0 may be set after startup. Refer to section 4-2, "Examples of 8-bit Timer Settings" for further details.

T

7	6	5	4	3	2	1	0
TM0 EN	TM0 LD	-	-	-	-	TM0 S1	TM0 S0
R/W	R/W	R	R	R	R	R/W	R/W
0 0/ 1	0 0/ 1	0 0	0 0	0 0	0 0	0 0/ 1	0 0/ 1

TM0MD:
x'00FE20'

**Timer 0 Mode
Register**

8/16-bit access register

- | | | |
|------|---------------------------------|---|
| 7 | Timer 0 count operation control | stop counting/count operation |
| 6 | Timer 0 base register setting | no function/set TM0BR to TM0BC, reset divide by 2 circuit, fix TMIO output at 0 |
| 1, 0 | Clock source | 00: TM0IO pin clock (event timer)
01: reserved
10: prescaler 0 clock
11: prescaler 1 clock |

7	6	5	4	3	2	1	0
TM1 EN	TM1 LD	-	-	-	-	TM1 S1	TM1 S0
R/W	R/W	R	R	R	R	R/W	R/W
0 0/ 1	0 0/ 1	0 0	0 0	0 0	0 0	0 0/ 1	0 0/ 1

TM1MD:
x'00FE21'

**Timer 1 Mode
Register**

8-bit access register
(16-bit access is possible from an even address)

- | | | |
|------|---------------------------------|---|
| 7 | Timer 1 count operation control | stop counting/count operation |
| 6 | Timer 1 base register setting | no function/set TM1BR to TM1BC, reset divide by 2 circuit, fix TMIO output at 0 |
| 1, 0 | Clock source | 00: TM1IO pin clock (event timer)
01: timer 0 cascade connection
10: prescaler 0 clock
11: prescaler 1 clock |

7	6	5	4	3	2	1	0
TM2 EN	TM2 LD	-	-	-	-	TM2 S1	TM2 S0
R/W	R/W	R	R	R	R	R/W	R/W
0 0/1	0 0/1	0 0	0 0	0 0	0 0	0 0/1	0 0/1

TM2MD:
x'00FE22'

**Timer 2 Mode
Register**

8/16-bit access register

- | | | |
|------|---------------------------------|---|
| 7 | Timer 2 count operation control | stop counting/count operation |
| 6 | Timer 2 base register setting | no function/set TM2BR to TM2BC, reset divide by 2 circuit, fix TMIO output at 0 |
| 1, 0 | Clock source | 00: TM2IO pin clock (event timer)
01: timer 1 cascade connection
10: prescaler 0 clock
11: prescaler 1 clock |

7	6	5	4	3	2	1	0
TM3 EN	TM3 LD	-	-	-	-	TM3 S1	TM3 S0
R/W	R/W	R	R	R	R	R/W	R/W
0 0/1	0 0/1	0 0	0 0	0 0	0 0	0 0/1	0 0/1

TM3MD:
x'00FE23'

**Timer 3 Mode
Register**

8-bit access register
(16-bit access is possible from an even address)

- | | | |
|------|---------------------------------|---|
| 7 | Timer 3 count operation control | stop counting/count operation |
| 6 | Timer 3 base register setting | no function/set TM3BR to TM3BC, reset divide by 2 circuit, fix TMIO output at 0 |
| 1, 0 | Clock source | 00: TM3IO pin clock (event timer)
01: timer 2 cascade connection
10: prescaler 0 clock
11: prescaler 1 clock |

T

7	6	5	4	3	2	1	0
TM4 EN	TM4 LD	-	-	-	-	TM4 S1	TM4 S0
R/W	R/W	R	R	R	R	R/W	R/W
0 0/1	0 0/1	0 0	0 0	0 0	0 0	0 0/1	0 0/1

TM4MD:
x'00FE24'

**Timer 4 Mode
Register**

8/16-bit access register

- | | | |
|------|---------------------------------|---|
| 7 | Timer 4 count operation control | stop counting/count operation |
| 6 | Timer 4 base register setting | no function/set TM4BR to TM4BC, reset divide by 2 circuit, fix TMIO output at 0 |
| 1, 0 | Clock source | 00: TM4IO pin clock (event timer)
01: timer 3 cascade connection
10: prescaler 0 clock
11: prescaler 1 clock |

7	6	5	4	3	2	1	0
TM5 EN	TM5 LD	-	-	-	-	TM5 S1	TM5 S0
R/W	R/W	R	R	R	R	R/W	R/W
0 0/1	0 0/1	0 0	0 0	0 0	0 0	0 0/1	0 0/1

TM5MD:
x'00FE25'

**Timer 5 Mode
Register**

8-bit access register

- | | | |
|------|---------------------------------|---|
| 7 | Timer 5 count operation control | stop counting/count operation |
| 6 | Timer 5 base register setting | no function/set TM5BR to TM5BC, reset divide by 2 circuit, fix TMIO output at 0 |
| 1, 0 | Clock source | 00: TM5IO pin clock (event timer)
01: timer 4 cascade connection
10: prescaler 0 clock
11: prescaler 1 clock |

(16-bit access is possible from an even address)

7	6	5	4	3	2	1	0
TM6 EN	TM6 LD	-	-	-	-	TM6 S1	TM6 S0
R/W	R/W	R	R	R	R	R/W	R/W
0 0/1	0 0/1	0 0	0 0	0 0	0 0	0 0/1	0 0/1

TM6MD:
x'00FE26'

**Timer 6 Mode
Register**

8/16-bit access register

- | | | |
|------|---------------------------------|---|
| 7 | Timer 6 count operation control | stop counting/count operation |
| 6 | Timer 6 base register setting | no function/set TM6BR to TM6BC, reset divide by 2 circuit, fix TMIO output at 0 |
| 1, 0 | Clock source | 00: TM6IO pin clock (event timer)
01: timer 5 cascade connection
10: prescaler 0 clock
11: prescaler 1 clock |

7	6	5	4	3	2	1	0
TM7 EN	TM7 LD	-	-	-	-	TM7 S1	TM7 S0
R/W	R/W	R	R	R	R	R/W	R/W
0 0/1	0 0/1	0 0	0 0	0 0	0 0	0 0/1	0 0/1

TM7MD:
x'00FE27'

**Timer 7 Mode
Register**

8-bit access register
(16-bit access is possible from an even address)

- | | | |
|------|---------------------------------|---|
| 7 | Timer 7 count operation control | stop counting/count operation |
| 6 | Timer 7 base register setting | no function/set TM7BR to TM7BC, reset divide by 2 circuit, fix TMIO output at 0 |
| 1, 0 | Clock source | 00: TM7IO pin clock (event timer)
01: timer 6 cascade connection
10: prescaler 0 clock
11: prescaler 1 clock |

T

7	6	5	4	3	2	1	0
TM8 EN	TM8 LD	-	-	-	-	TM8 S1	TM8 S0
R/W	R/W	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0	0	0	0	0/1	0/1

TM8MD:
x'00FE28'

**Timer 8 Mode
Register**

8/16-bit access register

- | | | |
|------|---------------------------------|---|
| 7 | Timer 8 count operation control | stop counting/count operation |
| 6 | Timer 8 base register setting | no function/set TM8BR to TM8BC, reset divide by 2 circuit, fix TMIO output at 0 |
| 1, 0 | Clock source | 00: TM8IO pin clock (event timer)
01: timer 7 cascade connection
10: prescaler 0 clock
11: prescaler 1 clock |

7	6	5	4	3	2	1	0
TM9 EN	TM9 LD	-	-	-	-	TM9 S1	TM9 S0
R/W	R/W	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0	0	0	0	0/1	0/1

TM9MD:
x'00FE29'

**Timer 9 Mode
Register**

8-bit access register
(16-bit access is possible from an even address)

- | | | |
|------|---------------------------------|---|
| 7 | Timer 9 count operation control | stop counting/count operation |
| 6 | Timer 9 base register setting | no function/set TM9BR to TM9BC, reset divide by 2 circuit, fix TMIO output at 0 |
| 1, 0 | Clock source | 00: TM9IO pin clock (event timer)
01: timer 8 cascade connection
10: prescaler 0 clock
11: prescaler 1 clock |

7	6	5	4	3	2	1	0
PS1 EN	PS1 LD	-	-	-	-	-	-
R/W	R/W	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0	0	0	0	0	0

PS0MD:
x'00FE2A'

Prescaler 0 Mode Register

8/16-bit access register

- | | | |
|---|-------------------------------------|--------------------------------|
| 7 | Prescaler 0 count operation control | stop counting/count operation |
| 6 | PS0BC setting | no function/set PS0BR to PS0BC |

7	6	5	4	3	2	1	0
PS1 EN	PS1 LD	-	-	-	-	-	-
R/W	R/W	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0	0	0	0	0	0

PS1MD:
x'00FE2B'

Prescaler 1 Mode Register

P

8-bit access register

(16-bit access is possible from an even address)

- | | | |
|---|-------------------------------------|--------------------------------|
| 7 | Prescaler 1 count operation control | stop counting/count operation |
| 6 | PS1BC setting | no function/set PS1BR to PS1BC |

T

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 EN	TM10 NLD	-	-	TM10 UD1	TM10 UDO	TM10 TGE	TM10 ONE	TM10 MD1	TM10 MDO	TM10 ECLR	TM10 LP	TM10 ASEL	TM10 S2	TM10 S1	TM10 SO
R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W						
0 0/1	0 0/1	0 0	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1

TM10MD:
x'00FE30'

Timer 10 Mode Register

16-bit access register

15	TM10BC count operation control	disable/enable	
14	TM10BC, T.F.F., RS.F.F operation selection	clear/operate	
11, 10	Up or down operation*	00: up counter 01: down counter 10: up when TM10IOA=1, down when =0 11: up when TM10IOB=1, down when =0	* Ignored when two-phase encoder is selected.
9	Count start external enable	disable/external trigger*	* TM10IOB (↓) sets TM10EN. When TM10BC=TM10CA, TM10EN is cleared.
8	Repeat or one-shot operation	repeat operation/one-shot operation	
7, 6	TM10CA, TM10CB operating modes	00: compare register (single buffer) is used 01: compare register (double buffer) is used 10: capture register is used TM10IOA (↑): capture A TM10IOA (↓): capture B 11: capture register is used TM10IOA (↑): capture A TM10IOB (↑): capture B	
5	When TM10IC pin is 1, TM10BC is	not cleared/cleared*	* Used with external synchronization.
4	When the values of TM10BC and TM10CA match, TM10BC is	not cleared/cleared*	* Used with PWM output.
3	Output to TM10IOA	RS.F.F. (one-phase)/T.F.F. (two-phase)	
2~0	Clock source	000: prescaler 0 clock 001: prescaler 1 clock 010: TM10IOB pin clock 011: SYSCLK clock 100: multiply by 4 two-phase encoder for TM10IOA, B 101: multiply by 1 two-phase encoder for TM10IOA, B 11*: reserved	With TM10LP=1 during up-counting, if TM10BC matches TM10CA, the count will continue to x'FFFF' and then in the next cycle, TM10BC will be cleared to 0. During down-counting, if TM10BC reaches 0, TM10BC will be set to the contents of TM10CA in the next cycle, regardless of the operation settings.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 BC15	TM10 BC14	TM10 BC13	TM10 BC12	TM10 BC11	TM10 BC10	TM10 BC9	TM10 BC8	TM10 BC7	TM10 BC6	TM10 BC5	TM10 BC4	TM10 BC3	TM10 BC2	TM10 BC1	TM10 BC0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15~0 Timer 10 count value

TM10BC:
x'00FE32'

Timer 10 Binary Counter

16-bit access register

This register is read only.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 CA15	TM10 CA14	TM10 CA13	TM10 CA12	TM10 CA11	TM10 CA10	TM10 CA9	TM10 CA8	TM10 CA7	TM10 CA6	TM10 CA5	TM10 CA4	TM10 CA3	TM10 CA2	TM10 CA1	TM10 CA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15~0 Timer 10 count cycle

set the count cycle – 1

TM10CA:
x'00FE34'

Timer 10 Compare/Capture Register A

16-bit access register

For capture settings, the captured value is read and a compare/capture A interrupt is generated. For compare settings, the PWM cycle is set. If using a single buffer and the values of TM10BC and TM10CA match, a compare/capture A interrupt will be generated.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 CAX15	TM10 CAX14	TM10 CAX13	TM10 CAX12	TM10 CAX11	TM10 CAX10	TM10 CAX9	TM10 CAX8	TM10 CAX7	TM10 CAX6	TM10 CAX5	TM10 CAX4	TM10 CAX3	TM10 CAX2	TM10 CAX1	TM10 CAX0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

15~0

As a register, read and write are not possible.
Only valid when the compare register has been set to double buffer.

TM10CAX:
x'00FE36'

Timer 10 Compare/Capture Register Set A

T

16-bit access register

For double buffer compare settings, the write signal of this register will cause the contents of TM10CA to be read. The PWM cycle is determined by TM10CAX. If the values of TM10BC and TM10CAX match, a compare/capture A interrupt will be generated and at the same time, the contents of TM10CA will be read.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 CB15	TM10 CB14	TM10 CB13	TM10 CB12	TM10 CB11	TM10 CB10	TM10 CB9	TM10 CB8	TM10 CB7	TM10 CB6	TM10 CB5	TM10 CB4	TM10 CB3	TM10 CB2	TM10 CB1	TM10 CB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15~0 Varies PWM or generates
interrupts

TM10CB:
x'00FE38'

**Timer 10 Compare/
Capture Register B**

16-bit access register

For capture settings, the captured value is read and a compare/capture B interrupt is generated. For compare settings, the PWM cycle is set. If using a single buffer and the values of TM10BC and TM10CB match, a compare/capture B interrupt will be generated.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 CBX15	TM10 CBX14	TM10 CBX13	TM10 CBX12	TM10 CBX11	TM10 CBX10	TM10 CBX9	TM10 CBX8	TM10 CBX7	TM10 CBX6	TM10 CBX5	TM10 CBX4	TM10 CBX3	TM10 CBX2	TM10 CBX1	TM10 CBX0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

15~0

As a register, read and write are not possible. Only valid when the compare register has been set to double buffer.

TM10CBX:
x'00FE3A'

**Timer 10 Compare/
Capture Register Set B**

16-bit access register

For double buffer compare settings, the write signal of this register will cause the contents of TM10CB to be read. The PWM cycle is determined by TM10CBX. If the values of TM10BC and TM10CBX match, a compare/capture B interrupt will be generated. If the values of TM10BC and TM10CAX, the contents of TM10CB will be read.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 EN	TM11 NLD	-	-	TM11 UD1	TM11 UDO	TM11 TGE	TM11 ONE	TM11 MD1	TC11 MD0	TM11 ECLR	TM11 LP	TM11 ASEL	TM11 S2	TM11 S1	TM11 S0
R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM11MD:
x'00FE40'

Timer 11 Mode Register

16-bit access register

15	TM11BC count operation control	disable/enable	
14	TM11BC, T.F.F., RS.F.F operation selection	clear/operate	
11, 10	Up or down operation*	00: up counter 01: down counter 10: up when TM11IOA=1, down when =0 11: up when TM11IOB=1, down when =0	* Ignored when two-phase encoder is selected.
9	Count start external enable	disable/external trigger*	* TM11IOB (↓) sets TM11EN. When TM11BC=TM11CA, TM11EN is cleared.
8	Repeat or one-shot operation	repeat operation/one-shot operation	
7, 6	TM11CA, TM11CB operating modes	00: compare register (single buffer) is used 01: compare register (double buffer) is used 10: capture register is used TM11IOA (↑): capture A TM11IOA (↓): capture B 11: capture register is used TM11IOA (↑): capture A TM11IOB (↑): capture B	
5	When TM11IC pin is 1, TM11BC is	not cleared/cleared*	* Used with external synchronization.
4	When the values of TM11BC and TM11CA match, TM11BC is	not cleared/cleared*	* Used with PWM output.
3	Output to TM11IOA	RS.F.F. (one-phase)/T.F.F. (two-phase)	
2~0	Clock source	000: prescaler 0 clock 001: prescaler 1 clock 010: TM11IOB pin clock 011: SYSCLK clock 100: multiply by 4 two-phase encoder for TM11IOA, B 101: multiply by 1 two-phase encoder for TM11IOA, B 11*: reserved	With TM11LP=1 during up-counting, if TM11BC matches TM11CA, the count will continue to x'FFFF' and then in the next cycle, TM11BC will be cleared to 0. During down-counting, if TM11BC reaches 0, TM11BC will be set to the contents of TM11CA in the next cycle, regardless of the operation settings.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 BC15	TM11 BC14	TM11 BC13	TM11 BC12	TM11 BC11	TM11 BC10	TM11 BC9	TM11 BC8	TM11 BC7	TM11 BC6	TM11 BC5	TM11 BC4	TM11 BC3	TM11 BC2	TM11 BC1	TM11 BC0
R 0 0/1															
0 0/1	0 0/1														

15~0 Timer 11 count value

TM11BC:
x'00FE42'

Timer 11 Binary Counter

16-bit access register

This register is read only.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 CA15	TM11 CA14	TM11 CA13	TM11 CA12	TM11 CA11	TM11 CA10	TM11 CA9	TM11 CA8	TM11 CA7	TM11 CA6	TM11 CA5	TM11 CA4	TM11 CA3	TM11 CA2	TM11 CA1	TM11 CA0
R/W 0 0/1															
0 0/1	0 0/1														

15~0 Timer 11 count cycle

set the count cycle – 1

TM11CA:
x'00FE44'

Timer 11 Compare/Capture Register A

16-bit access register

For capture settings, the captured value is read and a compare/capture A interrupt is generated. For compare settings, the PWM cycle is set. If using a single buffer and the values of TM11BC and TM11CA match, a compare/capture A interrupt will be generated.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 CAX15	TM11 CAX14	TM11 CAX13	TM11 CAX12	TM11 CAX11	TM11 CAX10	TM11 CAX9	TM11 CAX8	TM11 CAX7	TM11 CAX6	TM11 CAX5	TM11 CAX4	TM11 CAX3	TM11 CAX2	TM11 CAX1	TM11 CAX0
- 0 -	- 0 -	- 0 -	- 0 -	- 0 -	- 0 -	- 0 -	- 0 -	- 0 -	- 0 -	- 0 -	- 0 -	- 0 -	- 0 -		
0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	

15~0

As a register, read and write are not possible.
Only valid when the compare register has been set to double buffer.

TM11CAX:
x'00FE46'

Timer 11 Compare/Capture Register Set A

16-bit access register

For double buffer compare settings, the write signal of this register will cause the contents of TM11CA to be read. The PWM cycle is determined by TM11CAX. If the values of TM11BC and TM11CAX match, a compare/capture A interrupt will be generated and at the same time, the contents of TM11CA will be read.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11															
CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R/W															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15~0 Varies PWM or generates
interrupts

TM11CB: x'00FE48'

Timer 11 Compare/ Capture Register B

16-bit access register

For capture settings, the captured value is read and a compare/capture B interrupt is generated. For compare settings, the PWM cycle is set. If using a single buffer and the values of TM11BC and TM11CB match, a compare/capture B interrupt will be generated.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11	TM11	TM11	TM11	TM11	TM11	TM11	TM11	TM11	TM11	TM11	TM11	TM11	TM11	TM11	TM11
CBX15	CBX14	CBX13	CBX12	CBX11	CBX10	CBX9	CBX8	CBX7	CBX6	CBX5	CBX4	CBX3	CBX2	CBX1	CBX0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

15~0

As a register, read and write are not possible. Only valid when the compare register has been set to double buffer.

TM11CBX: x'00FE4A'

Timer 11 Compare/ Capture Register Set B

16-bit access register

For double buffer compare settings, the write signal of this register will cause the contents of TM11CB to be read. The PWM cycle is determined by TM11CBX. If the values of TM11BC and TM11CBX match, a compare/capture B interrupt will be generated. If the values of TM11BC and TM11CAX match, the contents of TM11CB will be read.

T

15	TM12EN	-	-	-	-	TM12TGE	TM12ONE	TM12MD1	TC12MD0	-	TM12LP	TM12ASEL	-	TM12S1	TM12S0
R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	0/1	0	0/1	0/1

TM12MD:
x'00FE50'

Timer 12 Mode Register

16-bit access register

15	TM12BC count operation control	disable/enable	
14	TM12BC, T.F.F., RS.F.F operation selection	clear/operate	
9	Count start external enable	disable/external trigger*	
8	Repeat or one-shot operation	repeat operation/one-shot operation	
7, 6	TM12CA, TM12CB operating modes	00: compare register (single buffer) is used 01: compare register (double buffer) is used 10: capture register is used TM12IOA (↑): capture A TM12IOA (↓): capture B 11: capture register is used TM12IOA (↑): capture A TM12IOB (↑): capture B	
4	When the values of TM12BC and TM12CA match, TM12BC is	not cleared/cleared*	* Used with PWM output.
3	Output to TM12IOA	RS.F.F. (one-phase)/T.F.F. (two-phase)	
1~0	Clock source	00: prescaler 0 clock 01: prescaler 1 clock 10: TM12IOB pin clock 11: SYSCLK clock	With TM12LP=1 during up-counting, if TM12BC matches TM12CA, the count will continue to x'FFFF' and then in the next cycle, TM12BC will be cleared to 0. During down-counting, if TM12BC reaches 0, TM12BC will be set to the contents of TM12CA in the next cycle, regardless of the operation settings.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM12 BC15	TM12 BC14	TM12 BC13	TM12 BC12	TM12 BC11	TM12 BC10	TM12 BC9	TM12 BC8	TM12 BC7	TM12 BC6	TM12 BC5	TM12 BC4	TM12 BC3	TM12 BC2	TM12 BC1	TM12 BC0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15~0 Timer 12 count value

TM12BC:
x'00FE52'

Timer 12 Binary Counter

16-bit access register

This register is read only.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM12 CA15	TM12 CA14	TM12 CA13	TM12 CA12	TM12 CA11	TM12 CA10	TM12 CA9	TM12 CA8	TM12 CA7	TM12 CA6	TM12 CA5	TM12 CA4	TM12 CA3	TM12 CA2	TM12 CA1	TM12 CA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15~0 Timer 12 count cycle

set the count cycle – 1

TM12CA:
x'00FE54'

Timer 12 Compare/Capture Register A

16-bit access register

For capture settings, the captured value is read and a compare/capture A interrupt is generated. For compare settings, the PWM cycle is set. If using a single buffer and the values of TM12BC and TM12CA match, a compare/capture A interrupt will be generated.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM12 CAX15	TM12 CAX14	TM12 CAX13	TM12 CAX12	TM12 CAX11	TM12 CAX10	TM12 CAX9	TM12 CAX8	TM12 CAX7	TM12 CAX6	TM12 CAX5	TM12 CAX4	TM12 CAX3	TM12 CAX2	TM12 CAX1	TM12 CAX0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15~0

As a register, read and write are not possible. Only valid when the compare register has been set to double buffer.

TM12CAX:
x'00FE56'

Timer 12 Compare/Capture Register Set A

16-bit access register

T

For double buffer compare settings, the write signal of this register will cause the contents of TM12CA to be read. The PWM cycle is determined by TM12CAX. If the values of TM12BC and TM12CAX match, a compare/capture A interrupt will be generated and the contents of TM12CA will be read.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM12 CB15	TM12 CB14	TM12 CB13	TM12 CB12	TM12 CB11	TM12 CB10	TM12 CB9	TM12 CB8	TM12 CB7	TM12 CB6	TM12 CB5	TM12 CB4	TM12 CB3	TM12 CB2	TM12 CB1	TM12 CB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15~0 Varies PWM or generates
interrupts

TM12CB:
x'00FE58'

**Timer 12 Compare/
Capture Register B**

16-bit access register

For capture settings, the captured value is read and a compare/capture B interrupt is generated. For compare settings, the PWM cycle is set. If using a single buffer and the values of TM12BC and TM12CB match, a compare/capture B interrupt will be generated.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM12 CBX15	TM12 CBX14	TM12 CBX13	TM12 CBX12	TM12 CBX11	TM12 CBX10	TM12 CBX9	TM12 CBX8	TM12 CBX7	TM12 CBX6	TM12 CBX5	TM12 CBX4	TM12 CBX3	TM12 CBX2	TM12 CBX1	TM12 CBX0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

15~0

As a register, read and write are not possible.
Only valid when the compare register has
been set to double buffer.

TM12CBX:
x'00FE5A'

**Timer 12 Compare/
Capture Register
Set B**

16-bit access register

For double buffer compare settings, the write signal of this register will cause the contents of TM12CB to be read. The PWM cycle is determined by TM12CBX. If the values of TM12BC and TM12CBX match, a compare/capture B interrupt will be generated. If the values of TM12BC and TM12CAX, the contents of TM12CB will be read.

7	6	5	4	3	2	1	0
-	-	-	SYA IRQ	SYA EN	SYA DIR	SYA MD1	SYA MDO
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0	0/1	0/1	0/1	0/1	0/1

SYAMD:
x'00FE60'

**Synchronous Output
A Mode Register**

8/16-bit access register

- | | | |
|-----|--|--|
| 4 | Timing for changing synchronous output | timer 1 underflow/timer 12A interrupt |
| 3 | Synchronous output enable | P13~P10/synchronous output A |
| 2 | Rotation direction | forward (CW)/reverse (CCW) |
| 1~0 | Operating modes | 00: arbitrary pattern output
(set by contents of SYSBUF)
01: 4-phase single excitation or 4-phase double excitation
10: 4-phase, 1-2 excitation
11: reserved |

7	6	5	4	3	2	1	0
-	-	-	SYB IRQ	SYB EN	SYB DIR	SYB MD1	SYB MDO
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0	0/1	0/1	0/1	0/1	0/1

SYBMD:
x'00FE61'

**Synchronous Output
B Mode Register**

8-bit access register

(16-bit access is possible from an even address)

- | | | |
|-----|--|--|
| 4 | Timing for changing synchronous output | timer 1 underflow/timer 12A interrupt |
| 3 | Synchronous output enable | P17~P14/synchronous output B |
| 2 | Rotation direction | forward (CW)/reverse (CCW) |
| 1~0 | Operating modes | 00: arbitrary pattern output
(set by contents of SYSBUF)
01: 4-phase single excitation or 4-phase double excitation
10: 4-phase, 1-2 excitation
11: reserved |

S
T

7	6	5	4	3	2	1	0
SYB BF3	SYB BF2	SYB BF1	SYB BF0	SYA BF3	SYA BF2	SYA BF1	SYA BF0
R/W							
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

SYBUF:
x'00FE62'

Synchronous Output Buffer

8/16-bit access register

7~4 Synchronous output B next pattern

During arbitrary pattern output, the pattern to be output at the next timing change

3~0 Synchronous output A next pattern

7	6	5	4	3	2	1	0
P1OUT7	P1OUT6	P1OUT5	P1OUT4	P1OUT3	P1OUT2	P1OUT1	P1OUT0
R/W							
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

P1OUT:
x'00FE64'

Port 1 Output Latch

8/16-bit access register

7~4 Synchronous output B initial output pattern

or Port 0 output pattern

3~0 Synchronous output A initial output pattern

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0 AR15	DMA0 AR14	DMA0 AR13	DMA0 AR12	DMA0 AR11	DMA0 AR10	DMA0 AR9	DMA0 AR8	DMA0 AR7	DMA0 AR6	DMA0 AR5	DMA0 AR4	DMA0 AR3	DMA0 AR2	DMA0 AR1	DMA0 AR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DMA0 AR23	DMA0 AR22	DMA0 AR21	DMA0 AR20	DMA0 AR19	DMA0 AR18	DMA0 AR17	DMA0 AR16
R	R	R	R	R	R	R	R	R/W							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DMA0 transfer address

sets the transfer address for channel 0

DM0TAPL:
x'00FE80'

D

DM0TAPH:
x'00FE82'

DMA0 Transfer Address Pointer

8/16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0 CT15	DMA0 CT14	DMA0 CT13	DMA0 CT12	DMA0 CT11	DMA0 CT10	DMA0 CT9	DMA0 CT8	DMA0 CT7	DMA0 CT6	DMA0 CT5	DMA0 CT4	DMA0 CT3	DMA0 CT2	DMA0 CT1	DMA0 CT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DMA0 CT23	DMA0 CT22	DMA0 CT21	DMA0 CT20	DMA0 CT19	DMA0 CT18	DMA0 CT17	DMA0 CT16
R	R	R	R	R	R	R	R	R/W							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DMA0 transfer count

sets the number of transfers for channel 0

DM0CNTL:
x'00FE84'

P

DM0CNTH:
x'00FE86'

DMA0 Transfer Count Register

8/16-bit access register

*After the transfer is completed,
the transfer count is 0.*

S

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	DMA0 IO9	DMA0 IO8	DMA0 IO7	DMA0 IO6	DMA0 IO5	DMA0 IO4	DMA0 IO3	DMA0 IO2	DMA0 IO1	DMA0 IO0
R	R	R	R	R	R	R/W									
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

9~0 DMA0 internal address

sets the lower 10 bits of the internal I/O address for channel 0

DM0IAPR:
x'00FE88'

DMA0 Internal Address Pointer

8/16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA0 EN	DMA0 IT	DMA0 UT	DMA0 MD	DMA0 SD	DMA0 MT	DMA0 AN1	DMA0 AN0	DMA0 ACK	DMA0 ST1	DMA0 ST0	DMA0 BG4	DMA0 BG3	DMA0 BG2	DMA0 BG1	DMA0 BG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W						
0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1	0 0/1						

DM0CTR:
x'00FE8A'

**DMA0 Control
Register**

D

16-bit access register

15	Execute enable	disable/enable
14	Enable interrupt generation	generate/do not generate
13	Transfer unit	word/byte
12	Transfer mode	burst transfer/single-word transfer
11	Transfer direction	source/destination
10	Transfer method	normal/continue
9, 8	Transfer addressing	00: increment 01: decrement 10: fixed 11: reserved
7	ACK output	pulse/level
6, 5	Transfer configuration	00: memory-internal I/O (M-I/O) 01: memory-memory (M-M) 10: memory-external device, 1 bus cycle (M-External device 1) 11: memory-external device, 2 bus cycles (M-External device 2)
4~0	Starting factor	00000: software 00001: A/D conversion complete interrupt 00010: serial 0 transmit interrupt 00011: serial 0 receive interrupt 00100: serial 1 transmit interrupt 00101: serial 1 receive interrupt 00110: timer 0 interrupt 00111: timer 1 interrupt 01000: timer 2 interrupt 01001: timer 3 interrupt 01010: timer 4 interrupt 01011: timer 5 interrupt 01100: timer 6 interrupt 01101: timer 7 interrupt 01110: timer 8 interrupt

01111: timer 9 interrupt
 10000: timer 10 underflow interrupt
 10001: timer 10 A interrupt
 10010: timer 10 B interrupt
 10011: timer 11 underflow interrupt
 10100: timer 11 A interrupt
 10101: timer 11 B interrupt
 10110: timer 12 A interrupt
 10111: timer 12 B interrupt
 11000: IRQ0 interrupt
 11001: IRQ1 interrupt
 11010: IRQ2 interrupt
 11011: IRQ3 interrupt
 11100: external request 0 edge interrupt
 11101: external request 1 edge interrupt
 11110: external request 0 level interrupt
 11111: external request 1 level interrupt

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	DMA0 BR2	DMA0 BR1	DMA0 BR0
R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1

DM0BIR:
x'00FE8C'

**DMA0 Burst
Interrupt Register**
8/16-bit access register

2~0 Interrupt level during burst transfer 000 (level 0)~111 (level 7)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA1 AR15	DMA1 AR14	DMA1 AR13	DMA1 AR12	DMA1 AR11	DMA1 AR10	DMA1 AR9	DMA1 AR8	DMA1 AR7	DMA1 AR6	DMA1 AR5	DMA1 AR4	DMA1 AR3	DMA1 AR2	DMA1 AR1	DMA1 AR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
-	-	-	-	-	-	-	-	-	DMA1 AR23	DMA1 AR22	DMA1 AR21	DMA1 AR20	DMA1 AR19	DMA1 AR18	DMA1 AR17	DMA1 AR16
R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	

DMA1 transfer address

sets the transfer address for channel 1

DM1TAPL:
x'00FE90'

DM1TAPH:
x'00FE92'

DMA1 Transfer Address Pointer

8/16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA1 CT15	DMA1 CT14	DMA1 CT13	DMA1 CT12	DMA1 CT11	DMA1 CT10	DMA1 CT9	DMA1 CT8	DMA1 CT7	DMA1 CT6	DMA1 CT5	DMA1 CT4	DMA1 CT3	DMA1 CT2	DMA1 CT1	DMA1 CT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
-	-	-	-	-	-	-	-	-	DMA1 CT23	DMA1 CT22	DMA1 CT21	DMA1 CT20	DMA1 CT19	DMA1 CT18	DMA1 CT17	DMA1 CT16
R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	

DMA1 transfer count

sets the number of transfers for channel 1

DM1CNTL:
x'00FE94'

DM1CNTH:
x'00FE96'

DMA1 Transfer Count Register

8/16-bit access register

*After the transfer is completed,
the transfer count is 0.*

Chapter 10 Appendix

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	DMA1 IO9	DMA1 IO8	DMA1 IO7	DMA1 IO6	DMA1 IO5	DMA1 IO4	DMA1 IO3	DMA1 IO2	DMA1 IO1	DMA1 IO0
R	R	R	R	R	R	R/W									
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

9~0 DMA1 internal address

sets the lower 10 bits of the internal I/O address for channel 1

DM1IAPR:
x'00FE98'

DMA1 Internal Address Pointer

8/16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA1 EN	DMA1 IT	DMA1 UT	DMA1 MD	DMA1 SD	DMA1 MT	DMA1 AN1	DMA1 AN0	DMA1 ACK	DMA1 ST1	DMA1 ST0	DMA1 BG4	DMA1 BG3	DMA1 BG2	DMA1 BG1	DMA1 BG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DM1CTR:
x'00FE9A'

**DMA1 Control
Register**

D

16-bit access register

15	Execute enable	disable/enable
14	Enable interrupt generation	generate/do not generate
13	Transfer unit	word/byte
12	Transfer mode	burst transfer/single-word transfer
11	Transfer direction	source/destination
10	Transfer method	normal/continue
9, 8	Transfer addressing	00: increment 01: decrement 10: fixed 11: reserved
7	ACK output	pulse/level
6, 5	Transfer configuration	00: memory-internal I/O (M-I/O) 01: memory-memory (M-M) 10: memory-external device, 1 bus cycle (M-External device 1) 11: memory-external device, 2 bus cycles (M-External device 2)
4~0	Starting factor	00000: software 00001: A/D conversion complete interrupt 00010: serial 0 transmit interrupt 00011: serial 0 receive interrupt 00100: serial 1 transmit interrupt 00101: serial 1 receive interrupt 00110: timer 0 interrupt 00111: timer 1 interrupt 01000: timer 2 interrupt 01001: timer 3 interrupt 01010: timer 4 interrupt 01011: timer 5 interrupt 01100: timer 6 interrupt 01101: timer 7 interrupt 01110: timer 8 interrupt

01111: timer 9 interrupt
 10000: timer 10 underflow interrupt
 10001: timer 10 A interrupt
 10010: timer 10 B interrupt
 10011: timer 11 underflow interrupt
 10100: timer 11 A interrupt
 10101: timer 11 B interrupt
 10110: timer 12 A interrupt
 10111: timer 12 B interrupt
 11000: IRQ0 interrupt
 11001: IRQ1 interrupt
 11010: IRQ2 interrupt
 11011: IRQ3 interrupt
 11100: external request 0 edge interrupt
 11101: external request 1 edge interrupt
 11110: external request 0 level interrupt
 11111: external request 1 level interrupt

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	DMA1 BR2	DMA1 BR1	DMA1 BR0
R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1

DM1BIR:
x'00FE9C'

**DMA1 Burst
Interrupt Register**

8/16-bit access register

2~0 Interrupt level during burst transfer 000 (level 0)~111 (level 7)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA2															
AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
R/W															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DMA2							
R	R	R	R	R	R	R	R	R/W							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DMA2 transfer address

sets the transfer address for channel 2

DM2TAPL:
x'00FEA0'

DM2TAPH:
x'00FEA2'

**DMA2 Transfer
Address Pointer**

8/16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA2															
CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
R/W															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DMA2							
R	R	R	R	R	R	R	R	R/W							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DMA2 transfer count

sets the number of transfers for channel 2

DM2CNTL:
x'00FEA4'

DM2CNTH:
x'00FEA6'

**DMA2 Transfer
Count Register**

8/16-bit access register

*After the transfer is completed,
the transfer count is 0.*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	DMA2 IO9	DMA2 IO8	DMA2 IO7	DMA2 IO6	DMA2 IO5	DMA2 IO4	DMA2 IO3	DMA2 IO2	DMA2 IO1	DMA2 IO0
R	R	R	R	R	R	R/W									
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

9~0 DMA2 internal address

sets the lower 10 bits of the internal I/O address for channel 2

DM2IAPR:
x'00FEA8'

DMA2 Internal Address Pointer

8/16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA2 EN	DMA2 IT	DMA2 UT	DMA2 MD	DMA2 SD	DMA2 MT	DMA2 AN1	DMA2 AN0	DMA2 ACK	DMA2 ST1	DMA2 ST0	DMA2 BG4	DMA2 BG3	DMA2 BG2	DMA2 BG1	DMA2 BG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DM2CTR:
x'00FEBA'

**DMA2 Control
Register**

D

16-bit access register

15	Execute enable	disable/enable
14	Enable interrupt generation	generate/do not generate
13	Transfer unit	word/byte
12	Transfer mode	burst transfer/single-word transfer
11	Transfer direction	source/destination
10	Transfer method	normal/continue
9, 8	Transfer addressing	00: increment 01: decrement 10: fixed 11: reserved
7	ACK output	pulse/level
6, 5	Transfer configuration	00: memory-internal I/O (M-I/O) 01: memory-memory (M-M) 10: memory-external device, 1 bus cycle (M-External device 1) 11: memory-external device, 2 bus cycles (M-External device 2)
4~0	Starting factor	00000: software 00001: A/D conversion complete interrupt 00010: serial 0 transmit interrupt 00011: serial 0 receive interrupt 00100: serial 1 transmit interrupt 00101: serial 1 receive interrupt 00110: timer 0 interrupt 00111: timer 1 interrupt 01000: timer 2 interrupt 01001: timer 3 interrupt 01010: timer 4 interrupt 01011: timer 5 interrupt 01100: timer 6 interrupt 01101: timer 7 interrupt 01110: timer 8 interrupt

01111: timer 9 interrupt
 10000: timer 10 underflow interrupt
 10001: timer 10 A interrupt
 10010: timer 10 B interrupt
 10011: timer 11 underflow interrupt
 10100: timer 11 A interrupt
 10101: timer 11 B interrupt
 10110: timer 12 A interrupt
 10111: timer 12 B interrupt
 11000: IRQ0 interrupt
 11001: IRQ1 interrupt
 11010: IRQ2 interrupt
 11011: IRQ3 interrupt
 11100: external request 0 edge interrupt
 11101: external request 1 edge interrupt
 11110: external request 0 level interrupt
 11111: external request 1 level interrupt

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	DMA2 BR2	DMA2 BR1	DMA2 BR0
R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1

DM2BIR:
x'00FEAC'

**DMA2 Burst
Interrupt Register**

8/16-bit access register

2~0 Interrupt level during burst transfer 000 (level 0)~111 (level 7)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA3															
AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
R/W															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DMA3							
R	R	R	R	R	R	R	R	R/W							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DMA3 transfer address

sets the transfer address for channel 3

DM3TAPL:
x'00FEB0'

DM3TAPH:
x'00FEB2'

DMA3 Transfer Address Pointer

8/16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA3															
CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
R/W															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DMA3							
R	R	R	R	R	R	R	R	R/W							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DMA3 transfer count

sets the number of transfers for channel 3

DM3CNTL:
x'00FEB4'

DM3CNTH:
x'00FEB6'

DMA3 Transfer Count Register

8/16-bit access register

*After the transfer is completed,
the transfer count is 0.*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	DMA3 IO9	DMA3 IO8	DMA3 IO7	DMA3 IO6	DMA3 IO5	DMA3 IO4	DMA3 IO3	DMA3 IO2	DMA3 IO1	DMA3 IO0
R	R	R	R	R	R	R/W									
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DM3IAPR:
x'00FEB8'

**DMA3 Internal
Address Pointer**

8/16-bit access register

9~0 DMA3 internal address sets the lower 10 bits of the internal I/O address for channel 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA3 EN	DMA3 IT	DMA3 UT	DMA3 MD	DMA3 SD	DMA3 MT	DMA3 AN1	DMA3 AN0	DMA3 ACK	DMA3 ST1	DMA3 ST0	DMA3 BG4	DMA3 BG3	DMA3 BG2	DMA3 BG1	DMA3 BG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DM3CTR:
x'00FEBA'

**DMA3 Control
Register**

D

16-bit access register

15	Execute enable	disable/enable
14	Enable interrupt generation	generate/do not generate
13	Transfer unit	word/byte
12	Transfer mode	burst transfer/single-word transfer
11	Transfer direction	source/destination
10	Transfer method	normal/continue
9, 8	Transfer addressing	00: increment 01: decrement 10: fixed 11: reserved
7	ACK output	pulse/level
6, 5	Transfer configuration	00: memory-internal I/O (M-I/O) 01: memory-memory (M-M) 10: memory-external device, 1 bus cycle (M-External device 1) 11: memory-external device, 2 bus cycles (M-External device 2)
4~0	Starting factor	00000: software 00001: A/D conversion complete interrupt 00010: serial 0 transmit interrupt 00011: serial 0 receive interrupt 00100: serial 1 transmit interrupt 00101: serial 1 receive interrupt 00110: timer 0 interrupt 00111: timer 1 interrupt 01000: timer 2 interrupt 01001: timer 3 interrupt 01010: timer 4 interrupt 01011: timer 5 interrupt 01100: timer 6 interrupt 01101: timer 7 interrupt 01110: timer 8 interrupt

01111: timer 9 interrupt
 10000: timer 10 underflow interrupt
 10001: timer 10 A interrupt
 10010: timer 10 B interrupt
 10011: timer 11 underflow interrupt
 10100: timer 11 A interrupt
 10101: timer 11 B interrupt
 10110: timer 12 A interrupt
 10111: timer 12 B interrupt
 11000: IRQ0 interrupt
 11001: IRQ1 interrupt
 11010: IRQ2 interrupt
 11011: IRQ3 interrupt
 11100: external request 0 edge interrupt
 11101: external request 1 edge interrupt
 11110: external request 0 level interrupt
 11111: external request 1 level interrupt

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	DMA3	DMA3	DMA3	
R	R	R	R	R	R	R	R	R	R	R	R	BR2	BR1	BR0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	

DM3BIR:
x'00FEBC'

**DMA3 Burst
Interrupt Register**

8/16-bit access register

2~0 Interrupt level during burst transfer 000 (level 0)~111 (level 7)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA4 AR15	DMA4 AR14	DMA4 AR13	DMA4 AR12	DMA4 AR11	DMA4 AR10	DMA4 AR9	DMA4 AR8	DMA4 AR7	DMA4 AR6	DMA4 AR5	DMA4 AR4	DMA4 AR3	DMA4 AR2	DMA4 AR1	DMA4 AR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DMA4 AR23	DMA4 AR22	DMA4 AR21	DMA4 AR20	DMA4 AR19	DMA4 AR18	DMA4 AR17	DMA4 AR16
R	R	R	R	R	R	R	R	R/W							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DMA4 transfer address

sets the transfer address for channel 4

DM4TAPL:
x'00FEC0'

DM4TAPH:
x'00FEC2'

**DMA4 Transfer
Address Pointer**

8/16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA4 CT15	DMA4 CT14	DMA4 CT13	DMA4 CT12	DMA4 CT11	DMA4 CT10	DMA4 CT9	DMA4 CT8	DMA4 CT7	DMA4 CT6	DMA4 CT5	DMA4 CT4	DMA4 CT3	DMA4 CT2	DMA4 CT1	DMA4 CT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DMA4 CT23	DMA4 CT22	DMA4 CT21	DMA4 CT20	DMA4 CT19	DMA4 CT18	DMA4 CT17	DMA4 CT16
R	R	R	R	R	R	R	R	R/W							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DMA4 transfer count

sets the number of transfers for channel 4

DM4CNTL:
x'00FEC4'

DM4CNTH:
x'00FEC6'

**DMA4 Transfer
Count Register**

8/16-bit access register

*After the transfer is completed,
the transfer count is 0.*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	DMA4 IO9	DMA4 IO8	DMA4 IO7	DMA4 IO6	DMA4 IO5	DMA4 IO4	DMA4 IO3	DMA4 IO2	DMA4 IO1	DMA4 IO0
R	R	R	R	R	R	R/W									
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

9~0 DMA4 internal address

sets the lower 10 bits of the internal I/O address for channel 4

DM4IAPR:
x'00FEC8'

DMA4 Internal Address Pointer

8/16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA4 EN	DMA4 IT	DMA4 UT	DMA4 MD	DMA4 SD	DMA4 MT	DMA4 AN1	DMA4 AN0	DMA4 ACK	DMA4 ST1	DMA4 ST0	DMA4 BG4	DMA4 BG3	DMA4 BG2	DMA4 BG1	DMA4 BG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DM4CTR:
x'00FECA'

**DMA4 Control
Register**

D

16-bit access register

15	Execute enable	disable/enable
14	Enable interrupt generation	generate/do not generate
13	Transfer unit	word/byte
12	Transfer mode	burst transfer/single-word transfer
11	Transfer direction	source/destination
10	Transfer method	normal/continue
9, 8	Transfer addressing	00: increment 01: decrement 10: fixed 11: reserved
7	ACK output	pulse/level
6, 5	Transfer configuration	00: memory-internal I/O (M-I/O) 01: memory-memory (M-M) 10: memory-external device, 1 bus cycle (M-External device 1) 11: memory-external device, 2 bus cycles (M-External device 2)
4~0	Starting factor	00000: software 00001: A/D conversion complete interrupt 00010: serial 0 transmit interrupt 00011: serial 0 receive interrupt 00100: serial 1 transmit interrupt 00101: serial 1 receive interrupt 00110: timer 0 interrupt 00111: timer 1 interrupt 01000: timer 2 interrupt 01001: timer 3 interrupt 01010: timer 4 interrupt 01011: timer 5 interrupt 01100: timer 6 interrupt 01101: timer 7 interrupt 01110: timer 8 interrupt

01111: timer 9 interrupt
 10000: timer 10 underflow interrupt
 10001: timer 10 A interrupt
 10010: timer 10 B interrupt
 10011: timer 11 underflow interrupt
 10100: timer 11 A interrupt
 10101: timer 11 B interrupt
 10110: timer 12 A interrupt
 10111: timer 12 B interrupt
 11000: IRQ0 interrupt
 11001: IRQ1 interrupt
 11010: IRQ2 interrupt
 11011: IRQ3 interrupt
 11100: external request 0 edge interrupt
 11101: external request 1 edge interrupt
 11110: external request 0 level interrupt
 11111: external request 1 level interrupt

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	DMA4 BR2	DMA4 BR1	DMA4 BR0
R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1

DM4BIR:
x'00FECC'

**DMA4 Burst
Interrupt Register**

8/16-bit access register

2~0 Interrupt level during burst transfer 000 (level 0)~111 (level 7)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA5 AR15	DMA5 AR14	DMA5 AR13	DMA5 AR12	DMA5 AR11	DMA5 AR10	DMA5 AR9	DMA5 AR8	DMA5 AR7	DMA5 AR6	DMA5 AR5	DMA5 AR4	DMA5 AR3	DMA5 AR2	DMA5 AR1	DMA5 AR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DMA5 AR23	DMA5 AR22	DMA5 AR21	DMA5 AR20	DMA5 AR19	DMA5 AR18	DMA5 AR17	DMA5 AR16
R	R	R	R	R	R	R	R	R/W							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DMA5 transfer address

sets the transfer address for channel 5

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA5 CT15	DMA5 CT14	DMA5 CT13	DMA5 CT12	DMA5 CT11	DMA5 CT10	DMA5 CT9	DMA5 CT8	DMA5 CT7	DMA5 CT6	DMA5 CT5	DMA5 CT4	DMA5 CT3	DMA5 CT2	DMA5 CT1	DMA5 CT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DMA5 CT23	DMA5 CT22	DMA5 CT21	DMA5 CT20	DMA5 CT19	DMA5 CT18	DMA5 CT17	DMA5 CT16
R	R	R	R	R	R	R	R	R/W							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DMA5 transfer count

sets the number of transfers for channel 5

DM5TAPL:
x'00FED0'

DM5TAPH:
x'00FED2'

DMA5 Transfer Address Pointer

8/16-bit access register

DM5CNTL:
x'00FED4'

DM5CNTH:
x'00FED6'

DMA5 Transfer Count Register

8/16-bit access register

*After the transfer is completed,
the transfer count is 0.*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	DMA5 IO9	DMA5 IO8	DMA5 IO7	DMA5 IO6	DMA5 IO5	DMA5 IO4	DMA5 IO3	DMA5 IO2	DMA5 IO1	DMA5 IO0
R	R	R	R	R	R	R/W									
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

9~0 DMA5 internal address

sets the lower 10 bits of the internal I/O address for channel 5

DM5IAPR:
x'00FED8'

DMA5 Internal Address Pointer

8/16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA5 EN	DMA5 IT	DMA5 UT	DMA5 MD	DMA5 SD	DMA5 MT	DMA5 AN1	DMA5 AN0	DMA5 ACK	DMA5 ST1	DMA5 ST0	DMA5 BG4	DMA5 BG3	DMA5 BG2	DMA5 BG1	DMA5 BG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DM5CTR:
x'00FEDA'

**DMA5 Control
Register**

D

16-bit access register

15	Execute enable	disable/enable
14	Enable interrupt generation	generate/do not generate
13	Transfer unit	word/byte
12	Transfer mode	burst transfer/single-word transfer
11	Transfer direction	source/destination
10	Transfer method	normal/continue
9, 8	Transfer addressing	00: increment 01: decrement 10: fixed 11: reserved
7	ACK output	pulse/level
6, 5	Transfer configuration	00: memory-internal I/O (M-I/O) 01: memory-memory (M-M) 10: memory-external device, 1 bus cycle (M-External device 1) 11: memory-external device, 2 bus cycles (M-External device 2)
4~0	Starting factor	00000: software 00001: A/D conversion complete interrupt 00010: serial 0 transmit interrupt 00011: serial 0 receive interrupt 00100: serial 1 transmit interrupt 00101: serial 1 receive interrupt 00110: timer 0 interrupt 00111: timer 1 interrupt 01000: timer 2 interrupt 01001: timer 3 interrupt 01010: timer 4 interrupt 01011: timer 5 interrupt 01100: timer 6 interrupt 01101: timer 7 interrupt 01110: timer 8 interrupt

01111: timer 9 interrupt
 10000: timer 10 underflow interrupt
 10001: timer 10 A interrupt
 10010: timer 10 B interrupt
 10011: timer 11 underflow interrupt
 10100: timer 11 A interrupt
 10101: timer 11 B interrupt
 10110: timer 12 A interrupt
 10111: timer 12 B interrupt
 11000: IRQ0 interrupt
 11001: IRQ1 interrupt
 11010: IRQ2 interrupt
 11011: IRQ3 interrupt
 11100: external request 0 edge interrupt
 11101: external request 1 edge interrupt
 11110: external request 0 level interrupt
 11111: external request 1 level interrupt

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	DMA5 BR2	DMA5 BR1	DMA5 BR0
R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1

DM5BIR:
x'00FEDC'

**DMA5 Burst
Interrupt Register**
8/16-bit access register

2~0 Interrupt level during burst transfer 000 (level 0)~111 (level 7)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA6 AR15	DMA6 AR14	DMA6 AR13	DMA6 AR12	DMA6 AR11	DMA6 AR10	DMA6 AR9	DMA6 AR8	DMA6 AR7	DMA6 AR6	DMA6 AR5	DMA6 AR4	DMA6 AR3	DMA6 AR2	DMA6 AR1	DMA6 AR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DMA6 AR23	DMA6 AR22	DMA6 AR21	DMA6 AR20	DMA6 AR19	DMA6 AR18	DMA6 AR17	DMA6 AR16
R	R	R	R	R	R	R	R	R/W							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DMA6 transfer address

sets the transfer address for channel 6

DM6TAPL:
x'00FEE0'

DM6TAPH:
x'00FEE2'

DMA6 Transfer Address Pointer

8/16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA6 CT15	DMA6 CT14	DMA6 CT13	DMA6 CT12	DMA6 CT11	DMA6 CT10	DMA6 CT9	DMA6 CT8	DMA6 CT7	DMA6 CT6	DMA6 CT5	DMA6 CT4	DMA6 CT3	DMA6 CT2	DMA6 CT1	DMA6 CT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DMA6 CT23	DMA6 CT22	DMA6 CT21	DMA6 CT20	DMA6 CT19	DMA6 CT18	DMA6 CT17	DMA6 CT16
R	R	R	R	R	R	R	R	R/W							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DMA6 transfer count

sets the number of transfers for channel 6

DM6CNTL:
x'00FEE4'

DM6CNTH:
x'00FEE6'

DMA6 Transfer Count Register

8/16-bit access register

*After the transfer is completed,
the transfer count is 0.*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	DMA6 IO9	DMA6 IO8	DMA6 IO7	DMA6 IO6	DMA6 IO5	DMA6 IO4	DMA6 IO3	DMA6 IO2	DMA6 IO1	DMA6 IO0
R	R	R	R	R	R	R/W									
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

9~0 DMA6 internal address

sets the lower 10 bits of the internal I/O address for channel 6

DM6IAPR:
x'00FEE8'

DMA6 Internal Address Pointer

8/16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA6 EN	DMA6 IT	DMA6 UT	DMA6 MD	DMA6 SD	DMA6 MT	DMA6 AN1	DMA6 AN0	DMA6 ACK	DMA6 ST1	DMA6 ST0	DMA6 BG4	DMA6 BG3	DMA6 BG2	DMA6 BG1	DMA6 BG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DM6CTR:
x'00FEAA'

**DMA6 Control
Register**

D

16-bit access register

15	Execute enable	disable/enable
14	Enable interrupt generation	generate/do not generate
13	Transfer unit	word/byte
12	Transfer mode	burst transfer/single-word transfer
11	Transfer direction	source/destination
10	Transfer method	normal/continue
9, 8	Transfer addressing	00: increment 01: decrement 10: fixed 11: reserved
7	ACK output	pulse/level
6, 5	Transfer configuration	00: memory-internal I/O (M-I/O) 01: memory-memory (M-M) 10: memory-external device, 1 bus cycle (M-External device 1) 11: memory-external device, 2 bus cycles (M-External device 2)
4~0	Starting factor	00000: software 00001: A/D conversion complete interrupt 00010: serial 0 transmit interrupt 00011: serial 0 receive interrupt 00100: serial 1 transmit interrupt 00101: serial 1 receive interrupt 00110: timer 0 interrupt 00111: timer 1 interrupt 01000: timer 2 interrupt 01001: timer 3 interrupt 01010: timer 4 interrupt 01011: timer 5 interrupt 01100: timer 6 interrupt 01101: timer 7 interrupt 01110: timer 8 interrupt

01111: timer 9 interrupt
 10000: timer 10 underflow interrupt
 10001: timer 10 A interrupt
 10010: timer 10 B interrupt
 10011: timer 11 underflow interrupt
 10100: timer 11 A interrupt
 10101: timer 11 B interrupt
 10110: timer 12 A interrupt
 10111: timer 12 B interrupt
 11000: IRQ0 interrupt
 11001: IRQ1 interrupt
 11010: IRQ2 interrupt
 11011: IRQ3 interrupt
 11100: external request 0 edge interrupt
 11101: external request 1 edge interrupt
 11110: external request 0 level interrupt
 11111: external request 1 level interrupt

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	DMA6 BR2	DMA6 BR1	DMA6 BR0
R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1

DM6BIR:
x'00FEEC'

**DMA6 Burst
Interrupt Register**

8/16-bit access register

2~0 Interrupt level during burst transfer 000 (level 0)~111 (level 7)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA7															
AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
R/W															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DMA7							
R	R	R	R	R	R	R	R	R/W							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DMA7 transfer address

sets the transfer address for channel 7

DM7TAPL:
x'00FEF0'

DM7TAPH:
x'00FEF2'

DMA7 Transfer Address Pointer

8/16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA7															
CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
R/W															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DMA7							
R	R	R	R	R	R	R	R	R/W							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DMA7 transfer count

sets the number of transfers for channel 7

DM7CNTL:
x'00FEF4'

DM7CNTH:
x'00FEF6'

DMA7 Transfer Count Register

8/16-bit access register

*After the transfer is completed,
the transfer count is 0.*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	DMA7 IO9	DMA7 IO8	DMA7 IO7	DMA7 IO6	DMA7 IO5	DMA7 IO4	DMA7 IO3	DMA7 IO2	DMA7 IO1	DMA7 IO0
R	R	R	R	R	R	R/W									
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

9~0 DMA7 internal address

sets the lower 10 bits of the internal I/O address for channel 7

DM7IAPR:
x'00FEF8'

DMA7 Internal Address Pointer

8/16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA7 EN	DMA7 IT	DMA7 UT	DMA7 MD	DMA7 SD	DMA7 MT	DMA7 AN1	DMA7 AN0	DMA7 ACK	DMA7 ST1	DMA7 ST0	DMA7 BG4	DMA7 BG3	DMA7 BG2	DMA7 BG1	DMA7 BG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

DM7CTR:
x'00FEFA'

**DMA7 Control
Register**

D

16-bit access register

15	Execute enable	disable/enable
14	Enable interrupt generation	generate/do not generate
13	Transfer unit	word/byte
12	Transfer mode	burst transfer/single-word transfer
11	Transfer direction	source/destination
10	Transfer method	normal/continue
9, 8	Transfer addressing	00: increment 01: decrement 10: fixed 11: reserved
7	ACK output	pulse/level
6, 5	Transfer configuration	00: memory-internal I/O (M-I/O) 01: memory-memory (M-M) 10: memory-external device, 1 bus cycle (M-External device 1) 11: memory-external device, 2 bus cycles (M-External device 2)
4~0	Starting factor	00000: software 00001: A/D conversion complete interrupt 00010: serial 0 transmit interrupt 00011: serial 0 receive interrupt 00100: serial 1 transmit interrupt 00101: serial 1 receive interrupt 00110: timer 0 interrupt 00111: timer 1 interrupt 01000: timer 2 interrupt 01001: timer 3 interrupt 01010: timer 4 interrupt 01011: timer 5 interrupt 01100: timer 6 interrupt 01101: timer 7 interrupt 01110: timer 8 interrupt

01111: timer 9 interrupt
 10000: timer 10 underflow interrupt
 10001: timer 10 A interrupt
 10010: timer 10 B interrupt
 10011: timer 11 underflow interrupt
 10100: timer 11 A interrupt
 10101: timer 11 B interrupt
 10110: timer 12 A interrupt
 10111: timer 12 B interrupt
 11000: IRQ0 interrupt
 11001: IRQ1 interrupt
 11010: IRQ2 interrupt
 11011: IRQ3 interrupt
 11100: external request 0 edge interrupt
 11101: external request 1 edge interrupt
 11110: external request 0 level interrupt
 11111: external request 1 level interrupt

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	DMA7 BR2	DMA7 BR1	DMA7 BR0
R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1

DM7BIR:
x'00FEFC'

**DMA7 Burst
Interrupt Register**

8/16-bit access register

2~0 Interrupt level during burst transfer 000 (level 0)~111 (level 7)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	SBT 1P	SBI 1P	SBT 0P	SBO 0P	SBI 0P	-	PKIP	P43P	P42P	P41P	P40P	DHP	DLP	
R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0/1	0/1	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1

- | | | |
|----|--|--------------------|
| 13 | SBT1 pin pull-up | no pull-up/pull-up |
| 12 | SBO1 pin pull-up | no pull-up/pull-up |
| 11 | SBI1 pin pull-up | no pull-up/pull-up |
| 10 | SBT0 pin pull-up | no pull-up/pull-up |
| 9 | SBO0 pin pull-up | no pull-up/pull-up |
| 8 | SBI0 pin pull-up | no pull-up/pull-up |
| 6 | $\overline{K17} \sim \overline{K10}$ pin pull-up | no pull-up/pull-up |
| 5 | P43 pin pull-up | no pull-up/pull-up |
| 4 | P42 pin pull-up | no pull-up/pull-up |
| 3 | P41 pin pull-up | no pull-up/pull-up |
| 2 | P40 pin pull-up | no pull-up/pull-up |
| 1 | D15~8 pin pull-up | no pull-up/pull-up |
| 0 | D7~0 pin pull-up | no pull-up/pull-up |

PPLU:
x'00FFB0'

Port Pull-up Control Register

D

8/16-bit access register

Bits 15, 14 and 7 must be set to '0'.

P

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	TM12 BO	TM12 AO	TM11 BO	TM11 AO	TM10 BO	TM10 AO	-	-	-	TM4O	TM3O	TM2O	TM1O	TM0O
R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0	0/1	0/1	0/1	0/1	0/1

TMDIR:
x'00FFB2'

Timer I/O Control Register

8/16-bit access register

- | | | |
|----|-------------------------|----------------------|
| 13 | TM12IOB pin I/O control | input pin/output pin |
| 12 | TM12IOA pin I/O control | input pin/output pin |
| 11 | TM11IOB pin I/O control | input pin/output pin |
| 10 | TM11IOA pin I/O control | input pin/output pin |
| 9 | TM10IOB pin I/O control | input pin/output pin |
| 8 | TM10IOA pin I/O control | input pin/output pin |
| 4 | TM4IO pin I/O control | input pin/output pin |
| 3 | TM3IO pin I/O control | input pin/output pin |
| 2 | TM2IO pin I/O control | input pin/output pin |
| 1 | TM1IO pin I/O control | input pin/output pin |
| 0 | TM0IO pin I/O control | input pin/output pin |

7	6	5	4	3	2	1	0
P0OUT7	P0OUT6	P0OUT5	P0OUT4	P0OUT3	P0OUT2	P0OUT1	P0OUT0
R/W							
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

P0OUT:
x'00FFC0'

**Port 0 Output
Register**

8/16-bit access register

7~0 Port 0 output data

For P1OUT (x'00FE64'), please refer to the synchronous output function of related registers.

7	6	5	4	3	2	1	0
-	-	-	-	P2OUT3	P2OUT2	P2OUT1	P2OUT0
R	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0	0	0/1	0/1	0/1	0/1

P2OUT:
x'00FFC2'

**Port 2 Output
Register**

8/16-bit access register

3~0 Port 2 output data

P

7	6	5	4	3	2	1	0
-	-	-	P3OUT4	P3OUT3	P3OUT2	P3OUT1	P3OUT0
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0	0/1	0/1	0/1	0/1	0/1

P3OUT:
x'00FFC3'

**Port 3 Output
Register**

8-bit access register

(16-bit access is possible from an even address)

T

4~0 Port 3 output data

7	6	5	4	3	2	1	0
P0IN7	P0IN6	P0IN5	P0IN4	P0IN3	P0IN2	P0IN1	P0IN0
R	R	R	R	R	R	R	R
port							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

P0IN:
x'00FFD0'
Port 0 Input Register
8/16-bit access register

7~0 Port 0 pin value

7	6	5	4	3	2	1	0
P1IN7	P1IN6	P1IN5	P1IN4	P1IN3	P1IN2	P1IN1	P1IN0
R	R	R	R	R	R	R	R
port							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

P1IN:
x'00FFD1'
Port 1 Input Register
8-bit access register
(16-bit access is possible from an even address)

7~0 Port 1 pin value

7	6	5	4	3	2	1	0
-	-	-	-	P2IN3	P2IN2	P2IN1	P2IN0
R	R	R	R	R	R	R	R
0	0	0	0	port	port	port	port
0	0	0	0	0/1	0/1	0/1	0/1

P2IN:
x'00FFD2'
Port 2 Input Register
8/16-bit access register

3~0 Port 2 pin value

7	6	5	4	3	2	1	0
-	-	-	P3IN4	P3IN3	P3IN2	P3IN1	P3IN0
R	R	R	R	R	R	R	R
0	0	0	port	port	port	port	port
0	0	0	0/1	0/1	0/1	0/1	0/1

4~0 Port 3 pin value

P3IN:
x'00FFD3'

Port 3 Input Register

8-bit access register

(16-bit access is possible from
an even address)

7	6	5	4	3	2	1	0
PODIR7	PODIR6	PODIR5	PODIR4	PODIR3	PODIR2	PODIR1	PODIR0
R/W							
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Port 0 I/O

input pin/output pin

P0DIR:
x'00FFE0'

Port 0 I/O Control Register

8/16-bit access register

7	6	5	4	3	2	1	0
P1DIR7	P1DIR6	P1DIR5	P1DIR4	P1DIR3	P1DIR2	P1DIR1	P1DIR0
R/W							
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7~0 Port 1 I/O

input pin/output pin

P1DIR:
x'00FFE1'

Port 1 I/O Control Register

8-bit access register

(16-bit access is possible from
an even address)

7	6	5	4	3	2	1	0
-	-	-	-	P2DIR3	P2DIR2	P2DIR1	P2DIR0
R	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0	0	0/1	0/1	0/1	0/1

3~0 Port 2 I/O

input pin/output pin

P2DIR:
x'00FFE2'

**Port 2 I/O Control
Register**
8/16-bit access register

7	6	5	4	3	2	1	0
-	-	-	P3DIR4	P3DIR3	P3DIR2	P3DIR1	P3DIR0
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0	0/1	0/1	0/1	0/1	0/1

4~0 Port 3 I/O

input pin/output pin

P3DIR:
x'00FFE3'

Port 3 I/O Control
Register

7	6	5	4	3	2	1	0
-	P3MD6	P3MD5	P3MD4	P3MD3	P3MD2	P3MD1	P3MD0
R	R/W						
0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1

P3MD:
x'00FFF3'

Port 3 Output Mode Register

8-bit access register

(16-bit access is possible from
an even address)

- | | | |
|------|---------------|---|
| 6, 4 | Port 3 output | 01: TM9 output
11: serial 1 clock output
*0: P34 output |
| 5, 3 | Port 3 output | 01: TM8 output
11: serial 0 clock output
*0: P33 output |
| 2 | Port 3 output | P32 output/TM7 output |
| 1 | Port 3 output | P31 output/TM6 output |
| 0 | Port 3 output | P30 output/TM5 output |

10-2-2 MN1020012 Internal Memory and Register Address Map

Chapter 10 Appendix

Lower Upper 20bits	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Notes	
x'00FC00'	IAGR [‡]												MEMCTR [‡]	CPUM [†]			Internal control registers	
x'00FC30'	G7ICR [‡] (VCT=14)	G6ICR [‡] (VCT=12)	G5ICR [‡] (VCT=10)	G4ICR [‡] (VCT=8)	G3ICR [‡] (VCT=6)	G2ICR [‡] (VCT=4)	G1ICR [‡] (VCT=2)	G0ICR [‡] (VCT=0)	G9ICR [‡] (VCT=18)	G8ICR [‡] (VCT=16)	G7ICR [‡] (VCT=14)	G6ICR [‡] (VCT=12)	MEMMD0 [†]	MEMMD1 [†]	MEMMD2 [†]	MEMMD3 [†]	Memory mode control registers	
x'00FC40'													EXTMD [‡]	G10ICR [‡] (VCT=18)	G9ICR [‡] (VCT=16)	G8ICR [‡] (VCT=14)	G7ICR [‡] (VCT=12)	Interrupt control registers
x'00FC50'														REFCNT [‡]	SC0STR [*]	SC0CTR [‡]	DRMCTR [‡]	DMA controller control registers
x'00FD00'														SC1STR [*]	SC1TRB [‡]	SC1CTR [‡]	SC0CTR [‡]	Serial interfaces 2 channels
x'00FD80'																		
x'00FDA0'	AN7BUF [*]	AN6BUF [‡]	ANSBUF [*]	AN4BUF [‡]	AN3BUF [*]	AN2BUF [‡]	ANIBUF [*]	AN0BUF [‡]									ANCTR [‡]	Analog-to-digital converter
x'00FE00'					PS1BC [*]	PS0BC [‡]	TM9BC [*]	TM8BC [‡]	TM7BC [*]	TM6BC [‡]	TM5BC [*]	TM4BC [‡]	TM3BC [*]	TM2BC [‡]	TM1BC [*]	TM0BC [‡]		
x'00FE10'					PS1BR [*]	PS0BR [‡]	TM9BR [*]	TM8BR [‡]	TM7BR [*]	TM6BR [‡]	TM5BR [*]	TM4BR [‡]	TM3BR [*]	TM2BR [‡]	TM1BR [*]	TM0BR [‡]		
x'00FE20'					PS1MD [*]	PS0MD [‡]	TM9MD [*]	TM8MD [‡]	TM7MD [*]	TM6MD [‡]	TM5MD [*]	TM4MD [‡]	TM3MD [*]	TM2MD [‡]	TM1MD [*]	TM0MD [‡]		13 timer channels
x'00FE30'						TM10CBX [†]		TM10CB [†]		TM10CAX [†]		TM10CA [†]		TM10BC [†]		TM10MD [†]		
x'00FE40'						TM11CBX [†]		TM11CB [†]		TM11CAX [†]		TM11CA [†]		TM11BC [†]		TM11MD [†]		
x'00FE50'						TM12CBX [†]		TM12CB [†]		TM12CAX [†]		TM12CA [†]		TM12BC [†]		TM12MD [†]		

‡= 8/16-bit access †= 16-bit access

*= 8-bit access (16-bit access is possible from an even address)

no symbol = 8-bit access

Upper 20bits	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Notes
x'00FE60'																	
x'00FE70'																	
x'00FE80'	DM0BIR	‡	DM0CTR	‡	DM0IAPR	‡	DM0CNTH	‡	DM0CNTL	‡	DM0TAPH	‡	DM0TAPL	‡			
x'00FE90'	DM1BIR	‡	DM1CTR	‡	DM1IAPR	‡	DM1CNTH	‡	DM1CNTL	‡	DM1TAPH	‡	DM1TAPL	‡			
x'00FEA0'	DM2BIR	‡	DM2CTR	‡	DM2IAPR	‡	DM2CNTH	‡	DM2CNTL	‡	DM2TAPH	‡	DM2TAPL	‡			
x'00FEB0'	DM3BIR	‡	DM3CTR	‡	DM3IAPR	‡	DM3CNTH	‡	DM3CNTL	‡	DM3TAPH	‡	DM3TAPL	‡			
x'00FEC0'	DM4BIR	‡	DM4CTR	‡	DM4IAPR	‡	DM4CNTH	‡	DM4CNTL	‡	DM4TAPH	‡	DM4TAPL	‡			
x'00FED0'	DM5BIR	‡	DM5CTR	‡	DM5IAPR	‡	DM5CNTH	‡	DM5CNTL	‡	DM5TAPH	‡	DM5TAPL	‡			
x'00FEE0'	DM6BIR	‡	DM6CTR	‡	DM6IAPR	‡	DM6CNTH	‡	DM6CNTL	‡	DM6TAPH	‡	DM6TAPL	‡			
x'00FEF0'	DM7BIR	‡	DM7CTR	‡	DM7IAPR	‡	DM7CNTH	‡	DM7CNTL	‡	DM7TAPH	‡	DM7TAPL	‡			
x'00FFB0'													TMDIR	‡	PPLU	‡	
x'00FFC0'													P3OUT	‡	P0OUT	‡	
x'00FFD0'													P3IN	‡	P1IN	‡	I/O ports
x'00FFE0'													P3DIR	‡	P1DIR	‡	
x'00FFF0'													P3MD	*			

‡= 8/16-bit access

*= 8-bit access (16-bit access is possible from an even address)

no symbol = 8-bit access

10-2-3 Pin Functions

Block	Pin Number	Pin Name	I/O Direction	Function	Port Number	Input Level	Schmitt Trigger	Pull-up Resistor	RESET	NORMAL	HALT	STOP	Bus Request
Power supply	4	VDD	IN	Power supply (+5V)	—	—	—	—	—	—	—	—	—
	18	VDD	IN		—	—	—	—	—	—	—	—	—
	29	VDD	IN		—	—	—	—	—	—	—	—	—
	39	VDD	IN		—	—	—	—	—	—	—	—	—
	62	VDD	IN		—	—	—	—	—	—	—	—	—
	76	VDD	IN		—	—	—	—	—	—	—	—	—
	96	VDD	IN		—	—	—	—	—	—	—	—	—
	118	VDD	IN		—	—	—	—	—	—	—	—	—
	9	VSS	IN		—	—	—	—	—	—	—	—	—
	27	VSS	IN		—	—	—	—	—	—	—	—	—
	32	VSS	IN		—	—	—	—	—	—	—	—	—
	44	VSS	IN		—	—	—	—	—	—	—	—	—
	66	VSS	IN		—	—	—	—	—	—	—	—	—
	87	VSS	IN		—	—	—	—	—	—	—	—	—
	109	VSS	IN		—	—	—	—	—	—	—	—	—
	123	VSS	IN		—	—	—	—	—	—	—	—	—
Analog power supply	82	AVDD	IN	Analog power supply (+5V)	—	—	—	—	—	—	—	—	—
	81	AVSS	IN		—	—	—	—	—	—	—	—	—
Clock	30	OSCI	IN	20-MHz oscillation	—	CMOS	Yes	—	—	—	—	—	—
	31	OSCO	OUT		—	—	—	H	OUT	OUT	H	OUT	—
	28	SYSCLK	OUT		—	—	—	H	OUT	OUT	H	OUT	—
Reset	52	/RST	IN	Oscillation with frequency half input oscillation	—	CMOS	Yes	—	—	—	—	—	—
Address bus	49	A23	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	50	A22	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	19	A21	OUT	Address bus outputs	—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	20	A20	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	21	A19	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	22	A18	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	23	A17	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	24	A16	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	25	A15	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	26	A14	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	33	A13	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	34	A12	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	35	A11	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	36	A10	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	37	A9	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	38	A8	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	40	A7	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	41	A6	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	42	A5	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	43	A4	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	45	A3	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	46	A2	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	47	A1	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
	48	A0	OUT		—	—	—	—	OUT	OUT	OUT	OUT	Hi-Z
Data bus	8	D15	IO	Data bus inputs/outputs	—	TTL	Yes	Programmable	Hi-Z	IO	Hi-Z	Hi-Z	Hi-Z
	7	D14	IO		—	TTL	Yes	Programmable	Hi-Z	IO	Hi-Z	Hi-Z	Hi-Z
	6	D13	IO		—	TTL	Yes	Programmable	Hi-Z	IO	Hi-Z	Hi-Z	Hi-Z
	5	D12	IO		—	TTL	Yes	Programmable	Hi-Z	IO	Hi-Z	Hi-Z	Hi-Z
	3	D11	IO		—	TTL	Yes	Programmable	Hi-Z	IO	Hi-Z	Hi-Z	Hi-Z
	2	D10	IO		—	TTL	Yes	Programmable	Hi-Z	IO	Hi-Z	Hi-Z	Hi-Z
	1	D9	IO		—	TTL	Yes	Programmable	Hi-Z	IO	Hi-Z	Hi-Z	Hi-Z
	128	D8	IO		—	TTL	Yes	Programmable	Hi-Z	IO	Hi-Z	Hi-Z	Hi-Z
	127	D7	IO		—	TTL	Yes	Programmable	Hi-Z	IO	Hi-Z	Hi-Z	Hi-Z
	126	D6	IO		—	TTL	Yes	Programmable	Hi-Z	IO	Hi-Z	Hi-Z	Hi-Z
	125	D5	IO		—	TTL	Yes	Programmable	Hi-Z	IO	Hi-Z	Hi-Z	Hi-Z
	124	D4	IO		—	TTL	Yes	Programmable	Hi-Z	IO	Hi-Z	Hi-Z	Hi-Z
	122	D3	IO		—	TTL	Yes	Programmable	Hi-Z	IO	Hi-Z	Hi-Z	Hi-Z
	121	D2	IO		—	TTL	Yes	Programmable	Hi-Z	IO	Hi-Z	Hi-Z	Hi-Z
	120	D1	IO		—	TTL	Yes	Programmable	Hi-Z	IO	Hi-Z	Hi-Z	Hi-Z
	119	D0	IO		—	TTL	Yes	Programmable	Hi-Z	IO	Hi-Z	Hi-Z	Hi-Z

Bus control signals	17	/RAS	OUT	DRAM RAS signal	—	—	—	H	OUT	H	H	H
	13	/CAS3,/CS3	OUT	DRAM CAS or chip select signals	—	—	—	H	OUT	H	H	H
	14	/CAS2,/CS2	OUT		—	—	—	H	OUT	H	H	H
	15	/CAS1,/CS1	OUT		—	—	—	H	OUT	H	H	H
	16	/CS0	OUT		—	—	—	H	OUT	H	H	H
	12	/RE	OUT	Memory read signal	—	—	—	H	OUT	H	H	Hi-Z
	10	/WEL	OUT	Memory write signal (lower byte: D7~D0)	—	—	—	H	OUT	H	H	Hi-Z
	11	/WEH	OUT	Memory write signal (upper byte: D15~D8)	—	—	—	H	OUT	H	H	Hi-Z
	58	/BR	IN	Bus request signal	—	CMOS	Yes	—	—	—	—	—
	59	/BG	OUT	Bus grant signal	—	—	—	—	—	—	—	—
	51	/BSMOD	IN	Block 0 data bus width specification (L: 16 bits, H: 8 bits)	—	CMOS	Yes	—	—	—	—	—
Analog inputs	86	AN7	IO	Analog inputs	P23	CMOS	—	—	—	—	—	—
	85	AN6	IO		P22	CMOS	—	—	—	—	—	—
	84	AN5	IO		P21	CMOS	—	—	—	—	—	—
	83	AN4	IO		P20	CMOS	—	—	—	—	—	—
	80	AN3	IN		—	CMOS	—	—	—	—	—	—
	79	AN2	IN		—	CMOS	—	—	—	—	—	—
	78	AN1	IN		—	CMOS	—	—	—	—	—	—
	77	AN0	IN		—	CMOS	—	—	—	—	—	—
Synchronous outputs	75	SYA3	IO	Synchronous output port A	P13	CMOS	Yes	—	—	—	—	—
	74	SYA2	IO		P12	CMOS	Yes	—	—	—	—	—
	73	SYA1	IO		P11	CMOS	Yes	—	—	—	—	—
	72	SYA0	IO		P10	CMOS	Yes	—	—	—	—	—
	91	SYB3	IO	Synchronous output port B	P17	CMOS	Yes	—	—	—	—	—
	90	SYB2	IO		P16	CMOS	Yes	—	—	—	—	—
	89	SYB1	IO		P15	CMOS	Yes	—	—	—	—	—
	88	SYB0	IO		P14	CMOS	Yes	—	—	—	—	—
Serial interface (Synchronous/UART)	94	SBI1	IN	Serial data inputs	—	CMOS	Yes	Programmable	—	—	—	—
	92	SBI0	IN		—	CMOS	Yes	Programmable	—	—	—	—
	95	SBO1	OUT	Serial data outputs	—	—	Yes	Programmable	H	OUT	OUT	OUT
	93	SBO0	OUT		—	—	Yes	Programmable	H	OUT	OUT	OUT
Interrupts	108	/IRQ3	IN	Interrupt inputs (individual)	P43	CMOS	Yes	Programmable	—	—	—	—
	107	/IRQ2	IN		P42	CMOS	Yes	Programmable	—	—	—	—
	106	/IRQ1	IN		P41	CMOS	Yes	Programmable	—	—	—	—
	105	/IRQ0	IN		P40	CMOS	Yes	Programmable	—	—	—	—
	104	/K17	IO		P07	CMOS	Yes	Programmable	—	—	—	—
	103	/K16	IO		P06	CMOS	Yes	Programmable	—	—	—	—
	102	/K15	IO		P05	CMOS	Yes	Programmable	—	—	—	—
	101	/K14	IO		P04	CMOS	Yes	Programmable	—	—	—	—
	100	/K13	IO	Keyboard interrupt inputs (ORed)	P03	CMOS	Yes	Programmable	—	—	—	—
	99	/K12	IO		P02	CMOS	Yes	Programmable	—	—	—	—
	98	/K11	IO		P01	CMOS	Yes	Programmable	—	—	—	—
	97	/K10	IO		P00	CMOS	Yes	Programmable	—	—	—	—
Timers	71	TM9IO,SBT1	IO	Timer clock inputs, timer output signals (TMIO9 and TMIO8 double as interface serial clocks)	P34	CMOS	Yes	Programmable	—	—	—	—
	70	TM8IO,SBT0	IO		P33	CMOS	Yes	Programmable	—	—	—	—
	69	TM7IO	IO		P32	CMOS	Yes	—	—	—	—	—
	68	TM6IO	IO		P31	CMOS	Yes	—	—	—	—	—
	67	TM5IO	IO		P30	CMOS	Yes	—	—	—	—	—
	65	TM4IO	IO		—	CMOS	Yes	—	IN	IO	IO	IO
	64	TM3IO	IO		—	CMOS	Yes	—	IN	IO	IO	IO
	63	TM2IO	IO		—	CMOS	Yes	—	IN	IO	IO	IO
	61	TM1IO	IO	Input capture inputs, Output compare outputs	—	CMOS	Yes	—	IN	IO	IO	IO
	60	TM0IO	IO		—	CMOS	Yes	—	IN	IO	IO	IO
	116	TM12IOA	IO		—	CMOS	Yes	—	—	—	—	—
	113	TM11OA	IO		—	CMOS	Yes	—	—	—	—	—
	110	TM10IA	IO	Timer counter clear signals	—	CMOS	Yes	—	—	—	—	—
	117	TM12IOB	IO		—	CMOS	Yes	—	—	—	—	—
	114	TM11IOB	IO		—	CMOS	Yes	—	—	—	—	—
	111	TM10IOB	IO		—	CMOS	Yes	—	—	—	—	—
	115	TM11IC	IN		—	CMOS	Yes	—	—	—	—	—
	112	TM10IC	IN	DMA controller	—	CMOS	Yes	—	—	—	—	—
	56	/DMAREQ1	IN		—	CMOS	Yes	—	—	—	—	—
	55	/DMAREQ0	IN		—	CMOS	Yes	—	—	—	—	—
	54	/DMAACK1	OUT		—	—	—	H	OUT	H	H	H
	53	/DMAACK0	OUT		—	—	—	H	OUT	H	H	H
	57	DMAEND	IN	DMA abort signal	—	CMOS	Yes	—	—	—	—	—

10-3 Summary of MN10200 Series Linear Address Edition Instructions

MN102L00 SERIES INSTRUCTION SET

Instruction	Mnemonic	Operation	OP EX.	Flag							Code Size	Cycle	Machine Code	
				VX	CX	NX	ZX	VF	CF	NF	ZF			
MOV	MOV Dm,An	Dm→An	— — — — — — — —	—	—	—	—	—	—	—	—	2	2	F2:30+Dm<<2+An
	MOV An,Dm	An→Dm	— — — — — — — —	—	—	—	—	—	—	—	—	2	2	F2:F0+An<<2+Dm
	MOV Dn,Dm	Dn→Dm	— — — — — — — —	—	—	—	—	—	—	—	—	1	1	80+Dn<<2+Dm
	MOV An,Am	An→Am	— — — — — — — —	—	—	—	—	—	—	—	—	2	2	F2:70+An<<2+Am
	MOV PSW,Dn	PSW→Dn	0 — — — — — — —	0	—	—	—	—	—	—	—	2	2	F3:F0+Dn
	MOV Dn,PSW	Dn→PSW	— ● ● ● ● ● ● ●	—	●	●	●	●	●	●	●	2	3	F3:D0+Dn<<2
	MOV MDR,Dn	MDR→Dn	0 — — — — — — —	0	—	—	—	—	—	—	—	2	2	F3:E0+Dn
	MOV Dn,MDR	Dn→MDR	— — — — — — — —	—	—	—	—	—	—	—	—	2	2	F3:C0+Dn<<2
	MOV (An),Dm	mem16(An)→Dm	S — — — — — — —	S	—	—	—	—	—	—	—	1	1	20+An<<2+Dm
	MOV (d8,An),Dm	mem16(An+d8)→Dm	S — — — — — — —	S	—	—	—	—	—	—	—	2	1	60+An<<2+Dm:d8
	MOV (d16,An),Dm	mem16(An+d16)→Dm	S — — — — — — —	S	—	—	—	—	—	—	—	4	2	F7:C0+An<<2+Dm:d16-l:d16-h
	MOV (d24,An),Dm	mem16(An+d24)→Dm	S — — — — — — —	S	—	—	—	—	—	—	—	5	3	F4:80+An<<2+Dm:d24-l:d24-m:d24-h
	MOV (Di,An),Dm	mem16(An+Di)→Dm	S — — — — — — —	S	—	—	—	—	—	—	—	2	2	F1:40+Di<<4+An<<2+Dm
	MOV (abs16),Dn	mem16(abs16)→Dn	S — — — — — — —	S	—	—	—	—	—	—	—	3	1	C8+Dn:abs16-l:abs16-h
	MOV (abs24),Dn	mem16(abs24)→Dn	S — — — — — — —	S	—	—	—	—	—	—	—	5	3	F4:C0+Dn:abs24-l:abs24-m:abs24-h
	MOV (An),Am	mem24(An)→Am	— — — — — — —	—	—	—	—	—	—	—	—	2	2	*2
	MOV (d8,An),Am	mem24(An+d8)→Am	— — — — — — —	—	—	—	—	—	—	—	—	2	2	70+An<<2+Am:d8
	MOV (d16,An),Am	mem24(An+d16)→Am	— — — — — — —	—	—	—	—	—	—	—	—	4	3	F7:B0+An<<2+Am:d16-l:d16-h
	MOV (d24,An),Am	mem24(An+d24)→Am	— — — — — — —	—	—	—	—	—	—	—	—	5	4	F4:F0+An<<2+Am:d24-l:d24-m:d24-h
	MOV (Di,An),Am	mem24(An+Di)→Am	— — — — — — —	—	—	—	—	—	—	—	—	2	3	F1:00+Di<<4+An<<2+Am
	MOV (abs16),Am	mem24(abs16)→Am	— — — — — — —	—	—	—	—	—	—	—	—	4	3	F7:30+An:abs16-l:abs16-h
	MOV (abs24),Am	mem24(abs24)→Am	— — — — — — —	—	—	—	—	—	—	—	—	5	4	F4:D0+An:abs24-l:abs24-m:abs24-h
	MOV Dm,(An)	Dm→mem16(An)	— — — — — — —	—	—	—	—	—	—	—	—	1	1	00+An<<2+Dm
	MOV Dm,(d8,An)	Dm→mem16(An+d8)	— — — — — — —	—	—	—	—	—	—	—	—	2	1	40+An<<2+Dm:d8
	MOV Dm,(d16,An)	Dm→mem16(An+d16)	— — — — — — —	—	—	—	—	—	—	—	—	4	2	F7:80+An<<2+Dm:d16-l:d16-h
	MOV Dm,(d24,An)	Dm→mem16(An+d24)	— — — — — — —	—	—	—	—	—	—	—	—	5	3	F4:00+An<<2+Dm:d24-l:d24-m:d24-h
	MOV Dm,(Di,An)	Dm→mem16(An+Di)	— — — — — — —	—	—	—	—	—	—	—	—	2	2	F1:C0+Di<<4+An<<2+Dm
	MOV Dn,(abs16)	Dn→mem16(abs16)	— — — — — — —	—	—	—	—	—	—	—	—	3	1	C0+Dn:abs16-l:abs16-h
	MOV Dn,(abs24)	Dn→mem16(abs24)	— — — — — — —	—	—	—	—	—	—	—	—	5	3	F4:40+Dn:abs24-l:abs24-m:abs24-h
	MOV Am,(An)	Am→mem24(An)	— — — — — — —	—	—	—	—	—	—	—	—	2	2	*3
	MOV Am,(d8,An)	Am→mem24(An+d8)	— — — — — — —	—	—	—	—	—	—	—	—	2	2	50+An<<2+Am:d8
	MOV Am,(d16,An)	Am→mem24(An+d16)	— — — — — — —	—	—	—	—	—	—	—	—	4	3	F7:A0+An<<2+Am:d16-l:d16-h
	MOV Am,(d24,An)	Am→mem24(An+d24)	— — — — — — —	—	—	—	—	—	—	—	—	5	4	F4:10+An<<2+Am:d24-l:d24-m:d24-h
	MOV Am,(Di,An)	Am→mem24(An+Di)	— — — — — — —	—	—	—	—	—	—	—	—	2	3	F1:80+Di<<4+An<<2+Am
	MOV An,(abs16)	An→mem24(abs16)	— — — — — — —	—	—	—	—	—	—	—	—	4	3	F7:20+An:abs16-l:abs16-h
	MOV An,(abs24)	An→mem24(abs24)	— — — — — — —	—	—	—	—	—	—	—	—	5	4	F4:50+An:abs24-l:abs24-m:abs24-h
	MOV imm8,Dn	imm8→Dn	S — — — — — — —	S	—	—	—	—	—	—	—	2	1	80+Dn<<2+Dn:imm8
	MOV imm16,Dn	imm16→Dn	S — — — — — — —	S	—	—	—	—	—	—	—	3	1	F8+Dn:imm16-l:imm16-h
	MOV imm24,Dn	imm24→Dn	— — — — — — —	—	—	—	—	—	—	—	—	5	3	F4:70+Dn:imm24-l:imm24-m:imm24-h
	MOV imm16,An	imm16→An	0 — — — — — — —	0	—	—	—	—	—	—	—	3	1	DC+An:imm16-l:imm16-h
	MOV imm24,An	imm24→An	— — — — — — —	—	—	—	—	—	—	—	—	5	3	F4:74+An:imm24-l:imm24-m:imm24-h
MOVX	MOVX (d8,An),Dm	mem24(An+d8)→Dm	— — — — — — —	—	—	—	—	—	—	—	—	3	3	F5:70+An<<2+Dm:d8
	MOVX (d16,An),Dm	mem24(An+d16)→Dm	— — — — — — —	—	—	—	—	—	—	—	—	4	3	F7:70+An<<2+Dm:d16-l:d16-h
	MOVX (d24,An),Dm	mem24(An+d24)→Dm	— — — — — — —	—	—	—	—	—	—	—	—	5	4	F4:B0+An<<2+Dm:d24-l:d24-m:d24-h
	MOVX Dm,(d8,An)	Dm→mem24(An+d8)	— — — — — — —	—	—	—	—	—	—	—	—	3	3	F5:50+An<<2+Dm:d8
	MOVX Dm,(d16,An)	Dm→mem24(An+d16)	— — — — — — —	—	—	—	—	—	—	—	—	4	3	F7:60+An<<2+Dm:d16-l:d16-h
	MOVX Dm,(d24,An)	Dm→mem24(An+d24)	— — — — — — —	—	—	—	—	—	—	—	—	5	4	F4:30+An<<2+Dm:d24-l:d24-m:d24-h
MOVB	MOVB (An),Dm	mem8(An)→Dm	S — — — — — — —	S	—	—	—	—	—	—	—	2	2	*4
	MOVB (d8,An),Dm	mem8(An+d8)→Dm	S — — — — — — —	S	—	—	—	—	—	—	—	3	2	F5:20+An<<2+Dm:d8
	MOVB (d16,An),Dm	mem8(An+d16)→Dm	S — — — — — — —	S	—	—	—	—	—	—	—	4	2	F7:D0+An<<2+Dm:d16-l:d16-h
	MOVB (d24,An),Dm	mem8(An+d24)→Dm	S — — — — — — —	S	—	—	—	—	—	—	—	5	3	F4:A0+An<<2+Dm:d24-l:d24-m:d24-h
	MOVB (Di,An),Dm	mem8(An+Di)→Dm	S — — — — — — —	S	—	—	—	—	—	—	—	2	2	F0:40+Di<<4+An<<2+Dm
	MOVB (abs16),Dn	mem8(abs16)→Dn	S — — — — — — —	S	—	—	—	—	—	—	—	4	2	*5
	MOVB (abs24),Dn	mem8(abs24)→Dns	S — — — — — — —	S	—	—	—	—	—	—	—	5	3	F4:C4+Dn:abs24-l:abs24-m:abs24-h
	MOVB Dm,(An)	Dm→mem8(An)	— — — — — — —	—	—	—	—	—	—	—	—	1	1	10+Dm<<2+An
	MOVB Dm,(d8,An)	Dm→mem8(An+d8)	— — — — — — —	—	—	—	—	—	—	—	—	3	2	F5:10+An<<2+Dm:d8
	MOVB Dm,(d16,An)	Dm→mem8(An+d16)	— — — — — — —	—	—	—	—	—	—	—	—	4	2	F7:90+An<<2+Dm:d16-l:d16-h
	MOVB Dm,(d24,An)	Dm→mem8(An+d24)	— — — — — — —	—	—	—	—	—	—	—	—	5	3	F4:20+An<<2+Dm:d24-l:d24-m:d24-h
	MOVB Dm,(Di,An)	Dm→mem8(An+Di)	— — — — — — —	—	—	—	—	—	—	—	—	2	2	F0:C0+Di<<4+An<<2+Dm

Notes: 1* It is not possible to specify that Dn=Dm.

2* This instruction is supported by the assembler. For "MOV (d8,An),Am" the assembler will generate a bit pattern for d8=0.

3* This instruction is supported by the assembler. For "MOV Am,(d8,An)" the assembler will generate a bit pattern for d8=0.

4* This instruction is supported by the assembler. The assembler generates bit patterns for the two instructions "MOVB (An),Dm" and "EXTXB Dm".

5* This instruction is supported by the assembler. The assembler generates bit patterns for the two instructions "MOVB (abs16),Dn" and "EXTXB Dn".

Instruction	Mnemonic	Operation	OP EX.	Flag							Code Size	Cycle	Machine Code	
				VX	CX	NX	ZX	VF	CF	NF	ZF			
MOVB	MOVB Dn,(abs16)	Dn→mem8(abs16)	—	—	—	—	—	—	—	—	—	3	1	C4+Dn:abs16-l:abs16-h
	MOVB Dn,(abs24)	Dn→mem8(abs24)	—	—	—	—	—	—	—	—	—	5	3	F4:44+Dn:abs24-l:abs24-m:abs24-h
MOVBU	MOVBU (An),Dm	mem8(An)→Dm	0	—	—	—	—	—	—	—	—	1	1	30+An<<2+Dm
	MOVBU (d8,An),Dm	mem8(An+d8)→Dm	0	—	—	—	—	—	—	—	—	3	2	F5:30+An<<2+Dm:d8
	MOVBU (d16,An),Dm	mem8(An+d16)→Dm	0	—	—	—	—	—	—	—	—	4	2	F7:50+An<<2+Dm:d16-l:d16-h
	MOVBU (d24,An),Dm	mem8(An+d24)→Dm	0	—	—	—	—	—	—	—	—	5	3	F4:90+An<<2+Dm:d24-l:d24-m:d24-h
	MOVBU (Di,An),Dm	mem8(An+Di)→Dm	0	—	—	—	—	—	—	—	—	2	2	F0:80+Di<<4+An<<2+Dm
	MOVBU (abs16),Dn	mem8(abs16)→Dn	0	—	—	—	—	—	—	—	—	3	1	CC+Dn:abs16-l:abs16-h
	MOVBU (abs24),Dn	mem8(abs24)→Dn	0	—	—	—	—	—	—	—	—	5	3	F4:C8+Dn:abs24-l:abs24-m:abs24-h
EXT	EXT Dn	If Dn.bp15=0, x'0000'→MDR If Dn.bp15=1, x'FFFF'→MDR	S	—	—	—	—	—	—	—	—	2	3	F3:C1+Dn<<2 *6
EXTX	EXTX Dn	If Dn.bp15=0, Dn&x'00FFFF'→Dn If Dn.bp15=1, Dn x'FF0000'→Dn	S	—	—	—	—	—	—	—	—	1	1	B0+Dn *7
EXTXU	EXTXU Dn	Dn&x'00FFFF'→Dn	0	—	—	—	—	—	—	—	—	1	1	B4+Dn *8
EXTXB	EXTXB Dn	If Dn.bp7=0 Dn&x'0000FF'→Dn If Dn.bp7=1 Dn x'FFFF00'→Dn	S	—	—	—	—	—	—	—	—	1	1	B8+Dn *9
EXTXBU	EXTXBU Dn	Dn&x'0000FF'→Dn	0	—	—	—	—	—	—	—	—	1	1	BC+Dn *10
ADD	ADD Dn,Dm	Dm+Dn→Dm	—	●	●	●	●	●	●	●	●	1	1	90+Dn<<2+Dm
	ADD Dm,An	An+Dm→An	—	●	●	●	●	●	●	●	●	2	2	F2:00+Dm<<2+An
	ADD An,Dm	Dm+An→Dm	—	●	●	●	●	●	●	●	●	2	2	F2:C0+An<<2+Dm
	ADD An,Am	Am+An→Am	—	●	●	●	●	●	●	●	●	2	2	F2:40+An<<2+Am
	ADD imm8,Dn	Dn+imm8→Dn	S	●	●	●	●	●	●	●	●	2	1	D4+Dn:imm8
	ADD imm16,Dn	Dn+imm16→Dn	S	●	●	●	●	●	●	●	●	4	2	F7:18+Dn:imm16-l:imm16-h
	ADD imm24,Dn	Dn+imm24→Dn	—	●	●	●	●	●	●	●	●	5	3	F4:60+Dn:imm24-l:imm24-m:imm24-h
	ADD imm8,An	An+imm8→An	S	●	●	●	●	●	●	●	●	2	1	D0+An:imm8
	ADD imm16,An	An+imm16→An	S	●	●	●	●	●	●	●	●	4	2	F7:08+An:imm16-l:imm16-h
	ADD imm24,An	An+imm24→An	—	●	●	●	●	●	●	●	●	5	3	F4:64+An:imm24-l:imm24-m:imm24-h
ADDC	ADDC Dn,Dm	Dm+Dn+CF→Dm	—	●	●	●	●	●	●	●	●	2	2	F2:80+Dn<<2+Dm
ADDNF	ADDNF imm8,An	An+imm8→An	S	—	—	—	—	—	—	—	—	3	2	F5:0C+An:imm8 *11
SUB	SUB Dn,Dm	Dm-Dn→Dm	—	●	●	●	●	●	●	●	●	1	1	A0+Dn<<2+Dm
	SUB Dm,An	An-Dm→An	—	●	●	●	●	●	●	●	●	2	2	F2:10+Dn<<2+An
	SUB An,Dm	Dm-An→Dm	—	●	●	●	●	●	●	●	●	2	2	F2:D0+An<<2+Dm
	SUB An,Am	Am-An→Am	—	●	●	●	●	●	●	●	●	2	2	F2:50+An<<2+Am
	SUB imm16,Dn	Dn-imm16→Dn	S	●	●	●	●	●	●	●	●	4	2	F7:1C+Dn:imm16-l:imm16-h
	SUB imm24,Dn	Dn-imm24→Dn	—	●	●	●	●	●	●	●	●	5	3	F4:68+Dn:imm24-l:imm24-m:imm24-h
	SUB imm16,An	An-imm16→An	S	●	●	●	●	●	●	●	●	4	2	F7:0C+An:imm16-l:imm16-h
SUBC	SUBC Dn,Dm	Dm-Dn-CF→Dm	—	●	●	●	●	●	●	●	●	2	2	F2:90+Dn<<2+Dm
	MUL	MUL Dn,Dm	—	?	?	?	?	0	?	●	●	2	12	F3:40+Dn<<2+Dm *12
MULU	MULU Dn,Dm	Dm*Dn→Dm (Dm*Dn)>>16→MDR	—	?	?	?	?	0	?	●	●	2	12	F3:50+Dn<<2+Dm *13
DIVU	DIVU Dn,Dm	(MDR<<16+Dm)/Dn→Dm ***MDR	—	?	?	?	?	0/1	?	●/?	●/?	2	13	F3:60+Dn<<2+Dm *14

Notes: 6* 32-bit sign extended word data

7* 24-bit sign extended word data

8* 24-bit zero extended word data

9* 24-bit sign extended byte data

10* 24-bit zero extended byte data

11* Addition without changing flag

12* 16×16 = 32 (signed)

13* 16×16 = 32 (unsigned)

14* 32÷16 = 16...16 (unsigned)

Chapter 10 Appendix

Instruction	Mnemonic	Operation	OP EX.	Flag							Code Size	Cycle	Machine Code	
				VX	CX	NX	ZX	VF	CF	NF	ZF			
CMP	CMP Dn,Dm	Dm-Dn	—	●	●	●	●	●	●	●	●	2	2	F3:90+Dn<<2+Dm
	CMP Dm,An	An-Dm	—	●	●	●	●	●	●	●	●	2	2	F2:20+Dm<<2+An
	CMP An,Dm	Dm-An	—	●	●	●	●	●	●	●	●	2	2	F2:E0+An<<2+Dm
	CMP An,Am	Am-Am	—	●	●	●	●	●	●	●	●	2	2	F2:60+An<<2+Am
	CMP imm8,Dn	Dn-imm8	S	●	●	●	●	●	●	●	●	2	1	D8+Dn:imm8
	CMP imm16,Dn	Dn-imm16	S	●	●	●	●	●	●	●	●	4	2	F7:48+Dn:imm16-l:imm16-h
	CMP imm24,Dn	Dn-imm24	—	●	●	●	●	●	●	●	●	5	3	F4:78+Dn:imm24-l:imm24-m:imm24-h
	CMP imm16,An	An-imm16	0	●	●	●	●	●	●	●	●	3	1	EC+An:imm16-l:imm16-h
	CMP imm24,An	An-imm24	—	●	●	●	●	●	●	●	●	5	3	F4:7C+An:imm24-l:imm24-m:imm24-h
AND	AND Dn,Dm	Dm&(x'FF0000 Dn)→Dm	—	—	—	—	—	0	0	●	●	2	2	F3:00+Dn<<2+Dm *15
	AND imm8,Dn	Dn&(x'FF0000 imm8)→Dn	0	—	—	—	—	0	0	●	●	3	2	F5:00+Dn:imm8 *15
	AND imm16,Dn	Dn&(x'FF0000 imm16)→Dn	—	—	—	—	—	0	0	●	●	4	2	F7:00+Dn:imm16-l:imm16-h *15
	AND imm16,PSW	PSW&imm16→PSW	—	●	●	●	●	●	●	●	●	4	3	F7:10:imm16-l:imm16-h *15
OR	OR Dn,Dm	Dm (Dn&x'00FFFF)→Dm	—	—	—	—	—	0	0	●	●	2	2	F3:10+Dn<<2+Dm *15
	OR imm8,Dn	Dn imm8→Dn	0	—	—	—	—	0	0	●	●	3	2	F5:08+Dn:imm8 *15
	OR imm16,Dn	Dn imm16→Dn	—	—	—	—	—	0	0	●	●	4	2	F7:40+Dn:imm16-l:imm16-h *15
	OR imm16,PSW	PSW imm16→PSW	—	●	●	●	●	●	●	●	●	4	3	F7:14:imm16-l:imm16-h *15
XOR	XOR Dn,Dm	Dm^x'00FFFF&Dn)→Dm	—	—	—	—	—	0	0	●	●	2	2	F3:20+Dn<<2+Dm *15
	XOR imm16,Dn	Dn^imm16→Dn	—	—	—	—	—	0	0	●	●	4	2	F7:4C+Dn:imm16-l:imm16-h *15
NOT	NOT Dn	Dn^x'00FFFF→Dn	—	—	—	—	—	0	0	●	●	2	2	F3:E4+Dn *15
ASR	ASR Dn	Dn.lsbit→CF Dn.bp→Dn.bp-1(bp15 – 1) Dn.bp15→Dn.bp15	—	—	—	—	—	0	●	●	●	2	2	F3:38+Dn *15
LSR	LSR Dn	Dn.lsbit→CF Dn.bp→Dn.bp-1(bp15 – 1) 0→Dn.bp15	—	—	—	—	—	0	●	0	●	2	2	F3:3C+Dn *15
ROR	ROR Dn	Dn.lsbit→temp Dn.bp→Dn.bp-1(bp15 – 1) CF→Dn.bp15 temp→CF	—	—	—	—	—	0	●	●	●	2	2	F3:34+Dn *15
ROL	ROL Dn	Dn.bp15→temp Dn.bp→Dn.bp+1(bp14 – 0) CF→Dn.lsbit temp→CF	—	—	—	—	—	0	●	●	●	2	2	F3:30+Dn *15
BTST	BTST imm8,Dn	Dn&imm8 *** PSW	0	—	—	—	—	0	0	0	●	3	2	F5:04+Dn:imm8
	BTST imm16,Dn	Dn&imm16 *** PSW	0	—	—	—	—	0	0	●	●	4	2	F7:04+Dn:imm16-l:imm16-h
BSET	BSET Dm,(An)	mem8(An)&Dm *** PSW mem8(An) Dm→mem8(An)	0	—	—	—	—	0	0	0	●	2	5	F0:20+An<<2+Dm *16
BCLR	BCLR Dm,(An)	mem8(An)&Dm *** PSW mem8(An)&(~Dm)→mem8(An)	0	—	—	—	—	0	0	0	●	2	5	F0:30+An<<2+Dm *16
Bcc	BEQ label	If ZF=1, PC+2+d8(label)→PC If ZF=0, PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E8:d8 *17
	BNE label	If ZF=0, PC+2+d8(label)→PC If ZF=1, PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E9:d8 *18
	BLT label	If (VF^NF)=1, PC+2+d8(label)→PC If (VF^NF)=0, PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E0:d8 *19

Notes: 15* 16-bit computation

16* Performed under the conditions of bus lock and disabled interrupts.

17* src=dest (lower 16 bits)

18* src≠dest (lower 16 bits)

19* src>dest (lower 16 bits, signed)

Instruction	Mnemonic	Operation	OP EX.	Flag							Code Size	Cycle	Machine Code	
				VX	CX	NX	ZX	VF	CF	NF	ZF			
Bcc	BLE label	If ((VF^NF) ZF)=1, PC+2+d8(label)→PC If ((VF^NF) ZF)=0, PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E3:d8 *20
	BGE label	If (VF^NF)=0, PC+2+d8(label)→PC If (VF^NF)=1, PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E2:d8 *21
	BGT label	If ((VF^NF) ZF)=0, PC+2+d8(label)→PC If ((VF^NF) ZF)=1, PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E1:d8 *22
	BCS label	If CF=1, PC+2+d8(label)→PC If CF=0, PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E4:d8 *23
	BLS label	If (CF ZF)=1, PC+2+d8(label)→PC If (CF ZF)=0, PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E7:d8 *24
	BCC label	If CF=0, PC+2+d8(label)→PC If CF=1, PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E6:d8 *25
	BHI label	If (CF ZF)=0, PC+2+d8(label)→PC If (CF ZF)=1, PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E5:d8 *26
	BVC label	If VF=0, PC+3+d8(label)→PC If VF=1, PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:FC:d8 *27
	BVS label	If VF=1, PC+3+d8(label)→PC If VF=0, PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:FD:d8 *28
	BNC label	If NF=0, PC+3+d8(label)→PC If NF=1, PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:FE:d8 *29
	BNS label	If NF=1, PC+3+d8(label)→PC If NF=0, PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:FF:d8 *30
	BRA label	PC+2+d8(label)→PC	—	—	—	—	—	—	—	—	—	2	2	EA:d8
Bccx	BEQX label	If ZX=1, PC+3+d8(label)→PC If ZX=0, PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:E8:d8 *31
	BNEX label	If ZX=0, PC+3+d8(label)→PC If ZX=1, PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:E9:d8 *32

Notes: 20* src>dest (lower 16 bits, signed)

21* src<dest (lower 16 bits, signed)

22* src<dest (lower 16 bits, signed)

23* src>dest (lower 16 bits, unsigned)

24* src>dest (lower 16 bits, unsigned)

25* src<dest (lower 16 bits, unsigned)

26* src<dest (lower 16 bits, unsigned)

27* VF=0

28* VF=1

29* NF=0

30* NF=1

31* src=dest (24 bits)

32* src≠dest (24 bits)

Chapter 10 Appendix

Instruction	Mnemonic	Operation	OP EX.	Flag							Code Size	Cycle	Machine Code
				VX	CX	NX	ZX	VF	CF	NF	ZF		
Bccx	BLTX label	If $(VX \wedge NX) = 1$, PC+3+d8(label)→PC If $(VX \wedge NX) = 0$, PC+3→PC	— — — — — — — — — — — —	—	3	3/2	F5:E0:d8	*33					
	BLEX label	If $((VX \wedge NX) \mid ZX) = 1$, PC+3+d8(label)→PC If $((VX \wedge NX) \mid ZX) = 0$, PC+3→PC	— — — — — — — — — — — —	—	3	3/2	F5:E3:d8	*34					
	BGEX label	If $(VX \wedge NX) = 0$, PC+3+d8(label)→PC If $(VX \wedge NX) = 1$, PC+3→PC	— — — — — — — — — — — —	—	3	3/2	F5:E2:d8	*35					
	BGTX label	If $((VX \wedge NX) \mid ZX) = 0$, PC+3+d8(label)→PC If $((VX \wedge NX) \mid ZX) = 1$, PC+3→PC	— — — — — — — — — — — —	—	3	3/2	F5:E1:d8	*36					
	BCSX label	If CX=1, PC+3+d8(label)→PC If CX=0, PC+3→PC	— — — — — — — — — — — —	—	3	3/2	F5:E4:d8	*37					
	BLSX label	If $(CX \mid ZX) = 1$, PC+3+d8(label)→PC If $(CX \mid ZX) = 0$, PC+3→PC	— — — — — — — — — — — —	—	3	3/2	F5:E7:d8	*38					
	BCCX label	If CX=0, PC+3+d8(label)→PC If CX=1, PC+3→PC	— — — — — — — — — — — —	—	3	3/2	F5:E6:d8	*39					
	BHIX label	If $(CX \mid ZX) = 0$, PC+3+d8(label)→PC If $(CX \mid ZX) = 1$, PC+3→PC	— — — — — — — — — — — —	—	3	3/2	F5:E5:d8	*40					
	BVCX label	If VX=0, PC+3+d8(label)→PC If VX=1, PC+3→PC	— — — — — — — — — — — —	—	3	3/2	F5:EC:d8	*41					
	BVSX label	If VX=1, PC+3+d8(label)→PC If VX=0, PC+3→PC	— — — — — — — — — — — —	—	3	3/2	F5:ED:d8	*42					
JMP	JMP label16	PC+3+d16(label16)→PC	— — — — — — — — — — — —	—	3	2	FC:d16-l:d16-h						
	JMP label24	PC+5+d24(label24)→PC	— — — — — — — — — — — —	—	5	4	F4:E0:d24-l:d24-m:d24-h						
	JMP (An)	An→PC	— — — — — — — — — — — —	—	2	3	F0:An<<2						

Notes: 33* src>dest (24 bits, signed)

34* src>dest (24 bits, signed)

35* src≤dest (24 bits, signed)

36* src<dest (24 bits, signed)

37* src>dest (24 bits, unsigned)

38* src≥dest (24 bits, unsigned)

39* src≤dest (24 bits, unsigned)

40* src<dest (24 bits, unsigned)

41* VX=0

42* VX=1

43* NX=0

44* NX=1

Instruction	Mnemonic	Operation	OP EX.	Flag							Code Size	Cycle	Machine Code	
				VX	CX	NX	ZX	VF	CF	NF	ZF			
JSR	JSR label16	A3-4→A3 PC+3→mem24(A3) PC+3+d16(label16)→PC	—	—	—	—	—	—	—	—	—	3	4	FD:d16-l:d16-h
	JSR label24	A3-4→A3 PC+5→mem24(A3) PC+5+d24(label24)→PC	—	—	—	—	—	—	—	—	—	5	5	F4:E1:d24-l:d24-m:d24-h
	JSR (An)	A3-4→A3 PC+2→mem24(A3) An→PC	—	—	—	—	—	—	—	—	—	2	5	F0:01+An<<2
NOP	NOP	PC+1→PC	—	—	—	—	—	—	—	—	—	1	1	F6
RTS	RTS	mem24(A3)→PC A3+4→A3	—	—	—	—	—	—	—	—	—	1	5	FE
RTI	RTI	mem16(A3)→PSW mem24(A3+2)→PC A3+6→A3	—	●	●	●	●	●	●	●	●	1	6	EB

How to Read INSTRUCTION SET

■ Explanation of symbols used in the chart

Dn, Dm, Di	Data register
An, Am	Address register
MDR, PSW, PC	Multiplication and division register, program status word, program counter
imm8, imm16, imm16-l, imm16-h	Constant
imm24, imm24-l, imm24-m, imm24-h	
d8, d16, d16-l, d16-h	Displacement
d24, d24-l, d24-m, d24-h	
abs16, abs16-l, abs16-h	Absolute address
abs24, abs24-l, abs24-m, abs24-h	
mem8 (An), mem8 (abs16), mem8 (abs24)	8-bit memory data referenced at the address enclosed in parenthesis
mem16 (An), mem16 (abs16), mem16 (abs24)	16-bit memory data referenced at the address enclosed in parenthesis
mem24 (Am), mem24 (abs16), mem24 (abs24)	24-bit memory data referenced at the address enclosed in parenthesis
.bp,.lsb,.msb	Bit specification
&, , ^	Logical AND, logical OR, exclusive OR
~, <<	Bit reversal, bit shift
VX, CX, NX, ZX	Extended overflow flag, extended carry flag, extended negative flag, extended zero flag
VF, CF, NF, ZF	Overflow flag, carry flag, negative flag, zero flag
temp	Temporary register inside CPU
→, ...	Assignment, reflection of computation results

■ OP EX. (Operand Extension)

O	zero extension
S	sign extension
—	not applicable

■ Flag

●	change
—	no change
0	normally 0
1	normally 1
?	undefined

■ Code Size

Unit: byte

■ Cycle

The minimum number of cycles are specified.

Unit: machine cycle

- a/b:
there are branches in the 'a' cycle
there are no branches in the 'b' cycle

■ Machine Code

[:] separates the byte units. [<<2] indicates a 2-bit shift.

Dn, Dm, Di, An, Am: register numbers

D0	00	A0	00
D1	01	A1	01
D2	10	A2	10
D3	11	A3	11

■ Notes

- Instructions that access 16-bit and 24-bit data must use an even memory address.
- All 8-bit displacements (d8) and 16-bit displacements (d16) are sign extended.

Chapter 10 Appendix

MN102L00 SERIES INSTRUCTION MAP

First Byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	MOV Dm, (An)															
1	MOVB Dm, (An)															
2	MOV (An), Dm															
3	MOVBU (An), Dm															
4	MOV Dm, (d8, An)															
5	MOV Am (d8, An)															
6	MOV (d8, An), Dm															
7	MOV (d8, An), Am															
8	MOV Dn, Dm (When src=dest, MOV imm8, Dn)															
9	ADD Dn, Dm															
A	SUB Dn, Dm															
B	EXTX Dn				EXTXU Dn				EXTXB Dn				EXTXBU Dn			
C	MOV Dn, (abs16)				MOVB Dn, (abs16)				MOV (abs16),Dn				MOVBU (abs16),Dn			
D	ADD imm8, An				ADD imm8, Dn				CMP imm8, Dn				MOV imm16, An			
E	BLT label	BGT label	BGE label	BLE label	BCS label	BHI label	BCC label	BLS label	BEQ label	BNE label	BRA label	RTI		CMP imm16, An		
F	Code extended (2 bytes)				Code extended (5 bytes)	Code extended (3 bytes)	NOP	Code extended (4 bytes)		MOV imm16, Dn			JMP label16	JSR label16	RTS	

Two-Byte Instructions (First byte: F0)

Second Byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JMP (A0)	JSR (A0)			JMP (A1)	JSR (A1)			JMP (A2)	JSR (A2)			JMP (A3)	JSR (A3)		
1																
2	BSET Dm, (An)															
3	BCLR Dm, (An)															
4																
5	MOVB (Di, An), Dm															
6																
7																
8																
9	MOVBU (Di, An), Dm															
A																
B																
C																
D	MOVB Dm, (Di, An)															
E																
F																

Two-Byte Instructions (First byte: F1)

Second Byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1											MOV (Di, An), Am					
2																
3																
4																
5											MOV (Di, An), Dm					
6																
7																
8																
9											MOV Am ,(Di, An)					
A																
B																
C																
D											MOV Dm, (Di, An)					
E																
F																

Two-Byte Instructions (First byte: F2)

Second Byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0											ADD Dm, An					
1											SUB Dm, An					
2											CMP Dm, An					
3											MOV Dm, An					
4											ADD An, Am					
5											SUB An, Am					
6											CMP An, Am					
7											MOV An, Am					
8											ADDC Dn, Dm					
9											SUBC Dn, Dm					
A																
B																
C											ADD An, Dm					
D											SUB An, Dm					
E											CMP An, Dm					
F											MOV An, Dm					

Chapter 10 Appendix

Two-Byte Instructions (First byte: F3)

Second Byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	AND Dn, Dm															
1	OR Dn, Dm															
2	XOR Dn, Dm															
3	ROL Dn		ROR Dn			ASR Dn			LSR Dn							
4	MUL Dn, Dm															
5	MULU Dn, Dm															
6	DIVU Dn, Dm															
7																
8																
9	CMP Dn, Dm															
A																
B																
C	MOV D0, MDR	EXT D0		MOV D1, MDR	EXT D1		MOV D2, MDR	EXT D2		MOV D3, MDR	EXT D3					
D	MOV D0, PSW			MOV D1, PSW			MOV D2, PSW			MOV D3, PSW						
E	MOV MDR, Dn		NOT Dn													
F	MOV PSW, Dn															

Five-Byte Instructions (First byte: F4)

Second Byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	MOV Dm, (d24, An)															
1	MOV Am, (d24, An)															
2	MOVB Dm, (d24, An)															
3	MOVX Dm, (d24, An)															
4	MOV Dn, (abs24)		MOVB Dn, (abs24)													
5	MOV An, (abs24)															
6	ADD imm24, Dn		ADD imm24, An		SUB imm24, Dn		SUB imm24, An									
7	MOV imm24, Dn		MOV imm24, An		CMP imm24, Dn		CMP imm24, An									
8	MOV (d24, An), Dm															
9	MOVBU (d24, An), Dm															
A	MOVB (d24, An), Dm															
B	MOVX (d24, An), Dm															
C	MOV (abs24), Dn		MOVB (abs24), Dn		MOVBU (abs24), Dn											
D	MOV (abs24), An															
E	JMP label24	JSR label24														
F	MOV (d24, An), Am															

Three-Byte Instructions (First byte: F5)

Second Byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	AND imm8, Dn				BTST imm8, Dn				OR imm8, Dn				ADDNF imm8, An			
1		MOV B Dm, (d8, An)														
2		MOV B (d8, An), Dm														
3		MOVBU (d8, An), Dm														
4																
5		MOVX Dm, (d8, An)														
6																
7		MOVX (d8, An), Dm														
8																
9																
A																
B																
C																
D																
E	BLTX label	BGTX label	BGEX label	BLEX label	BCSX label	BHIX label	BCCX label	BLSX label	BEQX label	BNEX label			BVCX label	BVSX label	BNCX label	BNSX label
F													BVC label	BVS label	BNC label	BNS label

Four-Byte Instructions (First byte: F7)

Second Byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	AND imm16, Dn				BTST imm16, Dn				ADD imm16, An			SUB imm16, An				
1	AND imm16 PSW				OR imm16 PSW				ADD imm16, Dn			SUB imm16, Dn				
2	MOV An, (abs16)															
3	MOV (abs16), An															
4	OR imm16, Dn								CMP imm16, Dn			XOR imm16, Dn				
5	MOVBU (d16, An), Dm															
6	MOVX Dm,(d16, An)															
7	MOVX (d16, An), Dm															
8	MOV Dm,(d16, An)															
9	MOVB Dm,(d16, An)															
A	MOV Am,(d16, An)															
B	MOV (d16, An), Am															
C	MOV (d16, An), Dm															
D	MOVB (d16, An), Dm															
E																
F																

10-4 Initialization Program

After reset, the initialization program must be located in block 0 (x'000000'~x'3FFFFF'). The initialization program first sets the number of wait cycles for block 0 in the MEMMD0 register. Next, the MEMCTR register is set. The handshake mode must be selected for the MEMCTR register setting. The number of wait cycles set in the MEMMD0 register become valid after the access that follows the MEMCTR register setting.

<pre>;Initialization Program init equ*</pre>	
<pre>;Block 0 memory mode setting mov MEM0_INIT,d0 mov d0, (Amemmd0)</pre>	The MEMMD0 register is set with the number of wait cycles for block 0.
<pre>;Handshake mode is set mov MEMCTR_INIT,d0 mov d0, (Amemctr)</pre>	Bit 8 (WAITSET) of the MEMCTR register is set to '0'.
<pre>;Block 1, 2, 3 memory mode setting mov MEM1_INIT,d0 mov d0, (Amemmd1) mov MEM2_INIT,d0 mov d0, (Amemmd2) mov MEM3_INIT,d0 mov d0, (Amemmd3)</pre>	The number of wait cycles for each block are set in the MEMMDn registers (n=1, 2, 3).
<pre>;DRAM/pseudo SRAM setting mov REFC_INIT,d0 mov d0, (Arefcnt) mov DRAMC_INIT,d0 mov d0, (Adrmctr)</pre>	If any MEMMDn register (n=1, 2, 3) was set for DRAM or pseudo SRAM, DRMCTR and REFCNT are set.
<pre>;Register initialization sub d0,d0 mov d0,d1 mov d0,d2 mov d0,d3 mov d0,a0 mov d0,a1 mov d0,a2</pre>	Registers are initialized to '0'. While this initialization is not absolutely necessary, it should be performed as a precaution.
<pre> mov STACK_TOP,a3</pre>	The initial value of the stack point is set. (An even address must be set.)
<pre>;Interrupt enable mov INIT_PSW,d0 mov d0, psw</pre>	If interrupts are to be used, after setting the stack, the interrupt mode is set. The PSW interrupt enable flag is set to '1'.



Handshake mode must be selected for the MN1020012's MEMCTR register setting.



The MEMMD0 register and MEMCTR register must be set in this sequence. If the settings are performed in another sequence write operations to the MEMCTR register are not guaranteed.

A value of x'0410' is recommended for MEMCTR_INIT.



The REFCNT register is 0 during reset. Without setting the refresh interval in the REFCNT register, if refresh is enabled by the DRMCTR register, a refresh cycle will be activated every cycle. Therefore, the REFCNT register must be set first.

In the program, the following symbols and register addresses are equivalent.

(Amemctr)=(x'FC02')
 (Amemmd0)=(x'FC30')
 (Amemmd1)=(x'FC32')
 (Amemmd2)=(x'FC34')
 (Amemmd3)=(x'FC36')
 (Arefcnt)=(x'FD02')
 (Adrmctr)=(x'FD00')

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