

# Yizhou Shan

Email: [ys@purdue.edu](mailto:ys@purdue.edu)

Phone: (+1)765-337-0133

## RESEARCH INTERESTS

My research interests span Operating Systems, Distributed Systems, and Non-Volatile Memory Systems, with a focus on building fast and reliable systems for datacenters. I work at the Wuklab under the supervision of Yiying Zhang.

## EDUCATION

**Purdue University** October 2016 – Present  
Ph.D. in Computer Engineering

**Institute of Computing Technology, Chinese Academy of Sciences** June 2016  
Graduate Coursework in Computer Science

**Beijing University of Aeronautics and Astronautics** June 2014  
B.E. in Computer Engineering

## PUBLICATIONS

Yizhou Shan, Shin-Yeh Tsai, Yiying Zhang, “**Distributed Shared Persistent Memory**”, Proceedings of the ACM Symposium on Cloud Computing 2017 (**SoCC’17**)

Yizhou Shan, Yilun Chen, Yutong Huang, Sumukh Hallymysore, Yiying Zhang, “**Lego: A Distributed, Decomposed OS for Resource Disaggregation**”, Poster at the 26th ACM Symposium on Operating Systems Principles (**SOSP’17**)

## RESEARCH EXPERIENCE

**Disaggregated Operating System** April 2017 – Present  
*Purdue University*

Design and implement a disaggregated operating system from scratch, for the emerging disaggregated datacenter architecture. Currently, the basic kernel functionalities are finished, we are focusing on the failure-tolerance part now.

**Distributed Shared Persistent Memory** September 2016 – April 2017  
*Purdue University*

Proposed the concept of distributed shared persistent memory. Designed and implemented Hotpot, an in-kernel RDMA-based distributed shared persistent memory system.

**NVM Emulator** October 2015 – January 2016  
*Institute of Computing Technology, Chinese Academy of Sciences*

Designed and implemented a NVM emulator in Linux kernel, which leverages Intel’s performance monitoring unit to emulate NVM’s slower read/write latency and smaller bandwidth on physical DRAM.

**ARMv8 CPU Project** June 2013 – September 2013  
*Institute of Computing Technology, Chinese Academy of Sciences*

Participated in the Register-Transfer Level design and verification of some blocks within cache unit and load-store unit.