Yongming Ding

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EDUCATION

Shanghai Jiao Tong University (SJTU), Shanghai
Master of Science in Electronic Science and Technology *Sep. 2016 - Present*
⋄ Overall GPA: 3.79/4.3 ⋄ Major GPA: 3.90/4.3
⋄ Awards: 1^{st} Prize in 12th China Graduate Electronics Design Contest
Bachelor of Science in Microelectronics *Sep. 2012 - Jun. 2016*
⋄ Overall GPA: 3.63/4.3 ⋄ Major GPA: 3.80/4.3
⋄ Received waiver for the National College Entrance Exam to enter SJTU, as 1st Prize in National Olympiad in Physics (Henan Province, top 0.01%)
⋄ Solid expertise in Python, Experienced in C/C++, Javascript, HTML/CSS, SQL, JAVA, MATLAB

INTERNSHIP

Ctrip Computer Technology Co.Ltd, Shanghai *July. 2015 - Dec. 2015*
Software Engineer Intern
⋄ Developed and improved software tools to enhance site reliability and increase products development efficiency.
⋄ Constructed "Alert-Subscribe", an alert event subscription system with another intern. Completed the back-end job including getting alert events periodically, classifying alert events with regular expression and sending notification to subscribers, using Python and SQL.
⋄ Independently designed and implemented "Prometheus", a Web service cluster consumers display platform, to show the dependency relationships between Web service clusters, using Django to create the back-end, Bootstrap for the front-end, MySQL for the database and Redis to store tasks scheduling queue.

PUBLICATIONS

Yongming Ding, Wei Jin, Guanghui He, Weifeng He. "Short Path Padding with Multiple-Vt cells for Wide-Pulsed-Latch Based Circuits at Ultra-Low Voltage." *IEEE International Conference on ASIC* (2017). Accepted.

RESEARCHES AND PROJECTS

Short Path Padding Technique Design *July. 2016 - present*
⋄ Designed and implemented a short path padding software system employing integer linear programming method, which supports up to a wide pulse of 1/3 cycle time in pulsed-latch pipelines.
⋄ Proposed step-by-step based and path group based schemes to reduce up to 80.9% runtime of the baseline padding algorithm and used multiple-Vt buffer cells to reduce 52.3% additional hardware cost on average.
Image Super-Resolution Using Convolutional Neural Network(CNN) *July. 2017*
⋄ Applied deep learning techniques to sharpen or improve the quality of a low-resolution image input by outputting a super-resolved high-resolution image output. Proposed a 7-layers CNN which got lower loss value and reduced 10% training time, compared with "waifu2x", a open source image super-resolution software.
"Eye of Providenc", Intelligent Monitoring System *May. 2017*
⋄ Led a group of 4 teammates to build an intelligent classroom monitoring system using face recognition, facial expression detection and speech identification techniques during "Hackthon SJTU 2017".
Three-dimensional Integrated Circuit(3D-IC) Partitioning Technique Design *Jan. 2016 - Jun. 2016*
⋄ Excellent graduate thesis in Department of Micro-Nano Electronics, Shanghai Jiao Tong University.
⋄ Designed a 3D-IC partitioning algorithm and evaluation platform for motion estimation(ME) module of HEVC, including the initial partition algorithm based on breath first search and the iterative optimization algorithm.
⋄ Achieved optimum partition for ME module. Reduced 43% of cut edges while area utilization rate reached 96%.
"Yorozuya", a Campus Labor and Information Exchange Platform *Nov. 2014*
⋄ Devoloped a web application for campus users to exchange labor and information in "Hackthon SJTU 2014" with a teammate. Users can release tasks on this app while the others can choose and finish jobs for reward.

HONORS, AWARDS AND CERTIFICATES

Senior skill level computer programmer (JAVA, ARM), occupational qalification certificate, China *2015, 2016*
Scholarship of Academic Excellence, Shanghai Jiao Tong University *2014, 2013*
Outstanding student, Shanghai Jiao Tong University *2014, 2013*
2^{nd} Prize in Shanghai Region, National College Student Physics Competition *2013*