Yongming Ding

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EDUCATION

Shanghai Jiao Tong University (SJTU), Shanghai

Master of Science in Electronic Science and Technology *Sep. 2016 – Mar. 2019(expected)*

◇ Major GPA: 4.00/4.00 Ranking: 1/116 ◇ Overall GPA: 3.72/4.00

◇ 1^{st} Prize in 12th China Graduate Electronics Design Contest (Ranked 2^{nd} in more than 100 teams in the final)

Bachelor of Science in Microelectronics *Sep. 2012 – Jun. 2016*

◇ Major GPA: 87.70/100 Ranking: 8/50 ◇ Overall GPA: 86.27/100

◇ Major GPA: 89.30/100(upper division) ◇ Overall GPA: 89.13/100(upper division)

◇ Received a waiver for the National College Entrance Exam to enter SJTU, as 1^{st} Prize in National Olympiad in Physics (Henan Province, top 0.01%)

PUBLICATIONS

Yongming Ding, Wei Jin, Guanghui He, Weifeng He. "Short Path Padding with Multiple-Vt cells for Wide-Pulsed-Latch Based Circuits at Ultra-Low Voltage." *IEEE International Conference on ASIC* (2017). Accepted.

RESEARCHES EXPERIENCE

Short Path Padding Technique Design *July 2016 – present*

Advised by Prof. Weifeng He *Research Center of Digital Circuit Design & SoC technology, SJTU*

- ◇ Designed and implemented a short path padding software system employing integer linear programming method, which supports up to a wide pulse of 1/3 cycle time in pulsed-latch pipelines.
- ◇ Proposed step-by-step based and path group based schemes to reduce 80.9% runtime of the baseline padding algorithm and used multiple-Vt buffer cells to reduce additional hardware cost by 52.3%, on average.

Microprocessor Design Based on Wide-Pulsed-Latch at Ultra-Low Voltage *May 2017 – present*

Advised by Prof. Weifeng He *Research Center of Digital Circuit Design & SoC technology, SJTU*

- ◇ Designed a low leakage 16x16 10T SRAM array for MIPS microprocessor working at ultra-low voltage 0.35V.
- ◇ Formed the boundary scan chain for testing and implemented clock generator module.
- ◇ The MIPS microprocessor is now in back-end process and will tape out on TSMC 65nm CMOS process soon.

Three-dimensional Integrated Circuit(3D-IC) Partitioning Technique Design *Jan. 2016 – Jun. 2016*

Advised by Prof. Weifeng He *Research Center of Digital Circuit Design & SoC technology, SJTU*

- ◇ Excellent graduate thesis in Department of Micro-Nano Electronics, Shanghai Jiao Tong University.
- ◇ Designed a 3D-IC partitioning algorithm for motion estimation(ME) module of HEVC, including an initial partition algorithm based on breadth first search and an iterative optimization algorithm.
- ◇ Achieved an optimum partition for the ME module, which reduced 42.9% of the cut edges while the area utilization rate reached 95.5%.

Design and Implementation of a Wearable Vital Signs Monitoring System *Mar. 2015 – Mar. 2016*

Advised by Prof. Guoxing Wang *Bio-Circuits and Systems Lab, SJTU*

- ◇ Led a group of 4 teammates to design a wearable signs monitoring system that includes respiratory rate, body temperature and blood oxygen saturation monitoring.
- ◇ Responsible for the overall system design and implementation of the blood oxygen saturation monitoring module.
- ◇ Designed a transmissive pulse oximetry probe with LEDs and Photodiode to obtain the PPG signal, the amplifying and conversion circuit for the PPG signal, and implemented the PCB for the circuit.
- ◇ Programmed an embedded system to convert the PPG signal into oxygen saturation value and transfer data to mobile devices through Bluetooth.

FPGA Implementation of FastICA Algorithm for Blind Source Separation *Oct. 2013 – Nov. 2014*

Advised by Prof. Jiang Jiang *Lab of Embedded Architecture, SJTU*

- ◇ Led a group of 4 teammates to implement a blind source separation system on FPGA using FastICA algorithm.
- ◇ Took charge of testing and verifying the FastICA algorithm on MATLAB and then implementing it on FPGA.
- ◇ The FPGA implementation greatly reduced the computation time, at least 40 times faster than software.

PROFESSIONAL EXPERIENCE

Shanghai Jiao Tong University, Shanghai *Feb. 2017 – Jun. 2017*
Teaching Assistant *Course Design for Digital Integrated Circuit Design (MR322)*

Ctrip Computer Technology Co.,Ltd., Shanghai *July 2015 – Dec. 2015*
Software Engineer Intern *Application Management Group, Ctrip Infrastructure Service*

- ◇ Developed and improved software tools to enhance site reliability and boost the efficiency of developing products.
- ◇ **Constructed "Alert-Subscribe", an alert event subscription system**.
  This system will send notifications to users through email or SMS when subscribed alert events happen, so that operation engineers can quickly fetch and fix alert events. Completed the back-end job including obtaining alert events periodically, classifying alert events with RegEx and sending notifications to subscribers.
- ◇ **Designed and implemented "Prometheus", a web service cluster consumers display platform**.
  This project was designed to show the dependency relationships between web service clusters.
  Implemented it independently using Django as a back-end framework, Bootstrap as the front-end framework, and MySQL and Redis database to store tasks scheduling queue.

SELECTED PROJECTS

Implementation of Unate Recursive Complement Algorithm *Aug. 2017*
Advised by Prof. Weikang Qian *Emerging Computing Technology Laboratory, SJTU*

- ◇ Developed a program that performs the unate recursive complement using the Unate Recursive Paradigm idea.
- ◇ Given an input file representing a Boolean function F as a Positional Cube Notation (PCN) cube list, this program will complement it and return the result as a PCN cube list.

Image Super-Resolution Using Convolutional Neural Network(CNN) *July 2017*
Advised by Prof. Haibao Chen *Innovative Computer Architecture Technology Lab, SJTU*

- ◇ Applied deep learning techniques to sharpen or improve the quality of a low-resolution image input by outputting a super-resolved high-resolution image. Proposed a 7-layers CNN which got lower loss value and reduced 10% training time, compared with "waifu2x", an open source image super-resolution software.

"Eye of Providence", an Intelligent Monitoring System *May 2017*

- ◇ Led a group of 4 teammates to build an intelligent classroom monitoring system using face recognition, facial expression detection and speech identification techniques during "Hackathon SJTU 2017".

RF Narrowband Low Noise Amplifier (LNA) Design *Nov. 2015*
Advised by Prof. Jianjun Zhou *Center for Analog/RF Integrated Circuits, SJTU*

- ◇ Designed a 2V 1.575GHz differential cascode LNA with 3mA bias current using additional inductors and capacitive cross-coupling to reduce noise and improve linearity. NF reached 1.93dB, S11 -13.37dB, S22 -20.29dB, S12 -34.17dB, S21 17.01dB, and IIP3 at 1.575GHz & 1.580GHz -10.77dBm.

Design and realization of 5-stage-pipeline MIPS processor *Nov. 2014*
Advised by Prof. Yongxin Zhu *Lab of Embedded Architecture, SJTU*

- ◇ Acted as a team leader and took charge of the module design and Verilog HDL code implementation.
- ◇ Resolved data hazards using forwarding and implemented dynamic branch prediction to deal with control hazards.

HONORS, AWARDS AND CERTIFICATES

Tang Youshu Scholarship, Shanghai Jiaotong University (4 recipients out of 116 students)	*2017*
3^{rd} Prize in National Post-Graduate Mathematic Contest in Modeling	*2017*
First-class Academic Graduate Student Scholarship, Shanghai Jiao Tong University	*2016*
Senior skill level computer programmer (JAVA, ARM), Occupational qualification certificate, China	*2015 & 2016*
Scholarship of Academic Excellence, Shanghai Jiao Tong University	*2014 & 2013*
Outstanding student, Shanghai Jiao Tong University	*2014 & 2013*
2^{nd} Prize in Shanghai Region, National College Student Physics Competition	*2013*

SKILLS AND INTERESTS

Programming	Python, Verilog HDL, C/C++, JAVA, Javascript, HTML/CSS, SQL, MATLAB
Software	Cadence, Design Compiler, IC Compiler, HSPICE, Vivado, ModelSim, ISE
Technologies	TensorFlow, FPGA, Scikit-learn, Django, Bootstrap, MySQL, Redis
Interests	Photography, Swimming, Post-rock, Table Tennis, Cycling