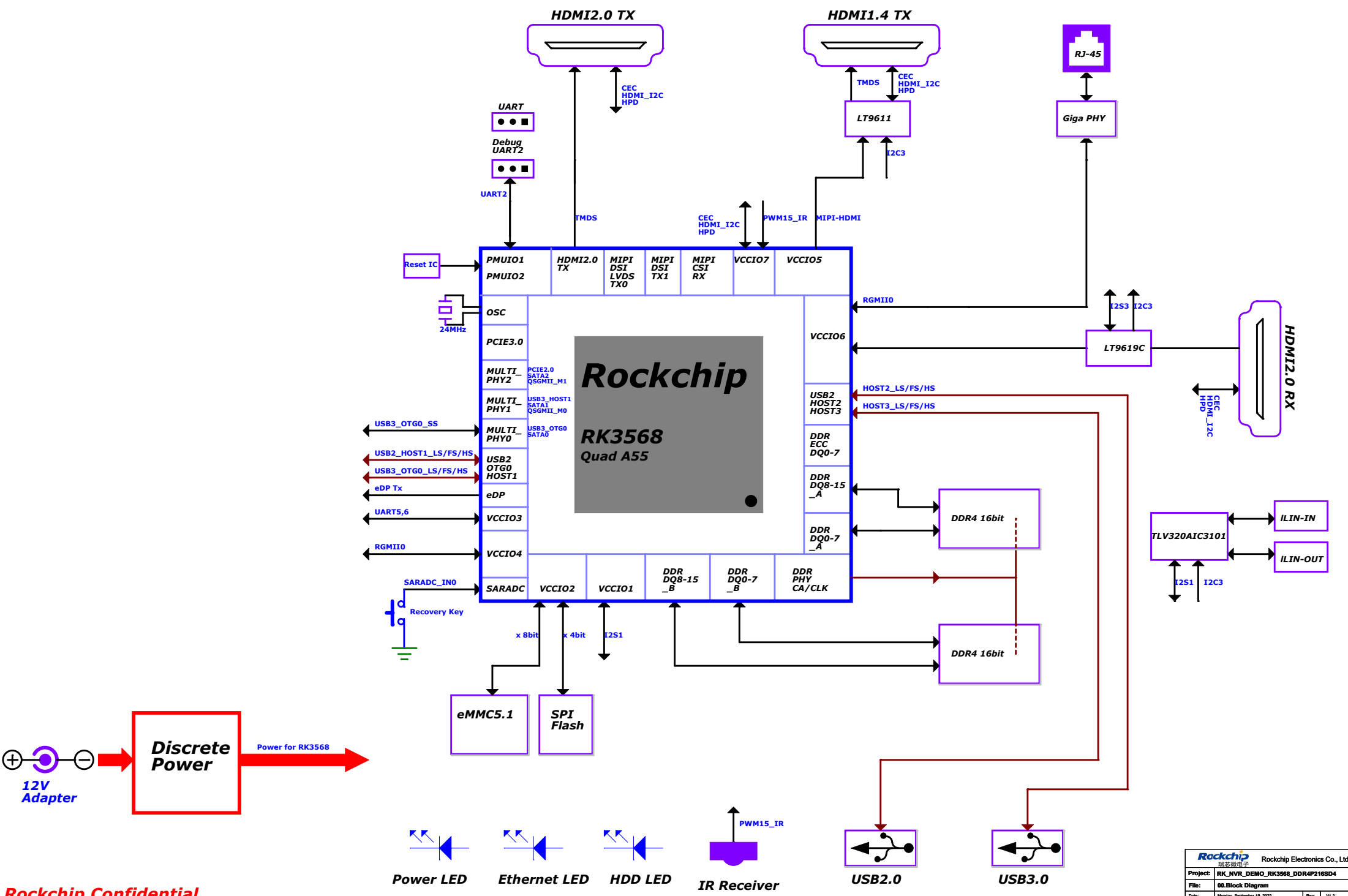
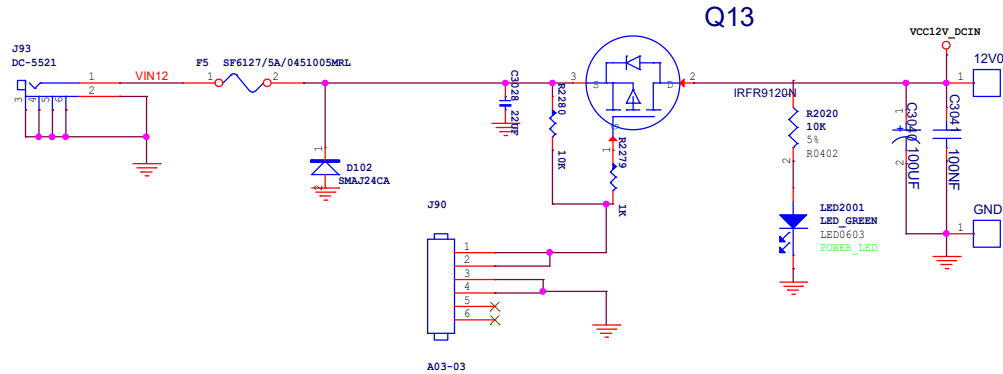


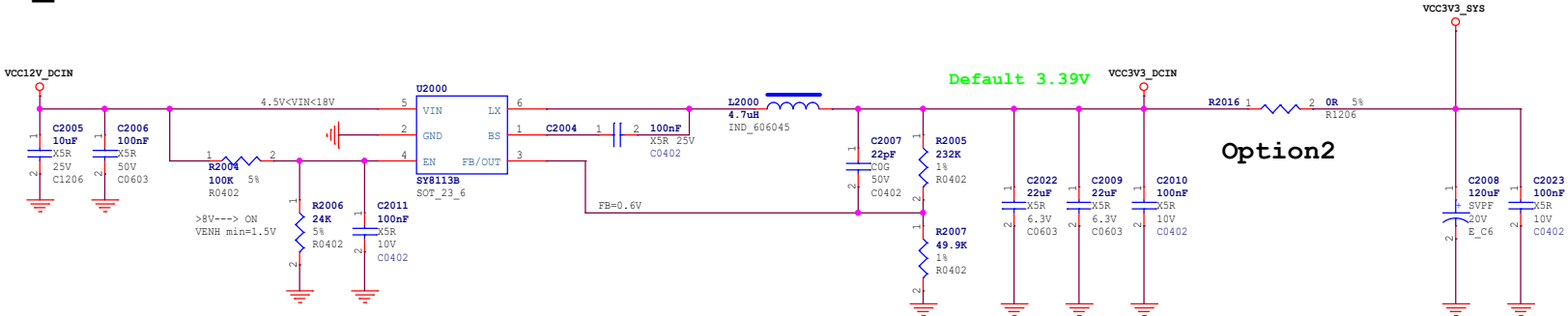
RK3568 NVR DEMO Block Diagram



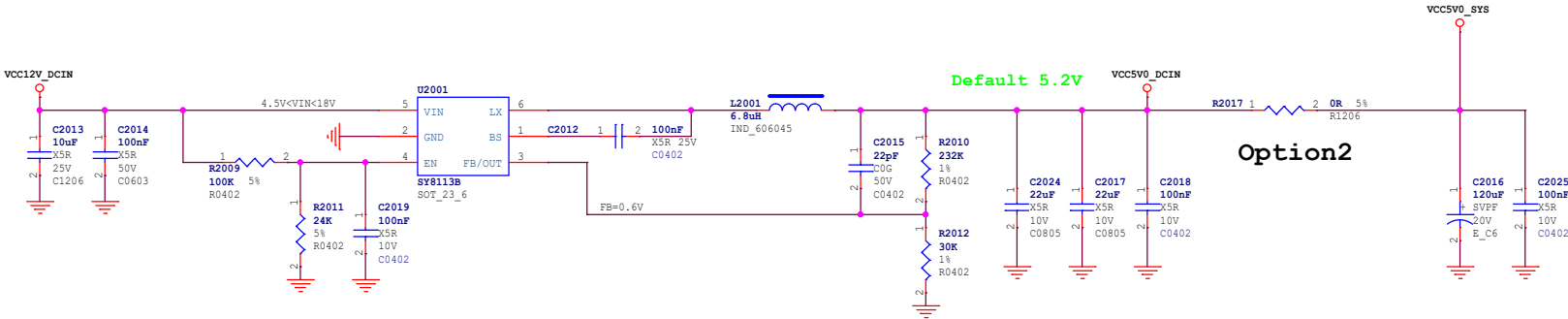
12V/3A DCIN



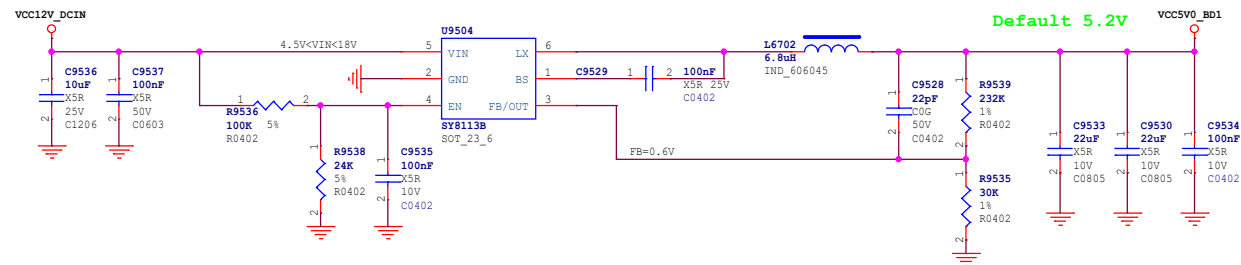
VCC3V3\_SYS



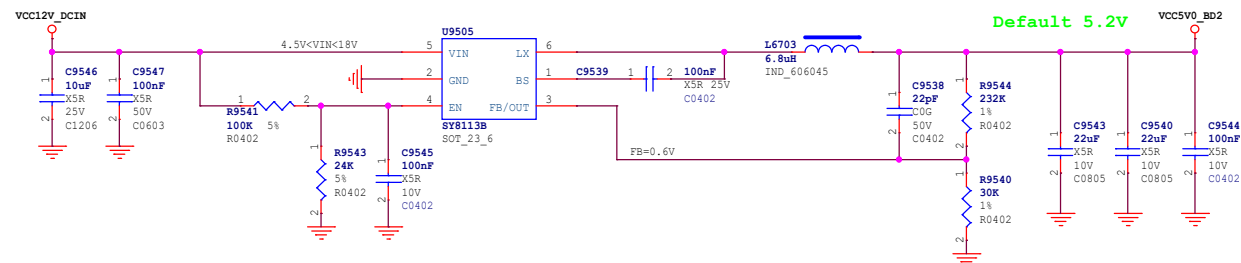
VCC5V0\_SYS



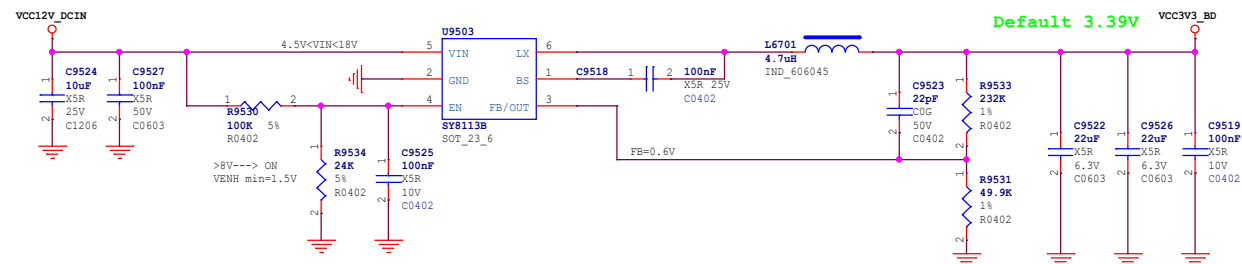
## VCC5V0\_BD1

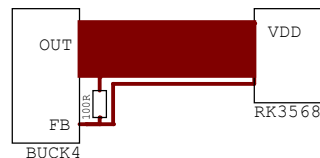


## VCC5V0\_BD2



## VCC3V3\_BD





The schematic diagram illustrates the RK809-5 DCDC converter, which is a 4-channel buck converter. It features four buck regulators (BUCK1, BUCK2, BUCK3, BUCK4) and a feedback network. The input is VDD\_LOGIC, and the output is VDD\_GPU. The feedback network consists of resistors R2100, R2101, R2102, R2103, R2104, R2105, R2106, R2107, R2108, R2109, R2110, R2111, R2112, R2113, R2114, R2115, R2116, R2117, R2118, R2119, R2120, R2121, R2122, R2123, R2124, R2125, R2126, R2127, R2128, R2129, R2130, R2131, R2132, R2133, R2134, R2135, R2136, R2137, R2138, R2139, R2140, R2141, R2142, R2143, R2144, R2145, R2146, R2147, R2148, R2149, R2150, R2151, R2152, R2153, R2154, R2155, R2156, R2157, R2158, R2159, R2160, R2161, R2162, R2163, R2164, R2165, R2166, R2167, R2168, R2169, R2170, R2171, R2172, R2173, R2174, R2175, R2176, R2177, R2178, R2179, R2180, R2181, R2182, R2183, R2184, R2185, R2186, R2187, R2188, R2189, R2190, R2191, R2192, R2193, R2194, R2195, R2196, R2197, R2198, R2199, R2200, R2201, R2202, R2203, R2204, R2205, R2206, R2207, R2208, R2209, R2210, R2211, R2212, R2213, R2214, R2215, R2216, R2217, R2218, R2219, R2220, R2221, R2222, R2223, R2224, R2225, R2226, R2227, R2228, R2229, R2230, R2231, R2232, R2233, R2234, R2235, R2236, R2237, R2238, R2239, R2240, R2241, R2242, R2243, R2244, R2245, R2246, R2247, R2248, R2249, R2250, R2251, R2252, R2253, R2254, R2255, R2256, R2257, R2258, R2259, R2260, R2261, R2262, R2263, R2264, R2265, R2266, R2267, R2268, R2269, R2270, R2271, R2272, R2273, R2274, R2275, R2276, R2277, R2278, R2279, R2280, R2281, R2282, R2283, R2284, R2285, R2286, R2287, R2288, R2289, R2290, R2291, R2292, R2293, R2294, R2295, R2296, R2297, R2298, R2299, R2300, R2301, R2302, R2303, R2304, R2305, R2306, R2307, R2308, R2309, R2310, R2311, R2312, R2313, R2314, R2315, R2316, R2317, R2318, R2319, R2320, R2321, R2322, R2323, R2324, R2325, R2326, R2327, R2328, R2329, R2330, R2331, R2332, R2333, R2334, R2335, R2336, R2337, R2338, R2339, R2340, R2341, R2342, R2343, R2344, R2345, R2346, R2347, R2348, R2349, R2350, R2351, R2352, R2353, R2354, R2355, R2356, R2357, R2358, R2359, R2360, R2361, R2362, R2363, R2364, R2365, R2366, R2367, R2368, R2369, R2370, R2371, R2372, R2373, R2374, R2375, R2376, R2377, R2378, R2379, R2380, R2381, R2382, R2383, R2384, R2385, R2386, R2387, R2388, R2389, R2390, R2391, R2392, R2393, R2394, R2395, R2396, R2397, R2398, R2399, R2400, R2401, R2402, R2403, R2404, R2405, R2406, R2407, R2408, R2409, R2410, R2411, R2412, R2413, R2414, R2415, R2416, R2417, R2418, R2419, R2420, R2421, R2422, R2423, R2424, R2425, R2426, R2427, R2428, R2429, R2430, R2431, R2432, R2433, R2434, R2435, R2436, R2437, R2438, R2439, R2440, R2441, R2442, R2443, R2444, R2445, R2446, R2447, R2448, R2449, R2450, R2451, R2452, R2453, R2454, R2455, R2456, R2457, R2458, R2459, R2460, R2461, R2462, R2463, R2464, R2465, R2466, R2467, R2468, R2469, R2470, R2471, R2472, R2473, R2474, R2475, R2476, R2477, R2478, R2479, R2480, R2481, R2482, R2483, R2484, R2485, R2486, R2487, R2488, R2489, R2490, R2491, R2492, R2493, R2494, R2495, R2496, R2497, R2498, R2499, R2500, R2501, R2502, R2503, R2504, R2505, R2506, R2507, R2508, R2509, R2510, R2511, R2512, R2513, R2514, R2515, R2516, R2517, R2518, R2519, R2520, R2521, R2522, R2523, R2524, R2525, R2526, R2527, R2528, R2529, R2530, R2531, R2532, R2533, R2534, R2535, R2536, R2537, R2538, R2539, R2540, R2541, R2542, R2543, R2544, R2545, R2546, R2547, R2548, R2549, R2550, R2551, R2552, R2553, R2554, R2555, R2556, R2557, R2558, R2559, R2560, R2561, R2562, R2563, R2564, R2565, R2566, R2567, R2568, R2569, R2570, R2571, R2572, R2573, R2574, R2575, R2576, R2577, R2578, R2579, R2580, R2581, R2582, R2583, R2584, R2585, R2586, R2587, R2588, R2589, R2590, R2591, R2592, R2593, R2594, R2595, R2596, R2597, R2598, R2599, R2600, R2601, R2602, R2603, R2604, R2605, R2606, R2607, R2608, R2609, R2610, R2611, R2612, R2613, R2614, R2615, R2616, R2617, R2618, R2619, R2620, R2621, R2622, R2623, R2624, R2625, R2626, R2627, R2628, R2629, R2630, R2631, R2632, R2633, R2634, R2635, R2636, R2637, R2638, R2639, R2640, R2641, R2642, R2643, R2644, R2645, R2646, R2647, R2648, R2649, R2650, R2651, R2652, R2653, R2654, R2655, R2656, R2657, R2658, R2659, R2660, R2661, R2662, R2663, R2664, R2665, R2666, R2667, R2668, R2669, R2670, R2671, R2672, R2673, R2674, R2675, R2676, R2677, R2678, R2679, R2680, R2681, R2682, R2683, R2684, R2685, R2686, R2687, R2688, R2689, R2690, R2691, R2692, R2693, R2694, R2695, R2696, R2697, R2698, R2699, R2700, R2701, R2702, R2703, R2704, R2705, R2706, R2707, R2708, R2709, R2710, R2711, R2712, R2713, R2714, R2715, R2716, R2717, R2718, R2719, R2720, R2721, R2722, R2723, R2724, R2725, R2726, R2727, R2728, R2729, R2730, R2731, R2732, R2733, R2734, R2735, R2736, R2737, R2738, R2739, R2740, R2741, R2742, R2743, R2744, R2745, R2746, R2747, R2748, R2749, R2750, R2751, R2752, R2753, R2754, R2755, R2756, R2757, R2758

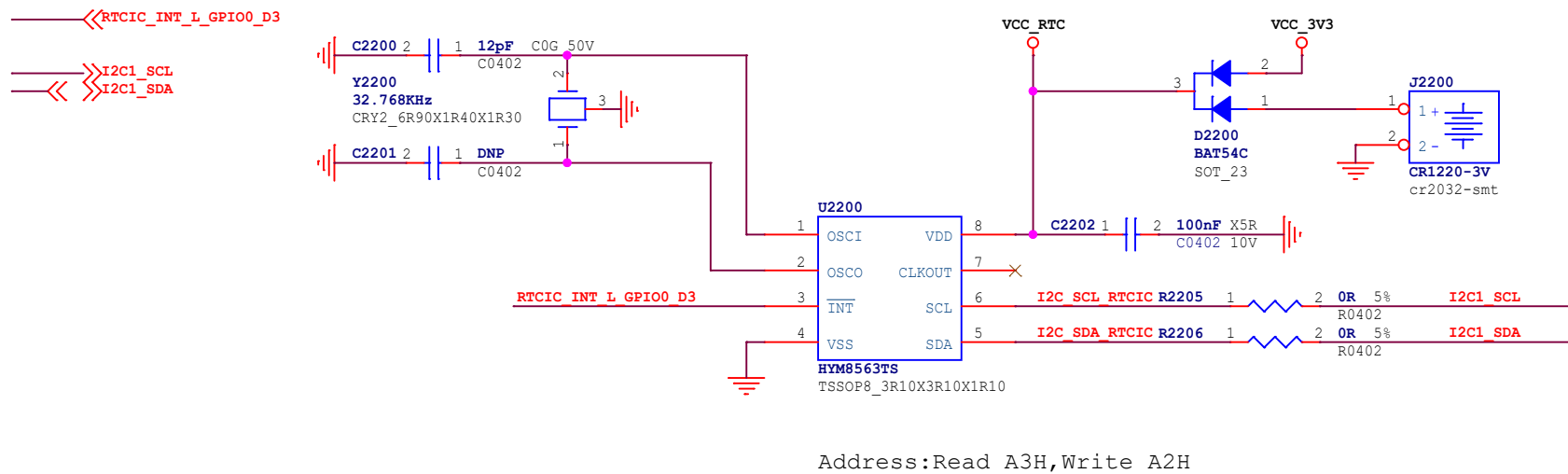
[illegible]

**Note:**  
If the external RTC IC is used,  
Can choose not mounted

The schematic diagram illustrates the internal circuitry of the QFN68\_7R00X7R00X0R80\_T module. Key components include the Y2100 crystal oscillator (32.768KHz) and the Gas Gauge IC. The module is powered by VCC3V3\_SYS and VCC\_RTC. The diagram shows the connections for various pins, including I2C0\_SDA\_PMIC, I2C0\_SCL\_PMIC, PMIC\_INT\_L, PMIC\_SLEEP\_H, RK809\_32KOUT\_WIFI, RK809\_CLK32KOUT, VCC3V3\_PMI, and VCC12V\_DCI. A note specifies that if an external RTC IC is used, the VCC\_RTC pin can be chosen not mounted.

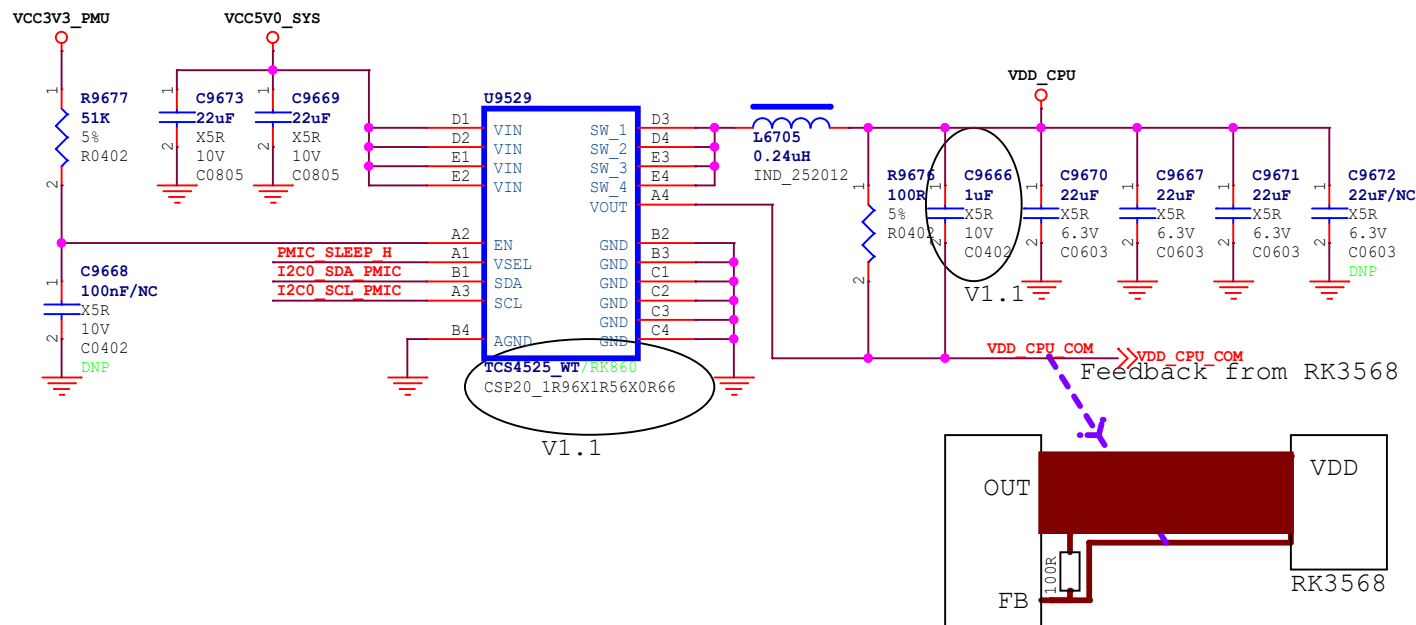
[illegible]

If RK809-5 codec is not used,  
then Pin 14,15,16,17,19,40 Tie VSS  
Pin 18,36,37,38,35,39,41,34,32,43,42  
Leave floating




## RTC IC

## VDD\_CPU



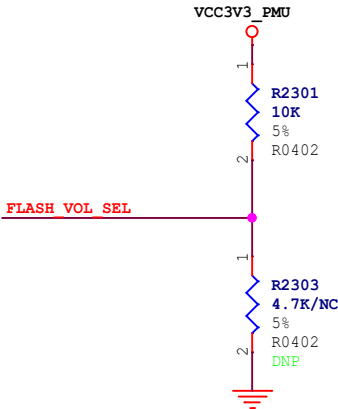
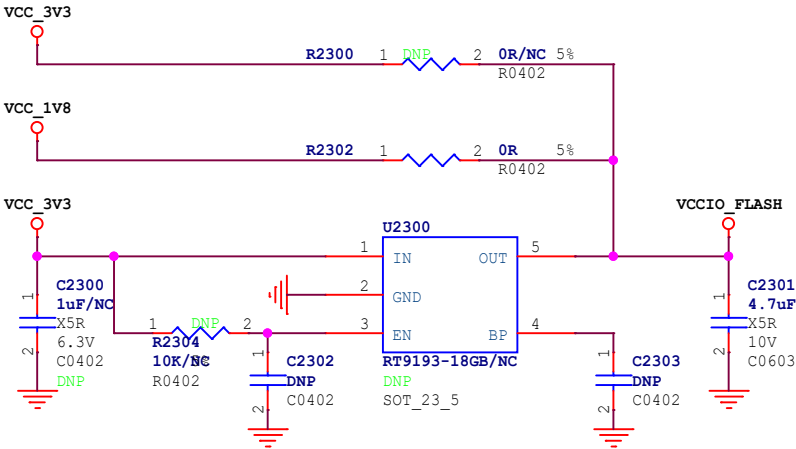
**Rockchip Confidential**

 瑞芯微电子		Rockchip Electronics Co., Ltd	
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4		
File:	A04.Power_other		
Date:	Friday, September 02, 2022		Rev: V1.2
Designed by:	Zhangdz	Reviewed by:	Default
		Sheet:	5 of 31

FLASH\_VOL\_SEL

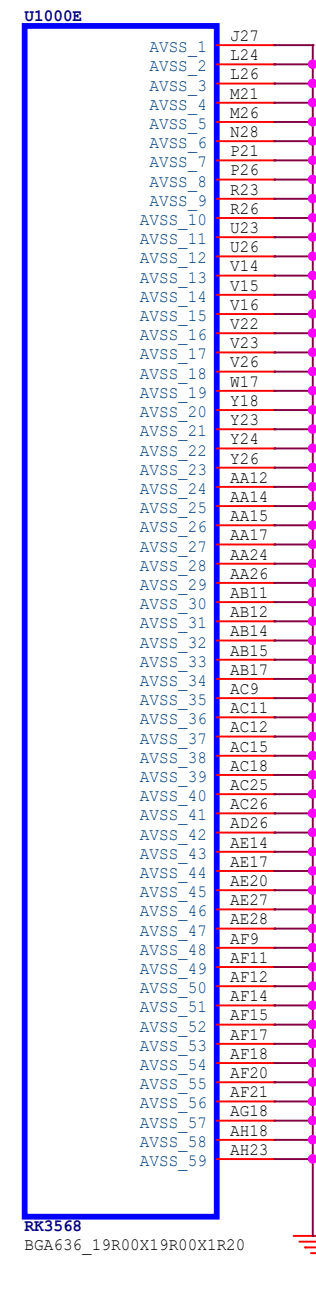
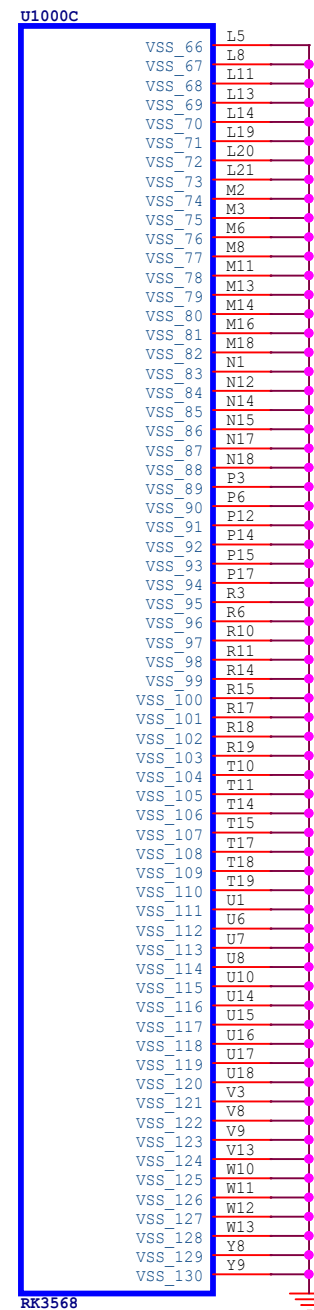
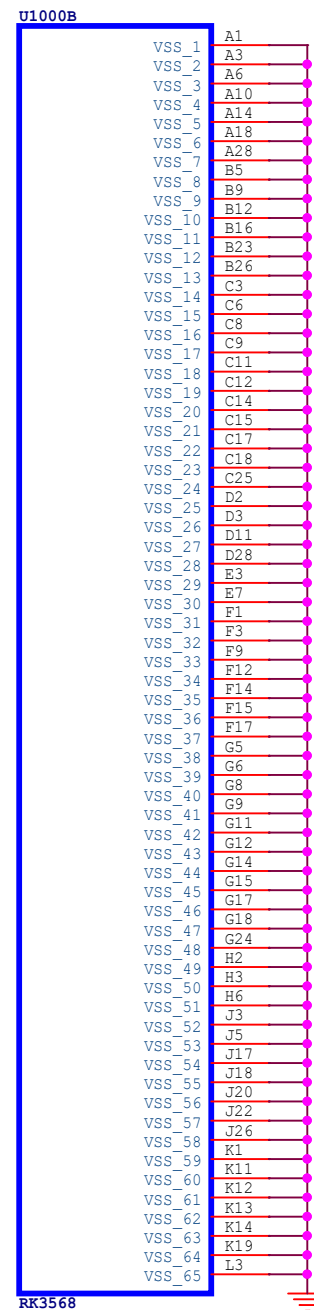
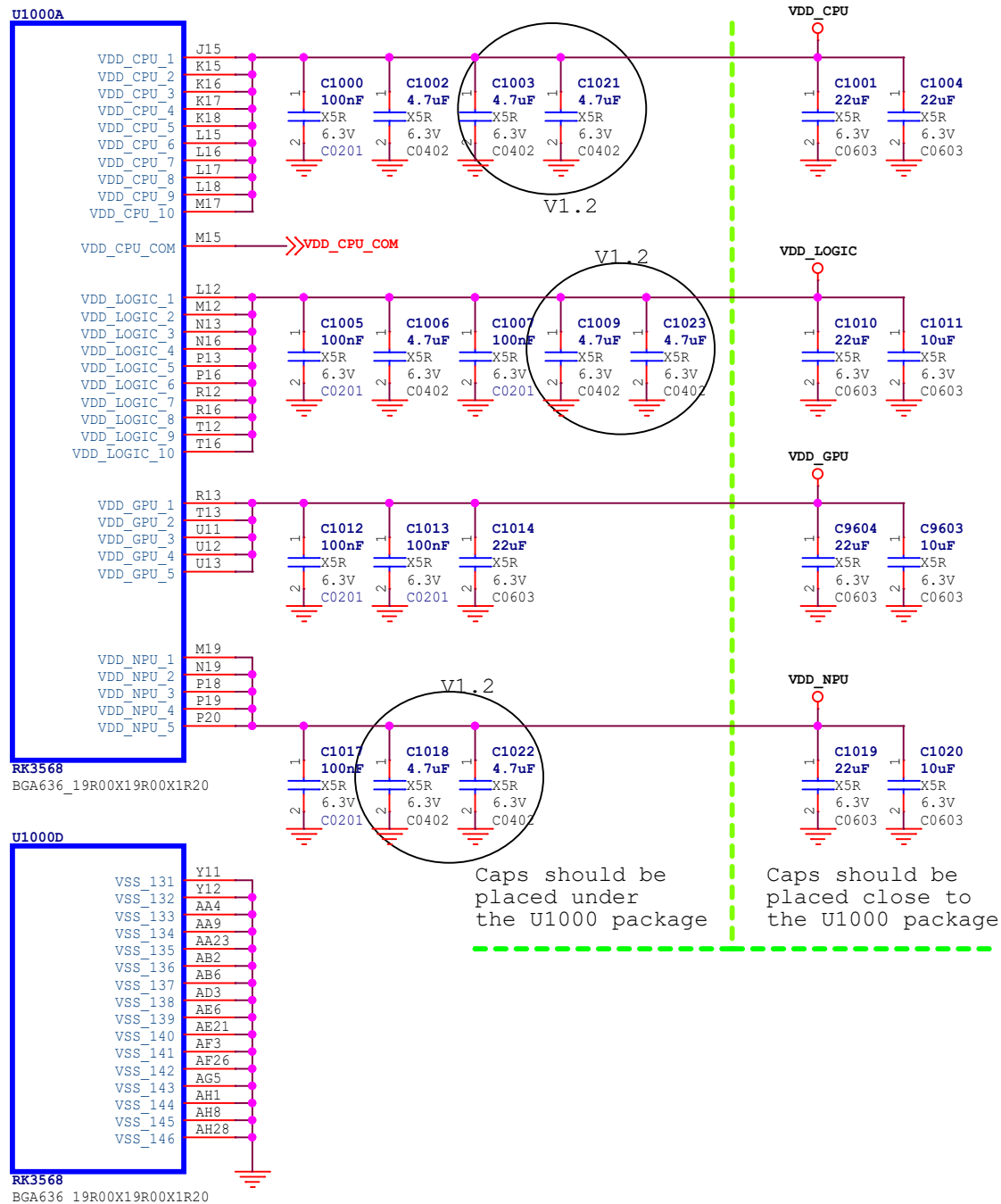
# Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)




Note:  
FLASH\_VOL\_SEL state decided  
to VCCIO2\_domain IO driven by default  
Logic=L: 3.3V IO driven  
Logic=H: 1.8V IO driven

# RK3568\_ABCDE (Power&Gnd)



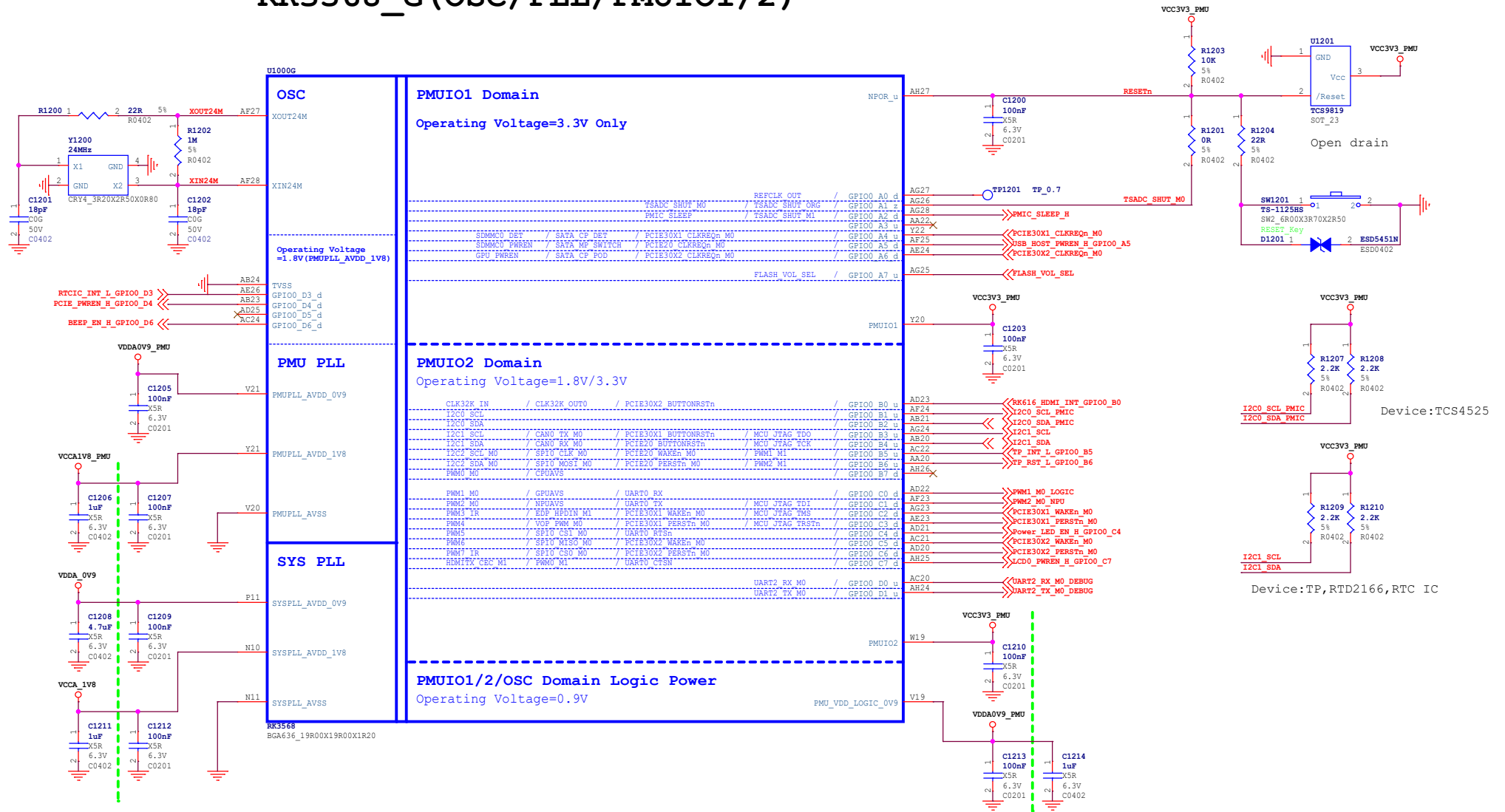
Rockchip Confidential

 瑞芯微电子		Rockchip Electronics Co., Ltd	
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4		
File:	B01.RK3568_Power/GND		
Date:	Monday, August 08, 2022		Rev: V1.2
Designed by:	Zhangdz	Reviewed by:	Default
		Sheet:	7 of 31

U1000F




# RK3568\_G (OSC/PLL/PMUIO1/2)



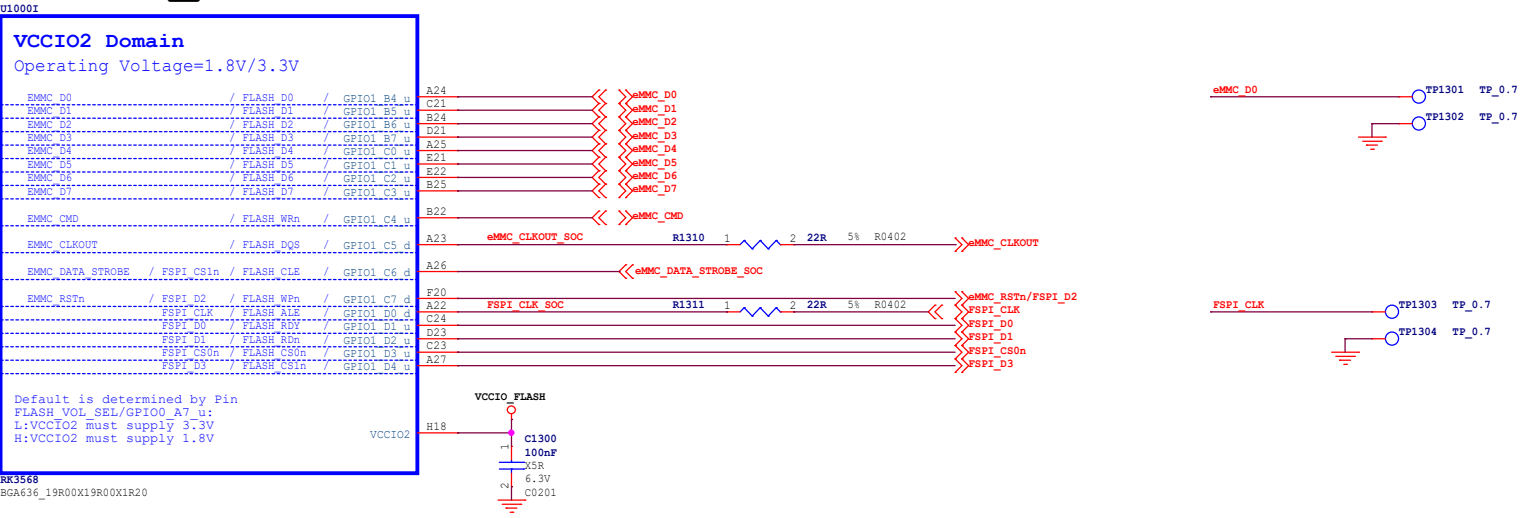
## Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

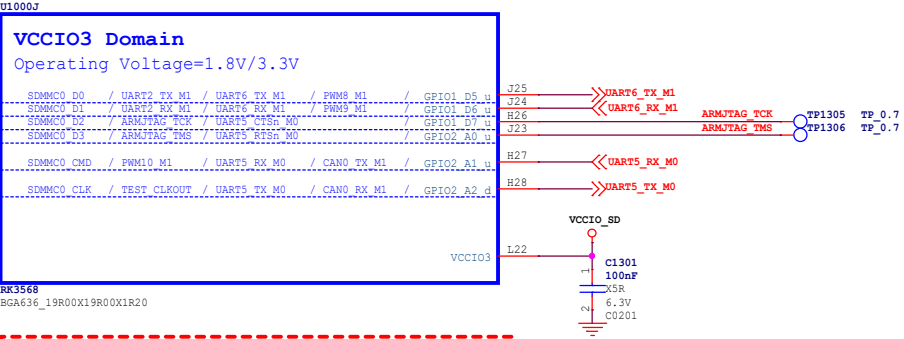
**Rockchip Confidential**

 瑞芯微电子		Rockchip Electronics Co., Ltd	
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4		
File:	B03.RK3568_OSC/PLL/PMUIO		
Date:	Monday, August 08, 2022		Rev: V1.2
Designed by:	Zhangtz	Reviewed by:	Default
Sheet:	9		of 31

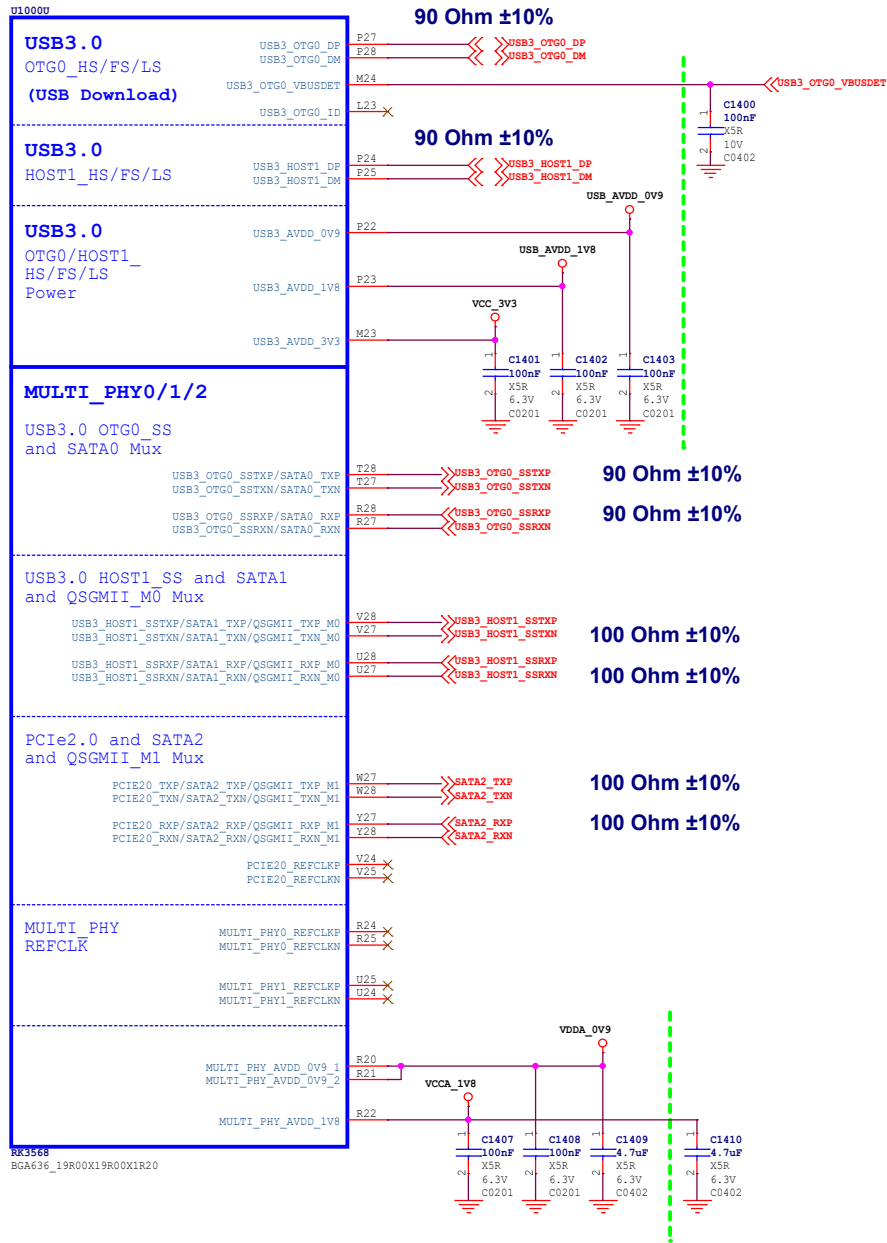
RK3568\_I (VCCIO2 Domain)



RK3568\_J (VCCIO3 Domain)



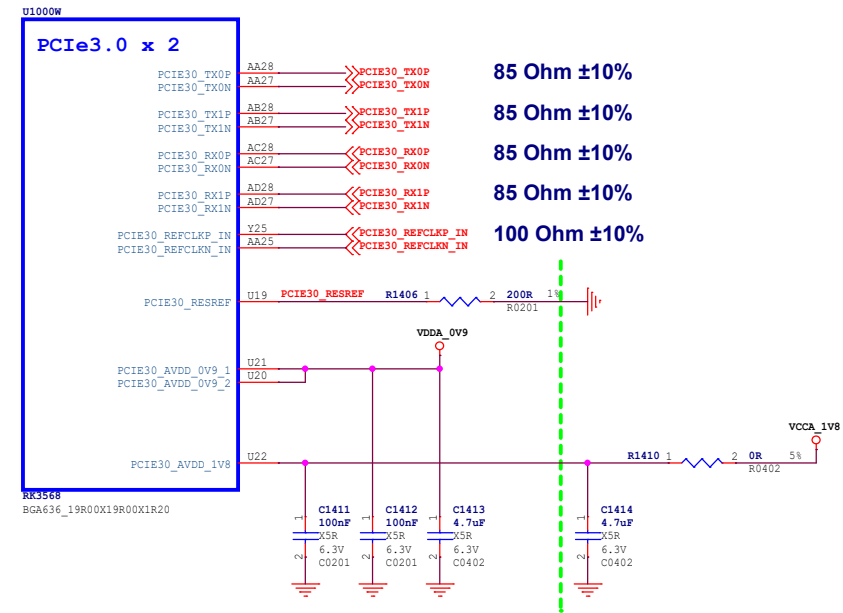
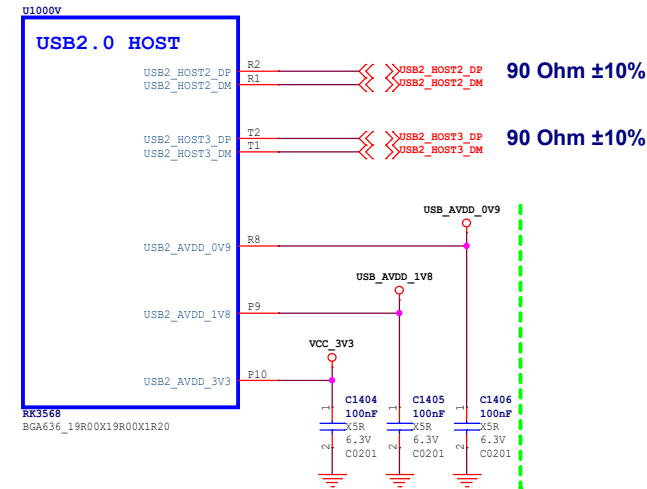
**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package



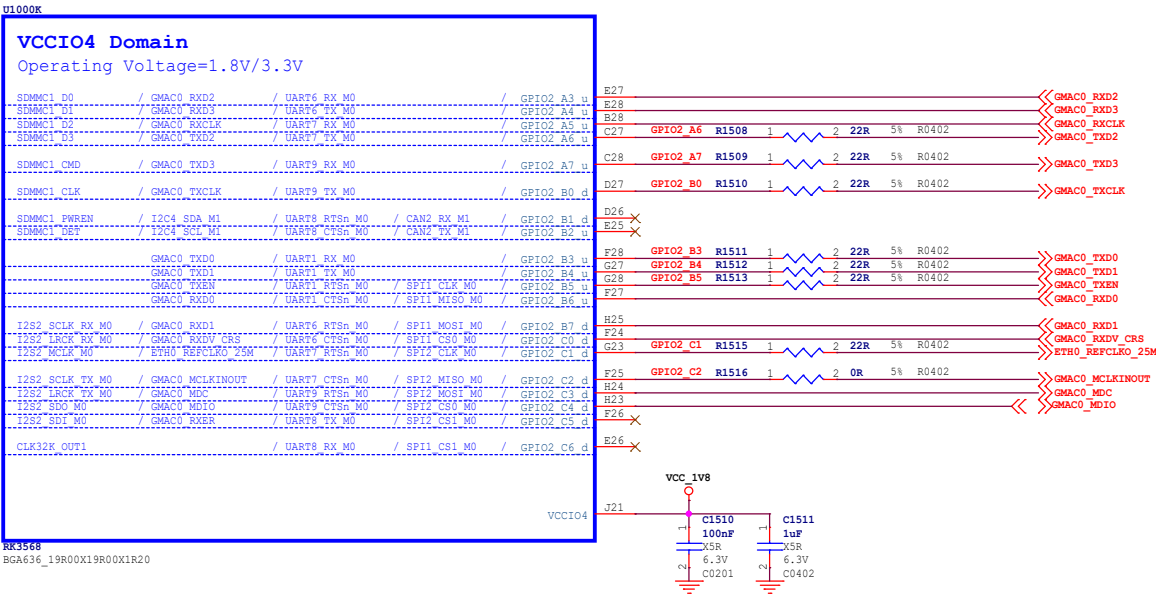
**Note:**

Caps of between dashed green lines and U1000  
should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

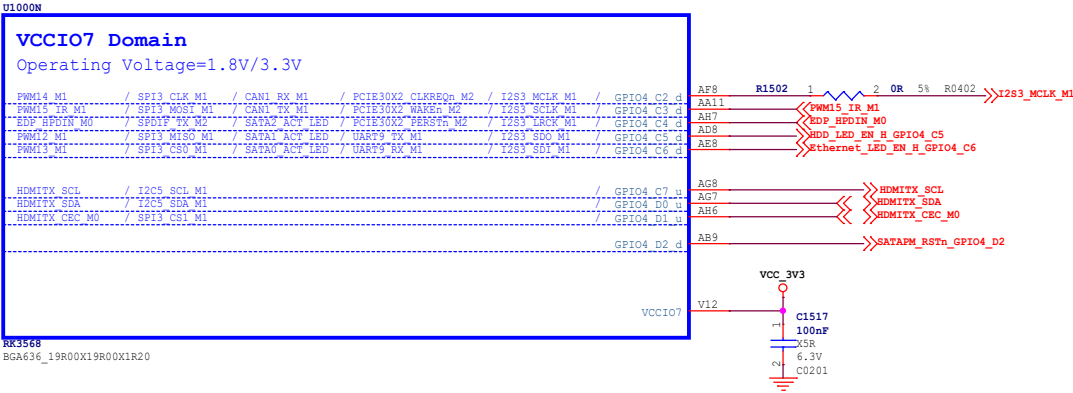
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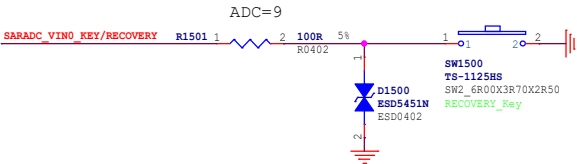
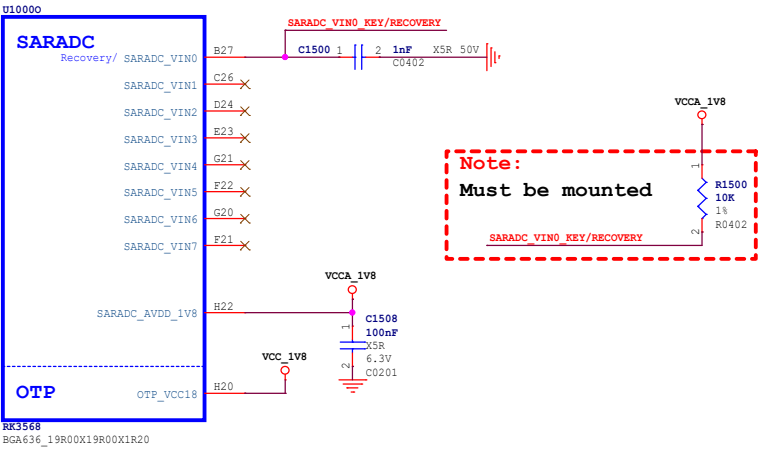
RK3568\_K (VCCIO4 Domain)



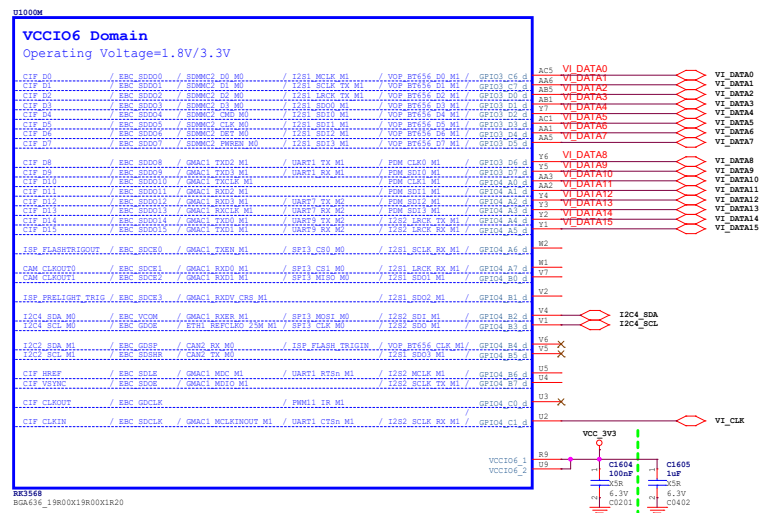
RK3568\_N (VCCIO7 Domain)



RK3568\_O (SARADC/OTP)



Note:  
Caps of between dashed green lines and U1000 should be placed under the U1000 package

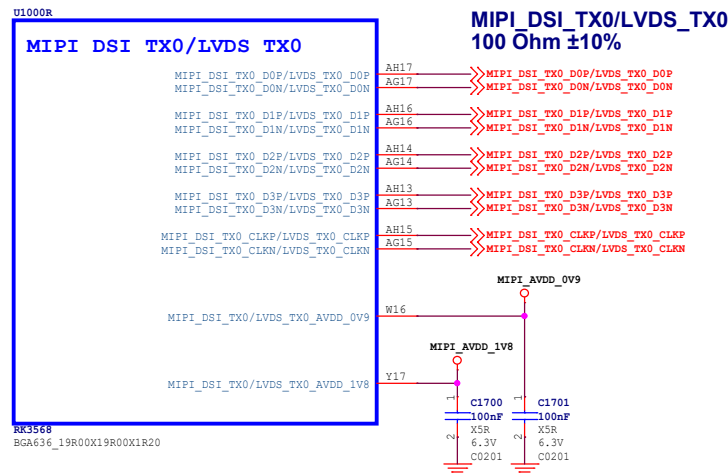


<b>Mode</b>	<b>16bit</b>	<b>12bit</b>	<b>10bit</b>	<b>8bit</b>
<i>CIF_D0</i>	<i>D0</i>	--	--	--
<i>CIF_D1</i>	<i>D1</i>	--	--	--
<i>CIF_D2</i>	<i>D2</i>	--	--	--
<i>CIF_D3</i>	<i>D3</i>	--	--	--
<i>CIF_D4</i>	<i>D4</i>	<i>D0</i>	--	--
<i>CIF_D5</i>	<i>D5</i>	<i>D1</i>	--	--
<i>CIF_D6</i>	<i>D6</i>	<i>D2</i>	<i>D0</i>	--
<i>CIF_D7</i>	<i>D7</i>	<i>D3</i>	<i>D1</i>	--
<i>CIF_D8</i>	<i>D8</i>	<i>D4</i>	<i>D2</i>	<i>D0</i>
<i>CIF_D9</i>	<i>D9</i>	<i>D5</i>	<i>D3</i>	<i>D1</i>
<i>CIF_D10</i>	<i>D10</i>	<i>D6</i>	<i>D4</i>	<i>D2</i>
<i>CIF_D11</i>	<i>D11</i>	<i>D7</i>	<i>D5</i>	<i>D3</i>
<i>CIF_D12</i>	<i>D12</i>	<i>D8</i>	<i>D6</i>	<i>D4</i>
<i>CIF_D13</i>	<i>D13</i>	<i>D9</i>	<i>D7</i>	<i>D5</i>
<i>CIF_D14</i>	<i>D14</i>	<i>D10</i>	<i>D8</i>	<i>D6</i>
<i>CIF_D15</i>	<i>D15</i>	<i>D11</i>	<i>D9</i>	<i>D7</i>

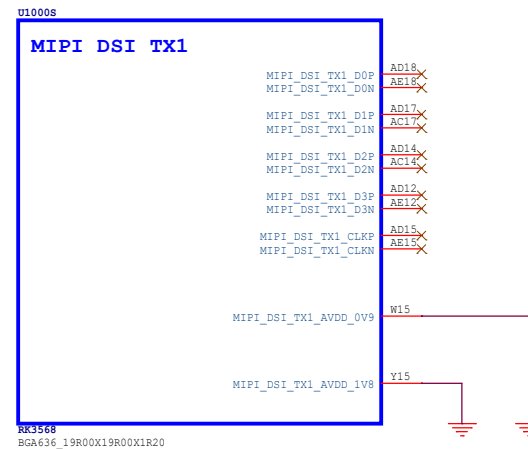
**Note:**  
Caps of between dashed green lines and U1000  
should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

AIC31\_EN

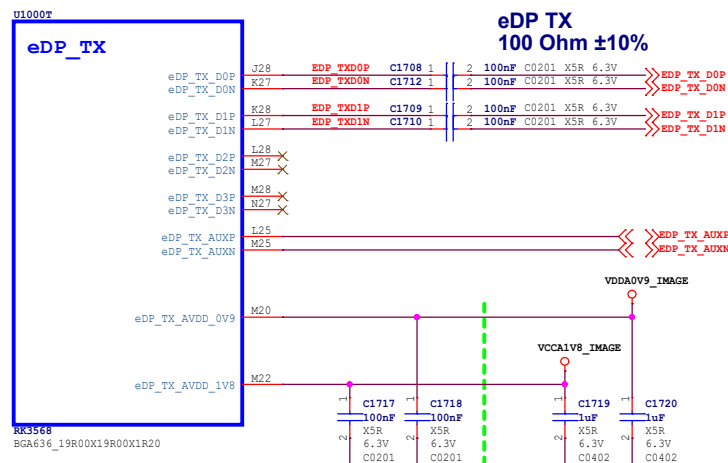
# RK3568\_R(MIPI\_DSI\_TX0/LVDS\_TX0)



# RK3568\_S(MIPI\_DSI\_TX1)



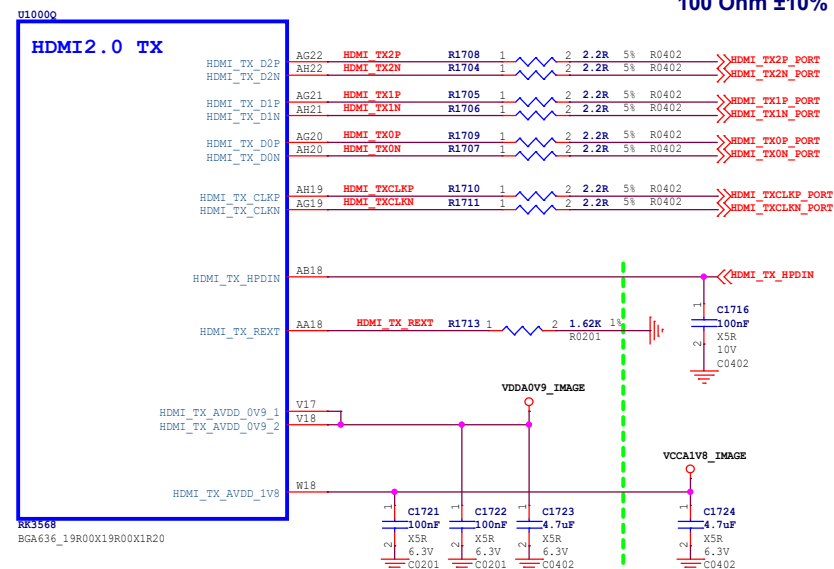
# RK3568\_T(eDP\_TX)



**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

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# RK3568\_Q(HDMI2.0\_TX)

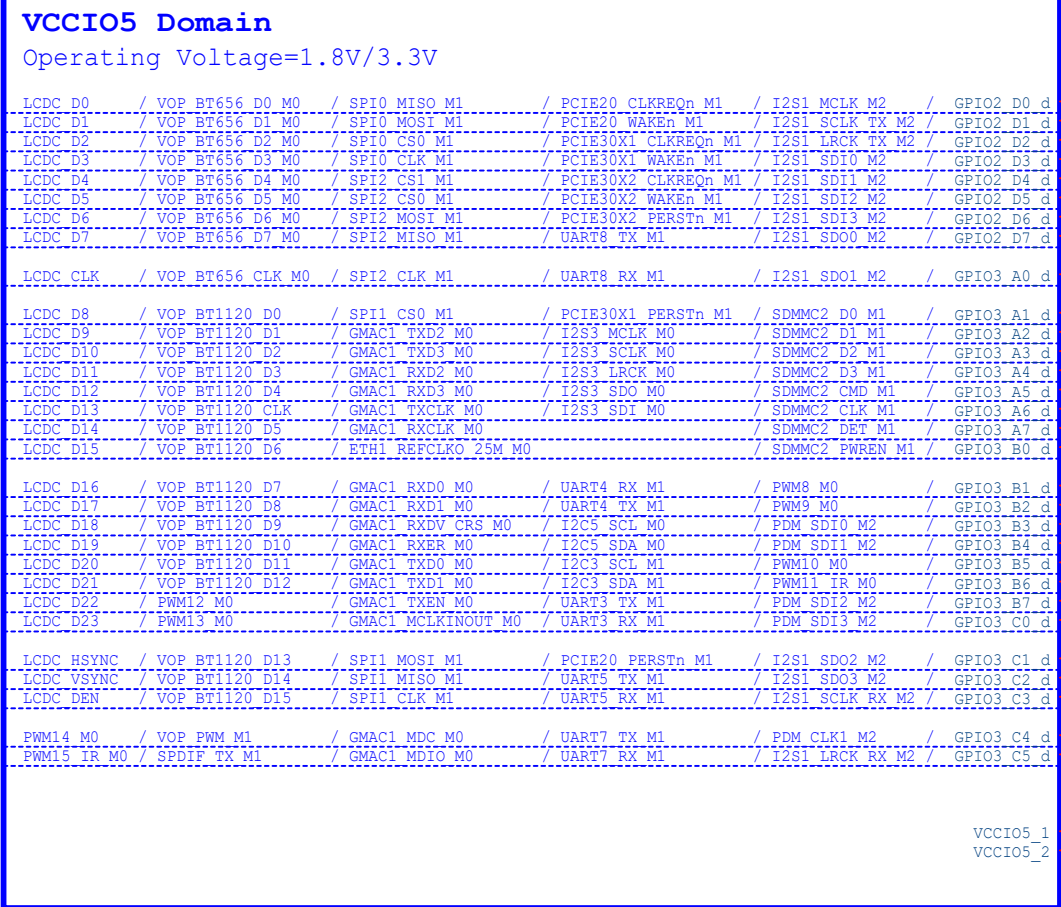


**HDMI TMDs trace**  
100 Ohm ±10%

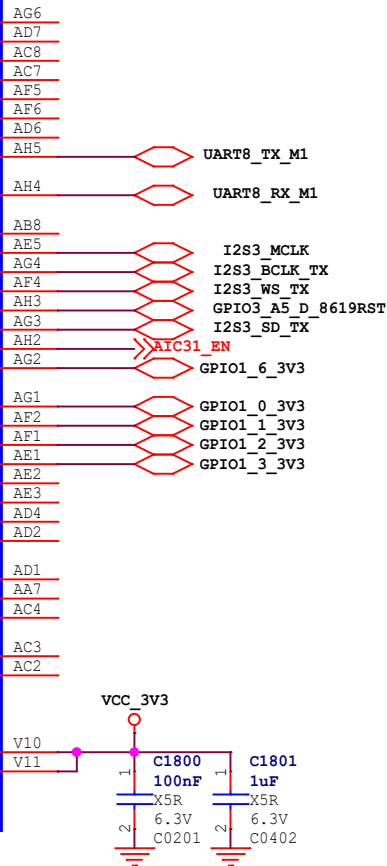
<b>Rockchip</b> 瑞芯微电子			
Rockchip Electronics Co., Ltd			
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4		
File:	B08.RK3568_VO Interface_1		
Date:	Monday, August 08, 2022	Rev:	V1.2
Designed by:	Zhangtz	Reviewed by:	Default
Sheet:	14	of	31

# RK3568\_L (VCCIO5 Domain)

U1000L




RK3568  
BGA636\_19R00X19R00X1R20



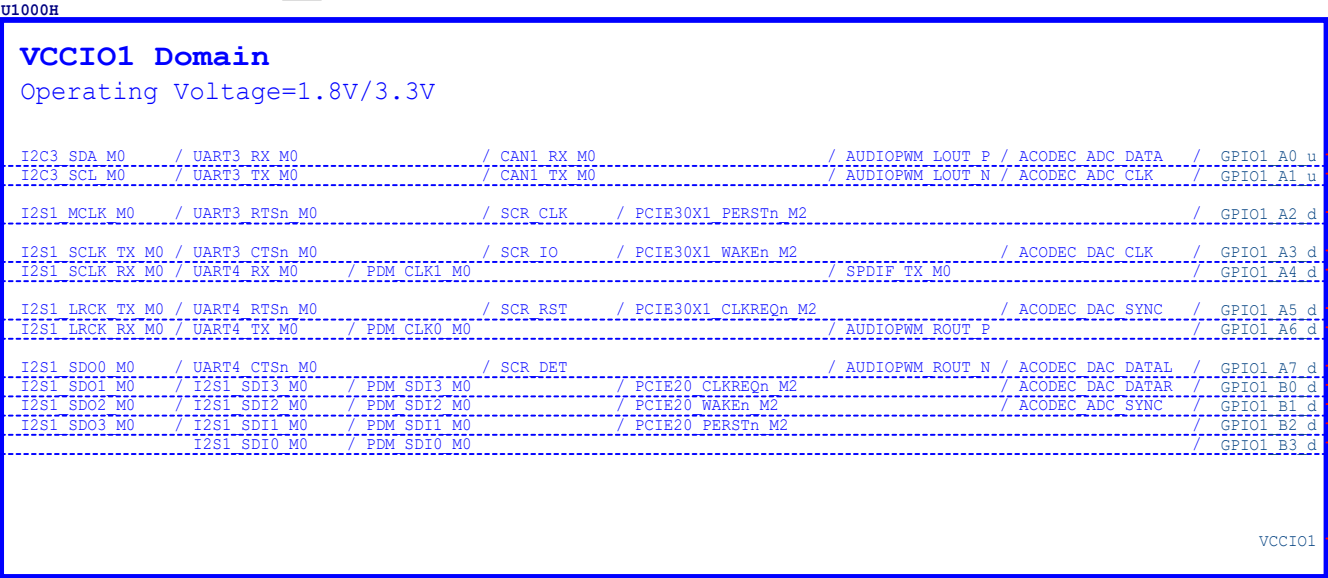
**Note:**

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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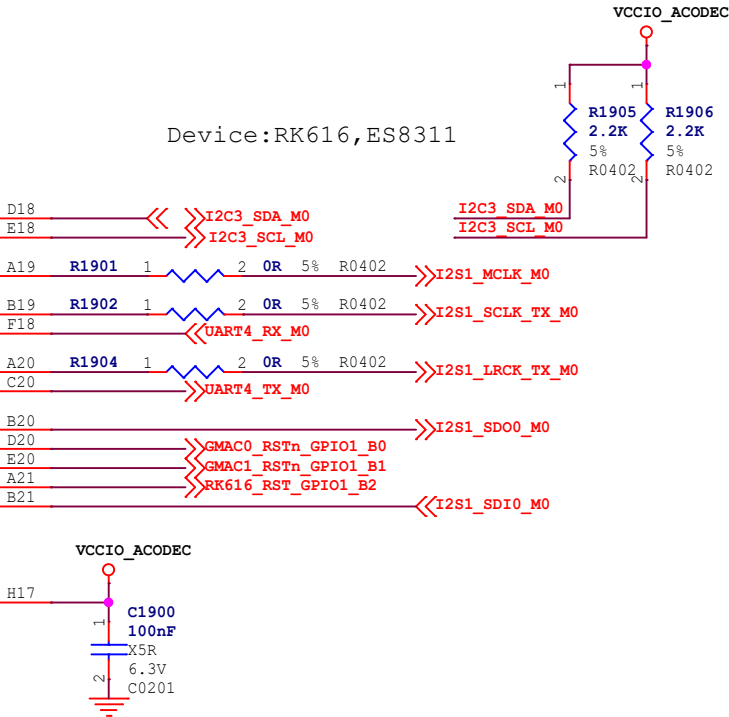
 瑞芯微电子		Rockchip Electronics Co., Ltd			
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	B09.RK3568_VO Interface_2				
Date:	Monday, August 08, 2022			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	15 of 31

# RK3568\_H(VCCIO1 Domain)



RK3568  
BGA636\_19R00X19R00X1R20


Device:RK616,ES8311



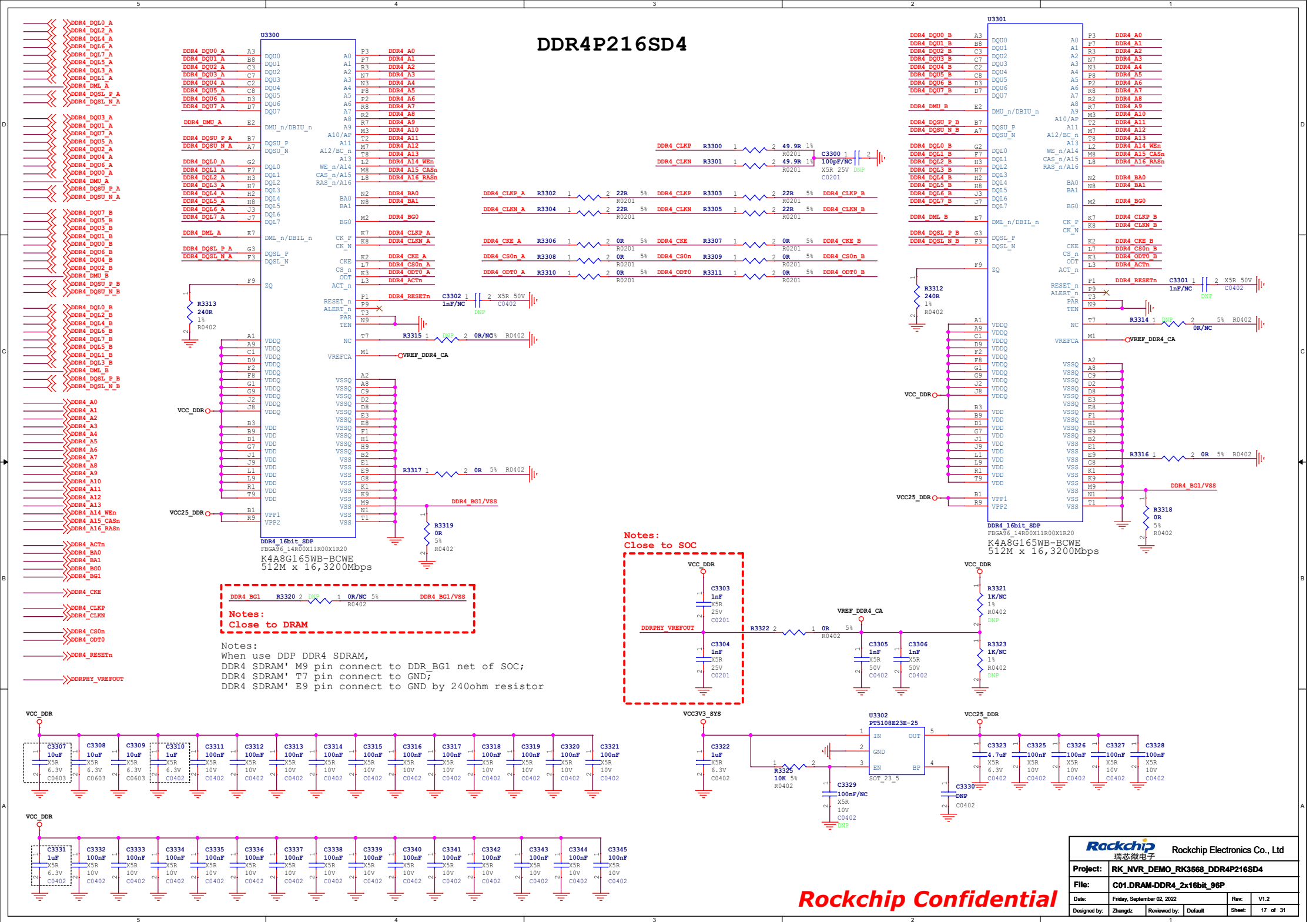
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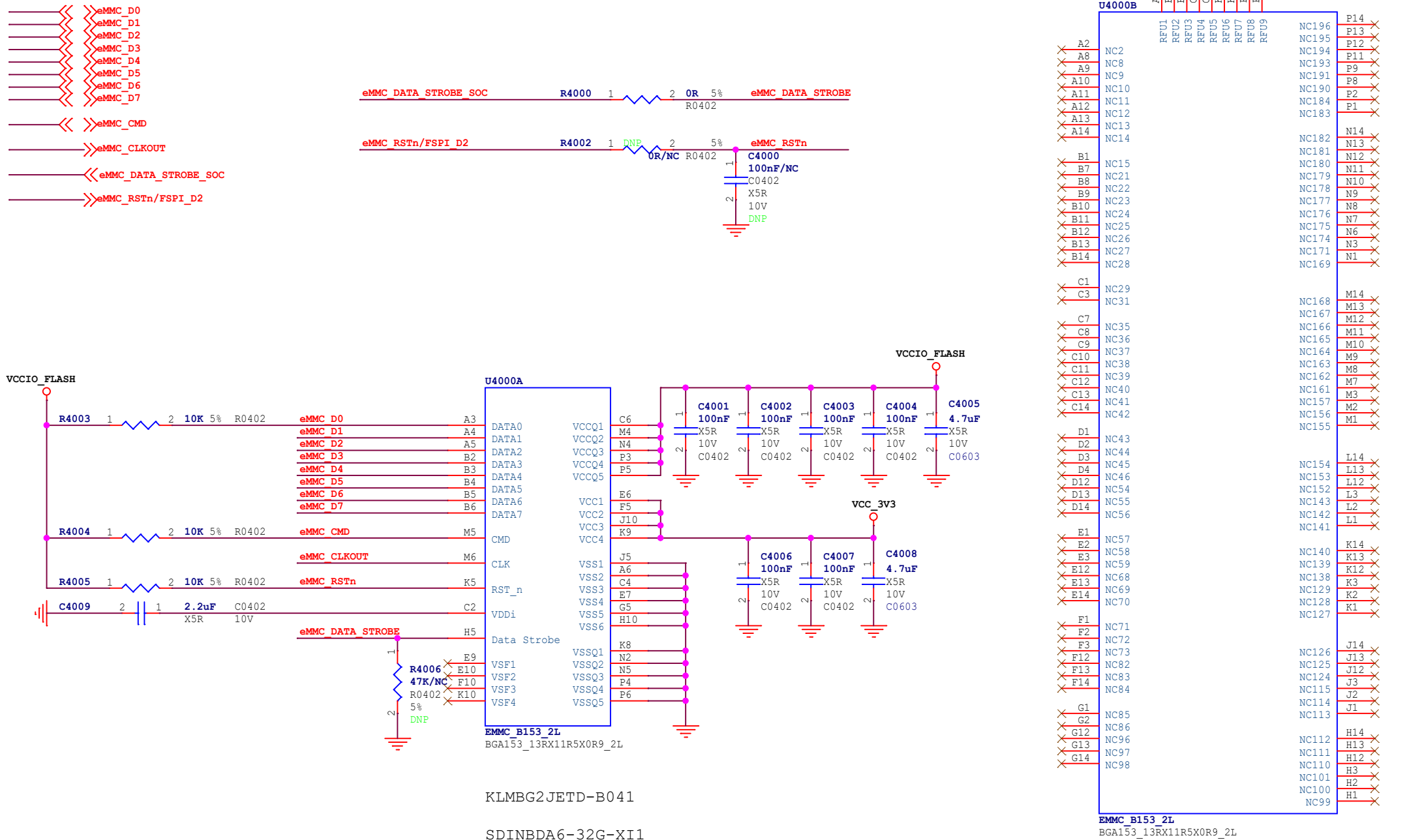
Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

 瑞芯微电子		Rockchip Electronics Co., Ltd	
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4		
File:	B10.RK3568_Audio Interface		
Date:	Monday, August 08, 2022		Rev: V1.2
Designed by:	Zhangdz	Reviewed by: Default	Sheet: 16 of 31







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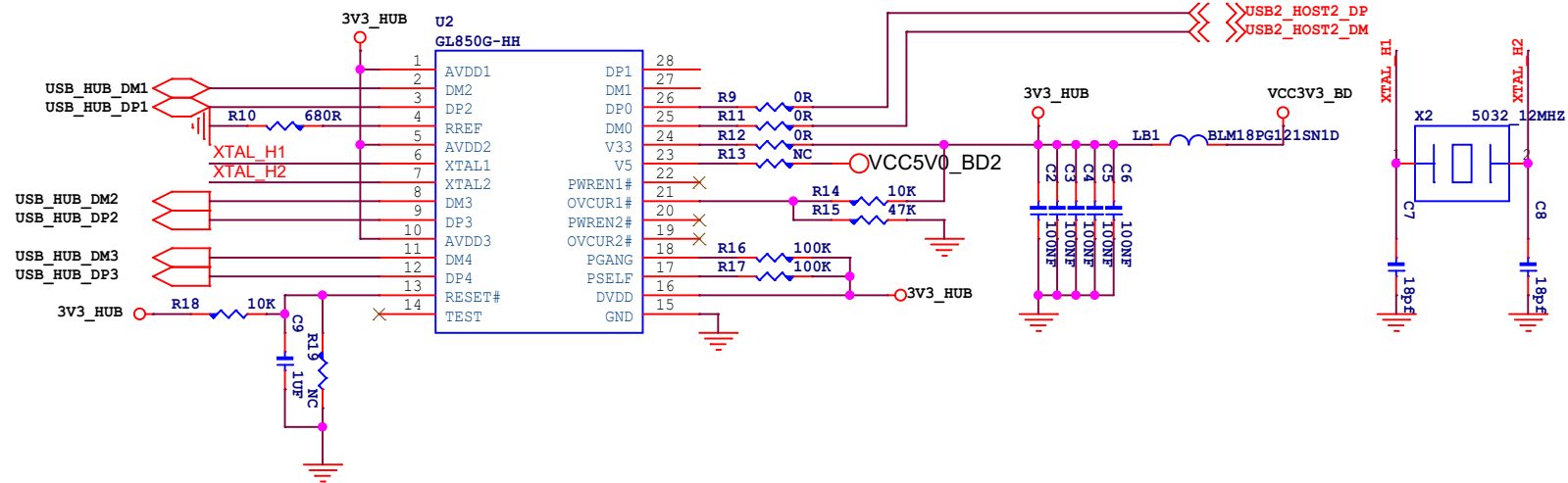
<div>Rockchip</div> <div>瑞芯微电子</div> <div>Rockchip Electronics Co., Ltd</div>			
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4		
File:	C02.Flash-eMMC Flash		
Date:	Friday, September 02, 2022	Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default
Sheet:	18	of	31






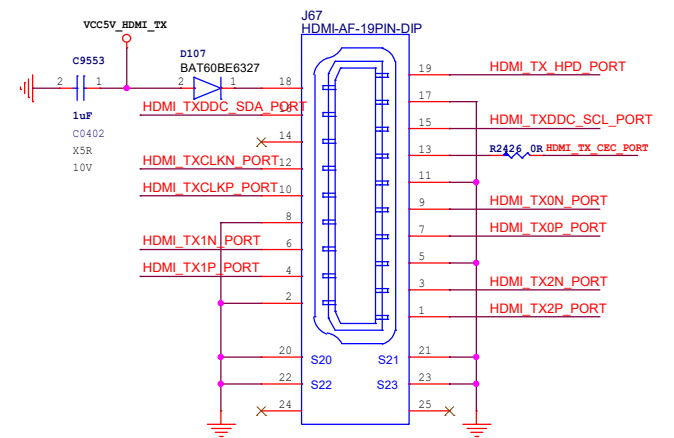
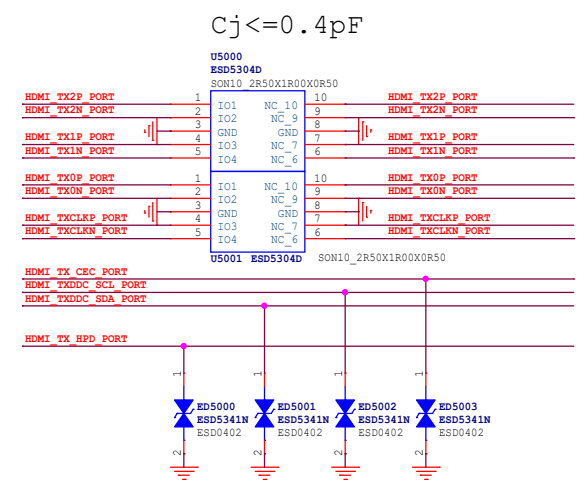
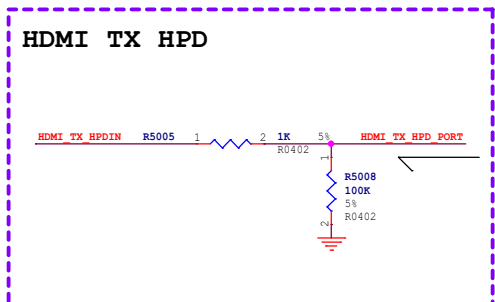
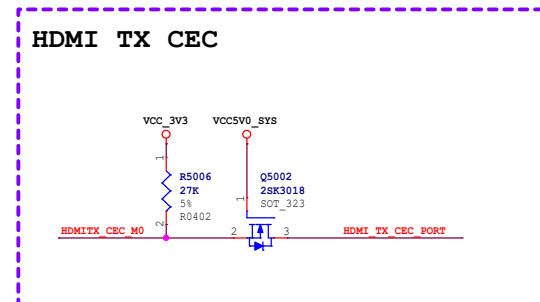
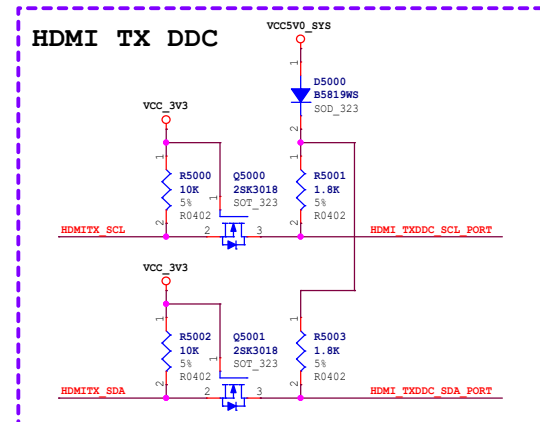
# USB HUB

The USB differential trace impedance is 90 OHM.  
The USB2.0 trace length is less than 8 inch.  
The USB3.0 trace length is less than 5 inch.

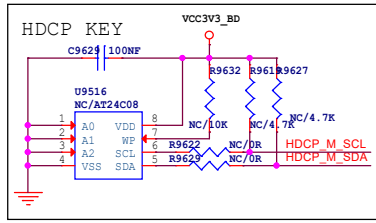
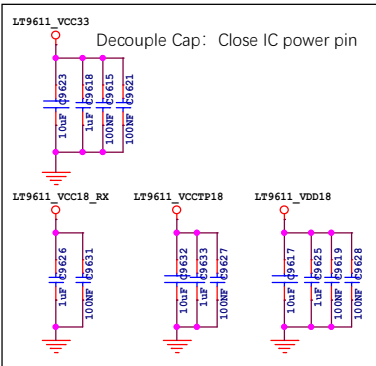
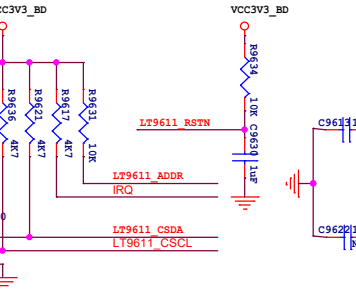
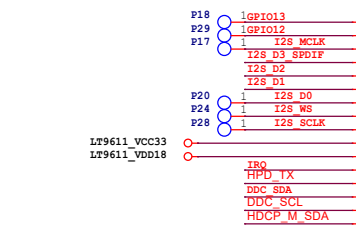
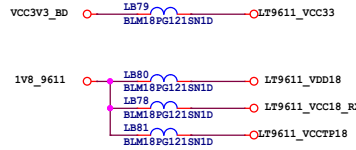
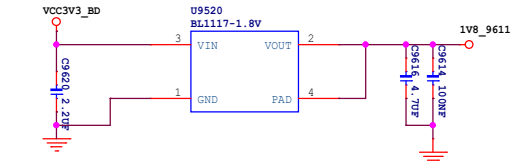


 瑞芯微电子		Rockchip Electronics Co., Ltd	
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4		
File:	D02.USB-HUB		
Date:	Monday, August 08, 2022		Rev: V1.2
Designed by:	Zhangdz	Reviewed by: Default	Sheet: 21 of 31

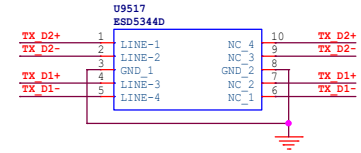
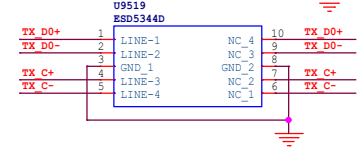
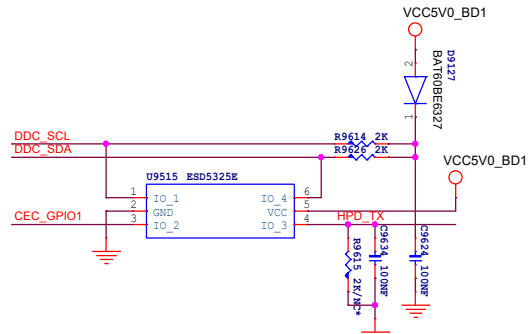
>>HDMI\_TX2P\_PORT  
>>HDMI\_TX2N\_PORT  
  
>>HDMI\_TX1P\_PORT  
>>HDMI\_TX1N\_PORT  
  
>>HDMI\_TX0P\_PORT  
>>HDMI\_TX0N\_PORT  
  
>>HDMI\_TXCLKP\_PORT  
>>HDMI\_TXCLKN\_PORT  
  
>>HDMI\_TX\_SCL  
>>HDMI\_TX\_SDA  
  
>>HDMI\_TX\_CEC\_M0  
>>HDMI\_TX\_HPDIN



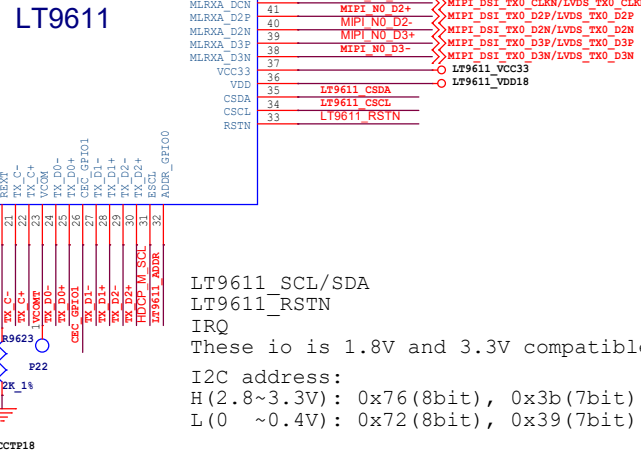
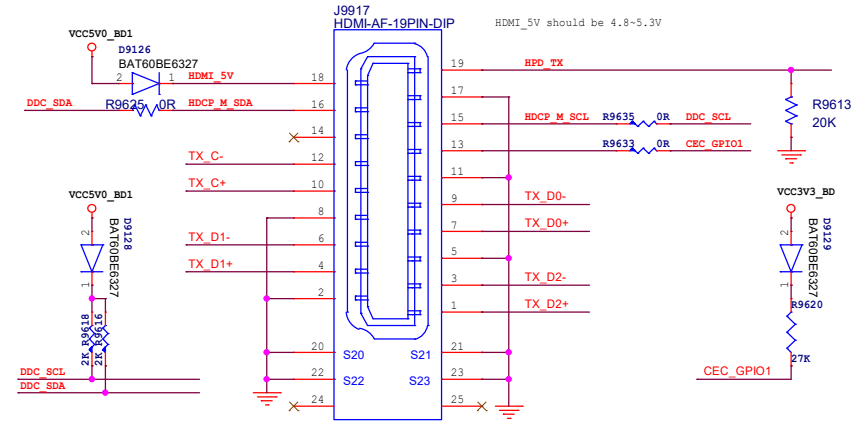
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HDMI信号阻抗控制在100欧姆  
HDMI信号以CLK作参考做等长  
MIPI信号阻抗控制在100欧姆  
MIPI信号以CLK作参考做等长  
MIPI信号长度限制3Inch



## HDMI OUT



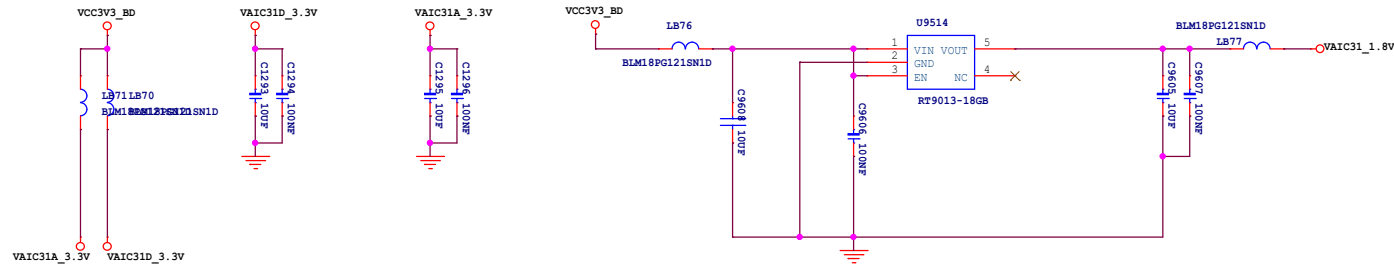
LT9611\_SCL/SDA  
LT9611\_RSTN  
IRQ  
These io is 1.8V and 3.3V compatible.  
I2C address:  
H(2.8~3.3V): 0x76(8bit), 0x3b(7bit)  
L(0 ~0.4V): 0x72(8bit), 0x39(7bit)



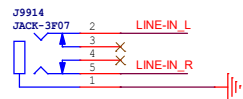


I2S1\_MCLK\_M0  
I2S1\_SCLK\_TX\_M0  
I2S1\_LRCK\_TX\_M0  
I2S1\_SDO0\_M0  
I2S1\_SDI0\_M0  
I2C3\_SDA\_M0  
I2C3\_SCL\_M0  
AIC31\_EN

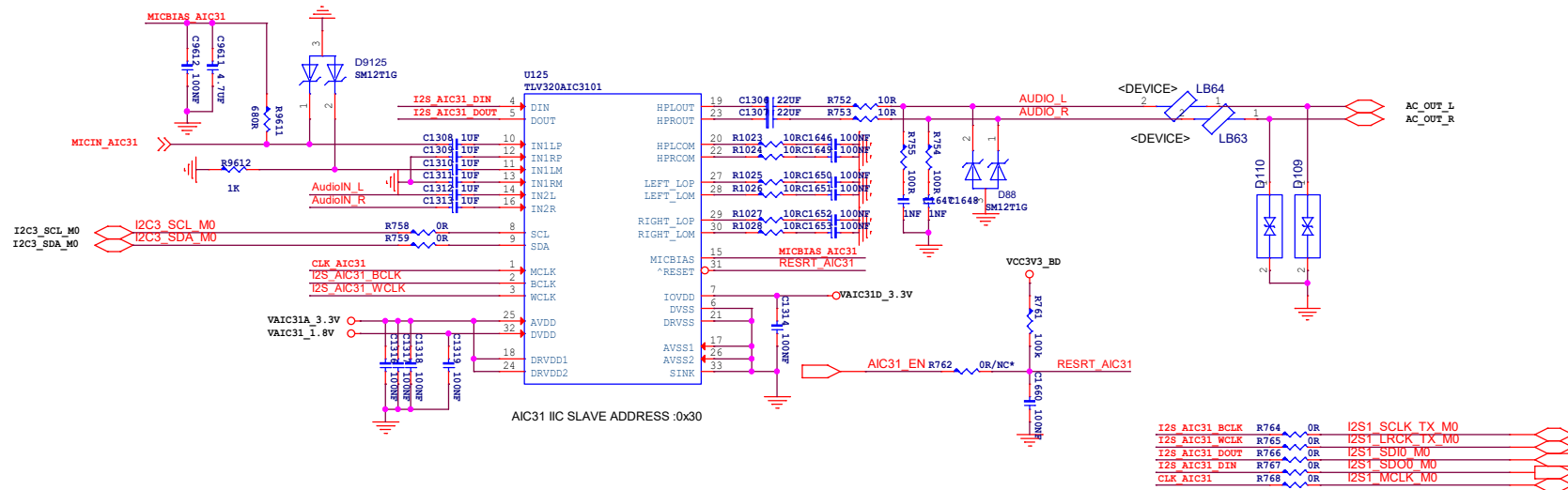
## Power

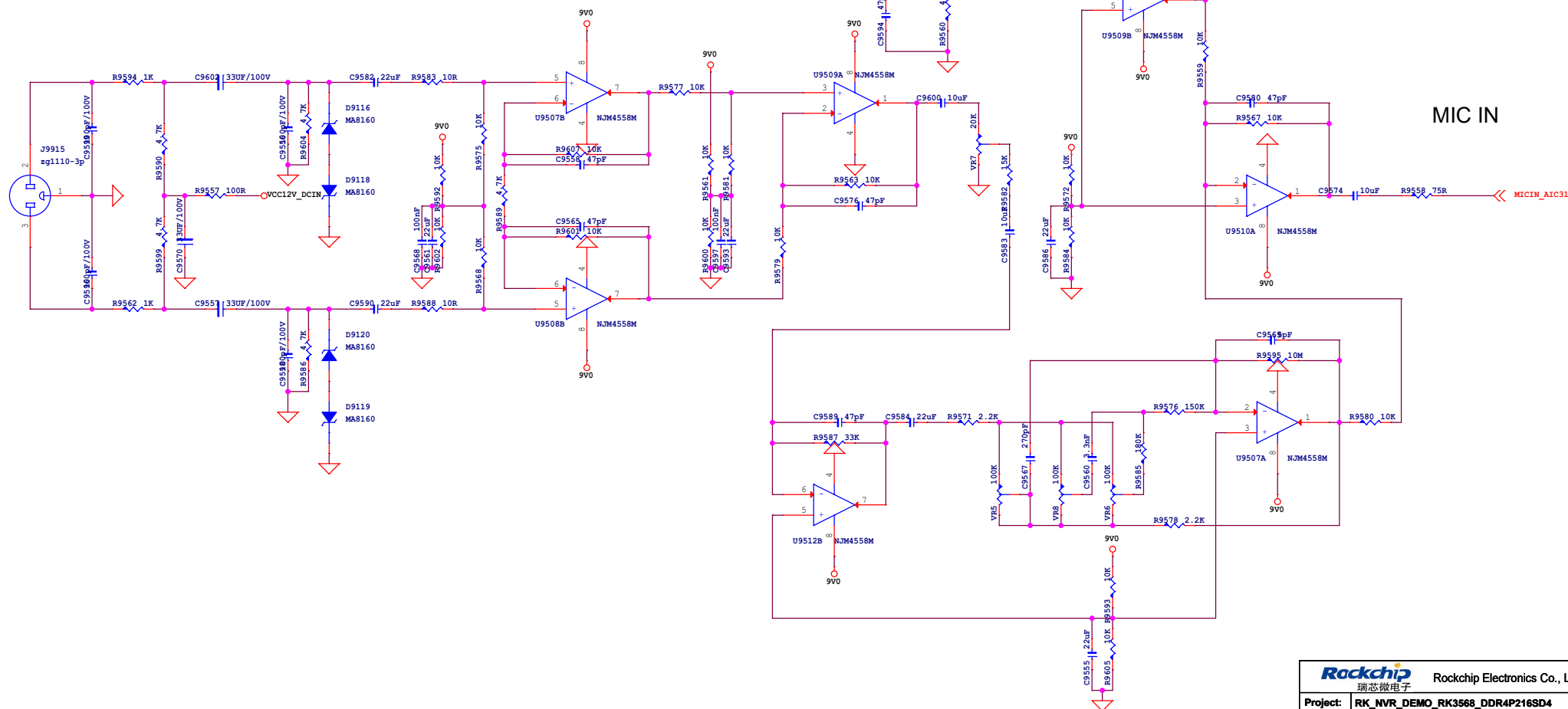
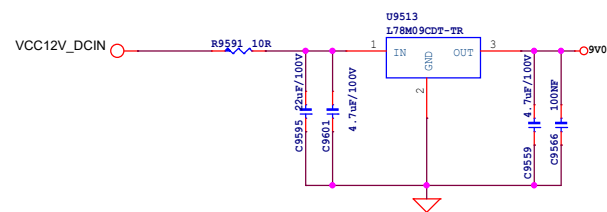


## Audio Input



## Audio Output

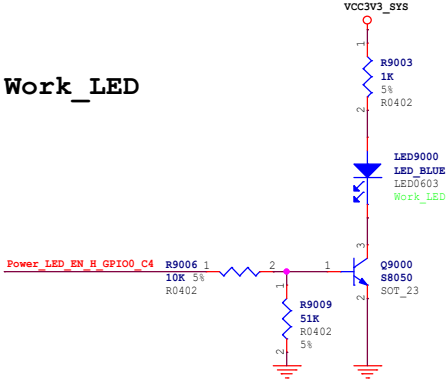




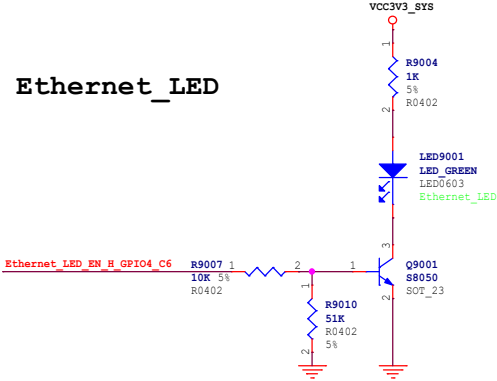


<<Pwm15\_IR\_M1  
>>Power\_LED\_EN\_H\_GPIO0\_C4  
>>Ethernet\_LED\_EN\_H\_GPIO4\_C6  
>>HDD\_LED\_EN\_H\_GPIO4\_C5

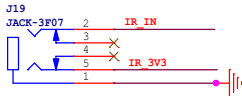
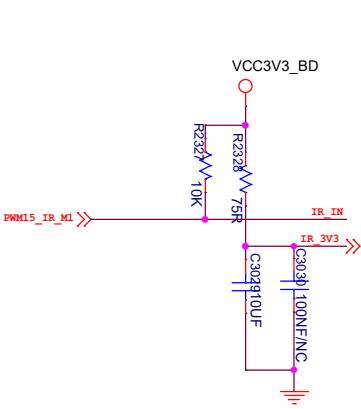
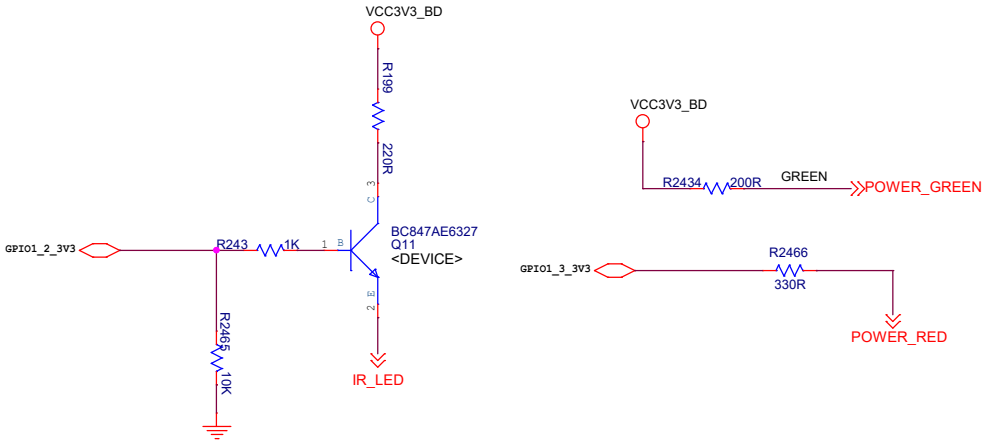
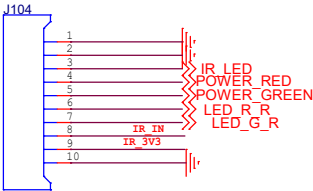
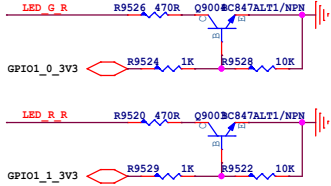
Work\_LED



Ethernet\_LED

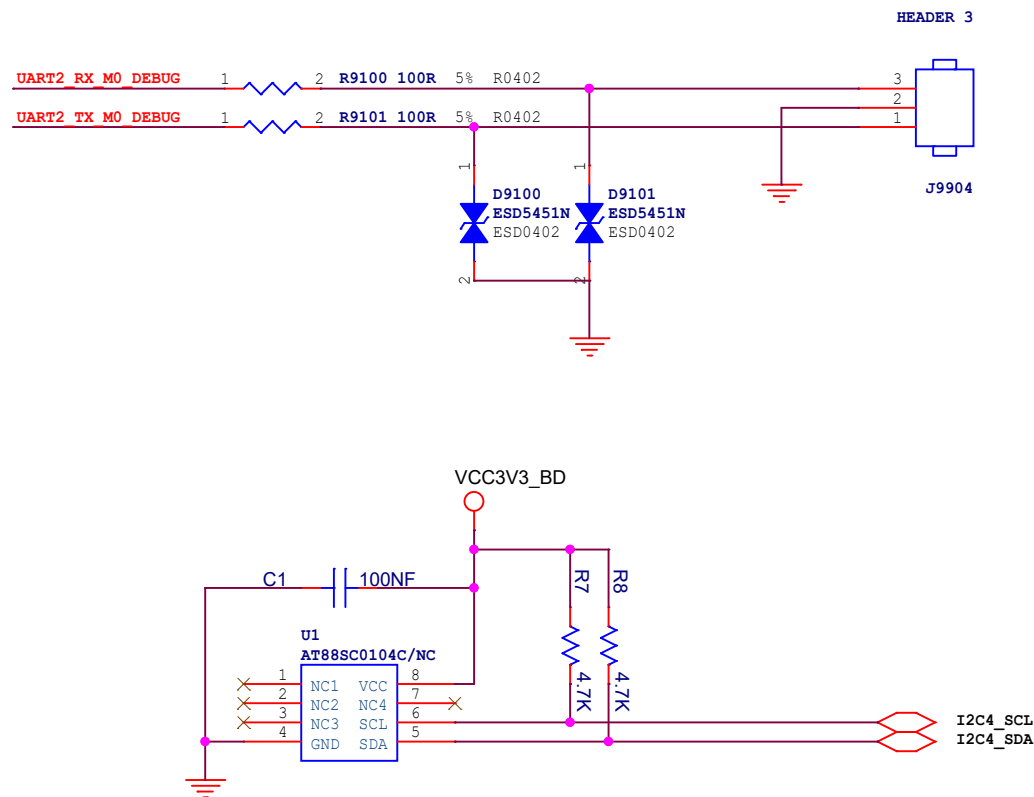


IR



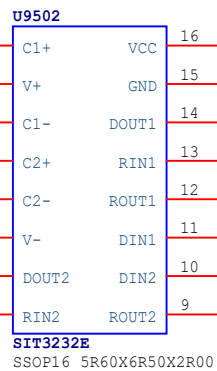
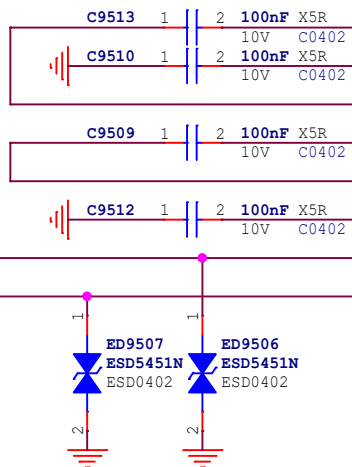
UART2\_RX\_M0\_DEBUG  
UART2\_TX\_M0\_DEBUG

# Debug UART2

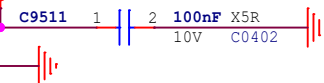


UART4\_TX\_M0  
UART4\_RX\_M0

J9909  
PH-3P



VCC3V3\_BD



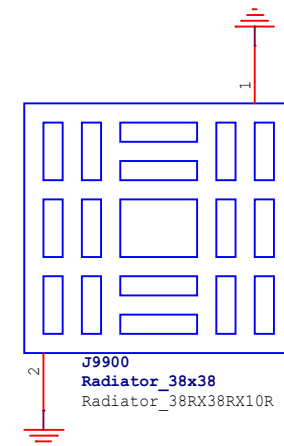
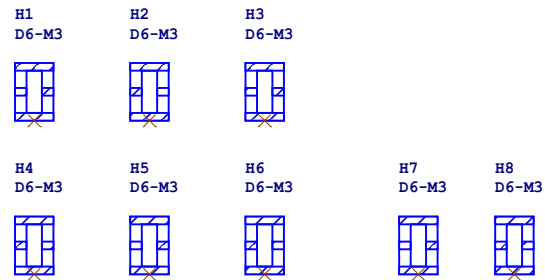
UART4\_TX\_M0  
UART4\_RX\_M0

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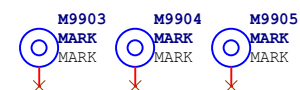
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4			
File:	D11.TTL_UART4			
Date:	Monday, August 15, 2022		Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet: 30 of 31



TOP Mark



BOTTOM Mark



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 瑞芯微电子		Rockchip Electronics Co., Ltd	
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4		
File:	D12.Mark/Hole/Heatsink		
Date:	Monday, August 15, 2022		Rev: V1.2
Designed by:	Zhangdz	Reviewed by:	Default
Sheet:		31 of 31	