Reference Schematics For RK3588

RK3588_AIOT_REF_SCH_V12

Main Functions Introduction

1) PMIC: 1xRK806-1+DiscretePower
2) RAM: 2xLPDDR4/4X_32bit or 2xLPDDR5_32bit
3) ROM: eMMC5.1(Default) or SPI Flash
4) Support: 1xSDMMC3.0 Card
5) Support: 1 x TYPEC3.0(With DP TX)+1 x USB3.0 HOST+ 1 x USB20 HOST or USB3.0/2.0 HUB
6) Support: 3 x SATA3.0 Connector (7pin) or SATA PM
7) Support: 1 x 4Lane PCIe3.0 Connector (Dual Mode)
8) Support: 2 x 4Lanes MIPI DPHY RX Camera
9) Support: 2 x 4Lanes MIPI D/CPHY RX Camera
10) Support: 1 x HDMI2.0 RX or HDMI IN to mipi
11) Support: 2 x HDMI2.1 TX or 2 x eDP1.3 TX
12) Support: 2 x 4Lanes MIPI D/CHY-TX
13) Support: 1xVGA Connector(DP to VGA)
14) Support: 1x4Lanes DP Port
15) Support: a/b/g/n/ac/ax 2T2R WIFI 6/5(PCIE/SDIO) +BT5.0
16) Support: 1x 10/100/1000 RJ45 Port(RGMII)
17) Support: 1x 10/100/1000 RJ45 Port(PCIE)
18) Support: 4G Module
19) Support: PCIE M.2
20) Support: 1xHeadphone+2xSPK+1xAnalog MIC

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Note

The power suffix S0 or S3 means:

S3: Keep power On during sleeping

S0:Power off during sleeping

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

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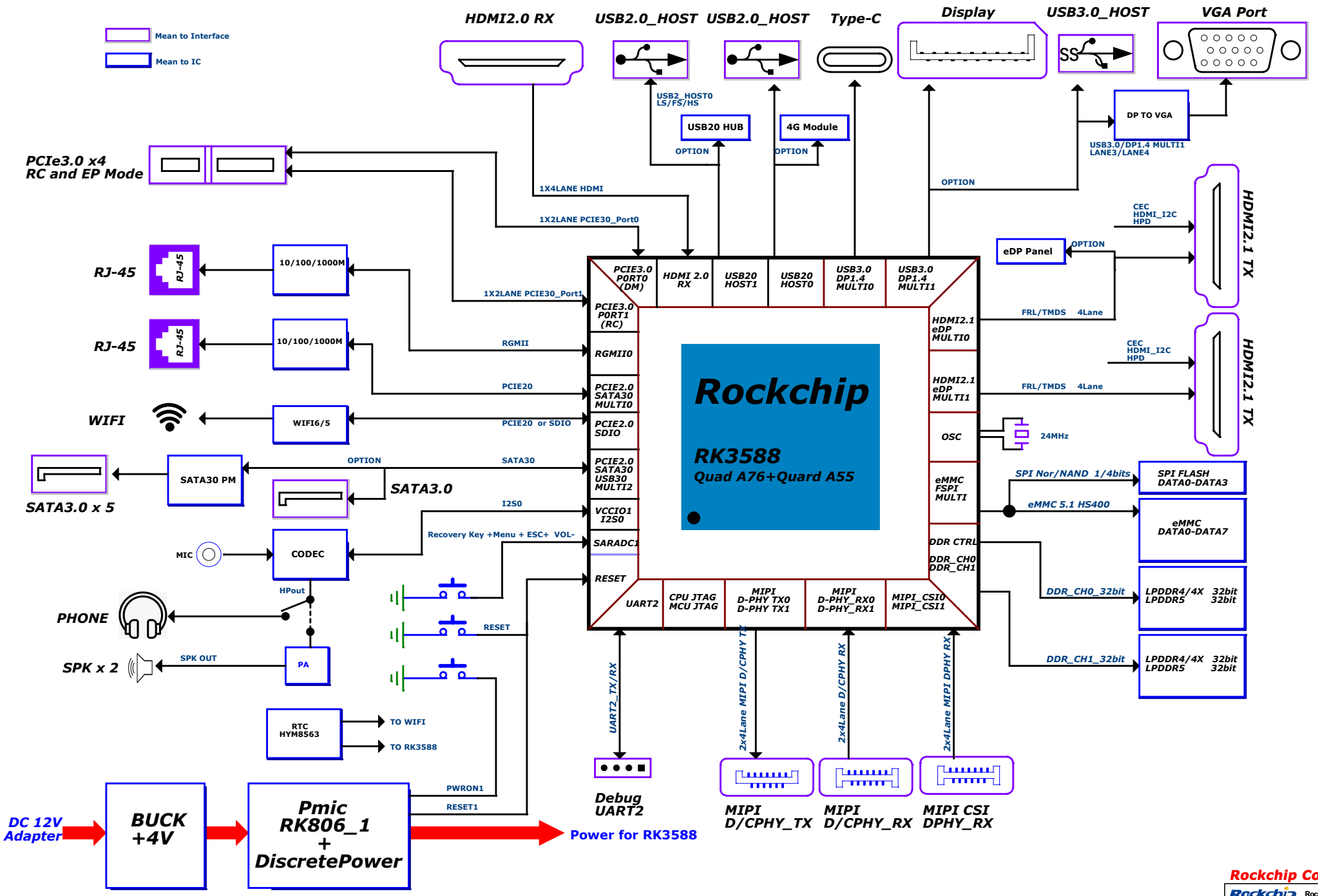
Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2021-12-28	Felix.ruan	1:Revision preliminary version	Chenw
V1.1	2022-02-15	Felix.ruan	1.更改C5808-C5810,C5816的电容两边网络一致的问题。 2.C5205-C5208的耐压值改成25V；C5304－C5307的耐压值改成25V； C5614－C5617的耐压值改成25V。 3.C1600,C1608的电容改成1UF/4V。 4.PCIEx1_0_PERSTn_M1_L网络改成PCIEx1_0_PERSTn_M2_L；PCIEx1_0_CLKREQn _M1_L网络改成PCIEx1_0_CLKREQn_M2_L；PCIEx1_0_WAKEn_M1_L/GPIO1_B3网 络改成PCIEx1_0_WAKEn_M2_L/GPIO1_B3。 5.删除预留的电源。VCC_1V8_S3_PLDO6，"VCC1V8_PMU_DDR_S3"网络的电源直接 接VCC_1V8_S3。 6."VGA_HPDIN_L"(Pin AK27)与"SDMMC_PWREN"(Pin T28)的IO分配互换。 7.为了减少待机功耗，PMUIO2的供电电源改成1.8V。 8.L2300，L2301，L2203，L2205，L2207，L2303的电感0.22uH(TDK)改为0.24uH(Sunlord)； L2201的电感0.22uH(TDK)改为0.22uH (Sunlord)，封装IND_404020。 9.R2001电阻封装改0805。 10.C4900改为NC，R4911的47K改为2K，R4908的100K改为10K，R4909的100K改为10K。 11.eARC的功能不支持，相关eARC的网络改成"HDMI0/1_TX_SBDP/N"	Chenw
V1.2	2022-05-25	Felix.ruan	1.增加AU5426/SI52144的PCIE时钟方案；时钟发生器的OE脚，增加PCIE30X4_CLKREQn* 的控制，在待机时关掉，达到省电目的-----PAGE80 2.更改PAGE04，PAGE10页电流实测数据 3.更改RK3588的封装，增加MIPI D/C PHY的使用描述（此接口的MIPI_DPHY_RX不建义 使用） 4.SPKPA型号TT8642改成TCS7191A-----PAGE70&71 5.HDMI的eARC通道两个电容NC，暂不支持eARC功能----PAGE50 6.新增图纸中2A/3A BUCK的厂家型号 7.增加AW88394的SPK PA参考电路	Chenw
V1.3	2022-08-30	Felix.ruan	1.HDMI的下拉电阻从499ohm改成590ohm。-------PAGE50 2.删掉网络"PMIC_PWR_CTRL3"（Pin T32）。-------PAGE11& PAGE22 3.MP8759增加MODE SELECT控制。------PAGE11&PAGE20 4.增加每个SATA只能扩展5个PORT标注。----PAGE18 5.HDMI RX AVDD0V75和USB20_DVDD_0V75电压改成VDD_0V75_S0----PAGE14&PAGE17 6.R8024，R8026，R8039电阻改为10K；R8007电阻改为300R。----PAGE80 7.HDMI/EDP_TX_VDD_0V75电压网络改为"HDMI_VDDA0V85_S0"，实际软件设置0.8375V。 8.增加PCIE的标注。----PAGE18 9.增加PAGE51.VI －HDMI IN TO MIPI RX 10.RGMII的型号RTL82111改为RK631----PAGE67 11.增加HDMI RX的使用注意事项标注---PAGE49	Chenw



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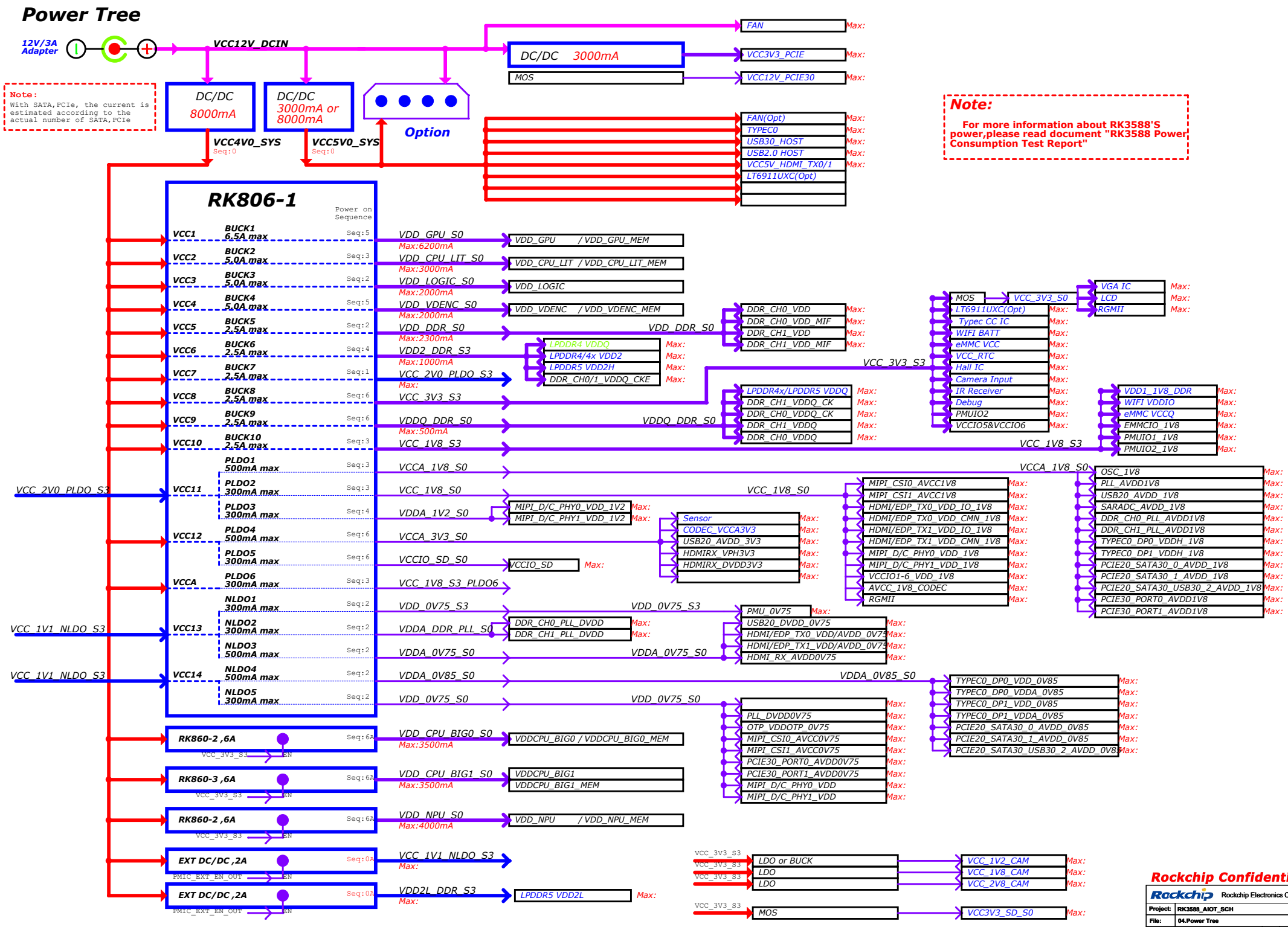
Power Tree



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Rockchip	Rockchip Electronics Co., Ltd
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Designed by:	RZF
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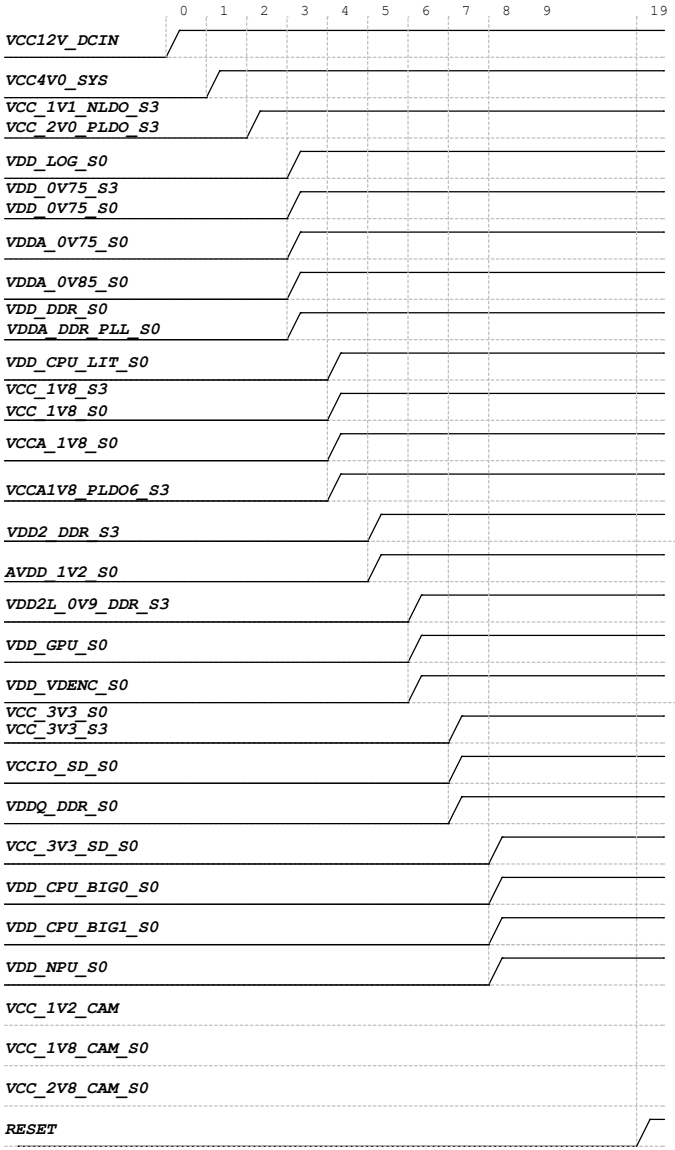
Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC4V0_SYS	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO	RK806-1_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_3V3_S3	EXT_BUCK	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	IO Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3	1.8V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin G20	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VCCIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_IO_SD	1.8V/3.3V
VCCIO3	Pin Y26	1.8V Only	VCCIO3_1V8	VCC_1V8_S0	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VCCIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_1V8_S0	1.8V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VCCIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_3V3_S0	3.3V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VCCIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	3.3V

IO Type	Operating Voltage
1.8V Only	VCCIO*_1V8=1.8V
1.8V or 3.3V	VCCIO*_1V8=1.8V VCCIO*=1.8V or 3.3V

Rockchip Electronics Co., Ltd					
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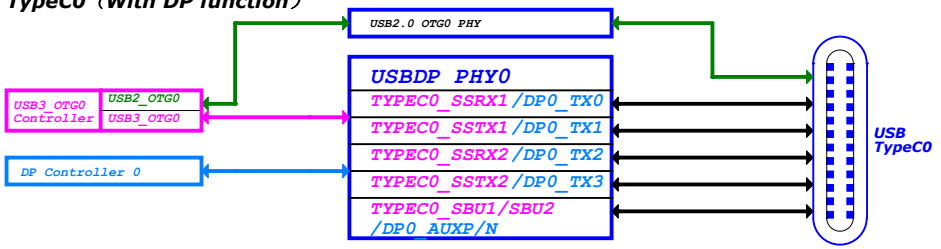
USB Controller Configure Table

Controller Name	Pin Name	Type-C Function	DPx4Lane Function		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1N/DP0_TX1N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2N/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N		DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N		DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM			TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
USB30 OTG1 Device or Host	TYPEC1_SBU1/DP1_AUXP TYPEC1_SBU2/DP1_AUXN	TYPEC1_SBU1 TYPEC1_SBU2	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN
	TYPEC1_SSRX1P/DP1_TX0P TYPEC1_SSRX1N/DP1_TX0N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX0P DP1_TX0N		DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N
	TYPEC1_SSTX1P/DP1_TX1P TYPEC1_SSTX1N/DP1_TX1N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX1P DP1_TX1N		DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N
	TYPEC1_SSRX2P/DP1_TX2P TYPEC1_SSRX2N/DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N		DP1_TX2P DP1_TX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N
	TYPEC1_SSTX2P/DP1_TX3P TYPEC1_SSTX2N/DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N		DP1_TX3P DP1_TX3N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N
USB20 OTG1 Device or Host	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM			TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM

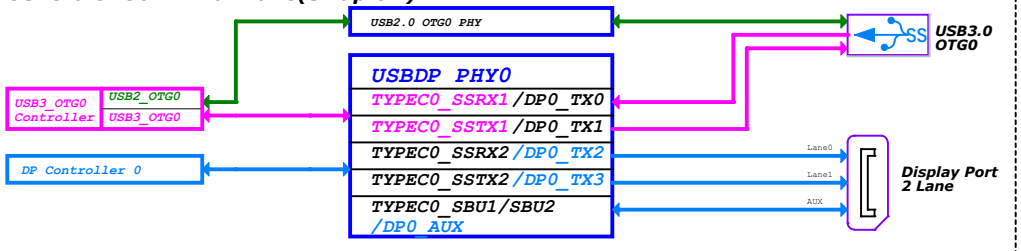
			OPTION1 USB30 HOST	OPTION2 USB30 HOST	OPTION3 USB30 HOST
USB30 HOST2	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN	USB30_2_SSTXP USB30_2_SSTXN	USB30_2_SSTXP USB30_2_SSTXN
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN	USB30_2_SSRXP USB30_2_SSRXN	USB30_2_SSRXP USB30_2_SSRXN
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM		
USB20 HOST1	USB20_HOST1_DP USB20_HOST1_DM			USB20_HOST1_DP USB20_HOST1_DM	
					TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM

Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3_TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1_TXDP/N

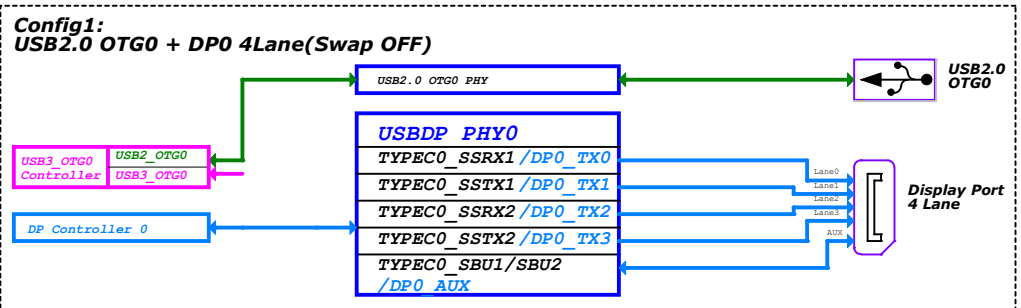
Config0:
TypeC0（With DP function）



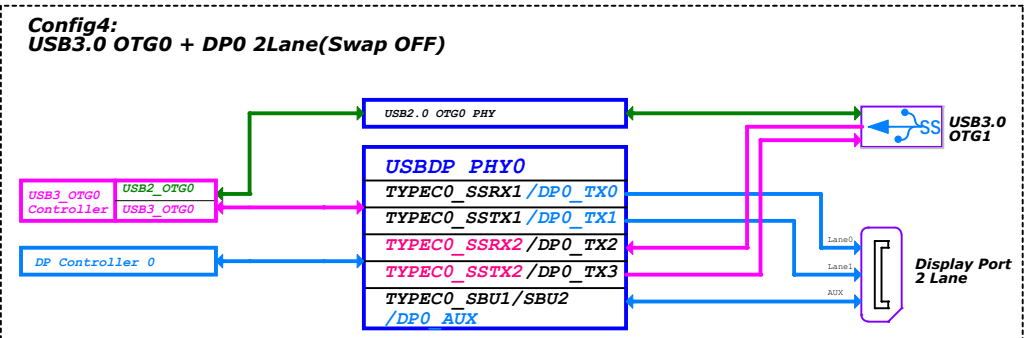
Config3:(Default)
USB3.0 OTG0 + DP0 2Lane(Swap ON)



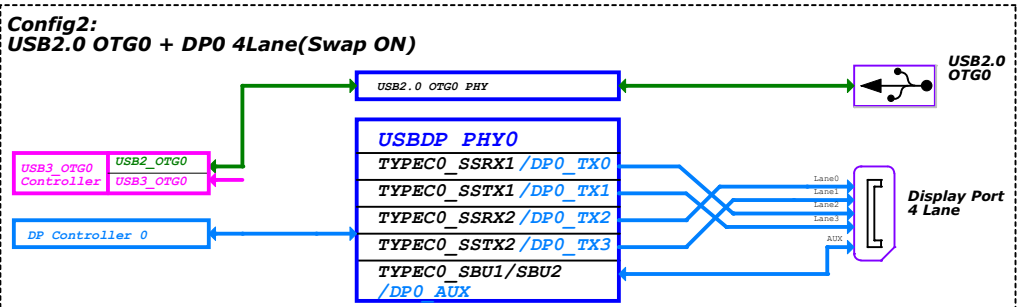
Config1:
USB2.0 OTG0 + DP0 4Lane(Swap OFF)



Config4:
USB3.0 OTG0 + DP0 2Lane(Swap OFF)



Config2:
USB2.0 OTG0 + DP0 4Lane(Swap ON)



Rockchip	Rockchip Electronics Co., Ltd
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File:	07.USB Controller Configure Tab
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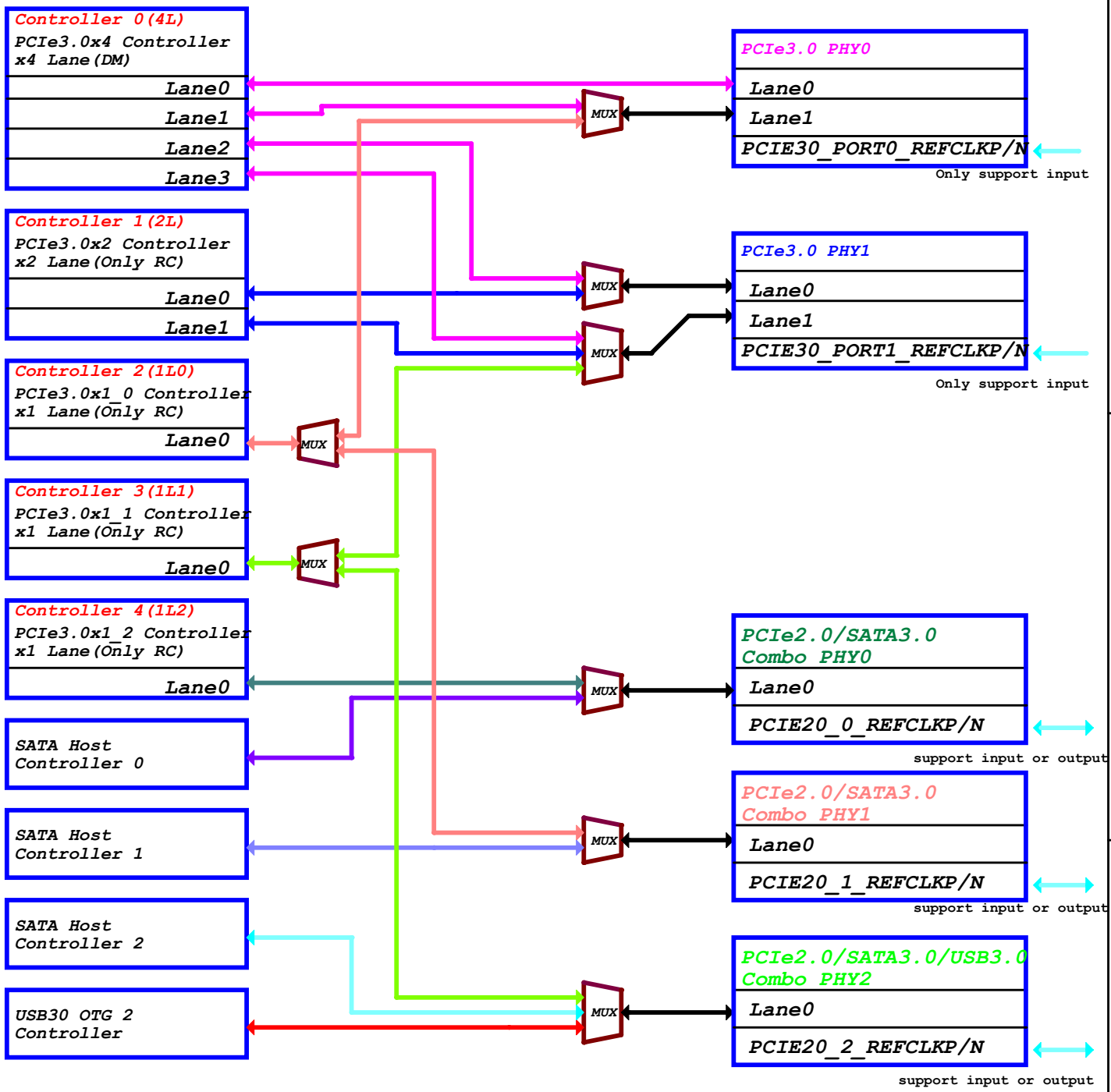
PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure			Control GPIO
	OPTION	CLK LANE	DATA LANE	
PCIE30X4 RC & EP	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0	PCIE30X4_CLKREQ_M* PCIE30X4_WAKEN_M* PCIE30X4_PERSTN_M* PCIE30X4_BUTTON_RSTN
	OPTION2	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	
	OPTION3	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT1_TX0 PCIE30_PORT0_RX0 PCIE30_PORT1_RX0 PCIE30_PORT0_TX1 PCIE30_PORT1_TX1 PCIE30_PORT0_RX1 PCIE30_PORT1_RX1	
PCIE30X2 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0	PCIE30X2_CLKREQ_M* PCIE30X2_WAKEN_M* PCIE30X2_PERSTN_M* PCIE30X2_BUTTON_RSTN
	OPTION2	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIE30X1_0 RC	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	PCIE30X1_0_CLKREQ_M* PCIE30X1_0_WAKEN_M*
	OPTION2	PCIE20_1_REFCLKP PCIE20_1_REFCLKN	PCIE20_1_TXP PCIE20_1_RXP PCIE20_1_TXN PCIE20_1_RXN	PCIE30X1_0_PERSTN_M* PCIE30X1_0_BUTTON_RSTN
PCIE30X1_1 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	PCIE30X1_1_CLKREQ_M* PCIE30X1_1_WAKEN_M*
	OPTION2	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TXP PCIE20_2_RXP PCIE20_2_TXN PCIE20_2_RXN	PCIE30X1_1_PERSTN_M* PCIE30X1_1_BUTTON_RSTN
PCIE20X1_2 RC	OPTION1	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TXP PCIE20_0_RXP PCIE20_0_TXN PCIE20_0_RXN	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Note:
PCIE30_PORT*_REF_CLKP/N is input gpio

PCIE20_*_REFCLKP/N is output or input gpio

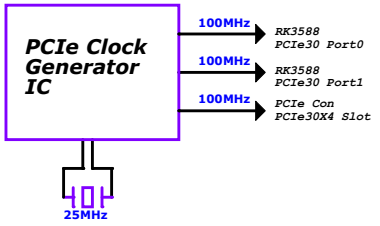
Note:
M*=Mean to M0 or M1,It's the same source,Just multiplex to M0 or M1, So,Only use one at the same time.

PCIe/SATA Function Combination

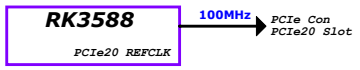
Function Combination

Function Item	PCIEX4	PCIEX2	PCIEX1	SATA
Option1	1(DM)	0	3(RC)	0
Option2	1(DM)	0	2(RC)	1
Option3	1(DM)	0	1(RC)	2
Option4	1(DM)	0	0	3
Option5	0	1(DM)+1(RC)	3(RC)	0
Option6	0	1(DM)+1(RC)	2(RC)	1
Option7	0	1(DM)+1(RC)	1(RC)	2
Option8	0	1(DM)+1(RC)	0	3
Option9	0	1(DM)	4(RC)	1
Option10	0	1(DM)	3(RC)	2
Option11	0	1(DM)	2(RC)	3
Option12	0	0	1(DM)+4(RC)	2
Option13	0	0	1(DM)+3(RC)	3

PCIe3.0 REFCLK



PCIe2.0 REFCLK



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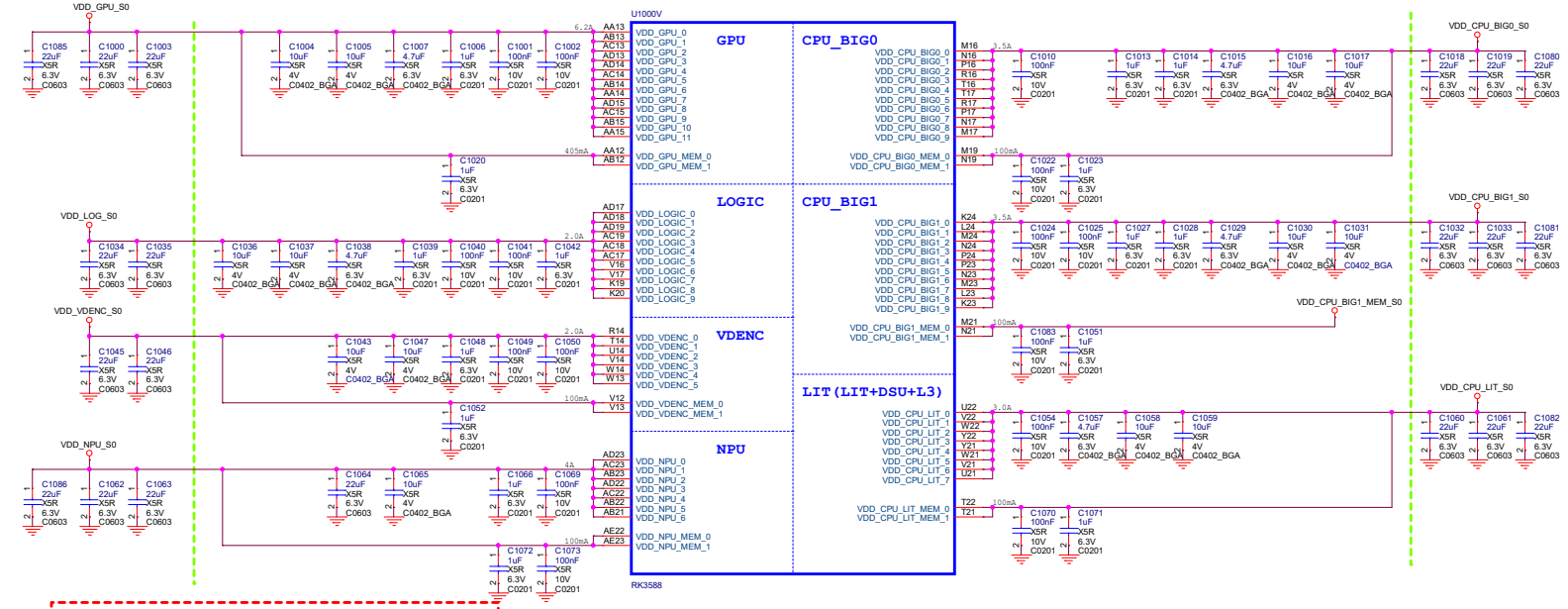
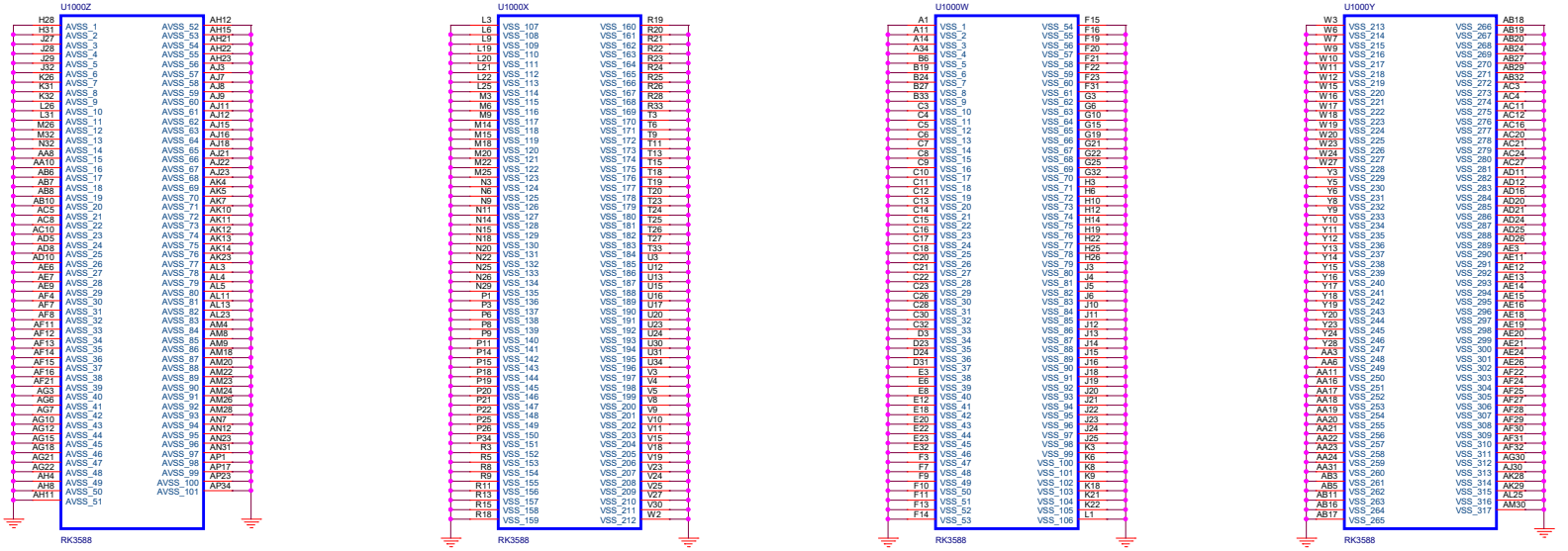
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	08.PCIE Fun Map		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
Designed by:	RZF	Reviewed by:	Sheet: 8 of 99

RK3588_V(POWER)



Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package



Rockchip Confidential

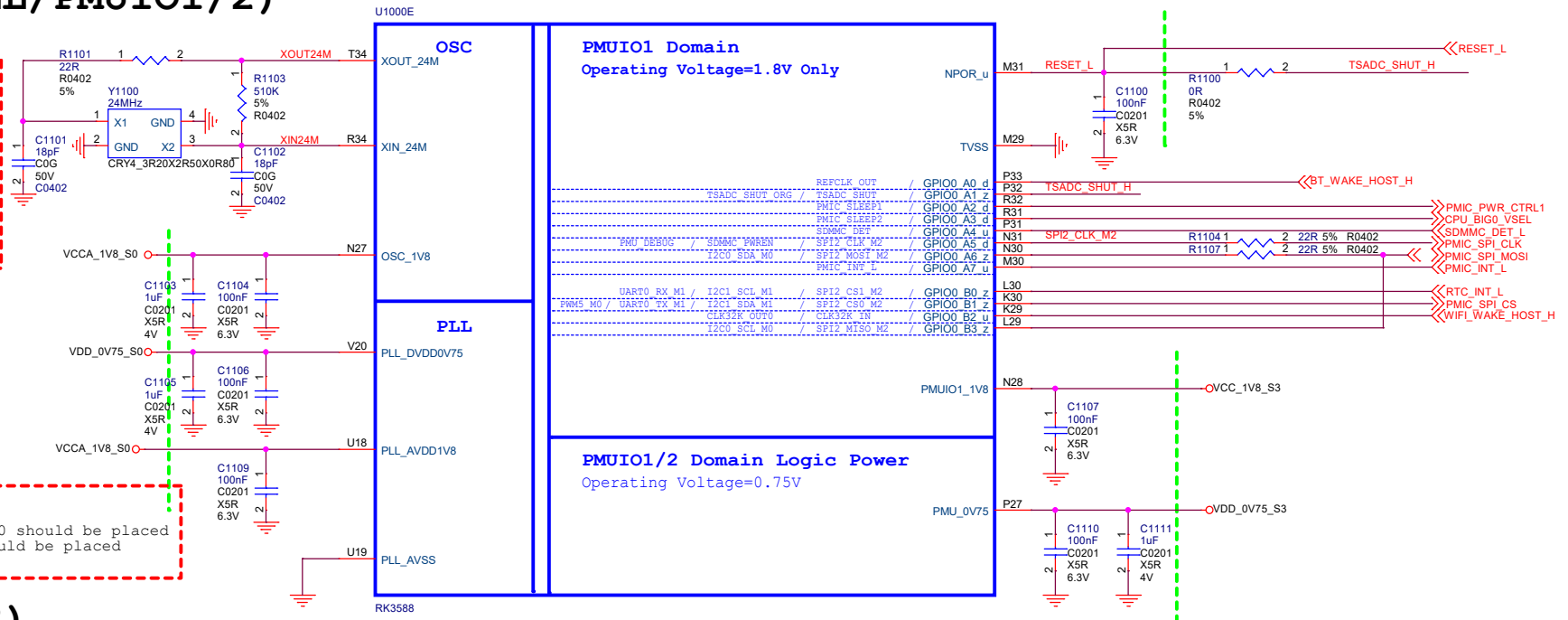
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588_AIOT_SCH
File:	10.RK3588_Power/GND
Date:	Wednesday, October 12, 2022
Rev:	V1.3
Designed by:	RZF
Reviewed by:	
Sheet:	10 of 99

RK3588_E(OSC/PLL/PMUIO1/2)

Note:
Adjusted the load capacitance according to the crystal specification

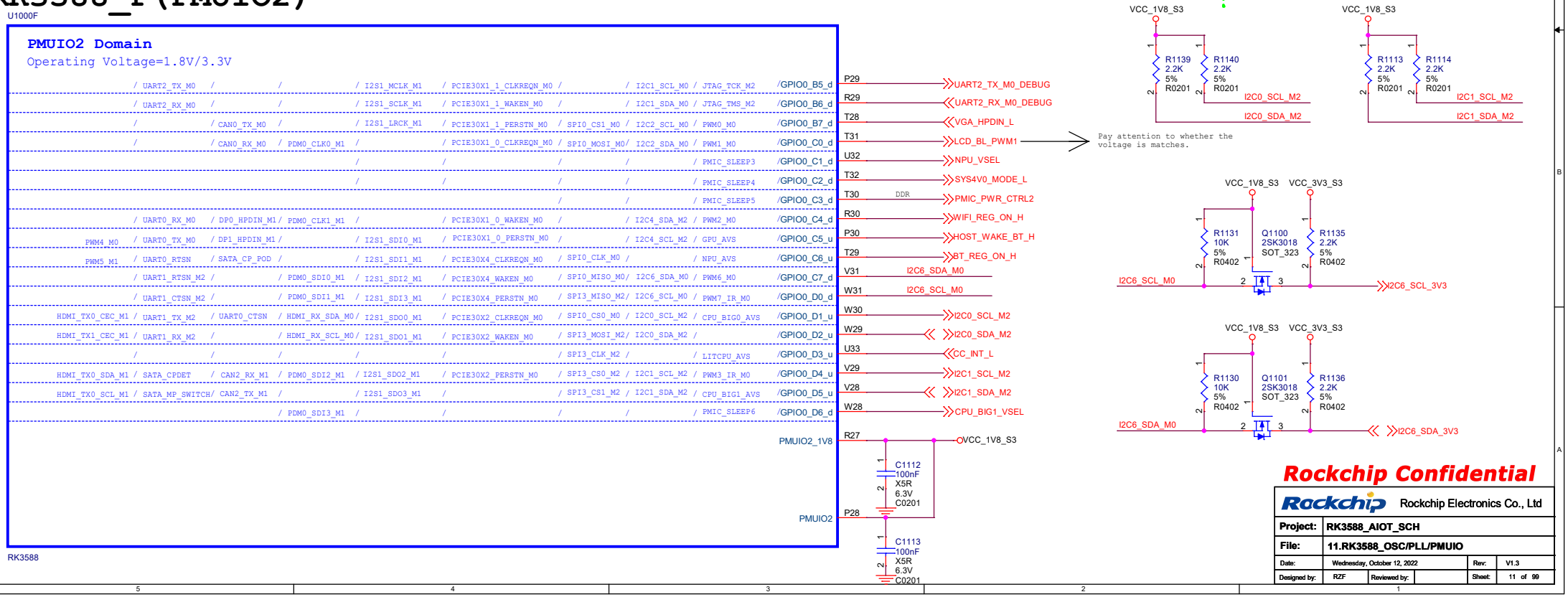
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF



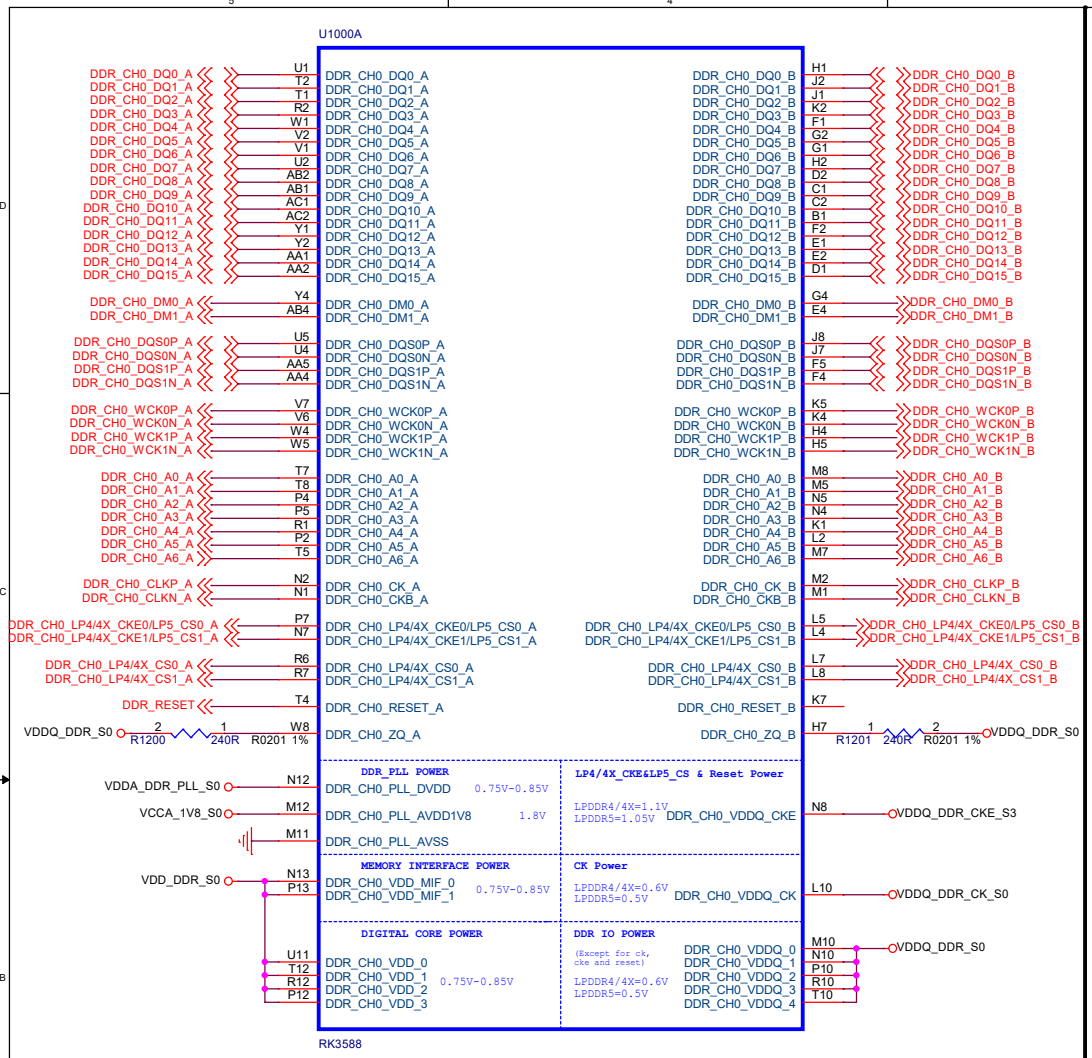
Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

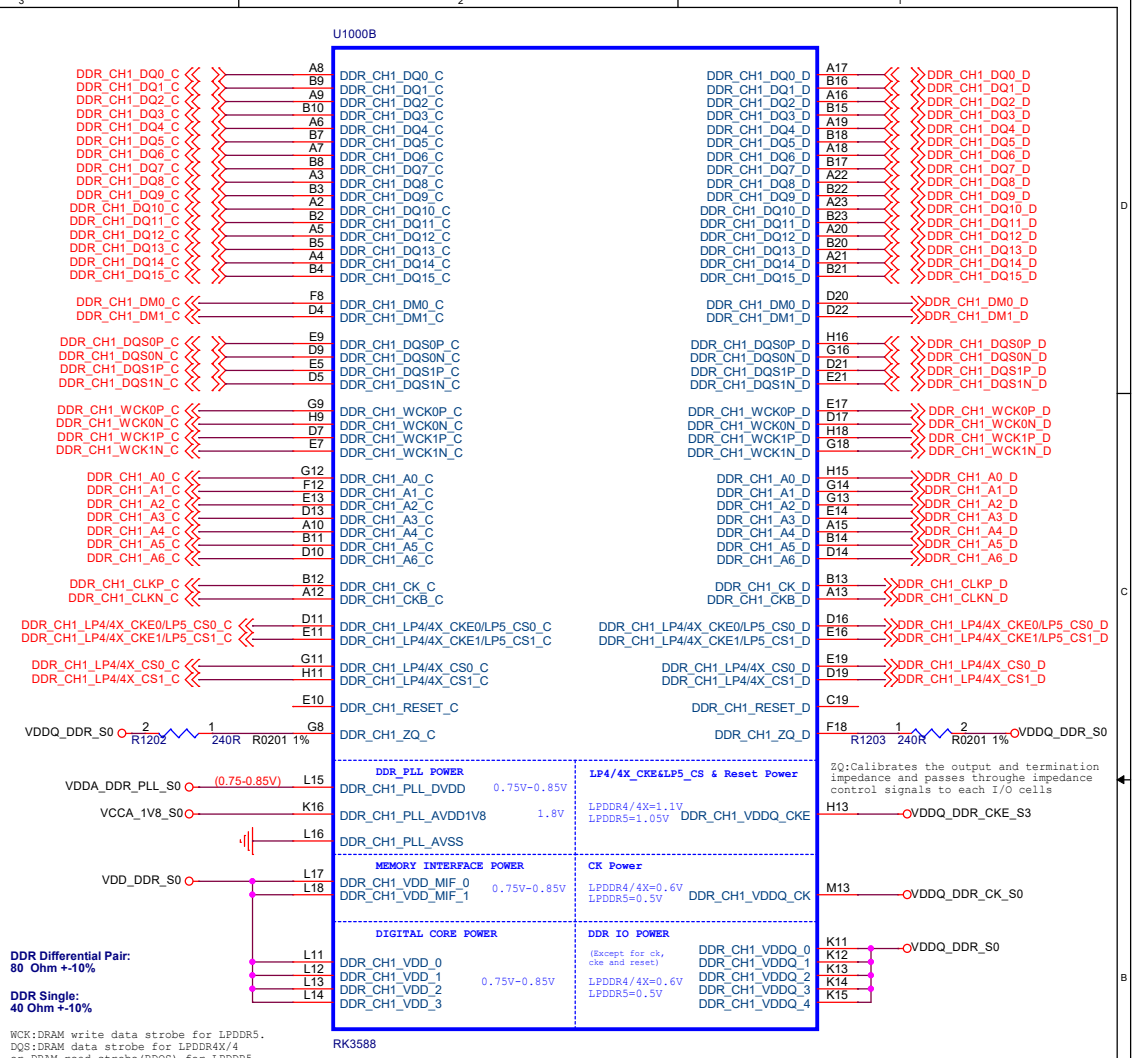
RK3588_F(PMUIO2)



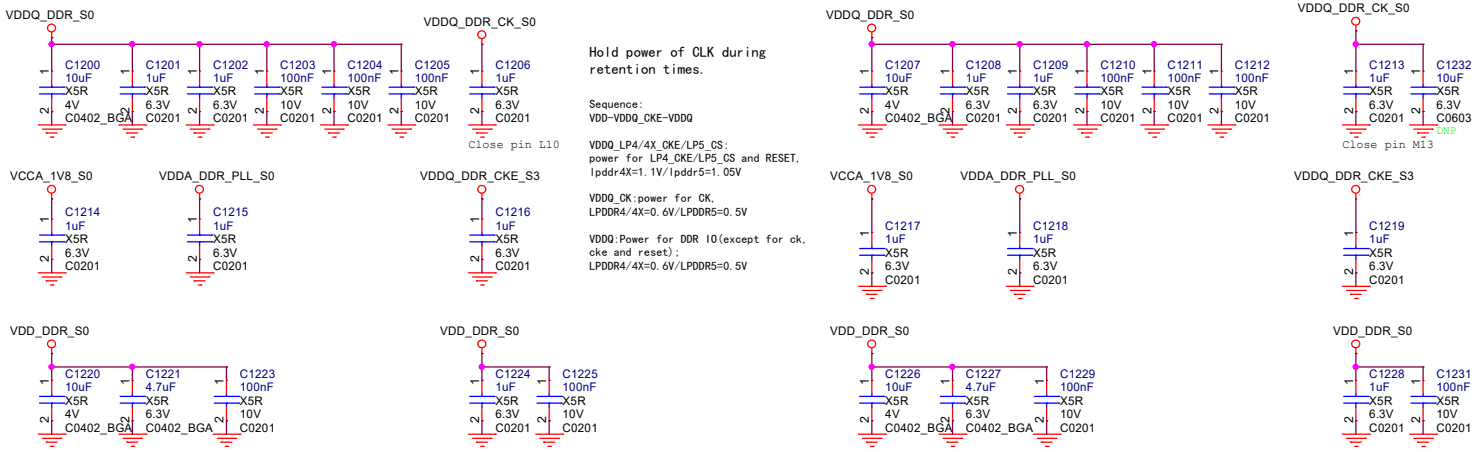
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	11.RK3588_OSC/PLL/PMUIO		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
Designed by: RZF	Reviewed by:	Sheet:	11 of 99



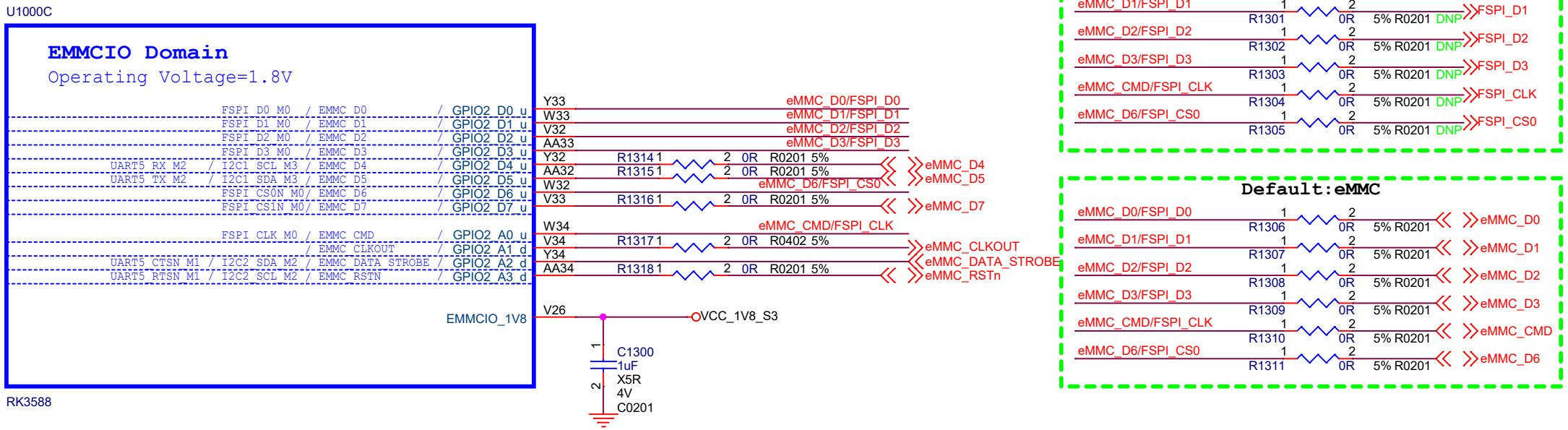


DDR FILTER

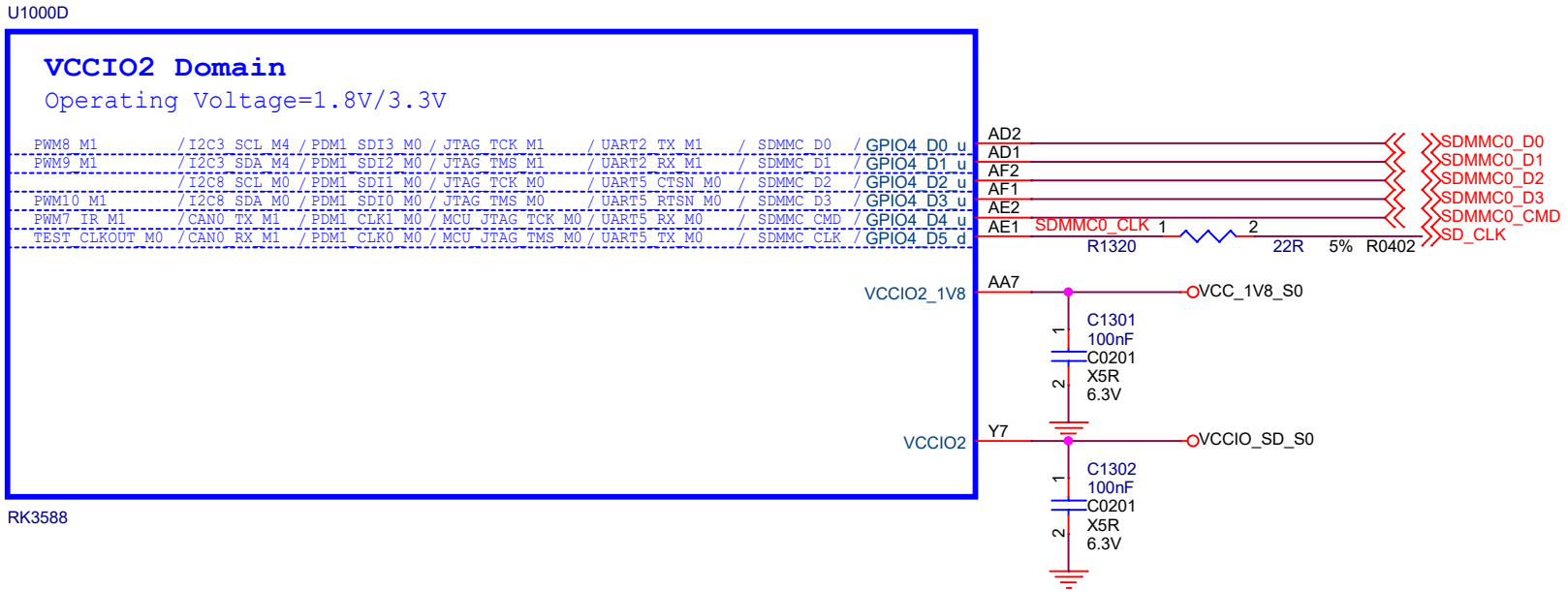


Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	12.RK3588 DDR Controler		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
Designed by: RZF	Reviewed by:	Sheet:	12 of 99

RK3588_C(EMMCIO Domain)



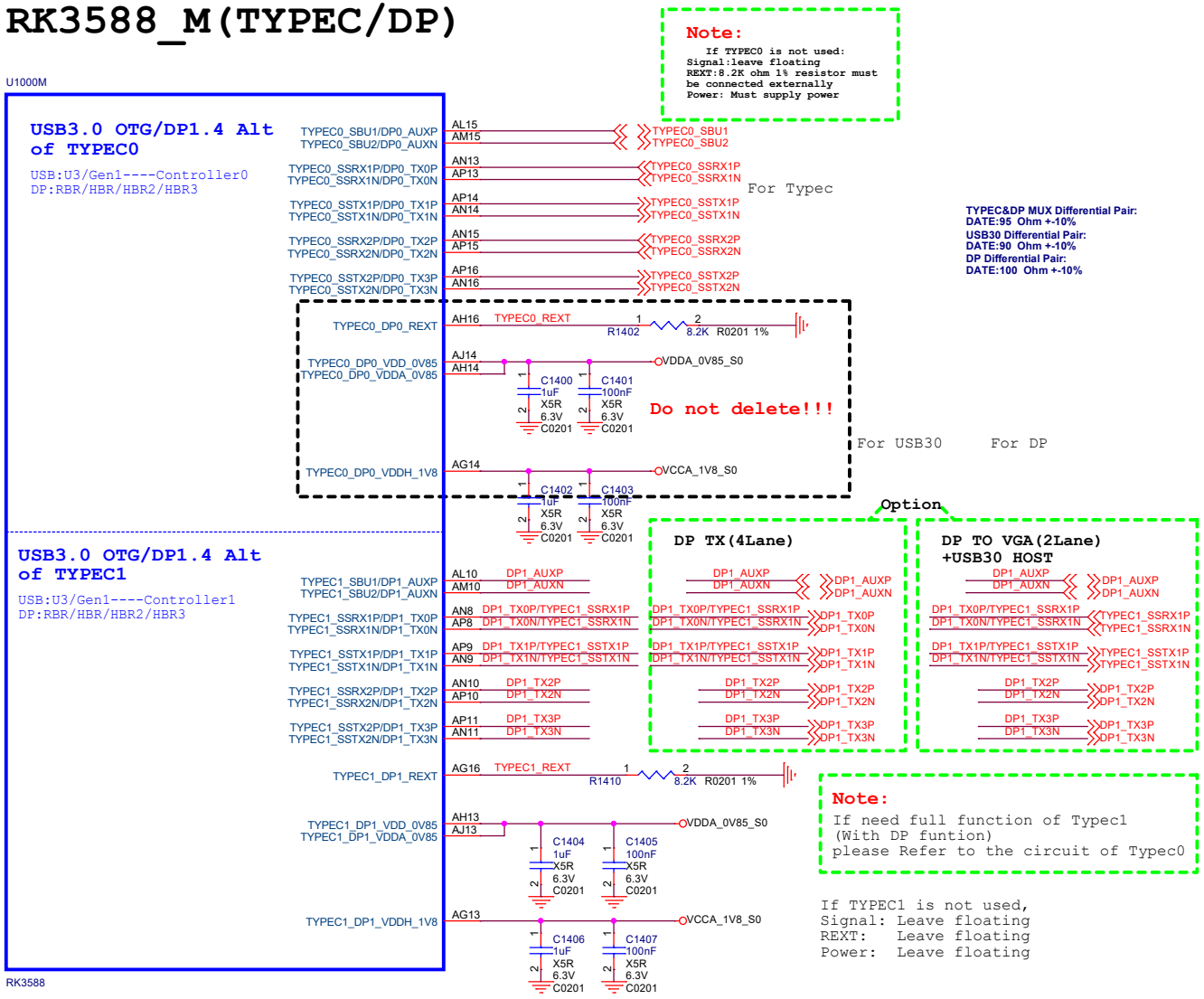
RK3588_D(VCCIO2 Domain)



Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	13.RK3588_Flash/SD Controller		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
Designed by: RZF	Reviewed by:	Sheet:	13 of 99

RK3588_M(TYPEC/DP)



Note:

If TYPEC0 is not used:
Signal:leave floating
REXT:8.2K ohm 1% resistor must be connected externally
Power: Must supply power

Note:

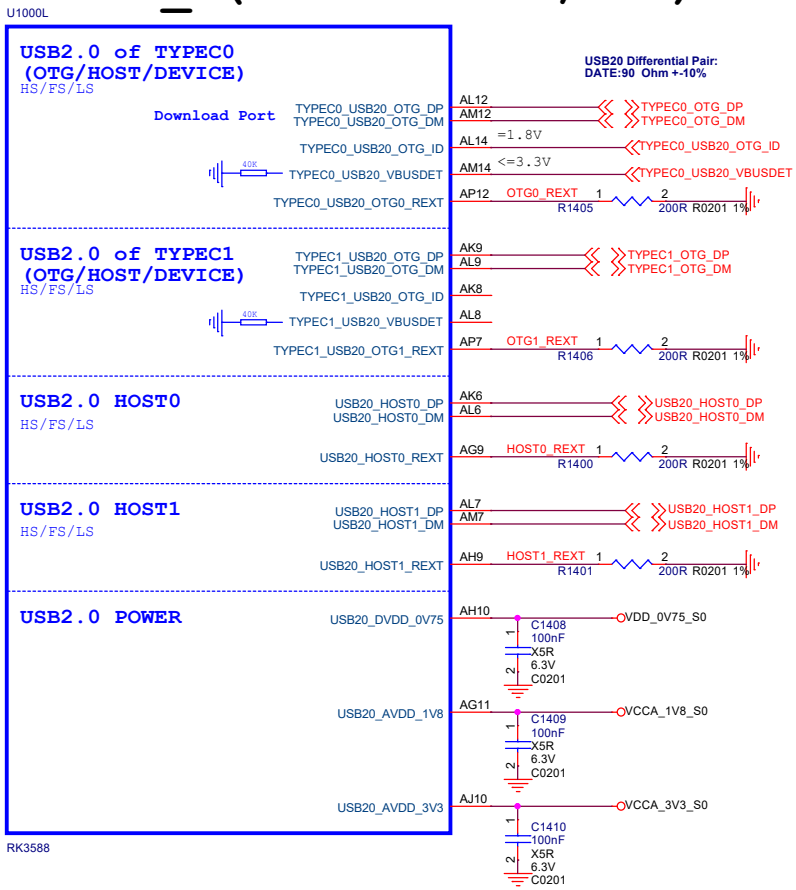
If need full function of Typec1 (With DP funtion) please Refer to the circuit of Typec0

If TYPEC1 is not used,
Signal: Leave floating
REXT: Leave floating
Power: Leave floating

USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*TYPEC_SSTX1P/1N&TYPEC_SSRX1P/1N or TYPEC_SSTX2P/2N&TYPEC_SSRX2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1 DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3 DP:Lane0 Lane1*

RK3588_L(USB2.0 HOST/OTG)



Note:

TYPEC0_USB20_OTG:

DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

TYPEC1_USB20_OTG:

If not used:
DP/DM:Leave floating
ID:Leave floating
VBUSDET:Leave floating
REXT:Leave floating
Power:Leave floating

USB20_HOST0/USB20_HOST1:

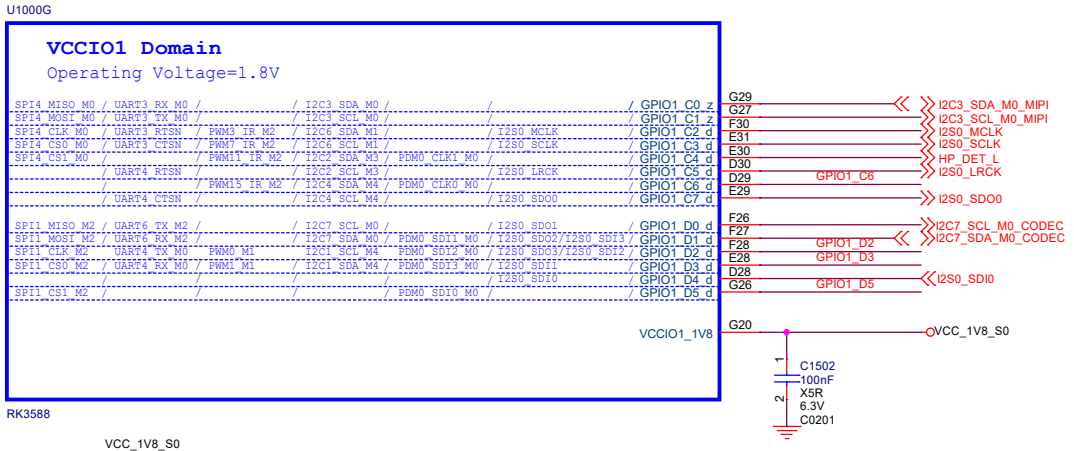
If not used:
DP/DM:Leave floating
REXT:Leave floating
Power:Leave floating

Note:

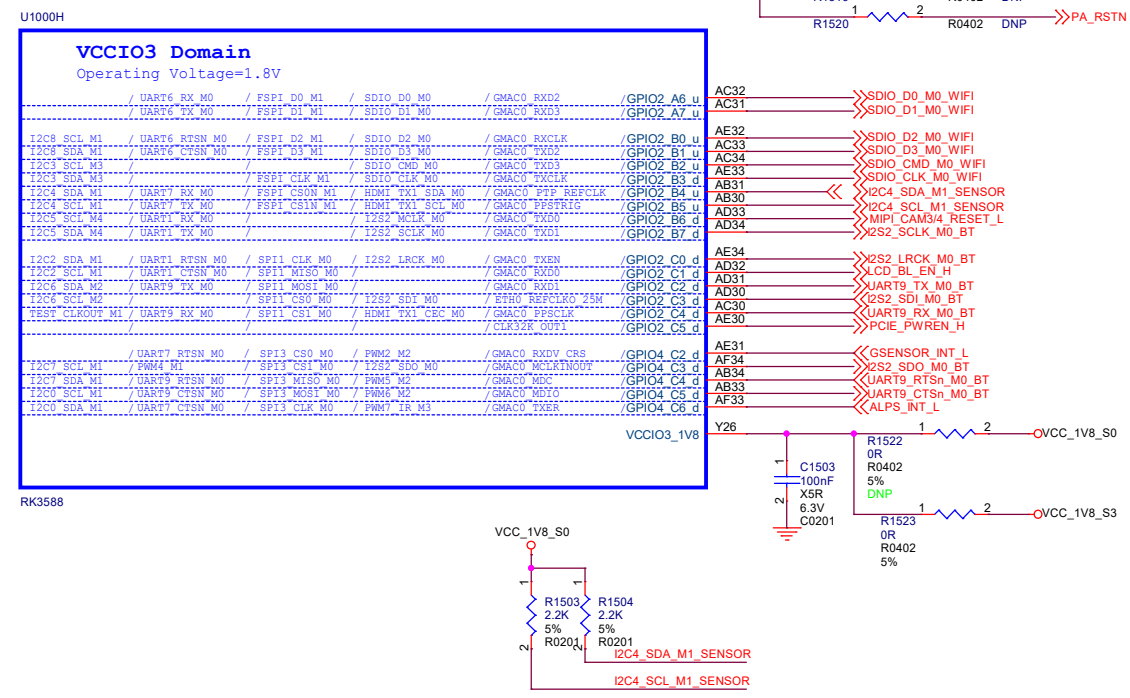
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	14.RK3588_USB30/USB20_Ctrl				
Date:	Wednesday, October 12, 2022		Rev:	V1.3	
Designed by:	RZF	Reviewed by:		Sheet:	14 of 99

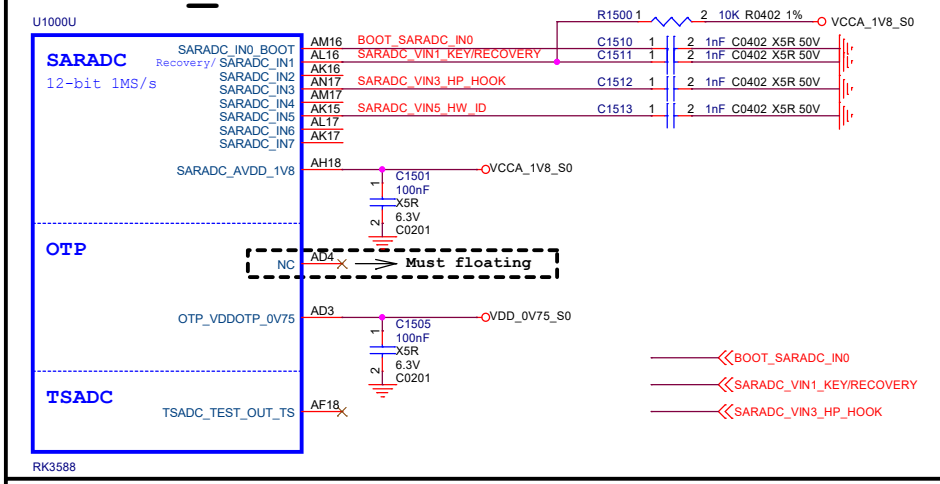
RK3588_G(VCCIO1 Domain)



RK3588_H(VCCIO3 Domain)



RK3588_U(SARADC/OTP)



BOOT MODE CONFIG

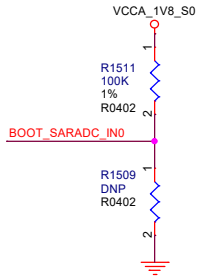


TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

BOARD ID CONFIG

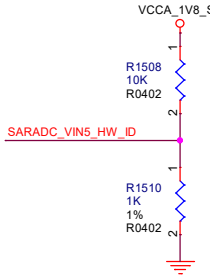
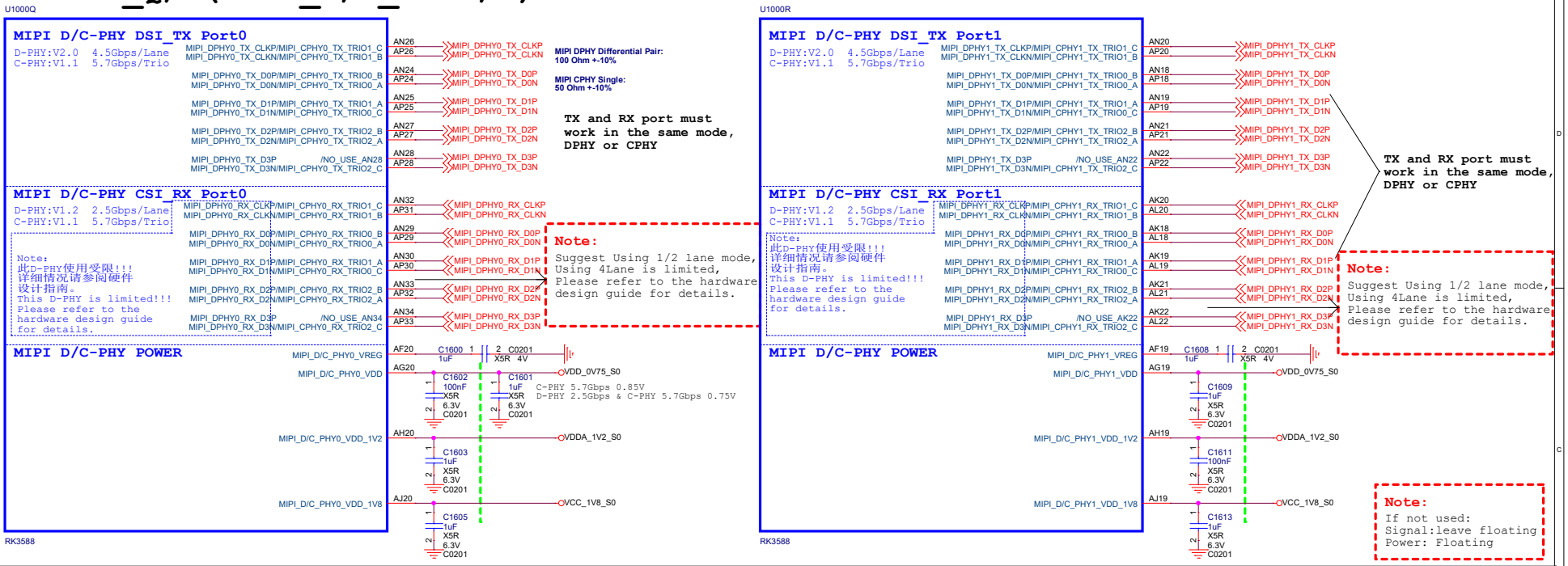


TABLE 2

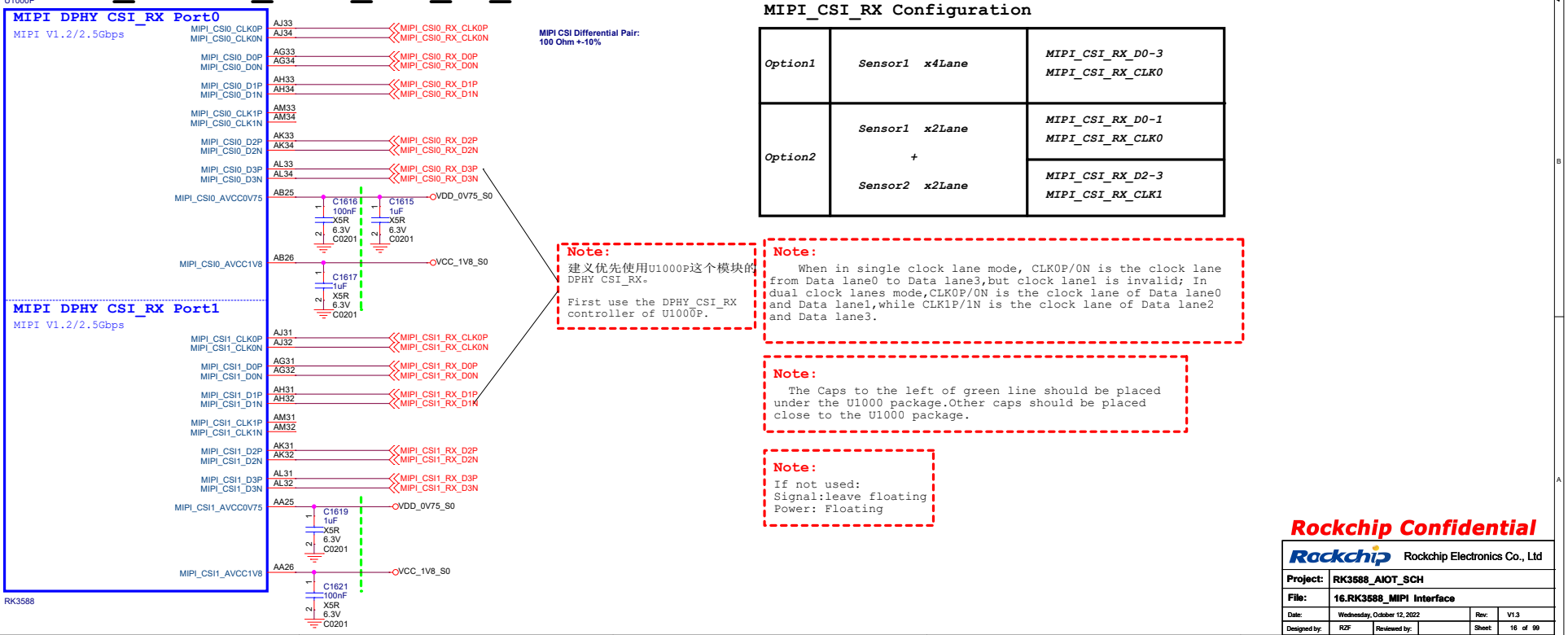
Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	V1.0
LEVEL2	100K	20K	682	0.3V	V2.0
LEVEL3	100K	51K	1365	0.6V	V3.0
LEVEL4	100K	100K	2047	0.9V	V4.0
LEVEL5	100K	200K	2730	1.2V	V5.0
LEVEL6	100K	499K	3412	1.5V	V6.0
LEVEL7	100K	DNP	4095	1.8V	V7.0

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	15.RK3588_SARADC/1.8V Only GPIO		
Date:	Friday, October 21, 2022	Rev:	V1.3
Designed by: RZF	Reviewed by:	Sheet:	15 of 99

RK3588_Q/R(MIPI_D/C_PHY0/1)



RK3588_P(MIPI_DPHY_CSI_RX_PHY)



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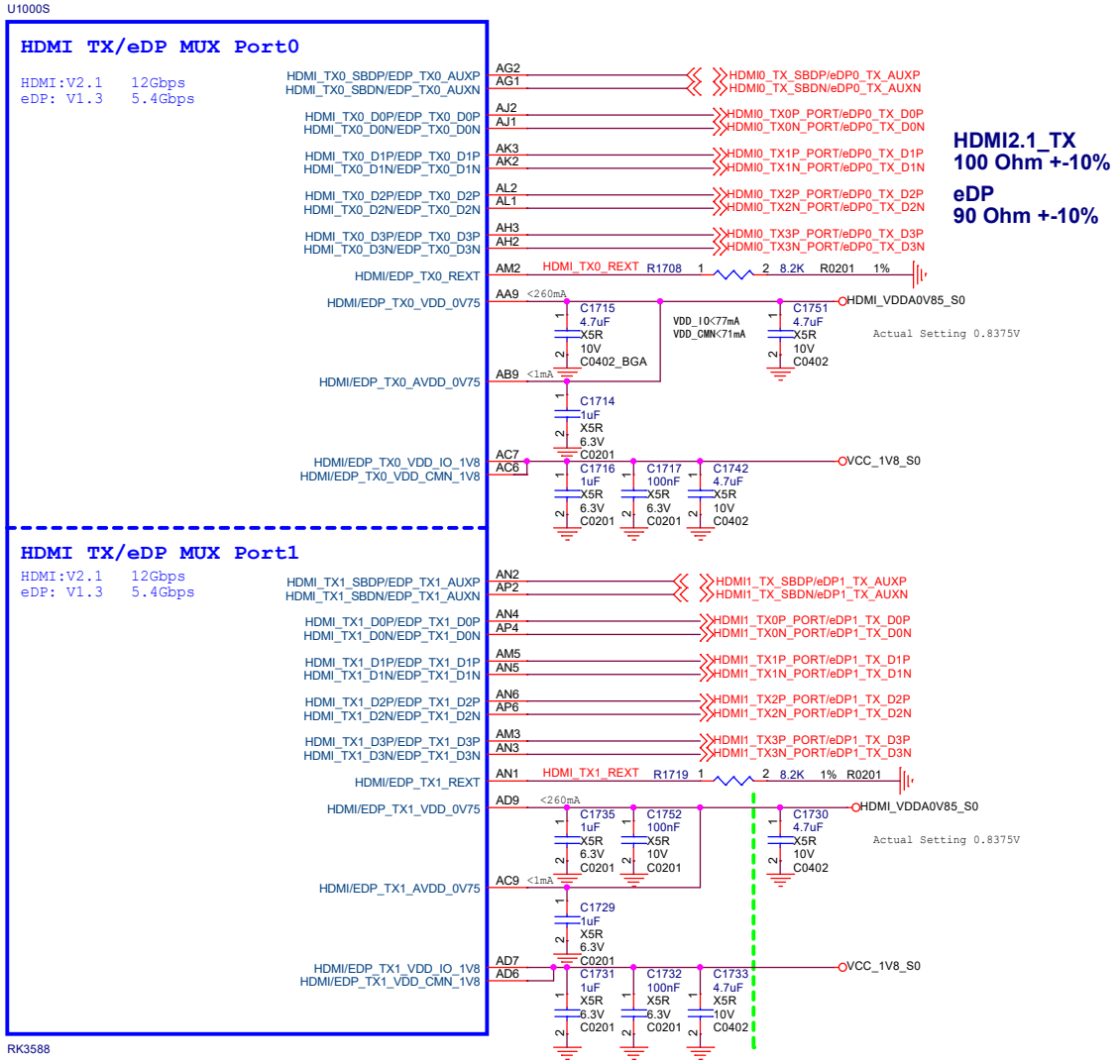
Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	16.RK3588_MIPI Interface		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
Designed by: RZF	Reviewed by:	Sheet:	16 of 99

RK3588_S(HDMI2.1 TX)

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.



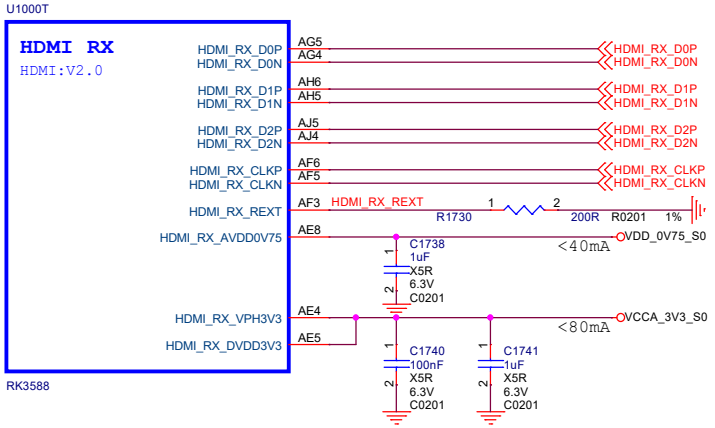
HDMI2.1_TX
100 Ohm +-10%

eDP
90 Ohm +-10%

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

RK3588_T(HDMI20 RX)



HDMI20_RX
100 Ohm +-10%

Note:
If not used:
Signal:leave floating
Power: Floating

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Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	17.RK3588_HDMI/eDP Interface				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:		Sheet:	17 of 99

RK3588_N(PCIE20)

Note:
If not used:
Signal:leave floating
Power: Floating

CLK Differential Pair: 100 Ohm±10%
DATA Differential Pair: PCIE20: 85 Ohm ±10% SATA30: 100 Ohm ±10% USB30: 90ohm ±10%

U1000N

PCIE20/SATA30 Mux0

PCIe20x1_2 1Lane(RC)--4(1L2)
SATA30 HOST Controller0
MUX

input or output

PCIE20_0_REFCLKP L32
PCIE20_0_REFCLKN L33
PCIE20_0_TXP/SATA30_0_TXP M34 → PCIE20_0_TXP/SATA30_0_TXP
PCIE20_0_TXN/SATA30_0_TXN M33 → PCIE20_0_TXN/SATA30_0_TXN
PCIE20_0_RXP/SATA30_0_RXP N33 → PCIE20_0_RXP/SATA30_0_RXP
PCIE20_0_RXN/SATA30_0_RXN N34 → PCIE20_0_RXN/SATA30_0_RXN
PCIE20_SATA30_0_AVDD_0V85 M28 → VDDA_0V85_S0
C1810 10uF X5R 4V C0402
PCIE20_SATA30_0_AVDD_1V8 M27 → VCCA_1V8_S0
C1808 1uF X5R 4V C0201

PCIe20x1_2 Controller:
Wake/clkreq/perstn Optional:
Option0: Pin AH24/AJ24/AG23
Option1 :Pin AJ25/AJ28/AK24

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30 Mux1

PCIe30x1_0 1Lane(RC)--2(1L0)
SATA30 HOST Controller1
MUX

input or output

PCIE20_1_REFCLKP H32 → PCIE20_1_REFCLKP
PCIE20_1_REFCLKN H33 → PCIE20_1_REFCLKN
PCIE20_1_TXP/SATA30_1_TXP K33 → PCIE20_1_TXP/SATA30_1_TXP
PCIE20_1_TXN/SATA30_1_TXN K34 → PCIE20_1_TXN/SATA30_1_TXN
PCIE20_1_RXP/SATA30_1_RXP J33 → PCIE20_1_RXP/SATA30_1_RXP
PCIE20_1_RXN/SATA30_1_RXN J34 → PCIE20_1_RXN/SATA30_1_RXN
PCIE20_SATA30_1_AVDD_0V85 L28 → VDDA_0V85_S0
C1818 100nF X5R 6.3V C0201
PCIE20_SATA30_1_AVDD_1V8 L27 → VCCA_1V8_S0
C1816 100nF X5R 6.3V C0201

PCIe30x1_0 Controller:
Wake/clkreq/perstn Optional:
Option0: Pin R30/T31/P30
Option1 :Pin AL28/AL29/AK27
Option2: Pin D27/E25/E24

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30/USB30 HOST Mux2

PCIe30x1_1 1Lane(RC)--3(1L1)
SATA30 HOST Controller2
USB30 HOST Controller2
MUX

input or output

PCIE20_2_REFCLKP G31
PCIE20_2_REFCLKN G30
PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP H30 → PCIE20_2_TXP/SATA30_2_TXP
PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN H29 → PCIE20_2_TXN/SATA30_2_TXN
PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP J31 → PCIE20_2_RXP/SATA30_2_RXP
PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN J30 → PCIE20_2_RXN/SATA30_2_RXN
PCIE20_SATA30_USB30_2_AVDD_0V85 K28 → VDDA_0V85_S0
C1806 1uF X5R 4V C0201
PCIE20_SATA30_USB30_2_AVDD_1V8 K27 → VCCA_1V8_S0
C1804 1uF X5R 4V C0201

PCIe30x1_1 Controller:
Wake/clkreq/perstn Optional:
Option0: Pin R29/P29/T28
Option1 :Pin AL30/AK30/AM29
Option2: Pin A25/A24/C25

PCIE20:Gen1/Gen2
USB 30:Gen1
SATA30:Gen1/Gen2/Gen3

RK3588

Note:
The SATA differential trace impedance is 100 OHM
The SATA trace length is less than 5 inch

Note:
每个SATA PORT最多只能扩展5个SATA，不支持二级扩展。
Each sata port can only expand 5 sata port at most,No support level-2 expand.

RK3588_O(PCIE30)

Note:
Only PCIE3.0 Controller 0 support RC and EP,Other controller only support RC Mode.

U1000O

PCIE30X4

PCIe30X4 4Lane(DM)--0(4L)
PCIe30x1_0 1Lane(RC)--2(1L0)
PCIE20/SATA30 MUX1
PCIe30x2 2Lane(RC)--1(2L)
PCIe30x1_1 1Lane(RC)--3(1L1)
PCIE20/SATA30/USB30 MUX2

PCIE30:
PCIe1.1(2.5Gbps)
PCIe2.1(5Gbps)
PCIe3.0(8Gbps)

PCIE30 PORT0

input
PCIE30_PORT0_REF_CLKP E33 → PCIE30_PORT0_REFCLKP_IN
PCIE30_PORT0_REF_CLKN E34 → PCIE30_PORT0_REFCLKN_IN

Lane0
PCIE30_PORT0_TX0P D32 → PCIE30_PORT0_TX0P
PCIE30_PORT0_TX0N D33 → PCIE30_PORT0_TX0N
PCIE30_PORT0_RX0P G33 → PCIE30_PORT0_RX0P
PCIE30_PORT0_RX0N G34 → PCIE30_PORT0_RX0N

Lane1
PCIE30_PORT0_TX1P C33 → PCIE30_PORT0_TX1P
PCIE30_PORT0_TX1N C34 → PCIE30_PORT0_TX1N
PCIE30_PORT0_RX1P F32 → PCIE30_PORT0_RX1P
PCIE30_PORT0_RX1N F33 → PCIE30_PORT0_RX1N

PCIE30_PORT0_RESREF B34 PCIE30_0_REF R1801 1 2 200R 1% R0201
PCIE30_PORT0_AVDD0V75 G24 → VDD_0V75_S0
C1802 1uF X5R 6.3V C0201
C1803 4.7uF X5R 10V C0402
PCIE30_PORT0_AVDD1V8 G23 → VCCA_1V8_S0
C1800 1uF X5R 6.3V C0201
C1801 4.7uF X5R 10V C0402

PCIE30 PORT1

input
PCIE30_PORT1_REF_CLKP A28 → PCIE30_PORT1_REFCLKP_IN
PCIE30_PORT1_REF_CLKN B28 → PCIE30_PORT1_REFCLKN_IN

Lane0
PCIE30_PORT1_TX0P B30 → PCIE30_PORT1_TX2P
PCIE30_PORT1_TX0N A30 → PCIE30_PORT1_TX2N
PCIE30_PORT1_RX0P B32 → PCIE30_PORT1_RX2P
PCIE30_PORT1_RX0N A32 → PCIE30_PORT1_RX2N

Lane1
PCIE30_PORT1_TX1P C29 → PCIE30_PORT1_TX3P
PCIE30_PORT1_TX1N B29 → PCIE30_PORT1_TX3N
PCIE30_PORT1_RX1P C31 → PCIE30_PORT1_RX3P
PCIE30_PORT1_RX1N B31 → PCIE30_PORT1_RX3N

PCIE30_PORT1_RESREF A33 PCIE30_1_REF R1807 1 2 200R 1% R0201
PCIE30_PORT1_AVDD0V75 H24 → VDD_0V75_S0
C1814 1uF X5R 6.3V C0201
C1815 4.7uF X5R C0402 10V
PCIE30_PORT1_AVDD1V8 H23 → VCCA_1V8_S0
C1812 100nF X5R 6.3V C0201
C1813 4.7uF X5R 10V C0402

CLK Differential Pair: 100 Ohm ±10%
DATA Differential Pair: PCIE30: 85 Ohm ±10%

PCIe30x4 Controller:
Wake/clkreq/perstn Optional:
Option0: Pin V31/T29/W31
Option1 :Pin AJ26/AL26/AJ27
Option2: Pin AH25/AH26/AG26
Option3: Pin D25/C27/D26

RK3588

Note:
If Port0 and Port1 are not used,
Port0 and Port1 REF_CLKP/N: Leave floating or tie to VSS
Port0 and Port1 Other Signal: Leave floating
Port0 and Port1 Power: Leave floating or tie to VSS

If Port0 is used ,Port1 is not used,
Port1 REF_CLKP/N: Leave floating or tie to VSS
Port1 Other Signal: Leave floating
Port1 Power: Must supply power

If Port1 is used ,Port0 is not used,
Port0 REF_CLKP/N: Leave floating or tie to VSS
Port0 Other Signal: Leave floating
Port0 Power: Must supply power

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	18.RK3588_PCIE30/PCIE20/SATA30				
Date:	Wednesday, October 12, 2022		Rev:	V1.3	
Designed by:	RZF	Reviewed by:		Sheet:	18 of 99

RK3588_J(VCCIO5 Domain)

U1000J

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

RK3588

RK3588_K(VCCIO6 Domain)

U1000K

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

RK3588

RK3588_I(VCCIO4 Domain)

U1000I

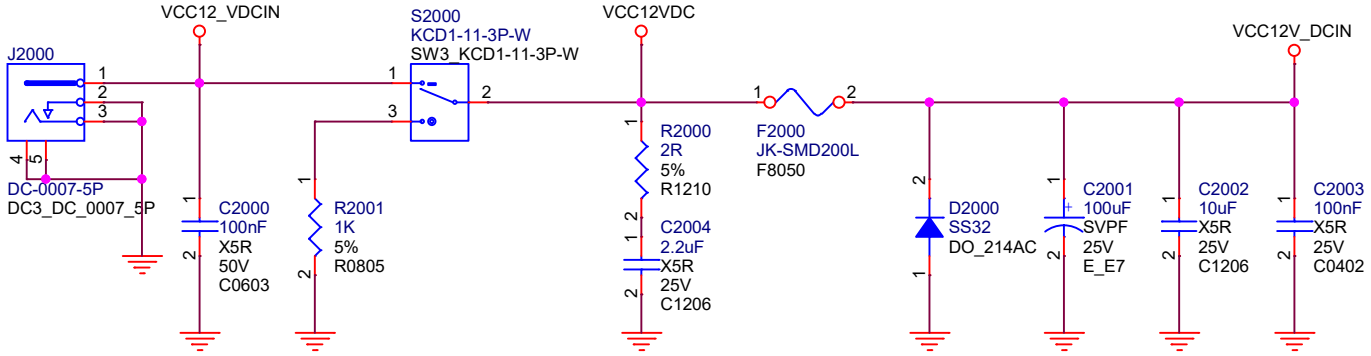
VCCIO4 Domain

Operating Voltage=1.8V/3.3V

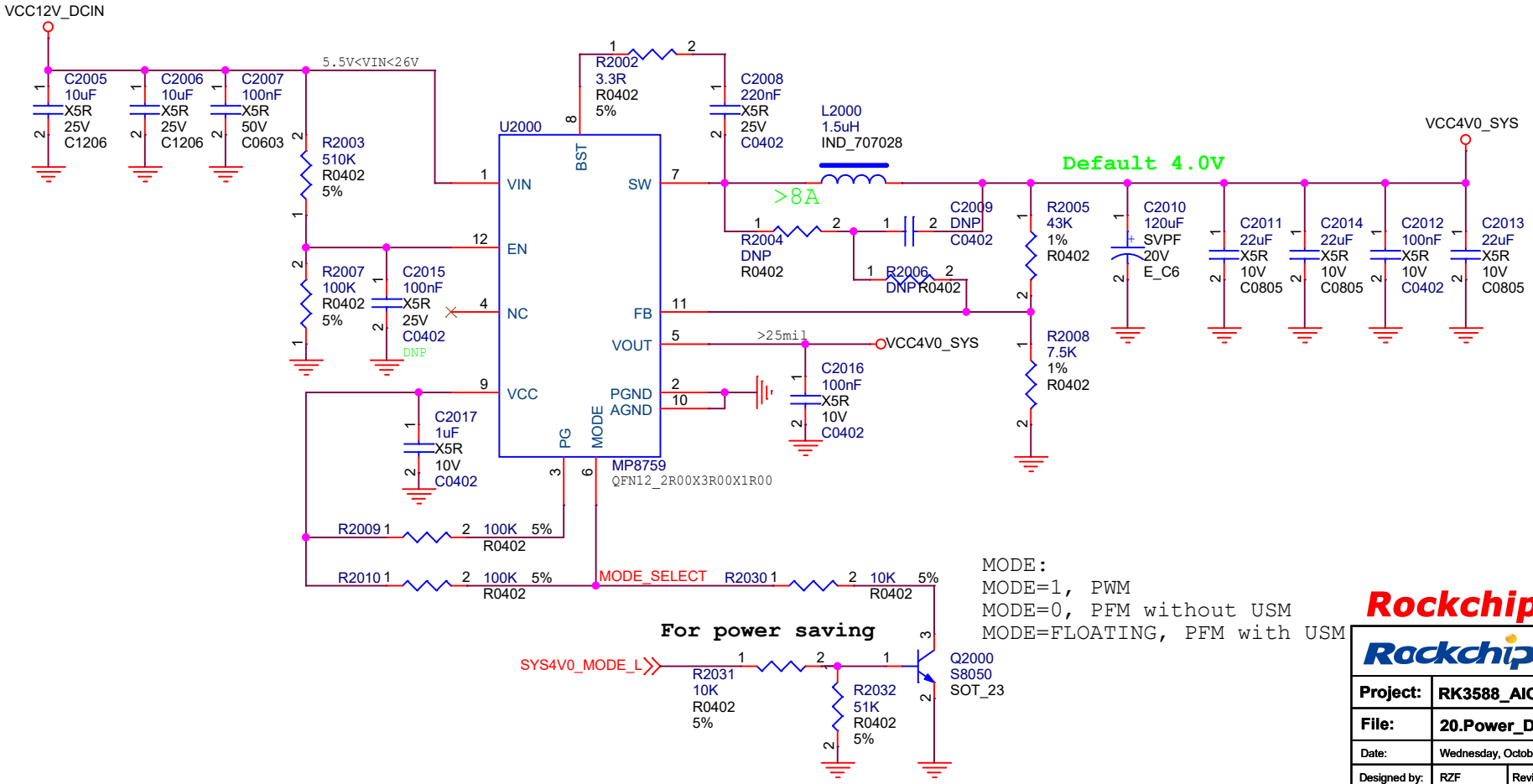
RK3588

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588_AIOT_SCH
File:	19.RK3588_1.8V/ 3.3V GPIO
Date:	Wednesday, October 12, 2022
Rev:	V1.3
Designed by:	RZF
Reviewed by:	
Sheet:	19 of 99

12V DCIN



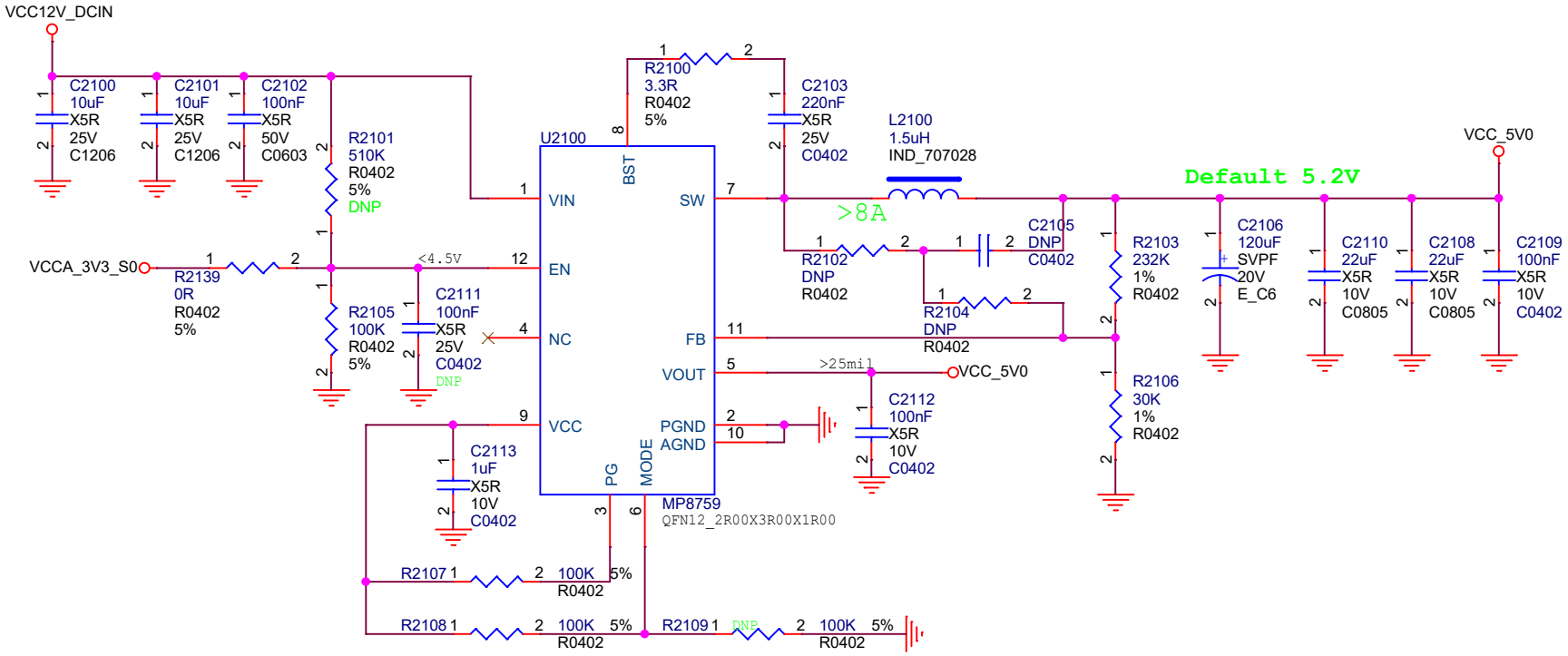
VCC4V0_SYS



Rockchip Confidential

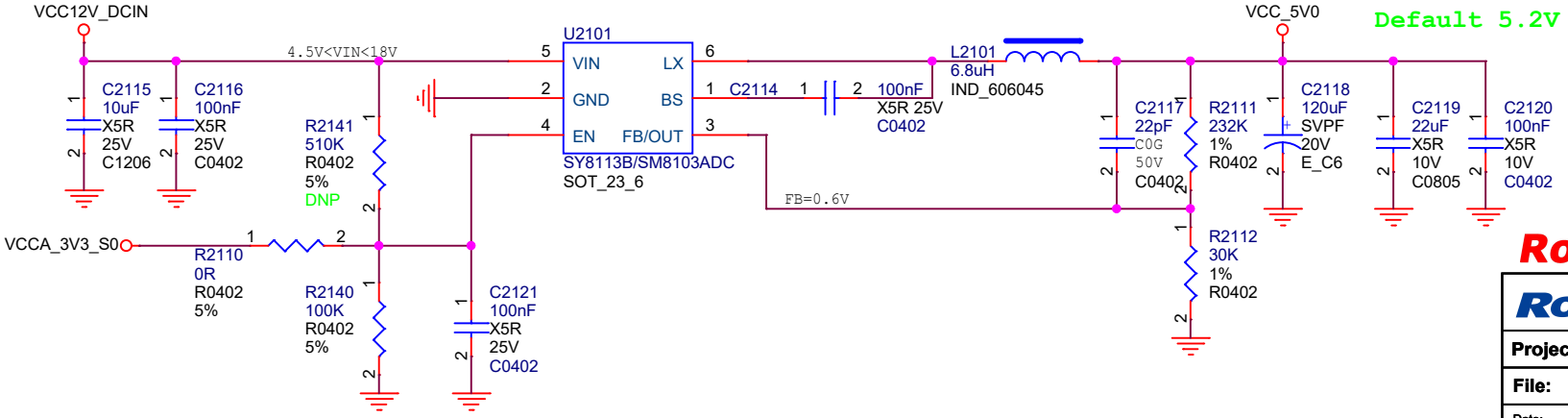
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	20.Power_DC IN/VCC4V0_SYS				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:	Default	Sheet:	20 of 99

VCC5V0_SYS
OPTION1:Output Support 5V/8A



Note:
DCDC power supply is recommended if the current exceeds 3A

VCC5V0_SYS
OPTION2:Output Support 5V/3A

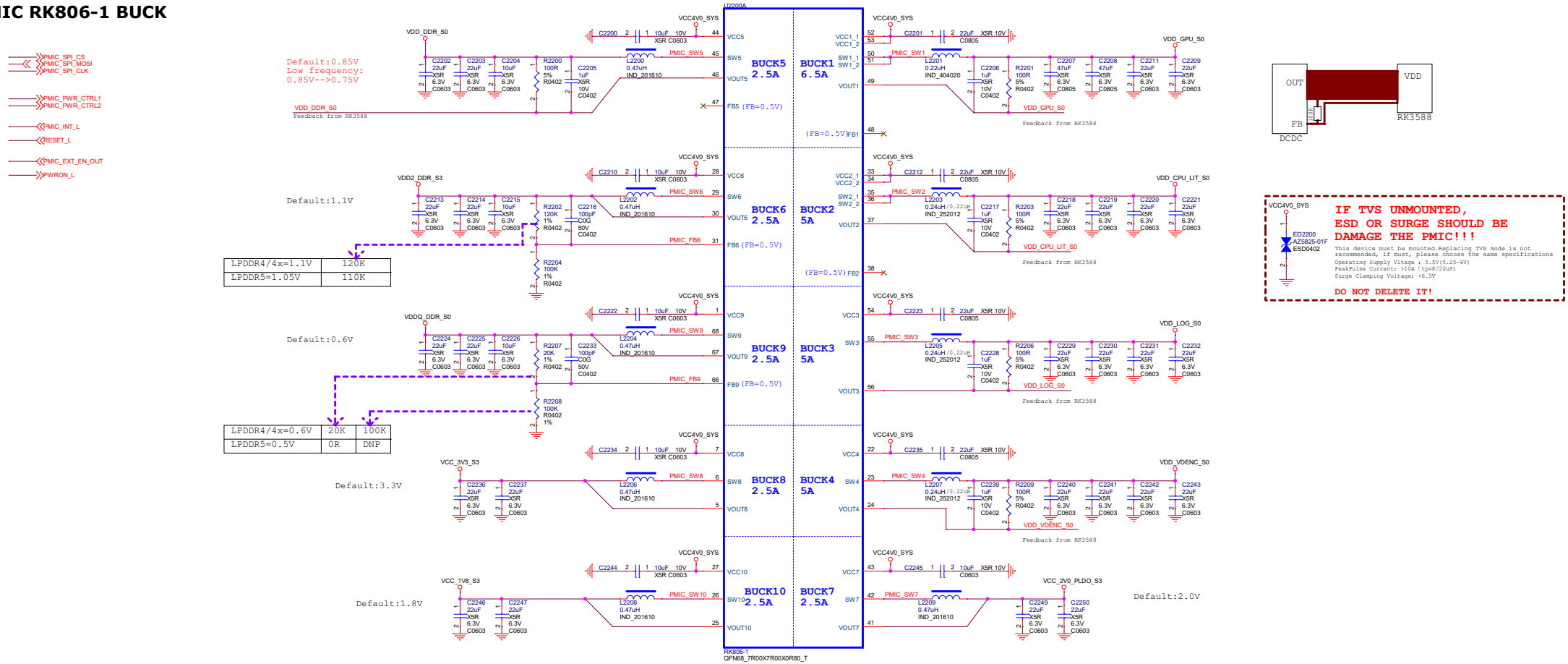


Note:
DCDC power supply is recommended if the current below 3A

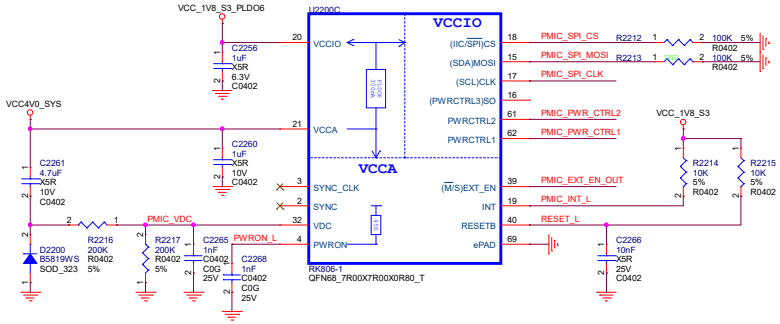
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	21.Power_Ext VCC_5V0				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:	<Checker>	Sheet:	21 of 99

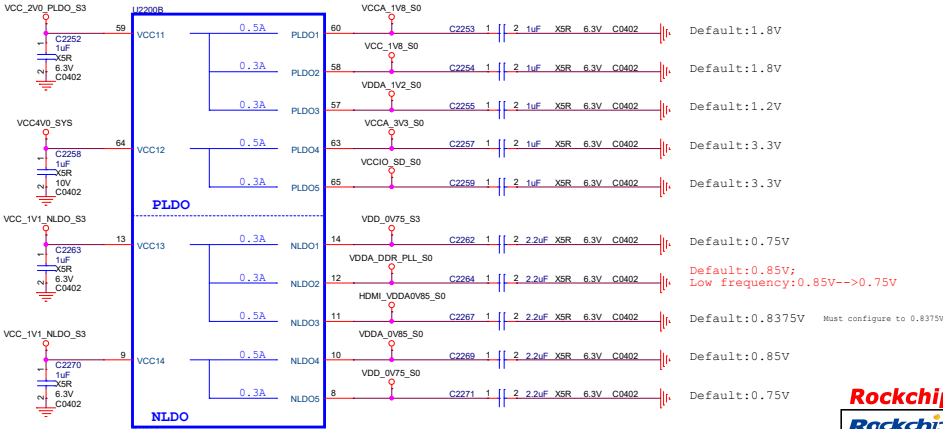
PMIC RK806-1 BUCK



PMIC RK806-1 Managerment

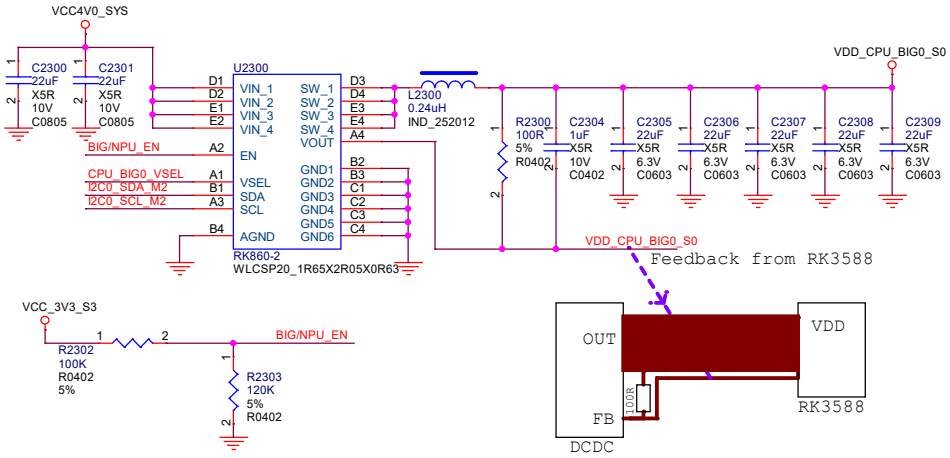


PMIC RK806-1 LDO

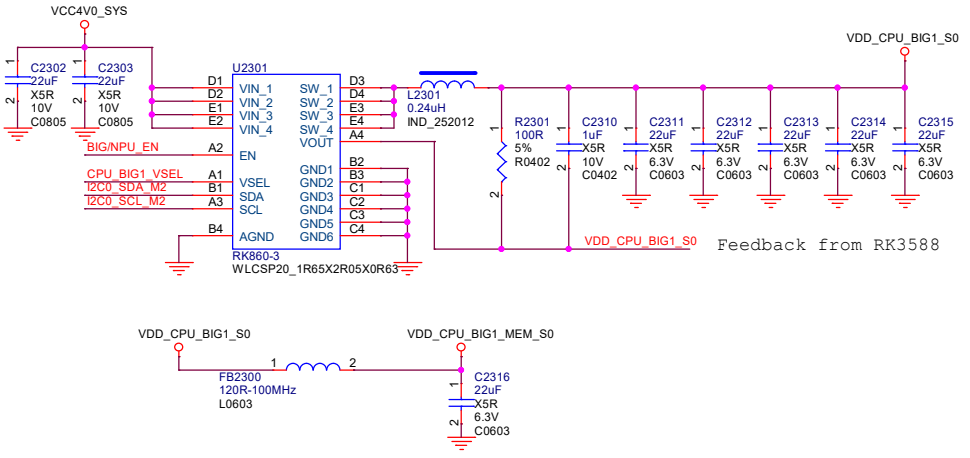


Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	22.Power-PMIC_RK806-1		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
Designed by:	RZF	Reviewed by: Default	Sheet: 22 of 99

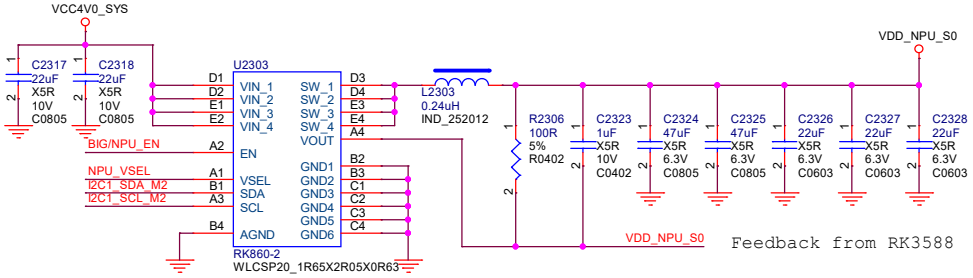
VDD_CPU_BIG0



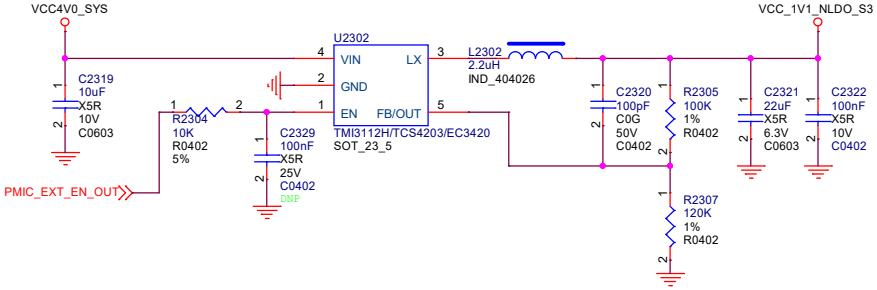
VDD_CPU_BIG1

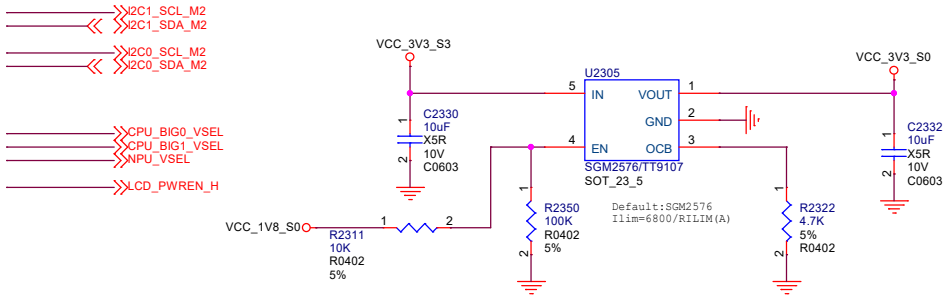


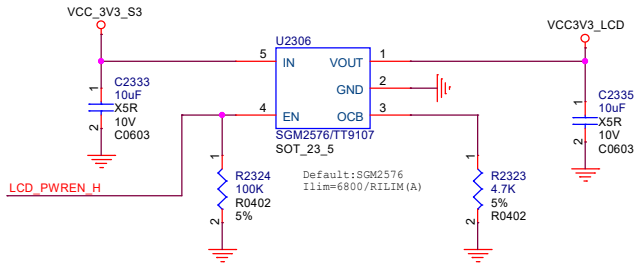
VDD_NPU



VCC_1V1_NLDO_S3



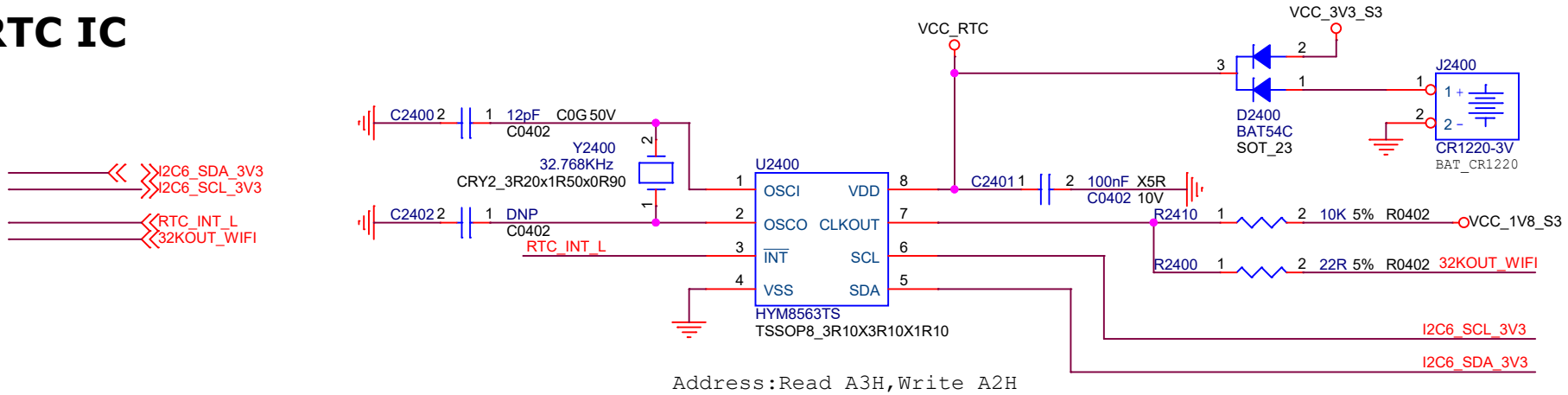




Rockchip Confidential

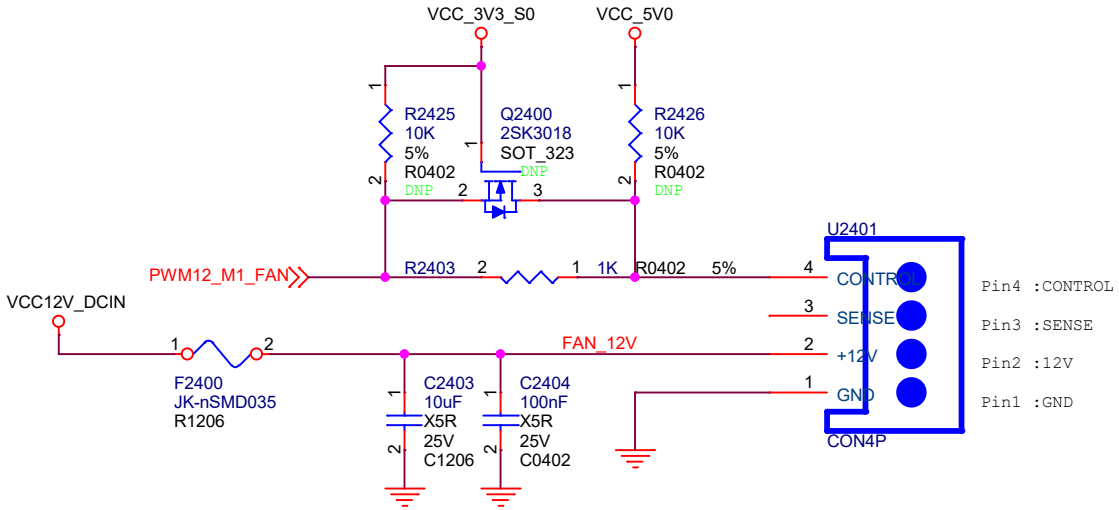
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	23.Power_Ext Discrete				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:	Default	Sheet:	23 of 99

RTC IC

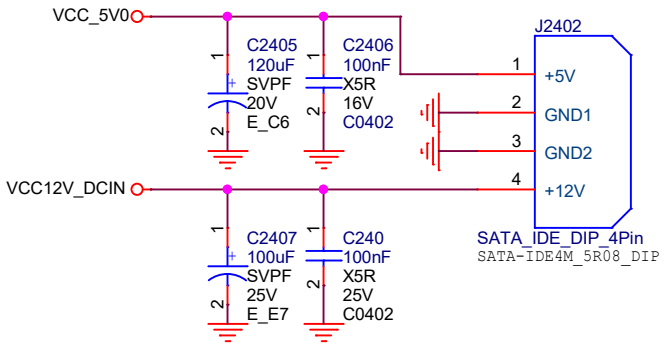


Address:Read A3H,Write A2H

FAN_POWER



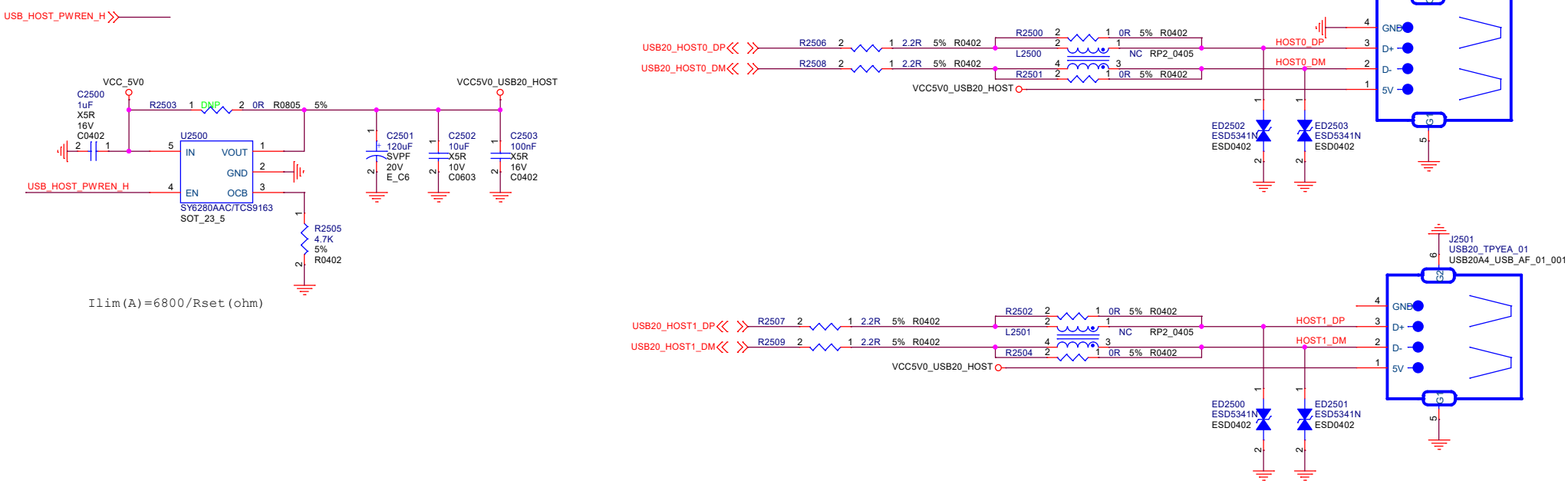
SATA_POWER



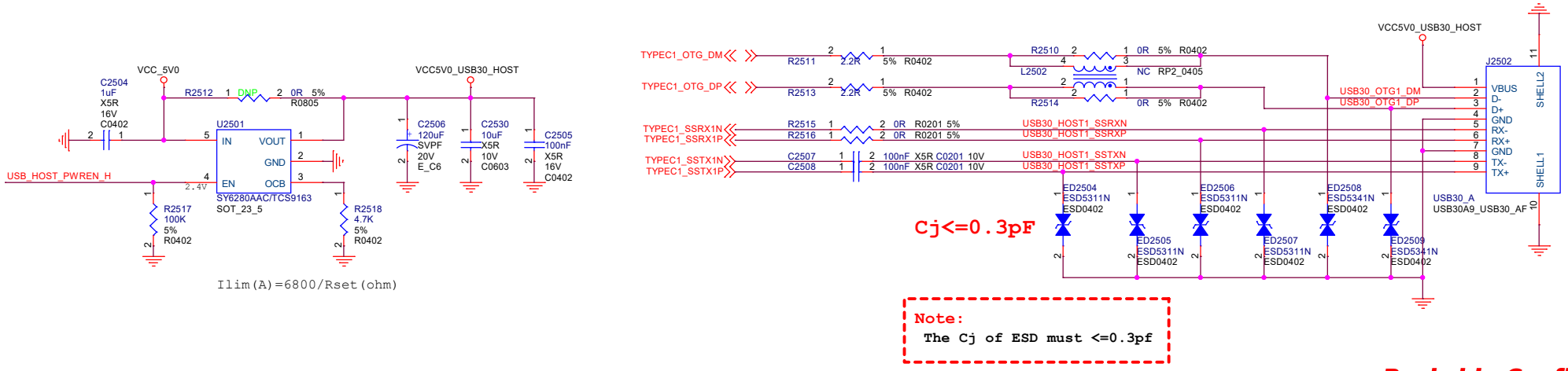
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	24.RTC/FAN/SATA POWER				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:		Sheet:	24 of 99

USB2.0 HOST PORT



USB3.0 HOST PORT

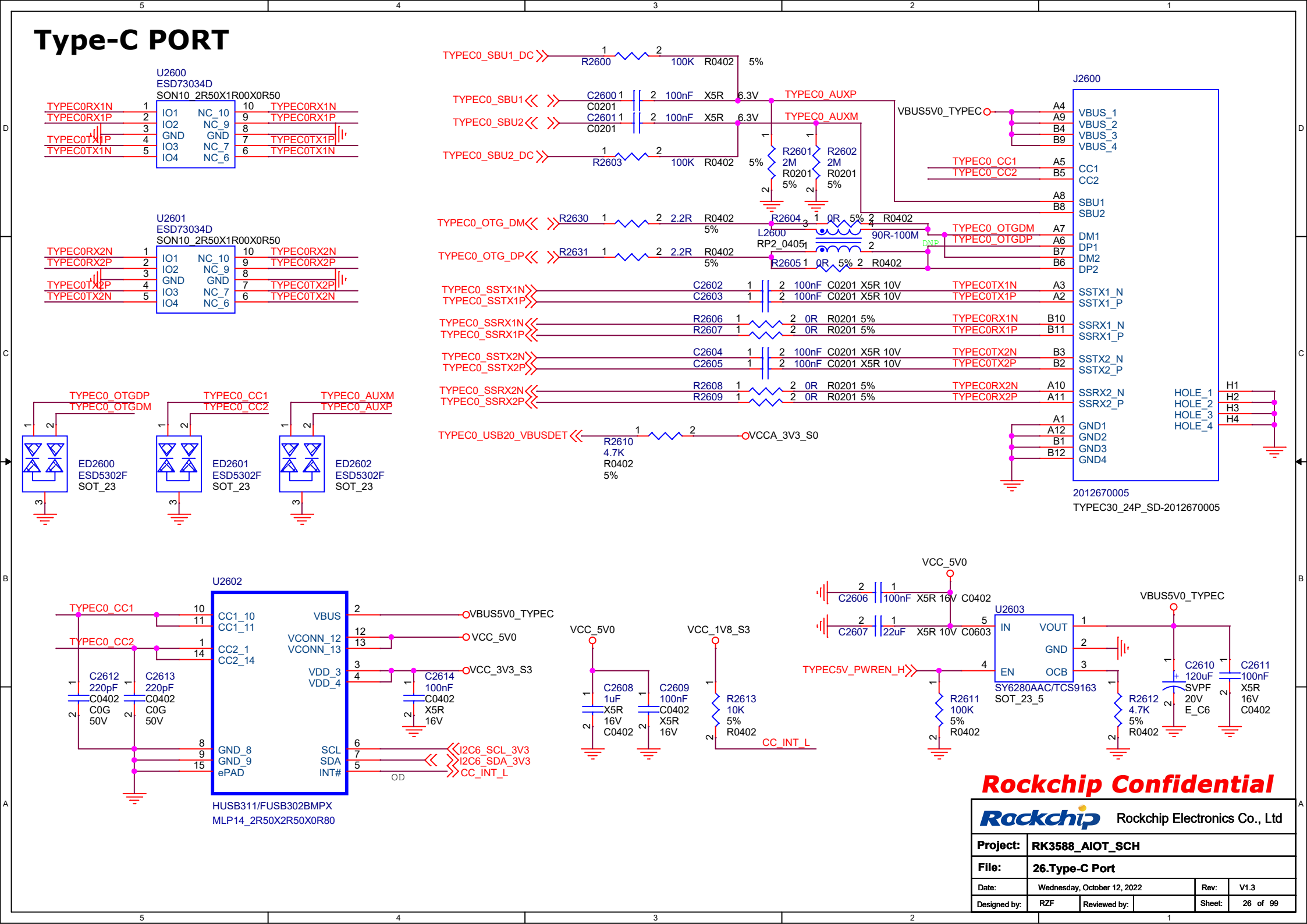


Note:
The Cj of ESD must <=0.3pf

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	25.USB20/USB30 Port				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:		Sheet:	25 of 99

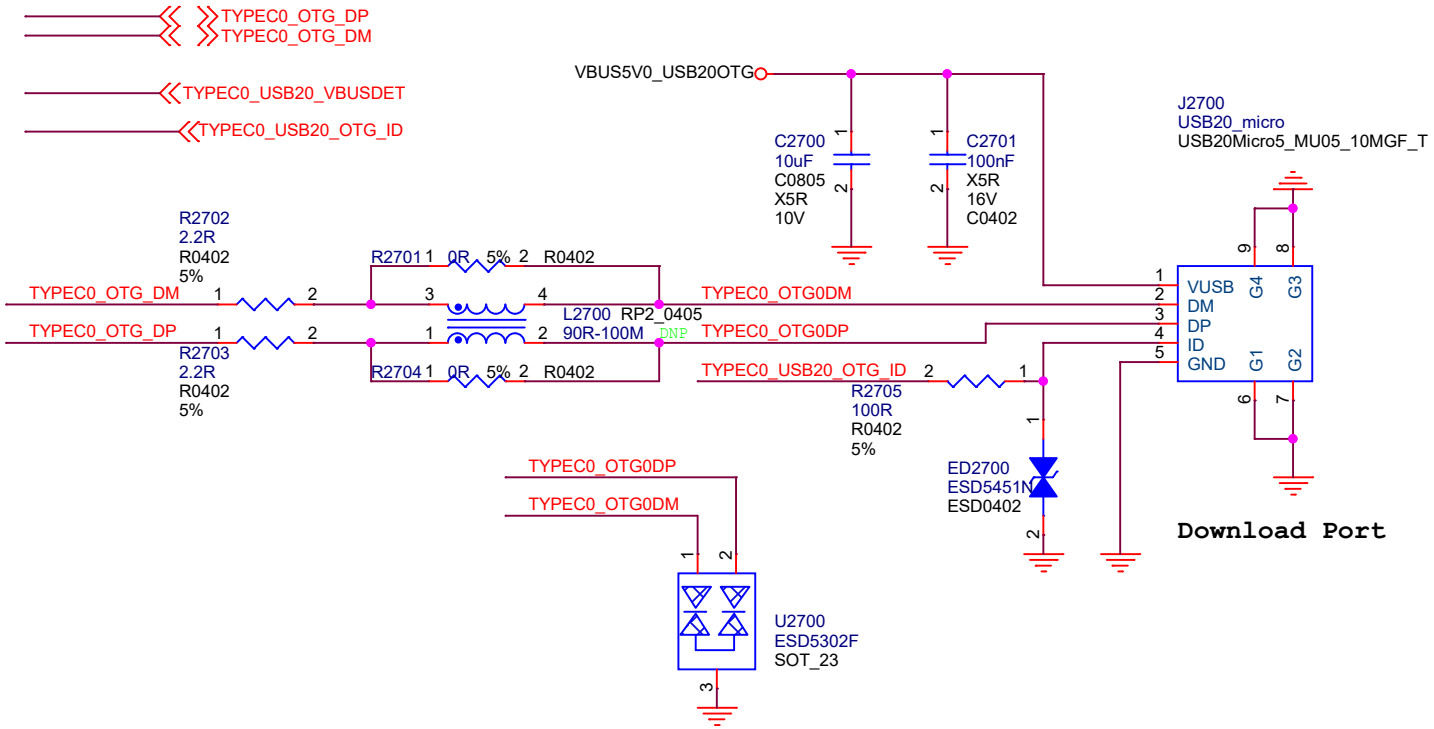
Type-C PORT



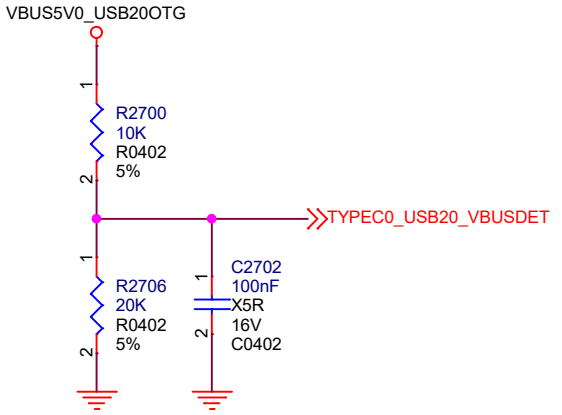
Rockchip Confidential

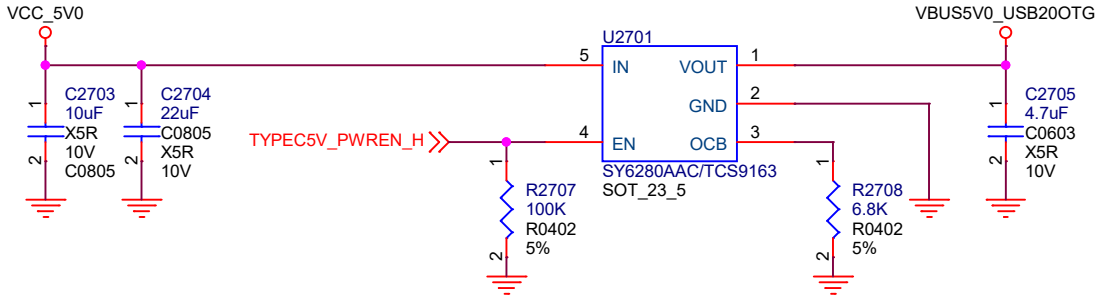
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	26.Type-C Port		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
Designed by:	RZF	Reviewed by:	Sheet: 26 of 99

USB2.0 Micro Port



USB Detection

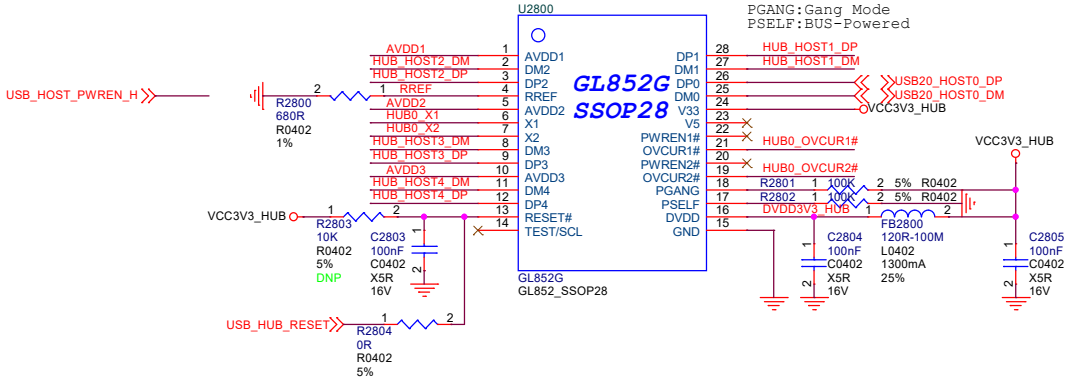




Rockchip Confidential

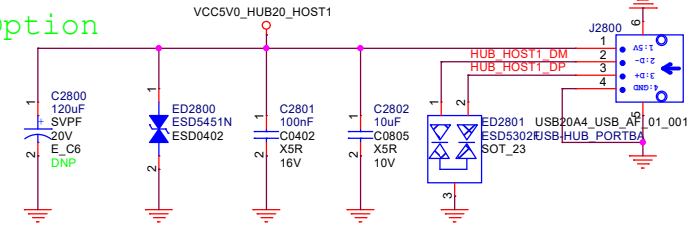
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	27.USB2.0 Micro Port(option)				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:		Sheet:	27 of 99

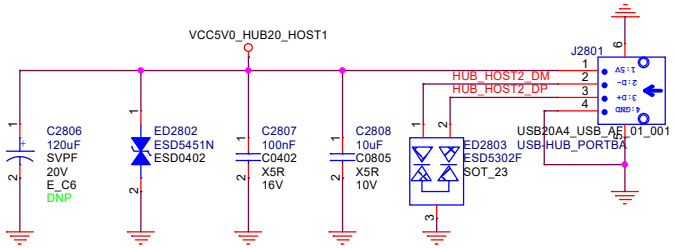
USB2.0 HUB

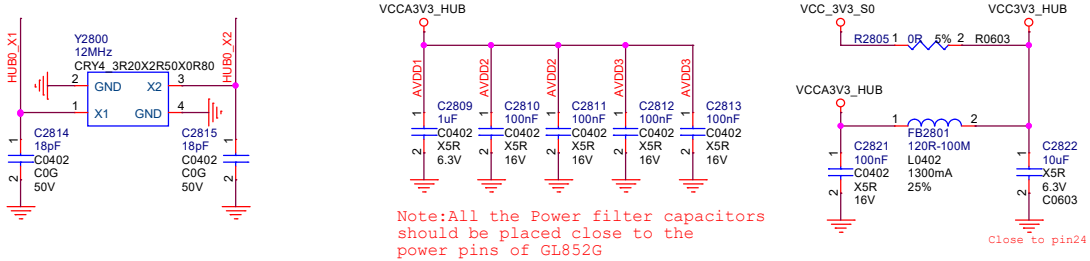


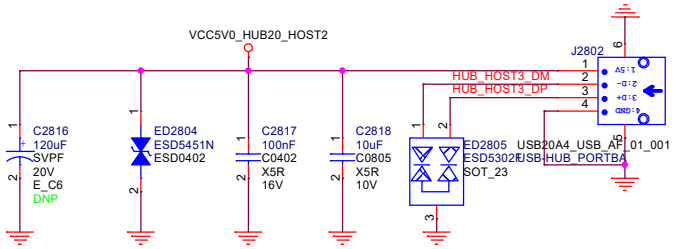
Note:
Used ECAP if want to drive mobile hard-disk and enough structure space for place.

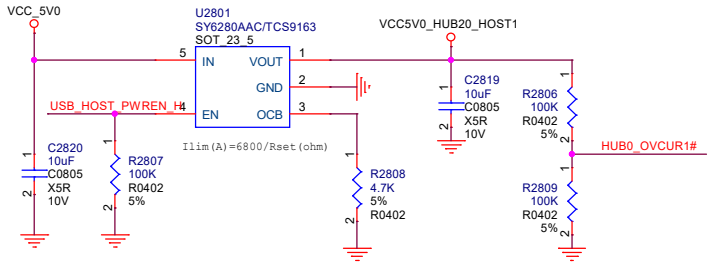
Option

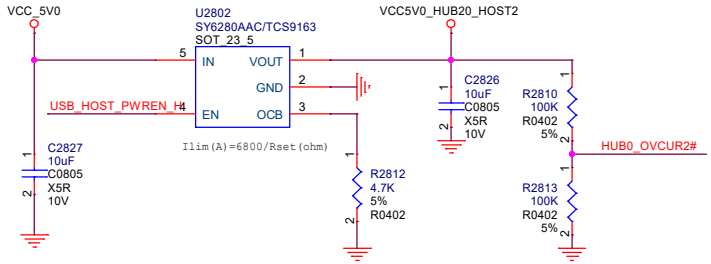


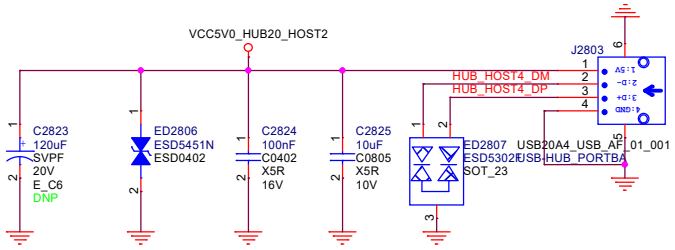








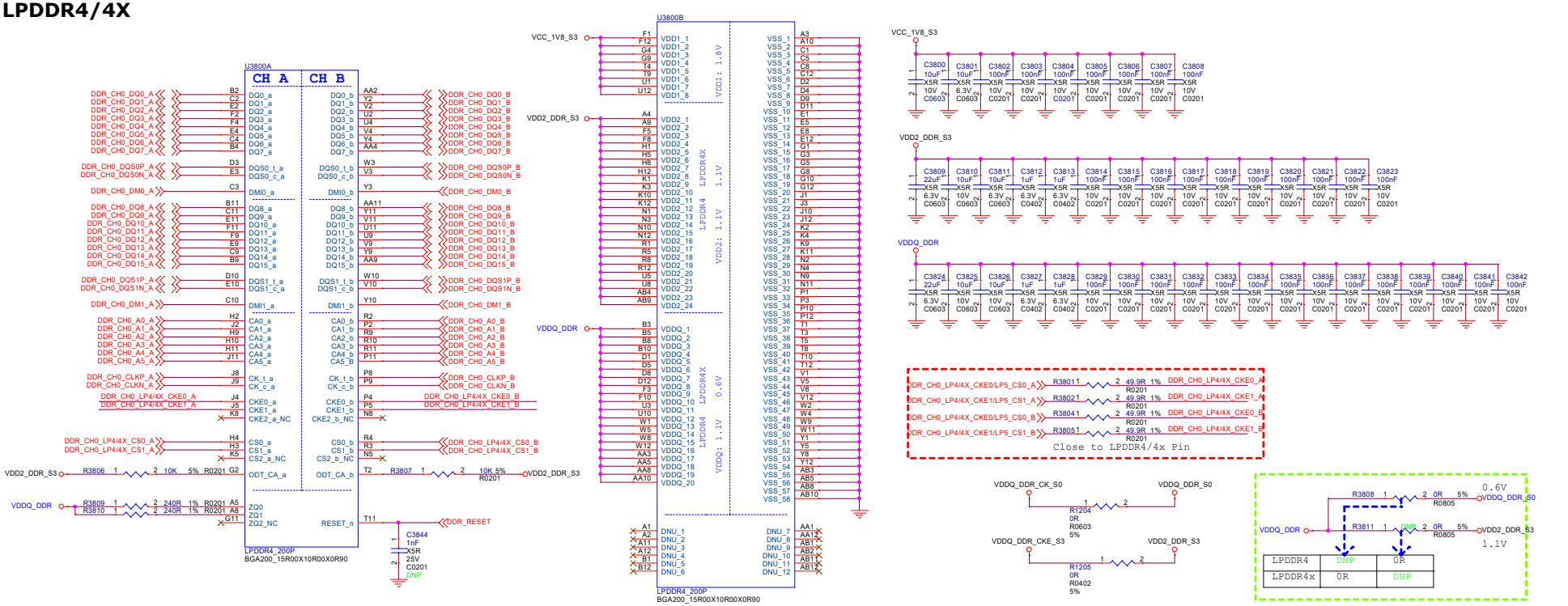


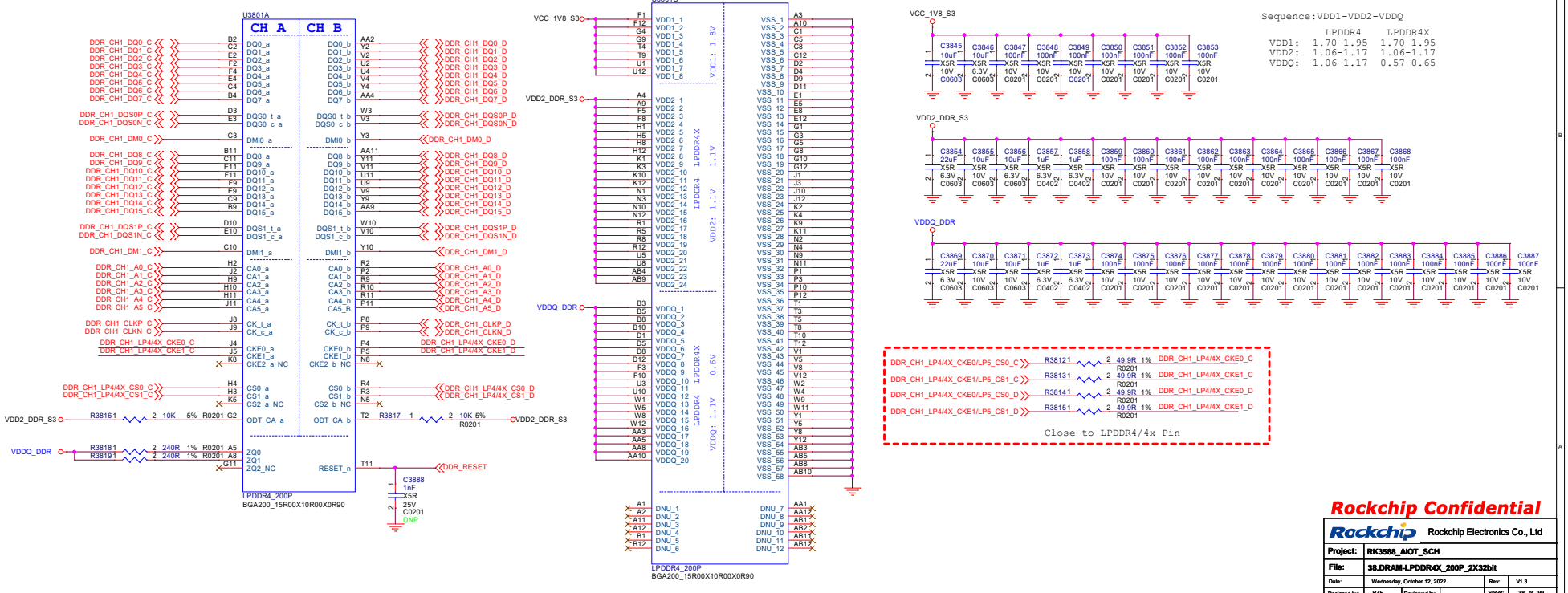


Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	28.USB HUB GL85x (option)				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:		Sheet:	28 of 99

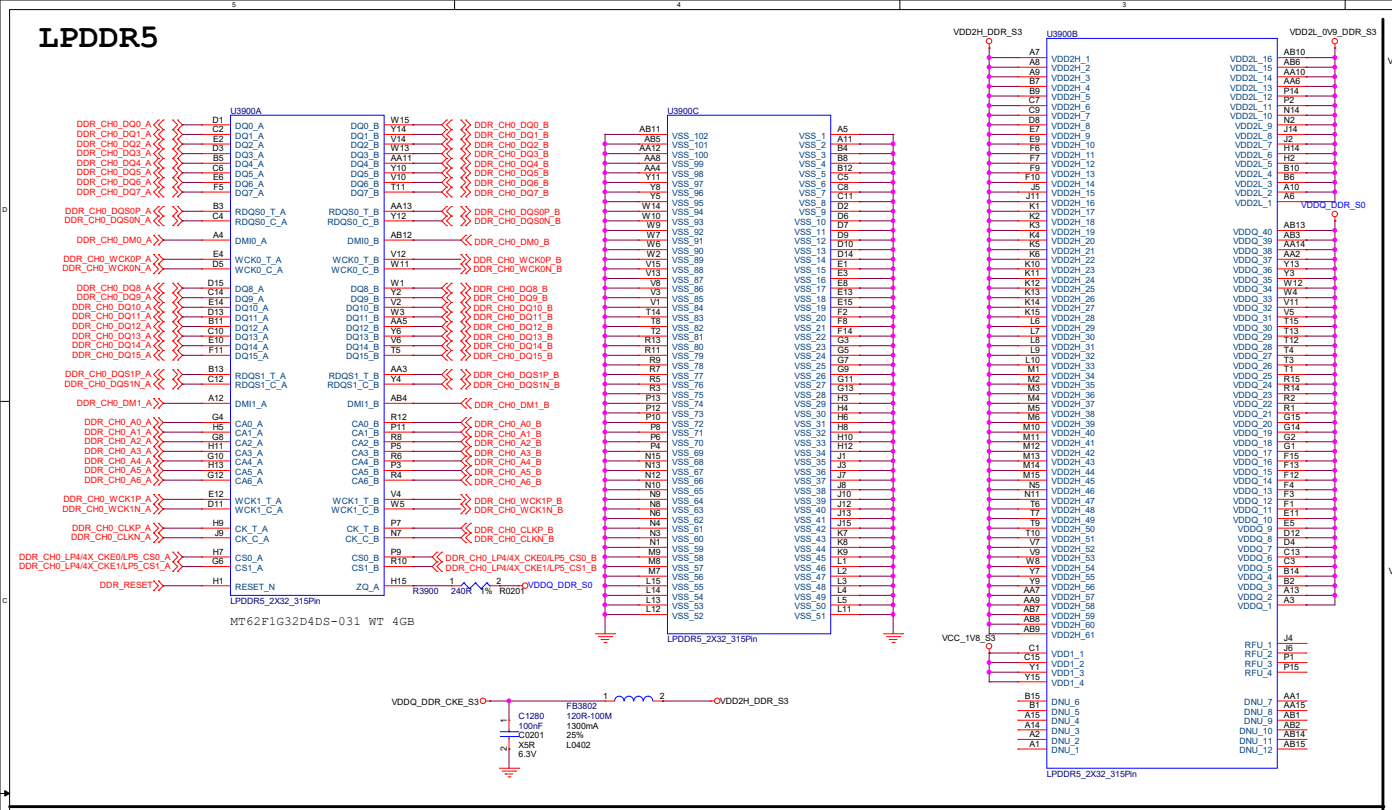
LPDDR4/4X

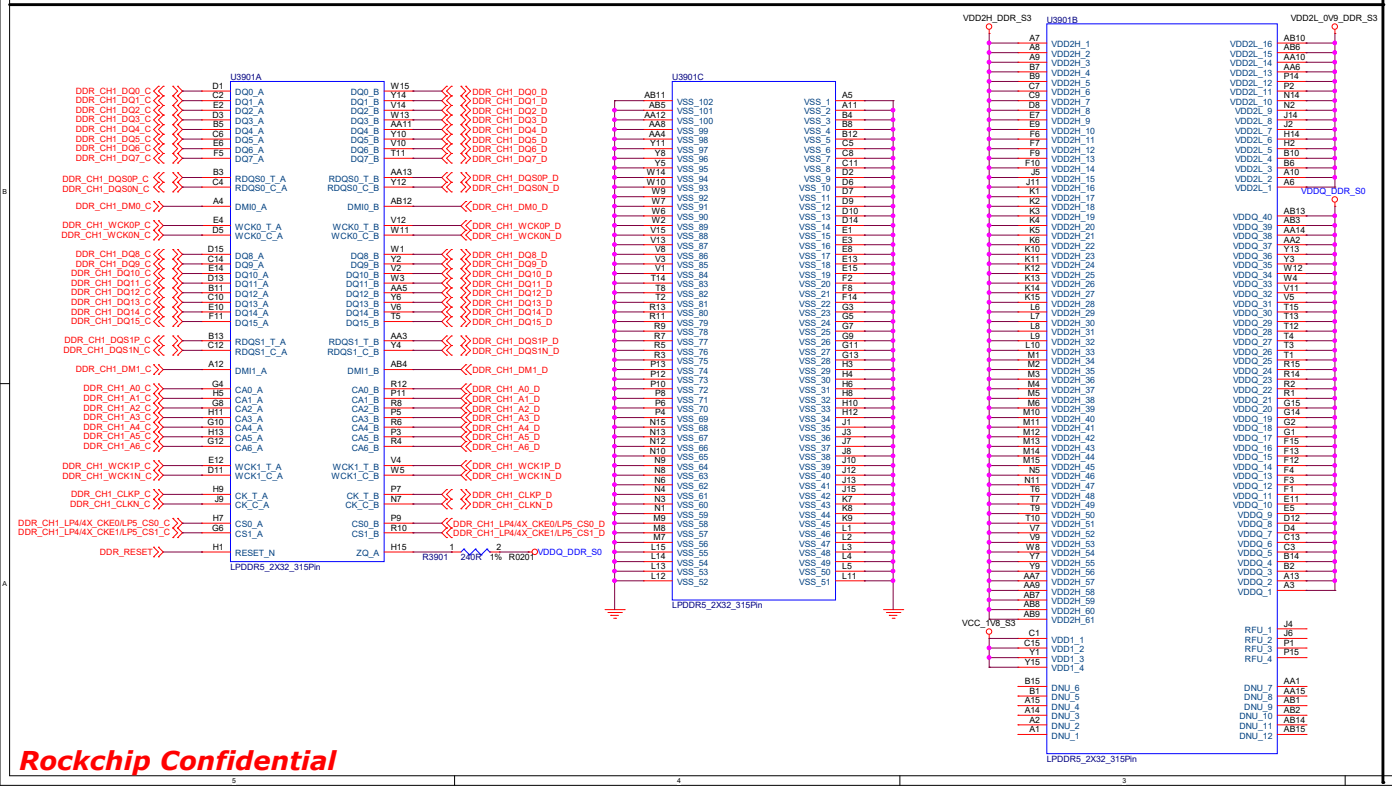


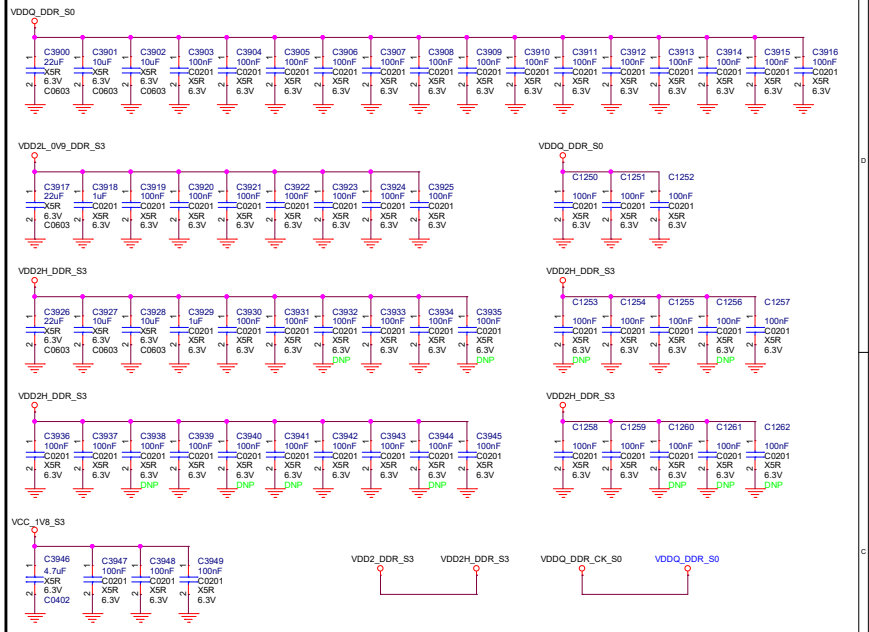


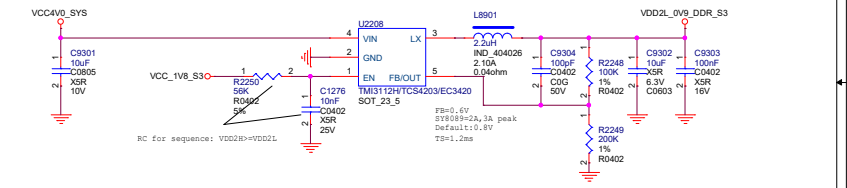
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588_AIOT_SCH
File:	38.DRAM-LPDDR4X_200P_2X32bit
Date:	Wednesday, October 12, 2022
Rev:	V1.3
Designed by:	RZF
Reviewed by:	
Sheet:	38 of 99

LPDDR5

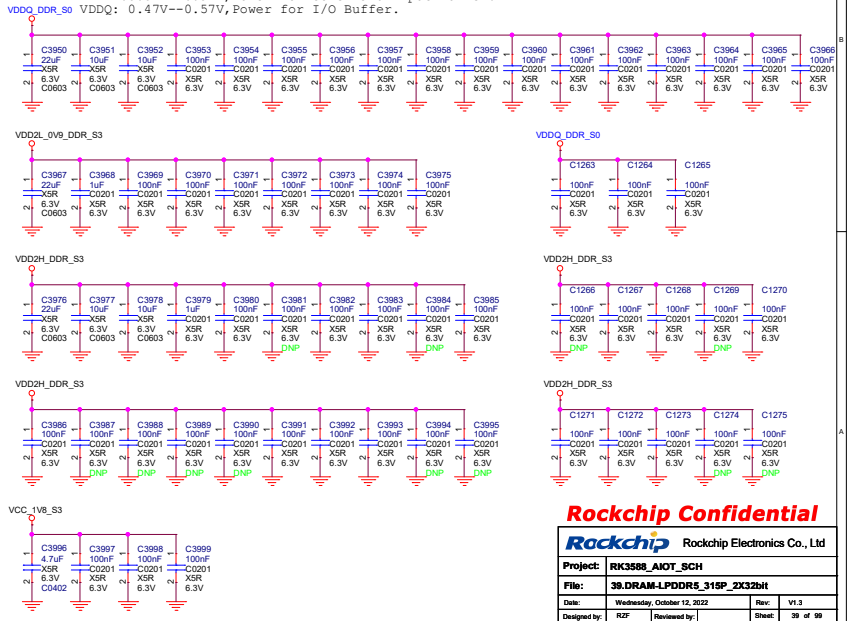








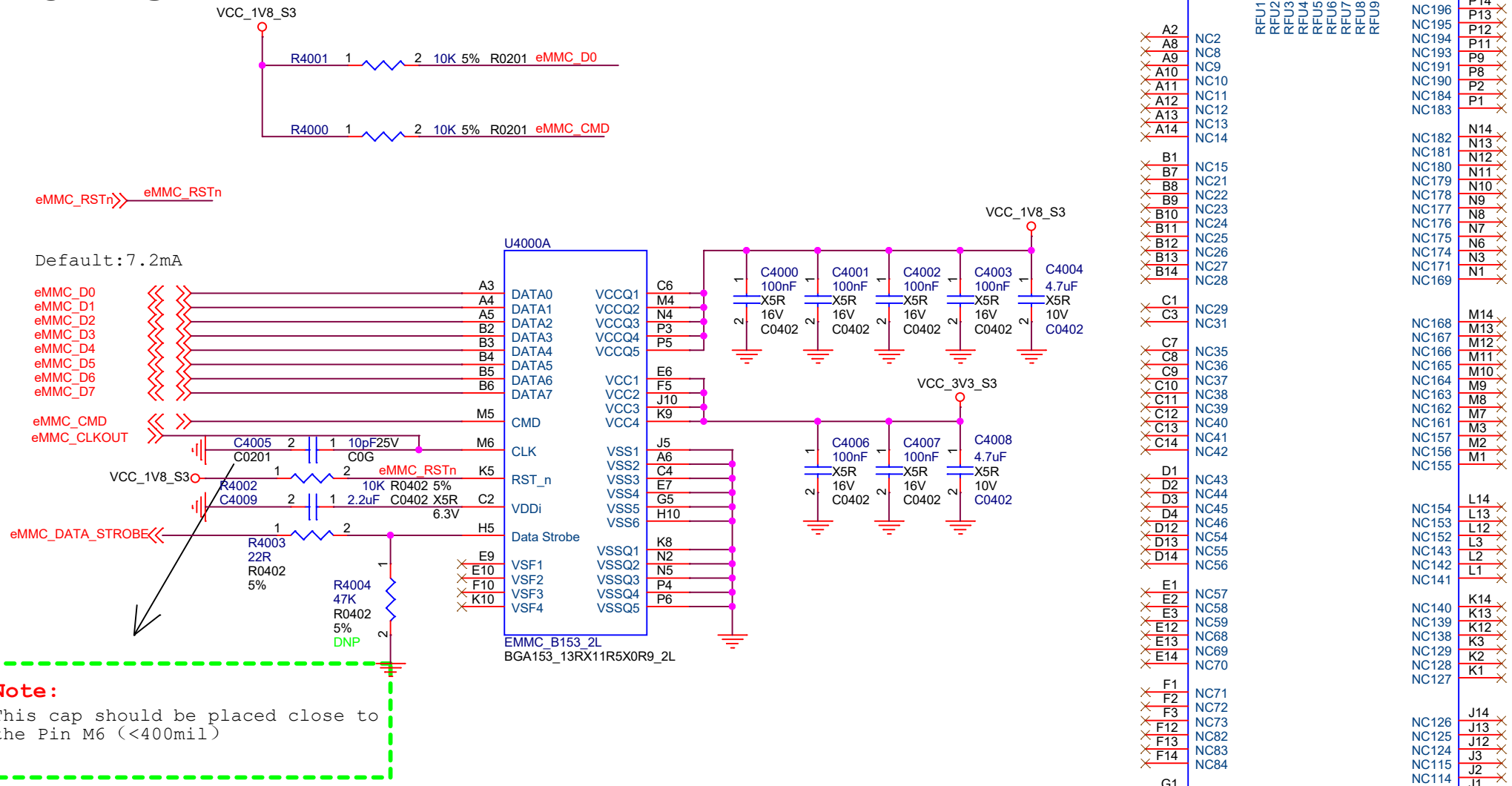
Power Sequence: VDD1>VDD2H>=VDD2L>VDDQ-200mV
VDD1: 1.70V--1.95V,Power for core1.
VDD2H:1.01V--1.12V,Power for core2 and Input Buffer.
VDD2L:0.87V--0.97V,Power for core2 and Input Buffer.
VDDQ: 0.47V--0.57V,Power for I/O Buffer.



Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	39.DRAM-LPDDR5_315P_2X32bit		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
Designed by:	RZF	Reviewed by:	Sheet: 39 of 99

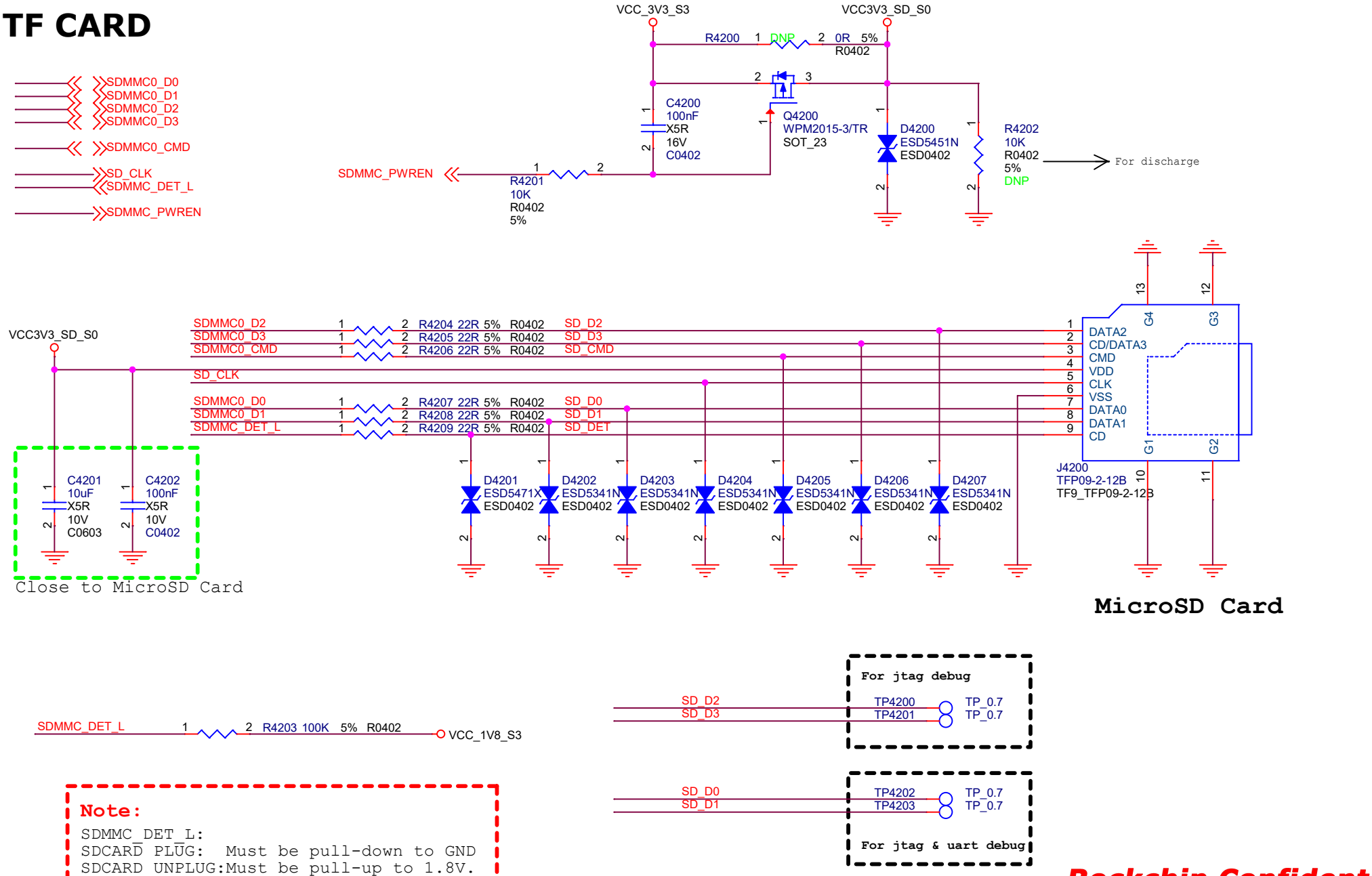
Rockchip Confidential

eMMC FLASH



Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	40.Flash-eMMC Flash		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
Designed by: RZF	Reviewed by:	Sheet:	40 of 99

TF CARD



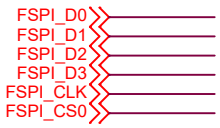
Note:

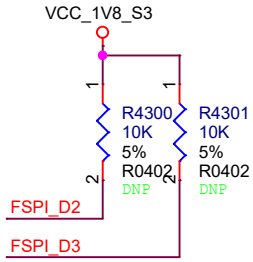
SDMMC_DET_L:
SDCARD PLUG: Must be pull-down to GND
SDCARD UNPLUG:Must be pull-up to 1.8V.

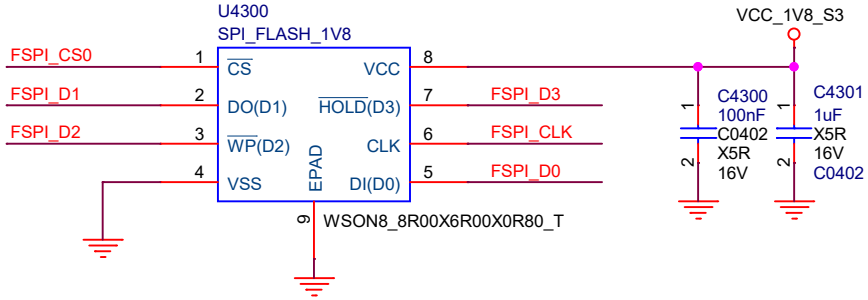
Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	42.Flash-TF Card		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
Designed by: RZF	Reviewed by:	Sheet:	42 of 99

Rockchip Confidential

SPI NOR OR NAND Flash







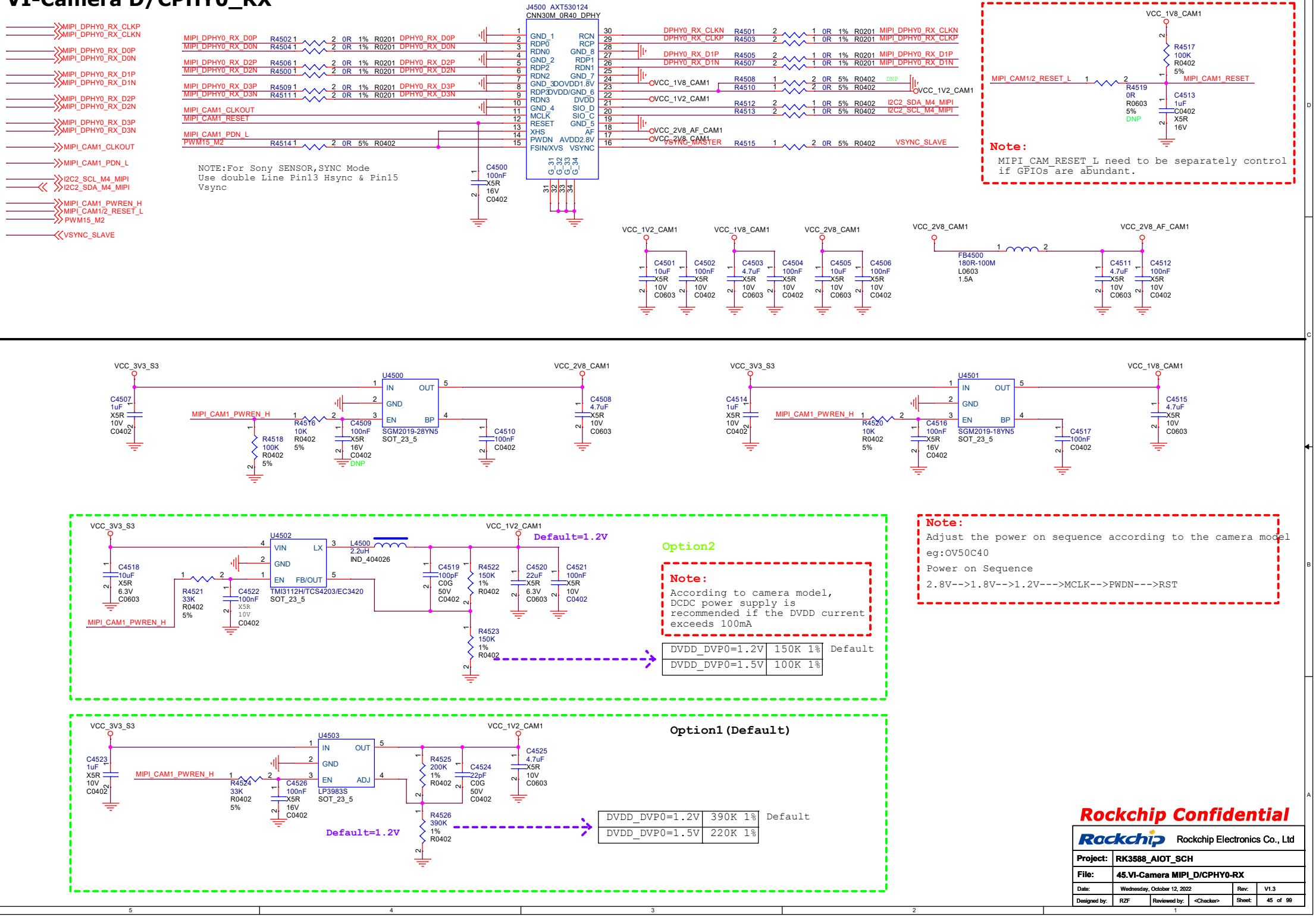
SPI FLASH:1.8V

Note:
When using SPI FLASH with only 1 bit, it needs to be stuffed.

Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	43.Flash-SPI FLASH(option)				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:		Sheet:	43 of 99

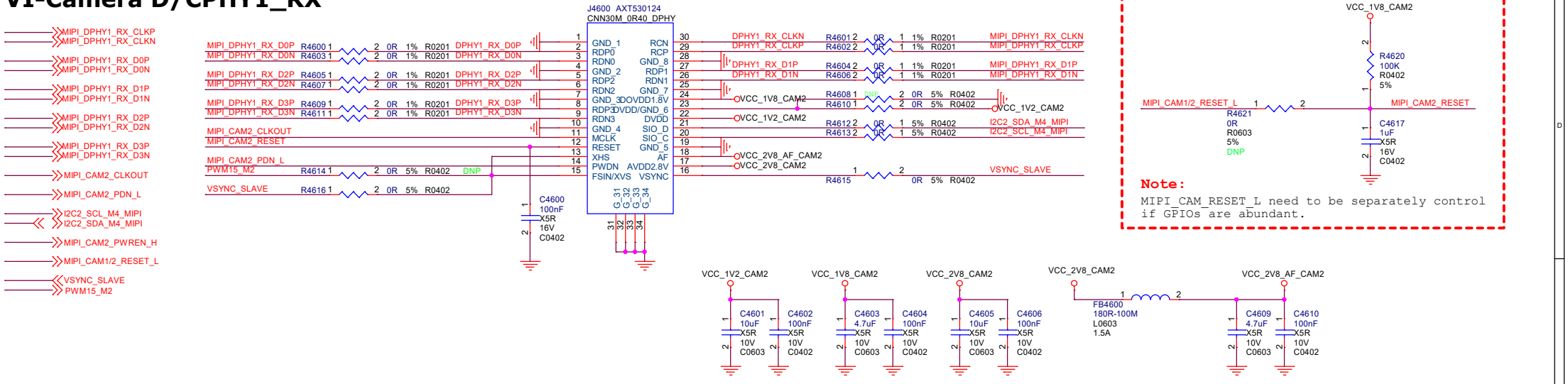
VI-Camera D/CPHY0_RX

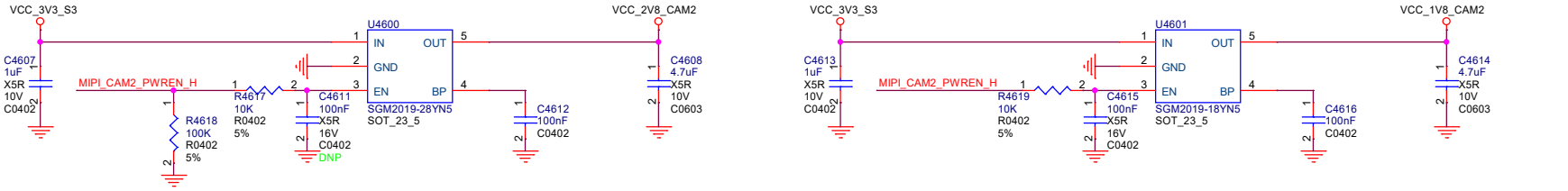


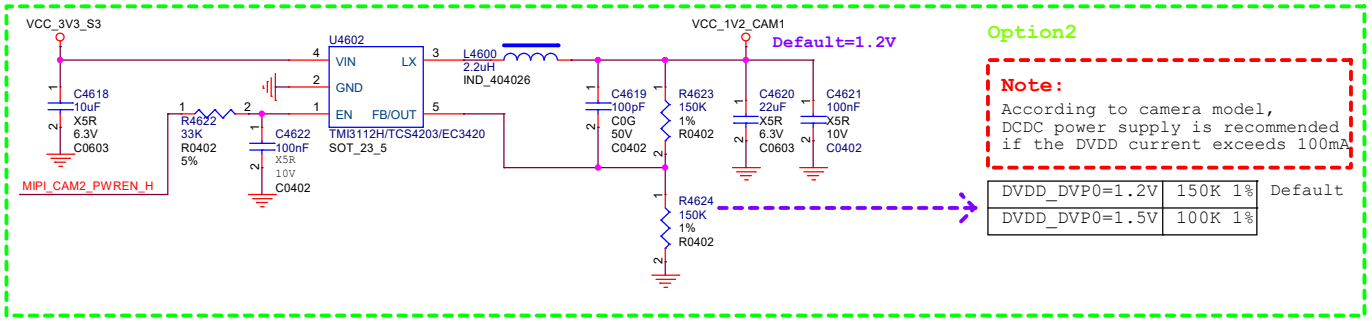
Rockchip Confidential

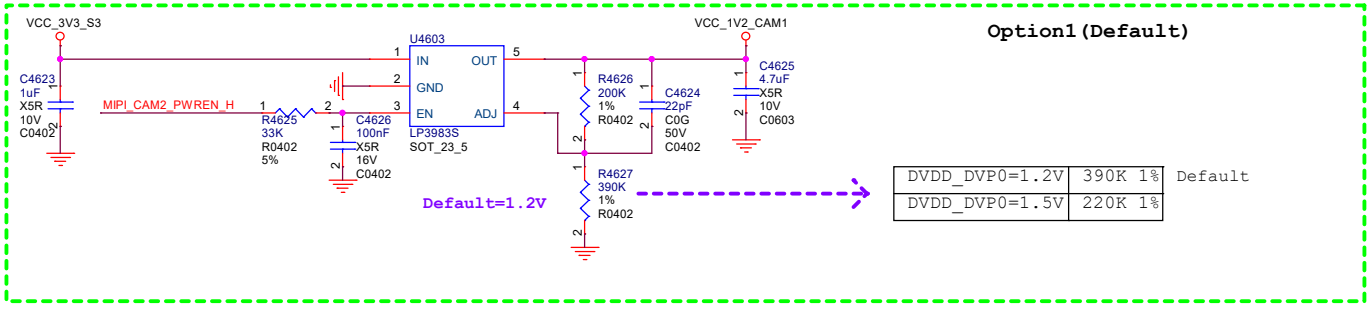
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	45.VI-Camera MIPI_D/CPHY0-RX				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:	<Checker>	Sheet:	45 of 99

VI-Camera D/CPHY1_RX







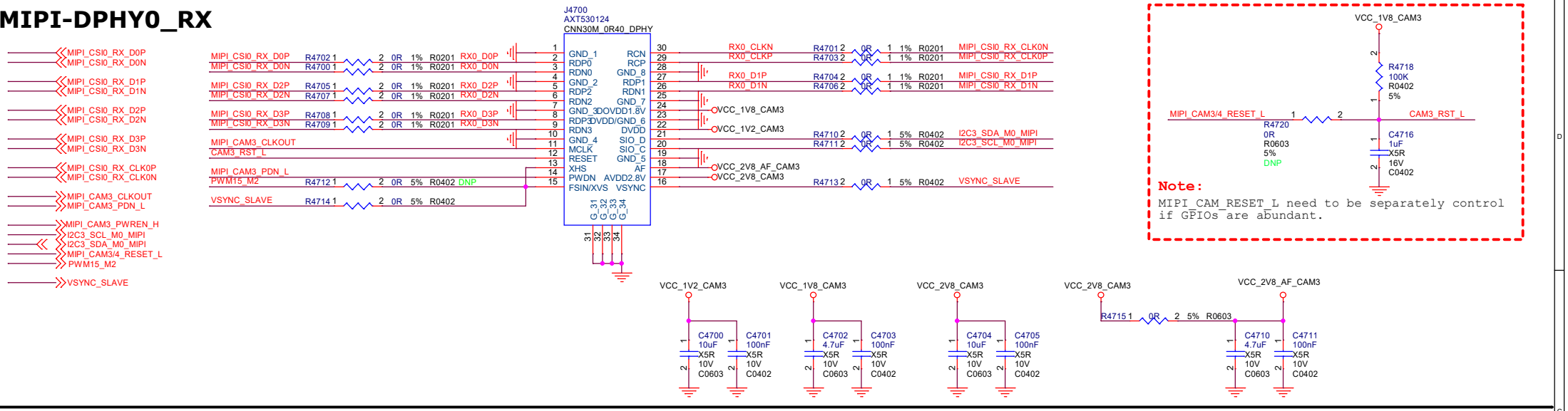


Note:
Adjust the power on sequence according to the camera model
eg:OV50C40
Power on Sequence
2.8V-->1.8V-->1.2V--->MCLK-->PWDN--->RST

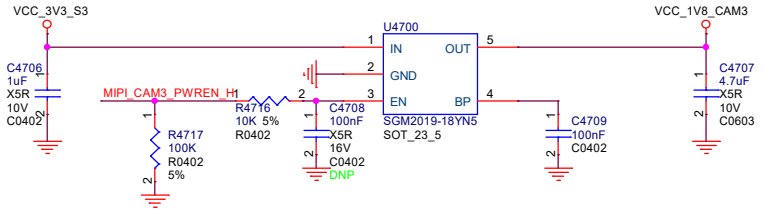
Rockchip Confidential

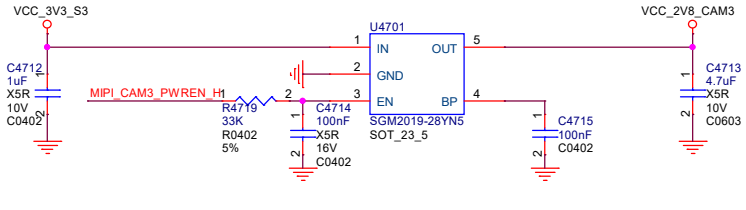
Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	46.VI-Camera MIPI_D/CPHY1-RX				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:	<Checker>	Sheet:	46 of 99

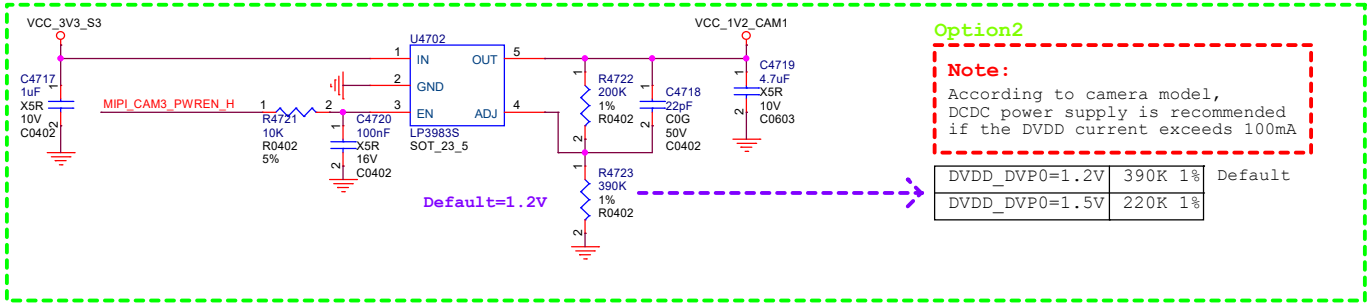
MIPI-DPHY0_RX



Note:
MIPI_CAM_RESET_L need to be separately control if GPIOs are abundant.







Option2

Note:
According to camera model, DCDC power supply is recommended if the DVDD current exceeds 100mA

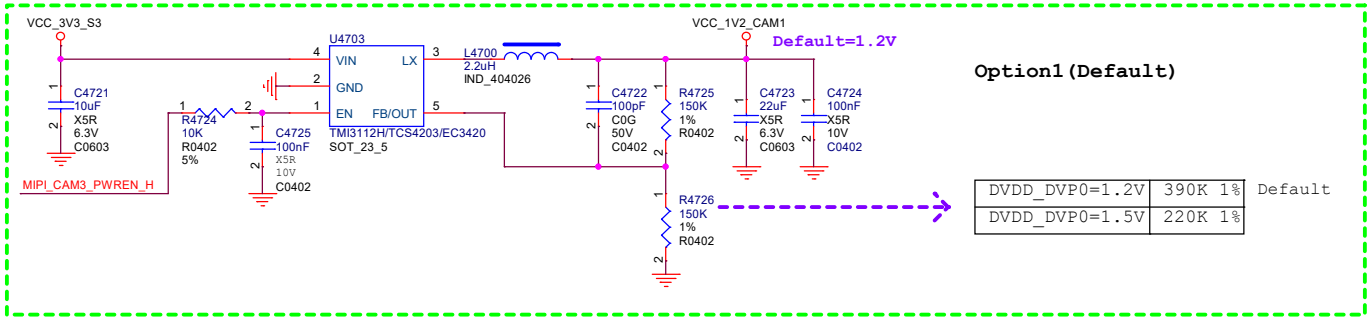
DVDD_DVP0=1.2V	390K 1%	Default
DVDD_DVP0=1.5V	220K 1%	

Note:
Adjust the power on sequence according to the camera model

eg:GC8034

Power on Sequence

1.8V-->1.2V-->2.8V--->MCLK-->PWDN--->RST



Option1(Default)

DVDD_DVP0=1.2V	390K 1%	Default
DVDD_DVP0=1.5V	220K 1%	

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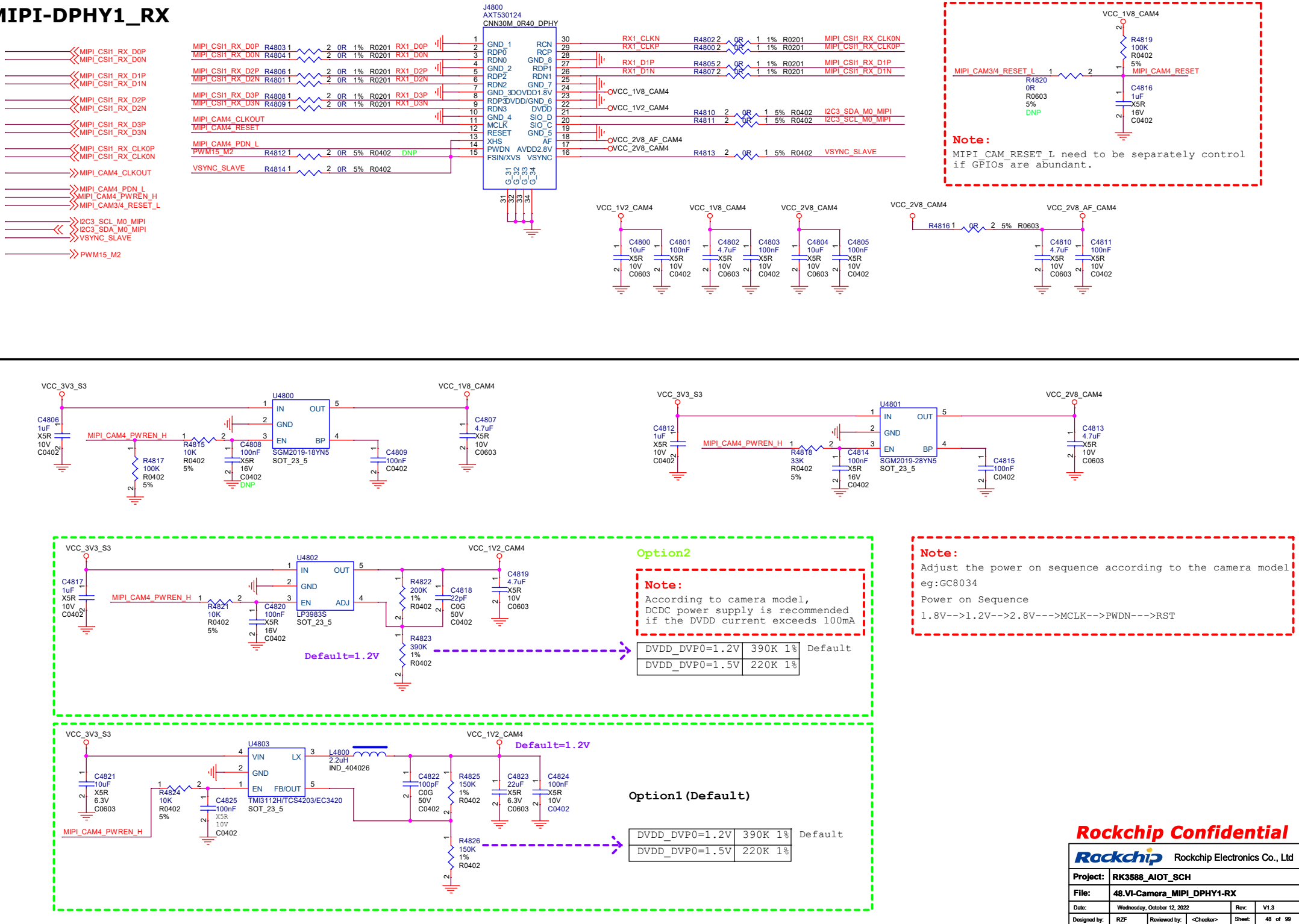
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	47.VI-Camera_MIPI_DPHY0-RX				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:	<Checker>	Sheet:	47 of 99

MIPI-DPHY1_RX



Note:
Adjust the power on sequence according to the camera model
eg:GC8034
Power on Sequence
1.8V-->1.2V-->2.8V--->MCLK-->PWDN--->RST

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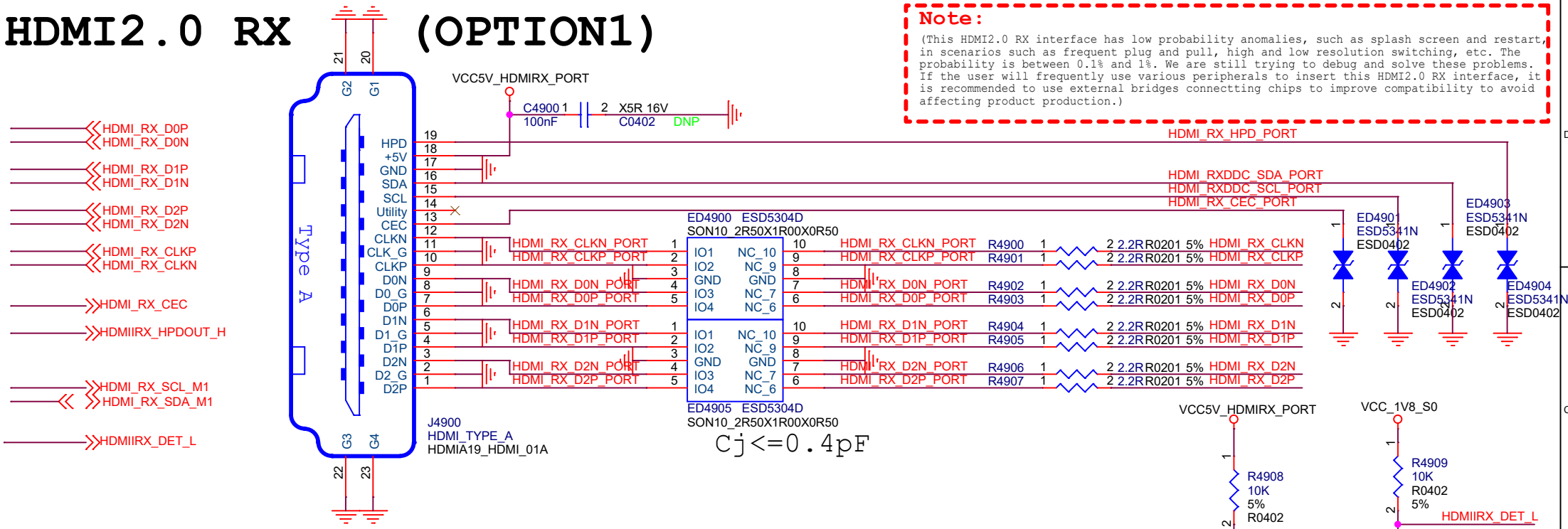
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	48.VI-Camera_MIPI_DPHY1-RX				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:	<Checker>	Sheet:	48 of 99

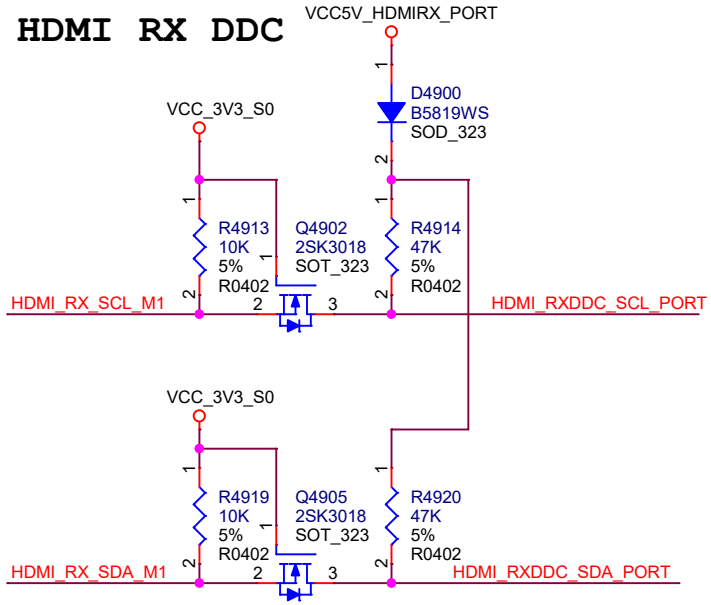
HDMI2.0 RX (OPTION1)

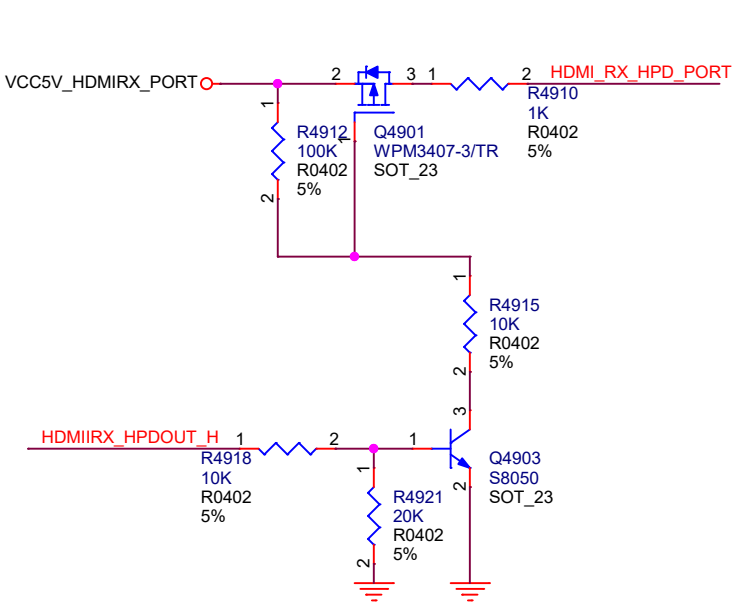
Note:

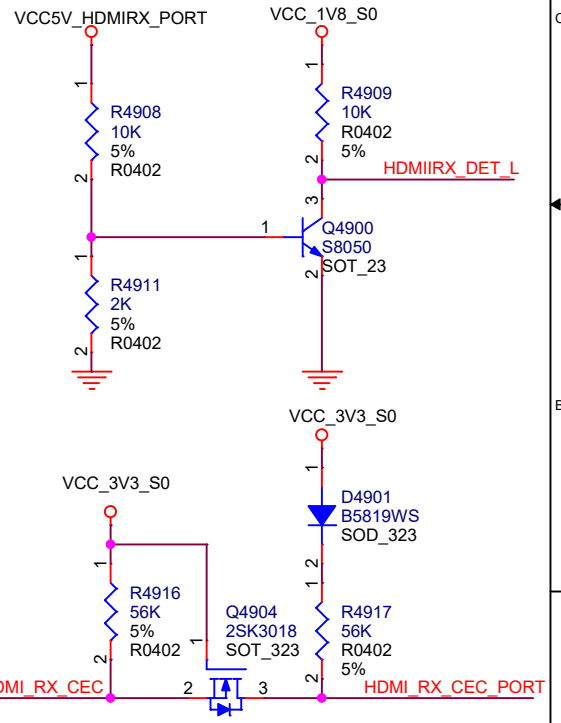
(This HDMI2.0 RX interface has low probability anomalies, such as splash screen and restart, in scenarios such as frequent plug and pull, high and low resolution switching, etc. The probability is between 0.1% and 1%. We are still trying to debug and solve these problems. If the user will frequently use various peripherals to insert this HDMI2.0 RX interface, it is recommended to use external bridges connectting chips to improve compatibility to avoid affecting product production.)



HDMI RX DDC







HPD:
Sink Side: Require output, Min 2.4V; Max 5.3V
Source Side:Require input and Detection.
Min 2.0V,Max:5.3V

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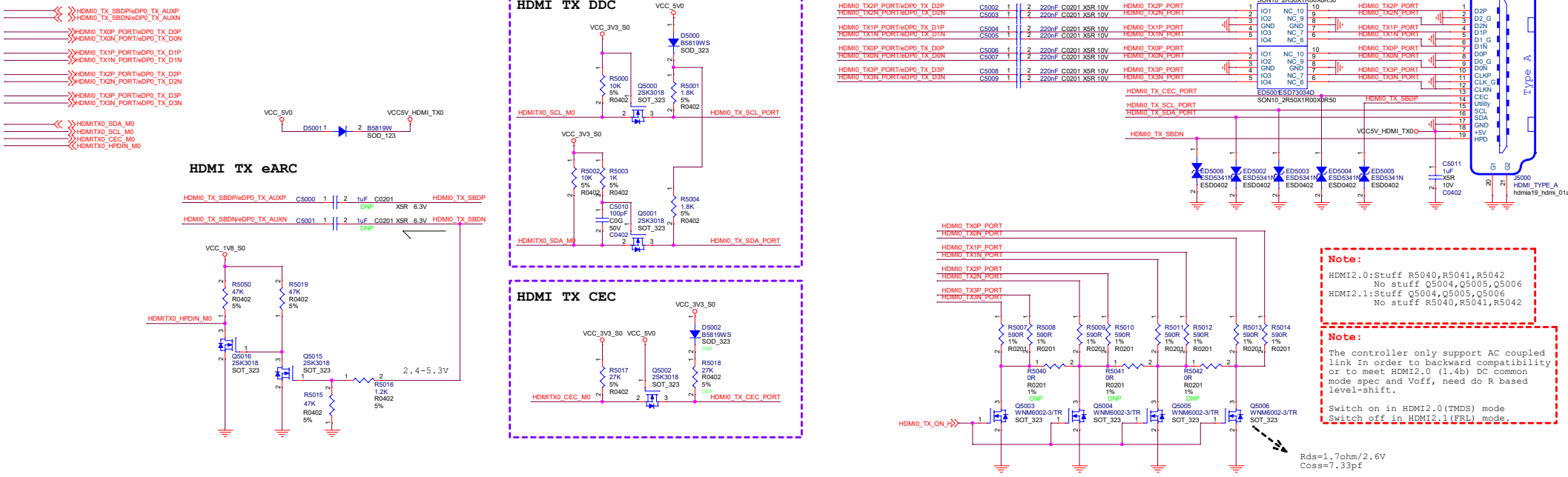
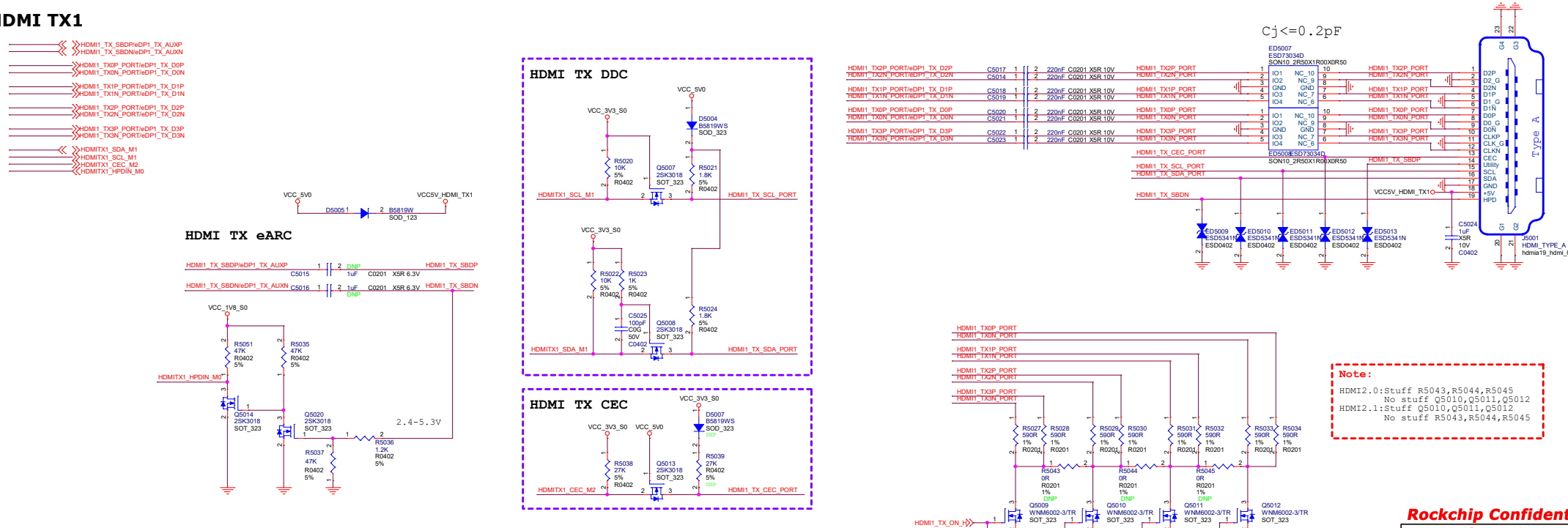
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	49.VI-HDMI2.0 RX				
Date:	Friday, October 21, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:		Sheet:	49 of 99

HDMI TX0



HDMI TX1



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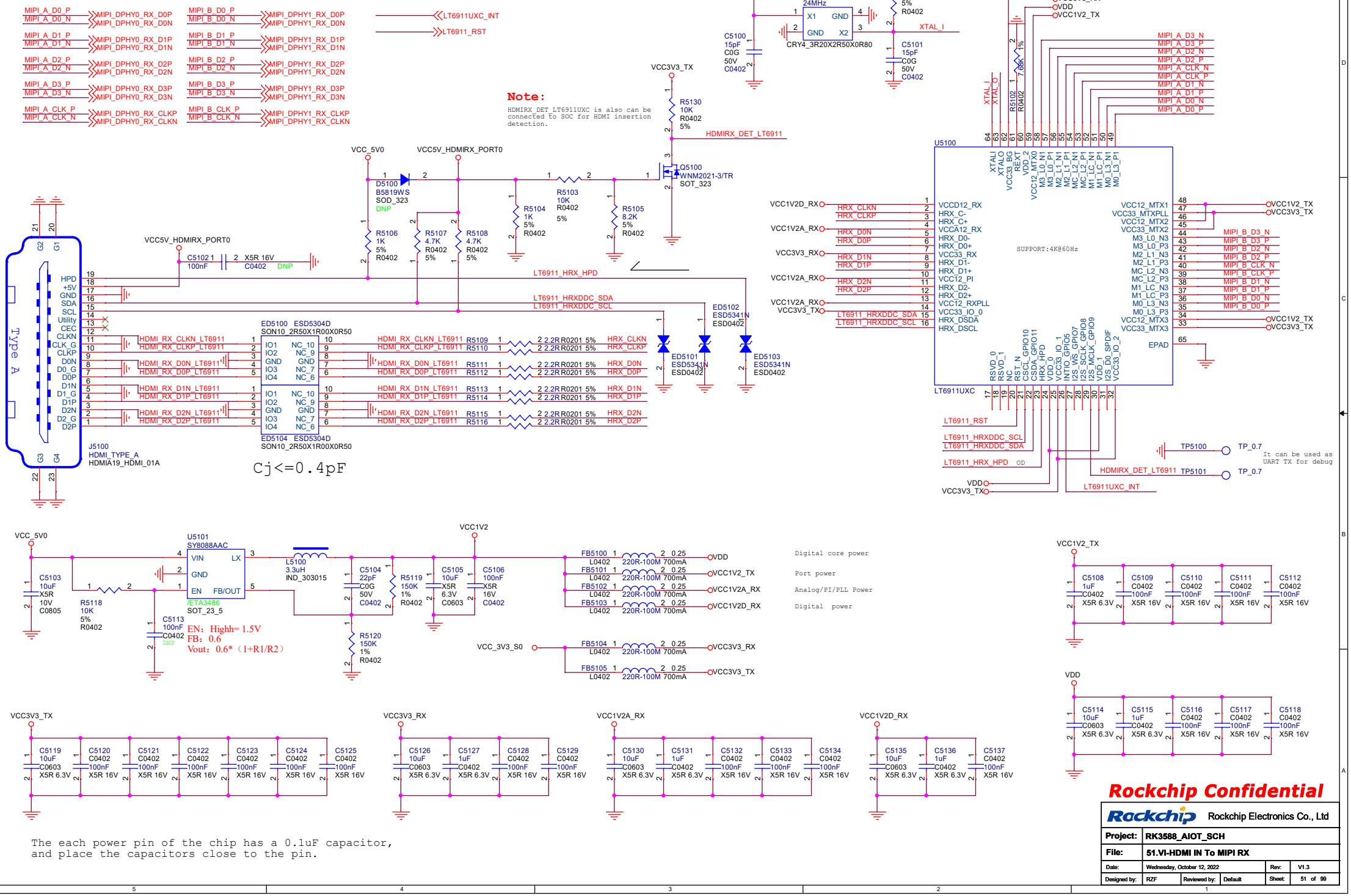
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	50.VO-HDMI2.1 TX		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
Designed by: RZF	Reviewed by:	Sheet:	50 of 99

HDMI2.0 RX(OPTION2)



The each power pin of the chip has a 0.1uF capacitor, and place the capacitors close to the pin.

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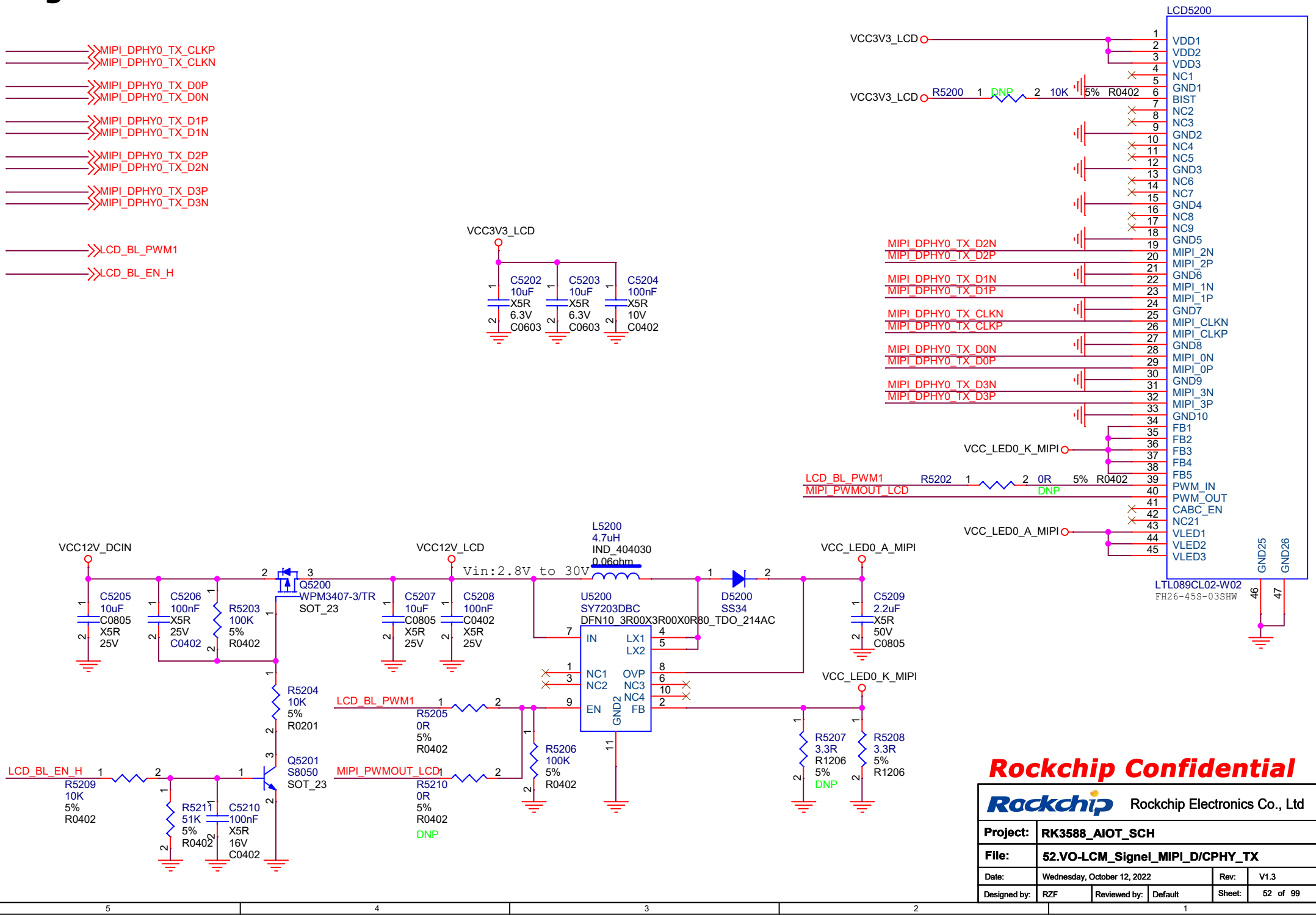
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	51.VI-HDMI IN To MIPI RX				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:	Default	Sheet:	51 of 99

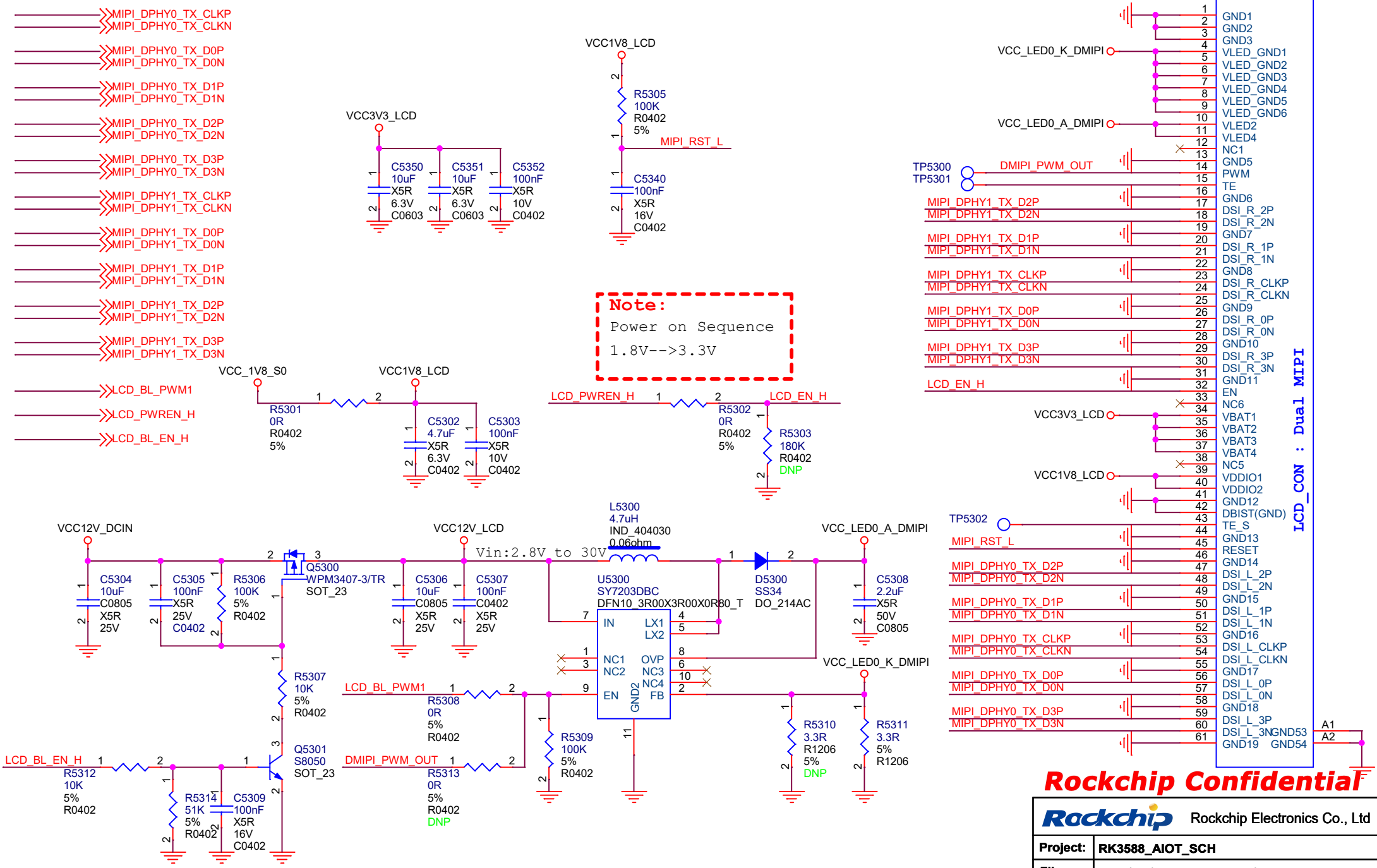
Single-MIPI0 LCM



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	52.VO-LCM_Signel_MIPI_D/CPHY_TX				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:	Default	Sheet:	52 of 99

Dual-MIPI LCM



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Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	53.VO-LCM_Dual MIPI_D/CPHY TX				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:	Default	Sheet:	53 of 99

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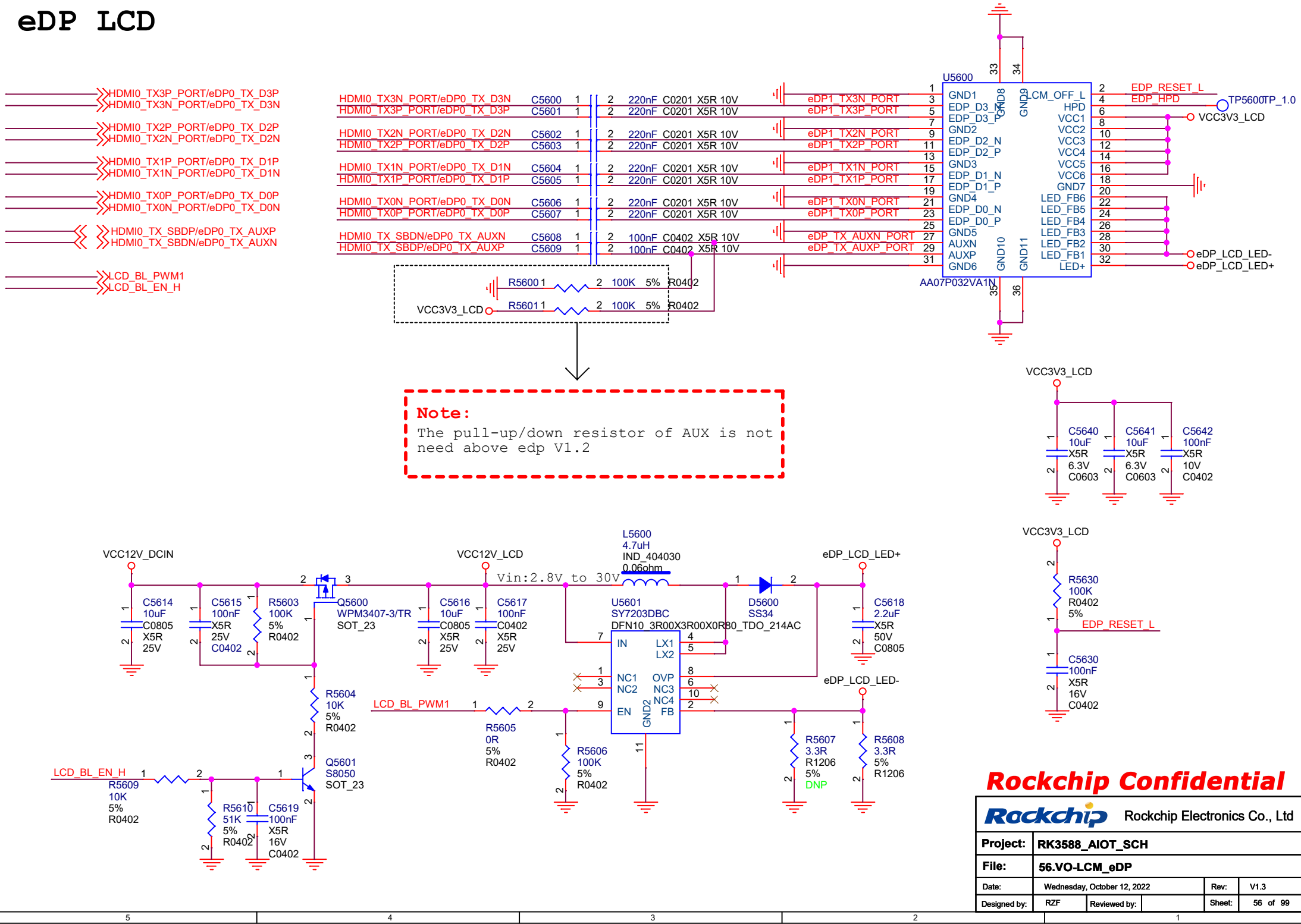
eDP LCD



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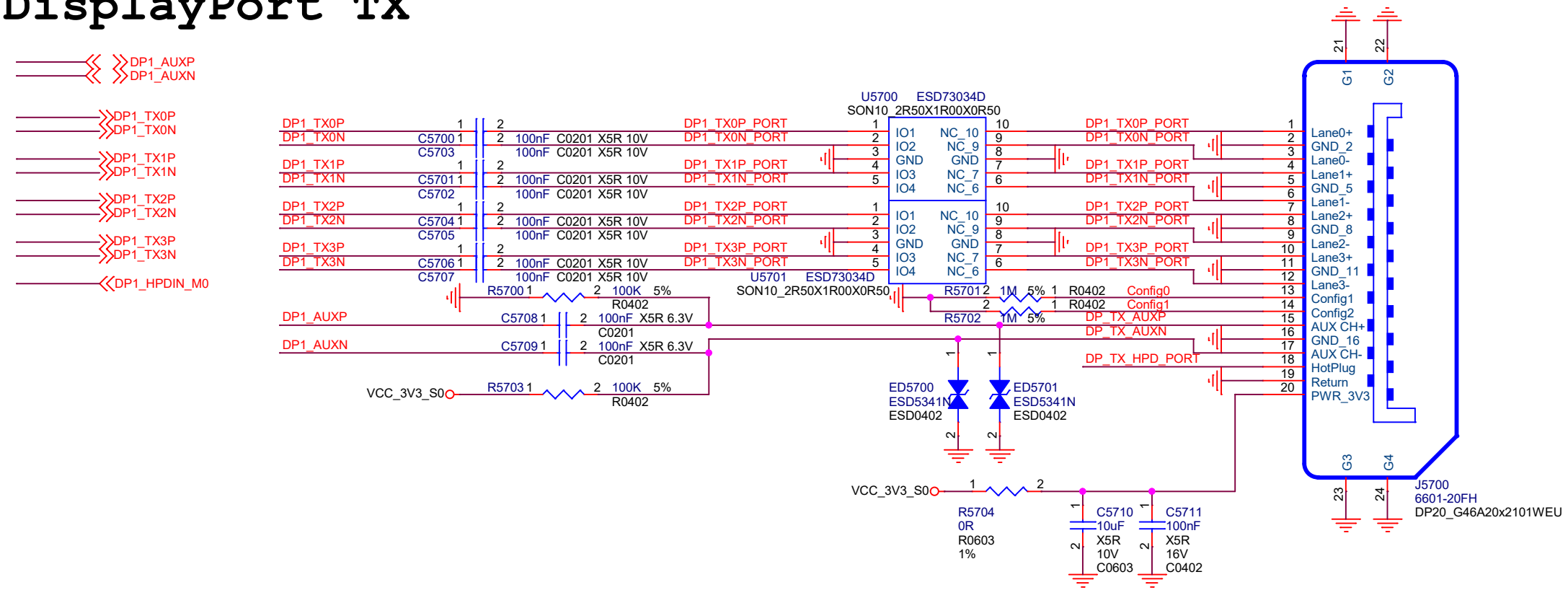
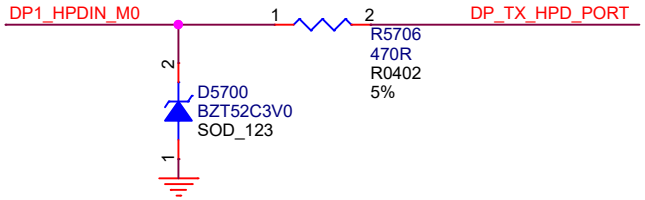
Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	56.VO-LCM_eDP		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
Designed by: RZF	Reviewed by:	Sheet:	56 of 99

DisplayPort TX



DP_TX_HPD

HPD Voltage:2.25-3.6V



Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	57.VO-DP		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
Designed by: RZF	Reviewed by:	Sheet:	57 of 99

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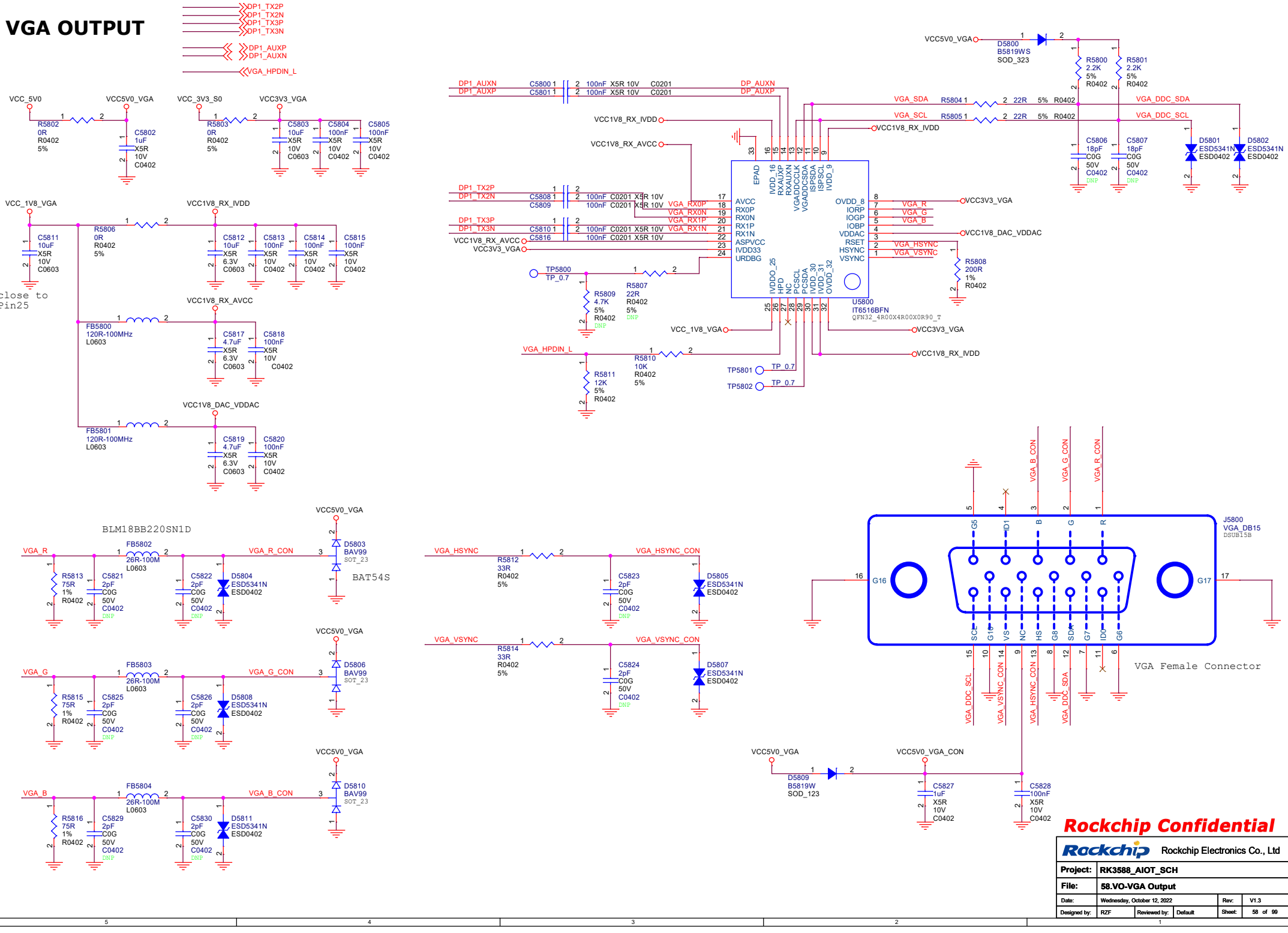
VGA OUTPUT



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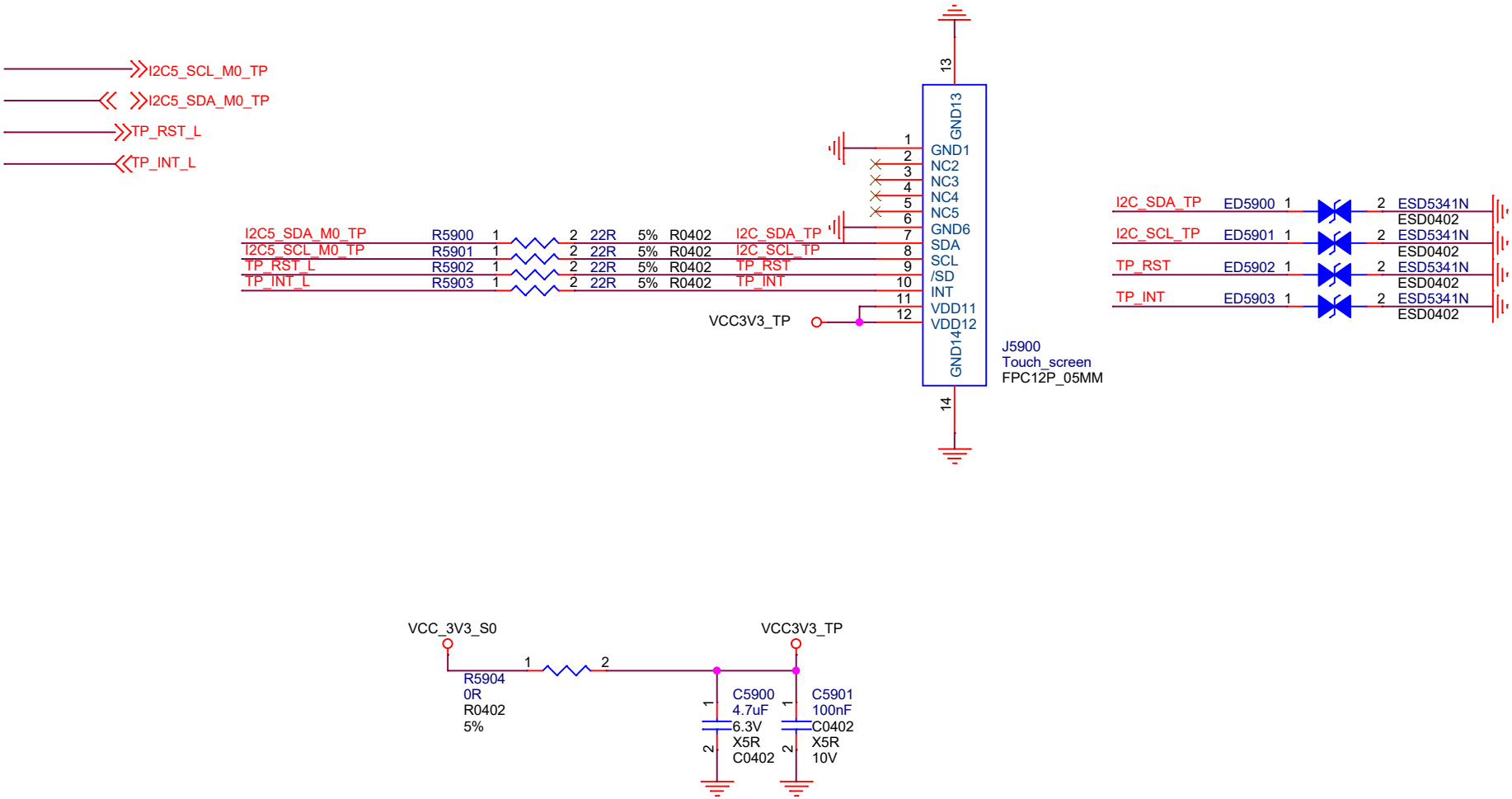
Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	58.VO-VGA Output				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:	Default	Sheet:	58 of 99

Touch Panel connector



Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	59.TP Connector_COF				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:	Default	Sheet:	59 of 99

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WIFI（802.11 a/b/g/n/ac 2x2 MIMO）

UART9_TX_M0_BT
UART9_RX_M0_BT
UART9_RTSn_M0_BT
UART9_CTSn_M0_BT

WIFI_REG_ON_H
BT_REG_ON_H
BT_WAKE_HOST_H
HOST_WAKE_BT_H
WIFI_WAKE_HOST_H

Note:
Adjusted the load capacitance according to the crystal specification.

50 Ohm RF trace

J6200 SMA-J-P-H-RA-TH1 ANT5_SMA_RA_TH1
C6200 10pF C0402 C0G 50V
C6201 DNP C0402
C6202 DNP C0402

J6201 SMA-J-P-H-RA-TH1 ANT5_SMA_RA_TH1
C6203 10pF C0402 C0G 50V
C6205 DNP C0402
C6206 DNP C0402

C6204 22pF C0402 C0G 50V
R6200 22R 5% R0402
Y6200 37.4MHz CRY4_3R20X2R50X0R80
C6207 22pF C0402 C0G 50V

U6200
AP6398S
MD50_AP6XXX_13RX15RX1R5

12	NC/NC/PCIE_PREST_L	BT_HOST_WAKE	50
13	XTAL_OUT	BT_WAKE	49
14	XTAL_IN	GPIO8_9/NC_BT_ANT/NC	48
15	WL_REG_ON	NC/GND/PCIE_TDP	47
16	WL_HOST_WAKE	GPIO4/NC/PCIE_TDN	46
17	SDIO_DATA_CMD	GPIO5/WL_UART_RX/PCIE_RDP	45
18	SDIO_DATA_CLK	NC/WL_UART_TX/PCIE_RDN	44
19	SDIO_DATA_3	UART_CTS_N	43
20	SDIO_DATA_2	UART_RTS_N	42
21	SDIO_DATA_0/HUSB_DP	UART_RXD	41
22	SDIO_DATA_1/HUSB_DM	UART_TXD	40
23	GND_10	GND_12	39
24	NC/SDIO_VSEL/PCIE_PME_L	BT_REG_ON	38
25	VIN_LDO	NC/NC/PCIE_CLKREQ_L	37

GND_9 GND_8 WL_ANT1 GND_7 GND_6 GND_5 GND_4 GND_3 GND_2 WL/BT_ANT0 GND_1
VIN_LDO_OUT PCM_SYNC PCM_IN PCM_OUT PCM_CLK LPO GND_11 NC/NC/PCIE_REFCLK_N VDDIO NC/NC/PCIE_REFCLK_P VBAT

R6204 0R 5% R0402
C6209 DNP C0402
C6208 10pF C0402 C0G 50V DNP
C6210 DNP C0402
ANT6200 ANT_JACK ANT_JACK
GND1 GND2

WIFI_REG_ON_H
WIFI_WAKE_HOST_H
SDIO_CMD_M0_WIFI → R6206 0R R0402 5% WIFI_CMD
SDIO_CLK_M0_WIFI → R6207 0R R0402 5% WIFI_CLK
SDIO_D3_M0_WIFI → R6208 0R R0402 5% WIFI_D3
SDIO_D2_M0_WIFI → R6209 0R R0402 5% WIFI_D2
SDIO_D0_M0_WIFI → R6210 0R R0402 5% WIFI_D0
SDIO_D1_M0_WIFI → R6211 0R R0402 5% WIFI_D1

VCCIO_WL → R6214 10K R0402 5%
SDIO_VSEL
R6217 10K 5% R0402 DNP

SDIO voltage select:
0: 3.3V 1:1.8V

C6211 4.7uF 10V X5R C0603
L6200 4.7uH IND_303012
1A_DCR<=80mohm

VBAT:(3.0-4.8V)/1.2A
VDDIO:(1.7-3.6V)/300mA.

I2S2_LRCK_M0_BT → R6219 22R R0402 5% PCM_SYNC_BT
I2S2_SDO_M0_BT → R6220 22R R0402 5% PCM_IN_BT
I2S2_SDI_M0_BT → R6221 22R R0402 5% PCM_OUT_BT
I2S2_SCLK_M0_BT → R6222 22R R0402 5% PCM_CLK_BT

VCC3V3_WL_VBAT
VCC_3V3_S3
R6218 0R R0805 1%
VCCIO_WL
VCC_1V8_S3
R6216 0R R0603 1%

1.6V<V<3.3V
32KOUT_WIFI
R6223 DNP R0402
C6213 DNP C0402
C6214 100nF X5R 10V C0402
C6215 100nF X5R 10V C0402
C6216 22uF X5R 10V C0805
C6212 1uF X5R 10V C0402

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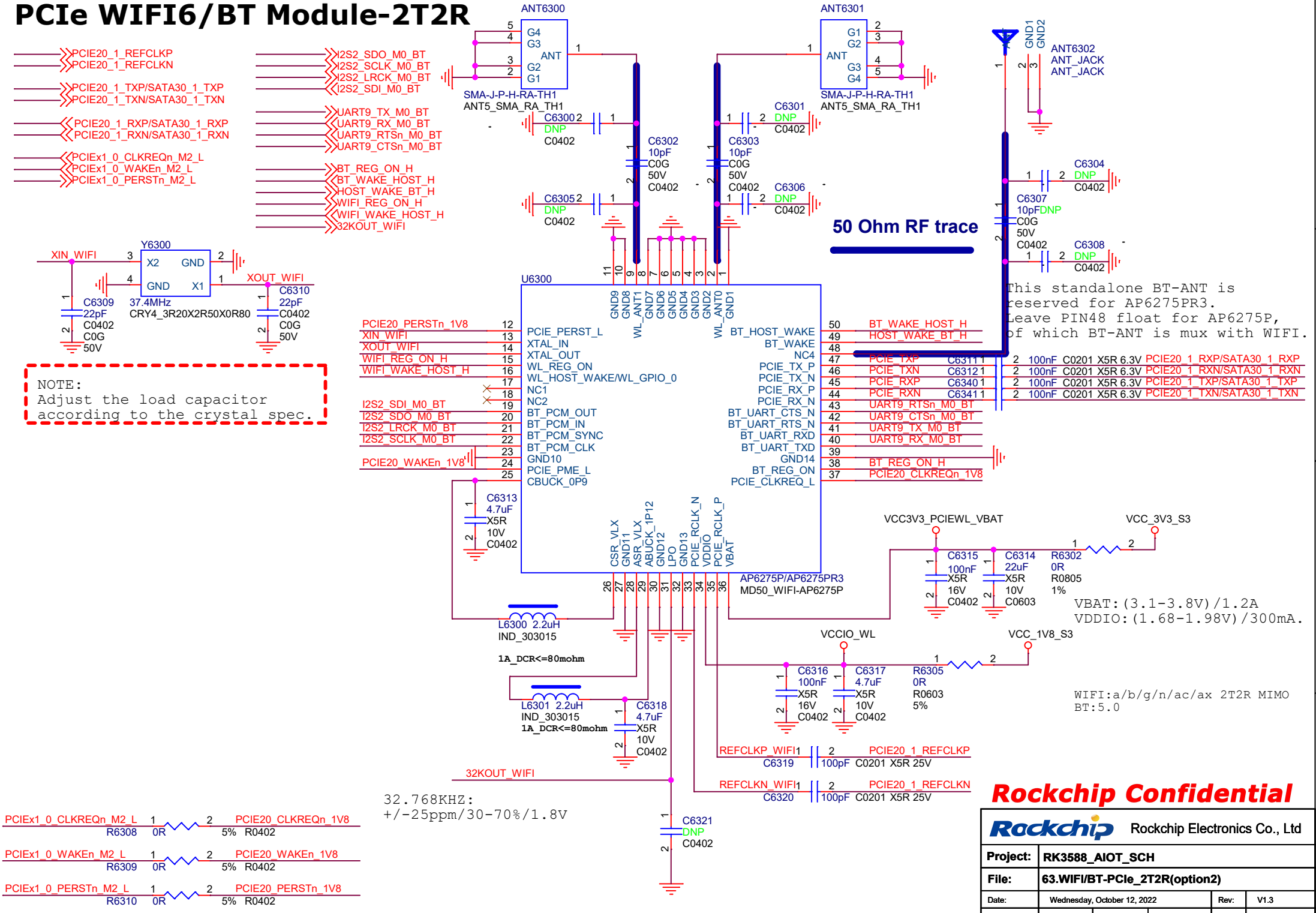
Rockchip Electronics Co., Ltd

Project:	RK3588_AIOT_SCH		
File:	62.WIFI/BT-SDIO_2T2R		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
Designed by: RZF	Reviewed by:	Sheet:	62 of 99

PCIe WIFI6/BT Module-2T2R



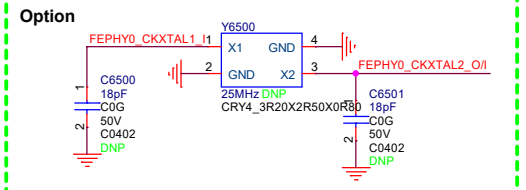
Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	63.WIFI/BT-PCIe_2T2R(option2)		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
Designed by: RZF	Reviewed by:	Sheet:	63 of 99

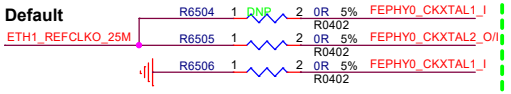
RMII

GMAC1_TXD0
GMAC1_TXD1
GMAC1_TXEN
GMAC1_RXD0
GMAC1_RXD1
GMAC1_RXDV_CRS
GMAC1_MCLKINOUT
GMAC1_MDC
GMAC1_MDIO
ETH1_REFCLKO_25M
GMAC1_RSTn_L

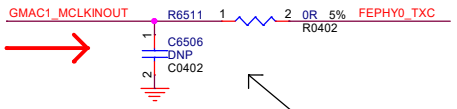
Option

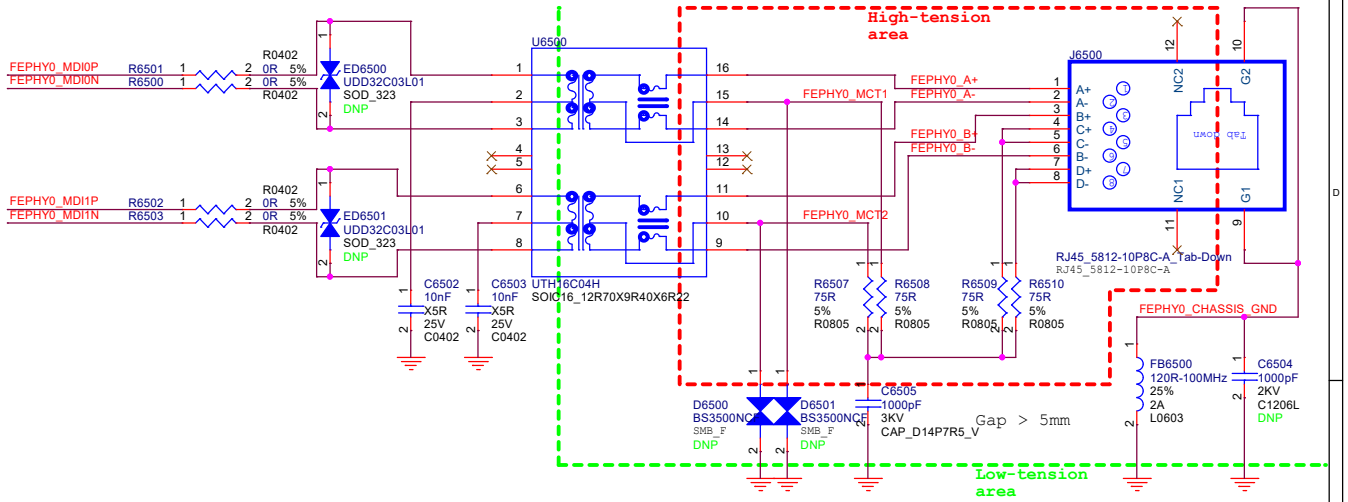


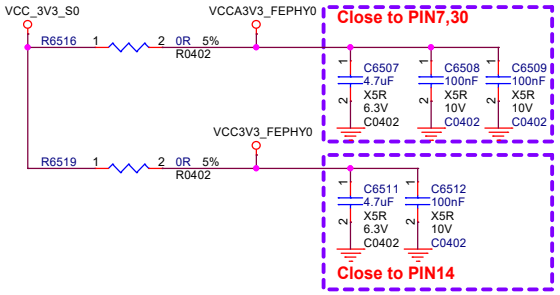
Default

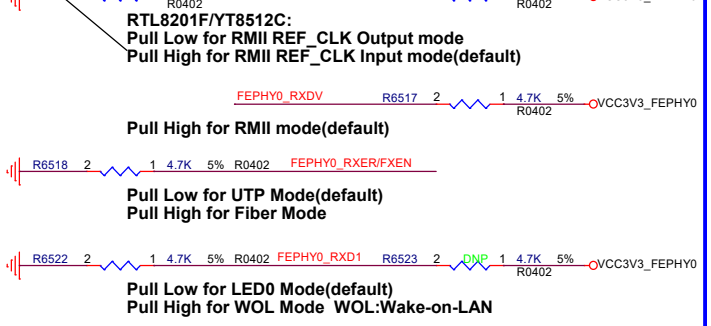


Default: Refclk:MAC output,PHY input

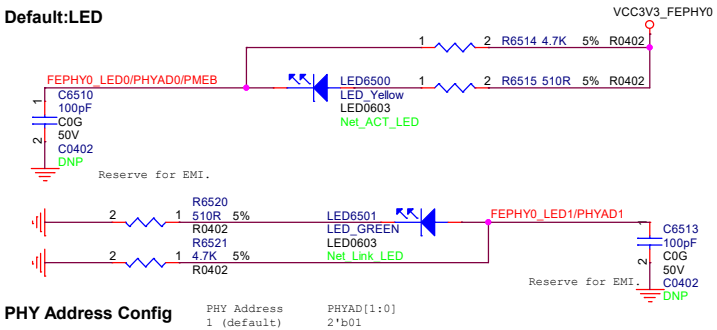






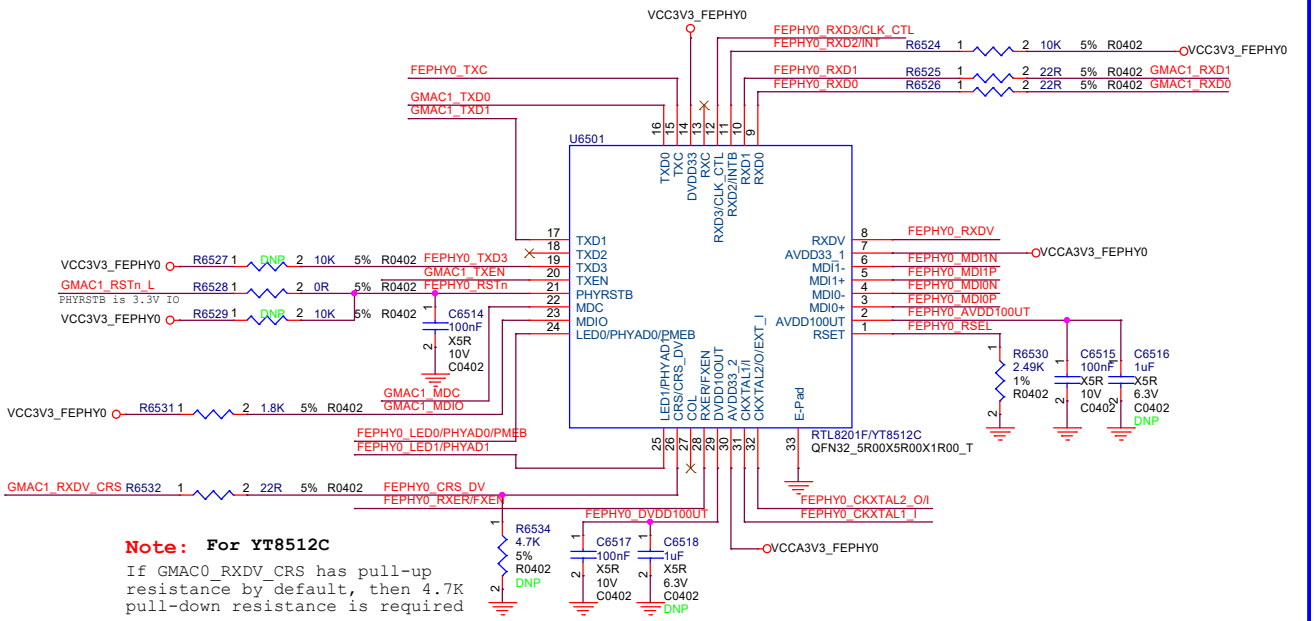


Default:LED



PHY Address Config

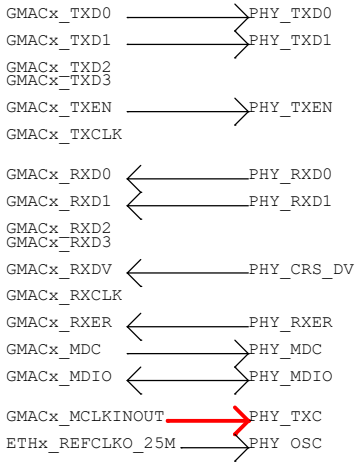
PHY Address	PHYAD[1:0]
1 (default)	2'b01



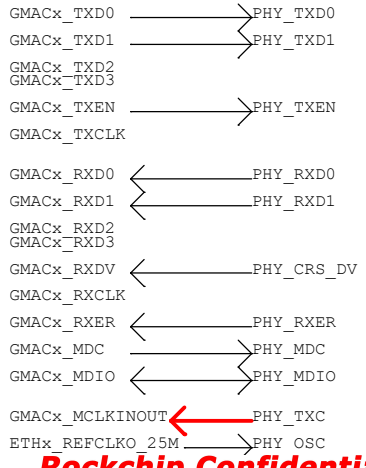
Note: For YT8512C

If GMAC0_RXDV_CRS has pull-up resistance by default, then 4.7K pull-down resistance is required

Default
Refclk:MAC output,PHY input



Refclk:MAC input,PHY output



Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	65.Ethernet-RMII(option)				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:	Default	Sheet:	65 of 99

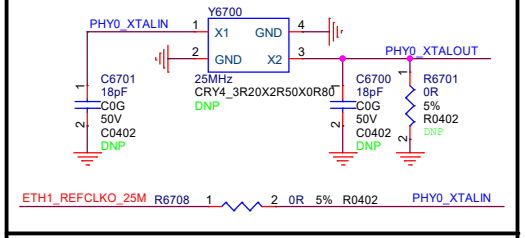
RGMII TO RJ45

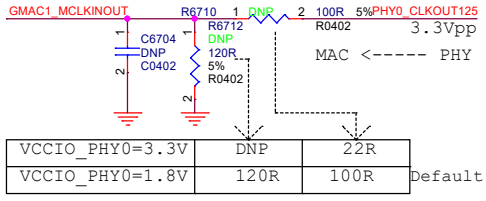
GMAC1_TXD0
GMAC1_TXD1
GMAC1_TXD2
GMAC1_TXD3
GMAC1_TXEN
GMAC1_TXCLK

GMAC1_RXD0
GMAC1_RXD1
GMAC1_RXD2
GMAC1_RXD3
GMAC1_RXDV_CRS

GMAC1_RXCLK
ETH1_REFCLKO_25M
GMAC1_MCLKINOUT
GMAC1_MDC
GMAC1_MDIO

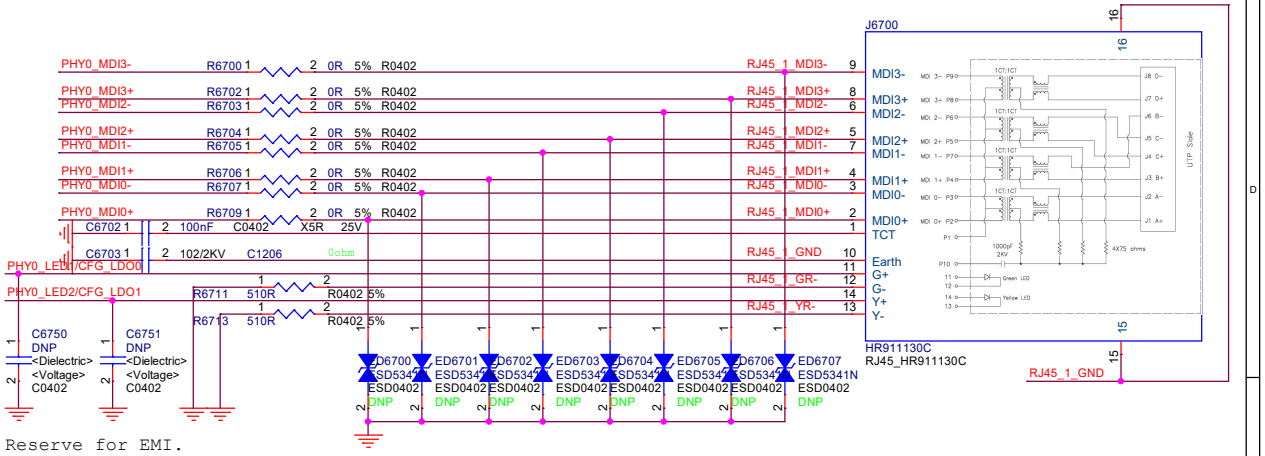
GMAC1_RSTn_L



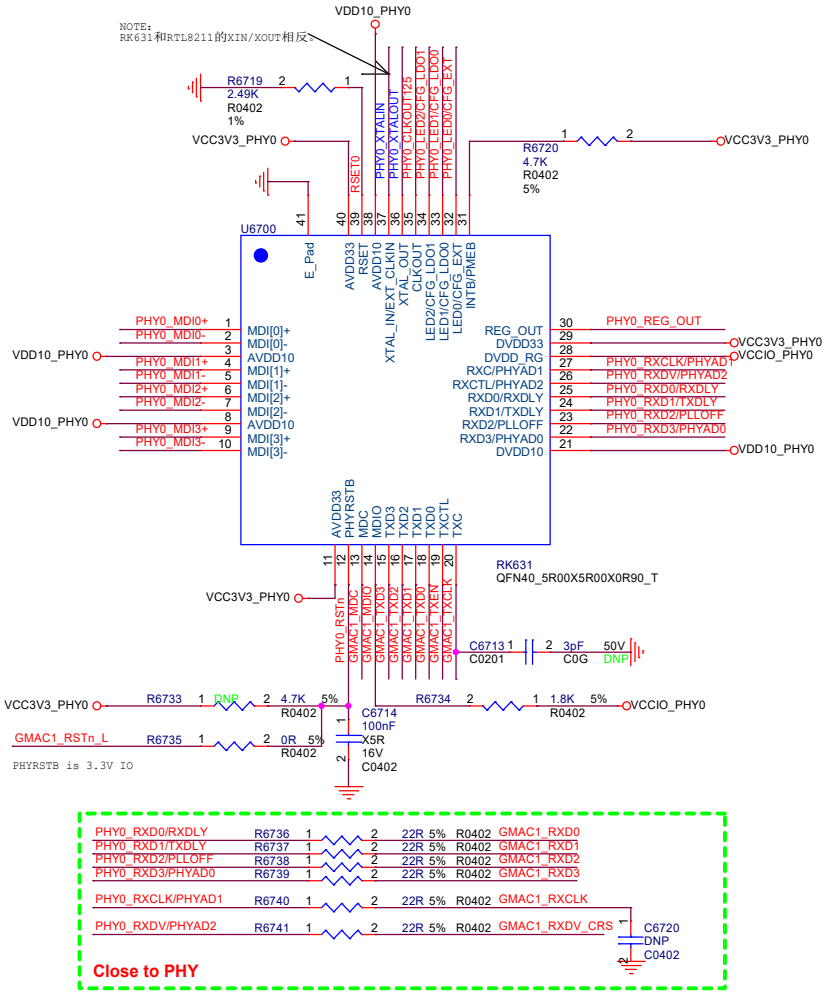


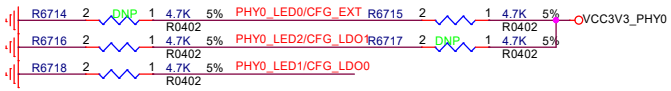
VCCIO_PHY0=3.3V	DNP	22R
VCCIO_PHY0=1.8V	120R	100R

Default



Reserve for EMI.





VCC_PHY0_IO Voltage Config

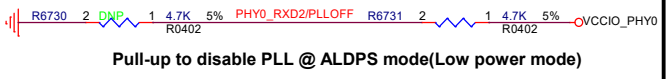
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V(default)	1'b1	2'b00	CFG_EXT: 1:External Power Source for IO pad. 0:Integrated LDO for IO pad CFG_LDO(1:0) 10:1.8V 00:3.3V
External 1.8V	1'b1	2'b10	
Internal 1.8V	1'b0	2'b10	

PHY Address Config

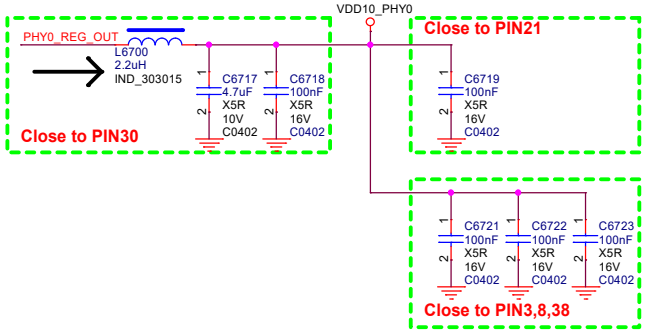
PHY Address	PHYAD[2:0]
1 (default)	3'b001

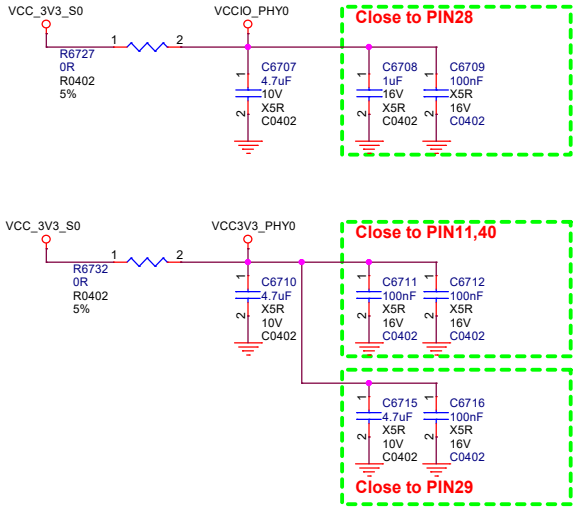
Pull-up for additional 2ns delay to RXC for data latching

Pull-up for additional 2ns delay to TXC for data latching



Pull-up to disable PLL @ ALDPS mode(Low power mode)





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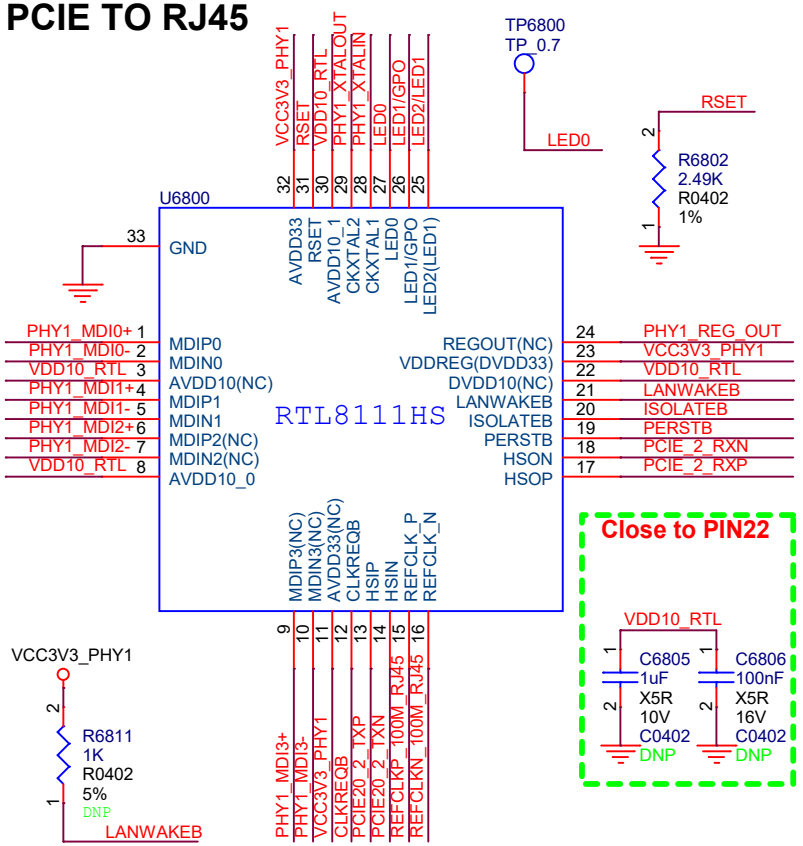
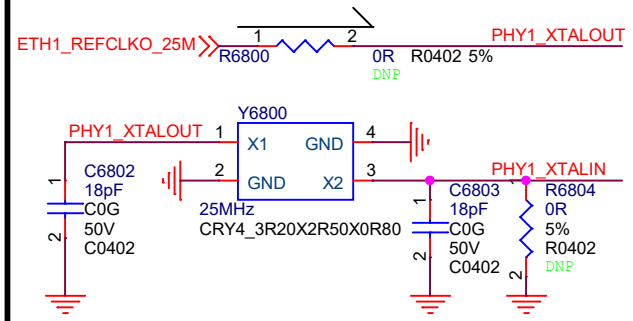
Rockchip	Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH			
File:	67.Ethernet-GPHY_RGMII1			
Date:	Wednesday, October 12, 2022		Rev:	V1.3
Designed by:	RZF	Reviewed by:	Default	Sheet: 67 of 99

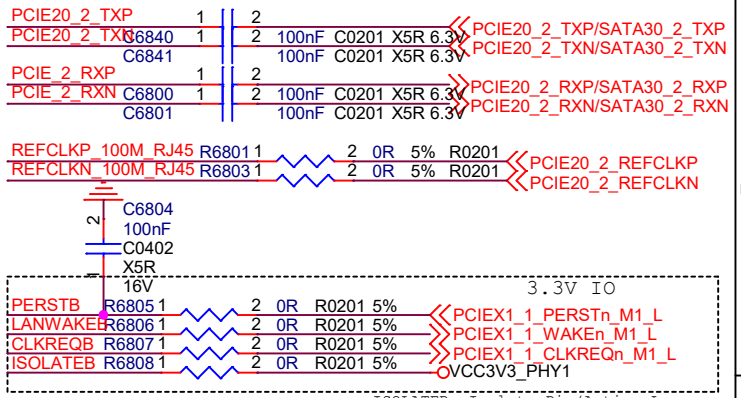
PCIE TO RJ45





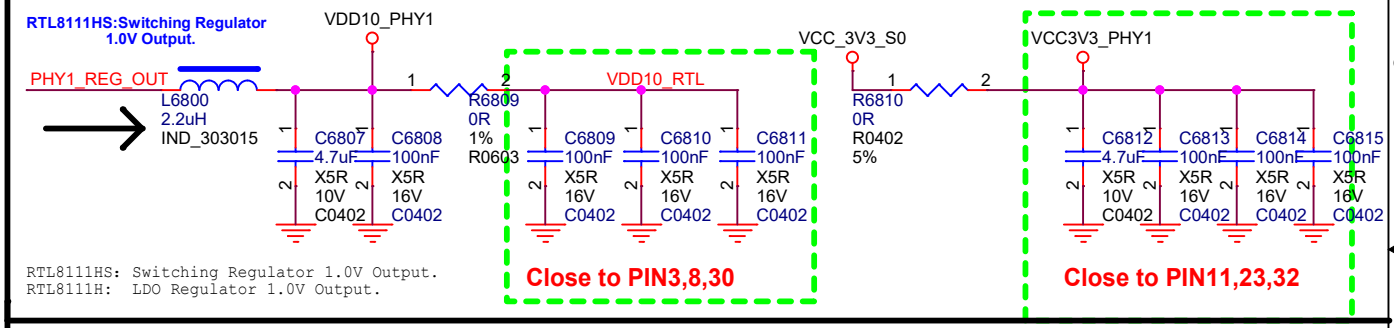
25Mhz Crystal: Stuff Y6800 C6802,No Stuff R6800,R6804
External Clock: Stuff R6804,R6800,No stuff: Y6800,C6802.

CKXTAL1(I): Input of 25Mhz Clock Reference.
CKXTAL2(IO): Input of External Clock Source
Output of 25Mhz Clock Reference.

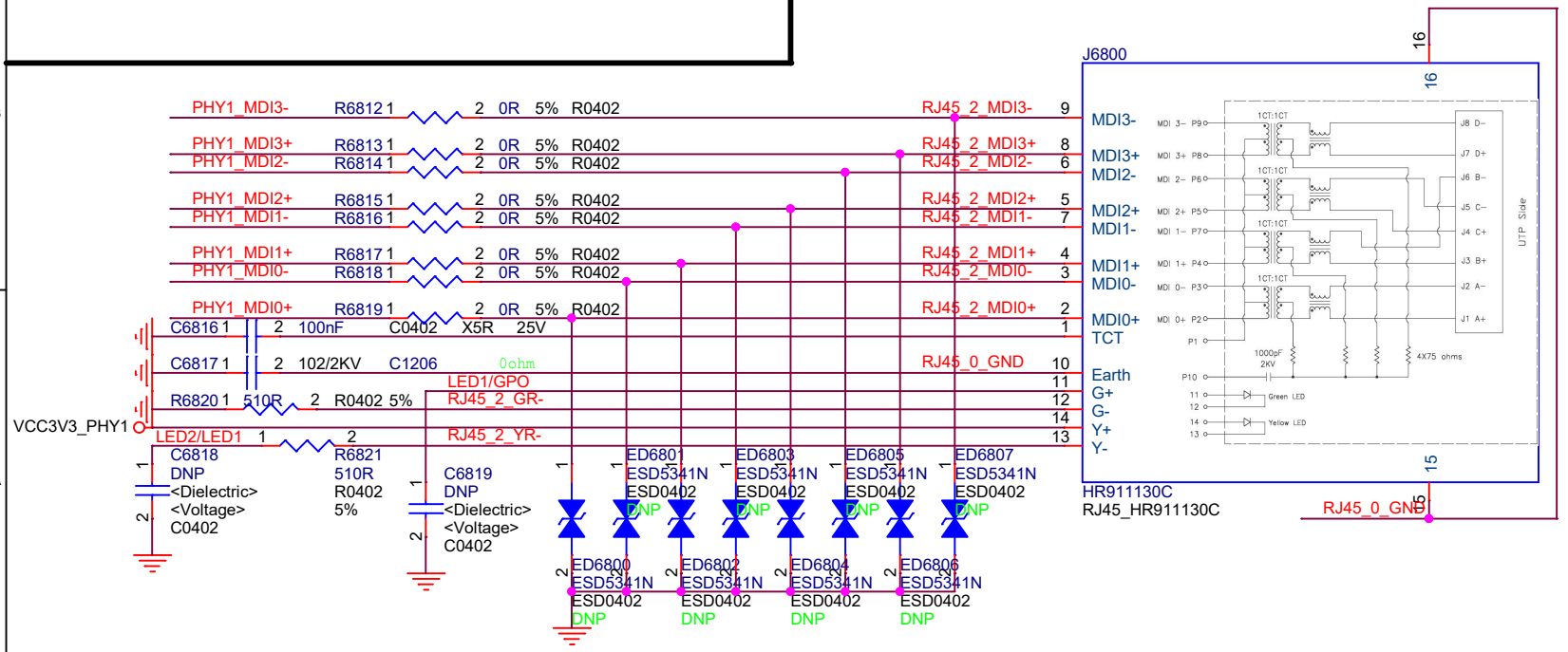


LANWAKEB:Power Management Event (Open Drain;Active Low,1.8V/3.3V compatible input/output mode with a weak external pull resistor)

ISOLATEB :Isolate Pin(Active Low, 1.8V/3,3V compatible input)Used to isolate the RTL8111HS from the PCI Express bus,The RTL8111HS will not drive its PCI Express input as long as the Isolate pin is asserted.



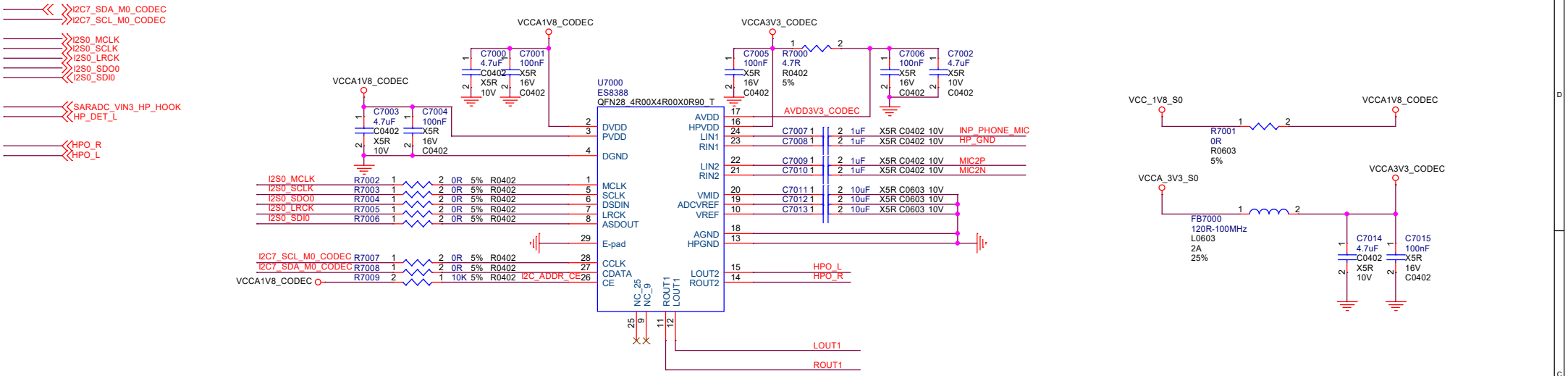
RTL8111HS: Switching Regulator 1.0V Output.
RTL8111H: LDO Regulator 1.0V Output.



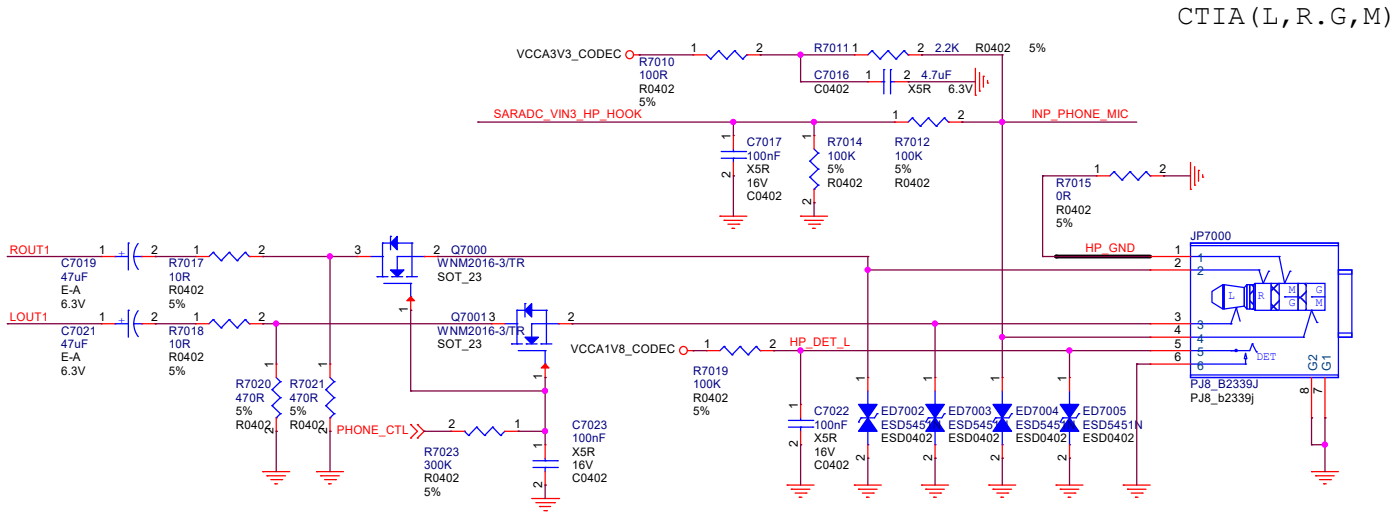
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	68.Ethernet-PCIE				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:	Default	Sheet:	68 of 99

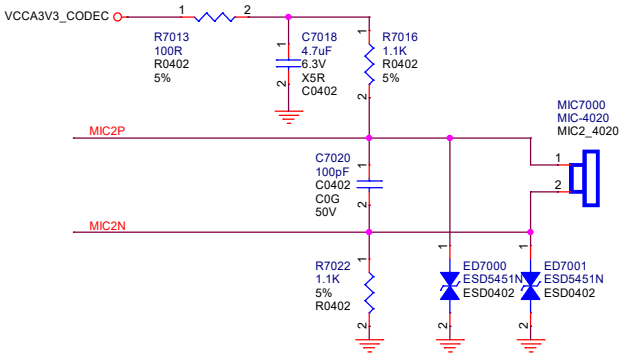
CODEC ES8388



EARPHONE



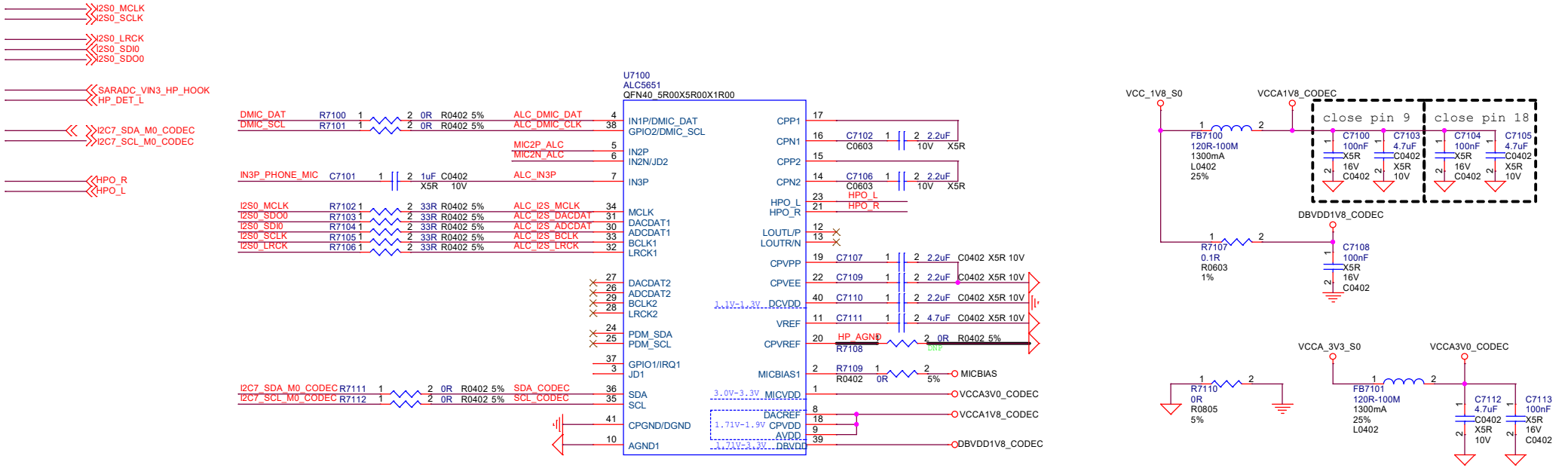
Analog MIC



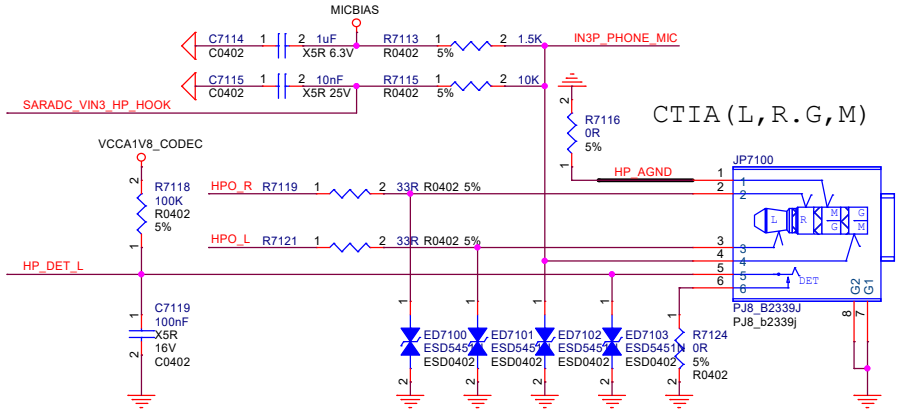
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	Audio Codec-ALC5651		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
Designed by:	RZF	Reviewed by:	Sheet: 70 of 99

CODEC ALC5651



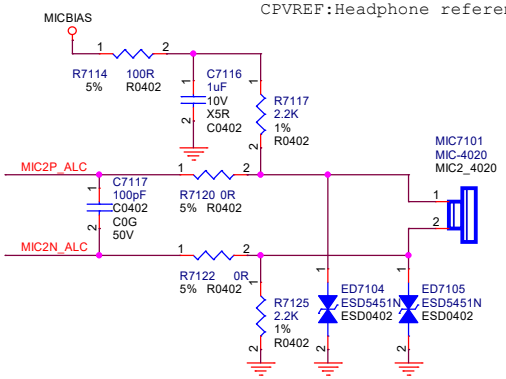
EARPHONE



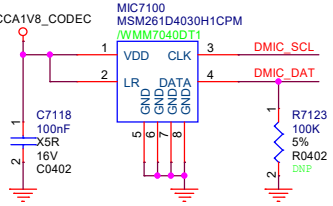
Analog MIC

Power Sequence:
DBVDD-MICVDD
DBVDD<150mA
MICVDD<10mA

CPVREF:Headphone reference ground.



DIGITAL MIC



Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	71.Audio Codec(option)				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:	Default	Sheet:	71 of 99

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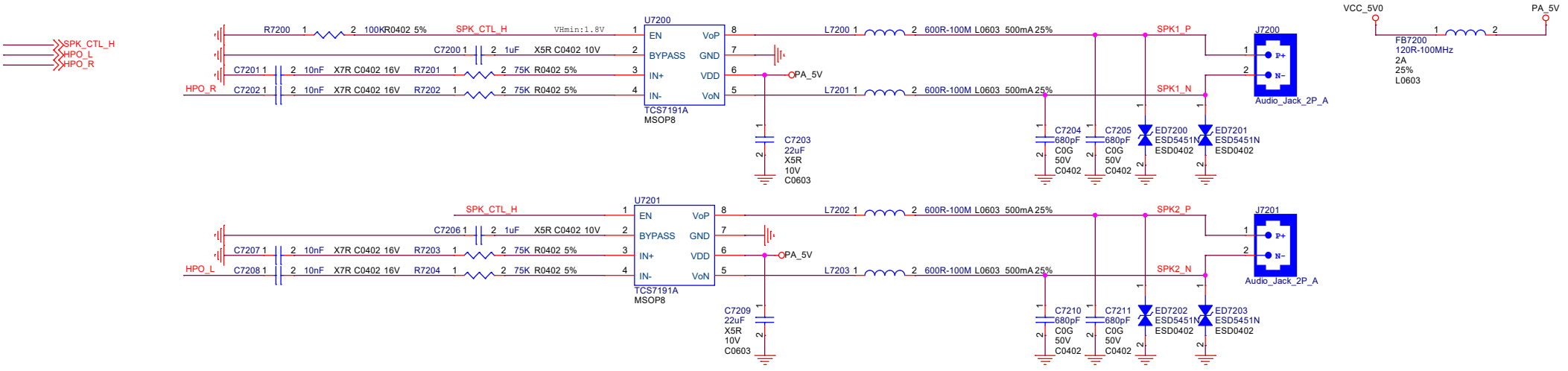
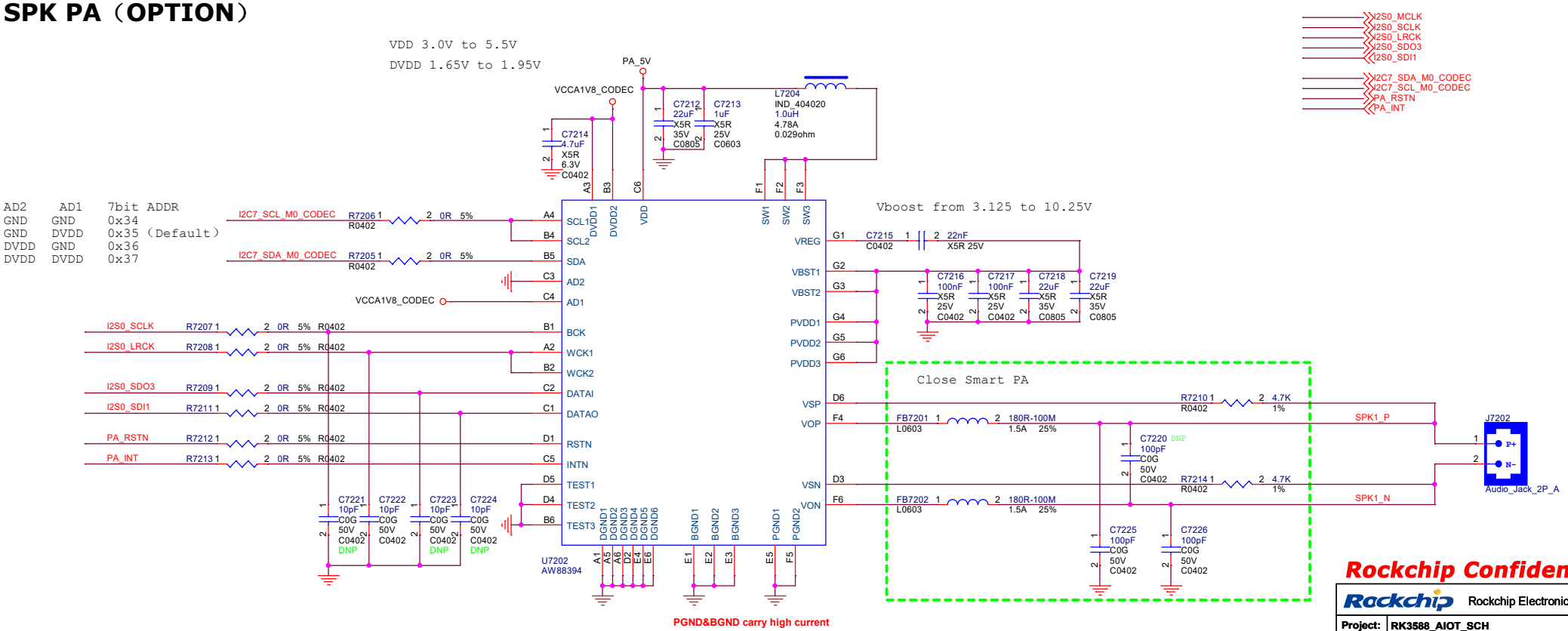
SPK PA（Default））

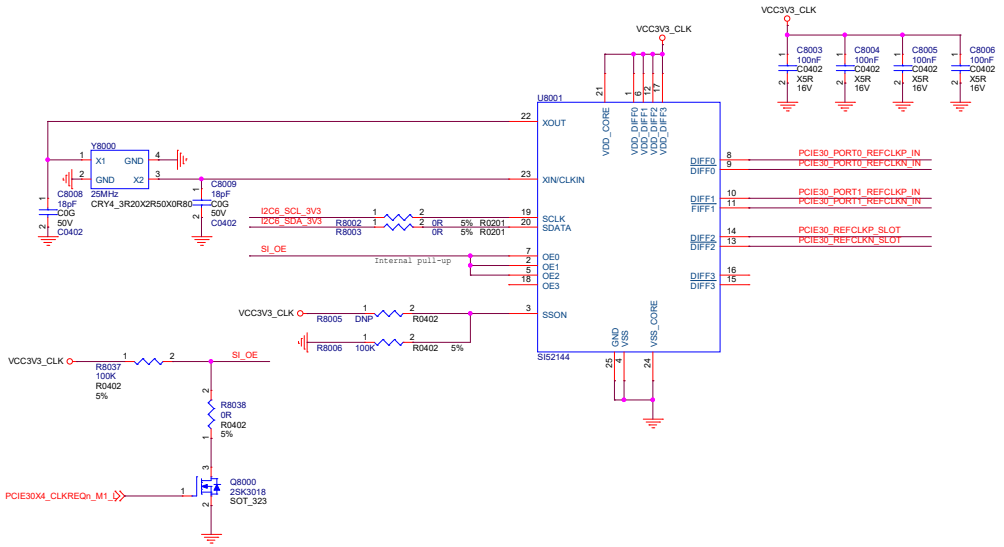


SPK PA（OPTION）

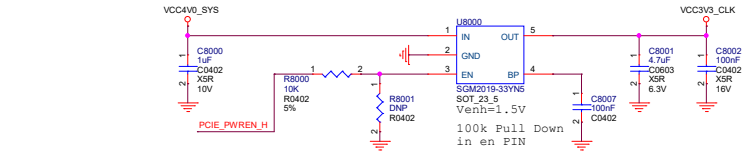


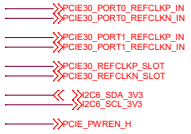
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	Audio Codec-ALC5651				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:		Sheet:	72 of 99

Crystal Generator(OPTION0)



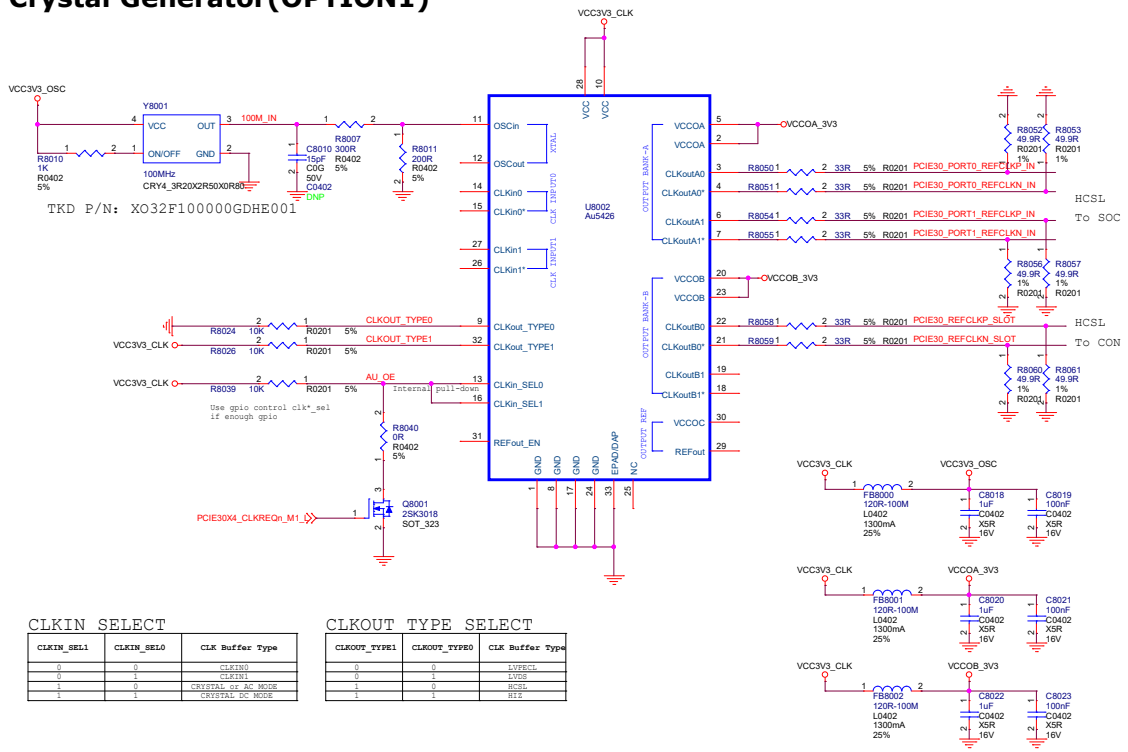
PCIe3.0 POWER





Note:
Please select one option

Crystal Generator(OPTION1)



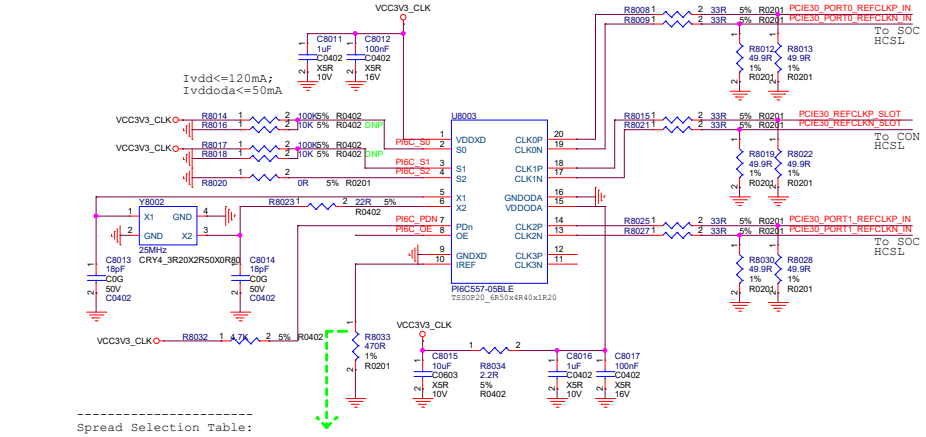
CLKIN SELECT

CLKIN_SEL1	CLKIN_SEL0	CLK Buffer Type
0	0	CLKIN0
0	1	CLKIN1
1	0	CRYSTAL OF AC MODE
1	1	CRYSTAL DC MODE

CLKOUT TYPE SELECT

CLKOUT_TYPE1	CLKOUT_TYPE0	CLK Buffer Type
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	HIZ

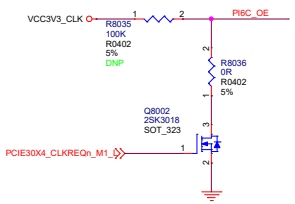
Crystal Generator(OPTION2)



Spread Selection Table:

SS0	SS1	Spread(%)
0	0	Center+/-0.25
1	0	-0.5
0	1	-0.75
1	1	No Spread

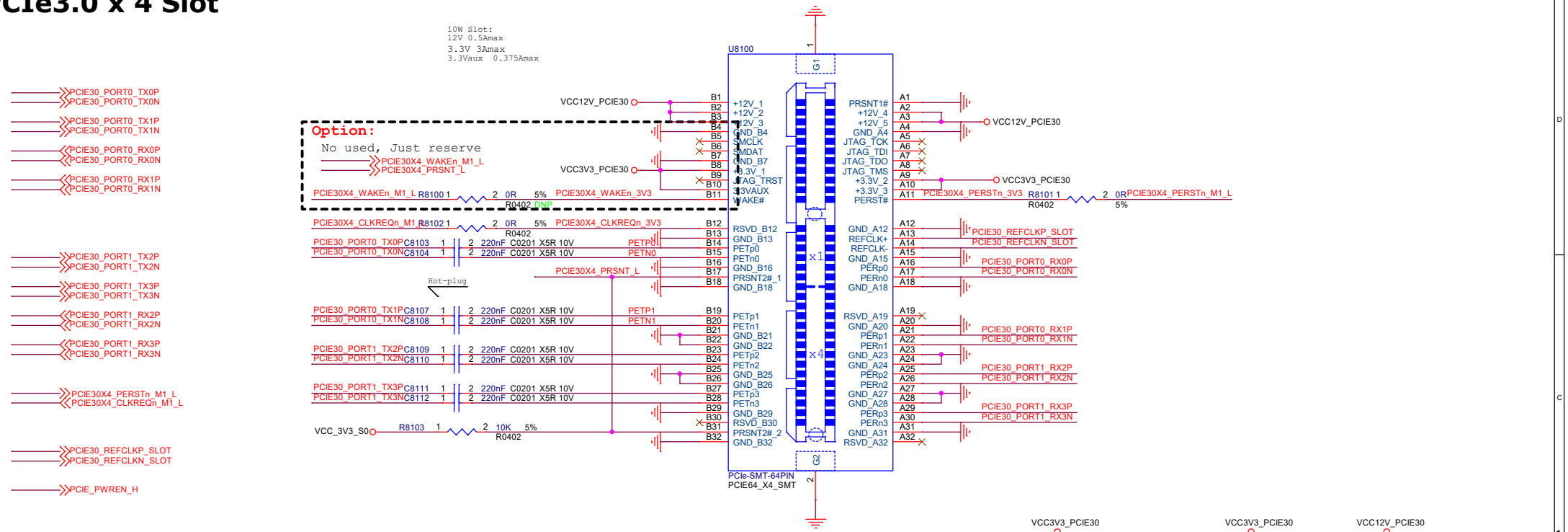
If board target trace impedance is 50ohm then R = 475ohm providing an IREF of 2.32 mA.The output current (IOH) is 6 * IREF.
Vih=6x2.32X50=696mV



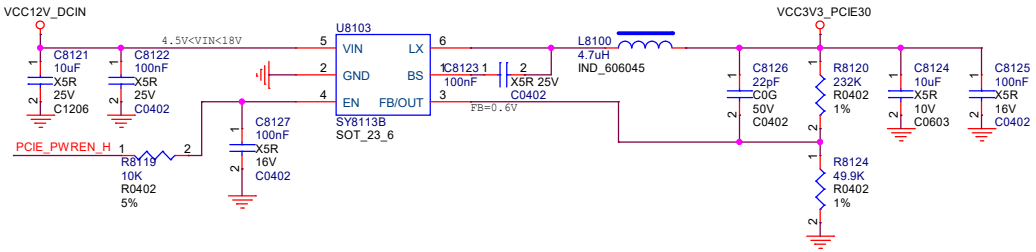
Rockchip Confidential

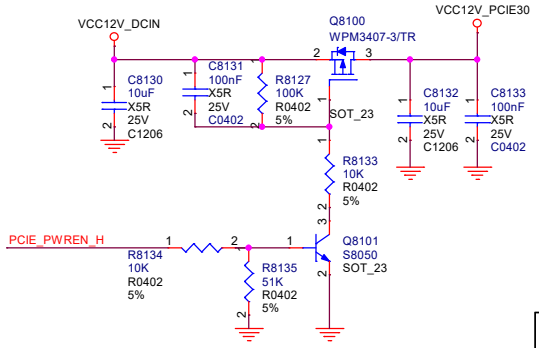
Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	80.PCIE-PCIE3.0 CLK GENERATOR		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
Designed by: RZF	Reviewed by:	Sheet:	80 of 99

PCIe3.0 x 4 Slot



PCIe3.0 POWER

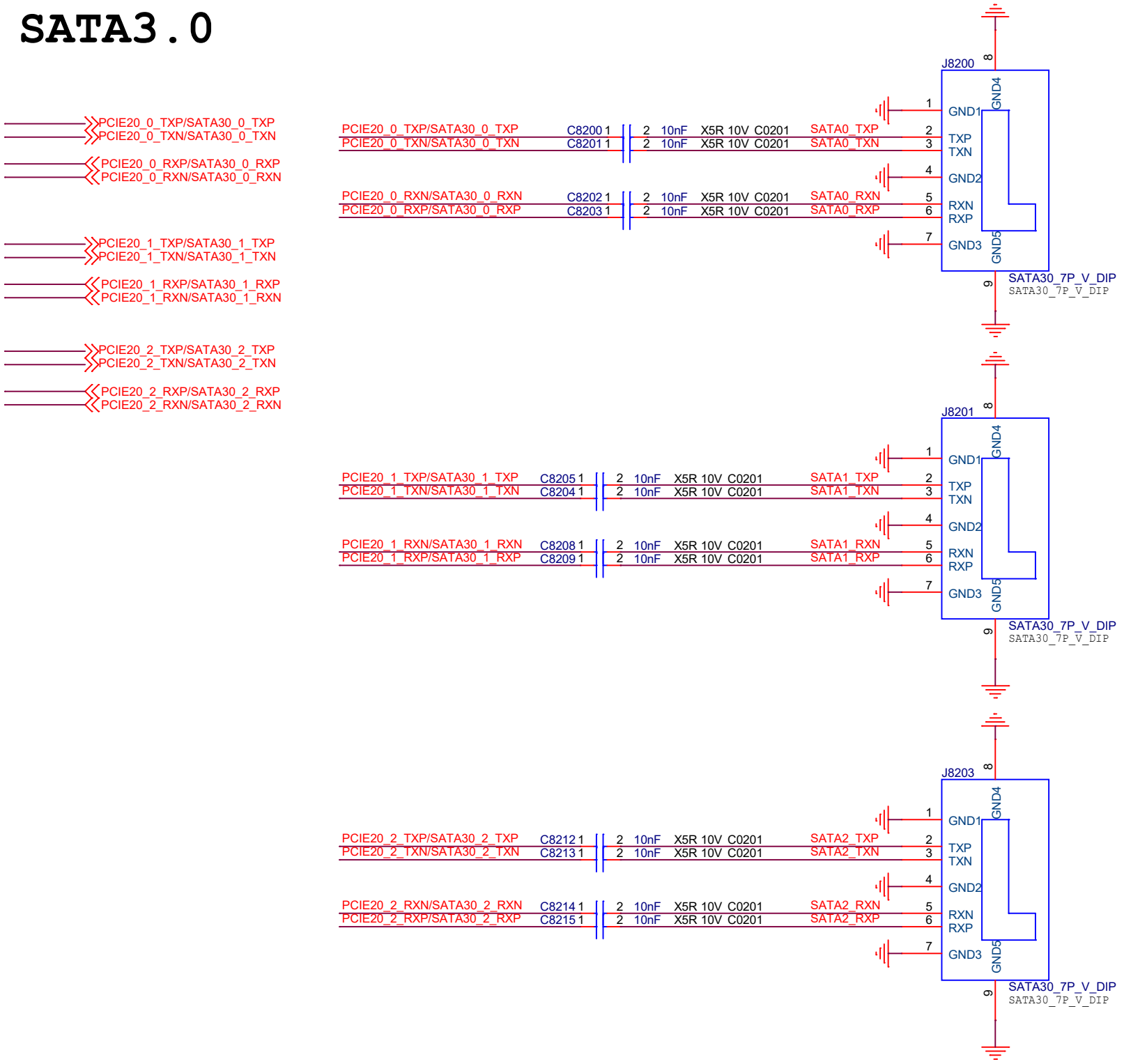




Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	81.PCIE-PCIE3.0_Slot				
Date:	Wednesday, October 12, 2022		Rev:	V1.3	
Designed by:	RZF	Reviewed by:		Sheet:	81 of 99

SATA3.0



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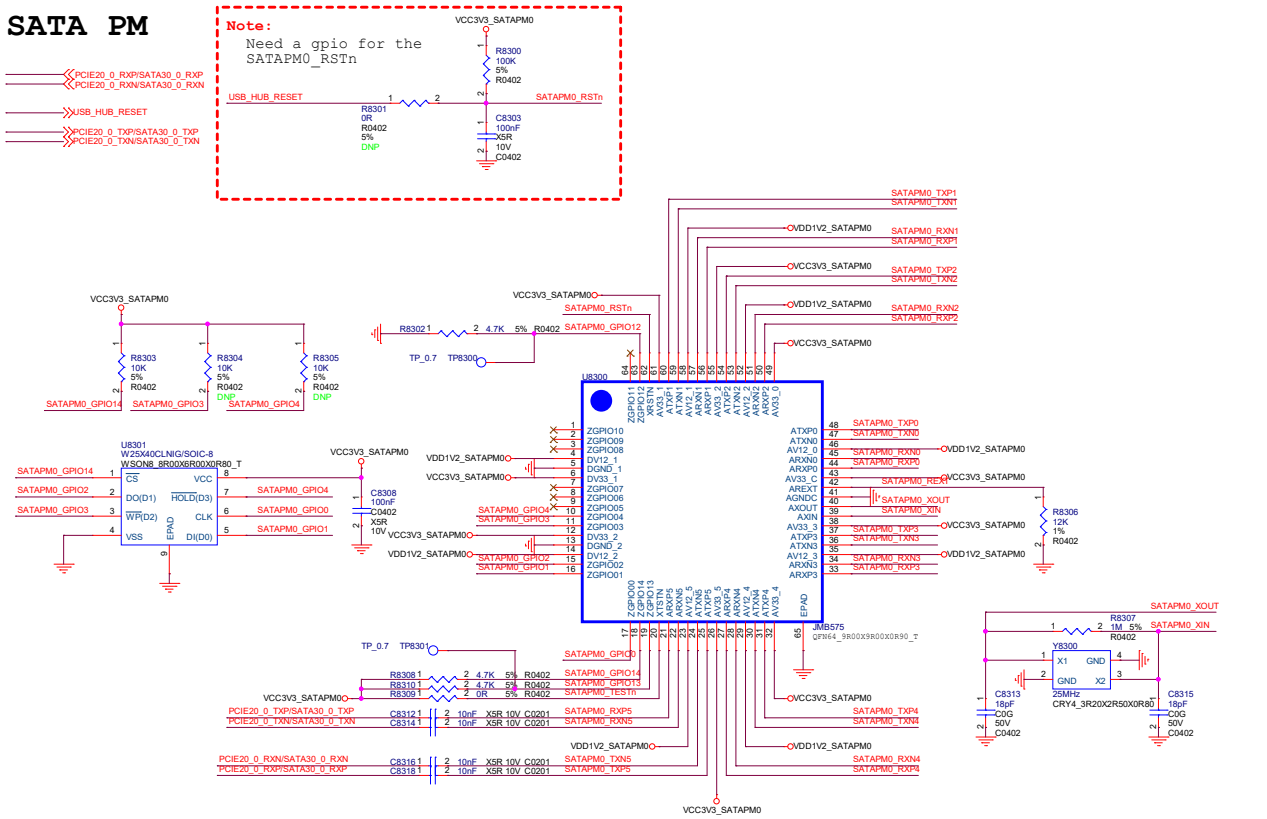
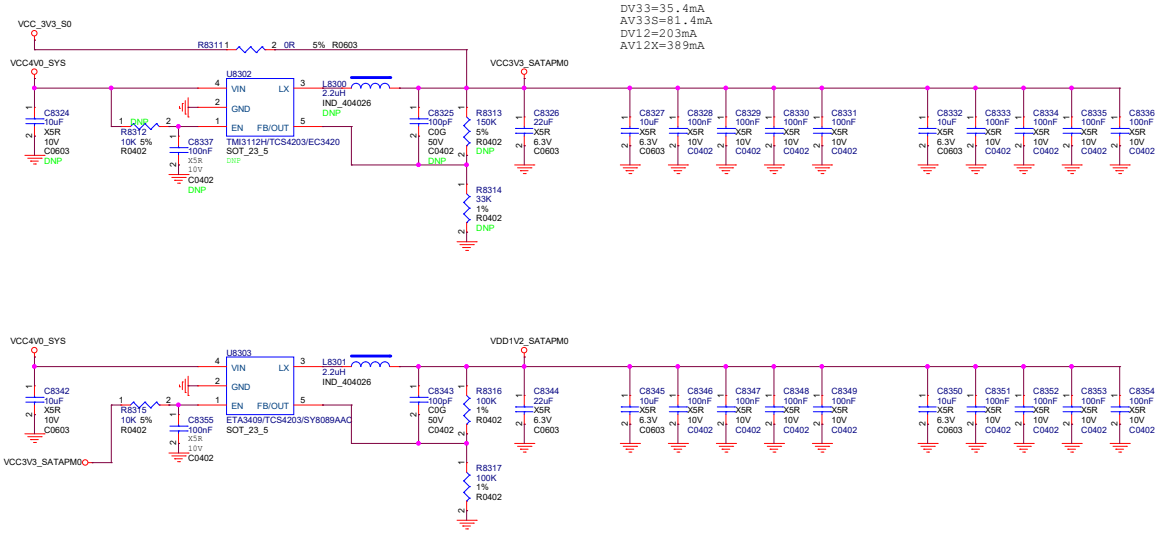
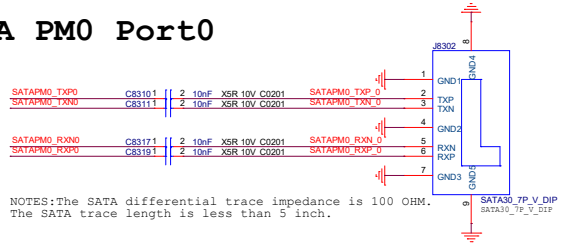
Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	82.SATA-SATA3.0 Slot_7P				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:	Default	Sheet:	82 of 99

SATA PM



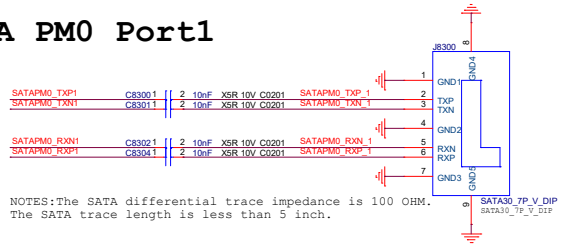


SATA PM0 Port0



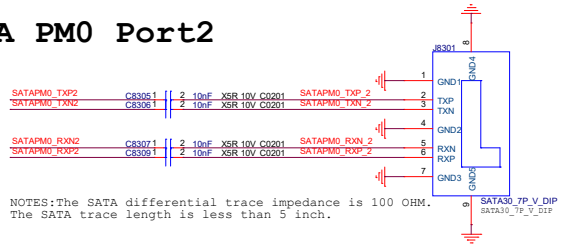
NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

SATA PM0 Port1



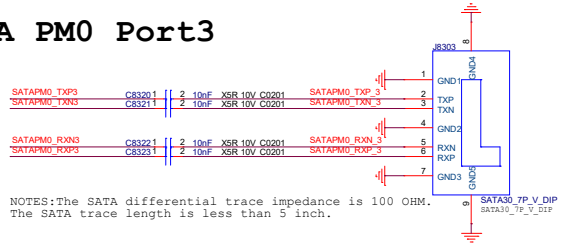
NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

SATA PM0 Port2



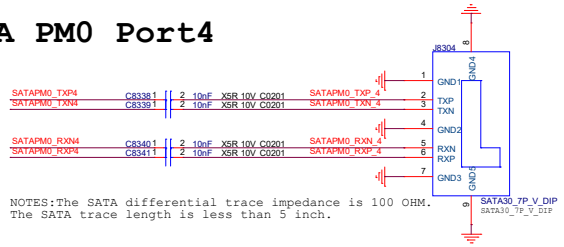
NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

SATA PM0 Port3



NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

SATA PM0 Port4



NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	83.SATA-SATA PM0(option)		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
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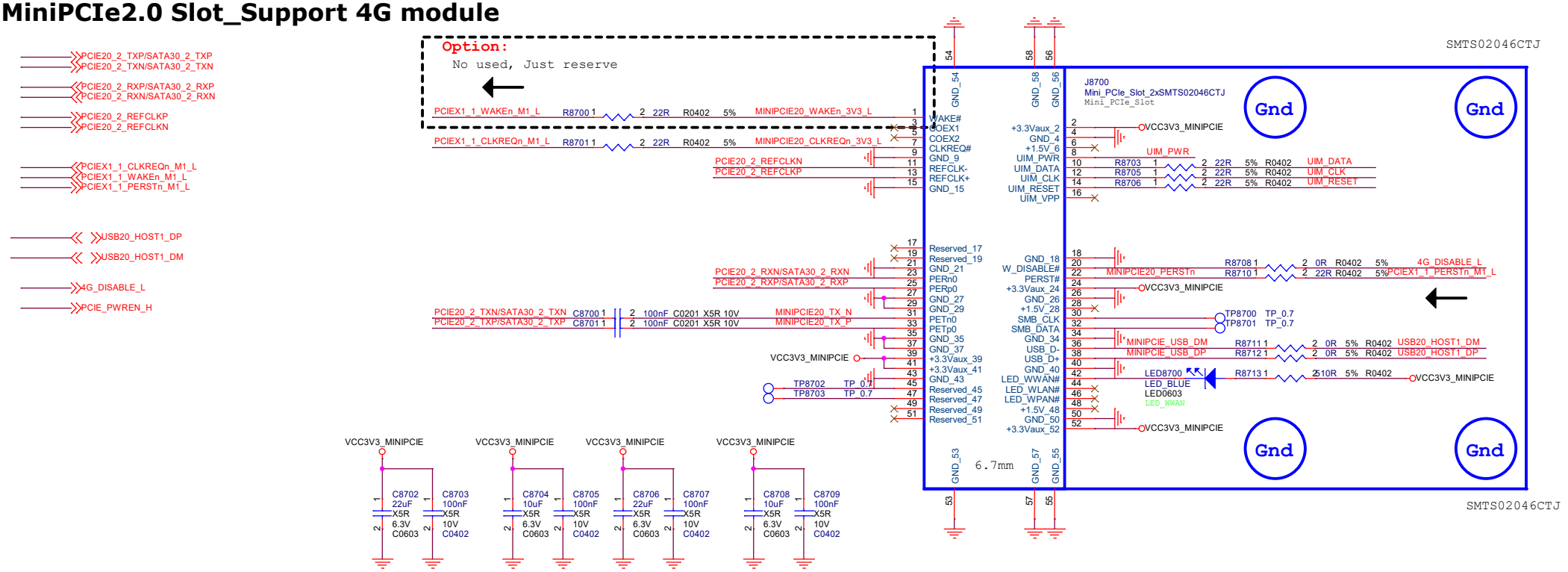
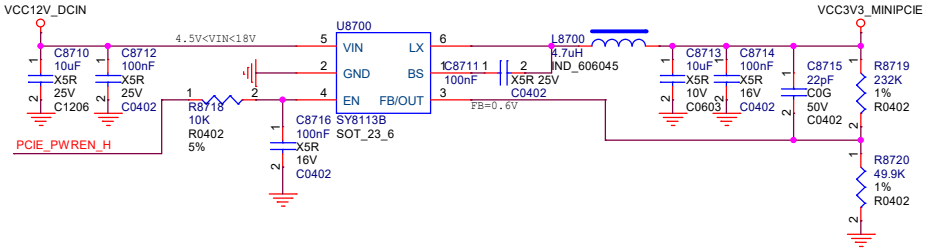
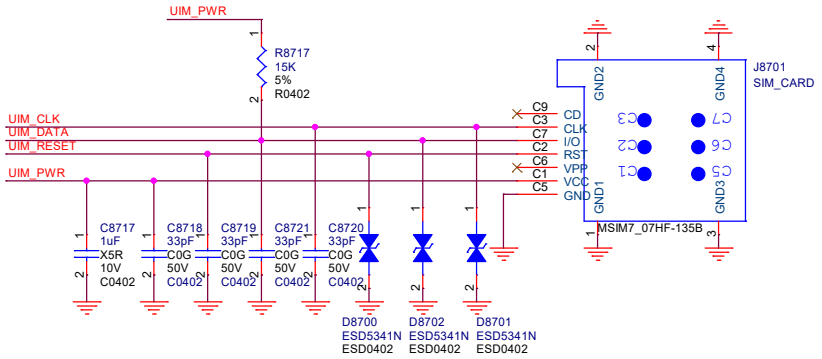
MiniPCIe2.0 Slot_Support 4G module



MiniPCIe2.0 Slot Power



Sim Card



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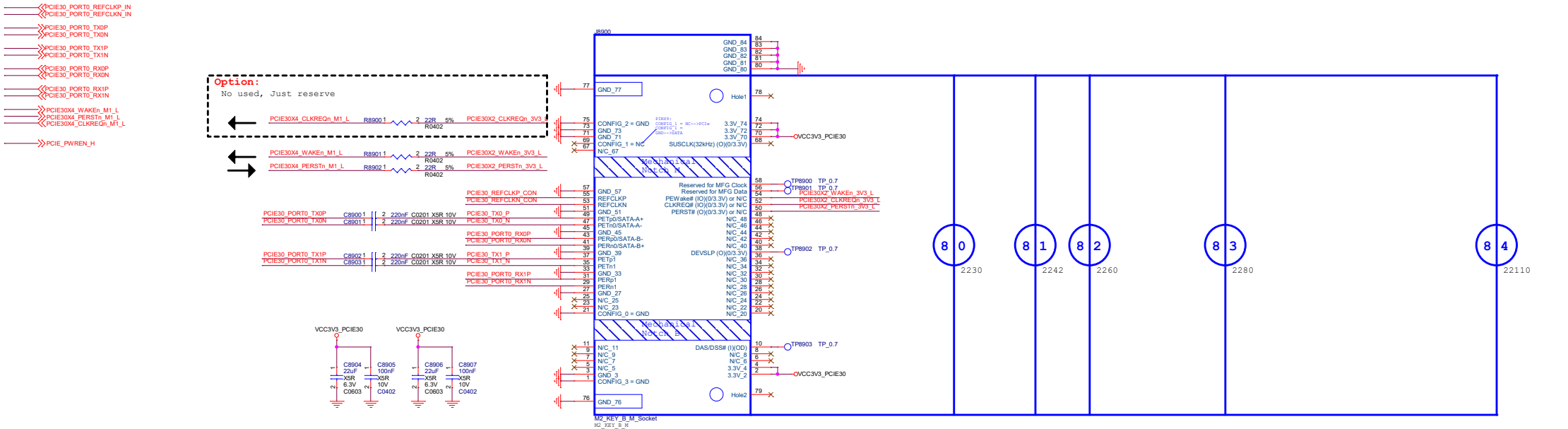
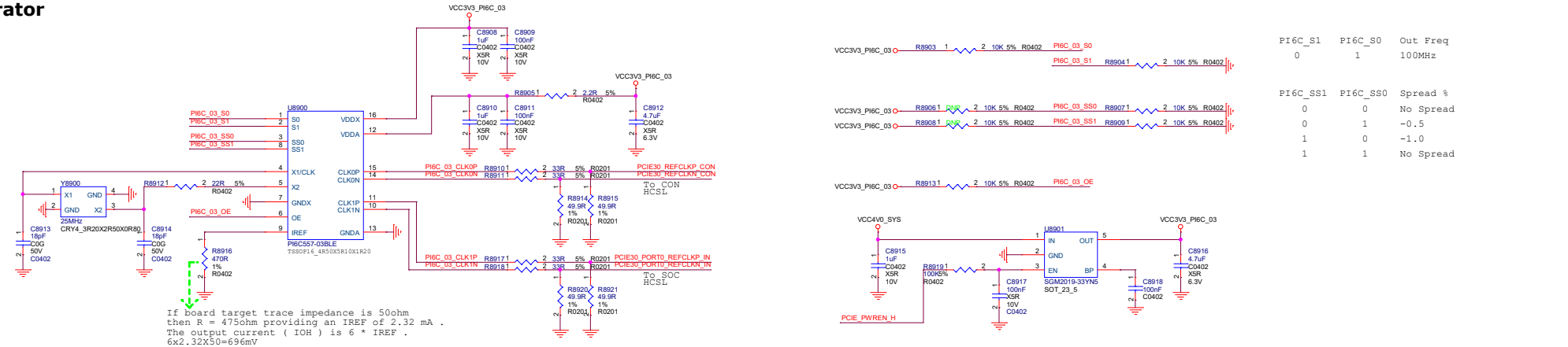
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	87.MiniPCIe2.0 Slot(option)				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:	Default	Sheet:	87 of 99

M.2_PCIe3.0 x 2Lanes



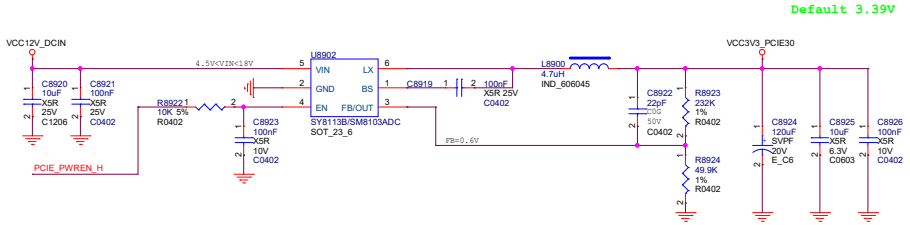
Crystal Generator



PI6C_S1	PI6C_S0	Out Freq
0	1	100MHz

PI6C_SS1	PI6C_SS0	Spread %
0	0	No Spread
0	1	-0.5
1	0	-1.0
1	1	No Spread

M.2 Power



Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	89.PCIE-M.2(option)		
Date:	Wednesday, October 12, 2022	Rev:	V1.3
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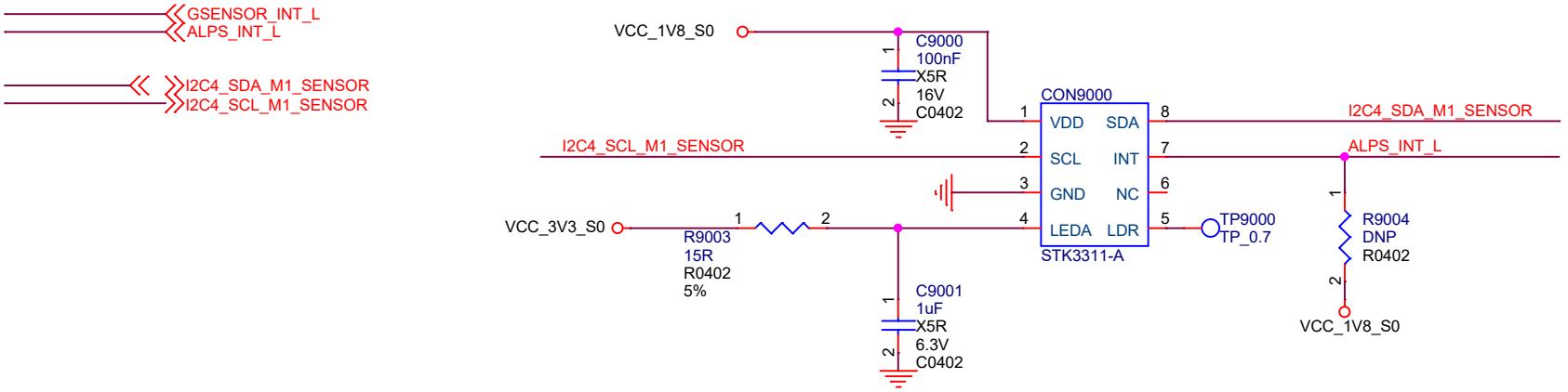
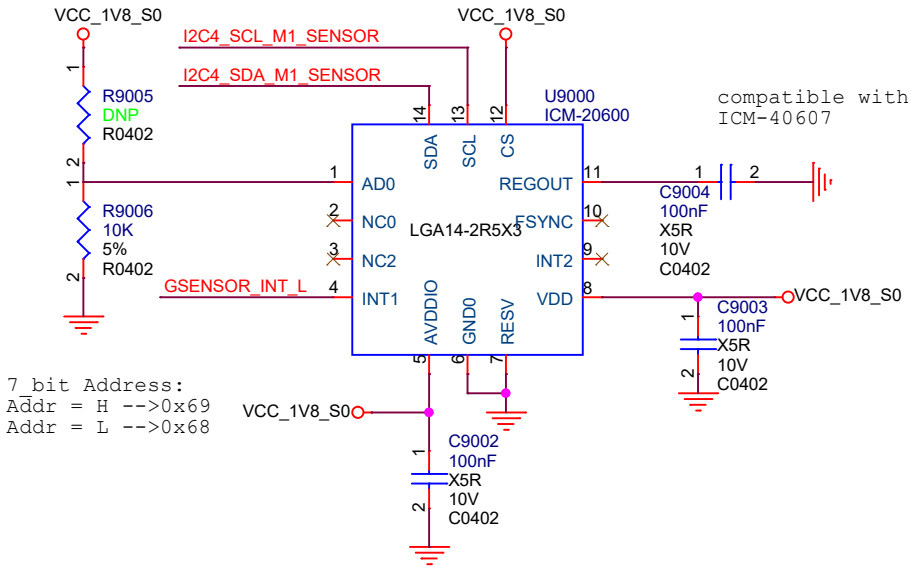
Sensor

Ambient Light+Proximity Sensor



Gyroscope+G-sensor



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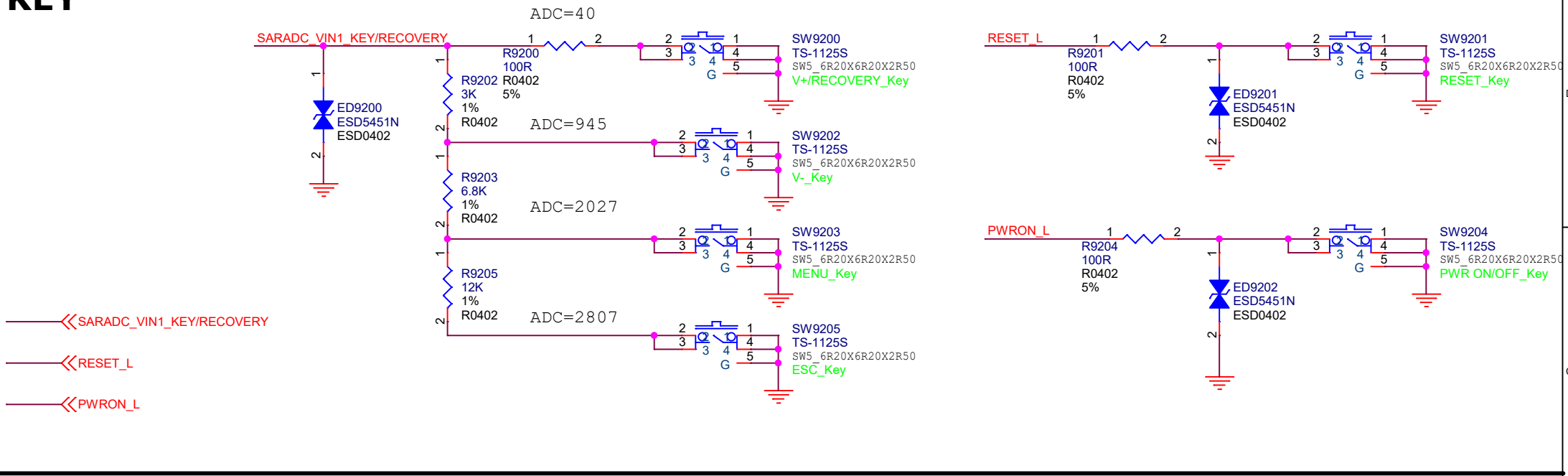
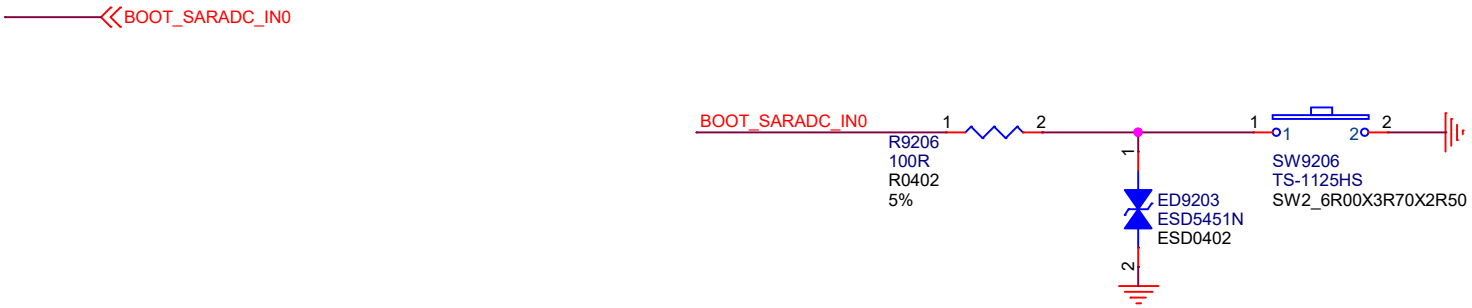
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	90.SENSOR				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:		Sheet:	90 of 99

KEY





Note:

If BOOT_SARADC_IN0=0V after power-on reset, then system will enter into Maskrom mode.

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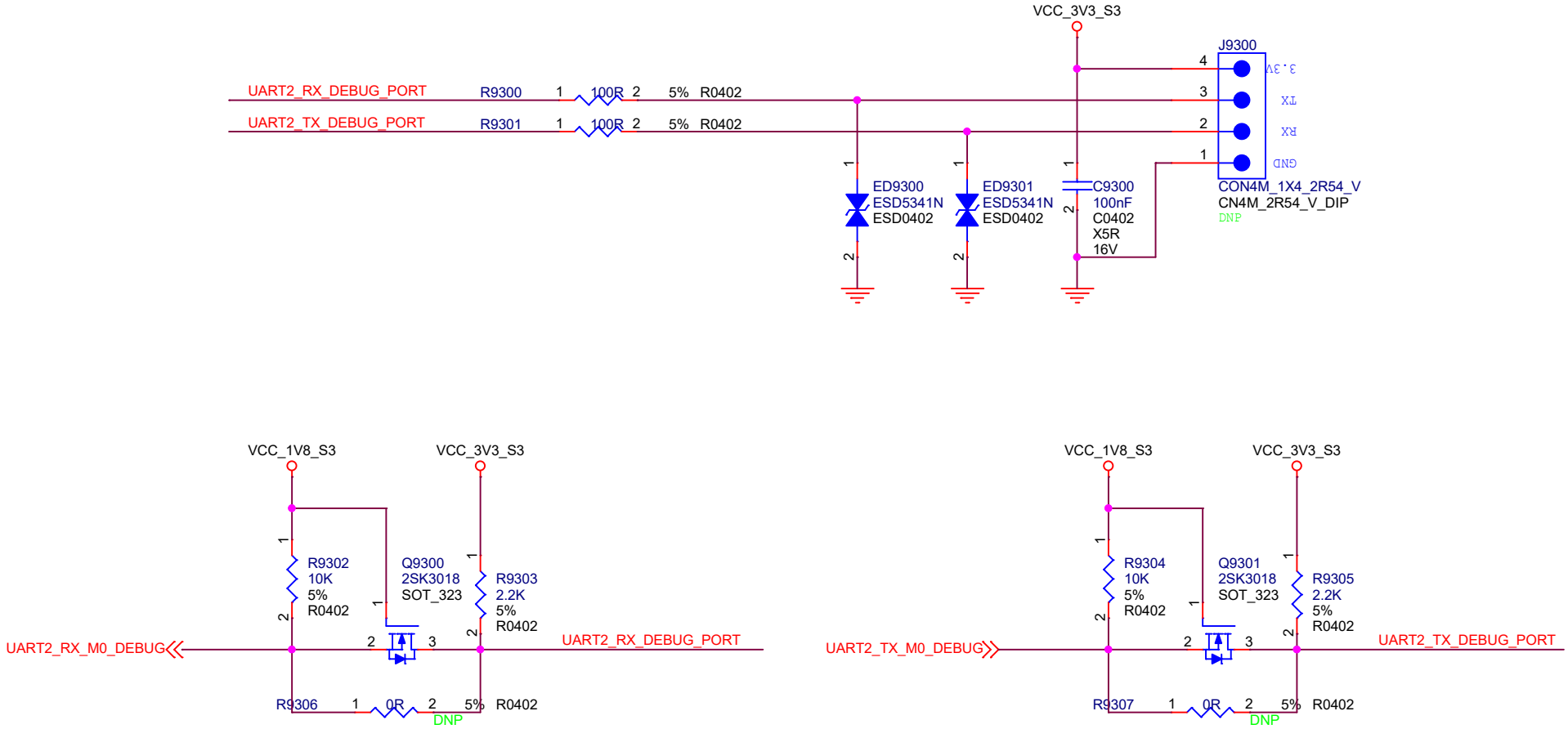
Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	92.KEY Array				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:		Sheet:	92 of 99

UART TO USB(DEBUG)



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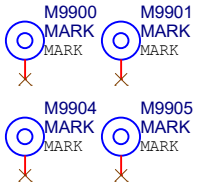
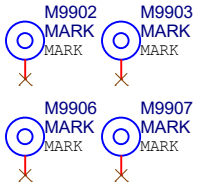
Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	93.Debug UART				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:		Sheet:	93 of 99

Mark

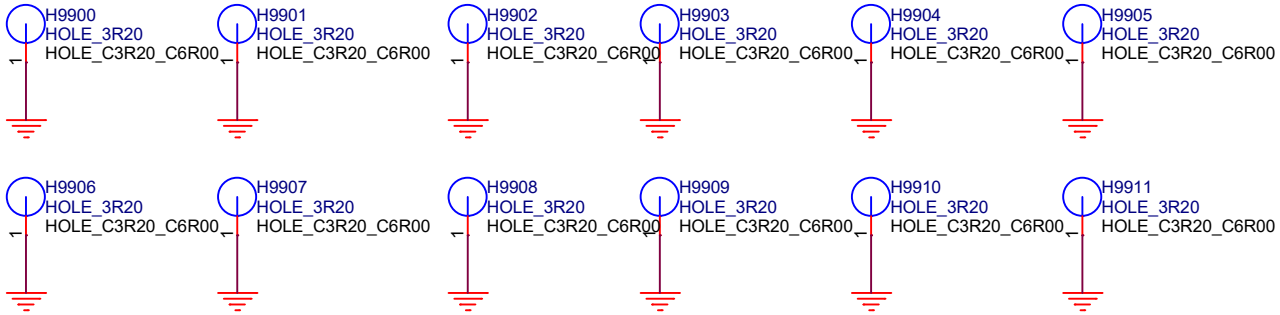
TOP Mark



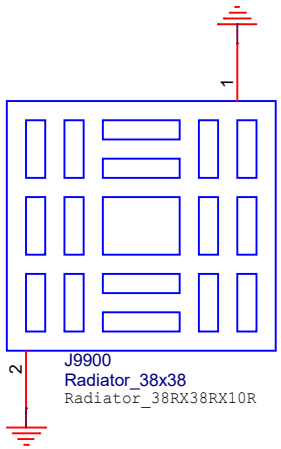
BOTTOM Mark



HOLE



HEATSINK



FAN:8CMX8CM

Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	**RK3588_AIOT_SCH**				
File:	**99.Mark/Hole/Heatsink**				
Date:	Wednesday, October 12, 2022			Rev:	V1.3
Designed by:	RZF	Reviewed by:		Sheet:	99 of 99