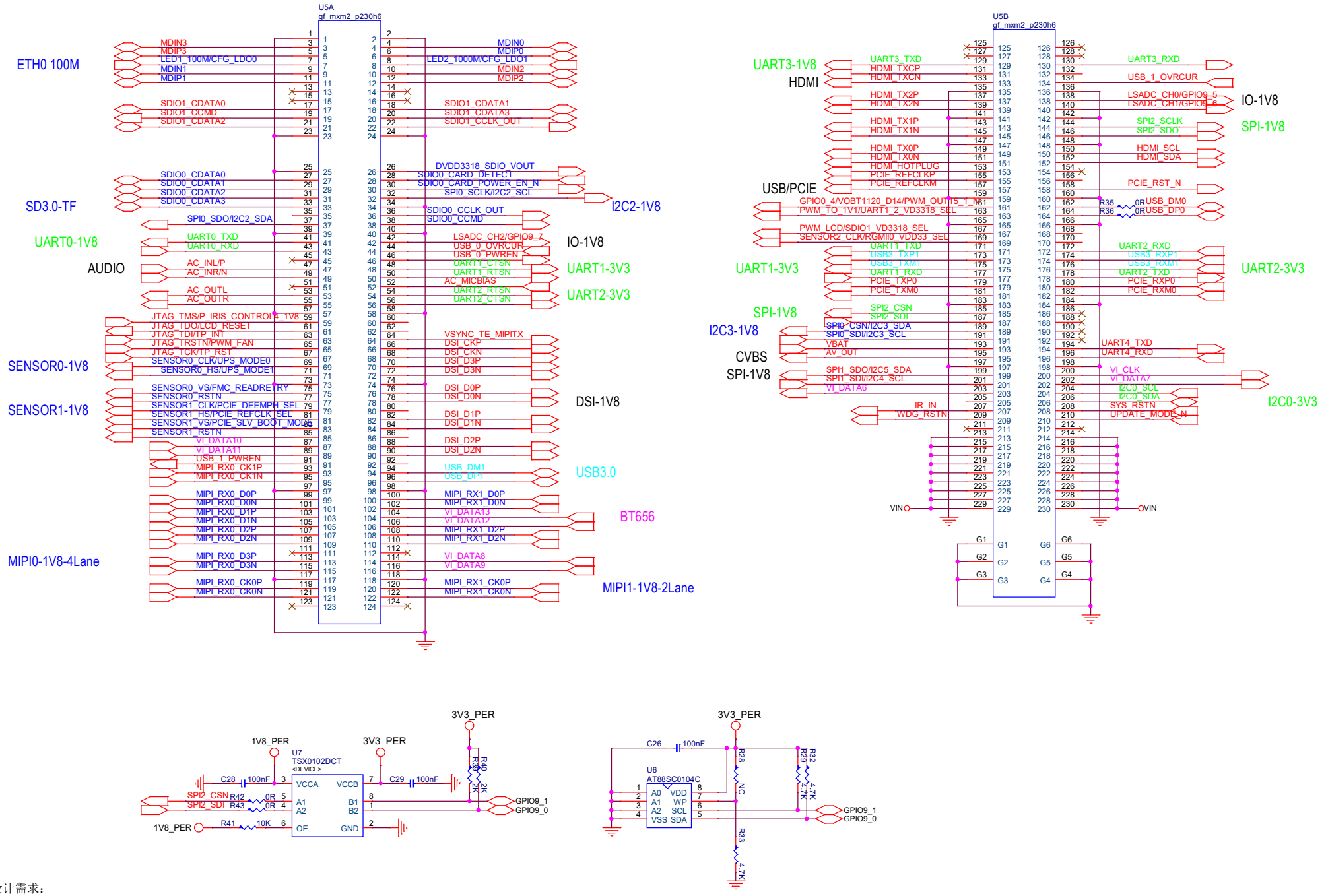


设计需求：

1.板卡尺寸：按照U5:MXM2封装绘制板框，定位孔不变，板厚1.2mm

2.MIPI0、1，DSI，ETH，HDMI信号做差分等长处理，阻抗100欧姆制作

3.SDIO0、1信号做等长，阻抗单端50欧姆制作

4.CVBS信号，阻抗单端50欧姆制作

5.USB/PCIE信号做差分等长，阻抗90欧姆制作

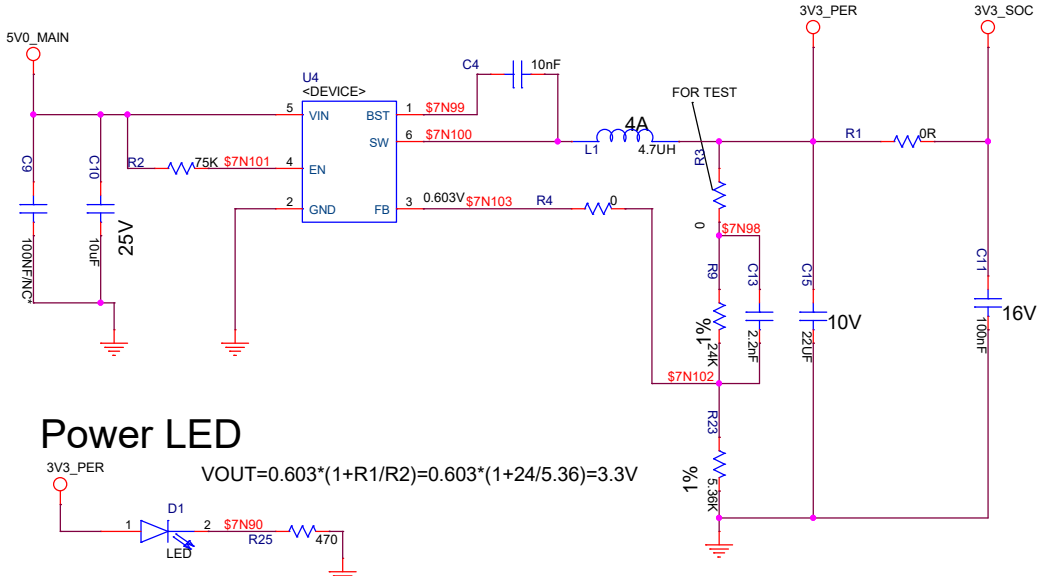
The type and specification of the components refer to the BOM

				NA	
				ECA NO	DATE
DESIGNED					
REVIEWED		SS928V100DMEB			
		VER	PART_NUMBER	SHEET 5 of 22	
		A			

Power Supply1

5V -> 3.3V

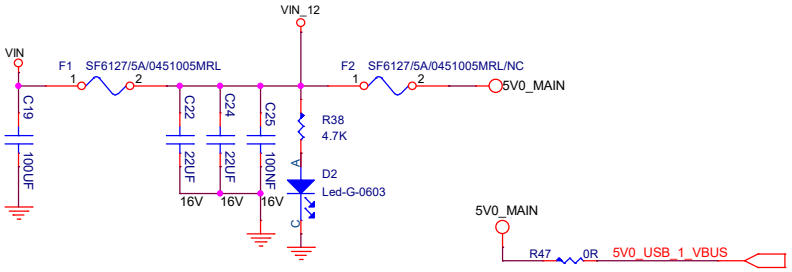
3A



Power LED

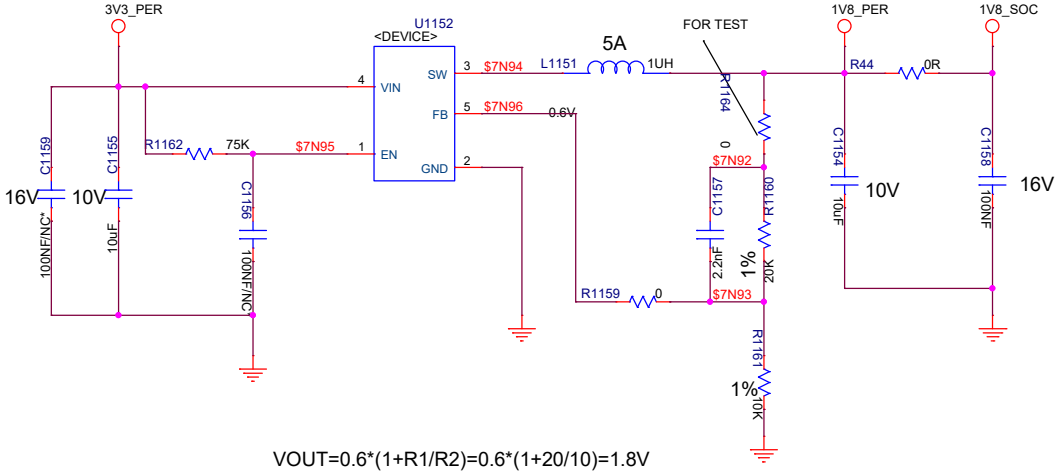
VOUT=0.603*(1+R1/R2)=0.603*(1+24/5.36)=3.3V

Power IN



3.3V->1.8V

2A



VOUT=0.6*(1+R1/R2)=0.6*(1+20/10)=1.8V

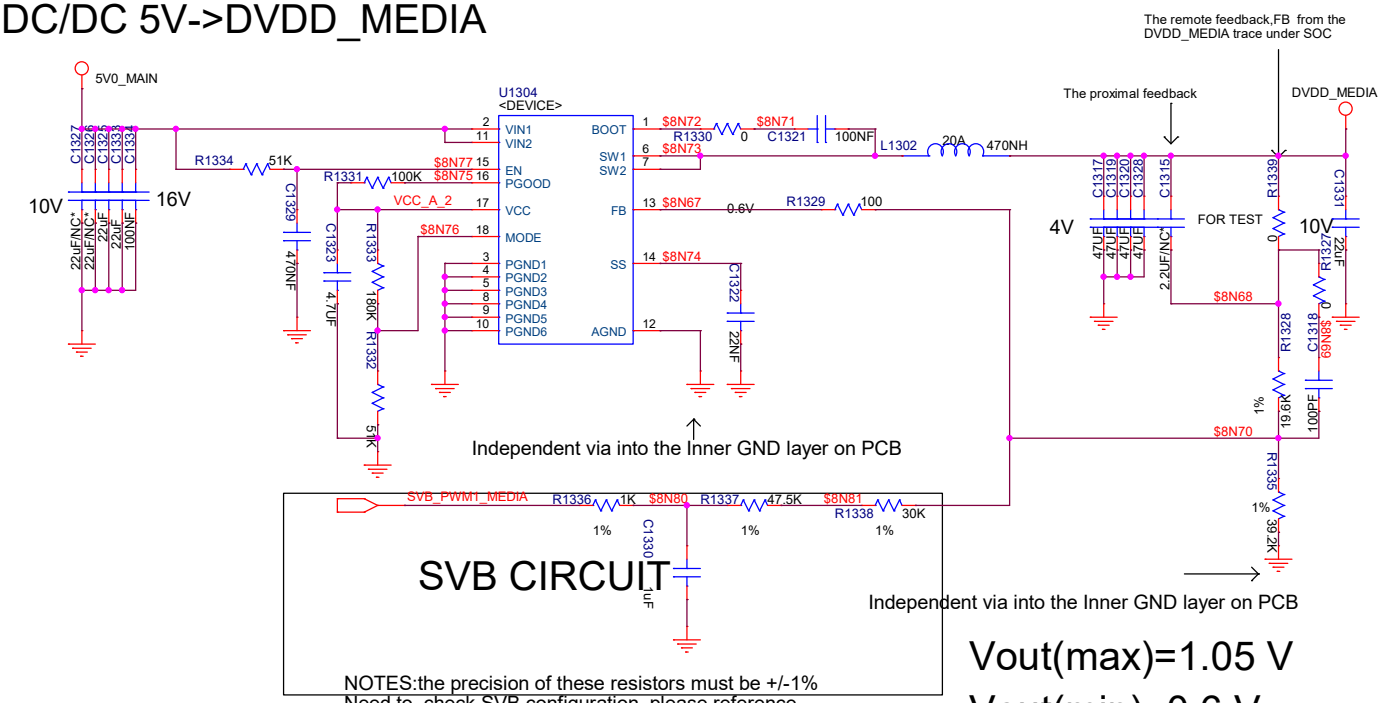
The type and specification of the components refer to the BOM

				NA	
				ECA NO	DATE
DESIGNED		SS928V100DMEB			
REVIEWED					
		VER	PART_NUMBER	SHEET 6 of 22	
		A			

Power Supply2

DC/DC 5V->DVDD_MEDIA

12A

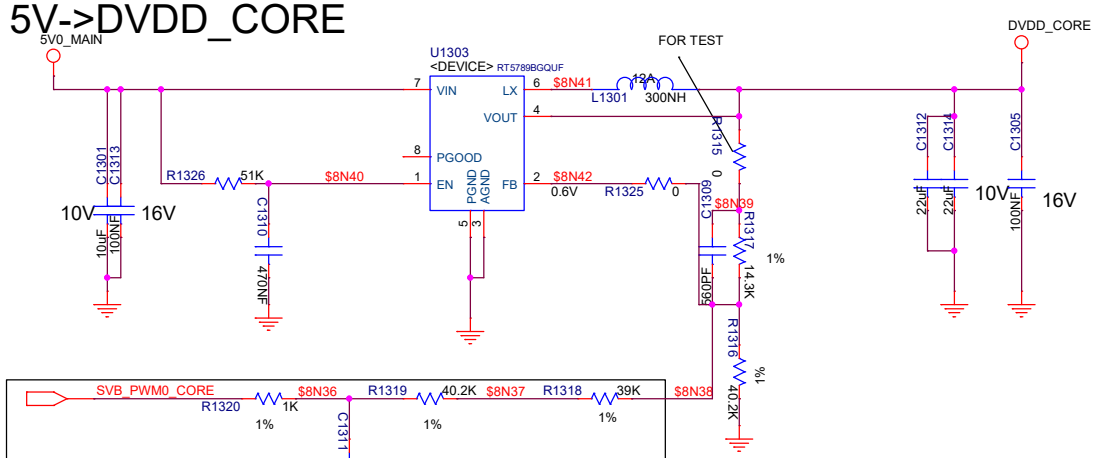


NOTES:the precision of these resistors must be +/-1%
Need to check SVB configuration ,please reference
to deliverables 02.only for reference\SVB\svb_check_tool

Vout(max)=1.05 V
Vout(min)=0.6 V

DC/DC 5V->DVDD_CORE

6A



NOTES:the precision of these resistors must be +/-1%
Need to check SVB configuration ,please reference
to deliverables 02.only for reference\SVB\svb_check_tool

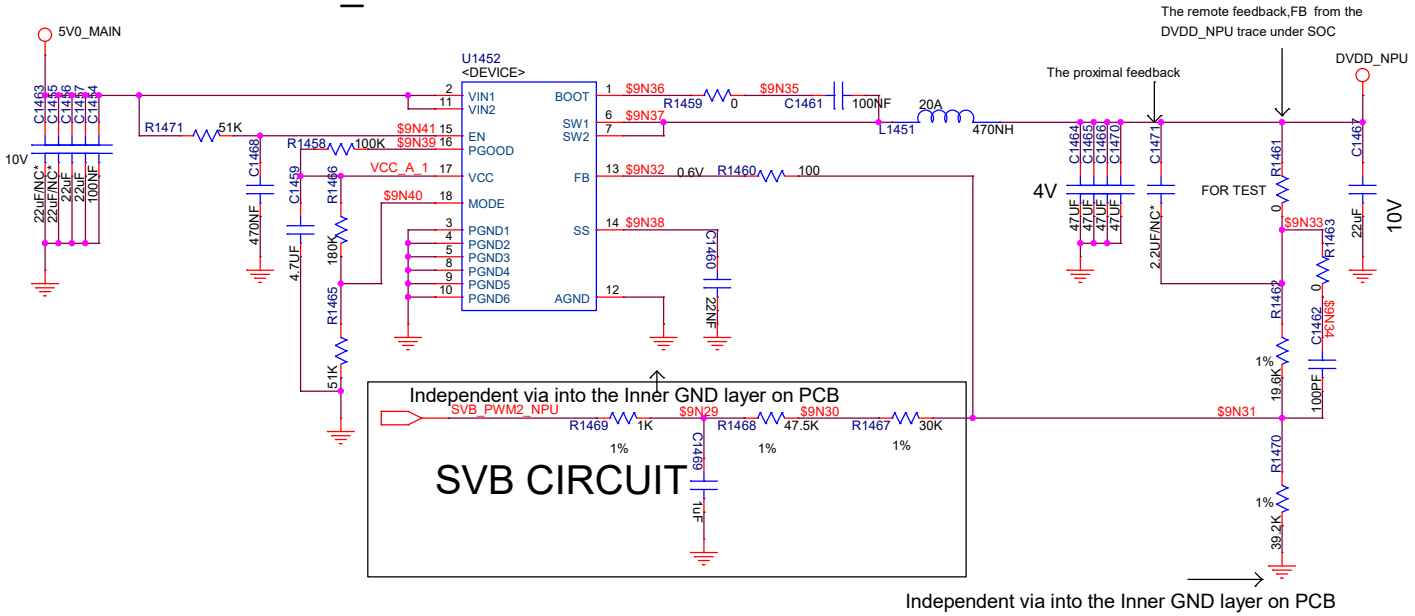
Vout(max)= 0.92V
Vout(min)=0.6 V

The type and specification of the components refer to the BOM

				NA	
				ECA NO	DATE
DESIGNED					
REVIEWED		SS928V100DMEB			
		VER	PART_NUMBER	SHEET 7 of 22	
		A			

Power Supply3

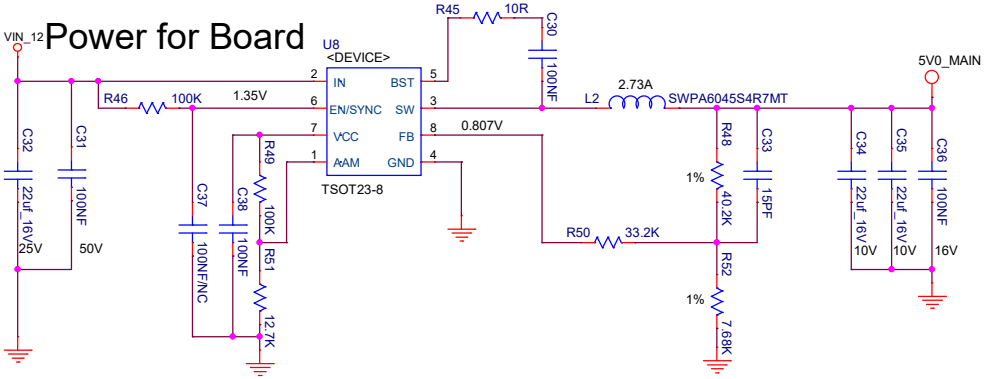
DC/DC 5V->DVDD_NPU



NOTES:the precision of these resistors must be +/-1%
Need to check SVB configuration ,please reference to deliverables 02.only for reference\SVB\svb_check_tool

Vout(max)=1.05V
Vout(min)=0.6V

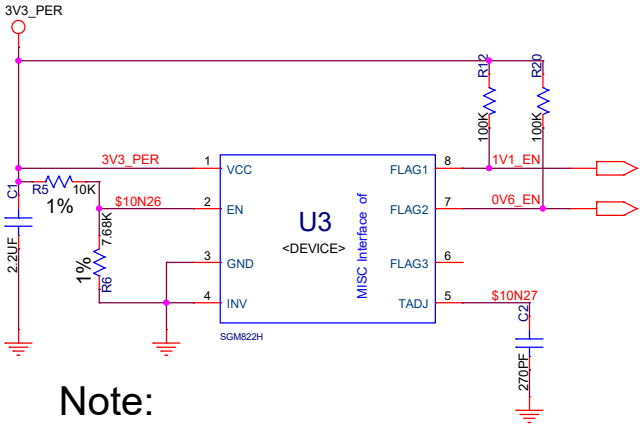
Power for Board



The type and specification of the components refer to the BOM

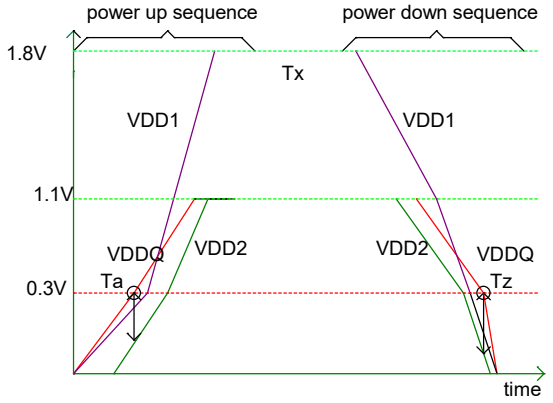
				NA	
				ECA NO	DATE
DESIGNED					
REVIEWED			SS928V100DMEB		
		VER	PART_NUMBER	SHEET 8 of 22	
		A			

LPDDR4/4X Power sequence



Note:
V=2.8V
VTH=1.22V

Note:The power sequence is a protocol specification for LPDDR4/4X.



power up sequence

After	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ-200mV

Ta is the point when any power supply first reaches 300mV

power down sequence

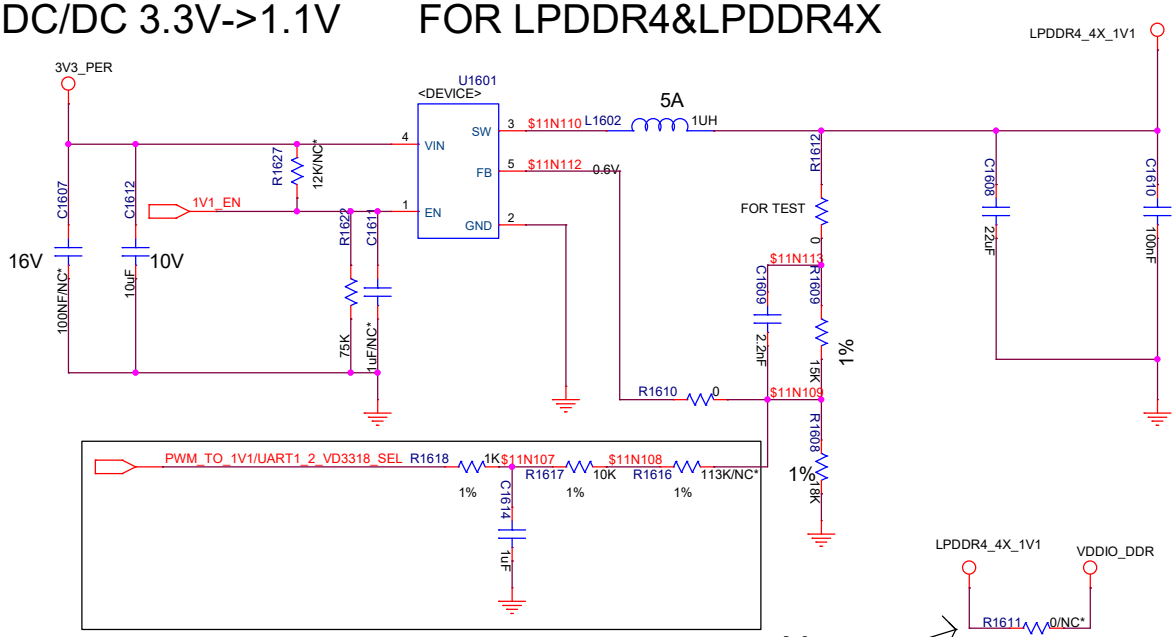
After	Applicable Conditions
Tx and Tz	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ-200mV

Tx is the point where any power supply drops below the mini value specified.
Tz is the point where all power supply are below 300mV.After Tz,the device is power off.

The type and specification of the components refer to the BOM

				NA	
				ECA NO	DATE
DESIGNED					
REVIEWED			SS928V100DMEB		
		VER	PART_NUMBER	SHEET 9 of 22	
		A			

DC/DC 3.3V->1.1V FOR LPDDR4&LPDDR4X



SVB CIRCUIT just for testing.Conventional design,SVB CIRCUIT is not required,set LPDDR4_4X_1V1 to 1.1V

VOUT=0.6*(1+R1/R2)=0.6*(1+15/18)=1.1V

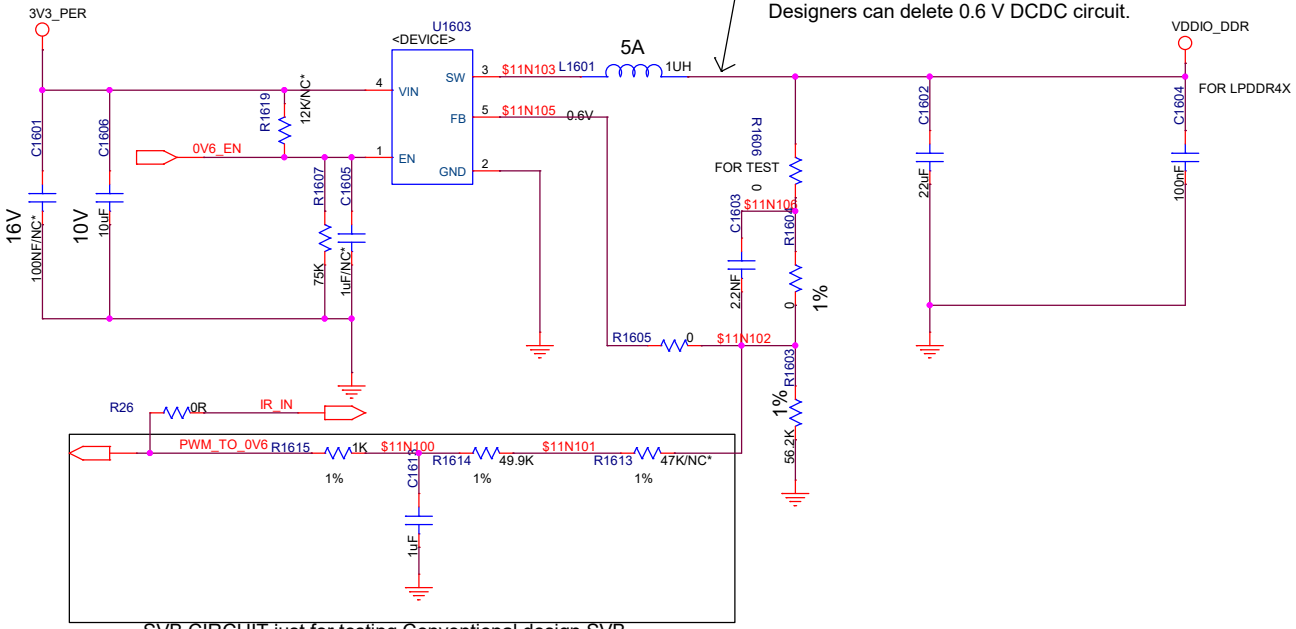
Note

SS928V100 default LPDDR4X

LPDDR4X_0V6_COM power supply is just used for LPDDR4X, if the product only supports LPDDR4, please connect VDDIO_DDR to LPDDR4_4X_1V1. Designers can delete 0.6 V DCDC circuit.

DC/DC 3.3V->0.6V FOR LPDDR4X

2A



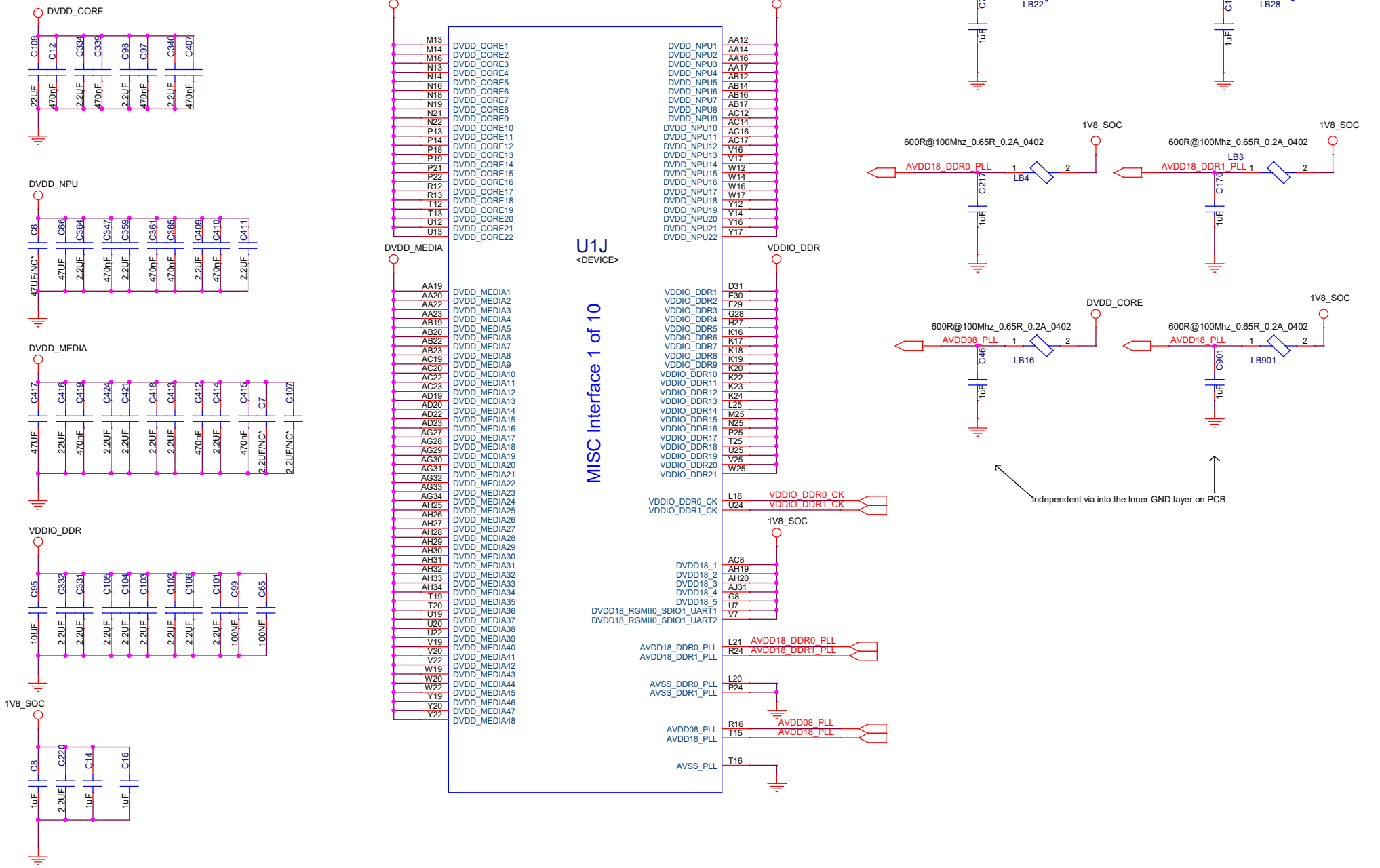
SVB CIRCUIT just for testing.Conventional design,SVB CIRCUIT is not required,set VDDIO_DDR to 0.6V

VOUT=0.6*(1+R1/R2)=0.6*(1+0/56.2)=0.6V

The type and specification of the components refer to the BOM

				NA	
				ECA NO	DATE
DESIGNED					
REVIEWED			SS928V100DMEB		
			VER	PART_NUMBER	SHEET 10 of 22
			A		

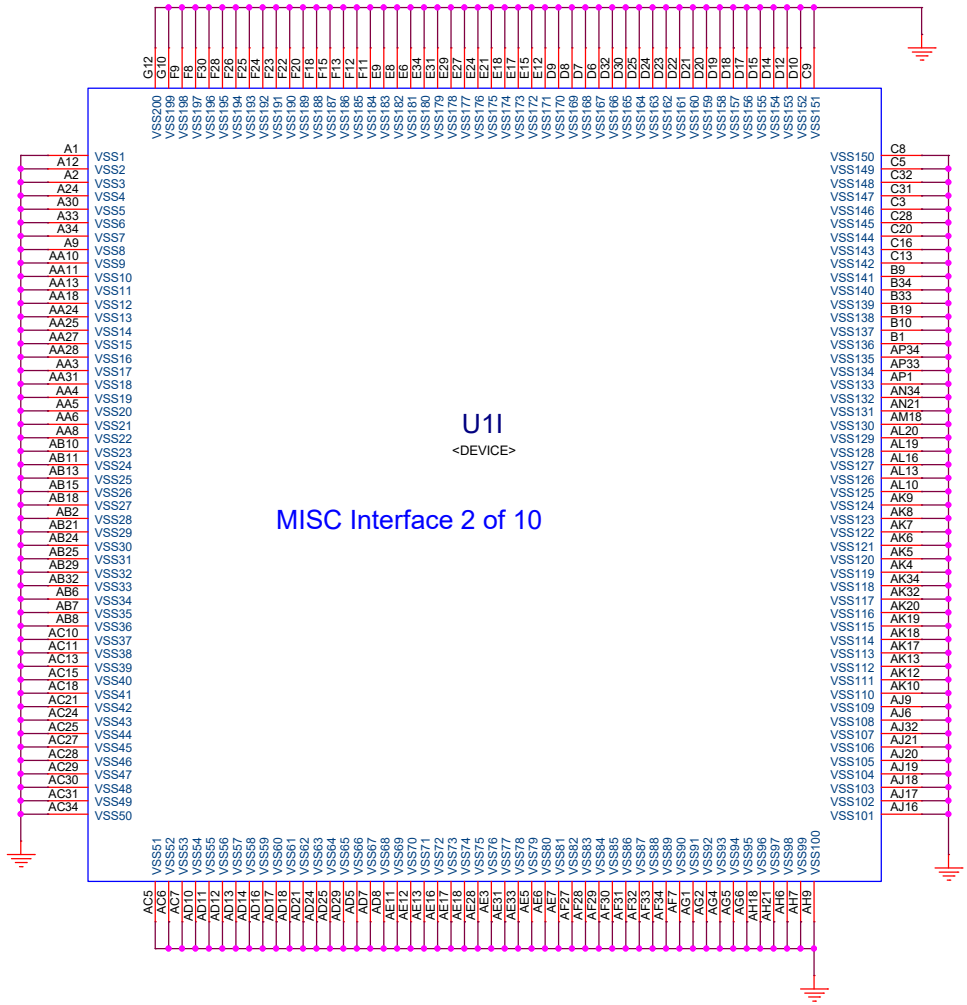
Power of core

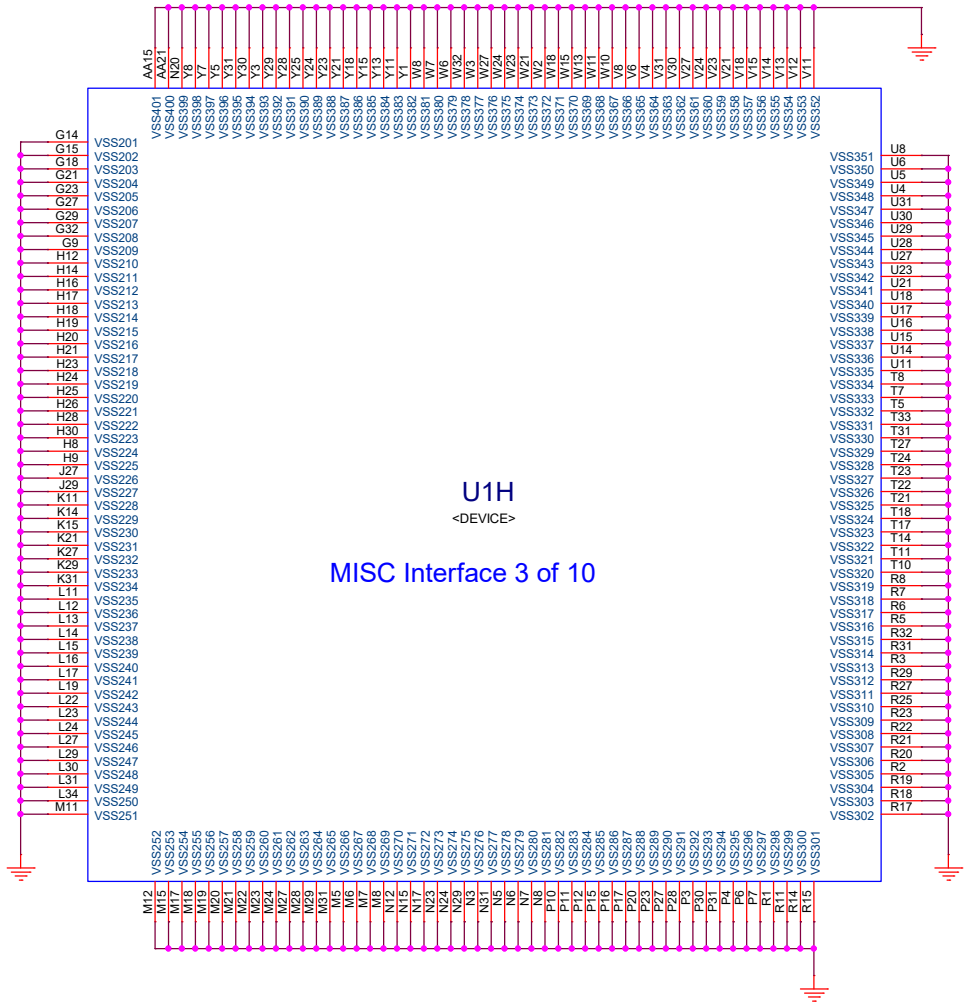


The type and specification of the components refer to the BOM

				NA	
				ECA NO	DATE
DESIGNED					
REVIEWED		SS928V100DMEB			
		VER	PART_NUMBER	SHEET 11 of 22	
		A			

GND of core





The type and specification of the components refer to the BOM

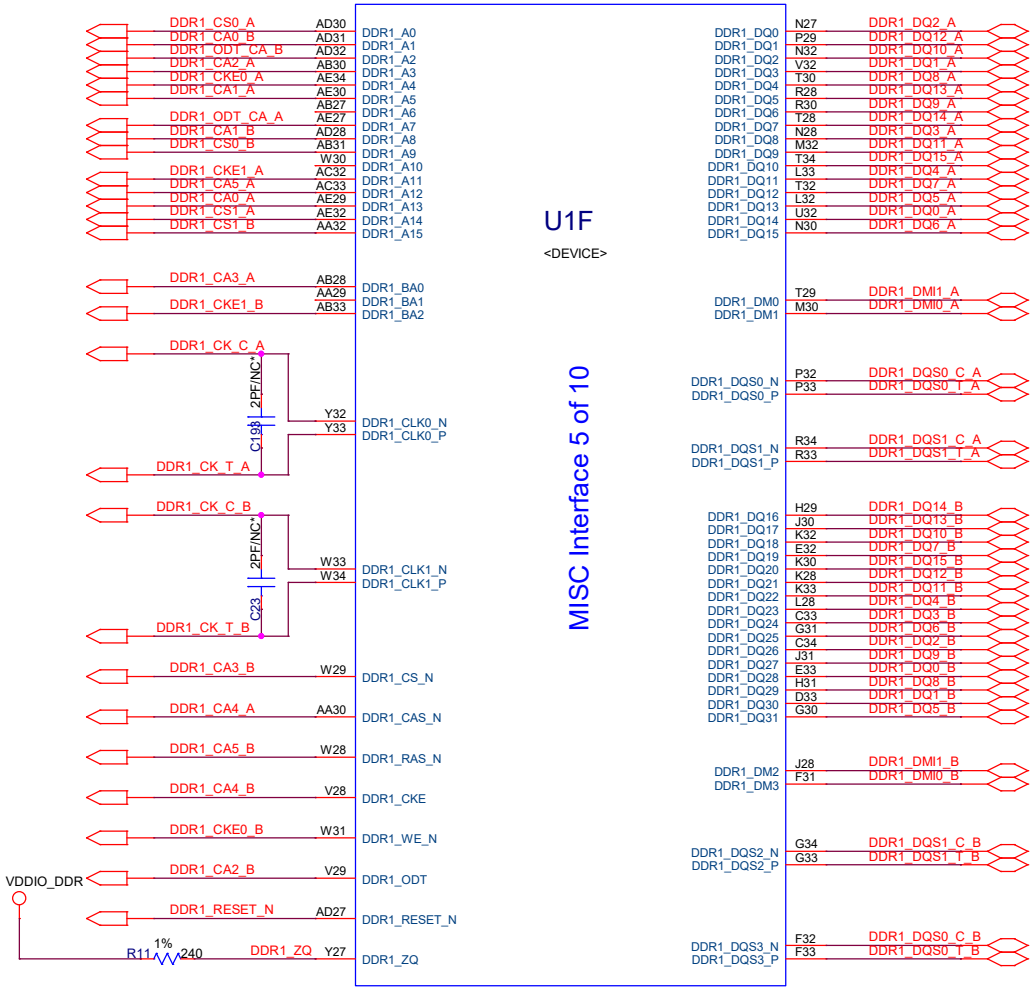
				NA	
				ECA NO	DATE
DESIGNED		SS928V100DMEB			
REVIEWED					
		VER	PART_NUMBER	SHEET 12 of 22	
		A			

DDRC0 of core

The type and specification of the components refer to the BOM

				NA	
				ECA NO	DATE
DESIGNED		SS928V100DMEB			
REVIEWED					
		VER	PART_NUMBER	SHEET 13 of 22	
		A			

DDRC1 of core



The type and specification of the components refer to the BOM

				NA	
				ECA NO	DATE
DESIGNED		SS928V100DMEB			
REVIEWED					
		VER	PART_NUMBER	SHEET 15 of 22	
		A			

SYS

Note:
The CL range of 24Mhz crystal is constained to 8-18pf,
it is suggested that customers to choose CL=12pf crystal.
The DL SPEC of the XTAL is 200uw.

C284 18pF — X3 24MHZ — GND2GND1 — R180 1MEG/NC* — R183 0 — $18N153 — just for test — $18N154 — C285 18pF — R152 470 — XIN / XOUT

1V8_SOC — 1000R@100Mhz_1.25R_0.25A_0402 LB13 — AVDD18_LSADC — C198 1uF

WDG_RSTN R31 0 — SYS_RSTN_OUT R30 0/NC* — WDG_RSTN/SYS_RSTN_OUT

5V0_MAIN — R515 27.4K 1% — AVDD18_PFI — R514 11.8K 1%

Note:
VL=4V
VTH_L=1.2V

For the sake of monitoring system power, R515 must be connected to the DC DC input power supply (5V0_MAIN)of DVDD_CORE ,When the 5V power down to 4 V, then AVDDD18_PFI = 1.2 V, the system automatically reset.

I2C address:0110010

3V3_PER — R2655 1K — OSC2651 <DEVICE> (T1, SCL, SDA, FOE, T2 / FOUT, INT, VDD, VBAT, GND) — I2C0_SCL / I2C0_SDA — $18N158 — $18N159 — $18N160 — R2654 1K — C2651 100nF — D2651 — VBAT — C2652 100nF

0x64

NOTES:(very important!!!)
when use RTC function and Coin battery,pay attention to the circuit.
you must use two same Schottky diode.
the forward voltage of Schottky diode VF<0.3V.

1V8_SOC — P8 DVDD18_OSC — XIN P2 — XOUT P1 — AVDD18_PFI R10 — AVDD18_LSADC AH17 — AVSS_LSADC AH16

LSADC_CH0/GPIO9_5 AN16 — LSADC_CH1/GPIO9_6 AP16 — LSADC_CH2/GPIO9_7 AN17 — PCIE_RST_N AP17

POR_ENABLE AL18 — SYS_RSTN AL17 — WDG_RSTN/SYS_RSTN_OUT AM16

SVB_PWM1_MEDIA P5 — SVB_PWM2_NPU N4 — SVB_PWM0_CORE R4 — $18N148 AJ33 — R2651 33 — SENSOR2_CLK/RGMII0_VDD33_SEL

PWM_LCD/SDIO1_VD3318_SEL AJ34

JTAG_TCK/TP_RST AL14 — JTAG_TDI/TP_INT AK15 — JTAG_TDO/LCD_RESET AK14 — JTAG_TMS/P_IRIS_CONTROL4_1V8 AL15 — JTAG_TRSTN/PWM_FAN AK16

PWM_TO_1V1/UART1_2_VD3318_SEL AL6 — GPIO0_4/VOBT1120_D14/PWM_OUT15_1_N AL5

U1E <DEVICE> — MISC Interface 8 of 10

SVB_PWM1/GPIO2_4 — SVB_PWM2/GPIO2_5 — SVB_PWM0/GPIO2_3 — PWM0_OUT0_0_P/GPIO16_7 — SENSOR0_CLK/SENSOR1_CLK — SENSOR2_CLK — RGMII0_IO_VDD33_SEL — PWM0_OUT1_0_P/GPIO17_0 — SDIO1_IO_VDD3318_SEL

JTAG_TCK/GPIO10_2/I2S_SD_TX — SPI3_SDI/UART5_TXD — PWM0_OUT13_0_P/PWM0_OUT15_2_N — JTAG_TDI/GPIO10_5/I2S_MCLK — SPI3_SCLK/PWM0_OUT10_0_P — JTAG_TDO/GPIO10_4/I2S_BCLK — SPI3_CSN/UART5_CTSN — PWM0_OUT11_0_P — JTAG_TMS/GPIO10_3/I2S_WS — SPI3_SDO/UART5_RTSN — PWM0_OUT12_0_P/PWM0_OUT15_2_P — JTAG_TRSTN/GPIO10_1/I2S_SD_RX — UART5_RXD/PWM0_OUT14_0_P — PWM0_OUT15_1_P

GPIO0_3/VO_BT1120_DATA15 — UART1_2_IO_VDD3318_SEL — PWM0_OUT15_0_P — GPIO0_4/VO_BT1120_DATA14 — RGB_DATA16/PWM0_OUT15_1_N

AVDD18_EMMC1 K12 — AVDD18_EMMC2 K13 — C127 1uF

EMMC_CLK/GPIO0_5/NF_DQ6 C7 — EMMC_CMD/GPIO0_6/NF_DQ7 B8 — EMMC_DATA0/GPIO0_7/NF_WEN B5 — EMMC_DATA1/GPIO1_0/NF_ALE A4 — EMMC_DATA2/GPIO1_1/NF_CLE B4 — EMMC_DATA3/GPIO1_2/NF_DQ3 B6 — EMMC_DATA4/SFC_WP_IO2/NF_DQ0 A5 — EMMC_DATA5/SFC_HOLD_IO3/NF_DQ2 A6 — EMMC_DATA6/SFC_MISO_IO1/NF_DQ1 C6 — EMMC_DATA7/SFC_CLK/NF_CSN A3 — EMMC_DS/SFC_MOSI_IO0/NF_DQ4 A7 — EMMC_RST_N/GPIO1_3/NF_DQ5 B7 — SFC_CS0N/NF_REN/GPIO1_4 B3 — SFC_CS1N/NF_RDY/PCIE_RST_N B2 — GPIO1_5 — EMMC_IO_ZCOMP E7

$18N46 0 — R92 — EMMC_CLK
EMMC_CMD
EMMC_DATA0
EMMC_DATA1
EMMC_DATA2
EMMC_DATA3
EMMC_DATA4/SFC_WP_IO2
EMMC_DATA5/SFC_HOLD_IO3
EMMC_DATA6/SFC_MISO_IO1
$18N45 10 — R2652 — EMMC_DATA7/SFC_CLK
EMMC_DS/SFC_MOSI_IO0
EMMC_RST_N
SFC_CS0N
PCIE_RSTN_SYS

EMMC_IO_ZCOMP — R223 1% 200

If this group of I/O is used as common GPIO, when designer wants the default I/O status to be high, It needs to be pulled up by 4.7KΩ when designer wants the default I/O status to be low,It needs to be pulled down by 1KΩ

DVDD33_RGMII0_1 U10 — DVDD33_RGMII0_2 V10 — C2652 1uF

3V3_SOC

Very important!!!
Notes:

the voltage difference between DVDD33_RGMII0 and DVDD18 within 1.98V during power-on and power-off. Or the total time is less than 4ms

when the voltage difference between DVDD33_RGMII0 and DVDD18 is more than 1.98V during power-on and power-off. RGMII0_IO_VDD33_SEL need to be pulled down,.if that is wrongly used , these I/O pins may be damaged.

EPHY0_CLK/GPIO4_2 — EPHY0_RSTN/GPIO4_3 — RGMII0_RXCK/GPIO3_3 — RGMII0_RXD0/RMII0_RXD0/GPIO3_1 — RGMII0_RXD1/RMII0_RXD1/GPIO3_0 — RGMII0_RXD2/GPIO2_7 — RGMII0_RXD3/GPIO2_6 — RGMII0_RXDV/RMII0_RXDV_CRS — GPIO3_2

$18N51 33 — R2653 — EPHY0_CLK
EPHY0_RSTN
RGMII0_RXCK
RGMII0_RXD0
RGMII0_RXD1
RGMII0_RXD2
RGMII0_RXD3
RGMII0_RXDV

RGMII0_TXCKOUT/TEST_CLK — RMII0_CLK/GPIO4_1 — RGMII0_TXD0/RMII0_TXD0/GPIO3_7 — FAST_BOOT_MODE — RGMII0_TXD1/RMII0_TXD1/GPIO3_6 — SFC_EMMC_BOOT_MODE — RGMII0_TXD2/GPIO3_5/BOOT_SEL1 — RGMII0_TXD3/GPIO3_4/BOOT_SEL0 — RGMII0_TXEN/RMII0_TXEN/GPIO4_0

$18N50 33 — R142 — RGMII0_TXCKOUT
$18N49 33 — R141 — RGMII0_TXD0/FAST_BOOT_MODE
$18N48 33 — R140 — RGMII0_TXD1/SFC_EMMC_BOOT_MODE
$18N47 33 — R139 — RGMII0_TXD2/BOOT_SEL1
$18N26 33 — R138 — RGMII0_TXD3/BOOT_SEL0
$18N31 33 — R137 — RGMII0_TXEN

MDIO0/GPIO4_5 — MDCK0/GPIO4_4

$18N27 33 — R159 — MDIO0 / MDCK0

3V3_PER

GPIO0_0/UPDATE_MODE_N — RGMII1_TXEN/RMII1_TXEN — PWM1_OUT15_0_P — DVDD3318_SDIO1 — GPIO0_1/IR_IN/EPHY1_CLK — PWM1_OUT14_0_P

UPDATE_MODE_N — R350 2K — R147 2K

IR_IN — R21 1K

I2C0_SCL / I2C0_SDA

I2C0_SCL/GPIO11_5 — I2C0_SDA/GPIO11_4 — 5V tolerence

Based on the use of scenarios,I2C0 can be pull up to 1.8V,3.3V,5V

TEST_MODE — AM17 TEST_MODE — R238 4.7K/NC*

	FUNCTION
0	normal mode
1	test mode

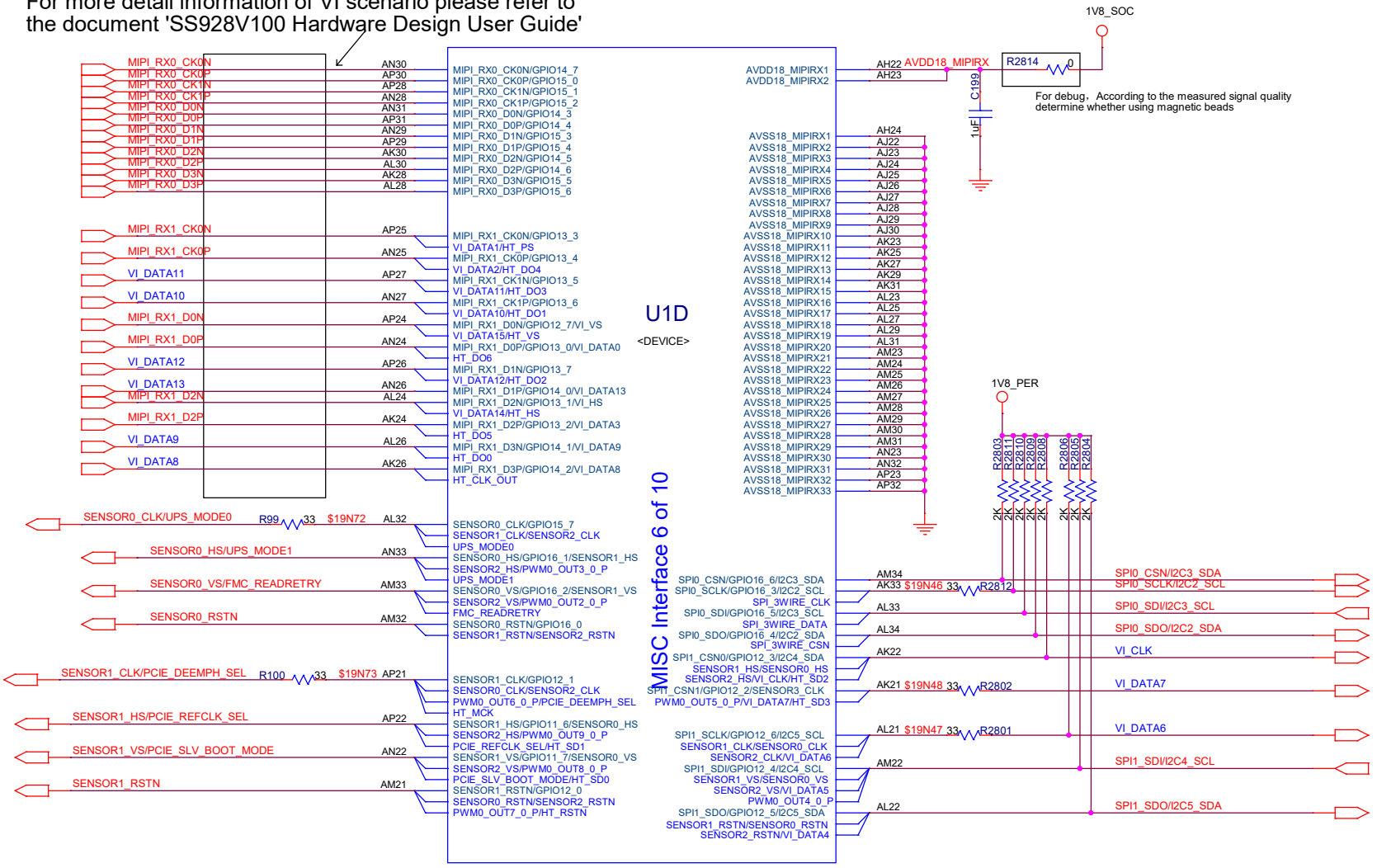
The type and specification of the components refer to the BOM

				NA	
				ECA NO	DATE
DESIGNED					
REVIEWED		SS928V100DMEB			
		VER	PART_NUMBER	SHEET 17 of 22	
		A			

VI&SENSOR CONTROL

The MIPI RX differential trace impedance is 100ohm.

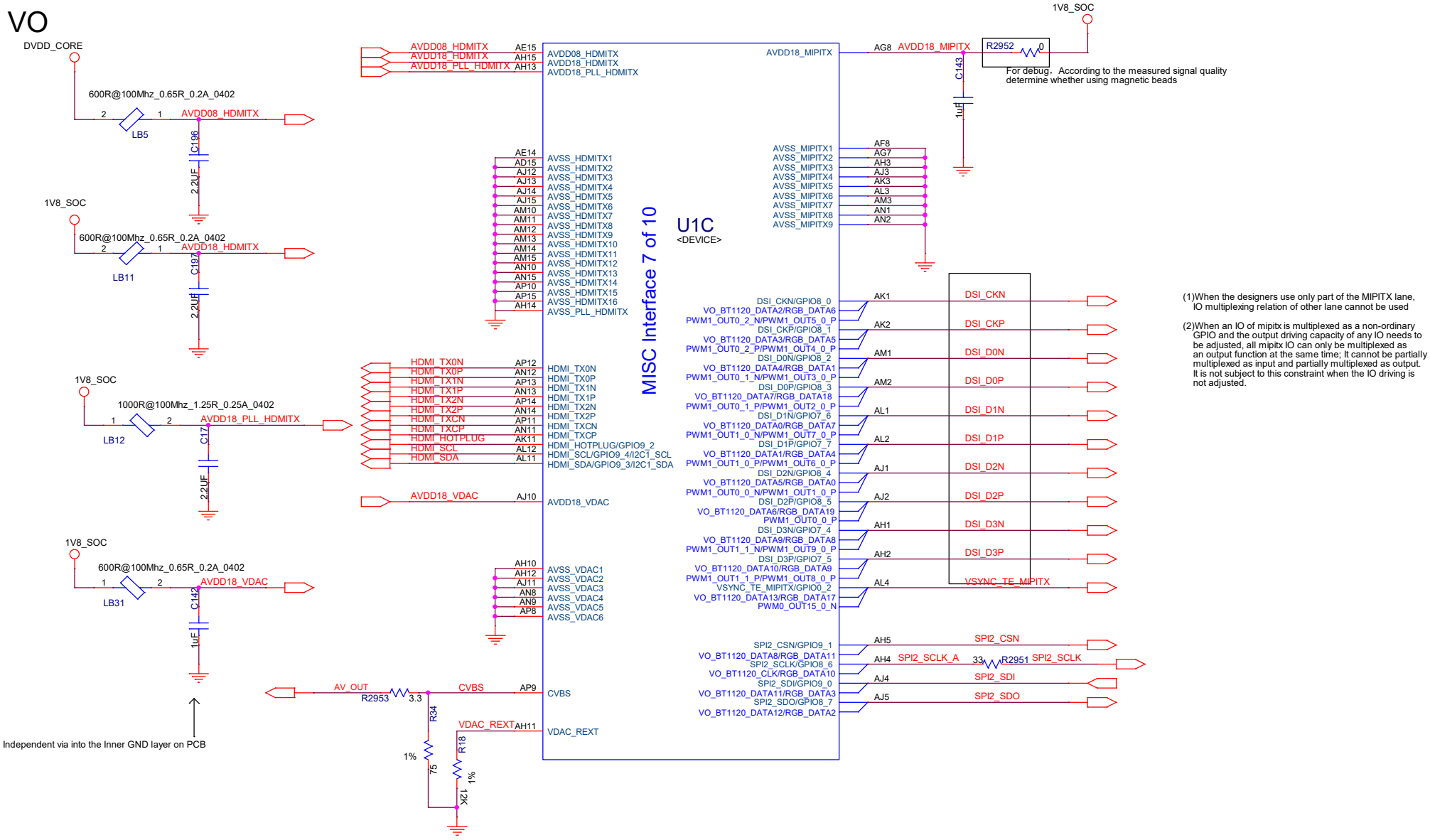
notes:(very important!)
For more detail information of VI scenario please refer to
the document 'SS928V100 Hardware Design User Guide'



The type and specification of the components refer to the BOM

				NA	
				ECA NO	DATE
DESIGNED					
REVIEWED		SS928V100DMEB			
		VER	PART_NUMBER	SHEET 18 of 22	
		A			

VO



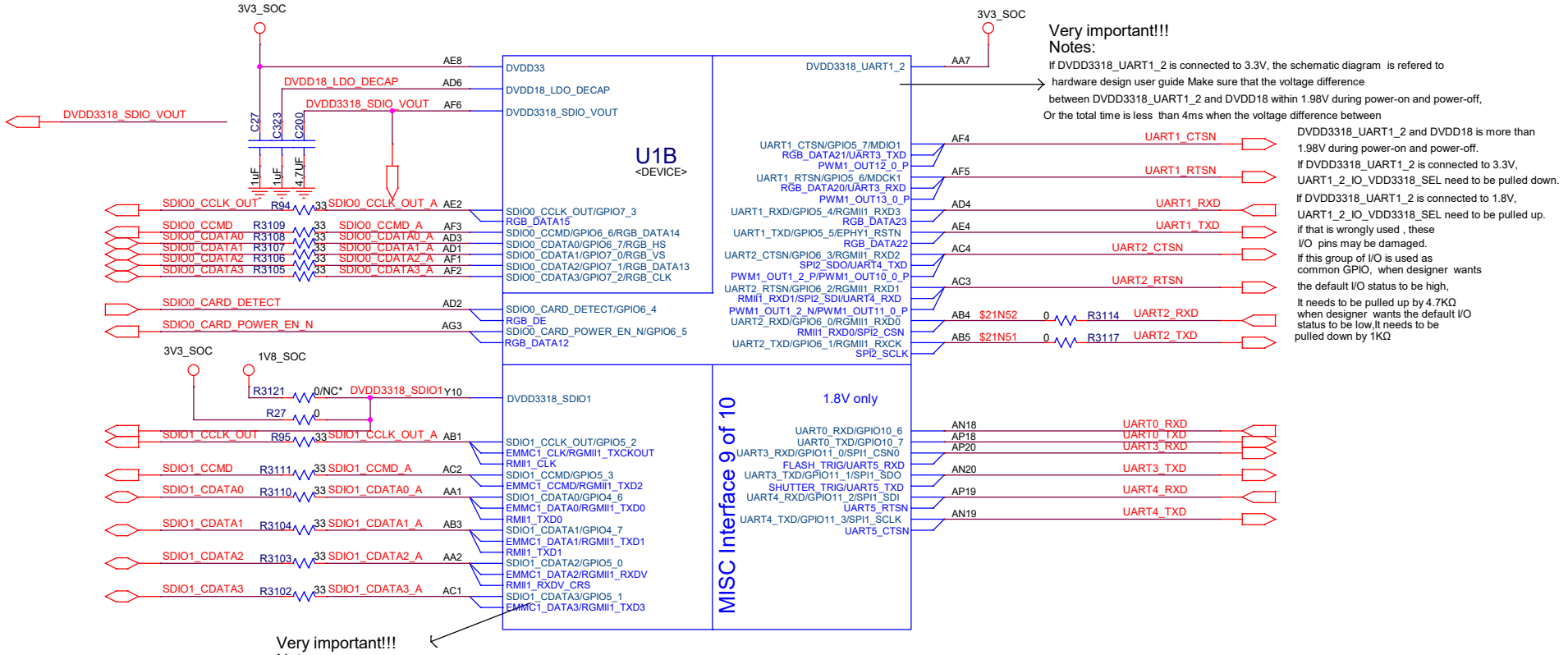
(1)When the designers use only part of the MIPITX lane, IO multiplexing relation of other lane cannot be used

(2)When an IO of mipitx is multiplexed as a non-ordinary GPIO and the output driving capacity of any IO needs to be adjusted, all mipitx IO can only be multiplexed as an output function at the same time; It cannot be partially multiplexed as input and partially multiplexed as output. It is not subject to this constraint when the IO driving is not adjusted.

The type and specification of the components refer to the BOM

				NA	
				ECA NO	DATE
DESIGNED					
REVIEWED		SS928V100DMEB			
		VER	PART_NUMBER	SHEET 19 of 22	
		A			

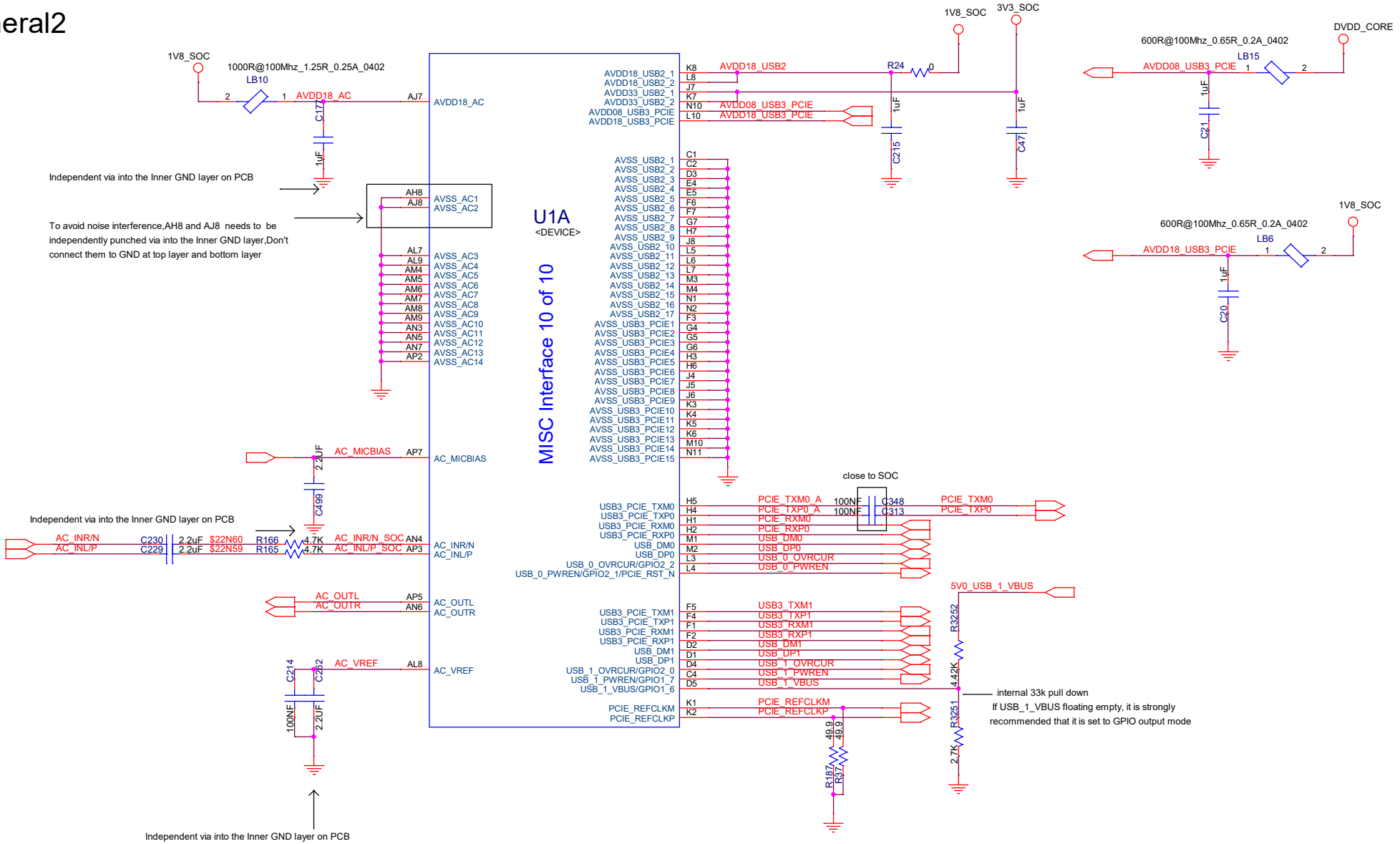
Peripheral1



The type and specification of the components refer to the BOM

				NA	
				ECA NO	DATE
DESIGNED		SS928V100DMEB			
REVIEWED					
		VER	PART_NUMBER	SHEET 20 of 22	
		A			

Peripheral2

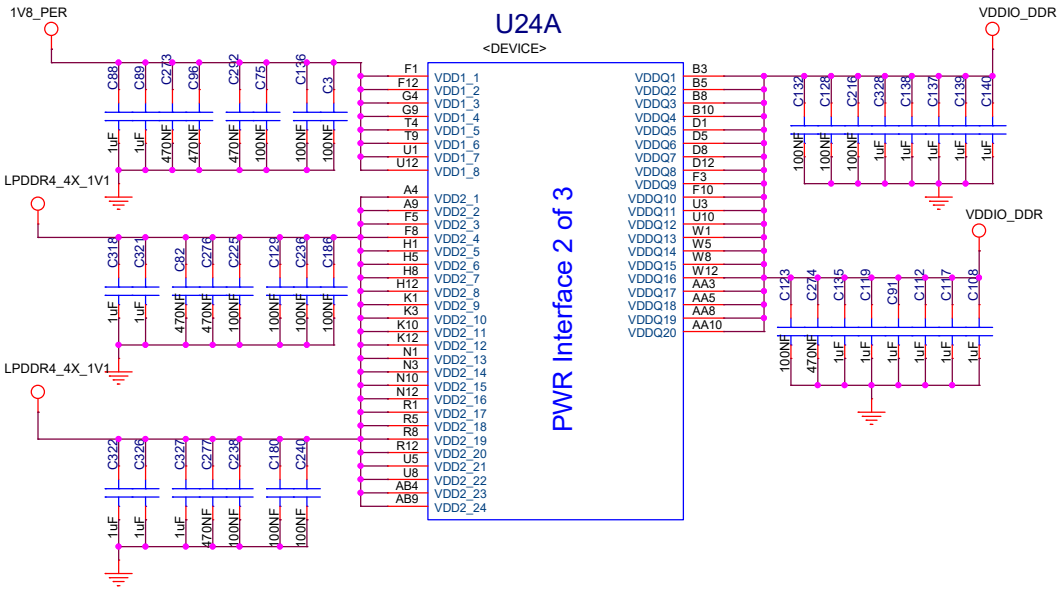


The type and specification of the components refer to the BOM

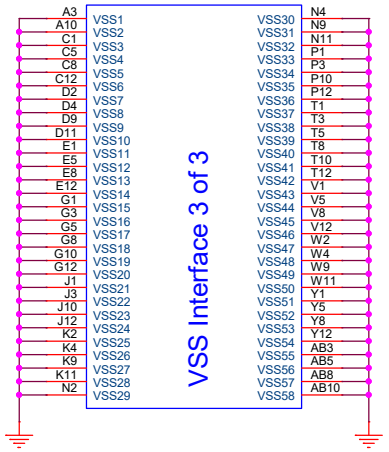
				NA	
				ECA NO	DATE
DESIGNED					
REVIEWED		SS928V100DMEB			
		VER	PART_NUMBER	SHEET 21 of 22	
		A			

LPDDR4X

Power



GND



IO

U24B

The type and specification of the components refer to the BOM

				NA	
				ECA NO	DATE
DESIGNED					
REVIEWED		SS928V100DMEB			
		VER	PART_NUMBER	SHEET 14 of 22	
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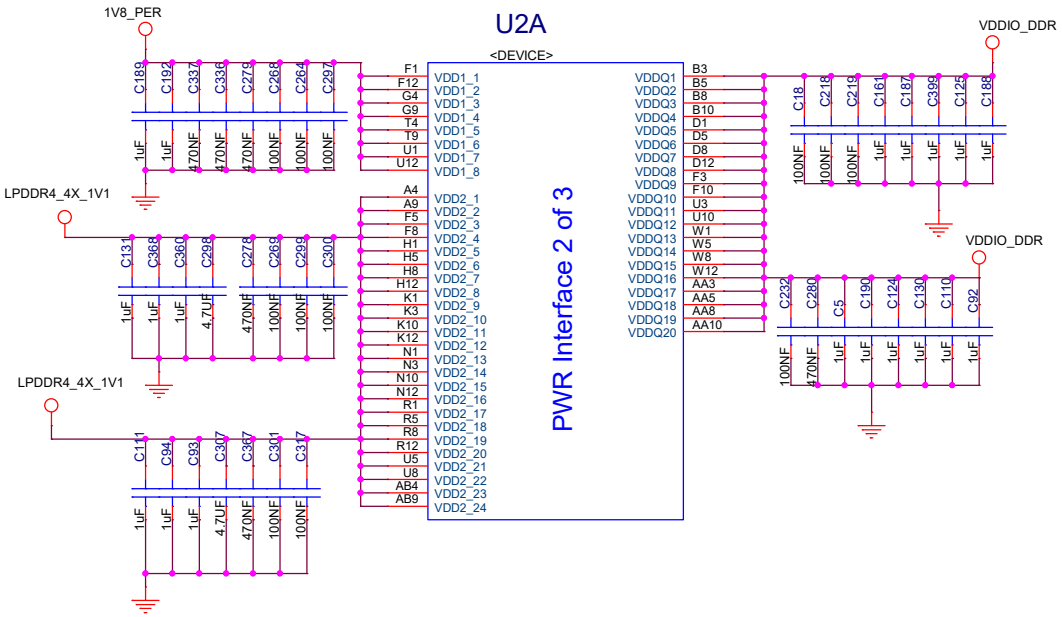
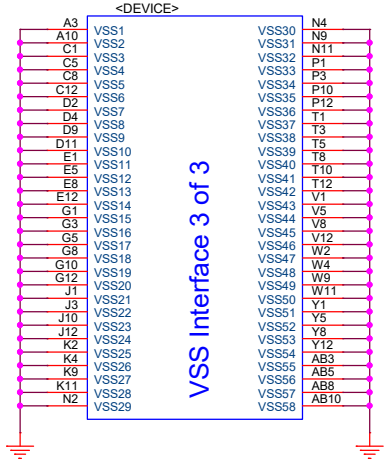
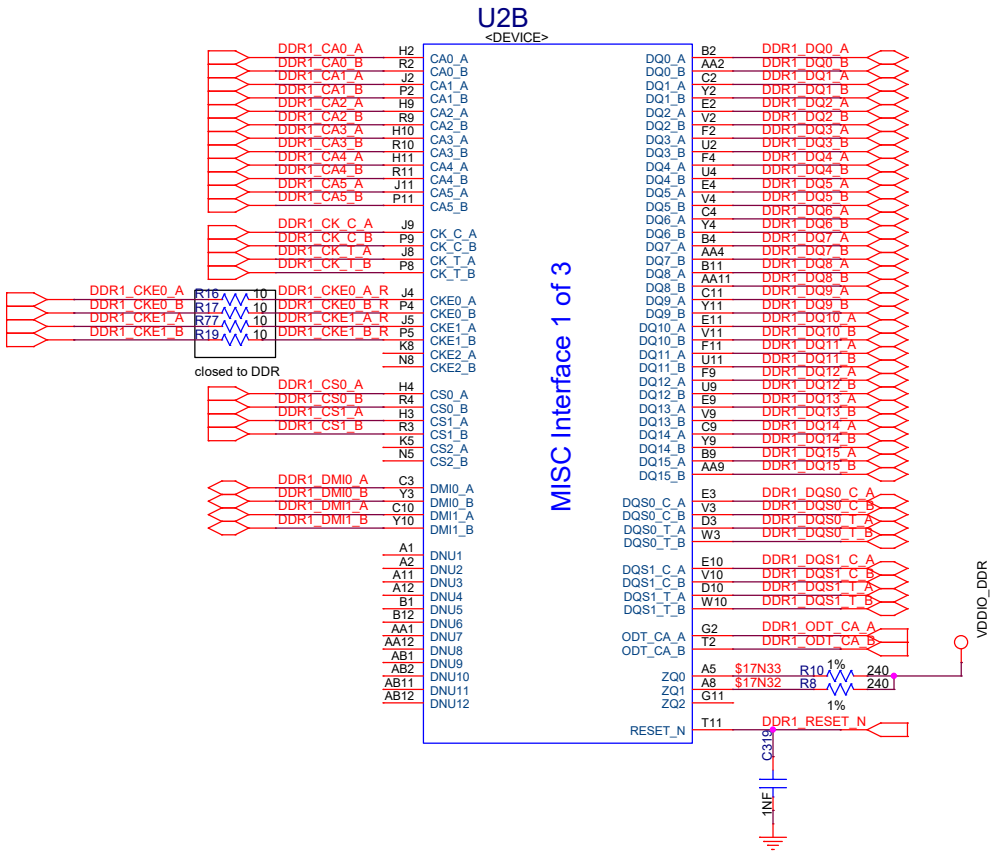
LPDDR4X Power



GND



IO



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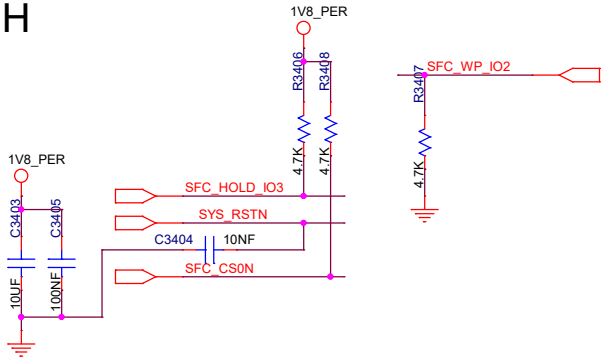
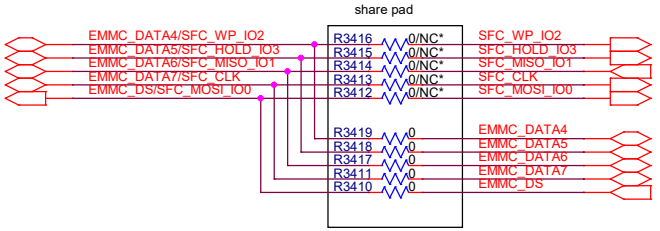
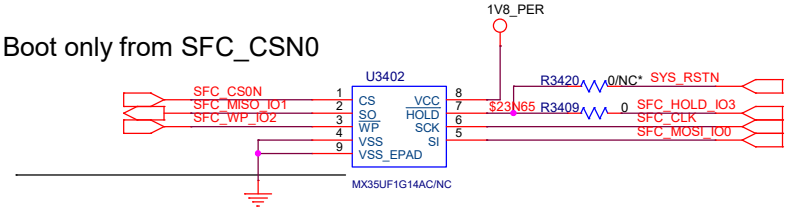
SPI FLASH

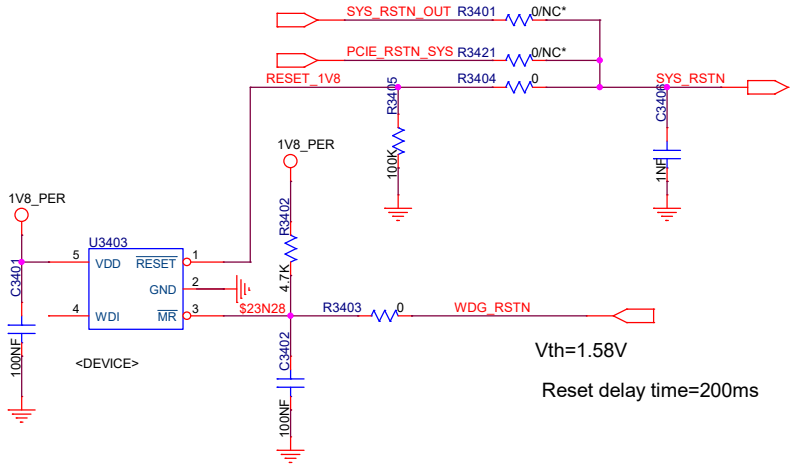




Boot only from SFC_CSN0



Reset



Vth=1.58V

Reset delay time=200ms

The type and specification of the components refer to the BOM

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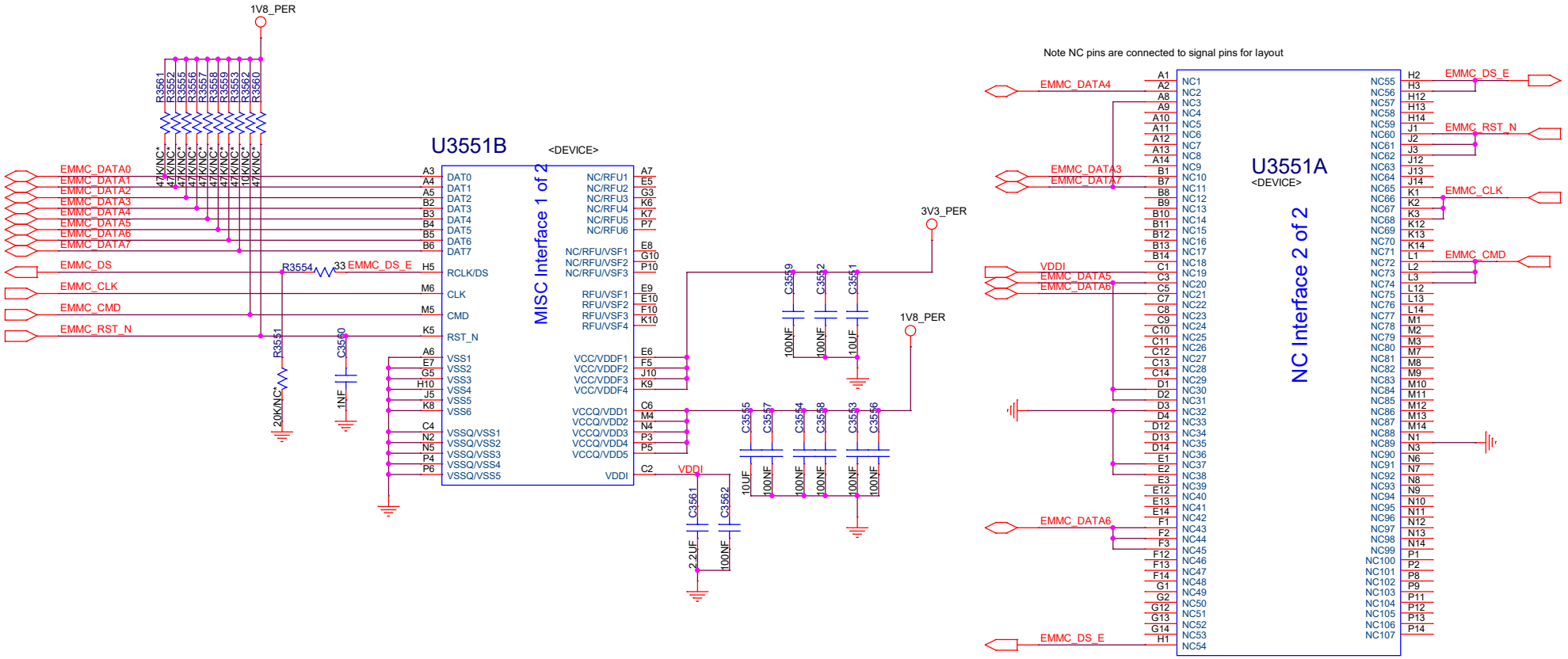
EMMC



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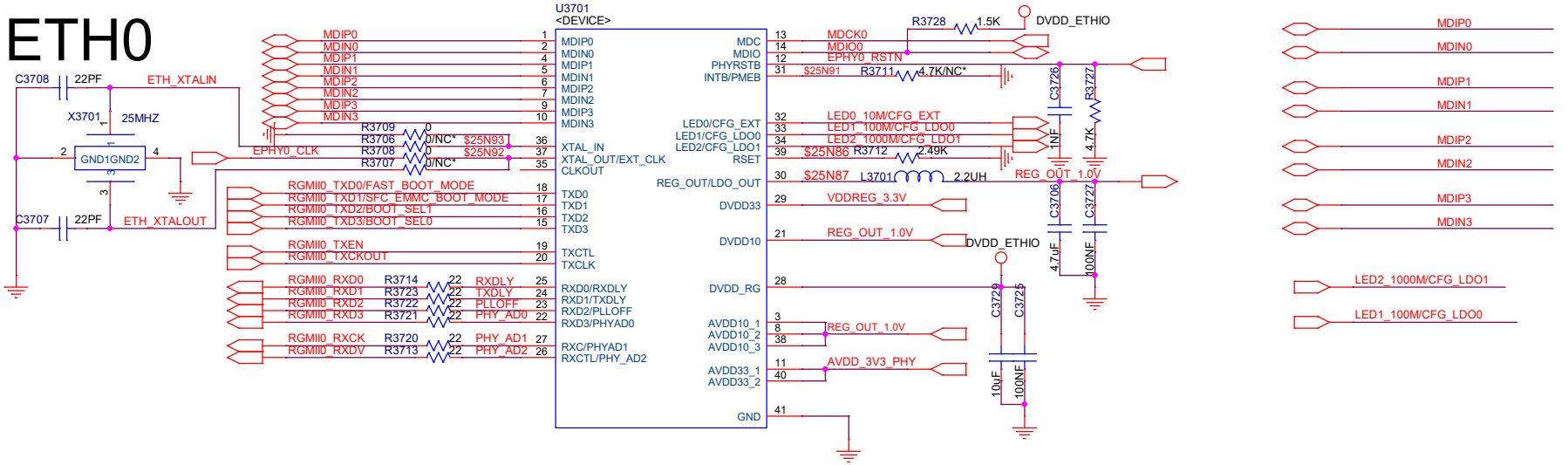
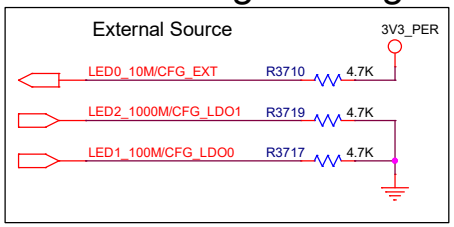
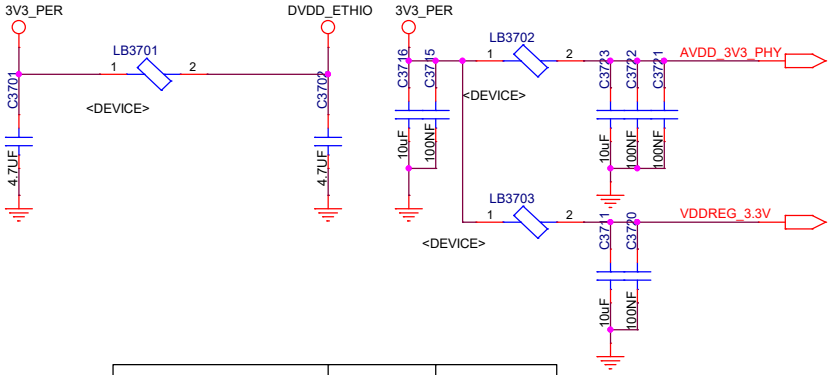
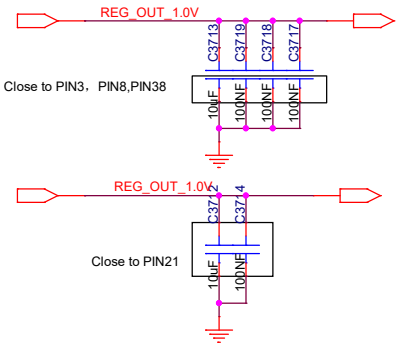
ETH0



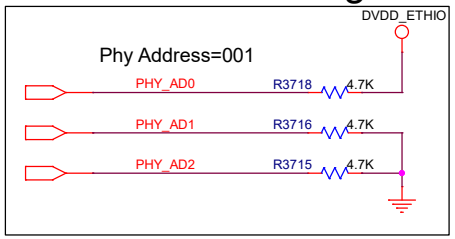
RGMII0 Voltage Config.







PHY Address Config.



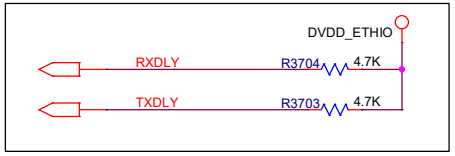
RGMII0 Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V(default)	1'b1	2'b00
External 1.8V	1'b1	2'b10
Internal 1.8V	1'b0	2'b10

PHY Address	PHYAD[2:0]
1	3'b001 (default)

LED2_1000M/CFG_LDO1

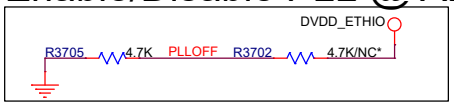
LED1_100M/CFG_LDO0

RGMII0 TXC/RXC Delay Config.



RXDLY=1 Add 2ns delay to RXC for RXD latching
TXDLY=1 Add 2ns delay to TXC for TXD latching
Pull-up disable PLL@ALDPS mode

Enable/Disable PLL @ ALDPS



The type and specification of the components refer to the BOM

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DESIGNED					
REVIEWED		SS928V100DMEB			
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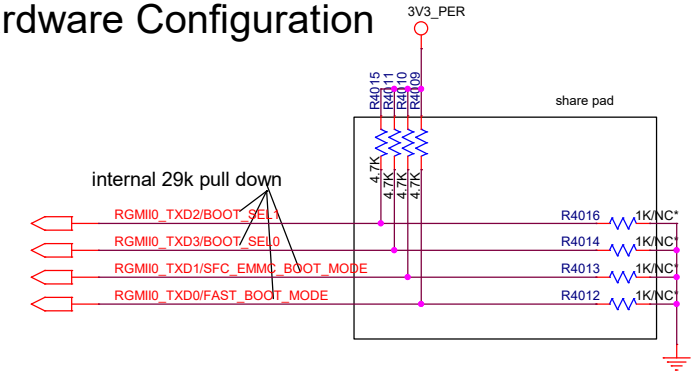
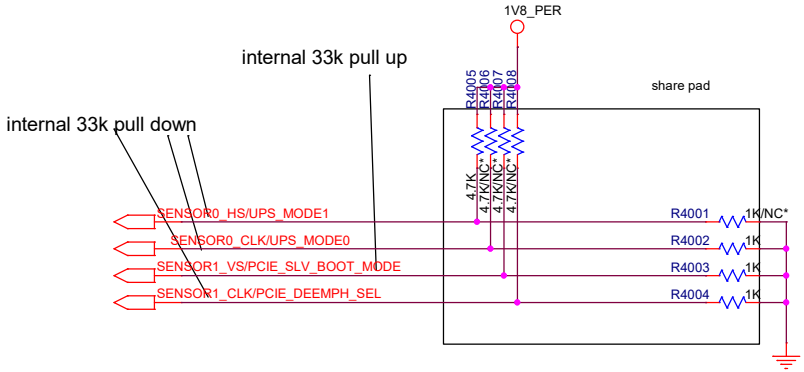
Hardware Configuration





BOOT_SEL[1:0]	SFC_EMMC_BOOT_MODE	MODE
00	0	SPI Nor Flash 3Byte
00	1	SPI Nor Flash 4Byte
01	0	SPI Nand Flash 1 wire
01	1	SPI Nand Flash 4 wire
10	X	Parallel NAND
11	0	EMMC 4bit
11	1	EMMC 8bit

FAST_BOOT_MODE	MODE
0	Normal BOOT
1	Fast BOOT

UPS_MODE[1:0]	PCIe/U3 MODE
00	PCIe X2
01	doule USB3
10	PCIe lane0+USB3 port1

PCIE_SLV_BOOT_MODE:	Function
0	Disable boot from PCIe
1	Boot from PCIe

PCIE_DEEMPH_SEL	PCIe PHY deemphasis
0	-3.5dB
1	-6dB

The type and specification of the components refer to the BOM

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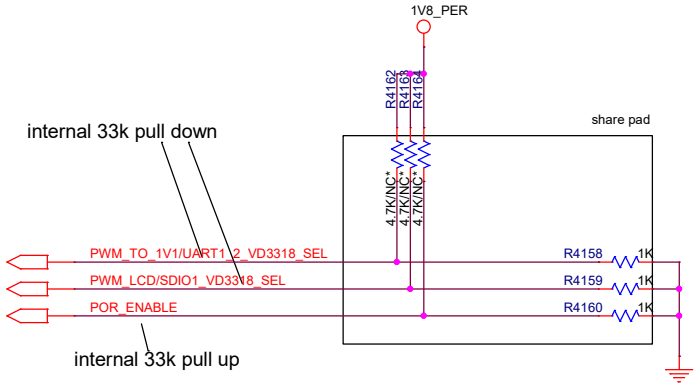
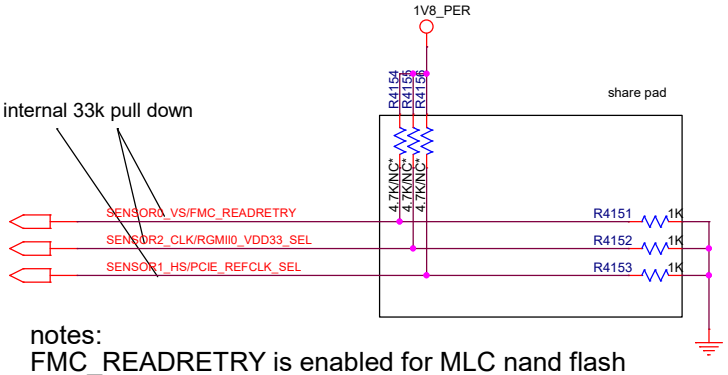
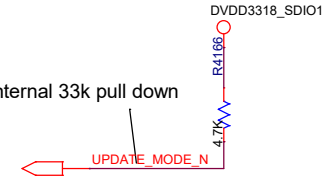
Hardware Configuration







notes:
FMC_READRETRY is enabled for MLC nand flash that support readretry.If nand flash do not support readretry,FMC_READRETRY is disabled

UART1_2_VD3318_SEL	UART1_2 IO VOLTAGE
0	3.3V
1	1.8V

SDIO1_VD3318_SEL	SDIO1 IO VOLTAGE
0	3.3V
1	1.8V

POR_ENABLE	Function
0	disable
1	enable

FMC_READRETRY	Function
0	disable
1	enable

RGMII0_VDD33_SEL	Function
0	3.3V

PCIE0_REFCLK_SEL:	Function
0	internal clock.
1	external clock.

UPDATE_MODE_N	Function
0	UPDATE MODE.
1	NORMAL MODE.

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