EVB Schematic For RK3399Pro

RK_EVB_RK3399Pro_LP3S178P332SD8_V1.4_20191108

PMIC: RK809-3 (5BUCK + 9LDO + Codec)
CPU RAM: LPDDR3
NPU RAM: LPDDR3
ROM: eMMC + TF card
Interface: MIPI CSI/MIPI DSI/UART/I2S/RMII/LCDC/PCIE/USB2/TYPEC/HDMI

Rockchip Fuzhou Rockchip Electronics 瑞芯微电子

Project:	RK3399Pro_EVB		
File:	00.Cover Page		
Date:	Wednesday, November 20, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	1 of 40

Index

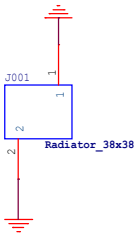
Note

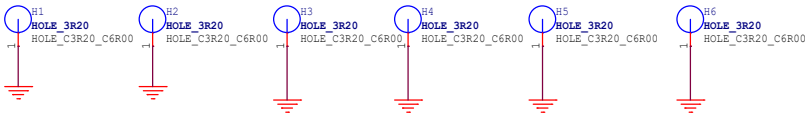
NOTE 1:
Component parameter description

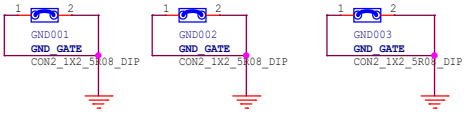
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted
3. If Flash is compatible, please notice when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted

NOTE 2:
Please use our recommended components to avoid too many changes.For more informations about the second source,please refer to our AVL.

Note
Option
Description
Remind



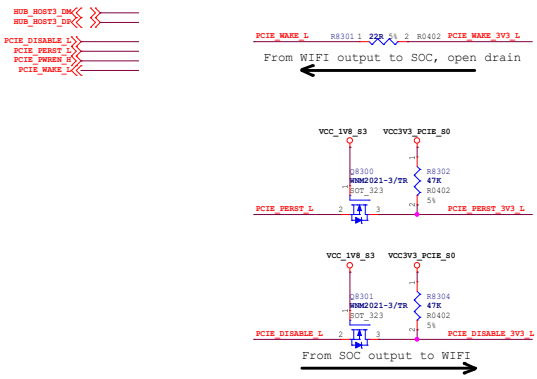




Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	01.Index		
Date:	Friday, November 08, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	2 of 40

Level Shift

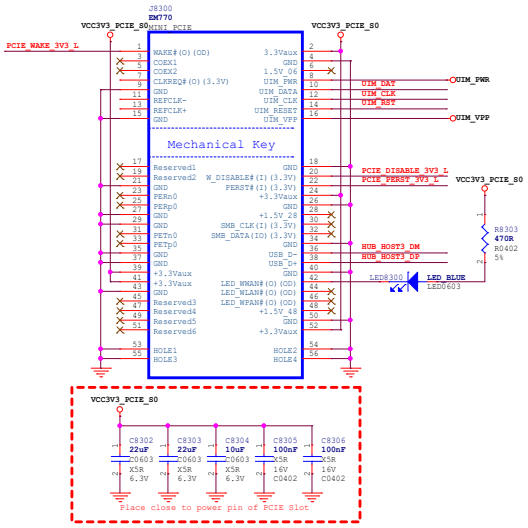
模块原理图设计说明（正式参考图请删除）：
PCIe端IO电平是3.3V，CPU端如果是1.8V就需要电平转换，如果是3.3V就不需要了。



PCIe Slot-Mini PCIe Card

Note:如果有与其他模块复用PCIE信号，需要增加PCIE Switch。

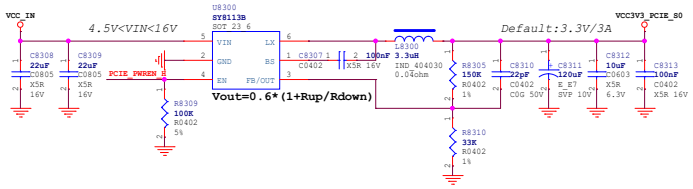
模块原理图设计说明（正式参考图请删除）：
设计是基于标准Mini PCIE接口设计，实际应用中，如使用支持SPK/MIC/UART等功能的3G/4G模组，请根据各模组规格进行调整。
管脚名中的TX/RX、I/O方向，是基于add-in Card金手指信号的方向，与SOC信号的方向正好相反，请注意。



POWER

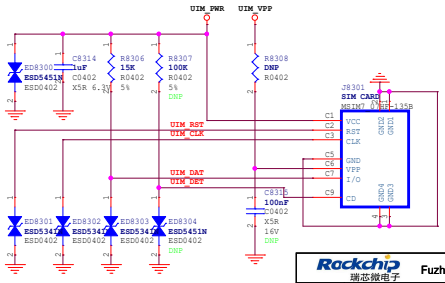
Note:Mini PCIE Card峰值工作电流较大，Spec最大约2.75A@3.3V，需要Buck单独供电，并预留大电容。

模块原理图设计说明（正式参考图请删除）：
如果系统电源中已有3.3V电源，可以删除该Buck电路，改成MOSFET电源开关电路以降低成本：



USIM Card

模块原理图设计说明（正式参考图请删除）：
标准Mini PCIE接口中是没有UIM_DET插入检测功能的，没有使用到检测可以删除下图中DNP器件。
如有使用到检测请根据模组规格进行调整，部分模组是使用Pin44 LED_WLAN#来检测的。



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics			
Project:	RK3399Pro_EVB			
File:	83.PCIe-PCIe2.0_Mini			
Date:	Tuesday, November 19, 2019	Rev:	V1.2	
Designed by: Linus.Lin	Reviewed by: <Checker>	Sheet:	3 of 4	

Revision History

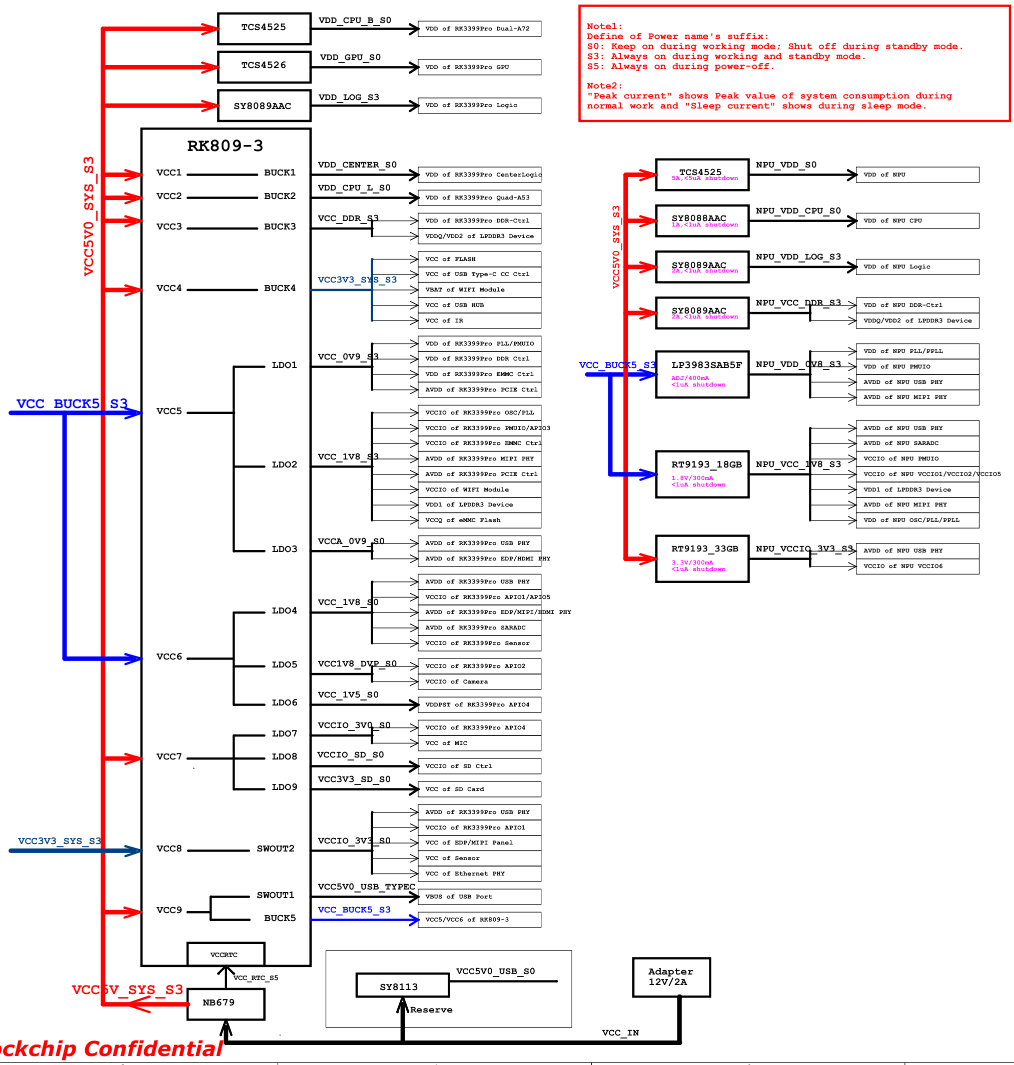
Version	Date	Author	Change Note	Approved
V1.0	2018.09.04	Felix	First edition for RK3399Pro	Wayne
V1.1	2018.11.12	Felix	Second edition for RK3399Pro	Wayne
V1.2	2019.02.15	Felix	1.C7001滤波电容移到电源前端R7011处。 2.R2114改成120K 1%;R2112改成68K 1%。 3.R2027改成300K。 4.LOG电源BUCK出来串一个R2251=0.02R电阻。 5.C6106,C6107电容改成18P。	Wayne
V1.3	2019.05.21	Linus	1.修改RK3399Pro封装，引出NPU_CIF以及NPU_MIPI信号； 2.修改NPU的连接方式，由U20 OTG+U30改为U20 HOST+PCIE。 3.连接NPU MIPI DSI与CPU MIPI CSI； 4.预留NPU_CIF接口，用于连接bt656数据； 5.预留NPU MIPI CSI接口，用于连接N4板子；	Wayne
V1.4	2019.11.08	Linus	1.修改J4600的信号，I2C由I2C4_SCL/SDA_TP改为I2C1_SCL/SDA_1V8； 2.删除Page 98-99的Power Test功能； 3.根据参考设计的修改，调整VCC_0V9_S3到LDO1，调整VCC_0V9_S0到LDO3。 4.增加USB2.0 HUB电路，扩展USB用于Mini PCIe。 5.增加Mini PCIe接口，修改USB PHY电源为S3电源支持USB唤醒。 6.更新RK809-3 Power-on Sequence表格。 7.删除VCC_DDRC电源及控制电路，电源与VCC_DDR电源合并。 8.VCC_RTC_S5增加测试电阻R2004。 9.根据WIFI晶体的CI，修改C6106/C6107成8pF。 10.NPU_USB20_AVDD_0V8/NPU_USB20_AVDD_1V8/NPU_MIPI_AVDD_0V8 和NPU_MIPI_AVDD_1V8增加1ohm电阻防浪涌； 11.R2000改成R1206封装； 12.C2150调整到R2160的pin2端。 13.C2260/C2261改为100nF；R2272改为27K；R2270改为118K； TPD4E05U06改为ESD5304D；C3127改为100pF; 14.增加电容C2278提高DCDC响应。 15.更新FUSB302B封装；更新RK809-3封装； 16.R3108/R3109/C3127贴片；R1122/R2602/R2607 DNP 17.修改NPU_VDD_LOG_S0为NPU_VDD_LOG_S3; 18.NPU_PWREN电源使能脚合并，修改R2230为20K，修改R2218/R2233为39K； 修改R2227为82K；增加电容C2279/C2280/C2281/C2282； 19.修改FB2100/FB2101为1.5A规格；修改FB1400为1R/0402； 20.C2213/C2219/C2229/C2271修改为22pF； 21.修改VDD_LOG_S0为VDD_LOG_S3；	Wayne

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RK3399Pro_EVB				
File:	02.Revision History				
Date:	Wednesday, November 20, 2019			Rev:	V1.3
Designed by:	Linus.Lin	Reviewed by:	<Checker>	Sheet:	3 of 50

Power Diagram and Sequence

Note1:
Define of Power name's suffix:
S0: Keep on during working mode; Shut off during standby mode.
S3: Always on during working and standby mode.
S5: Always on during power-off.

Note2:
"Peak current" shows Peak value of system consumption during normal work and "Sleep current" shows during sleep mode.



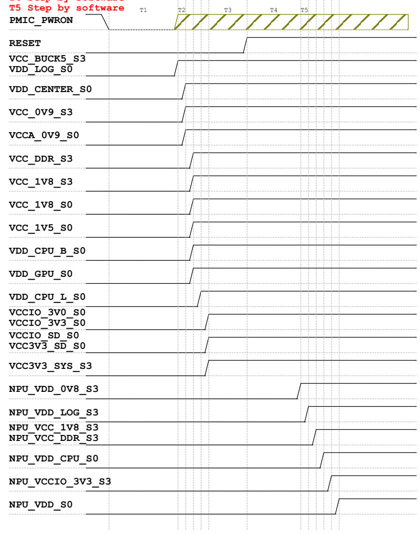
TCS4525
VDD_CPU_B_S0
VDD of RK3399Pro Dual-A72
TCS4526
VDD_GPU_S0
VDD of RK3399Pro GPU
SY8089AAC
VDD_LOG_S3
VDD of RK3399Pro Logic
RK809-3
VCC1
BUCK1
VCC2
BUCK2
VCC3
BUCK3
VCC4
BUCK4
VCC5
LDO1
LDO2
LDO3
VCC6
LDO4
LDO5
LDO6
VCC7
LDO7
LDO8
LDO9
VCC8
SWOUT2
VCC9
SWOUT1
BUCK5
VCCRTC
VCC5V0_SYS_S3
VCC_BUCK5_S3
VCC3V3_SYS_S3
VDD_CENTER_S0
VDD of RK3399Pro CenterLogic
VDD_CPU_L_S0
VDD of RK3399Pro Quad-A53
VCC_DDR_S3
VDD of RK3399Pro DDR-Ctrl
VDDQ/VDD2 of LPDDR3 Device
VCC of FLASH
VCC of USB Type-C CC Ctrl
VBAT of WIFI Module
VCC of USB HUB
VCC of IR
VCC_0V9_S3
VDD of RK3399Pro PLL/PMUIO
VDD of RK3399Pro DDR Ctrl
VDD of RK3399Pro EMMC Ctrl
AVDD of RK3399Pro PCIE Ctrl
VCC_1V8_S3
VCCIO of RK3399Pro OSC/PLL
VCCIO of RK3399Pro PMUIO/APIO3
VCCIO of RK3399Pro EMMC Ctrl
AVDD of RK3399Pro MIPI PHY
AVDD of RK3399Pro PCIE Ctrl
VCCIO of WIFI Module
VDD1 of LPDDR3 Device
VCCQ of eMMC Flash
VCCA_0V9_S0
AVDD of RK3399Pro USB PHY
AVDD of RK3399Pro EDP/HDMI PHY
VCC_1V8_S0
AVDD of RK3399Pro USB PHY
VCCIO of RK3399Pro APIO1/APIO5
AVDD of RK3399Pro EDP/MIPI/HDMI PHY
AVDD of RK3399Pro SARADC
VCCIO of RK3399Pro Sensor
VCC1V8_DVP_S0
VCCIO of RK3399Pro APIO2
VCCIO of Camera
VCC_1V5_S0
VDDPST of RK3399Pro APIO4
VCCIO_3V0_S0
VCCIO of RK3399Pro APIO4
VCC of MIC
VCCIO_SD_S0
VCCIO of SD Ctrl
VCC3V3_SD_S0
VCC of SD Card
VCCIO_3V3_S0
AVDD of RK3399Pro USB PHY
VCCIO of RK3399Pro APIO1
VCC of EDP/MIPI Panel
VCC of Sensor
VCC of Ethernet PHY
VCC5V0_USB_TYPEC
VBUS of USB Port
VCC5/VCC6 of RK809-3
VCC_RTC_S5
NB679
SY8113
VCC5V0_USB_S0
Reserve
Adapter
12V/2A
VCC_IN
TCS4525
5A,<5uA shutdown
NPU_VDD_S0
VDD of NPU
SY8088AAC
1A,<1uA shutdown
NPU_VDD_CPU_S0
VDD of NPU CPU
SY8089AAC
2A,<1uA shutdown
NPU_VDD_LOG_S3
VDD of NPU Logic
SY8089AAC
2A,<1uA shutdown
NPU_VCC_DDR_S3
VDD of NPU DDR-Ctrl
VDDQ/VDD2 of LPDDR3 Device
LP3983SAB5F
ADJ/400mA
<1uA shutdown
NPU_VDD_0V8_S3
VDD of NPU PLL/PPLL
VDD of NPU PMUIO
AVDD of NPU USB PHY
AVDD of NPU MIPI PHY
RT9193_18GB
1.8V/300mA
<1uA shutdown
NPU_VCC_1V8_S3
AVDD of NPU USB PHY
AVDD of NPU SARADC
VCCIO of NPU PMUIO
VCCIO of NPU VCCIO1/VCCIO2/VCCIO5
VDD1 of LPDDR3 Device
AVDD of NPU MIPI PHY
VDD of NPU OSC/PLL/PPLL
RT9193_33GB
3.3V/300mA
<1uA shutdown
NPU_VCCIO_3V3_S3
AVDD of NPU USB PHY
VCCIO of NPU VCCIO6

Rockchip Confidential

RK3399Pro Power-on Sequence

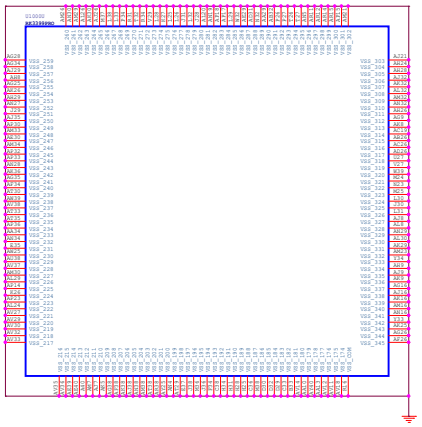
Power Name	PMIC Channel	Time Slot (step 2ms)	Default voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_BUCK5_S3	RK809-3 BUCK5	Slot: 1	3.3V/Adj	2.5A	ON	ON	0.56A	
VDD_LOG_S3	Ext(SY8089)	Slot: 1A	0.9V	2.0A	ON	ON	1.27A	
VDD_CENTER_S0	RK809-3 BUCK1	Slot: 2	0.9V	2.5A	ON	OFF		
VCC_0V9_S3	RK809-3 LDO1	Slot: 2	0.9V	0.4A	ON	ON	0.29A	
VCCA_0V9_S0	RK809-3 LDO3	Slot: 2	0.9V	0.1A	ON	OFF		
VCC_DDR_S3	RK809-3 BUCK3	Slot: 3	1.25V	1.5A	ON	ON	0.85A	
VCC_1V8_s3	RK809-3 LDO2	Slot: 3	1.8V	0.4A	ON	ON	0.27A	
VCC_1V8_S0	RK809-3 LDO4	Slot: 3	1.8V	0.4A	ON	OFF		
VCC_1V5_S0	RK809-3 LDO6	Slot: 3	1.5V	0.4A	ON	OFF		
VDD_CPU_B_S0	Ext(TCS4525)	Slot: 3A	0.9V	6.0A	ON	OFF	3.10A	
VDD_GPU_S0	Ext(TCS4526)	Slot: 3B	0.9V	6.0A	ON	OFF	3.48A	
VDD_CPU_L_S0	RK809-3 BUCK2	Slot: 4	0.9V	2.5A	ON	OFF	0.93A	
VCCIO_3V0_S0	RK809-3 LDO7	Slot: 5	3.0V	0.4A	ON	OFF		
VCCIO_3V3_S0	RK809-3 SWOUT2	Slot: 5	3.3V	2.1A	ON	OFF		
VCC3V3_SYS_S3	RK809-3 BUCK4	Slot: 5	3.3V	1.5A	ON	ON	0.38A	
VCCIO_SD_S0	RK809-3 LDO8	Slot: 5	3.3V	0.4A	ON	OFF		
VCC3V0_SD_S0	RK809-3 LDO9	Slot: 5	3.3V	0.4A	ON	OFF		
VCC1V5_DVP_S0	RK809-3 LDO5	N/A	1.5V	0.4A	OFF	OFF		
VCC1V8_DVP_S0	Ext(rt9193)	N/A	1.8V	0.3A	OFF	OFF		
VCC2V8_DVP_S0	Ext(rt9193)	N/A	2.8V	0.3A	OFF	OFF		
VCC5V0_USB_TYPEC	RK809-3 SWOUT1	N/A	5.0V	2.1A	OFF	OFF		
RESET	RK809 sent out Reset signal for CPU(timing:10); Then CPU sent out NPU's power-on signal							
NPU_VDD_0V8_S3	Ext(lp3983)	Slot: 11	0.8V	0.4A	ON	ON	0.06A	
NPU_VDD_LOG_S3	Ext(sy8089aac)	Slot: 12	0.8V	2.0A	ON	ON	0.28A	
NPU_VCC_1V8_S3	Ext(rt9193)	Slot: 13	1.8V	0.3A	ON	ON	0.11A	
NPU_VCC_DDR_S3	Ext(sy8089aac)	Slot: 13	1.25V	2.0A	ON	ON	0.52A	
NPU_VDD_CPU_S0	Ext(sy8088aac)	Slot: 14	0.85V	1.0A	ON	OFF	0.19A	
NPU_VCCIO_3V3_S3	Ext(rt9193)	Slot: 15	3.3V	0.3A	ON	ON	TBD	
NPU_VDD_S0	Ext(tcs4525)	Slot: 16	0.85V	6.0A	ON	OFF	2.06A	
NPU_REF_CLK	CPU sent out 24M clk for npu.							
NPU_RESET	CPU send out Reset signal for NPU by software.							

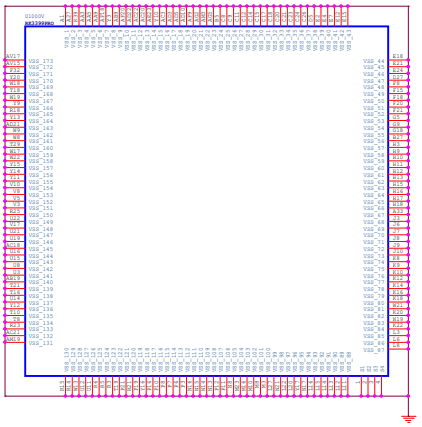
Note:
T1=100ms.
T2 Step=2ms
T3=10ms
T4 Step by software
T5 Step by software

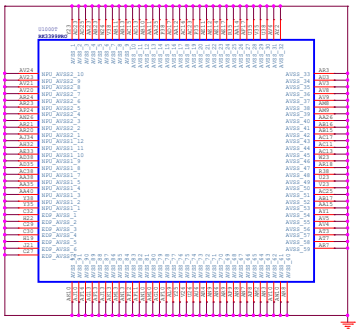


T1
T2
T3
T4
T5
PMIC_PWRON
RESET
VCC_BUCK5_S3
VDD_LOG_S0
VDD_CENTER_S0
VCC_0V9_S3
VCCA_0V9_S0
VCC_DDR_S3
VCC_1V8_S3
VCC_1V8_S0
VCC_1V5_S0
VDD_CPU_B_S0
VDD_GPU_S0
VDD_CPU_L_S0
VCCIO_3V0_S0
VCCIO_3V3_S0
VCCIO_SD_S0
VCC3V3_SD_S0
VCC3V3_SYS_S3
NPU_VDD_0V8_S3
NPU_VDD_LOG_S3
NPU_VCC_1V8_S3
NPU_VCC_DDR_S3
NPU_VDD_CPU_S0
NPU_VCCIO_3V3_S3
NPU_VDD_S0

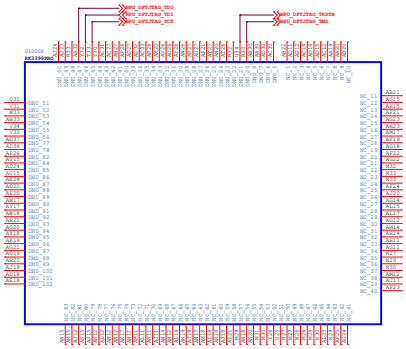
POWER GROUND







NC & DNU



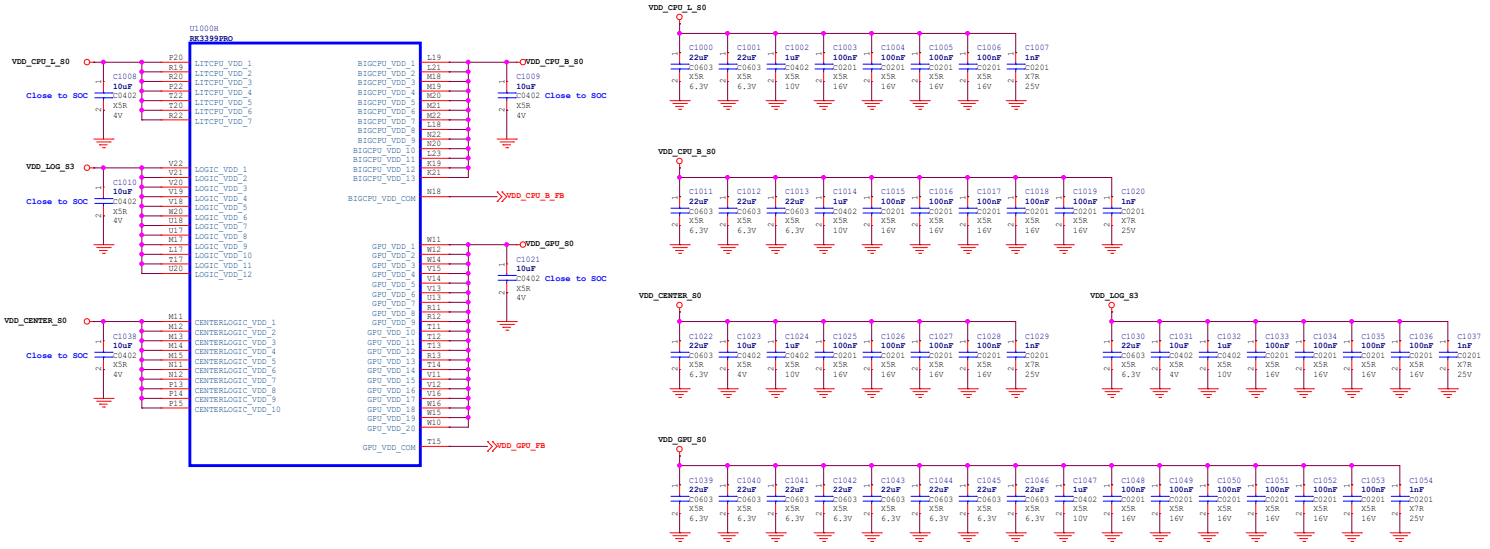
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	RK3399Pro_EVB
File:	08.RK3399Pro GND
Date:	Friday, November 08, 2019
Designed by:	Linus Lin
Rev:	V1.3
Sheet:	6 of 40

I2C MAP

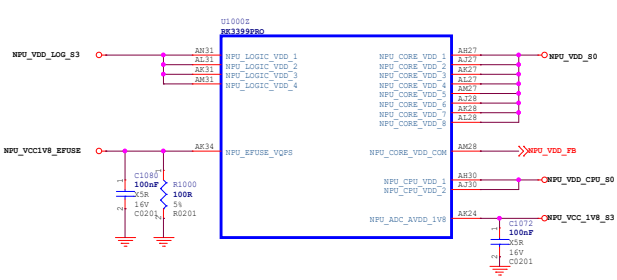
Port	Pin Name	Domain	Bus Name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Slave Bus Capability	Note
I2C0	I2C0_SCL/GPIO1_C0_u I2C0_SDA/GPIO1_B7_u	PMUIO2	I2C0_SCL_PMIC I2C0_SDA_PMIC	VCC_1V8_S3	RK809-3	0x20	100kHz,400kHz	Rockchip PMIC
					TCS4525	0x1c	100kHz,400kHz,3.4MHz	Torch-chip BUCK
					TCS4526	0x10	100kHz,400kHz,3.4MHz	Torch-chip BUCK
I2C1	I2C1_SCL/GPIO4_A2_u I2C1_SDA/GPIO4_A1_u	APIO5	I2C1_SCL_1V8 I2C1_SDA_1V8	VCC_1V8_S0	CAMERA	N/A	100kHz,400kHz	MIPI/CIF CAMERA
					MPU6500	0x68	100kHz,400kHz	InvenSense Gyroscope+Accelerometer
					AK8963C	0x0d	100kHz,400kHz	AsahiKASEI COMPASS
					N4	0x30	100kHz,400kHz	Nextchip 4-AHD
I2C2	I2C2_SCL/GPIO2_A1_u I2C2_SDA/GPIO2_A0_u	APIO2	NC					
I2C3	I2C3_SCL/GPIO4_C1_u I2C3_SDA/GPIO4_C0_u	APIO4	I2C3_SCL_HDMI I2C3_SDA_HDMI	VCCIO_3V0_S0	HDMI	N/A	100kHz,400kHz	HDMI
I2C4	I2C4_SCL/GPIO1_B4_u I2C4_SDA/GPIO1_B3_u	PMUIO2	I2C4_SCL_TP I2C4_SDA_TP	VCC_1V8_S3	Touch IC	N/A	100kHz,400kHz	Touch IC
I2C5	I2C5_SCL/GPIO3_B3_u I2C5_SDA/GPIO3_B2_u	APIO1	NC					
I2C6	I2C6_SCL/GPIO2_B2_u I2C6_SDA/GPIO2_B1_u	APIO2	NC					
I2C7	I2C7_SCL/GPIO2_B0_u I2C7_SDA/GPIO2_A7_u	APIO2	NC					
I2C8	I2C8_SCL/GPIO1_C5_u I2C8_SDA/GPIO1_C4_u	PMUIO2	I2C8_SCL_CC I2C8_SDA_CC	VCC_1V8_S3	ET7301B FUSB302B	0x40,0x46	100kHz,400kHz,1MHz	ETEK USB Type-C Mux Fairchild USB Type-C Mux
NPU I2C1	NPU_I2C1_SCL/GPIO0_C0_u NPU_I2C1_SDA/GPIO0_C1_u	NPU_VCC_1V8	NPU_I2C1_SCL NPU_I2C1_SDA	NPU_VCC_1V8_S3	TCS4525	0x1c	100kHz,400kHz,3.4MHz	Torch-chip DC-DC BUCK
NPU I2C3	NPU_I2C3_SCL/GPIO2_D0_u NPU_I2C3_SDA/GPIO2_D1_u	NPU_VCC_1V8_S3	NPU_I2C3_SCL NPU_I2C3_SDA	NPU_VCC_1V8_S3	CAMERA	N/A	100kHz,400kHz	CIF CAMERA

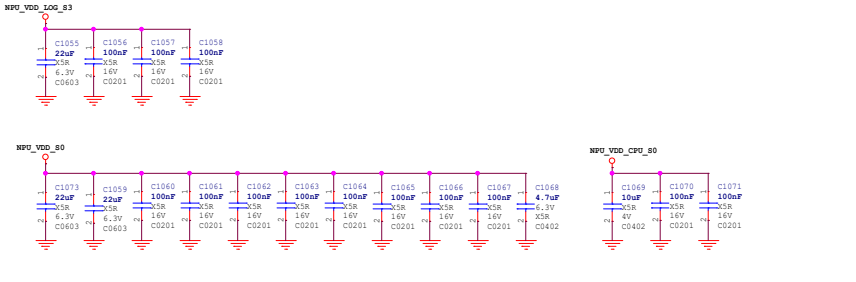
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RK3399Pro_EVB				
File:	05.I2C MAP				
Date:	Friday, November 08, 2019			Rev:	V1.3
Designed by:	Linus.Lin	Reviewed by:	<Checker>	Sheet:	6 of 50

Power



NPU Power

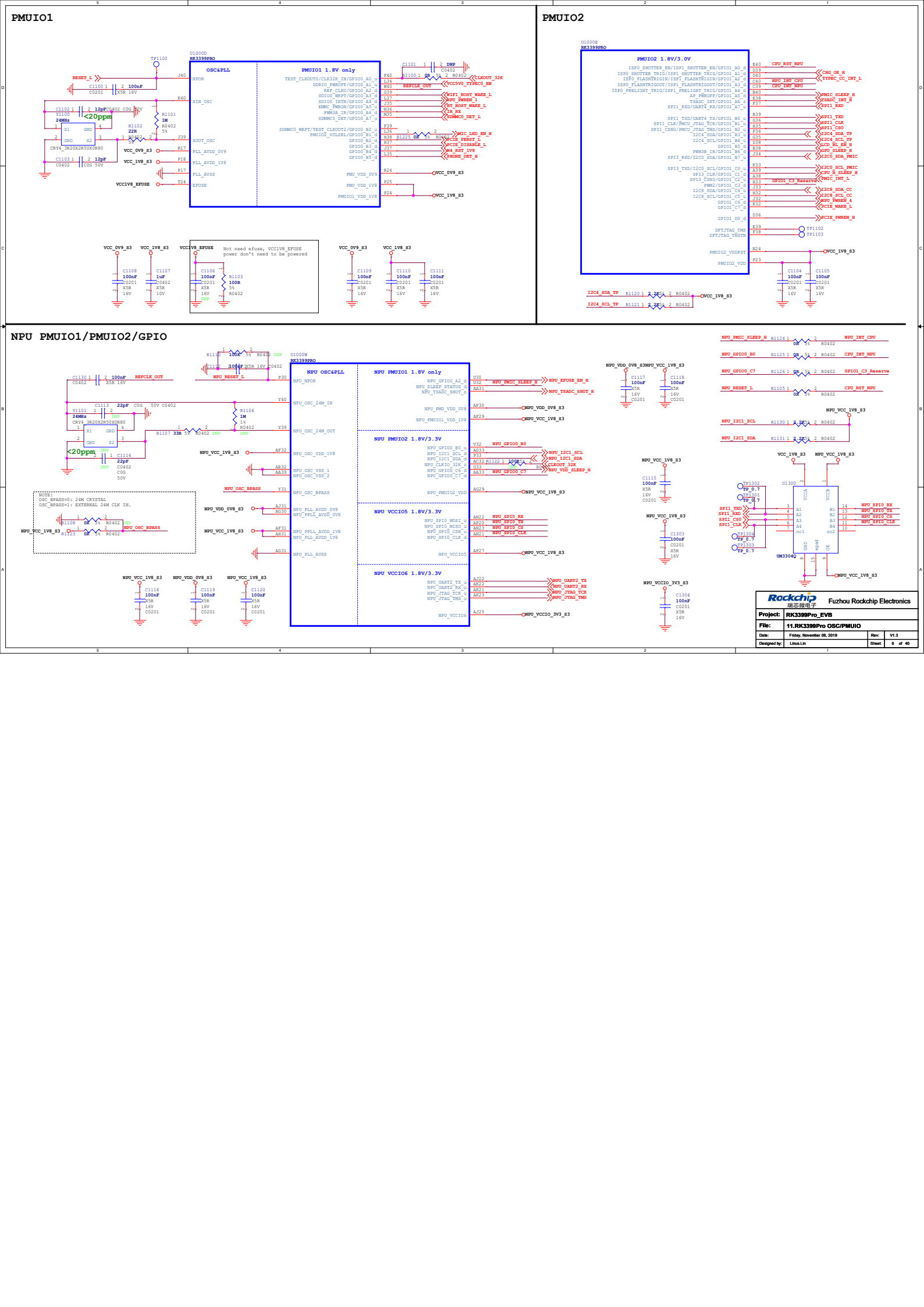




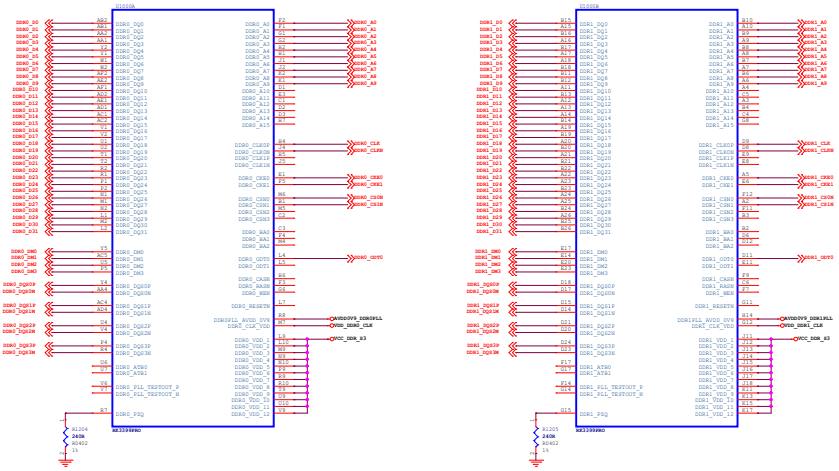
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	RK3399Pro_EVB
File:	10.RK3399Pro Power
Date:	Friday, November 08, 2019
Rev:	V1.3
Designed by:	Linus.Lin
Sheet	7 of 40

IO Power Domain Map

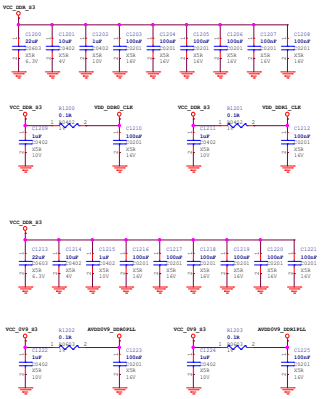
IO Domain	Pin No.	Support of IO Voltage			Default Actual assigned IO Domain Voltage			Notes
		1.8V	3.0V	3.3V	Net Name of Power Supply	Power Source	Voltage	
PMUIO1	***GPIO0***	✓	✗	✗	*VCC_1V8_S3*	*RK809_LDO2*	*1.8V*	
PMUIO2	***GPIO1***	✓	✓	✗	*VCC_1V8_S3*	*RK809_LDO2*	*1.8V*	*GPIO0_B1/PMUIO2_VOLSEL pin defined as a set pin for PMUIO2 part voltage domain after power-on reset.It is pull-down for 1.8V or pull-up for 3.0V*
APIO1	***GPIO3***	✗	✗	✓	*VCCIO_3V3_S0*	*RK809_SW2*	*3.3V*	
APIO2	***GPIO2ab***	✓	✓	✗	*VCC1V8_DVP_S0*	*RK809_LDO5*	*1.8V*	
APIO3	***GPIO2cd***	✓	✗	✗	*VCC_1V8_S3*	*RK809_LDO2*	*1.8V*	
APIO4	***GPIO4cd***	✓	✓	✗	*VCCIO_3V0_S0*	*RK809_LDO7*	*3.0V*	
APIO5	***GPIO4a***	✓	✓	✗	*VCC_1V8_S0*	*RK809_LDO4*	*1.8V*	
SDMMC0	***GPIO4b***	✓	✓	✗	*VCCIO_SD_S0*	*RK809_LDO8*	*1.8V/3.0V auto*	
NPU PMUIO1	***GPIO0a***	✓	✗	✗	*NPU_VCC_1V8_S3*	*Ext_LDO*	*1.8V*	
NPU PMUIO2	***GPIO0bc***	✓	✓	✓	*NPU_VCC_1V8_S3*	*Ext_LDO*	*1.8V*	
NPU VCCIO2	***GPIO2***	✓	✓	✓	*NPU_VCC_1V8_S3*	*Ext_LDO*	*1.8V*	
NPU VCCIO5	***GPIO1b***	✓	✓	✓	*NPU_VCC_1V8_S3*	*Ext_LDO*	*1.8V*	
NPU VCCIO6	***GPIO4a***	✓	✓	✓	*NPU_VCCIO_3V3_S3*	*Ext_LDO*	*3.3V*	


PMUIO1
PMUIO2
NPU PMUIO1/PMUIO2/GPIO
U1000D
RK3399PRO
OSC&PLL
PMUIO1 1.8V only
PMUIO2 1.8V/3.0V
U1000E
U1000W
NPU OSC&PLL
NPU PMUIO1 1.8V only
NPU PMUIO2 1.8V/3.3V
NPU VCCIO5 1.8V/3.3V
NPU VCCIO6 1.8V/3.3V
Not need efuse, VCC1V8_EFUSE power don't need to be powered
NOTE:
OSC_BPASS=0: 24M CRYSTAL
OSC_BPASS=1: EXTERNAL 24M CLK IN.
Rockchip
Fuzhou Rockchip Electronics
Project: RK3399Pro_EVB
File: 11.RK3399Pro OSC/PMUIO
Date: Friday, November 08, 2019
Rev: V1.3
Designed by: Linus.Lin
Sheet: 8 of 40

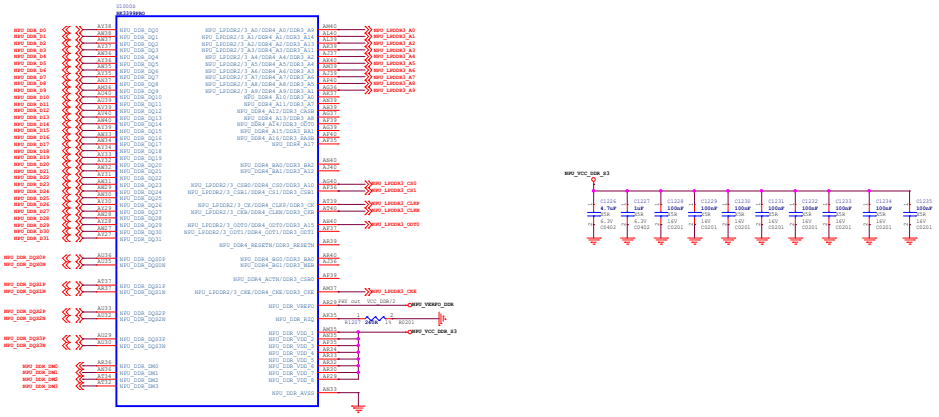
DDR Controller



DDR FILTER



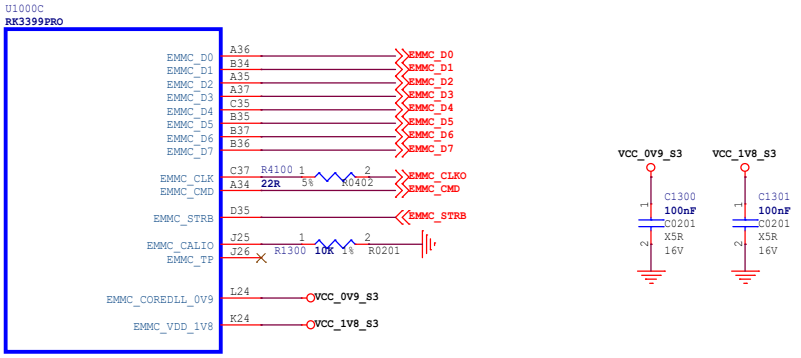
NPU DDR Controller



LPDDR3/LPDDR2	DDR3
A0	A9
A1	A14
A2	A13
A3	A11
A4	A2
A5	A4
A6	A3
A7	A6
A8	A5
A9	A1
	A0
	A7
	CASB
	A8
	ODT0
	BA1
	RASB
	CSB0
	BA2
	A12
	BA0
	WEB
CK	CK
CKB	CKB
CKE	CKE
CSB0	A10
CSB1	CSB1
ODT0	A15
ODT1	ODT1
	RESETN

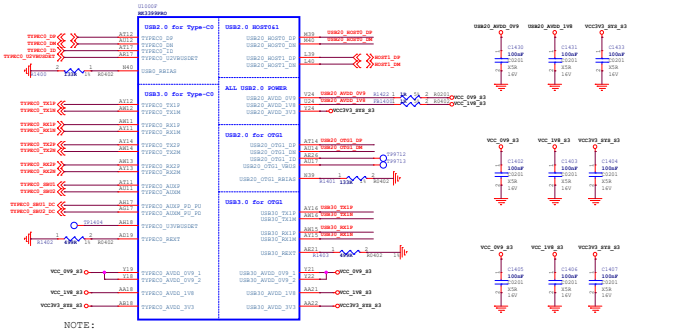
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	RK3399Pro_EVB
File:	12.RK3399Pro DDR Controller
Date:	Friday, November 09, 2018
Rev:	V1.0
Designed by:	Linus Lin
Sheet:	9 of 46

EMMC Controller

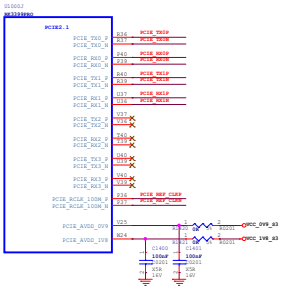


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	13.RK3399Pro EMMC Controller		
Date:	Friday, November 08, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	10 of 40

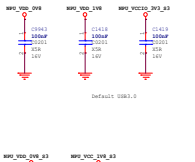
USB

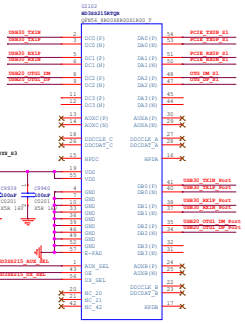


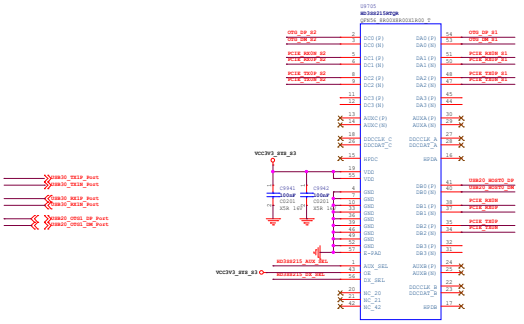
PCIE



NPU PCIE/USB

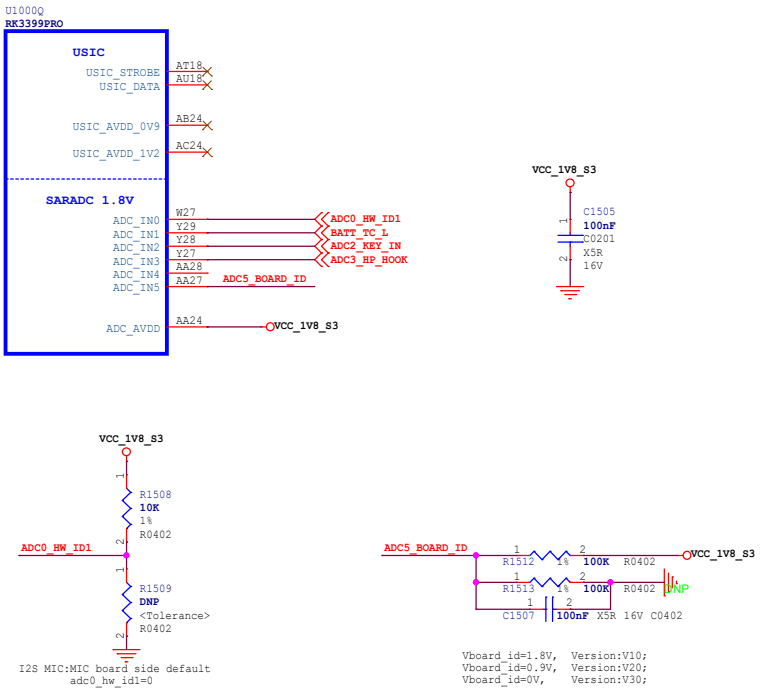






Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	RK3399Pro_EVB
File:	14.RK3399Pro USB/PCIE Centrella
Date:	Tuesday, November 19, 2019
Rev:	V1.3
Designed by:	Linus Lin
Sheet:	11 of 48

SARADC

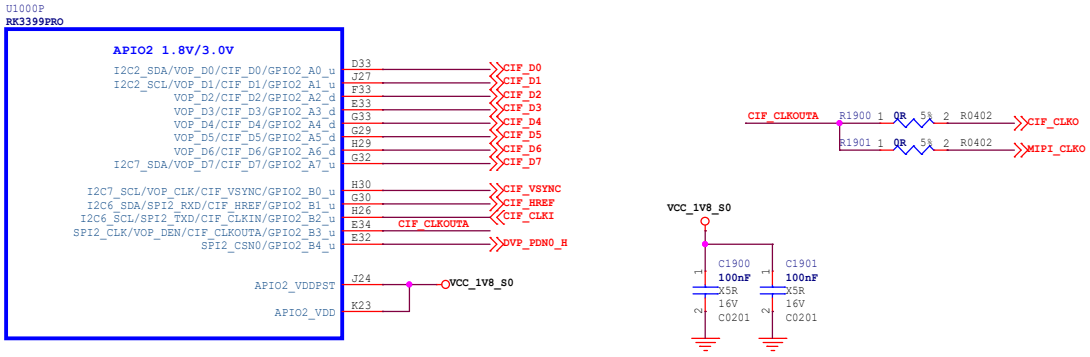


I2S MIC:MIC board side default
adc0_hw_id1=0

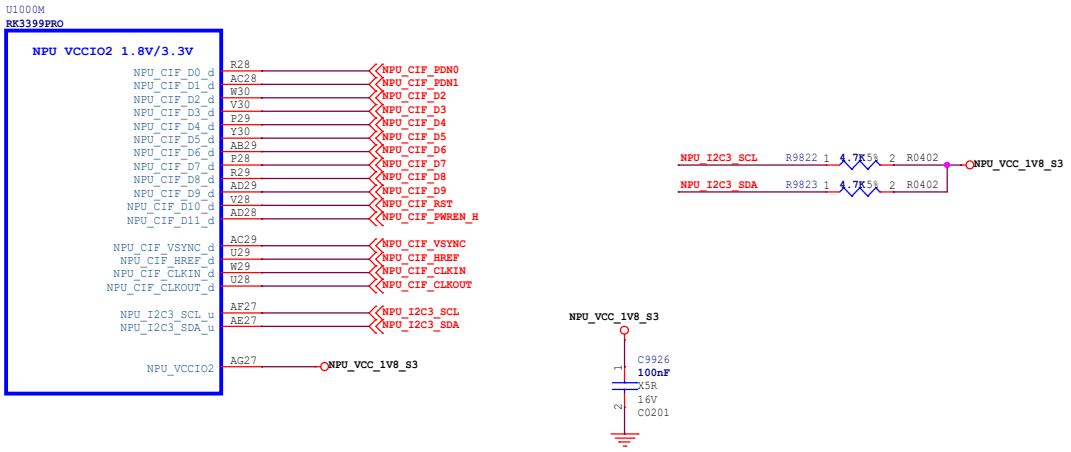
Vboard_id=1.8V, Version:V10;
Vboard_id=0.9V, Version:V20;
Vboard_id=0V, Version:V30;

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	15.RK3399Pro SARADC/USIC		
Date:	Friday, November 08, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	12 of 40

VOP/CIF

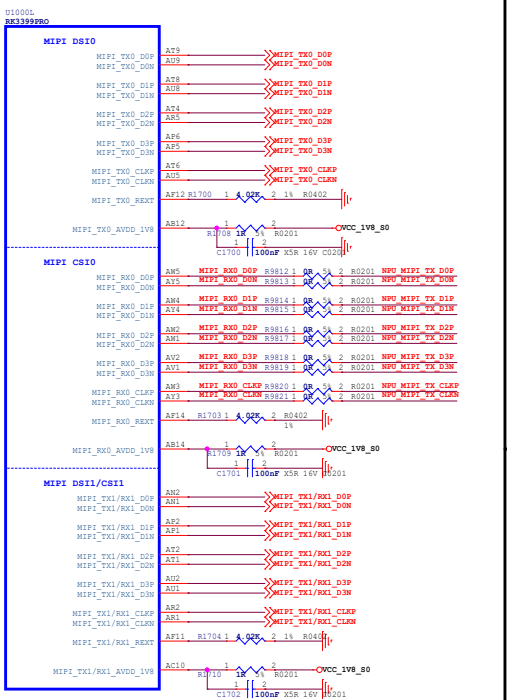


NPU CIF

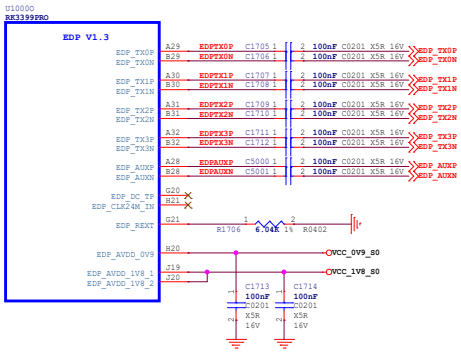


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	16.RK3399Pro VOP/CIF		
Date:	Friday, November 08, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	13 of 40

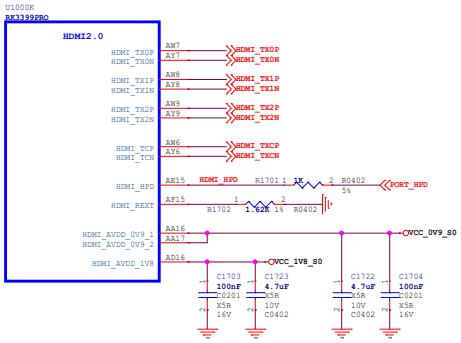
MIPI CSI/DSI



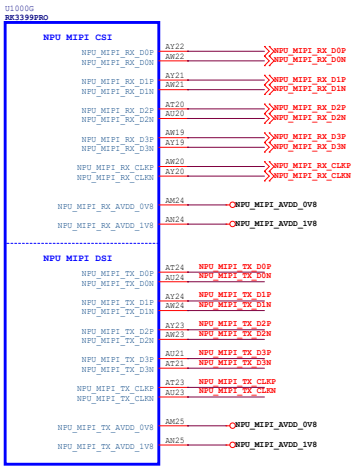
EDP

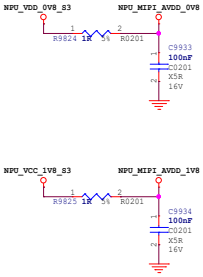


HDMI



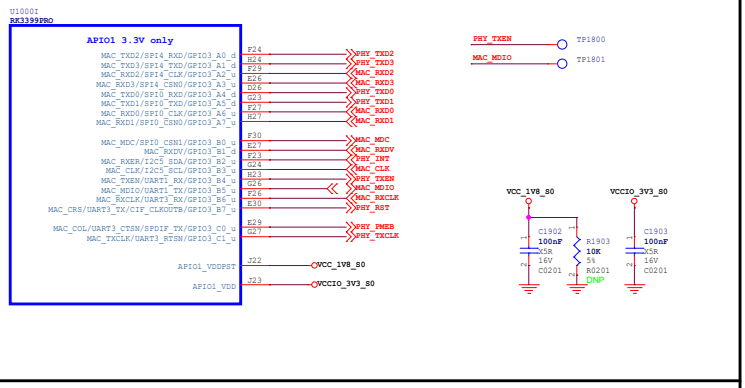
NPU MIPI CSI/DSI





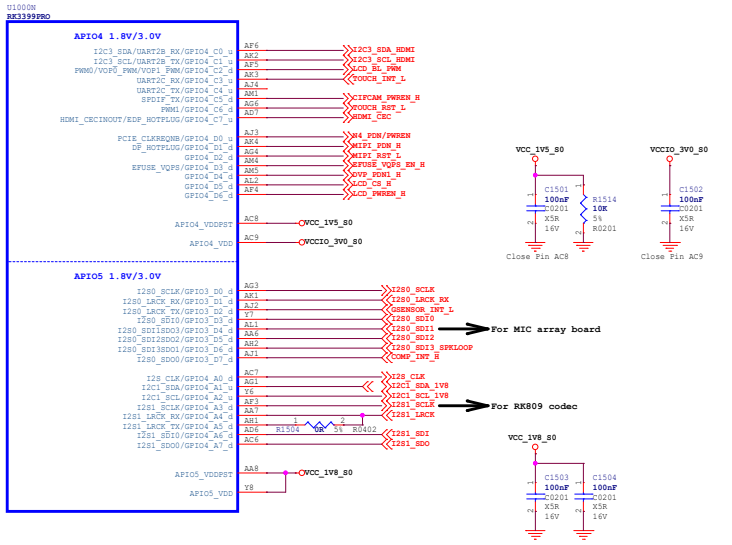
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	17.RK3399Pro Display		
Date:	Friday, November 08, 2019	Rev.	V1.3
Designed by:	Linus.Lin	Sheet	14 of 40

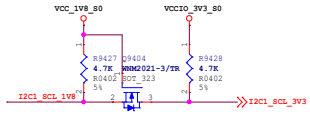
APIO1

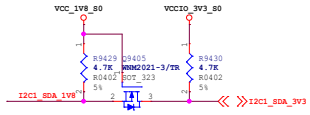


SDMMC0/APIO3

APIO4/APIO5

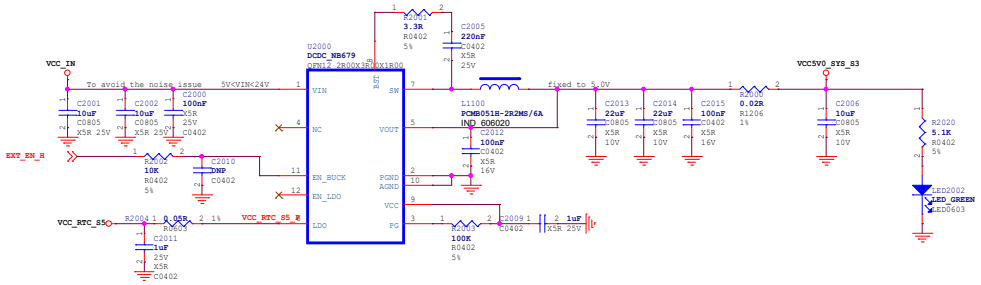




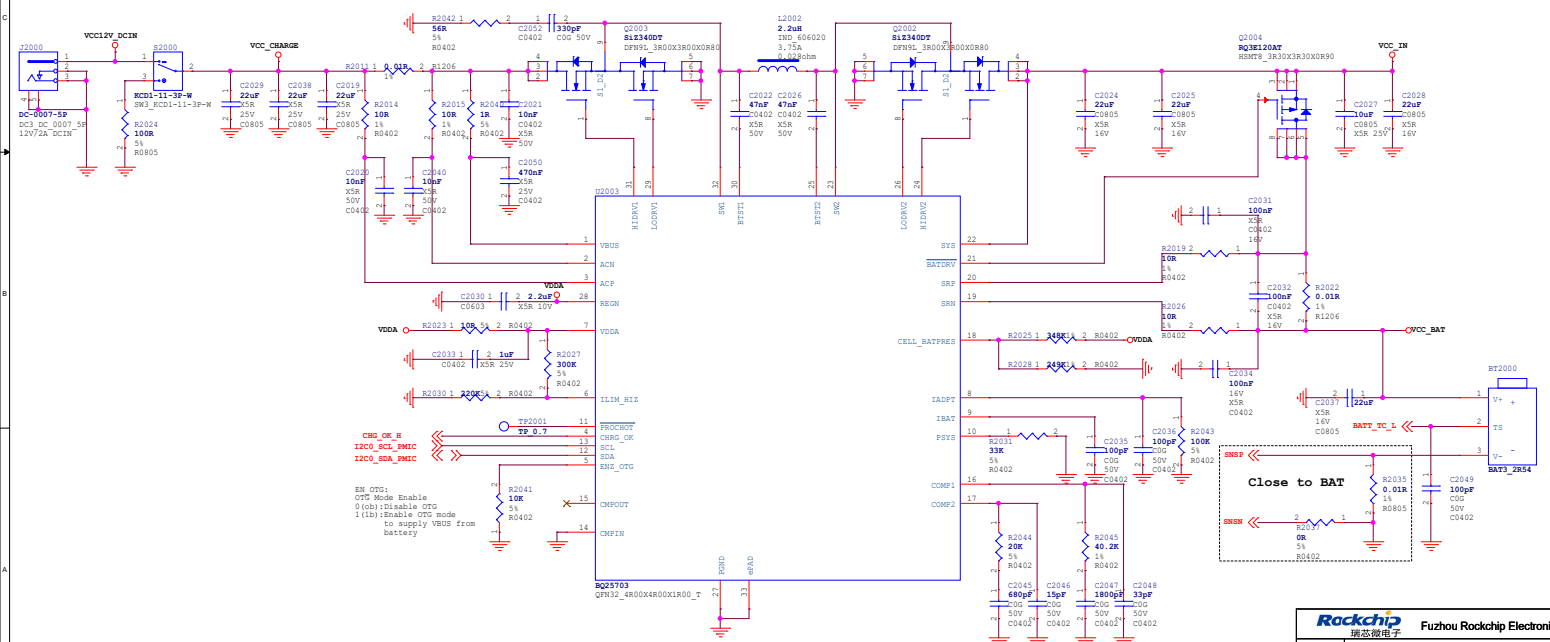


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	18.RK3399Pro GPIO		
Date:	Friday, November 08, 2019	Rev.	V1.3
Designed by:	Linus.Lin	Sheet	15 of 40

SYSTEM Power

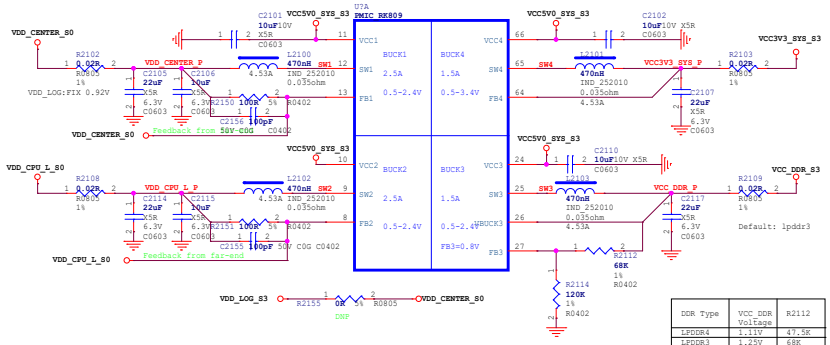


DC IN



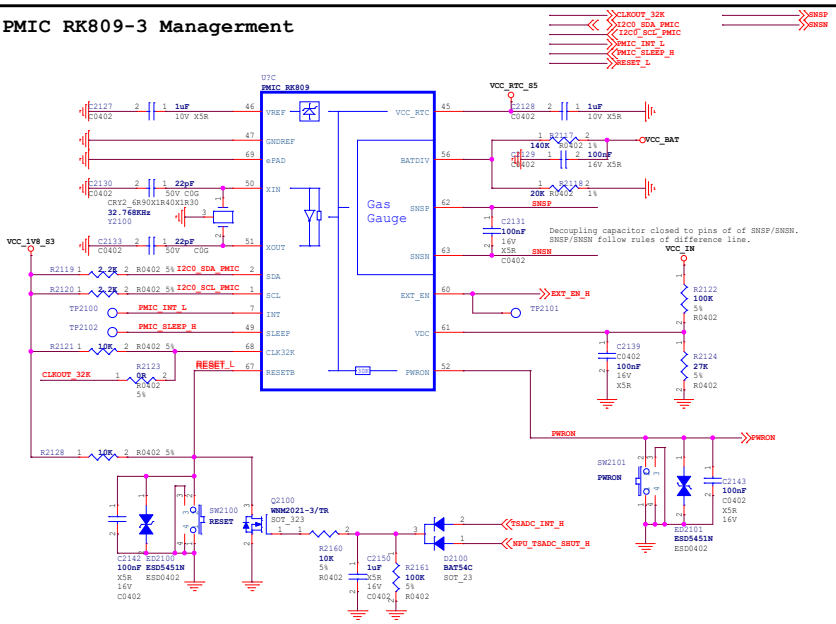
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	20.Power DC IN		
Date:	Tuesday, November 19, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	16 of 40

PMIC RK809-3 DCDC

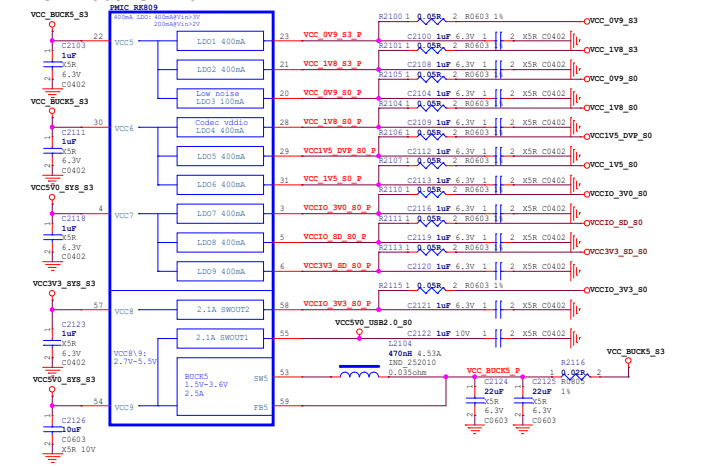


DDR Type	VCC_DDR Voltage	R2112
LPDDR4	1.11V	47.5K
LPDDR3	1.25V	68K
DDR3L	1.35V	82K
DDR3	1.53V	110K

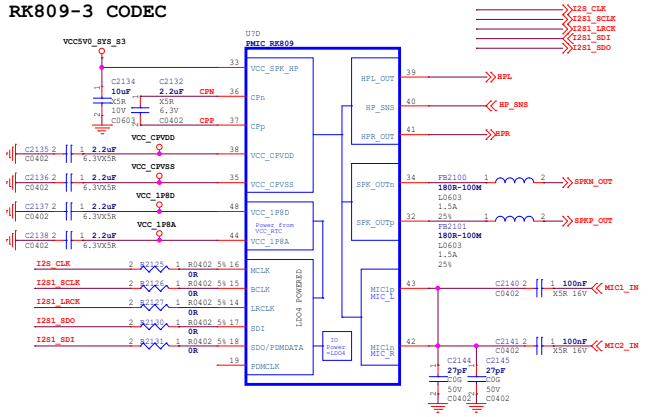
PMIC RK809-3 Managerment



PMIC RK809-3 LDO

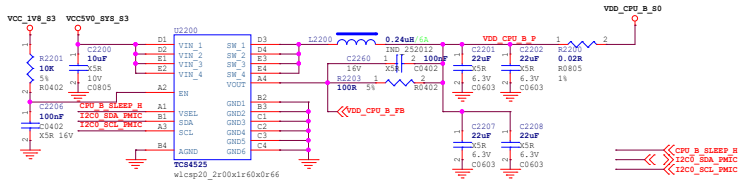


PMIC RK809-3 CODEC

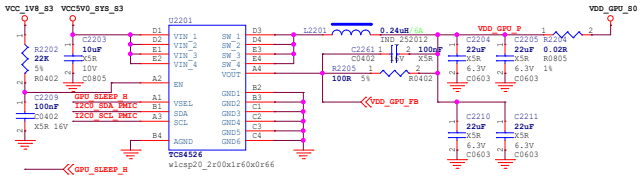


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	RK3399Pro_EVB
File:	21:Power PMIC RK809-3
Date:	Friday, November 08, 2019
Rev:	V1.3
Designed by:	Linus.Lin
Sheet:	17 of 40

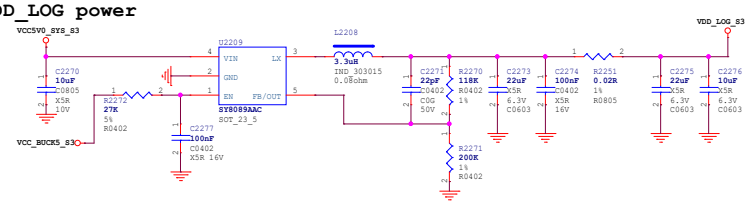
VDD_CPU_B power

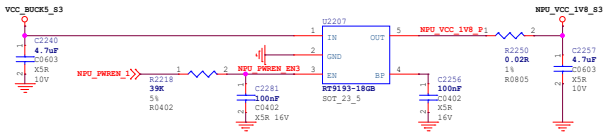


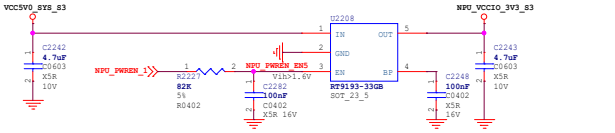
VDD_GPU power

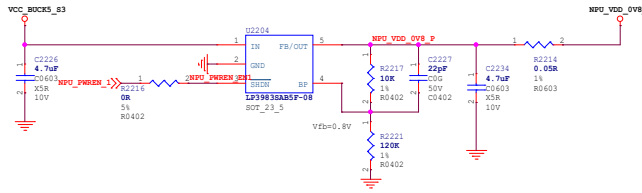


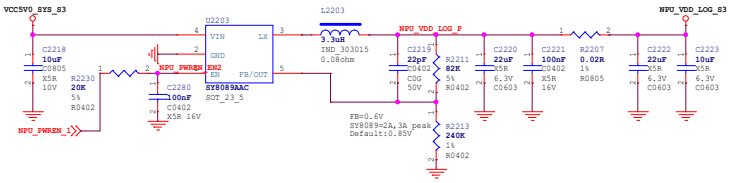
VDD_LOG power

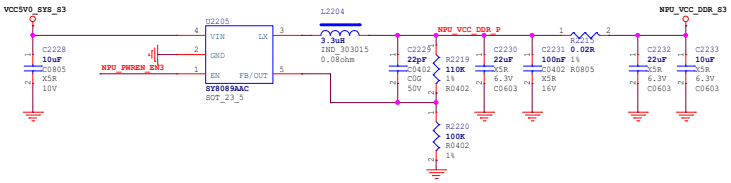


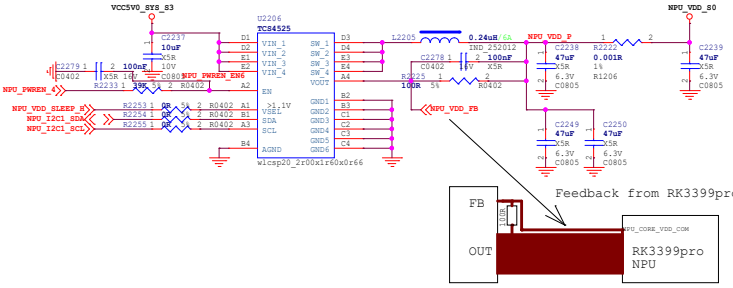


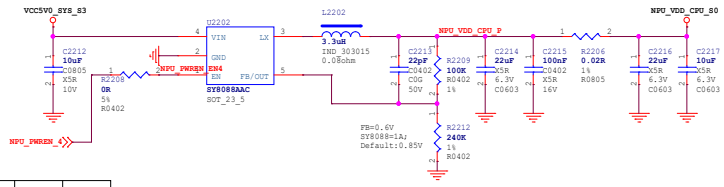










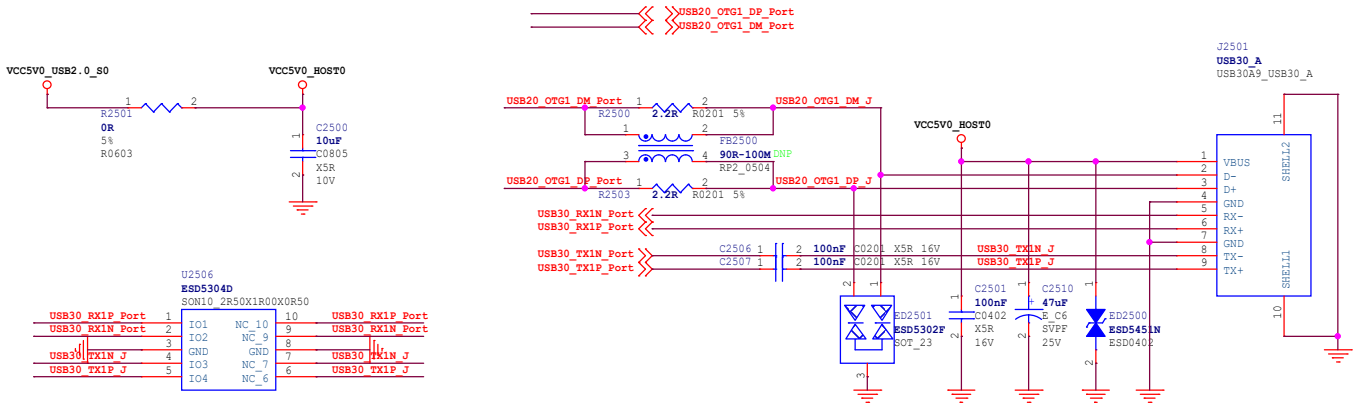


DDR Type	VCC_DDR Voltage	R2219
DDR4	1.25V	110K
LPDDR3	1.25V	110K
DDR3L	1.35V	127K
DDR3	1.53V	154K

NPU Part power

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	RK3399Pro_EVB
File:	22.Power CPU/GPU/NPU
Date:	Tuesday, November 19, 2019
Rev:	V1.3
Designed by:	Linus.Lin
Sheet:	18 of 40

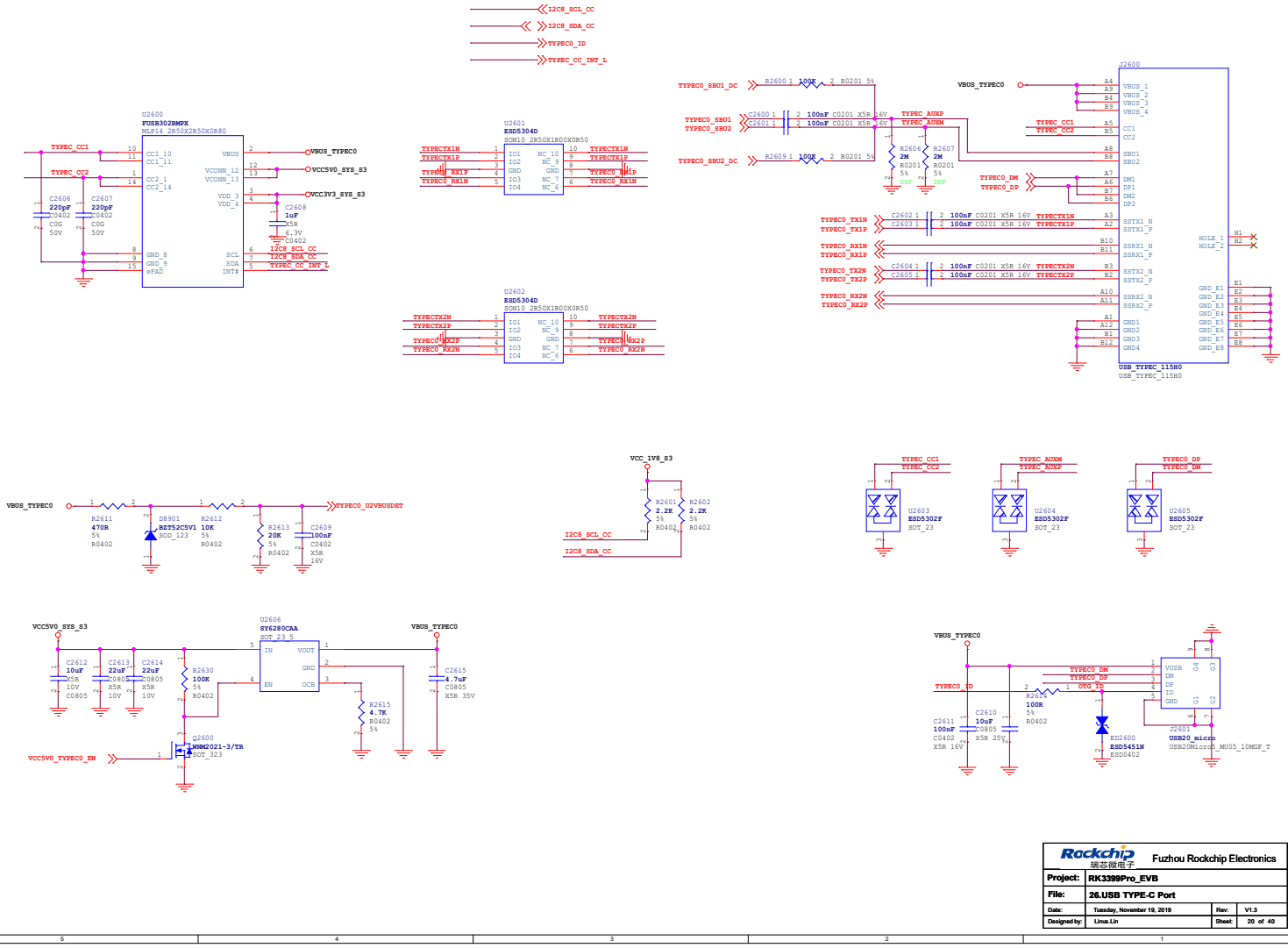
USB3.0 HOST



Note:All the ESD components should be placed close to the port

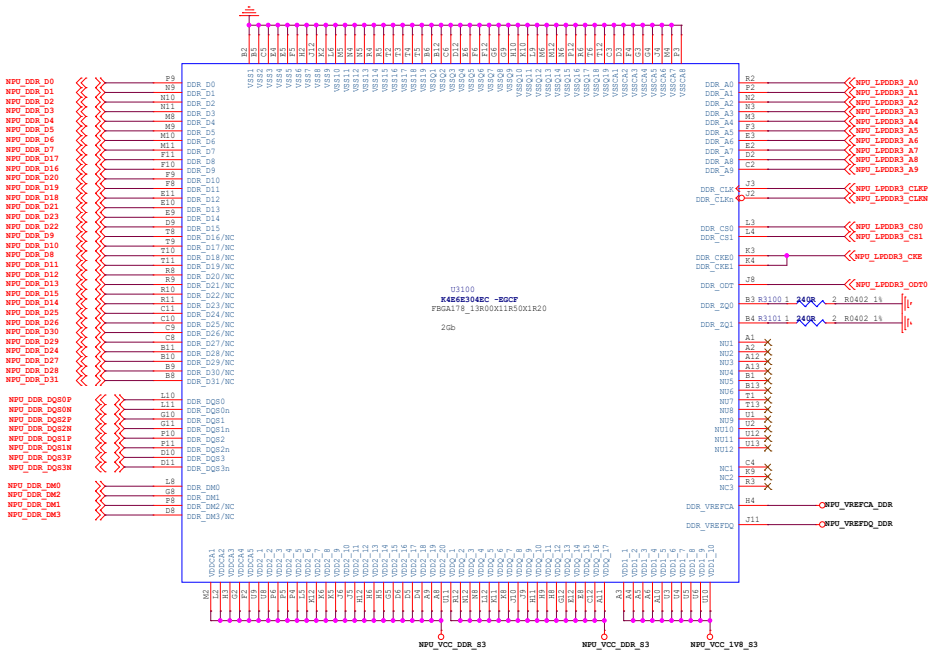
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	25.USB HOST Port		
Date:	Friday, November 08, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	19 of 40

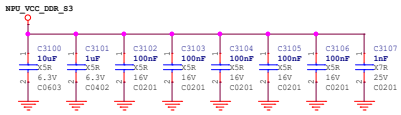
USB Type-C

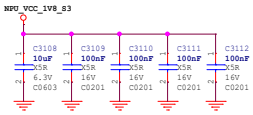


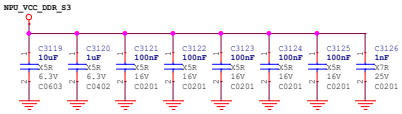
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	RK3399Pro_EVB
File:	26.USB TYPE-C Port
Date:	Tuesday, November 19, 2019
Rev:	V1.3
Designed by:	Linus.Lin
Sheet:	20 of 40

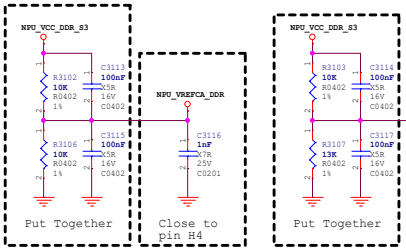
NPU LPDDR3 1x32bit

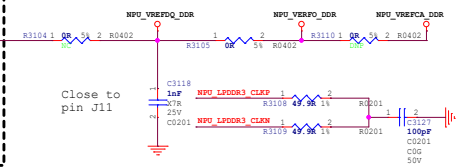












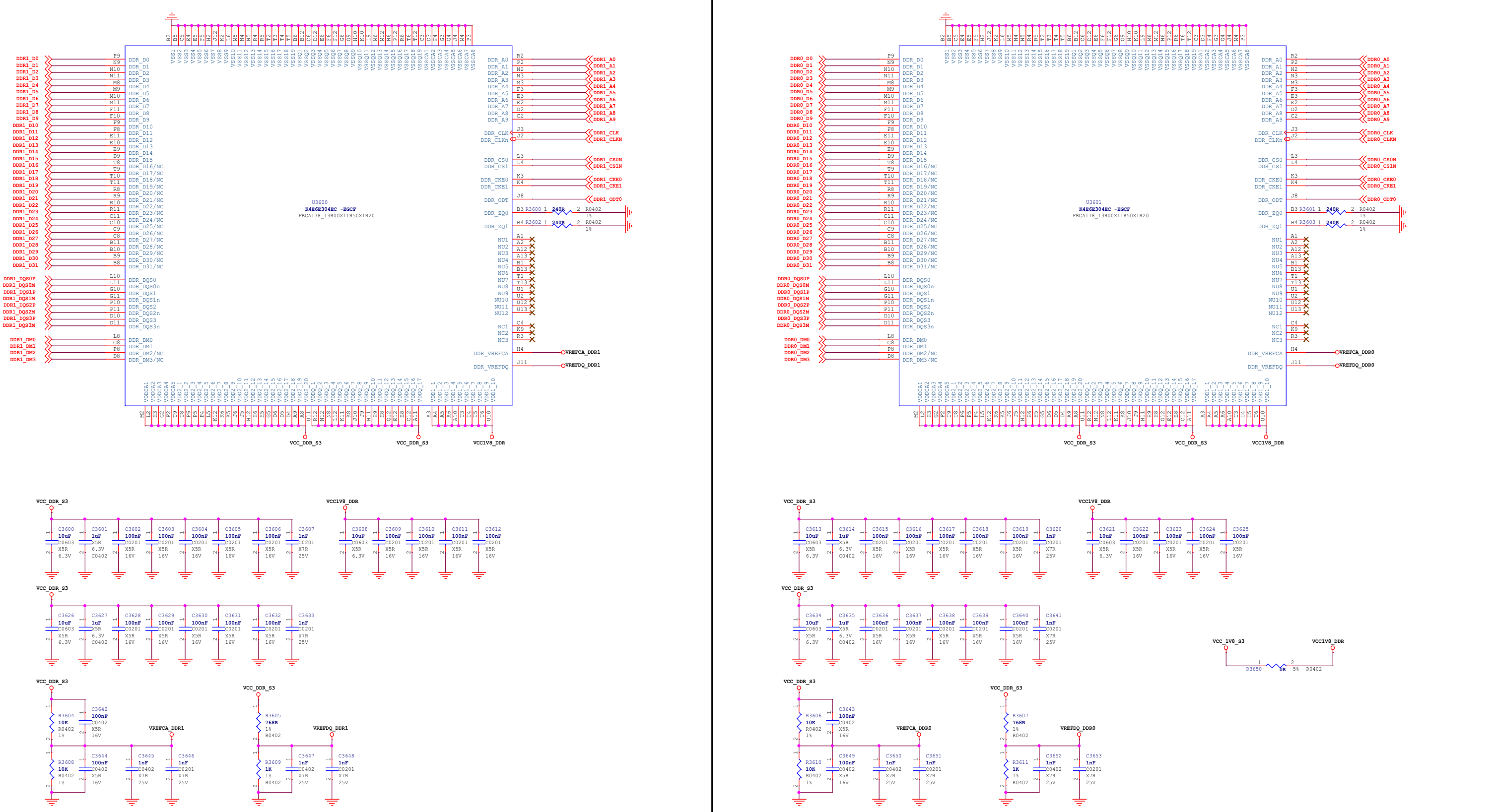
Note:All the power filter capacitors should be placed close to the power pins of LPDDR3

Note:
Vih=VCC
Vil=VCC*Ron/(Ron+Rodt)
VREFDQ_DDR=(Vih+Vil)/2

eg:VCC=1.2V,Ron=34ohm,Rodt=240ohm
so,Vih=1.2V,Vil=0.149V,VREFDQ_DDR=0.674V

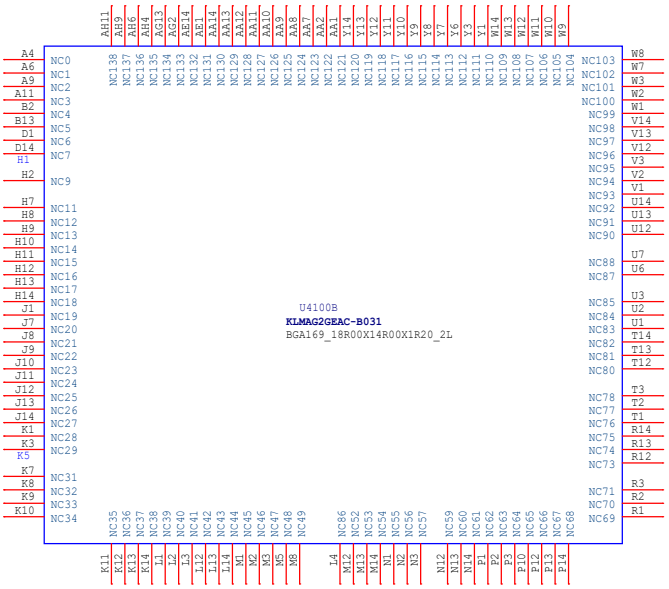
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	RK3399Pro_EVB
File:	31.NPU RAM-LPDDR3 1x32bit
Date:	Friday, November 08, 2019
Rev:	V1.3
Designed by:	Linus.Lin
Sheet:	21 of 40

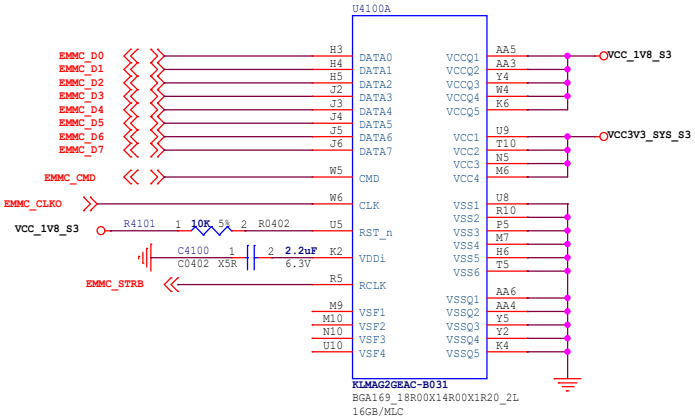
LPDDR3

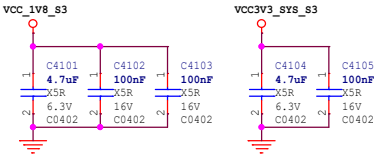


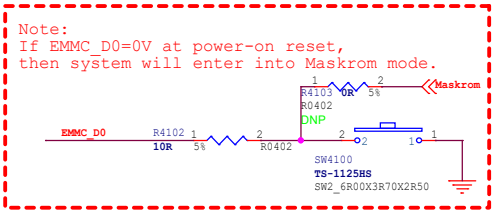
Fuzhou Rockchip Electronics	
Project:	RK3399Pro_EVB
File:	36.RAM-LPDDR3(178P)
Date:	Friday, November 08, 2019 — Rev: V1.3
Designed by:	Linus.Lin — Sheet: 22 of 40

eMMC









Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	41.EMMC		
Date:	Friday, November 08, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	23 of 40

USB2.0 HUB

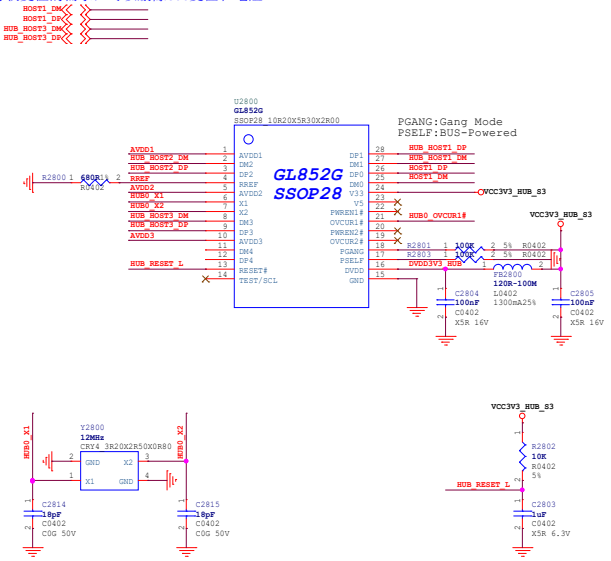
Note:

模块原理图设计说明（正式参考图请删除）：

HOST1_DP/DM是SOC给出来的信号。

有些HUB芯片的晶体必须要加1M电阻，否则不起振，更换的时候请注意。

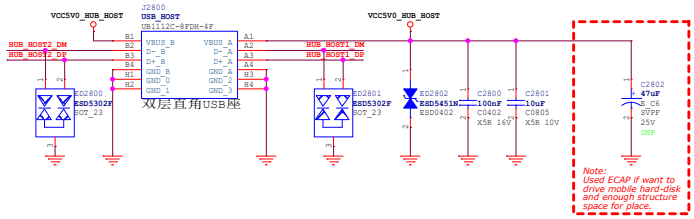
如果没有软复位的需求，可以删除SOC复位和电阻。



USB2.0 Port

Note:Note:All the ESD components should be placed close to the port

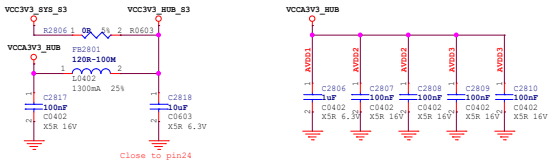
模块原理图设计说明（正式参考图请删除）：



Power

Note:All the Power filter capacitors should be placed close to the power pins of GL852G.

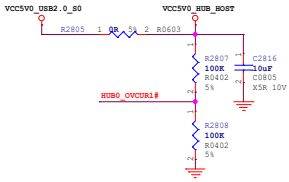
模块原理图设计说明（正式参考图请删除）：



Over-Current Protection

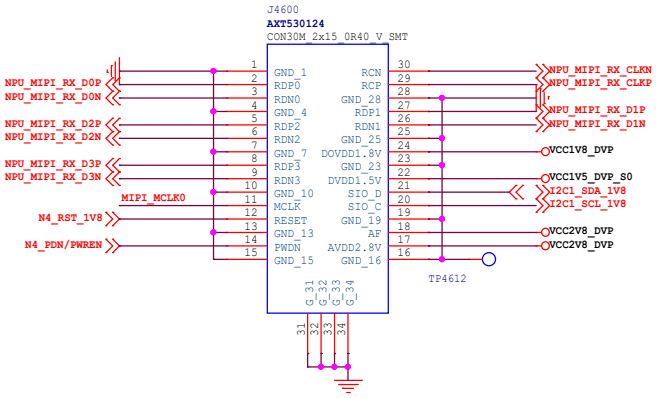
Note:Note:All the ESD components should be placed close to the port

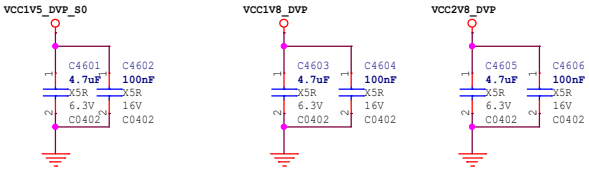
模块原理图设计说明（正式参考图请删除）：

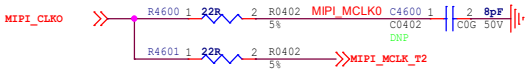


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	28.USB HUB-USB2.0		
Date:	Tuesday, November 19, 2019	Rev:	V1.2
Designed by: Linus.Lin	Reviewed by: <Checker>	Sheet:	23 of 49

MIPI CSI of N4

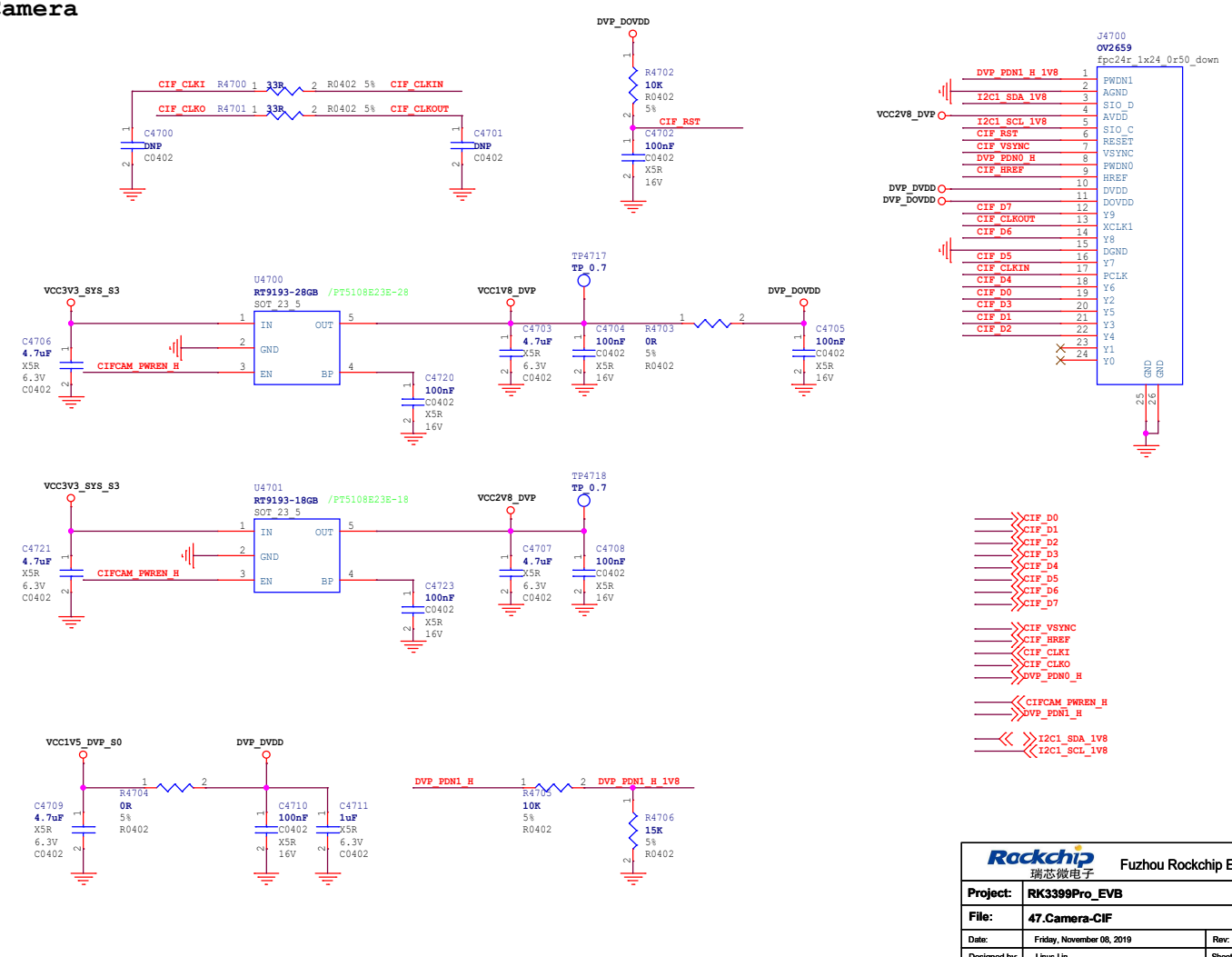






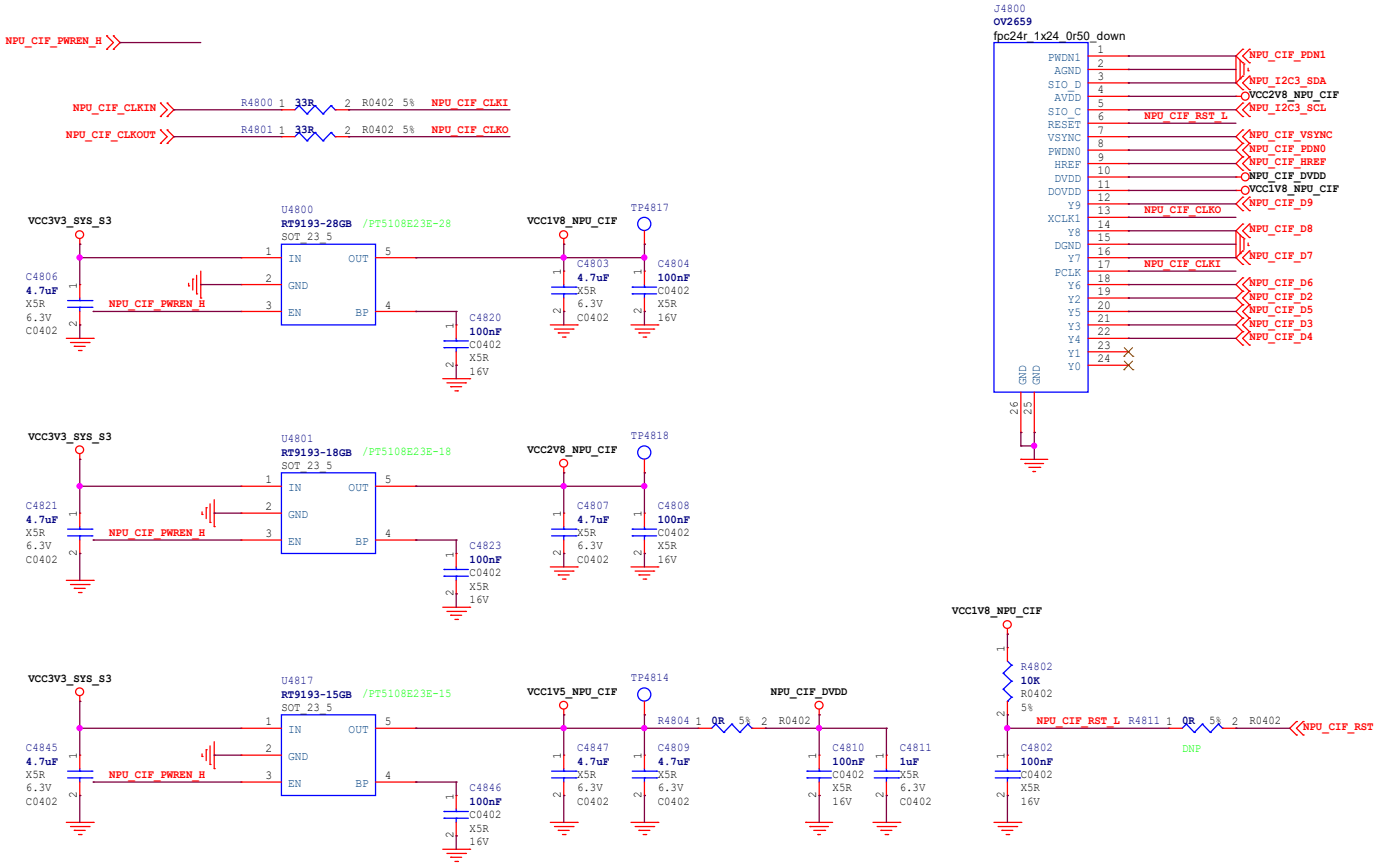
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	46.MIPI CSI to N4		
Date:	Friday, November 08, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	24 of 40

CIF Camera



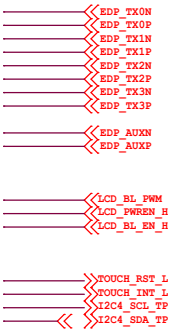
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	47.Camera-CIF		
Date:	Friday, November 08, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	25 of 40

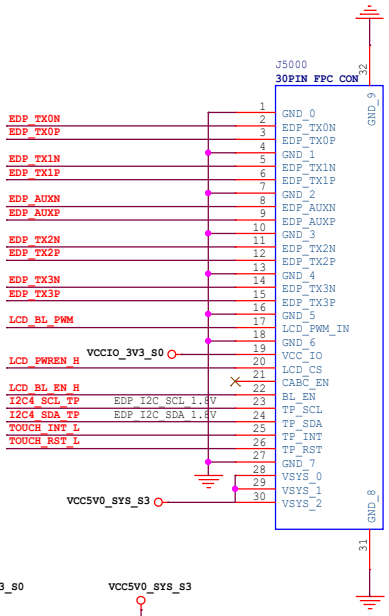
CIF Camera(bt656)

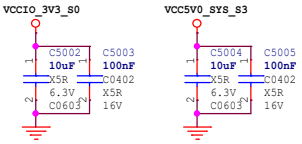


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	48.Camera-NPU CIF		
Date:	Friday, November 08, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	26 of 40

eDP PORT

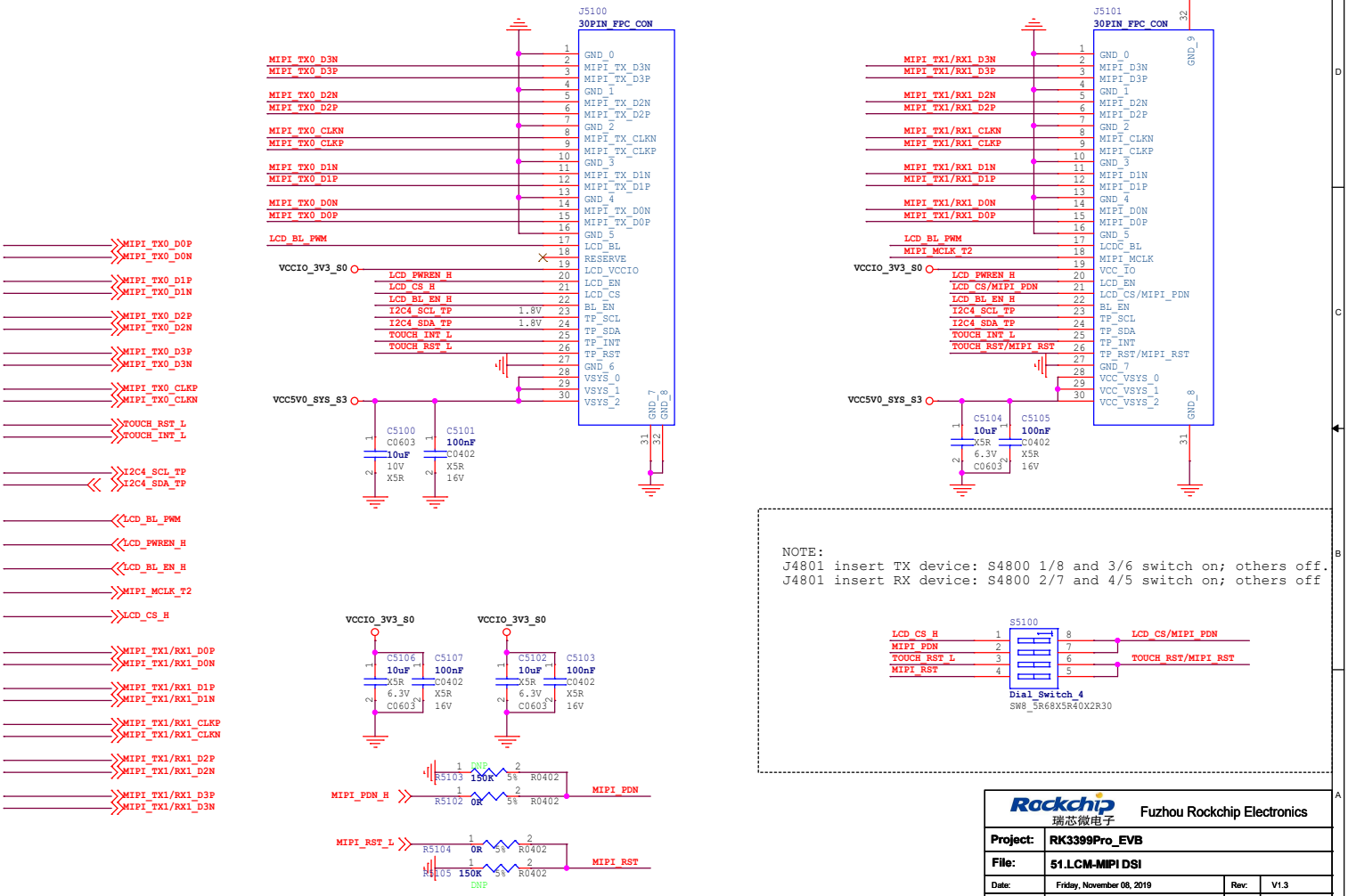






Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	50.LCM-eDP Panel		
Date:	Friday, November 08, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	27 of 40

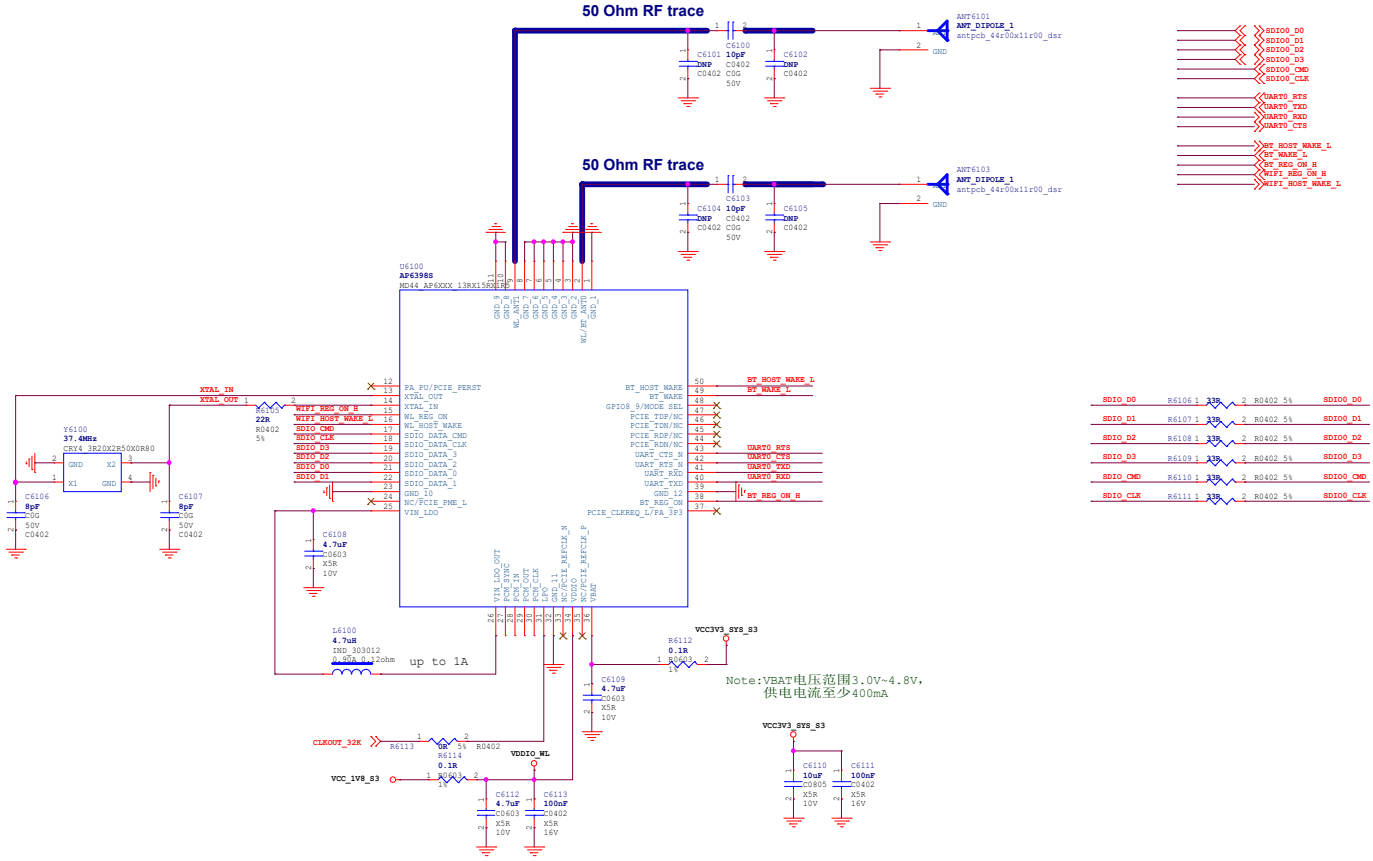
MIPI DSI



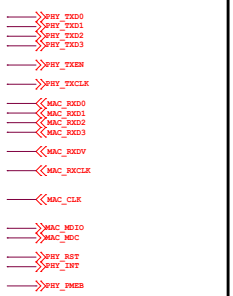
NOTE:
J4801 insert TX device: S4800 1/8 and 3/6 switch on; others off.
J4801 insert RX device: S4800 2/7 and 4/5 switch on; others off

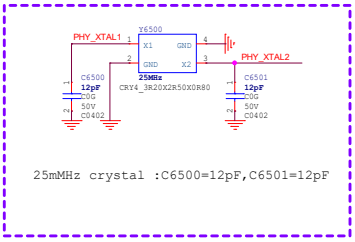
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	51.LCM-MIPI DSI		
Date:	Friday, November 08, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	28 of 40

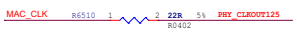
WIFI/BT MODULE

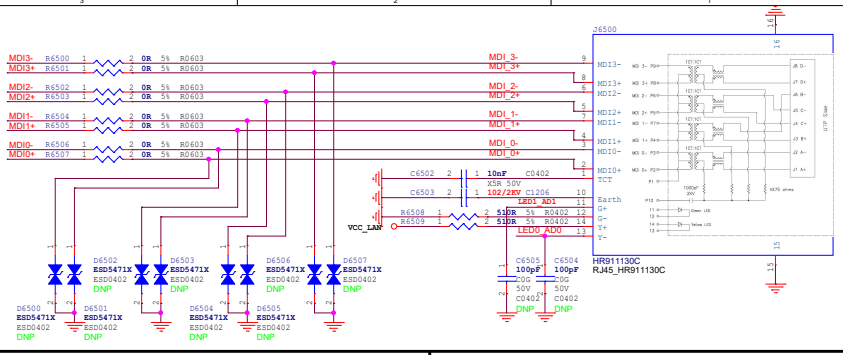


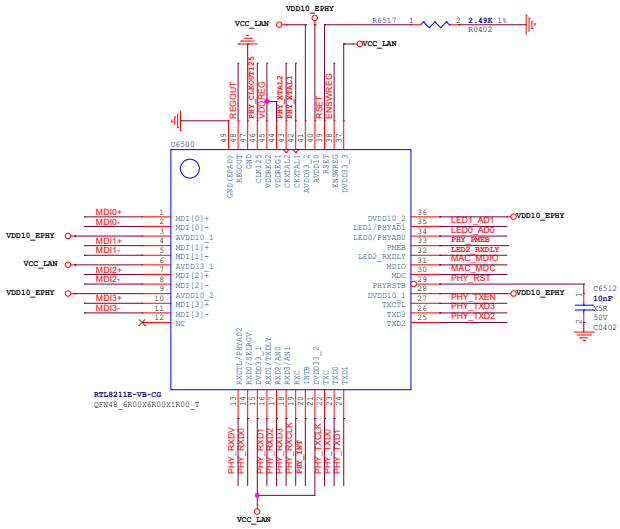
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	61.WIFI/BT AP6398S		
Date:	Tuesday, November 19, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	29 of 40

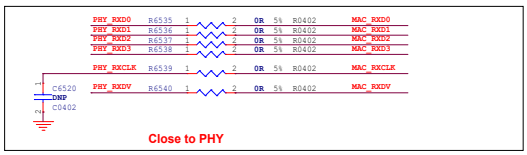


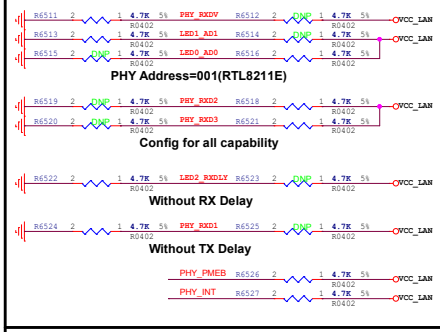


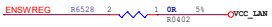




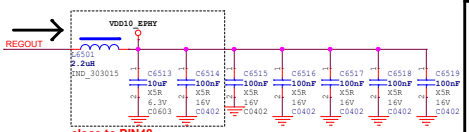


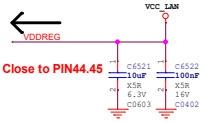


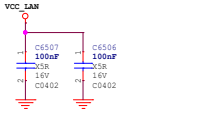


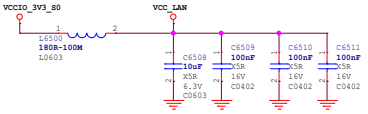


Connect ENSWREG to AVDD33 to enable
Switching regulator or connect ENSWREG
to GND to disable Switching regulator.







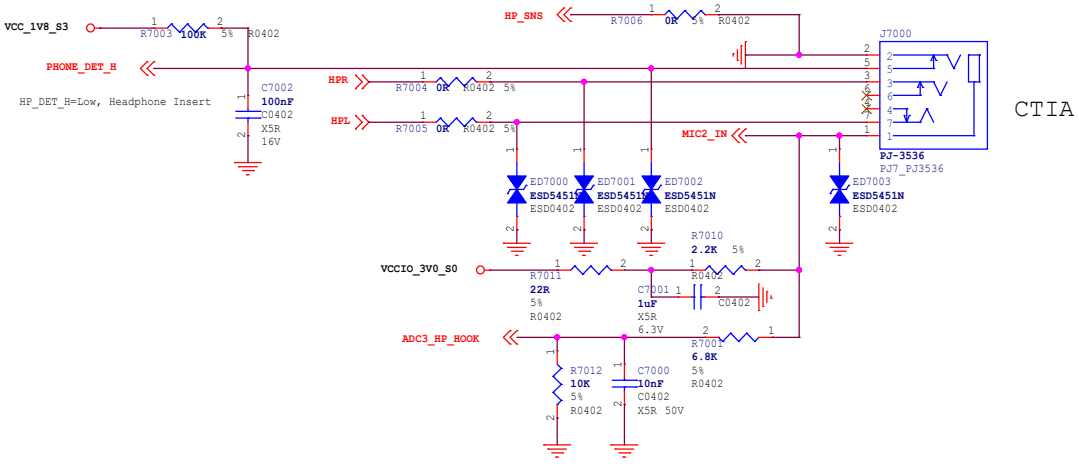


Pull down for 2.5V RGMII(RTL8211D/8211E)
Pull up for 3.3V RGMII (RTL8211D/8211E)
Pull up1.5 /1.8V RGMII (RTL8211E-VL only)

RGMII 1000M

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	65.RGMII-10/100/1000M		
Date:	Friday, November 08, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	30 of 40

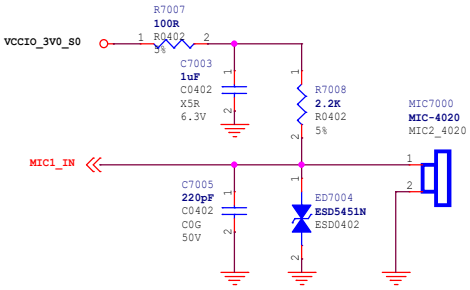
HEADPHONE



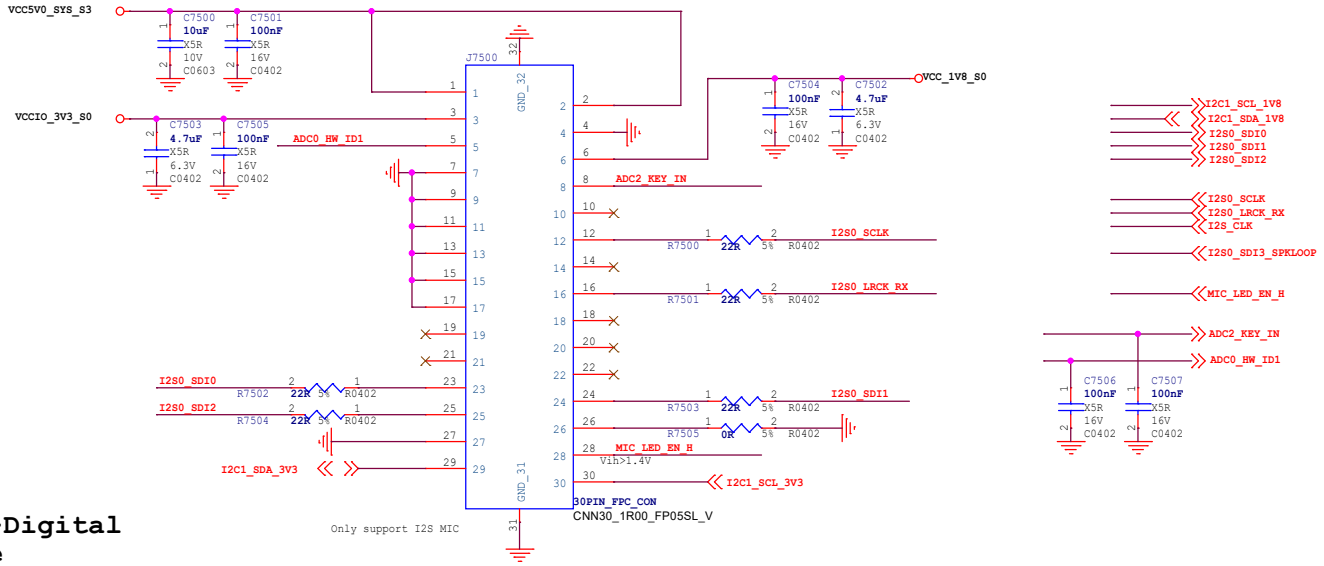
CTIA

SPEAKER

MIC

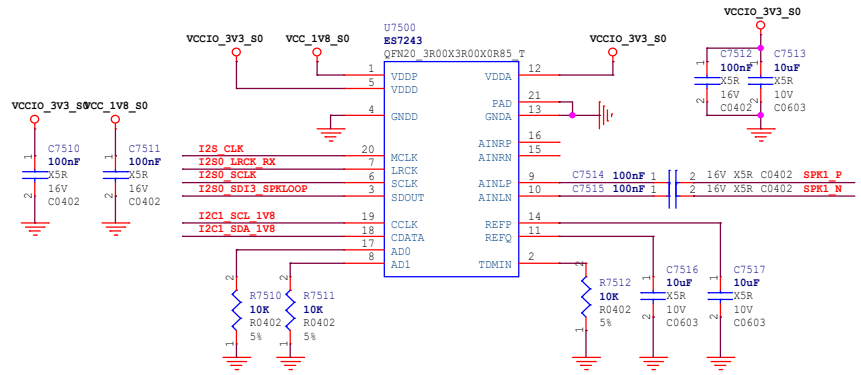


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	70.AUDIO1		
Date:	Wednesday, November 20, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	31 of 40



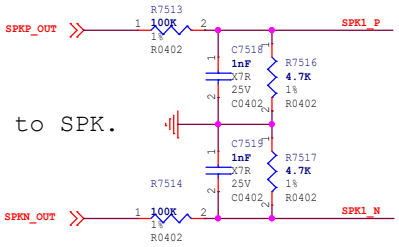
MIC Array-Digital Interface

ADC Loopback



I2C Chip ID = 0x26

Place this loopback ADC close to Amplifier.

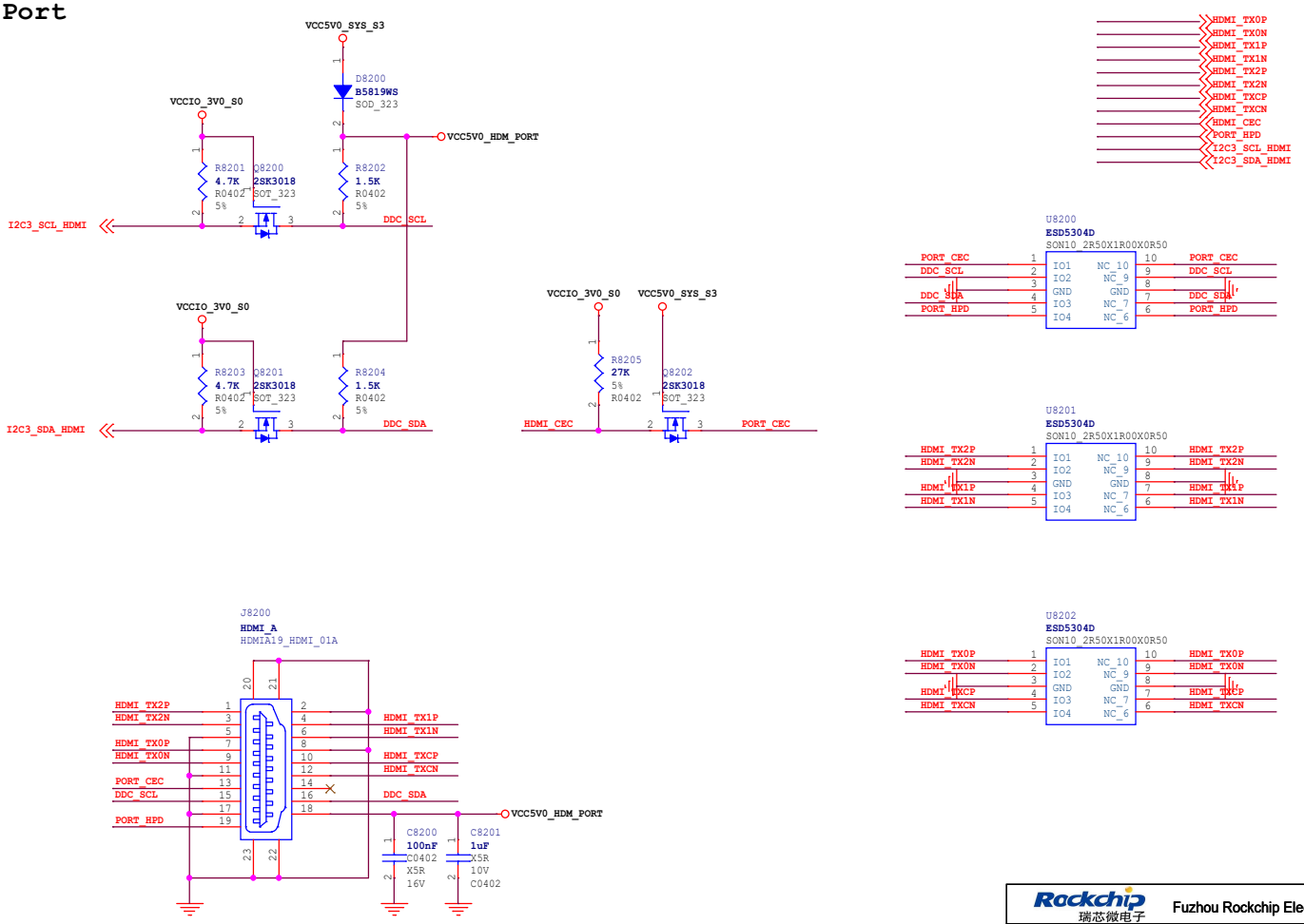


Closed to SPK.

Notice the divided voltage should be suit to the ADC input parameters.

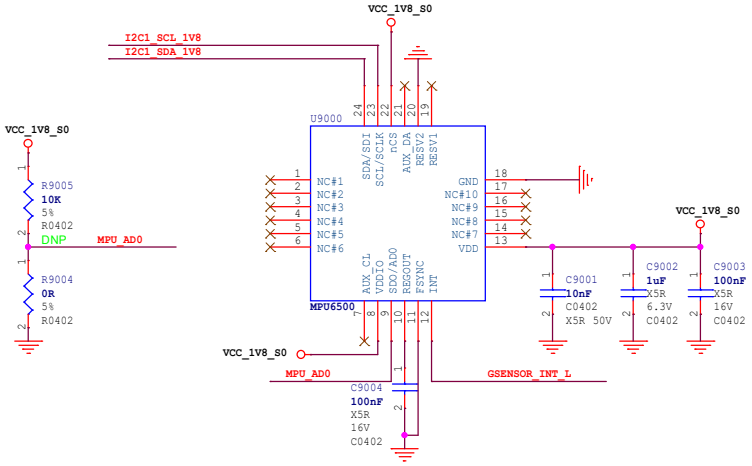
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	75.AUDIO2-MIC Array Connector		
Date:	Wednesday, November 20, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	32 of 40

HDMI Port



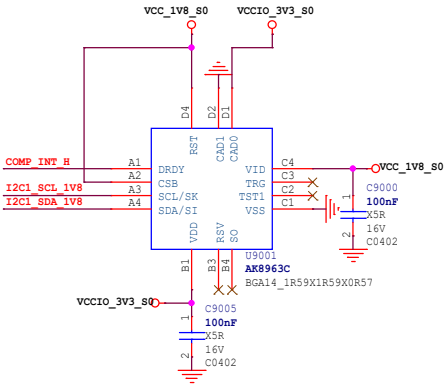
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	82.HDMI Port		
Date:	Friday, November 08, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	33 of 40

Gyroscope+G-sensor

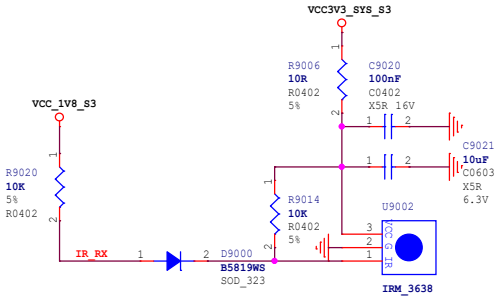


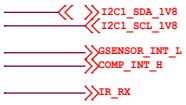
Compass

Note:
The first pin of AK8963C must be place on the lower left corner of PCB.



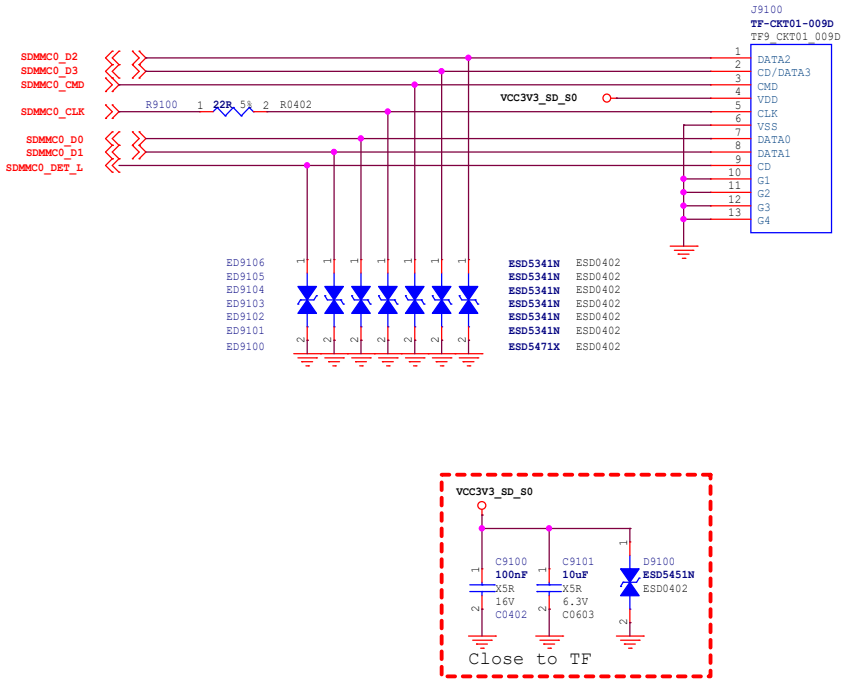
IR





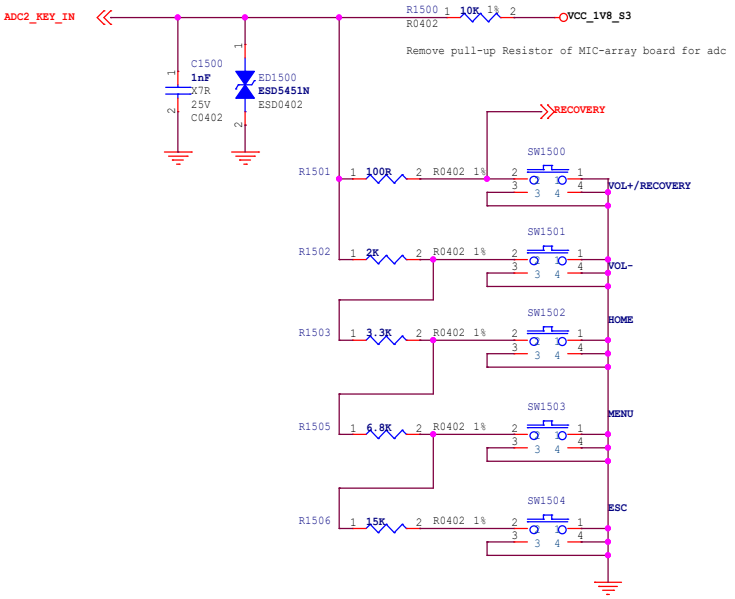
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	90.Sensor		
Date:	Tuesday, November 19, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	34 of 40

TF Card



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	91.TF Card		
Date:	Friday, November 08, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	35 of 40

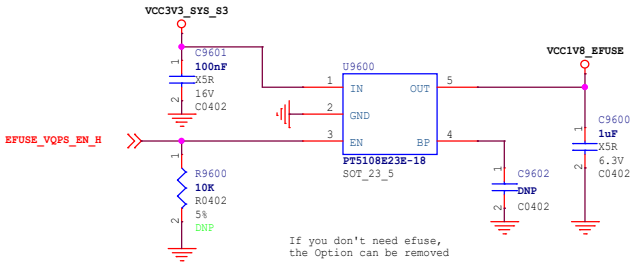
Key Array



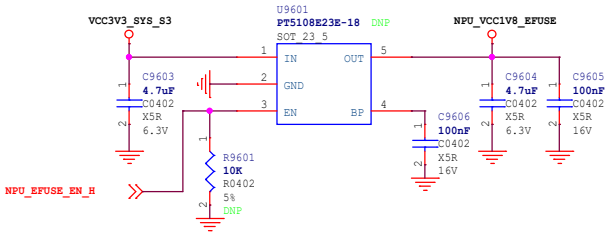
Key Name	SARADC
VOL+/RECOVERY	10
VOL-	170
HOME	354
MENU	560
ESC	747

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	92.Key Array		
Date:	Friday, November 08, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	36 of 40

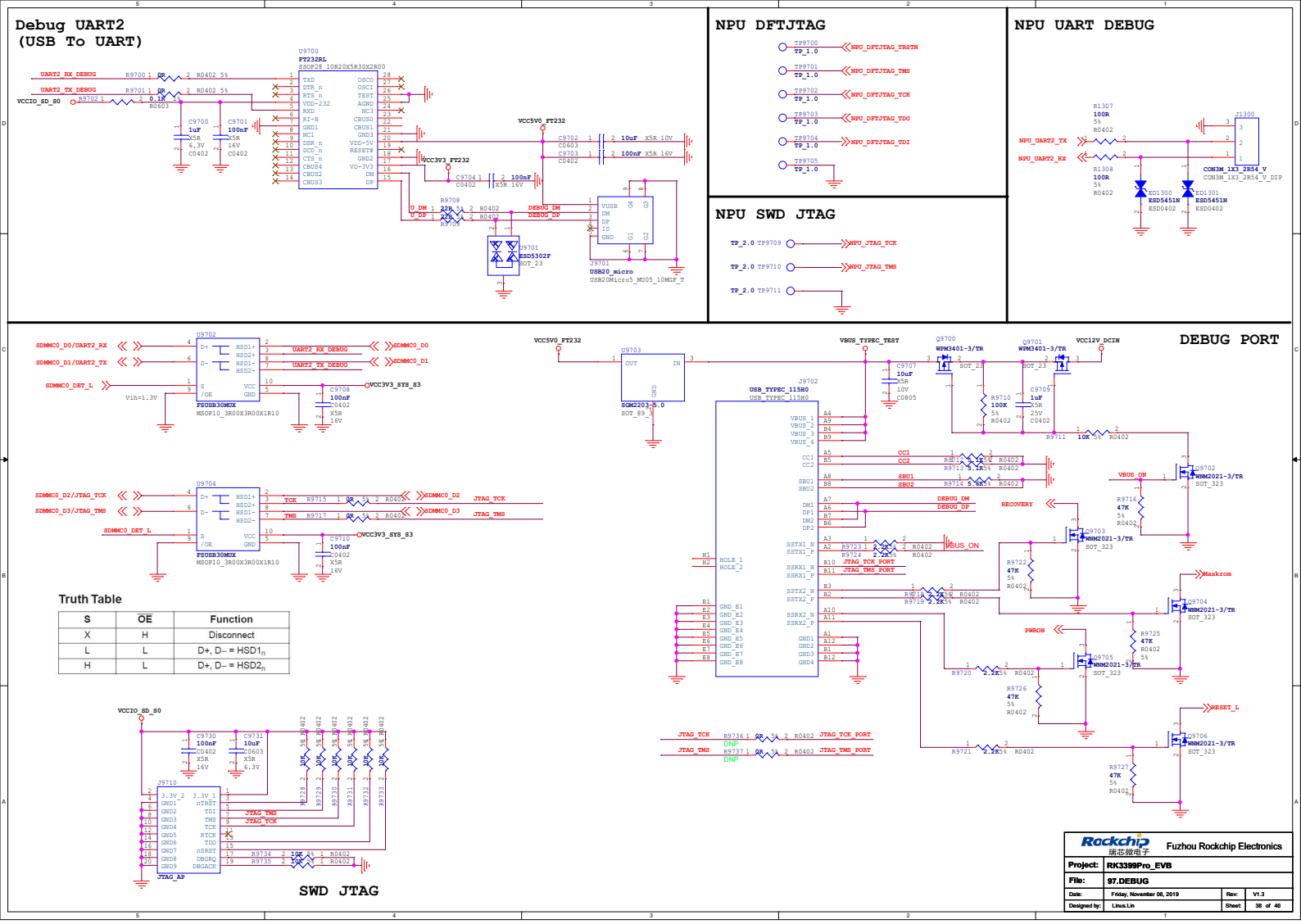
EFUSE POWER



NPU EFUSE POWER



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399Pro_EVB		
File:	96.EFUSE		
Date:	Friday, November 08, 2019	Rev:	V1.3
Designed by:	Linus.Lin	Sheet:	37 of 40


Debug UART2
(USB To UART)
NPU DFTJTAG
NPU UART DEBUG
NPU SWD JTAG
DEBUG PORT
SWD JTAG
Truth Table
S
OE
Function
X
H
Disconnect
L
L
D+, D– = HSD1n
H
L
D+, D– = HSD2n
Fuzhou Rockchip Electronics
Project: RK3399Pro_EVB
File: 97.DEBUG
Date: Friday, November 08, 2019
Rev: V1.3
Designed by: Linus.Lin
Sheet: 38 of 40