

密级状态：绝密（ ） 秘密（ ） 内部资料（ ） 公开（√）

# RK3588\_HW\_Test\_Report\_Summary

福州硬件开发中心

瑞芯微电子股份有限公司

版本号：V1.2\_20220829

## 更改记录

版本	修改人	修改日期	修改说明	备注
V1.1	福州硬件开发中心	2022.03.31	首次发布	
V1.2	福州硬件开发中心	2022.08.29	1) 电源稳波测试数据更新。---PAGE6 2) 上电时序测试更新为RK806-1。---PAGE7 3) 更新核心模块的极限电流表。---PAGE12	

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## 01 电源纹波测试



测试条件：

测试环境: RK3588 EVB7, 环境温度24°C, TSADC最高75°C。

测试场景：Antutu8.4.3,stressapptest。

测试要求：打开余辉功能，示波器通道  $50\Omega$ ，关闭带宽限制。

测试结果：

## 02.上电时序测试



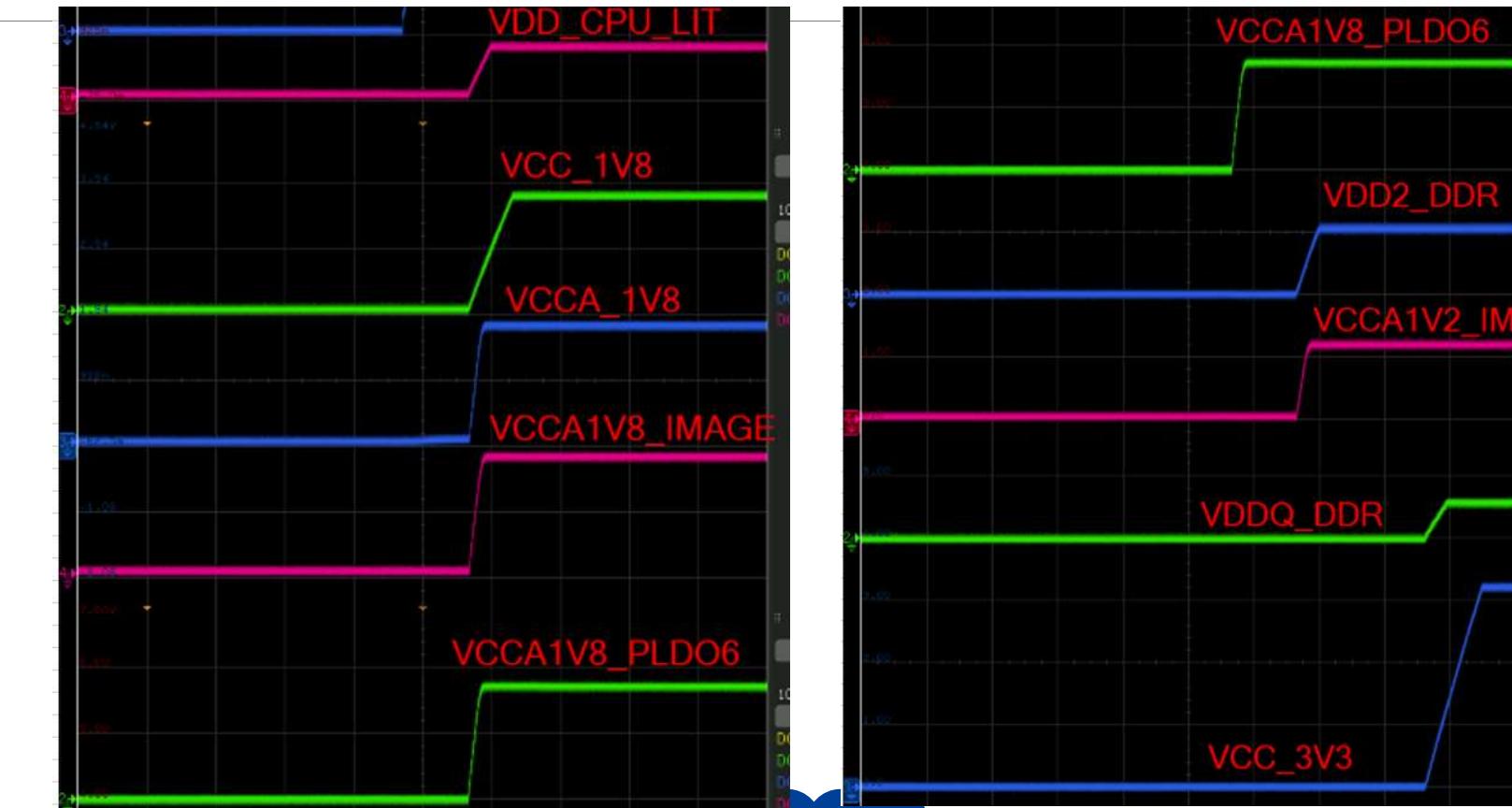
测试环境：RK3588 NVR DEMO，单RK806—1



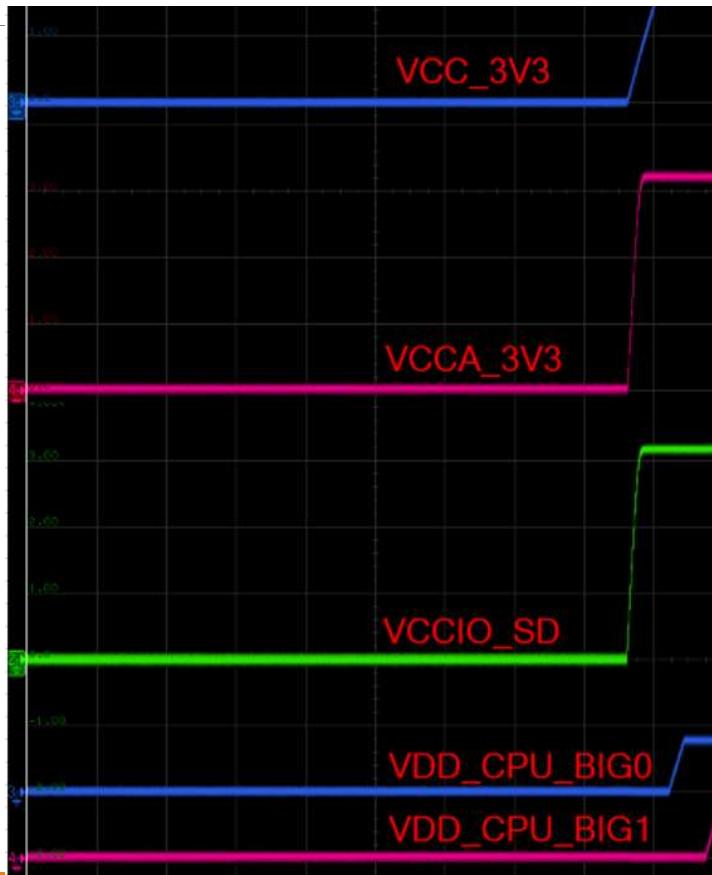
## 02.上电时序测试



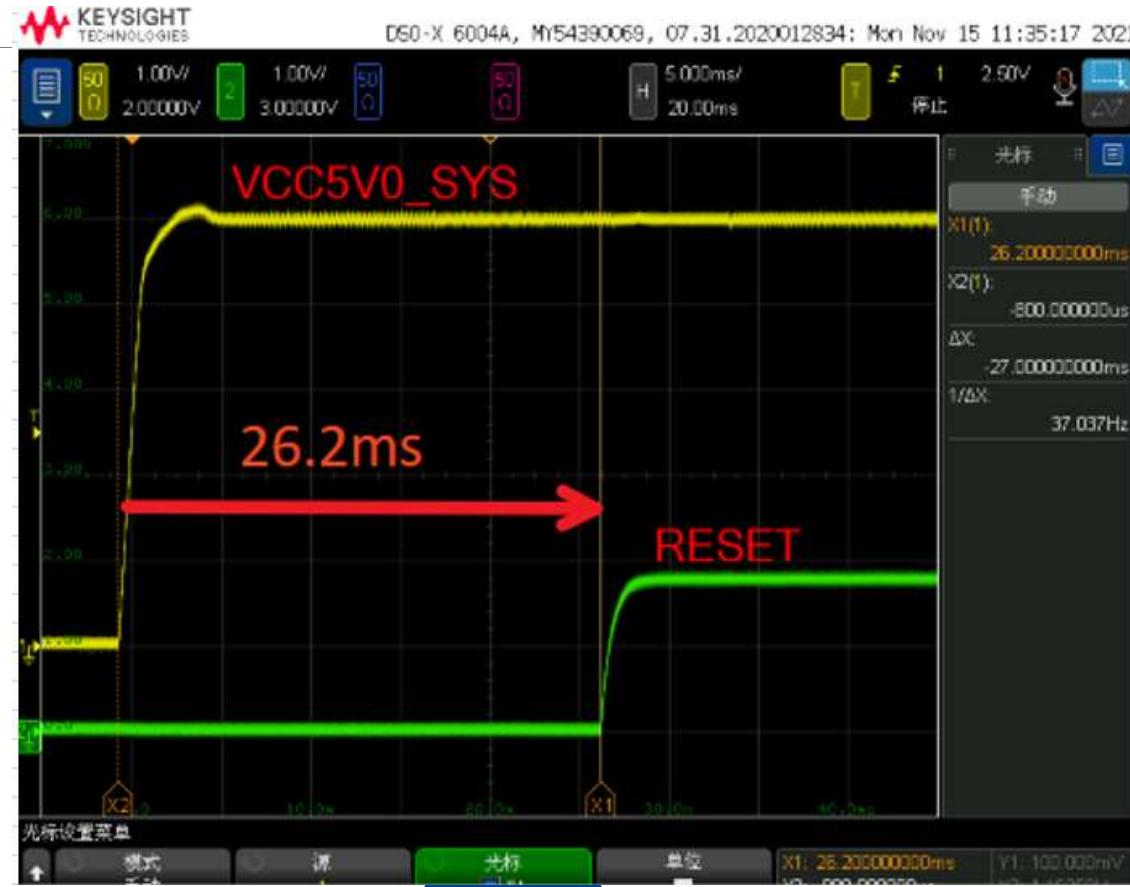
## 02.上电时序测试



## 02.上电时序测试



## 02.上电时序测试



## 03.功耗测试



RK3588各个核心模块的极限电流如下：

### RK3588核心模块极限电流（高温）参考

测试条件：芯片结温100℃；

散热情况：裸板，无散热片；

测试方法：开发板工作稳定后，运行15分钟记录；

运行场景：不同模块在运行各自极限场景环境下测试所得；

注意：以下数据为内部研发板上的测试数据，仅供设计参考，不代表芯片的最终能力。功耗与产品实际应用场景强相关，如需深度优化，可与技术支持人员进一步探讨；

核心模块 极限电流	电源网络	电压 (V)	峰值电流 (A)	峰值功率 (W)	备注
	VDD_CPU_BIG0_S0	0.980	4.00	3.92	频率2400MHz
	VDD_CPU_BIG1_S0	0.980	4.00	3.92	频率2400MHz
	VDD_CPU_LIT_S0	0.950	3.00	2.85	频率1800MHz
	VDD_LOG_S0	0.750	2.50	1.88	
	VDD_GPU_S0	0.850	6.50	5.53	频率1000MHz
	VDD_NPU_S0	0.850	4.00	3.40	频率1000MHz
	VDD_VDENC_S0	0.775	2.50	1.94	频率750MHz
	VDD_DDR_S0	0.870	2.50	2.18	频率2112MHz

更详细的电流参数请参考发布的“RK3588 Power Consumption Test Report V1.1\_20220829\_CN”

# 04.LPDDR4



LPDDR4 Test Report								
Hardware Ver:	RK_NVR_DEMO_RK3588_LP4XD200P232SD8_V10_20210929new_final_lint.ord	Software Ver:	rk3588_spl_loader_v1.01.102_1cs.bin	TESTER:	测试工位	TEST DATA:	2021.11.26-12.6	
Measurement Point								
Power	Clock	Address Signal		Write DQS	Write DQ		Read DQS	Read DQ
Type	Frequency (MHz)	Supply(v)	Vref	Test Tool		Probe		
LPDDR4-4266	2112	1.1		KEYSIGHT DSA91304A		KEYSIGHT 1169A(12Ghz)		
Test name	Signal Name	Description	Test item	Unit	Spec limited		Measure	Test Result
CLK/CLK# Test (SDRAM die near-end)	CLK/CLK#	CK differential input voltage	Vindiff_CK	mV	360	--	1005	Pass
		Differential Input Cross Point Voltage relative to VDD/2 for CK_t-CK_c	VDX(CK)	mv	-120	120	-50	Pass
		Single-ended Maximum amplitude for CK_t-CK_c	Vmax	V	--	1.4	0.452	Pass
		Single-ended Minimum amplitude for CK_t-CK_c	Vmin	V	-0.3	--	-0.041	Pass
		Average Clock Period	tCK(avg)	ns	0.469	100	0.473278	Pass
		Absolute Clock Period	tCK(abs)	ns	0.439	--	0.484	Pass
		Absolute High Pulse Width	tCH(abs)	ns	0.20167	0.26733	0.228	Pass
		Absolute Low Pulse Width	tCL(abs)	ns	0.20167	0.26733	0.23	Pass
		Clock Period Jitter	tJIT(per)	ps	-30	30	-11	Pass
		Cycle-to-Cycle Period Jitter	tJIT(cc)	ps	--	60	15	Pass
Address, Command Test (SDRAM die near-end)	ADDRESSn	Maximum amplitude for Address, Command	Vmax	V	--	1.4	0.573	Pass
		Minimum amplitude for Address, Command	Vmin	V	-0.3	--	-0.132	Pass
		Rx timing window total	TCIVW_total	ps	--	142.0454545	410	Pass
		Rx Mask voltage - p-p total	VCIVW_total	mV	--	145	--	Pass
		CA input pulse width	TCIPW	ps	284.0909091	--	435	Pass
		CA AC input swing pk-pk	VIHL_AC	mV	180	--	742	Pass

## 04.LPDDR4



Write Test (SDRAM die near-end)	DQSn/DQSn#	DQS differential input voltage	Vindiff_DQS	mV	340		—	554	600	Pass	<a href="#">Vindiff_DQS_W</a>	
		Max amplitude for DQS_t, DQS_c , TDQS_t, TDQS_c	Vmax	V	--		1.4	0.315	0.349	Pass	<a href="#">Vmax_DQS_W</a>	
		Minimum amplitude for DQS_t, DQS_c , TDQS_t, TDQS_c	Vmin	V	-0.3		—	-0.024	0.012	Pass	<a href="#">Vmin_DQS_W</a>	
		DQS latching transition to associated clock edge	tDQSS	ps	355.1136364		591.8560606	430	466	Pass	<a href="#">tDQSS</a>	
		DQS input high pulse width	tDQSH	ps	189.3939394					Null	<a href="#">tDQSH</a>	
		DQS input low pulse width	tDQLS	ps	189.3939394					Null	<a href="#">tDQLS</a>	
		DQS falling edge to CK setup time	tDSS	ps	94.6969697		—	251		Pass	<a href="#">tDSS</a>	
		DQS falling edge hold time from CK	tDSH	ps	94.6969697		—	200		Pass	<a href="#">tDSH</a>	
	DQn /DMn/DBI	Maximum amplitude	Vmax	V	--		1.4	0.339	-0.004	Pass	<a href="#">Vmax_DQ_W</a>	
		Minimum amplitude	Vmin	V	-0.3		—	-0.073	0.008	Pass	<a href="#">Vmin_DQ_W</a>	
		Rx timing window total	TdIVW_total	ps			59.18560606			pass	<a href="#">TdIVW_total_W</a>	<a href="#">测量示意图四</a>
		Rx Mask voltage - p-p total	VdIVW_total	mV			120			pass	<a href="#">VdIVW_total_W</a>	<a href="#">测量示意图四</a>
		DQ input pulse width	TdIPW	ps	106.5340909		—	195		Pass	<a href="#">TdIPW_W</a>	<a href="#">测量示意图五</a>
		DQ AC input swing pk-pk	VIHL_AC	mV	170		—	473		Pass	<a href="#">VIHL_AC_W</a>	<a href="#">测量示意图六</a>
Read Test (CPU die near-end)	DQSn/DQSn#	DQS differential input voltage	Vindiff_DQS	mV	340		—	680	779	Pass	<a href="#">Vindiff_DQS_R</a>	
		Maximum amplitude for DQS_t, DQS_c , TDQS_t, TDQS_c	Vmax	V	--		1.4		0.393	Pass	<a href="#">Vmax_DQS_R</a>	
		Minimum amplitude for DQS_t, DQS_c , TDQS_t, TDQS_c	Vmin	V	-0.3		—	-0.052		Pass	<a href="#">Vmin_DQS_R</a>	
		DQS Rise to DQ read High level time	tDQSQ-R-H	ps	--		42.61363636		35	Pass	<a href="#">tDQSQ-R-H</a>	
	DQn /DMn	DQS Rise to DQ read Low level time	tDQSQ-R-L	ps	--		42.61363636		27	Pass	<a href="#">tDQSQ-R-L</a>	
		DQS Fall to DQ read High level time	tDQSQ-F-H	ps	--		42.61363636		25	Pass	<a href="#">tDQSQ-F-H</a>	
		DQS Fall to DQ read Low level time	tDQSQ-F-L	ps	--		42.61363636		28	Pass	<a href="#">tDQSQ-F-L</a>	
		Rx Mask voltage - p-p total	VdIVW_total	mV	--		120			Pass	<a href="#">VdIVW_total_R</a>	<a href="#">测量示意图四</a>
		DQ input pulse width	TdIPW	ps	106.5340909		—	167		Pass	<a href="#">TdIPW_R</a>	<a href="#">测量示意图五</a>
		DQ AC input swing pk-pk	VIHL_AC	mV	170		—	521		Pass	<a href="#">VIHL_AC_R</a>	<a href="#">测量示意图六</a>

## 04.LPDDR4



VDDQ (CPU die near-end) (SDRAM die near-end)	VDDQ	I/O buffer power	VDDQ	V	1.06	1.1	1.17			Null	<a href="#">VDDQ</a>	
VDD2	VDD2	Core 2 power	VDD2	V	1.06	1.1	1.17			Null	<a href="#">VDD2</a>	
VDD1 (CPU die near-end) (SDRAM die near-end)	VDD1	Core 1 power	VDD1	V	1.7	1.8	1.95			Null	<a href="#">VDD1</a>	

# 05.LPDDR5



LPDDR5 Test Report(除了眼图，其他测试项见自动化测试报告)										
Power		Clock	Address Signal	Control Signal	Write DQ\$	Write DQ	Read DQ\$	Read DQ	Measurement Point	
Type	Frequency (MHz)	Supply(V)	CA Vref	CS Vref	DQ Write Vref	DQ Read Vref	Test Tool			Probe
LPDDR5-5500	687.5	0.5	182.5mv	304mv	127mv	130mv	KEYSIGHT DSA81304A		KEYSIGHT 1169A(12GHz)	
Test name	Signal Name	Description	Test item	Unit	Spec limited	Measure	Test Result	Waveform	Remark	
CS Test (SDRAM die near-end)	CSn (SDR模式)	CS Rx mask width at VrefCS	tCSIVW1	ps	436.363636	--		PASS	tCSIVW1	测量示意图一
		CS Rx mask width at vCSIVW	tCSIVW2	ps	320	--		PASS	tCSIVW2	测量示意图一
		CS Rx mask height	vCSIVW	mV	180	--		PASS	vCSIVW	测量示意图一
		CS Rx pulse width	tCSIPW	ps	872.727273	--	1388.9	Pass	tCSIPW	测量示意图一
		CS Rx pulse amplitude	vCSIHL_AC	mV	240	--	360.23	Pass	vCSIHL_AC	测量示意图一
Address, CommandTest (SDRAM die near-end)	ADDRESSn (DDR模式)	CA Rx mask width at Vref	tCIVW1	ps	218.181818	--		PASS	tCIVW1	测量示意图二、三
		CA Rx mask width at vCIVW	tCIVW2	ps	130.909091	--		PASS	tCIVW2	测量示意图二、三
		CA Rx mask height	vCIVW	mV	155	--		PASS	vCIVW	测量示意图二、三
		CA Rx pulse width	tCIPW	ps	436.363636	--	675.8	Pass	tCIPW	测量示意图二、三
		CA Rx pulse amplitude	vCIHL_AC	mV	190	--	289.66	Pass	vCIHL_AC	测量示意图二、三
DQ Write Test (DRAM die near-end)	DQn / DMn	DQ Rx mask width at TBD	tDIVW1	ps	63.6363636	--		PASS	tDIVW1	测量示意图四、五
		DQ Rx mask width at vDIVW	tDIVW2	ps	32.7272727	--		PASS	tDIVW2	测量示意图四、五
		DQ Rx mask height	vDIVW	mV	100	--		PASS	vDIVW	测量示意图四、五
		DQ Rx pulse width	tDIPW	ps	81.8181818	--	144.47	Pass	tDIPW	测量示意图四、五
		DQ Rx pulse width above / below vDIVW	tDIHL	ps	45.4545455	--		PASS	tDIHL	测量示意图四、五
		DQ Rx pulse amplitude	vDIHL_AC	mV	140	--	198.33	Pass	vDIHL_AC	测量示意图四、五
DQ Read Test (CPU die near-end)	DQn / DMn	DQ Rx mask width at TBD	tDIVW1_R	ps	63.6363636	--		PASS	tDIVW1_R	测量示意图四、五
		DQ Rx mask width at vDIVW	tDIVW2_R	ps	32.7272727	--		PASS	tDIVW2_R	测量示意图四、五
		DQ Rx mask height	vDIVW_R	mV	100	--		PASS	vDIVW_R	测量示意图四、五
		DQ Rx pulse width	tDIPW_R	ps	81.8181818	--	139.97	Pass	tDIPW_R	测量示意图四、五
		DQ Rx pulse width above / below vDIVW	tDIHL_R	ps	45.4545455	--		PASS	tDIHL_R	测量示意图四、五
		DQ Rx pulse amplitude	vDIHL_AC_R	mV	140	--	179.59	Pass	vDIHL_AC_R	测量示意图四、五

# 06.EMMC



eMMC SI Test Report												
CLK Frequency (MHz)		IO Power Supply(V)		NOTE: 1.All timing values are measured relative to 50% of voltage level. 2.Rise and fall times are measured of voltage level(Please see below VOHmin、VOLmax、VIHmin、VILmax of the test table.) 建议先测试填写电源部分,为后面信号测试提供高低电平的参考。 3.测试结果根据指标要求,如果指标是大于等于Min值,则测试结果记录最小值。如果指标是小于等于Max值,则测试结果记录最大值。如果指标是大于等于Min值,同时小于等于Max值,则测试结果记录最小值和最大值。								
Signal Name	Parameter	Test Item	Descriprion	Spec limited			Unit	Measure		Test Result	Test Waveform	Remark
				Min	Typical	Max		Min	Max			
High-speed dual rate interface timing (referenced to CLK-DDR mode)	Clock	tPERIOD	CLK period	5			ns	5.05		Pass	tPERIOD	
		-	-	-			-	-		Null	-	
		CKSR	Slew rate	1.125			V/ns	1.629		Pass	CKSR	
		-	-	-			-	-		Null	-	
	Data Input	tCKDDC	Duty cycle distortion	0		0.3	ns	0.09	0.11	Pass	tCKDDC	
		tCKMPW	Minimum pulse width	2.2				2.35		Pass	tCKMPW	
		tISUddr	Data Input setup time	0.4			ns	0.904		Pass	tISUddr	
	Data Output	tIHddr	Data Input hold time	0.4			ns	0.854		Pass	tIHddr	
		DSR_IN	Data Input Slew Rate	1.125				1.773		Pass	DSR_IN	
		tRQ-DAT	Output skew	-		0.4	ns	-	0.285	Pass	tRQ-DAT	
		tRQH-DAT	Data Output hold skew	-		0.4	ns	-	0.358	Pass	tRQH-DAT	
High-speed dual rate interface timing (referenced to CLK-SDR mode)	CMD Input	DSR_OUT	Data Output Slew Rate	1.125			V/ns	2.08		Pass	DSR_OUT	
		-	-	-			-	-		Null	-	
	CMD Output	tISU-CMD	Input setup time	1.4			ns	2.5		Pass	tISU-CMD	
		tIH-CMD	Input Hold time	0.8				2.23		Pass	tIH-CMD	
		tRQ-CMD	Output skew	-		0.4	ns	-	0.236	Pass	tRQ-CMD	
High-speed dual rate interface timing (referenced to CLK-DDR mode)	DS	tRQH-CMD	Output hold skew	-		0.4	ns	-	0.236	Pass	tRQH-CMD	
		CMDSR-OUT	CMD Output Slew rate	1.125				2.419		Pass	CMDSR-OUT	
		-	-	-			-	-		Null	-	
		tPERIOD_DS	Data Strobe Cycle time	5			ns	5.05		Pass	tPERIOD_DS	
	DSSR	Data Strobe Slew Rate	1.125			V/ns	1.525		Pass	DSSR		
voltage	DC/AC	tDSDCD	Data Strobe Duty Cycle Distortion Time	0		0.2	ns	0.115	0.14	Pass	tDSDCD	
		tDSMPW	Data Strobe Minimum Pulse Width Time	2				2.17		Pass	tDSMPW	
		Vcc	Supply voltage (eMMC)	1.7		1.95	V	1.8	1.8	Pass	Vcc	
		tPRUL	Supply power-up Time for 1.8V	-		25	ms	-	0.493	Pass	tPRUL	
		VIHCLK	Input HIGH voltage	-		2.1	V	-	2.322	Fail	VIHCLK	
		VILCLK	Input LOW voltage	-0.3				-	-0.406	Fail	VILCLK	
		VIHData	Input HIGH voltage	1.17		2.1		-	1.768	Fail	VIHData	
		VILDData	Input LOW voltage	-0.3		0.63		-	0.031	0.107	Pass	VILDData

注意：信号有轻微上下冲，不影响EMMC的实际运行稳定性，风险可控。

eMMC SI Test Report															
CLK Frequency (MHz)			IO Power Supply(V)		NOTE:										
HS200			1.7-1.95		1.All timing values are measured relative to 50% of voltage level. 2.Rise and fall times are measured of voltage level(Please see below VOHmin、VOLmax、VIHmin、VILmax of the test table.) 建议先测试填写电源部分,为后面信号测试提供高低电平的参考。 3.测试结果根据指标要求。如果指标是大于等于Min值,则测试结果记录最小值。如果指标是小于等于Max值,则测试结果记录最大值。如果指标是大于等于Min值,同时小于等于Max值,则测试结果记录最小值和最大值。										
Signal Name	Parameter	Test Item	Descriprion			Spec limited		Unit	Measure		Test Result	Test Waveform	Remark		
HS200 Clock signal timing						Min	Typical	Max	Min	Max					
			tPERIOD			5		ns	5.05		Pass	tPERIOD			
			Duty Cycle			30		%	48.3	50.9	Pass	Duty Cycle			
			-			-		-	Null	Null	-	-			
			-			-		-	Null	Null	-	-			
			tTLH			Clock rise time			1.01		0.41	Pass	tTLH		
			tTHL			Clock fall time			1.01		0.419	Pass	tTHL		
			tiSU			Data Input setup time			1.4		2.35	Pass	tiSU		
			tiH			Data Input hold time			0.8		2.21	Pass	tiH		
			-			-			-	Null	Null	-	-		
-			tPH			Device output momentary phasw from CLK input to CMD or DATA lines output			10.1		ns	1.54	Pass	tPH	
			tVW			tWH=2.88ns at 200MHz			2.90375		ns	3.63	Pass	tVW	
			-			-			-	Null	Null	-	-		
			-			-			-	Null	Null	-	-		
			-			-			-	Null	Null	-	-		
-			tiSU-CMD			Input setup time			1.4		ns	2.46	Pass	tiSU-CMD	
			tiH-CMD			Input Hold time			0.8		ns	2.29	Pass	tiH-CMD	
			tPH			Device output momentary phasw from CLK input to CMD or DATA lines output			-		ns	1.3	Pass	tPH	
			tVW			tWH=2.88ns at 200MHz			2.90375		ns	3.85	Pass	tVW	
			-			-			-	Null	Null	-	-		
-			-			-			-	Null	Null	-	-		
			-			-			-	Null	Null	-	-		
			-			-			-	Null	Null	-	-		
			-			-			-	Null	Null	-	-		
			-			-			-	Null	Null	-	-		
voltage			Vcc			Supply voltage (eMMC)			1.7	1.95	V	1.8	1.8	Pass	Vcc
			tPRUL			Supply power-up Time for 1.8V			-	25	ms		0.493	Pass	tPRUL
			VIHCLK			Input HIGH voltage			-	2.1			1.926	Pass	VIHCLK
			VILCLK			Input LOW voltage			-0.3				-0.111	Pass	VILCLK
			VIHData			Input HIGH voltage			1.17	2.1	V	1.789	1.952	Pass	VIHData
			VILDData			Input LOW voltage			-0.3	0.63	V	0.05	0.117	Pass	VILDData

# 07.PCIE3.0



## PCIE30x4 GEN1测试综述



### Test Report

Overall Result **PASS**

Test Configuration Details	
Application	
Name	D8040PCIE PCI Express
Version	4.70.10.0
Test Session Details	
Infinium SW Version	08.70.00001
Infinium Model Number	DSOv254A
Infinium Serial Number	MY 61380102
Debug Mode Used	No
Last Test Date	2021-11-16 11:04:25 UTC +08:00

#### Summary of Results

Test Statistics		
Failed	0	
Passed	8	
Total	8	

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	RootComplex Tests, Unit Interval (2.5 GT/s)	400.00300 ps	48.8 %	399.88000 ps <= VALUE <= 400.12000 ps
✓	0	1	RootComplex Tests, Template Tests (2.5 GT/s)	Pass	100.0 %	VALUE = 0.000
✓	0	1	RootComplex Tests, Median to Max Jitter (2.5 GT/s)	19.43 ps	74.8 %	VALUE <= 77.00 ps
✓	0	1	RootComplex Tests, Eye-Width (2.5 GT/s)	373.03 ps	51.6 %	VALUE >= 246.00 ps
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Transition) (2.5 GT/s)	867.7 mV	36.9 %	274.0 mV <= VALUE <= 1.2000 V
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Non Transition) (2.5 GT/s)	812.4 mV	40.9 %	253.0 mV <= VALUE <= 1.2000 V

# 07.PCIE3.0



## PCIE30x4 GEN2测试综述

KEYSIGHT TECHNOLOGIES

### Test Report

Overall Result: PASS

Test Configuration Details	
Application	
Name:	D9040PCIe PCI Express
Version:	4.70.10.0
Test Session Details	
Infinium SW Version:	06.70.00001
Infinium Model Number:	DSO/254A
Infinium Serial Number:	MY61380102
Debug Mode Used:	No
Last Test Date:	2021-11-16 11:13:09 UTC +08:00

#### Summary of Results

Test Statistics:

Failed	0
Passed	12
Total	12

Margin Thresholds:

Warning	< 5 %
Critical	< 0 %

Test Results:

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	RootComplex_Tests_Unit Interval (5.0 GT/s)	200.0200 ps	48.3 %	199.94000 ps <= VALUE <= 200.08000 ps
✓	0	1	RootComplex_Tests_Template Tests (5.0 GT/s)	Pass	100.0 %	VALUE = 0.000
✓	0	1	RootComplex_Tests_Peak Differential Output Voltage (Transition) (5.0 GT/s)	663.4 mV	46.0 %	225.0 mV <= VALUE <= 1,200.0 V
✓	0	1	RootComplex_Tests_Peak Differential Output Voltage (Non Transition) (5.0 GT/s)	577.1 mV	36.1 %	225.0 mV <= VALUE <= 1,200.0 V
✓	0	1	RootComplex_Tests_Eye-Width with crosstalk (5.0 GT/s)	163.23 ps	71.8 %	VALUE >= 95.00 ps
✓	0	1	RootComplex_Tests_RMS Random Jitter with crosstalk (5.0 GT/s)	2.136 ps	37.4 %	VALUE <= 3.410 ps
✓	0	1	RootComplex_Tests_Maximum Deterministic Jitter with crosstalk (5.0 GT/s)	6.740 ps	88.2 %	VALUE <= 57.000 ps
✓	0	1	RootComplex_Tests_Total Jitter at BER-12 with crosstalk (5.0 GT/s)	36.768 ps	66.0 %	VALUE <= 105.000 ps
✓	0	1	RootComplex_Tests_Eye-Width without crosstalk (5.0 GT/s)	162.99 ps	50.8 %	VALUE >= 108.00 ps
✓	0	1	RootComplex_Tests_RMS Random Jitter without crosstalk (5.0 GT/s)	2.113 ps	38.0 %	VALUE <= 3.410 ps
✓	0	1	RootComplex_Tests_Maximum Deterministic Jitter without crosstalk (5.0 GT/s)	7.307 ps	83.4 %	VALUE <= 44.000 ps
✓	0	1	RootComplex_Tests_Total Jitter at BER-12 without crosstalk (5.0 GT/s)	37.012 ps	50.8 %	VALUE <= 92.000 ps

# 07.PCIE3.0



## PCIE30x4 GEN3测试综述



### Test Report

Overall Result **PASS**

Test Configuration Details	
Application	
Name	D9040PCIC PCI Express
Version	4.70.10.0
Test Session Details	
Infinium SW Version	08.70.00001
Infinium Model Number	DSO/254A
Infinium Serial Number	MY 81380102
Debug Mode Used	No
Last Test Date	2021-11-16 11:31:58 UTC +08:00

#### Summary of Results

Test Statistics	
Failed	0
Passed	5
Total	5

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	RootComplex Tests, Unit Interval (8.0 GT/s)	125.00400 ps	45.0 %	124.98000 ps <= VALUE <= 125.04000 ps
✓	0	1	RootComplex Tests, Template Tests (8.0 GT/s)	Pass	100.0 %	VALUE = 0.000
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Transition) (8.0 GT/s)	324.5 mV	24.9 %	34.0 mV <= VALUE <= 1.2000 V
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Non Transition) (8.0 GT/s)	329.8 mV	25.4 %	34.0 mV <= VALUE <= 1.2000 V
✓	0	1	RootComplex Tests, Eye-Width (8.0 GT/s)	98.17 ps	133.1 %	VALUE >= 41.25 ps

# 08.PCIE2.0



## RK3588\_PCIE2.0\_DATA\_5G



### Test Report

Overall Result: **PASS**

Test Configuration Details	
Application	
Name	D9040PCIC PCI Express
Test Session Details	
Version	4.70.10.0
Infinium SW Version	08.60.00601
Infinium Model Number	DSC91304A
Infinium Serial Number	MY52260147
Debug Mode Used	No
Last Test Date	2022-03-05 11:33:23 UTC +08:00

#### Summary of Results

Test Statistics		
Failed	0	
Passed	12	
Total	12	

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass #	Failed #	Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	RootComplex Tests, Unit Interval (5.0 GT/s)	200.00500 ps	45.8 %	199.94000 ps <= VALUE <= 200.06000 ps
✓	0	1	RootComplex Tests, Template Tests (5.0 GT/s)	Pass	100.0 %	VALUE = 0.000
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Transition)(5.0 GT/s)	638.0 mV	37.6 %	300.0 mV <= VALUE <= 1.2000 V
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Non Transition)(5.0 GT/s)	598.1 mV	32.9 %	300.0 mV <= VALUE <= 1.2000 V
✓	0	1	RootComplex Tests, Eye-Width with crosstalk (5.0 GT/s)	150.45 ps	58.4 %	VALUE >= 95.00 ps
ⓘ	0	1	RootComplex Tests, RMS Random Jitter with crosstalk (5.0 GT/s)	2.175 ps		Information Only
✓	0	1	RootComplex Tests, Maximum Deterministic Jitter with crosstalk (5.0 GT/s)	18.983 ps	66.7 %	VALUE <= 57.000 ps
✓	0	1	RootComplex Tests, Total Jitter at BER-12 with crosstalk (5.0 GT/s)	49.545 ps	52.8 %	VALUE <= 105.000 ps
✓	0	1	RootComplex Tests, Eye-Width without crosstalk (5.0 GT/s)	150.80 ps	39.4 %	VALUE >= 108.00 ps
ⓘ	0	1	RootComplex Tests, RMS Random Jitter without crosstalk (5.0 GT/s)	2.161 ps		Information Only
✓	0	1	RootComplex Tests, Maximum Deterministic Jitter without crosstalk (5.0 GT/s)	19.014 ps	56.8 %	VALUE <= 44.000 ps
✓	0	1	RootComplex Tests, Total Jitter at BER-12 without crosstalk (5.0 GT/s)	49.398 ps	46.3 %	VALUE <= 92.000 ps

# 08.PCIE2.0



## RK3588\_PCIE2.0\_CLK\_5G



### Test Report

Overall Result: **PASS**

Test Configuration Details	
Application	
Name	D9040PCIC PCI Express
Version	4.70.10.0
Test Session Details	
Infinium SW Version	06.60.00601
Infinium Model Number	DSO91304A
Infinium Serial Number	MY52280147
Debug Mode Used	No
Last Test Date	2022-03-05 11:24:00 UTC +08:00

#### Summary of Results

Test Statistics		
Failed	0	
Passed	4	
Total	4	

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	Reference Clock, High frequency > 1.5MHz RMS Jitter (Common Clk) (5.0 GT/s)	2.76 ps	11.0 %	VALUE <= 3.10 ps
✓	0	1	Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Common Clk) (5.0 GT/s)	010 fs	69.7 %	VALUE <= 3.00 ps
✓	0	1	Reference Clock, High frequency > 1.5MHz RMS Jitter (Data Clk) (5.0 GT/s)	3.44 ps	14.0 %	VALUE <= 4.00 ps
✓	0	1	Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Data Clk) (5.0 GT/s)	1.15 ps	84.7 %	VALUE <= 7.50 ps

# 09.SATA3.0



## RK3588\_SATA\_6G

### Summary of Results

Test Statistics	
Failed	0
Passed	25
Total	25

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass #	Failed #	Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	PHY-01 : Channel Speed, FBaud & Unit Interval (Gen3)	166.9697 ps	38.0 %	166.6083 ps <= VALUE <= 167.5583 ps
✓	0	1	PHY-03 : Spread-Spectrum Modulation Frequency	31.105 kHz	36.8 %	30.000 kHz <= VALUE <= 33.000 kHz
✓	0	1	PHY-04(a) : Spread-Spectrum Modulation Deviation (Min)	-4.149 kppm of Fbaud	21.1 %	-5.350 kppm of Fbaud <= VALUE <= 350 ppm of Fbaud
✓	0	1	PHY-04(b) : Spread-Spectrum Modulation Deviation (Max)	94 ppm of Fbaud	4.5 %	-5.350 kppm of Fbaud <= VALUE <= 350 ppm of Fbaud
✓	0	1	PHY-04(c) : Spread-Spectrum Modulation DFDT (Min) (Informative)	-880 ppm/us	14.8 %	-1.250 kppm/us <= VALUE <= 1.250 kppm/us
✓	0	1	PHY-04(d) : Spread-Spectrum Modulation DFDT (Max) (Informative)	922 ppm/us	13.1 %	-1.250 kppm/us <= VALUE <= 1.250 kppm/us
✓	0	1	TSG-02(a) : Rise Time (Gen3) (Informative)	68.67 ps	24.1 %	33.00 ps <= VALUE <= 80.00 ps
✓	0	1	TSG-02(b) : Fall Time (Gen3) (Informative)	68.73 ps	24.0 %	33.00 ps <= VALUE <= 80.00 ps
✓	0	1	TSG-03(a) : Differential Skew, HFTP (Gen1, Gen2, Gen3) (Informative)	2.00 ps	85.5 %	VALUE <= 20.00 ps
✓	0	1	TSG-03(b) : Differential Skew, MFTP (Gen1, Gen2, Gen3) (Informative)	2.06 ps	89.7 %	VALUE <= 20.00 ps
✓	0	1	TSG-04(a) : AC Common Mode Voltage, MFTP (Gen3)	8.83 mV	92.6 %	VALUE <= 120.00 mV
✓	0	1	TSG-04(b) : AC Common Mode Voltage, HFTP (Gen3)	12.71 mV	89.4 %	VALUE <= 120.00 mV
✓	0	1	TSG-13(d) : TJ after CIC, LBP, Clock To Data, JTF Defined (BER=1E-12) (Gen3)	335.90 mUI	35.4 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13(e) : TJ after CIC, LBP, Clock To Data, JTF Defined (BER=1E-8) (Gen3)	260.80 mUI	43.3 %	VALUE <= 460.00 mUI
✓	0	1	TSG-13(d) : TJ after CIC, HFTP, Clock To Data, JTF Defined (BER=1E-12) (Gen3) (Informative)	217.80 mUI	58.2 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13(e) : TJ after CIC, HFTP, Clock To Data, JTF Defined (BER=1E-8) (Gen3) (Informative)	160.20 mUI	65.2 %	VALUE <= 460.00 mUI
✓	0	1	TSG-13(d) : TJ after CIC, MFTP, Clock To Data, JTF Defined (BER=1E-12) (Gen3) (Informative)	213.30 mUI	59.0 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13(e) : TJ after CIC, MFTP, Clock To Data, JTF Defined (BER=1E-8) (Gen3) (Informative)	152.20 mUI	68.9 %	VALUE <= 460.00 mUI
✓	0	1	TSG-13(d) : TJ after CIC, LFTP, Clock To Data, JTF Defined (BER=1E-12) (Gen3) (Informative)	221.30 mUI	57.4 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13(e) : TJ after CIC, LFTP, Clock To Data, JTF Defined (BER=1E-8) (Gen3) (Informative)	162.40 mUI	64.7 %	VALUE <= 460.00 mUI
✓	0	1	TSG-13(d) : TJ after CIC, SSOP, Clock To Data, JTF Defined (BER=1E-12) (Gen3) (Informative)	333.20 mUI	35.9 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13(e) : TJ after CIC, SSOP, Clock To Data, JTF Defined (BER=1E-8) (Gen3) (Informative)	259.80 mUI	43.5 %	VALUE <= 460.00 mUI
✓	0	1	TSG-14 : TX Maximum Differential Voltage Amplitude (Gen3)	684.00 mV	24.0 %	VALUE <= 900.00 mV
✓	0	1	TSG-15 : TX Minimum Differential Voltage Amplitude (UI=5E8) (Gen3)	302.70 mV	51.4 %	VALUE >= Vdiff_Min_Gen3i_Limit V
✓	0	1	TSG-17(b) : Tx Emphasis, MFTP (Host) (Gen3)	-1.667 dB	9.5 %	-2.000 dB <= VALUE <= 1.500 dB

# 09.SATA3.0



## RK3588\_SATA\_6G

### Summary of Results

Test Statistics		
Failed	0	
Passed	21	
Total	21	

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	PHY-01 : Channel Speed, FBaud & Unit Interval (Gen3)	166.6712 ps	6.6 %	166.6083 ps <= VALUE <= 167.5583 ps
✓	0	1	PHY-02 : Frequency Long-Term Stability / Accuracy (Gen3)	-27 ppm	46.1 %	-350 ppm <= VALUE <= 350 ppm
✓	0	1	TSG-02[a] : Rise Time (Gen3) (Informative)	65.39 ps	31.1 %	33.00 ps <= VALUE <= 80.00 ps
✓	0	1	TSG-02[b] : Fall Time (Gen3) (Informative)	85.73 ps	30.4 %	33.00 ps <= VALUE <= 80.00 ps
✓	0	1	TSG-03[a] : Differential Skew, HFTP (Gen1, Gen2, Gen3) (Informative)	5.85 ps	70.8 %	VALUE <= 20.00 ps
✓	0	1	TSG-03[b] : Differential Skew, MFTP (Gen1, Gen2, Gen3) (Informative)	8.05 ps	69.8 %	VALUE <= 20.00 ps
✓	0	1	TSG-04[a] : AC Common Mode Voltage, MFTP (Gen3)	17.54 mV	85.4 %	VALUE <= 120.00 mV
✓	0	1	TSG-04[b] : AC Common Mode Voltage, HFTP (Gen3)	24.49 mV	79.6 %	VALUE <= 120.00 mV
✓	0	1	TSG-13[d] : TJ after CIC, LBP, Clock To Data, JTF Defined (BER=1E-12) (Gen3)	327.80 mUI	37.0 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13[e] : TJ after CIC, LBP, Clock To Data, JTF Defined (BER=1E-8) (Gen3)	272.40 mUI	40.8 %	VALUE <= 480.00 mUI
✓	0	1	TSG-13[d] : TJ after CIC, HFTP, Clock To Data, JTF Defined (BER=1E-12) (Gen3) (Informative)	198.70 mUI	61.8 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13[e] : TJ after CIC, HFTP, Clock To Data, JTF Defined (BER=1E-8) (Gen3) (Informative)	128.00 mUI	72.0 %	VALUE <= 480.00 mUI
✓	0	1	TSG-13[d] : TJ after CIC, MFTP, Clock To Data, JTF Defined (BER=1E-12) (Gen3) (Informative)	204.80 mUI	60.7 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13[e] : TJ after CIC, MFTP, Clock To Data, JTF Defined (BER=1E-8) (Gen3) (Informative)	141.20 mUI	69.3 %	VALUE <= 480.00 mUI
✓	0	1	TSG-13[d] : TJ after CIC, LFTP, Clock To Data, JTF Defined (BER=1E-12) (Gen3) (Informative)	207.00 mUI	60.2 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13[e] : TJ after CIC, LFTP, Clock To Data, JTF Defined (BER=1E-8) (Gen3) (Informative)	142.90 mUI	68.9 %	VALUE <= 480.00 mUI
✓	0	1	TSG-13[d] : TJ after CIC, SSOP, Clock To Data, JTF Defined (BER=1E-12) (Gen3) (Informative)	317.10 mUI	39.0 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13[e] : TJ after CIC, SSOP, Clock To Data, JTF Defined (BER=1E-8) (Gen3) (Informative)	270.00 mUI	41.3 %	VALUE <= 480.00 mUI
✓	0	1	TSG-14 : TX Maximum Differential Voltage Amplitude (Gen3)	753.70 mV	16.3 %	VALUE <= 900.00 mV
✓	0	1	TSG-15 : TX Minimum Differential Voltage Amplitude (UI=5E6) (Gen3)	312.10 mV	56.1 %	VALUE >= Vdiff_Min_Gen3i_Limit V
✓	0	1	TSG-17[b] : Tx Emphasis, MFTP (Host) (Gen3)	-1.497 dB	14.4 %	-2.000 dB <= VALUE <= 1.500 dB

# 10.HDMI TX



hdmi1.4\_1920x1080x60Hz

## Summary of Results

Test Statistics	
Failed	0
Passed	32
Total	32

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	7-9: Clock Jitter	36 mTbit	85.6 %	VALUE <= 250 mTbit
✓	0	1	7-4: Clock Rise Time	110.881 ps	47.8 %	VALUE >= 75.000 ps
✓	0	1	7-4: Clock Fall Time	109.416 ps	45.9 %	VALUE >= 75.000 ps
✓	0	1	7-8: Clock Duty Cycle(Minimum)	49.954	24.9 %	>=40%
✓	0	1	7-8: Clock Duty Cycle(Maximum)	50.082	16.5 %	<=60%
✓	0	1	7-2: VL Clock +	2.813 V	29.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	1	7-2: VL Clock -	2.801 V	33.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	1	7-7: Intra-Pair Skew - Clock	2 mTbit	49.3 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	7-10: D0 Mask Test	0.000	50.0 %	No Mask Failures
✓	0	1	7-10: D0 Data Jitter	38 m	87.3 %	<=0.3Tbit
✓	0	1	7-4: D0 Rise Time	100.649 ps	34.2 %	VALUE >= 75.000 ps
✓	0	1	7-4: D0 Fall Time	101.496 ps	35.3 %	VALUE >= 75.000 ps
✓	0	1	7-2: VL D0+	2.810 V	30.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	1	7-2: VL D0-	2.811 V	29.7 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	1	7-7: Intra-Pair Skew - Data Lane 0	-4 mTbit	48.7 %	-150 mTbit <= VALUE <= 150 mTbit

## 10.HDMI TX



✓	0	1	<u>7-10: D1 Mask Test</u>	0.000	50.0 %	No Mask Failures
✓	0	1	<u>7-10: D1 Data Jitter</u>	37 m	87.7 %	<=0.3Tbit
✓	0	1	<u>7-4: D1 Rise Time</u>	92.904 ps	23.9 %	VALUE >= 75.000 ps
✓	0	1	<u>7-4: D1 Fall Time</u>	91.817 ps	22.4 %	VALUE >= 75.000 ps
✓	0	1	<u>7-2: VL D1+</u>	2.804 V	32.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	1	<u>7-2: VL D1-</u>	2.805 V	31.7 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	1	<u>7-7: Intra-Pair Skew - Data Lane 1</u>	-10 mTbit	46.7 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	<u>7-10: D2 Mask Test</u>	0.000	50.0 %	No Mask Failures
✓	0	1	<u>7-10: D2 Data Jitter</u>	36 m	88.0 %	<=0.3Tbit
✓	0	1	<u>7-4: D2 Rise Time</u>	100.412 ps	33.9 %	VALUE >= 75.000 ps
✓	0	1	<u>7-4: D2 Fall Time</u>	97.366 ps	29.8 %	VALUE >= 75.000 ps
✓	0	1	<u>7-2: VL D2+</u>	2.810 V	30.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	1	<u>7-2: VL D2-</u>	2.805 V	31.7 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	1	<u>7-7: Intra-Pair Skew - Data Lane 2</u>	-12 mTbit	46.0 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	<u>7-6: Inter-Pair Skew - D0/D2</u>	-800 纽Tpixel	49.8 %	-200 mTpixel <= VALUE <= 200 mTpixel
✓	0	1	<u>7-6: Inter-Pair Skew - D1/D2</u>	-700 纽Tpixel	49.8 %	-200 mTpixel <= VALUE <= 200 mTpixel
✓	0	1	<u>7-6: Inter-Pair Skew - D0/D1</u>	-2 mTpixel	49.5 %	-200 mTpixel <= VALUE <= 200 mTpixel

# 10.HDMI TX



hdmi2.0\_4k\_60Hz

## Summary of Results

Test Statistics	
Failed	0
Passed	32
Total	32

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Worst Actual	Worst Margin	Pass Limits
✓	0	5	7-9: Clock Jitter	81 mTbit	67.6 %	VALUE <= 250 mTbit
✓	0	5	7-4: Clock Rise Time	95.362 ps	27.1 %	VALUE >= 75.000 ps
✓	0	5	7-4: Clock Fall Time	98.641 ps	31.5 %	VALUE >= 75.000 ps
✓	0	5	7-8: Clock Duty Cycle(Minimum)	49.922	24.8 %	>=40%
✓	0	5	7-8: Clock Duty Cycle(Maximum)	50.209	16.3 %	<=60%
✓	0	5	7-2: VL_Clock_+	2.824 V	25.3 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	5	7-2: VL_Clock_-	2.819 V	27.0 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	5	7-7: Intra-Pair Skew - Clock	-28 mTbit	40.7 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	5	7-10: D2 Mask Test	0.000	50.0 %	No Mask Failures
✓	0	5	7-10: D2 Data Jitter	81 m	73.0 %	<=0.3Tbit
✓	0	5	7-4: D2 Rise Time	84.832 ps	13.1 %	VALUE >= 75.000 ps
✓	0	5	7-4: D2 Fall Time	81.923 ps	9.2 %	VALUE >= 75.000 ps

## 10. HDMI TX



✓	0	5	<u>7-2: VL D2+</u>	2.815 V	28.3 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	5	<u>7-2: VL D2-</u>	2.818 V	27.3 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	5	<u>7-7: Intra-Pair Skew - Data Lane 2</u>	-21 mTbit	43.0 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	5	<u>7-10: D0 Mask Test</u>	0.000	50.0 %	No Mask Failures
✓	0	5	<u>7-10: D0 Data Jitter</u>	83 m	72.3 %	<=0.3Tbit
✓	0	5	<u>7-4: D0 Rise Time</u>	90.687 ps	20.9 %	VALUE >= 75.000 ps
✓	0	5	<u>7-4: D0 Fall Time</u>	89.428 ps	19.2 %	VALUE >= 75.000 ps
✓	0	5	<u>7-2: VL D0+</u>	2.816 V	28.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	5	<u>7-2: VL D0-</u>	2.828 V	24.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	5	<u>7-7: Intra-Pair Skew - Data Lane 0</u>	-12 mTbit	46.0 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	5	<u>7-10: D1 Mask Test</u>	0.000	50.0 %	No Mask Failures
✓	0	5	<u>7-10: D1 Data Jitter</u>	113 m	62.3 %	<=0.3Tbit
✓	0	5	<u>7-4: D1 Rise Time</u>	87.437 ps	16.6 %	VALUE >= 75.000 ps
✓	0	5	<u>7-4: D1 Fall Time</u>	88.462 ps	17.9 %	VALUE >= 75.000 ps
✓	0	5	<u>7-2: VL D1-</u>	2.819 V	27.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	5	<u>7-7: Intra-Pair Skew - Data Lane 1</u>	-17 mTbit	44.3 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	5	<u>7-2: VL D1+</u>	2.816 V	28.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	4	<u>7-6: Inter-Pair Skew - D0/D1</u>	-3 mTpixel	49.3 %	-200 mTpixel <= VALUE <= 200 mTpixel
✓	0	4	<u>7-6: Inter-Pair Skew - D1/D2</u>	-5 mTpixel	48.8 %	-200 mTpixel <= VALUE <= 200 mTpixel
✓	0	4	<u>7-6: Inter-Pair Skew - D0/D2</u>	-4 mTpixel	49.0 %	-200 mTpixel <= VALUE <= 200 mTpixel

# 10.HDMI TX



FRL\_12G

## Summary of Results

Test Statistics	
Failed	0
Passed	81
Total	81

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
①	1	1	Save Lane D3 Waveform(TP1) (LTP8) (All lanes transmit)	0.000		Information Only
①	1	1	Save Lane D3 Waveform(TP1) (LTP8)	0.000		Information Only
①	1	1	Save Lane D3 Waveform(TP1) (LTP3)	0.000		Information Only
①	1	1	Save Lane D3 Waveform(TP1) (LTP4)	0.000		Information Only
①	1	1	Save Lane D0 Waveform(TP1) (LTP5) (All lanes transmit)	0.000		Information Only
①	1	1	Save Lane D0 Waveform(TP1) (LTP5)	0.000		Information Only

## 10.HDMI TX



(i)	1	Save Lane D0 Waveform(TP1) (LTP3)	0.000	Information Only
(i)	1	Save Lane D0 Waveform(TP1) (LTP4)	0.000	Information Only
(i)	1	Save Lane D3 and D0 Waveform	0.000	Information Only
(i)	1	Save Lane D1 Waveform(TP1) (LTP6) (All lanes transmit)	0.000	Information Only
(i)	1	Save Lane D1 Waveform(TP1) (LTP6)	0.000	Information Only
(i)	1	Save Lane D1 Waveform(TP1) (LTP3)	0.000	Information Only
(i)	1	Save Lane D1 Waveform(TP1) (LTP4)	0.000	Information Only
(i)	1	Save Lane D2 Waveform(TP1) (LTP7)	0.000	Information Only
(i)	1	Save Lane D2 Waveform(TP1) (LTP3)	0.000	Information Only
(i)	1	Save Lane D2 Waveform(TP1) (LTP4)	0.000	Information Only
(i)	1	Save Lane D1 and D2 Waveform	0.000	Information Only
(i)	1	Save Lane D2 Waveform(TP1) (LTP7) (All lanes transmit)	0.000	Information Only
(i)	1	Save Lane D0 and D1 Waveform	0.000	Information Only
✓ 0	1	HFR1-3: D3+ Rise Slew Rate	3.771 mV/ps	76.4 % VALUE <= 16.000 mV/ps
✓ 0	1	HFR1-3: D3- Rise Slew Rate	4.067 mV/ps	74.6 % VALUE <= 16.000 mV/ps
✓ 0	1	HFR1-3: D3+ Fall Slew Rate	4.129 mV/ps	74.2 % VALUE <= 16.000 mV/ps
✓ 0	1	HFR1-3: D3- Fall Slew Rate	4.207 mV/ps	73.7 % VALUE <= 16.000 mV/ps
✓ 0	1	HFR1-1: D3 DC Common Mode	3.301 V	3.5 % 2.500 V <= VALUE <= 3.330 V
✓ 0	1	HFR1-2: Vs.e Min D3+	3.085 V	5.5 % VALUE >= FRLVs.eMinLimit V
✓ 0	1	HFR1-2: Vs.e Max D3+	3.516 V	4.3 % VALUE <= FRLVs.eMaxLimit V
✓ 0	1	HFR1-2: Vs.e Min D3-	3.088 V	5.6 % VALUE >= FRLVs.eMinLimit V
✓ 0	1	HFR1-2: Vs.e Max D3-	3.518 V	4.3 % VALUE <= FRLVs.eMaxLimit V

## 10. HDMI TX



✓	0	1	HER1-5: D3 Data Rate	-23.740 ppm	46.0 %	-300.000 ppm <= VALUE <= 300.000 ppm
✓	0	1	HER1-8: D3 AC Common Mode Noise	42 mV	72.0 %	VALUE <= 150 mV
✓	0	1	HER1-6: D3 RJ Measurement Test	78 mTbit	38.7 %	1 mTbit <= VALUE <= 200 mTbit
✓	0	1	HER1-7: D3 Eye Mask Test - Category 3 Worst Cable Model (WCMB)	0.000	50.0 %	No Mask Failures
✓	0	1	HER1-7: D3 Eye Mask Test - Category 3 Short Cable Model (SCMB)	0.000	50.0 %	No Mask Failures
✓	0	1	HER1-3: D0+ Rise Slew Rate	4.017 mV/ps	74.9 %	VALUE <= 16.000 mV/ps
✓	0	1	HER1-3: D0- Rise Slew Rate	4.118 mV/ps	74.3 %	VALUE <= 16.000 mV/ps
✓	0	1	HER1-3: D0+ Fall Slew Rate	4.158 mV/ps	74.0 %	VALUE <= 16.000 mV/ps
✓	0	1	HER1-3: D0- Fall Slew Rate	4.321 mV/ps	73.0 %	VALUE <= 16.000 mV/ps
✓	0	1	HER1-1: D0 DC Common Mode	3.300 V	3.6 %	2.500 V <= VALUE <= 3.330 V
✓	0	1	HER1-2: Vs e Min D0+	3.085 V	5.5 %	VALUE >= FRLVs eMinLimit V
✓	0	1	HER1-2: Vs e Max D0+	3.518 V	4.3 %	VALUE <= FRLVs eMaxLimit V
✓	0	1	HER1-2: Vs e Min D0-	3.082 V	5.4 %	VALUE >= FRLVs eMinLimit V
✓	0	1	HER1-2: Vs e Max D0-	3.517 V	4.3 %	VALUE <= FRLVs eMaxLimit V
✓	0	1	HER1-5: D0 Data Rate	-23.968 ppm	46.0 %	-300.000 ppm <= VALUE <= 300.000 ppm
✓	0	1	HER1-8: D0 AC Common Mode Noise	52 mV	65.3 %	VALUE <= 150 mV
✓	0	1	HER1-6: D0 RJ Measurement Test	77 mTbit	38.2 %	1 mTbit <= VALUE <= 200 mTbit
✓	0	1	HER1-7: D0 Eye Mask Test - Category 3 Worst Cable Model (WCMB)	0.000	50.0 %	No Mask Failures
✓	0	1	HER1-7: D0 Eye Mask Test - Category 3 Short Cable Model (SCMB)	0.000	50.0 %	No Mask Failures
✓	0	1	HER1-3: D1+ Rise Slew Rate	3.923 mV/ps	75.5 %	VALUE <= 16.000 mV/ps
✓	0	1	HER1-3: D1- Rise Slew Rate	4.060 mV/ps	74.6 %	VALUE <= 16.000 mV/ps
✓	0	1	HER1-3: D1+ Fall Slew Rate	4.169 mV/ps	73.9 %	VALUE <= 16.000 mV/ps
✓	0	1	HER1-3: D1- Fall Slew Rate	4.260 mV/ps	73.4 %	VALUE <= 16.000 mV/ps
✓	0	1	HER1-1: D1 DC Common Mode	3.300 V	3.6 %	2.500 V <= VALUE <= 3.330 V
✓	0	1	HER1-2: Vs e Min D1+	3.091 V	5.7 %	VALUE >= FRLVs eMinLimit V
✓	0	1	HER1-2: Vs e Max D1+	3.516 V	4.3 %	VALUE <= FRLVs eMaxLimit V
✓	0	1	HER1-2: Vs e Min D1-	3.080 V	5.3 %	VALUE >= FRLVs eMinLimit V
✓	0	1	HER1-2: Vs e Max D1-	3.524 V	4.1 %	VALUE <= FRLVs eMaxLimit V

## 10.HDMI TX



✓	0	1	HFR1-5: D1 Data Rate	-24.403 ppm	45.9 %	-300.000 ppm <= VALUE <= 300.000 ppm
✓	0	1	HFR1-8: D1 AC Common Mode Noise	35 mV	76.7 %	VALUE <= 150 mV
✓	0	1	HFR1-6: D1 RJ Measurement Test	78 mTbit	38.7 %	1 mTbit <= VALUE <= 200 mTbit
✓	0	1	HFR1-7: D1 Eye Mask Test - Category 3 Worst Cable Model (WCM3)	0.000	50.0 %	No Mask Failures
✓	0	1	HFR1-7: D1 Eye Mask Test - Category 3 Short Cable Model (SCMB)	0.000	50.0 %	No Mask Failures
✓	0	1	HFR1-3: D2+ Rise Slew Rate	4.221 mV/ps	73.6 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-3: D2- Rise Slew Rate	4.127 mV/ps	74.2 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-3: D2+ Fall Slew Rate	4.408 mV/ps	72.5 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-3: D2- Fall Slew Rate	4.408 mV/ps	72.5 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-1: D2 DC Common Mode	3.300 V	3.6 %	2.500 V <= VALUE <= 3.330 V
✓	0	1	HFR1-2: Vs.e Min D2+	3.083 V	5.4 %	VALUE >= FRLVs.eMinLimit V
✓	0	1	HFR1-2: Vs.e Max D2+	3.515 V	4.4 %	VALUE <= FRLVs.eMaxLimit V
✓	0	1	HFR1-2: Vs.e Min D2-	3.082 V	5.4 %	VALUE >= FRLVs.eMinLimit V
✓	0	1	HFR1-2: Vs.e Max D2-	3.519 V	4.2 %	VALUE <= FRLVs.eMaxLimit V
✓	0	1	HFR1-5: D2 Data Rate	-24.018 ppm	48.0 %	-300.000 ppm <= VALUE <= 300.000 ppm
✓	0	1	HFR1-8: D2 AC Common Mode Noise	50 mV	68.7 %	VALUE <= 150 mV
✓	0	1	HFR1-6: D2 RJ Measurement Test	78 mTbit	38.7 %	1 mTbit <= VALUE <= 200 mTbit
✓	0	1	HFR1-7: D2 Eye Mask Test - Category 3 Worst Cable Model (WCM3)	0.000	50.0 %	No Mask Failures
✓	0	1	HFR1-7: D2 Eye Mask Test - Category 3 Short Cable Model (SCMB)	0.000	50.0 %	No Mask Failures
✓	0	1	HFR1-4: Inter-Pair Skew - D3/D0	39 mTBit	49.5 %	InterpairSkew ThresholdNeg TBit <= VALUE <= InterpairSkew ThresholdPos TBit
✓	0	1	HFR1-4: Inter-Pair Skew - D1/D2	5 mTBit	49.9 %	InterpairSkew ThresholdNeg TBit <= VALUE <= InterpairSkew ThresholdPos TBit
✓	0	1	HFR1-4: Inter-Pair Skew - D0/D1	-101 mTBit	48.7 %	InterpairSkew ThresholdNeg TBit <= VALUE <= InterpairSkew ThresholdPos TBit
✓	0	1	HFR1-4: Inter-Pair Skew - D3/D1	-62 mTBit	49.2 %	InterpairSkew ThresholdNeg TBit <= VALUE <= InterpairSkew ThresholdPos TBit
✓	0	1	HFR1-4: Inter-Pair Skew - D3/D2	-57 mTBit	49.3 %	InterpairSkew ThresholdNeg TBit <= VALUE <= InterpairSkew ThresholdPos TBit
✓	0	1	HFR1-4: Inter-Pair Skew - D0/D2	-98 mTBit	48.8 %	InterpairSkew ThresholdNeg TBit <= VALUE <= InterpairSkew ThresholdPos TBit

# 11.TYPEC—DP



## DisplayPort

### Summary of Results

Test Statistics	
Failed	0
Passed	18
Total	18

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Worst Actual	Worst Margin	Pass Limits
✓	0	10	3.3 Lane 0 - Peak to Peak Voltage Test - PRBS_7	864 mV	37.4 %	VALUE <= 1.380 V
✓	0	10	3.3 Lane 1 - Peak to Peak Voltage Test - PRBS_7	888 mV	35.8 %	VALUE <= 1.380 V
✓	0	10	3.3 Lane 2 - Peak to Peak Voltage Test - PRBS_7	824 mV	40.3 %	VALUE <= 1.380 V
✓	0	10	3.3 Lane 3 - Peak to Peak Voltage Test - PRBS_7	872 mV	36.8 %	VALUE <= 1.380 V
✓	0	1	3.1 Lane 0 - Eye Diagram Test - PRBS_7	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 1 - Eye Diagram Test - PRBS_7	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 2 - Eye Diagram Test - PRBS_7	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 3 - Eye Diagram Test - PRBS_7	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	4	3.12 Lane 0 - Total Jitter Test (HBR) - PRBS_7	216.100 mUI	48.5 %	VALUE <= 420.000 mUI
✓	0	4	3.12 Lane 1 - Total Jitter Test (HBR) - PRBS_7	150.800 mUI	64.1 %	VALUE <= 420.000 mUI
✓	0	4	3.12 Lane 2 - Total Jitter Test (HBR) - PRBS_7	242.700 mUI	42.2 %	VALUE <= 420.000 mUI
✓	0	4	3.12 Lane 3 - Total Jitter Test (HBR) - PRBS_7	220.000 mUI	47.6 %	VALUE <= 420.000 mUI
✓	0	4	3.11 Lane 0 - Non ISI Jitter Test (HBR) - PRBS_7	136.800 mUI	50.4 %	VALUE <= 276.000 mUI
✓	0	4	3.11 Lane 1 - Non ISI Jitter Test (HBR) - PRBS_7	111.800 mUI	59.5 %	VALUE <= 276.000 mUI
✓	0	4	3.11 Lane 2 - Non ISI Jitter Test (HBR) - PRBS_7	154.900 mUI	43.9 %	VALUE <= 276.000 mUI
✓	0	4	3.11 Lane 3 - Non ISI Jitter Test (HBR) - PRBS_7	146.500 mUI	46.9 %	VALUE <= 276.000 mUI

# 11.TYPEC—DP



## DisplayPort

### Summary of Results

Test Statistics		
Failed	0	
Passed	24	
Total	24	

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	3.1 Lane 0 - Eye Diagram Test (TP3_EQ) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 1 - Eye Diagram Test (TP3_EQ) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 2 - Eye Diagram Test (TP3_EQ) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 3 - Eye Diagram Test (TP3_EQ) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 0 - Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 1 - Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 2 - Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 3 - Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.12 Lane 0 - Total Jitter Test (TP3_EQ)(HBR2) - HBR2CPAT	171.300 mUI	70.5 %	VALUE <= 580.000 mUI
✓	0	1	3.12 Lane 1 - Total Jitter Test (TP3_EQ)(HBR2) - HBR2CPAT	179.300 mUI	89.1 %	VALUE <= 580.000 mUI
✓	0	1	3.12 Lane 2 - Total Jitter Test (TP3_EQ)(HBR2) - HBR2CPAT	179.500 mUI	69.1 %	VALUE <= 580.000 mUI
✓	0	1	3.12 Lane 3 - Total Jitter Test (TP3_EQ)(HBR2) - HBR2CPAT	189.300 mUI	67.4 %	VALUE <= 580.000 mUI
✓	0	1	3.12 Lane 0 - Total Jitter Test with No Cable Model (TP3_EQ)(HBR2) - HBR2CPAT	200.000 mUI	85.5 %	VALUE <= 580.000 mUI
✓	0	1	3.12 Lane 1 - Total Jitter Test with No Cable Model (TP3_EQ)(HBR2) - HBR2CPAT	198.000 mUI	85.9 %	VALUE <= 580.000 mUI
✓	0	1	3.12 Lane 2 - Total Jitter Test with No Cable Model (TP3_EQ)(HBR2) - HBR2CPAT	210.800 mUI	63.7 %	VALUE <= 580.000 mUI
✓	0	1	3.12 Lane 3 - Total Jitter Test with No Cable Model (TP3_EQ)(HBR2) - HBR2CPAT	205.800 mUI	84.5 %	VALUE <= 580.000 mUI
✓	0	1	3.12 Lane 0 - Deterministic Jitter Test (TP3_EQ) - HBR2CPAT	79.000 mUI	83.9 %	VALUE <= 490.000 mUI
✓	0	1	3.12 Lane 1 - Deterministic Jitter Test (TP3_EQ) - HBR2CPAT	88.800 mUI	82.3 %	VALUE <= 490.000 mUI
✓	0	1	3.12 Lane 2 - Deterministic Jitter Test (TP3_EQ) - HBR2CPAT	89.200 mUI	81.8 %	VALUE <= 490.000 mUI
✓	0	1	3.12 Lane 3 - Deterministic Jitter Test (TP3_EQ) - HBR2CPAT	98.500 mUI	79.9 %	VALUE <= 490.000 mUI
✓	0	1	3.12 Lane 0 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT	104.400 mUI	78.7 %	VALUE <= 490.000 mUI
✓	0	1	3.12 Lane 1 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT	104.100 mUI	78.8 %	VALUE <= 490.000 mUI
✓	0	1	3.12 Lane 2 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT	113.700 mUI	78.8 %	VALUE <= 490.000 mUI
✓	0	1	3.12 Lane 3 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT	114.300 mUI	78.7 %	VALUE <= 490.000 mUI

## DisplayPort

## Summary of Results

## Test Statistics

Failed	0
Passed	12
Total	12

## Margin Thresholds

Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	3.1 Lane 0 - Eye Diagram Test (TP3_ CTLE) - TPS4	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 1 - Eye Diagram Test (TP3_ CTLE) - TPS4	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 2 - Eye Diagram Test (TP3_ CTLE) - TPS4	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 3 - Eye Diagram Test (TP3_ CTLE) - TPS4	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.11 Lane 0 - Total Jitter Test (TP3_ CTLE) - TPS4	261.200 mUI	44.4 %	VALUE <= 470.000 mUI
✓	0	1	3.11 Lane 1 - Total Jitter Test (TP3_ CTLE) - TPS4	259.800 mUI	44.7 %	VALUE <= 470.000 mUI
✓	0	1	3.11 Lane 2 - Total Jitter Test (TP3_ CTLE) - TPS4	275.100 mUI	41.5 %	VALUE <= 470.000 mUI
✓	0	1	3.11 Lane 3 - Total Jitter Test (TP3_ CTLE) - TPS4	245.400 mUI	47.8 %	VALUE <= 470.000 mUI
✓	0	1	3.11 Lane 0 - Non ISI Jitter Test (TP3_ CTLE) - TPS4	98.800 mUI	57.0 %	VALUE <= 230.000 mUI
✓	0	1	3.11 Lane 1 - Non ISI Jitter Test (TP3_ CTLE) - TPS4	99.200 mUI	56.9 %	VALUE <= 230.000 mUI
✓	0	1	3.11 Lane 2 - Non ISI Jitter Test (TP3_ CTLE) - TPS4	108.300 mUI	52.9 %	VALUE <= 230.000 mUI
✓	0	1	3.11 Lane 3 - Non ISI Jitter Test (TP3_ CTLE) - TPS4	95.200 mUI	58.6 %	VALUE <= 230.000 mUI

## RK3588 eDP 1.62G RBR

## Summary of Results

Test Statistics		
Failed	0	
Passed	3	
Total	3	

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Worst Actual	Worst Margin	Pass Limits
✓	0	10	Lane 0 - Peak to Peak Differential Voltage Test (PRBS 7)	1.156 V	16.2 %	VALUE <= 1.380 V
✓	0	10	Lane 0 - Differential Voltage Level Test (PRBS 7)	377.518 mV	31.3 %	DiffVoltageLevelAbsoluteMinLimit V <= VALUE <= DiffVoltageLevelAbsoluteMaxLimit V
✓	0	10	Lane 0 - Pre-Emphasis Level Test (PRBS 7)	3.063 dB	38.4 %	PreEmphasisLevelAbsoluteMinLimit dB <= VALUE <= PreEmphasisLevelAbsoluteMaxLimit dB

## RK3588 eDP 2.7G HBR

## Summary of Results

Test Statistics		
Failed	0	
Passed	3	
Total	3	

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Worst Actual	Worst Margin	Pass Limits
✓	0	10	Lane 0 - Peak to Peak Differential Voltage Test (PRBS 7)	1.061 V	23.1 %	VALUE <= 1.380 V
✓	0	10	Lane 0 - Differential Voltage Level Test (PRBS 7)	703.833 mV	8.0 %	DiffVoltageLevelAbsoluteMinLimit V <= VALUE <= DiffVoltageLevelAbsoluteMaxLimit V
✓	0	10	Lane 0 - Pre-Emphasis Level Test (PRBS 7)	5.203 dB	16.8 %	PreEmphasisLevelAbsoluteMinLimit dB <= VALUE <= PreEmphasisLevelAbsoluteMaxLimit dB

# 12.eDP



## RK3588 eDP 5.4G HBR2

### Summary of Results

Test Statistics	
Failed	0
Passed	3
Total	3

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Worst Actual	Worst Margin	Pass Limits
✓	0	10	Lane 0 - Peak to Peak Differential Voltage Test (PLTPAT)	1.117 V	19.1 %	VALUE <= 1.380 V
✓	0	10	Lane 0 - Differential Voltage Level Test (PLTPAT)	897.914 mV	3.4 %	DiffVoltageLevelAbsoluteMinLimit V <= VALUE <= DiffVoltageLevelAbsoluteMaxLimit V
✓	0	10	Lane 0 - Pre-Emphasis Level Test (PLTPAT)	5.170 dB	15.4 %	PreEmphasisLevelAbsoluteMinLimit dB <= VALUE <= PreEmphasisLevelAbsoluteMaxLimit dB

# 13.MIPI D/C PHY



## MIPI D-PHY TX

### Summary of Results

#### Test Statistics

Failed	0
Passed	12
Total	12

#### Margin Thresholds

Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	1.3.7 HS Data TX Static Common Mode Voltage(Vcmtx)	195.84 mV	45.8 %	150.00 mV <= VALUE <= 250.00 mV
✓	0	1	1.3.8 HS Data TX Vcmtx Mismatch	710 碪V	85.8 %	VALUE < 5.00 mV
✓	0	1	1.3.4 HS Data TX Differential Voltage(VOD0 Pulse)	-225.50 mV	34.2 %	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	1.3.4 HS Data TX Differential Voltage(VOD1 Pulse)	215.04 mV	42.3 %	140.00 mV <= VALUE <= 270.00 mV
✓	0	1	1.3.5 HS Data TX Differential Voltage Mismatch (Pulse)	10.45 mV	25.4 %	VALUE < 14.00 mV
✓	0	1	1.3.6 HS Data TX Single Ended Output High Voltage(VOHHS Pulse)	309.07 mV	14.1 %	VALUE <= 360.00 mV
✓	0	1	1.4.7 HS Clock TX Static Common Mode Voltage(Vcmtx)	200.68 mV	49.3 %	150.00 mV <= VALUE <= 250.00 mV
✓	0	1	1.4.8 HS Clock TX Vcmtx Mismatch	620 碪V	87.6 %	VALUE < 5.00 mV
✓	0	1	1.4.4 HS Clock TX Differential Voltage(VOD0 Pulse)	-224.39 mV	35.1 %	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	1.4.4 HS Clock TX Differential Voltage(VOD1 Pulse)	218.33 mV	39.7 %	140.00 mV <= VALUE <= 270.00 mV
✓	0	1	1.4.5 HS Clock TX Differential Voltage Mismatch (Pulse)	6.06 mV	56.7 %	VALUE < 14.00 mV
✓	0	1	1.4.6 HS Clock TX Single Ended Output High Voltage(VOHHS Pulse)	319.96 mV	11.1 %	VALUE <= 360.00 mV

# 13.MIPI D/C PHY



## MIPI D-PHY RX

### Summary of Results

Test Statistics		
Failed	0	
Passed	27	
Total	27	

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass #	Failed #	Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	1.3.7 HS Data TX Static Common Mode Voltage(Vcmtx)	221.94 mV	28.1 %	160.00 mV <= VALUE <= 250.00 mV
✓	0	1	1.3.8 HS Data TX Vcmtx Mismatch	910 磷V	81.8 %	VALUE < 5.00 mV
✓	0	1	1.3.10 HS Data TX Common-Level Variations Above 450MHz (VCMTX(HF))	5.31 mV	64.6 %	VALUE < 15.00 mV
✓	0	1	1.3.9 HS Data TX Common-Level Variations Between 50-450MHz (VCMTX(LF))	7.63 mV	69.5 %	VALUE < 25.00 mV
✓	0	1	1.3.4 HS Data TX Differential Voltage(VD00 Pulse)	-211.99 mV	44.6 %	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	1.3.4 HS Data TX Differential Voltage(VD01 Pulse)	201.83 mV	47.6 %	140.00 mV <= VALUE <= 270.00 mV
✓	0	1	1.3.5 HS Data TX Differential Voltage Mismatch (Pulse)	10.16 mV	27.4 %	VALUE < 14.00 mV
✓	0	1	1.3.6 HS Data TX Single Ended Output High Voltage(VOHHHS Pulse)	327.51 mV	9.0 %	VALUE <= 360.00 mV
✓	0	1	1.4.9 HS Clock TX Common-Level Variations Between 50-450MHz (VCMTX(LF))	6.43 mV	74.3 %	VALUE < 25.00 mV
✓	0	1	1.4.7 HS Clock TX Static Common Mode Voltage(Vcmbs)	228.20 mV	21.8 %	160.00 mV <= VALUE <= 250.00 mV
✓	0	1	1.4.10 HS Clock TX Common-Level Variations Above 450MHz (VCMTX(HF))	6.65 mV	55.7 %	VALUE < 15.00 mV
✓	0	1	1.4.4 HS Clock TX Differential Voltage(VD00 Pulse)	-222.25 mV	36.7 %	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	1.4.4 HS Clock TX Differential Voltage(VD01 Pulse)	222.92 mV	36.2 %	140.00 mV <= VALUE <= 270.00 mV
✓	0	1	1.4.5 HS Clock TX Differential Voltage Mismatch (Pulse)	870 磷V	95.2 %	VALUE < 14.00 mV
✓	0	1	1.4.6 HS Clock TX Single Ended Output High Voltage(VOHHHS Pulse)	338.81 mV	5.9 %	VALUE <= 360.00 mV
✓	0	1	1.4.17 HS Clock Instantaneous (Ulinst)(Min)	371 ps	371.0 %	VALUE >= Ulinst_Min_Limit s
✓	0	1	1.3.1 HS Entry: DATA TLPX	57.59 ns	15.2 %	VALUE >= 50.00 ns
✓	0	1	1.3.2 HS Entry: DATA TX THS-PREPARE	52.43 ns	23.8 %	THSPrepare_LimitMin s <= VALUE <= THSPrepare_LimitMax s
✓	0	1	1.3.3 HS Entry: DATA TX THS-PREPARE+THS-ZERO	176.07 ns	18.2 %	VALUE >= TXTHSPrepareTHSZero_LimitMin s
✓	0	1	1.3.13 HS Exit: DATA TX THS-TRAIL	71.94 ns	16.8 %	VALUE >= TXTHSTrail_LimitMin s
✓	0	1	1.3.14 HS Exit: DATA TX TREOT	9.74 ns	72.2 %	VALUE <= 35.00 ns
✓	0	1	1.3.15 HS Exit: DATA TX TEOT	81.68 ns	25.6 %	VALUE <= TXTEOT_LimitMax s
✓	0	1	1.3.16 HS Exit: DATA TX THS-EXIT	4.90679 無s	490E+01 %	VALUE >= 100.00 ns
✓	0	1	1.5.3 HS Clock Rising Edge Alignment to First Payload Bit	Pass	100.0 %	VALUE <= 500.0000000000 m
✓	0	1	1.4.17 HS Clock Instantaneous (Ulinst)(Max)	431 ps	98.6 %	VALUE < 12.500 ns
✓	0	1	1.5.4 Data-to-Clock Skew (TSKEW(TX))(Max,Min)	-102 mUlinst	24.5 %	MinMaxTSkewTest_LimitMin Ulinst <= VALUE <= MinMaxTSkewTest_LimitMax Ulinst
✓	0	1	1.5.4 Data-to-Clock Skew (TSKEW(TX))(Mean)	-4 mUlinst	49.0 %	MeanTSkewTest_LimitMin Ulinst <= VALUE <= MeanTSkewTest_LimitMax Ulinst

# 14.MIPI DPHY



## MIPI D-PHY RX

### Summary of Results

Test Statistics		
Failed	1	
Passed	51	
Total	52	

Pass #	Failed #	Trials	Test Name	Actual Value	Pass Limits
✓	0	1	1.3.7 HS Data TX Static Common Mode Voltage(Vcmtx)	223.56 mV	150.00 mV <= VALUE <= 250.00 mV
✓	0	1	1.3.8 HS Data TX Vomtx Mismatch	300 mV	VALUE < 6.00 mV
✓	0	1	1.3.10 HS Data TX Common-Level Variations Above 450MHz (VCMTX(HF))	6.65 mV	VALUE < 15.00 mV
✓	0	1	1.3.9 HS Data TX Common-Level Variations Between 50-450MHz (VCMTX(LF))	8.90 mV	VALUE < 25.00 mV
✓	0	1	1.3.4 HS Data TX Differential Voltage(VODO Pulse)	-221.37 mV	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	1.3.6 HS Data TX Single Ended Output High Voltage(VOHHS Pulse)	193.08 mV	140.00 mV <= VALUE <= 270.00 mV
✓	0	1	1.3.8 HS Data TX Single Ended Output Low Voltage(VOLHS Pulse)	331.17 mV	VALUE <= 360.00 mV
✓	0	1	1.4.17 HS Clock Instantaneous (Ulinst)(Max)	438 ps	VALUE < 12.500 ns
✓	0	1	1.3.3 HS Entry: DATA TX THS-PREPARE+THS-ZERO	175.80 ns	VALUE >= TXTHSPrepareTHSZero_LimitMin s
✗	1	1	1.3.11 HS Data TX 20%-80% Rise Time (tR)(Burst Data)	188 ps	VALUE < DataRiseTime_LimitMax s
✓	0	1	1.3.11 HS Data TX 20%-80% Rise Time (tR)(Burst Data)(Min Conformance Limit)(Informative)	188 ps	VALUE > DataRiseTime_LimitMin s
✓	0	1	1.3.12 HS Data TX 80%-20% Fall Time (tF)(Burst Data)	118 ps	VALUE < DataFallTime_LimitMax s
✓	0	1	1.3.12 HS Data TX 80%-20% Fall Time (tF)(Burst Data)(Min Conformance Limit)(Informative)	118 ps	VALUE > DataFallTime_LimitMin s
✓	0	1	1.4.9 HS Clock TX Common-Level Variations Between 50-450MHz (VCMTX(LF))	6.21 mV	VALUE < 25.00 mV
✓	0	1	1.4.7 HS Clock TX Static Common Mode Voltage(Vcmbo)	224.59 mV	150.00 mV <= VALUE <= 250.00 mV
✓	0	1	1.4.8 HS Clock TX Vomtx Mismatch	1.55 mV	VALUE < 6.00 mV
✓	0	1	1.4.10 HS Clock TX Common-Level Variations Above 450MHz (VCMTX(HF))	7.14 mV	VALUE < 15.00 mV
✓	0	1	1.4.4 HS Clock TX Differential Voltage(VODO Pulse)	-192.02 mV	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	1.4.4 HS Clock TX Differential Voltage(VOD1 Pulse)	186.99 mV	140.00 mV <= VALUE <= 270.00 mV
✓	0	1	1.4.5 HS Clock TX Differential Voltage Mismatch (Pulse)	5.03 mV	VALUE < 14.00 mV
✓	0	1	1.4.6 HS Clock TX Single Ended Output High Voltage(VOHHS Pulse)	323.96 mV	VALUE <= 360.00 mV
✓	0	1	1.4.3 HS Entry: CLK TX TCLK-PREPARE+TCLK-ZERO	377.39 ns	VALUE >= 300.00 ns
✓	0	1	1.4.11 HS Clock TX 20%-80% Rise Time (tR)(Burst Clock)	155 ps	VALUE < CLKRiseTime_LimitMax s
✓	0	1	1.4.11 HS Clock TX 20%-80% Rise Time (tR)(Burst Clock)(Min Conformance Limit)(Informative)	155 ps	VALUE > CLKRiseTime_LimitMin s
✓	0	1	1.4.12 HS Clock TX 80%-20% Fall Time (tF)(Burst Clock)	153 ps	VALUE < CLKFallTime_LimitMax s
✓	0	1	1.4.12 HS Clock TX 80%-20% Fall Time (tF)(Burst Clock)(Min Conformance Limit)(Informative)	153 ps	VALUE > CLKFallTime_LimitMin s
✓	0	1	1.4.17 HS Clock Instantaneous (Ulinst)(Min)	361 ps	VALUE >= Ulinst_Min_Limit s
✓	0	1	1.3.1 HS Entry: DATA TLPX	57.46 ns	VALUE >= 50.00 ns
✓	0	1	1.3.2 HS Entry: DATA TX THS-PREPARE	51.59 ns	THSPrepare_LimitMin s <= VALUE <= THSPrepare_LimitMax s
✓	0	1	1.3.13 HS Exit: DATA TX THS-TRAIL	74.99 ns	VALUE >= TXTHSTail_LimitMin s
✓	0	1	1.3.14 HS Exit: DATA TX TREOT	7.33 ns	VALUE <= 35.00 ns
✓	0	1	1.3.15 HS Exit: DATA TX TEOT	82.32 ns	VALUE <= TXTEOT_LimitMax s

# 15.USB3.0



## USB3.0 HOST

### Summary of Results

Test Statistics	
Failed	0
Passed	23
Total	23

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name (click to jump)	Actual Value	Margin	Pass Limits
✓	0	1	<a href="#">LFPS Peak-Peak Differential Output Voltage</a>	1.0821 V	29.5 %	800.0 mV <= VALUE <= 1.2000 V
✓	0	1	<a href="#">LFPS Period (tPeriod)</a>	41.6479 ns	27.1 %	20.0000 ns <= VALUE <= 100.0000 ns
✓	0	1	<a href="#">LFPS Burst Width (tBurst)</a>	1.0500 µs	43.8 %	600.0 ns <= VALUE <= 1.4000 µs
✓	0	1	<a href="#">LFPS Repeat Time Interval (tRepeat)</a>	10.0418 µs	49.5 %	6.0000 µs <= VALUE <= 14.0000 µs
✓	0	1	<a href="#">LFPS Rise Time</a>	256.1 ps	93.6 %	VALUE <= 4.0000 ns
✓	0	1	<a href="#">LFPS Fall Time</a>	259.2 ps	93.5 %	VALUE <= 4.0000 ns
✓	0	1	<a href="#">LFPS Duty cycle</a>	51.0477 %	44.8 %	40.0000 % <= VALUE <= 60.0000 %
✓	0	1	<a href="#">LFPS AC Common Mode Voltage</a>	33.0 mV	67.0 %	VALUE <= 100.0 mV
✓	0	1	<a href="#">SG TSSC-Freq-Dev-Min</a>	-4.828473 kppm	29.5 %	-5.300000 kppm <= VALUE <= -3.700000 kppm
✓	0	1	<a href="#">SG TSSC-Freq-Dev-Max</a>	225.193 ppm	12.5 %	TSSCMin ppm <= VALUE <= TSSCMax ppm
✓	0	1	<a href="#">SG SSC Modulation Rate</a>	31.113316 kHz	37.1 %	30.000000 kHz <= VALUE <= 33.000000 kHz
✓	0	1	<a href="#">SG SSC Slew Rate</a>	4.838 ms	51.6 %	VALUE <= 10.000 ms
✓	0	1	<a href="#">SG SSC df/dt</a>	346.0 ppm/us	72.3 %	VALUE <= 1.2500 kppm/us
ⓘ	0	1	<a href="#">SG Short Channel Random Jitter</a>	709 fs	100.0 %	Information Only
✓	0	1	<a href="#">SG Short Channel Maximum Deterministic Jitter</a>	27.461 ps	68.1 %	VALUE <= 86.000 ps
✓	0	1	<a href="#">SG Short Channel Total Jitter at BER-12</a>	37.432 ps	71.6 %	VALUE <= 132.000 ps
✓	0	1	<a href="#">SG Short Channel Template Test</a>	0.000	100.0 %	VALUE = 0.000
✓	0	1	<a href="#">SG Short Channel Differential Output Voltage</a>	445.9 mV	31.4 %	100.0 mV <= VALUE <= 1.2000 V
ⓘ	0	1	<a href="#">SG Random Jitter (CTLE ON)</a>	654 fs	100.0 %	Information Only
✓	0	1	<a href="#">SG Far End Maximum Deterministic Jitter (CTLE ON)</a>	46.918 ps	45.4 %	VALUE <= 86.000 ps
✓	0	1	<a href="#">SG Far End Total Jitter at BER-12 (CTLE ON)</a>	56.118 ps	57.5 %	VALUE <= 132.000 ps
✓	0	1	<a href="#">SG Far End Template Test (CTLE ON)</a>	0.000	100.0 %	VALUE = 0.000
✓	0	1	<a href="#">SG Far End Differential Output Voltage (CTLE ON)</a>	230.6 mV	11.9 %	100.0 mV <= VALUE <= 1.2000 V

# 16.USB2.0



## USB2.0 DEVICE

### Summary of Results

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✓	0	1	<a href="#">EL_38 EL_39 Device Suspend Timing Response</a>	3.064 ms	48.8 %	3.000 ms <= VALUE <= 3.125 ms
✓	0	1	<a href="#">EL_40 Device Resume Timing Response</a>	Pass	100.0 %	Pass/Fail
✓	0	1	<a href="#">EL_27 Device CHIRP Response to Reset from Hi-Speed Operation</a>	3.563 ms	16.0 %	3.100 ms <= VALUE <= 6.000 ms
✓	0	1	<a href="#">EL_28 Device CHIRP Response to Reset from Suspend</a>	20.322 µs	0.3 %	2.500 µs <= VALUE <= 6.00000 ms

## USB2.0 HOST

### Summary of Results

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✓	0	1	<a href="#">EL_33 CHIRP Timing Response</a>	5.307 µs	5.3 %	1 ns <= VALUE <= 100.000 µs
✓	0	1	<a href="#">EL_34 CHIRP K Width</a>	50.064 µs	49.7 %	40.000 µs <= VALUE <= 60.000 µs
✓	0	1	<a href="#">EL_34 CHIRP J Width</a>	50.070 µs	49.7 %	40.000 µs <= VALUE <= 60.000 µs
✓	0	1	<a href="#">EL_35 SOF Timing Response</a>	304.230 µs	48.9 %	100.000 µs <= VALUE <= 500.000 µs

# 17.RGMII



## RGMII SI TEST Report

PHY and Power Supply Type	Drive strength (mA)	NOTE: 测试前先选择PHY和Power类型，测试点及参考电平参照Remark说明。										
		Test item	Unit	Spec limited			Measure			Test Result	Waveform	
Realtek-1.8V				Min	Typical	Max	Min	Mean	Max			
		MDC Cycle Time	tMCC	ns	80.00					Null	tMCC	
		MDC High Time	tMCH	ns	32.00					Null	tMCH	
		MDC Low Time	tMCL	ns	32.00					Null	tMCL	
		MDC Input High Voltage	Vih_MDC	V	1.20					Null	Vih MDC	
		MDC Input Low Voltage	Vil_MDC	V		0.50				Null	Vil MDC	
		MDIO Setup Time	tMSU	ns	10.00					Null	tMSU	
		MDIO Hold Time	tMHT	ns	10.00					Null	tMHT	
		MDIO Clock Rise to MDIO Valid	tMRV	ns		300.00				Null	tMRV	
		MDIO Input High Voltage	Vih_MDIO	V	1.20					Null	Vih MDIO	
		MDIO Input Low Voltage	Vil_MDIO	V		0.50				Null	Vil MDIO	
		CPU MDIO Input Setup Time	CPU_tMSU	ns	-	-				Null	CPU_tMSU	
		CPU MDIO Input Hold time	CPU_tMHT	ns						Null	CPU_tMHT	
		CPU MDIO Input High Voltage	CPU_Vih_MDIO	V						Null	CPU_Vih MDIO	
		CPU MDIO Input Low Voltage	CPU_Vil_MDIO	V						Null	CPU_Vil MDIO	
		CLK period	tGCC_CLK	ns	7.20	8.80				Null	tGCC_CLK	
		CLK frequency deviation	FD_CLK	ppm	-	-				Null	FD_CLK	
		CLK Duty Cycle	tDuty_CLK	%	-	-				Null	tDuty CLK	
		CLK Rise Time	tR_CLK	ns		-				Null	tR_CLK	
		CLK Fall Time	tF_CLK	ns		-				Null	tF_CLK	
		TXC clock period	tGCC_TXC	ns	36.0	40.0	44.0	39.88	40	40.1	Pass	tGCC_TXC
		TXC Duty Cycle	tDuty_TXC	%	40	50	60	49.9	50	50.1	Pass	tDuty_TXC
		TXC Rise Time	tR_TXC	ns		0.75			0.548	Pass	tR_TXC	
		TXC Fall Time	tF_TXC	ns		0.75			0.46	Pass	tF_TXC	
		RXC clock period	tGCC_RXC	ns	36.0	40.0	44.0	39.79	40	40.14	Pass	tGCC_RXC
		RXC Duty Cycle	tDuty_RXC	%	40	50	60	49.5	49.9	50.2	Pass	tDuty_RXC
		RXC Rise Time	tR_RXC	ns		0.75			1.24	Fail	tR_RXC	
		RXC Fall Time	tF_RXC	ns		0.75			1.09	Fail	tF_RXC	
		TXD Input High Voltage	Vih_TXD	V	1.20			1.76	1.808	Pass	Vih_TXD	
		TXD Input Low Voltage	Vil_TXD	V				-0.02	0.024	Pass	Vil_TXD	
		TXD to Clock Input Setup	tSETUP	ns	1.2	2.0		1.44	-	Pass	tSETUP	
		TXD to Clock Input Hold	tHOLD	ns	1.2	2.0		37.66	-	Pass	tHOLD	
		RXD CPU Input High Voltage	CPU_Vih_RXD	V				1.76	-	1.8	Null	CPU_Vih_RXD
		RXD CPU Input Low Voltage	CPU_Vil_RXD	V				-0.062	-	-0.003	Null	CPU_Vil_RXD
		RXD to Clock Input Setup	CPU_ISETUP	ns				1.48	-	-	Null	CPU_ISETUP
		RXD to Clock Input Hold	CPU_IHOLD	ns				37.47	-	-	Null	CPU_IHOLD

NOTE: tR\_RXC/tF\_RXC为RGMII PHY (RTL8211) 过来的信号，与RK3588无关，可不关注。

# 18.SDMMC



## SD Spec SI Test Reports

### SD Signal Integrity and Timing Analysis

4 Data Lane Speed Mode	Drive strength (mA)	Power supply (V)	NOTE: The test points need to be at the far end of the signal output.								
			Spec limited			Measure			Test Result	Waveform	Remark
SDR104	1.7-1.95	Min	Typical	Max	MIN	Mean	MAX	Pass			
SD_CLK	Trace length mils	Description	Test item	Unit	Min	Typical	Max	MIN	Mean	MAX	Test Result
		Frequence	tPP	MHz	0		208	-	148.5	-	Do not care
		Clock Cycle	tCLK	ns	4.8		-	6.64	6.83	-	Pass
		Clock Duty	tDUTY	%	30		70	47.8	-	50.5	Pass
		Time of Low Level to High Level	tCR	ns	-		1.366	-	-	0.553	Pass
SD_CMD		Time of High Level to Low Level	tCF	ns	-		1.366	-	-	0.538	Pass
		Setup Time of Input	tISU	ns	1.4		-	2.93	-	-	Pass
		Hold Time of Input	tIH		0.8		-	3.05	-	-	Pass
		Card Output Phase	tOP		0		13.66	-	-	4.05	Pass
SD_Data		Output valid data window	tODW		4.098		-	6.08	-	-	Pass
		Setup Time of Input	tISU	ns	1.4		-	2.65	-	-	Pass
		Hold Time of Input	tIH		0.8		-	3.08	-	-	Pass
		Card Output Phase	tOP		0		13.66	-	-	4.16	Pass
		Output valid data window	tODW		4.098		-	5.97	-	-	Pass

### Push-pull mode bus signal level For 1.7V-1.95V VDDIO range

1.7-1.95						Measure		Test Result	Waveform	Remark
Parameter	Symbol	Min	Max	Unit	Conditions	MIN	MAX	Null		
IO Power Supply Voltage	VDD	1.7	1.95	V				Null	-	
CPU Input High Voltage of CMD	CPU-VIH-CMD	根据指标	CPU规格书填写	V		1.856	1.993	Null	CPU-VIH-CMD	
CPU Input Low Voltage of CMD	CPU-VIL-CMD	根据指标	CPU规格书填写	V		-0.047	0.05	Null	CPU-VIL-CMD	
CPU Input High Voltage of Data	CPU-VIH-Data	根据指标	CPU规格书填写	V		1.89	1.95	Null	CPU-VIH-Data	
CPU Input Low Voltage of Data	CPU-VIL-Data	根据指标	CPU规格书填写	V		-0.277	0.03	Null	CPU-VIL-Data	
Device InputHigh Voltage of CLK	VIH-CLK	1.27	2	V		1.75	1.79	Pass	SD VIH CLK	
Device InputLow Voltage of CLK	VIL-CLK	-0.3	0.58	V		-0.077	-0.019	Pass	SD VIL CLK	
Device InputHigh Voltage of CMD	VIH-CMD	1.27	2	V		1.7	1.8	Pass	SD VIH CMD	
Device InputLow Voltage of CMD	VIL-CMD	-0.3	0.58	V		-0.057	0.023	Pass	SD VIL CMD	
Device InputHigh Voltage of Data	VIH-Data	1.27	2	V		1.77	1.82	Pass	SD VIH DATA	
Device InputLow Voltage of Data	VIL-Data	-0.3	0.58	V		-0.012	0.043	Pass	SD VIL DATA	
		-	-	V				Do not care	-	

## SPDIF Test Report

### SPDIF Signal Integrity and Timing Analysis

Drive strength (ohm)	Power supply (V)	NOTE: The test points need to be at the far end of the signal output.										
Signal Name	Description	Test item	Unit	25M Spec limited			Measure		Test Result	Waveform	Remark	
				Min	Typical	Max	Min	Max				
SPDIF_TX	Frequence	Freq	MHz				3.058	3.072	Pass	<a href="#">SPDIF-Freq</a>		
	Rise Time	tRISE	ns	0.1		25	1.550	2.200	Pass	<a href="#">SPDIF-tRISE</a>		
	Fall Time	tFALL	ns	0.1		25	0.900	2.260	Pass	<a href="#">SPDIF-tFALL</a>		
	Jitter	Tjitter	ns	-		15	-	0.510	Pass	<a href="#">SPDIF-Jitter</a>		
	Signal Voltage	VIH	V				1.810	1.880	Pass	<a href="#">SPDIF-VIH</a>		

## Uart2 M0 3.3V SI Test Report

Baud rate	Power supply (V)	NOTE: The test points need to be at the far end of the signal output.									
Normal model											
Signal Name	Description	Test item	Unit	Spec limited			Measure		Test Result	Waveform	Remark
				Min	Typical	Max	Min	Max			
TX	Baud rate	TX-BR	Mb/s	2.82		3.18	2.998	3.001	Pass	<a href="#">TX-BR</a>	
	Pulse duration	TX-Tw	ns	331.3333		335.33333	333.15	333.60	Pass	<a href="#">TX-Tw</a>	
	Input HIGH voltage	VIH	V	2		3.6	3.21	3.22	Pass	<a href="#">TX-VIH</a>	
	Input LOW voltage	VIL	V	-0.3		0.8	0.040	0.060	Pass	<a href="#">TX-VIL</a>	
RX	Baud rate	RX-BR	Mb/s	2.82		3.18	2.992	3.01	Pass	<a href="#">RX-BR</a>	板载FT232R测试
	Pulse duration	RX-Tw	ns	320		350	326.45	328.60	Pass	<a href="#">RX-Tw</a>	
	Input HIGH voltage	VIH	V	2		3.6	3.22	3.24	Pass	<a href="#">RX-VIH</a>	
	Input LOW voltage	VIL	V	-0.3		0.8	0.040	0.060	Pass	<a href="#">RX-VIL</a>	

## I<sup>2</sup>S0 SI Test Report

Channels (Ch)	Sampling Digit (bits)	Sample Rate (kHz)	Power supply (V)	NOTE: 1.The test points need to be at the far end of the signal output.							
8	16	48	1.8								
Signal Name	Test item	Description	Unit	Spec limited			Measure			Test Result	Waveform
				Min	Typical	Max	Min	Mean	Max	Pass	Remark
MCLK	fMCLK	Frequency	MHz	8.144	12.288	24.576	12.28	12.29	12.3	Pass	fMCLK
	dMCLK	MCLK Duty Cycle	%	45.00		55.00	49.91	49.976	50.03	Pass	dMCLK
	VIH-MCLK	High-level Input Voltage	V	1.26		2.10	1.732	1.738	1.75	Pass	VIH-MCLK
	VIL-MCLK	Low-level Input Voltage	V	-0.30		0.54	0.051	0.059	0.08	Pass	VIL-MCLK
LRCLK	fLRCLK	Frequency	kHz	46.56	48	49.44	47.998	47.999	48.001	Pass	fLRCLK
	tLRCLKH	High Time(μs)	us	9.79		11.04	10.416	10.417	10.417	Pass	tLRCLKH
	tLRCLKL	Low Time(μs)	us	9.79		11.04	10.417	10.417	10.418	Pass	tLRCLKL
	VIH-LRCLK	High-level Input Voltage	V	1.26		2.10	1.783	1.793	1.793	Pass	VIH-LRCLK
	VIL-LRCLK	Low-level Input Voltage	V	-0.30		0.54	0.012	0.012	0.012	Pass	VIL-LRCLK
SCLK	fBCLK	Frequency	MHz	2.92	3.072	3.23	3.0698	3.072	3.0736	Pass	fBCLK
	dBCLK	BCLK Duty Cycle	%	45.00		55.00	49.98	49.994	50.02	Pass	dBCLK
	t <sub>sclk</sub>	sclk pulse width high	ns	113.93		211.59	162.65	162.75	162.85	Pass	t <sub>sclk</sub>
	t <sub>lsclk</sub>	sclk pulse width low	ns	113.93		211.59	162.70	162.78	162.90	Pass	t <sub>lsclk</sub>
	VIH-BCLK	High-level Input Voltage	V	1.26		2.10	1.741	1.7528	1.759	Pass	VIH-BCLK
	VIL-BCLK	Low-level Input Voltage	V	-0.30		0.54	0.033	0.042	0.042	Pass	VIL-BCLK
SDO	VIH-SDO	High-level Input Voltage	V	1.26		2.10	1.809	1.818	1.818	Pass	VIH-SDO
	VIL-SDO	Low-level Input Voltage	V	-0.30		0.54	-0.009	0.000	0.000	Pass	VIL-SDO
SDI	VOH-SDI	CPU High-level Input Voltage	V	1.26		2.10	1.760	1.769	1.769	Pass	VOH-SDI
	VOL-SDI	CPU Low-level Input Voltage	V	-0.30		0.54	-0.002	0.002	0.007	Pass	VOL-SDI
Timing	t <sub>od_sclk2irok</sub>	i2s <sub>x</sub> _lrck_rx/i2s <sub>x</sub> _lrck_tx delay time from i2s <sub>x</sub> _sclk falling edge	ns	-162.76		97.66	1.5		1.92	Pass	t <sub>od_sclk2irok</sub>
	t <sub>susdi</sub>	i2s <sub>x</sub> _sdi setup time to i2s <sub>x</sub> _sclk rising edge	ns	85.10		-	94			Pass	t <sub>susdi</sub>
	t <sub>heldi</sub>	i2s <sub>x</sub> _sdi hold time from i2s <sub>x</sub> _sclk rising edge	ns	81.38		-	187.5			Pass	t <sub>heldi</sub>
	t <sub>od_sclk2sdo</sub>	i2s <sub>x</sub> _sdo propagation delay from i2s <sub>x</sub> _sclk falling edge	ns	-81.38		97.66	1.93		3.95	Pass	t <sub>od_sclk2sdo</sub>

指标根据  
CPU规格书  
填写

Jitter	Tj-MCLK	MCLK Total Jitter	ns	-		3.00			0.17	Pass	<u>Tj-MCLK</u>	
	Tj-BCLK	MCLK Total Jitter	ns	-		3.00			0.41	Pass	<u>Tj-BCLK</u>	

## 22.PDM



### PDM 1.8V

PDM_1.8V SI Test Report										
PDM Signal Integrity and Timing Analysis										
Power supply (V)										
1.7-1.95	NOTE: The test points need to be at the far end of the signal output.									
Signal Name	Description	Test item	Unit	Limited	Measure	Test Result	Waveform			
CLK	Frequency of PDM_CLK	fCLK	MHz	1.024	6.144	3.0703	3.072	3.0731	Pass	fCLK
	Duty cycle of PDM_CLK	Tduty	%	45	55	49.95	49.978	50.00	Pass	Tduty
	CLK Rise Time	tR_CLK	ns	20	-	-	-	2.50	Pass	tR_CLK
	CLK Fall Time	tF_CLK		20	-	-	-	2.55	Pass	tF_CLK
SDI	Input SDI hold time to PDM_CLK rising edge	thdp	ns	0	39.6	-	-	-	Pass	thdp
	Input SDI setup time to PDM_CLK rising edge	tsup		16.1	96	-	-	-	Pass	tsup
	Input SDI hold time to PDM_CLK falling edge	thdn		0	38.8	-	-	-	Pass	thdn
	Input SDI setup time to PDM_CLK falling edge	tsun		16.1	94.4	-	-	-	Pass	tsun
Voltage	CLK low level input voltage	VIL_CLK	V	0.54	0	-	0.01	Pass	VIL_CLK	
	CLK high level input voltage	VIH_CLK		1.26	1.76	-	1.77	Pass	VIH_CLK	
	SDI low level input voltage at rising edge	VIL_SDI		0.54	0.03	-	0.04	Pass	VIL_SDI	
	SDI high level input voltage at rising edge	VIH_SDI		1.26	1.67	-	1.68	Pass	VIH_SDI	

### PDM 3.3V

PDM1_3.3V SI Test Report										
PDM Signal Integrity and Timing Analysis										
Power supply (V)										
2.7-3.6	NOTE: The test points need to be at the far end of the signal output.									
Signal Name	Description	Test item	Unit	Limited	Measure	Test Result	Waveform			
CLK	Frequency of PDM_CLK	fCLK	MHz	1.024	6.144	3.0703	3.072	3.0736	Pass	fCLK
	Duty cycle of PDM_CLK	Tduty	%	45	55	49.95	49.982	50.02	Pass	Tduty
	CLK Rise Time	tR_CLK	ns	20	-	-	-	2.55	Pass	tR_CLK
	CLK Fall Time	tF_CLK		20	-	-	-	2.45	Pass	tF_CLK
SDI	Input SDI hold time to PDM_CLK rising edge	thdp	ns	0	18.66	-	-	-	Pass	thdp
	Input SDI setup time to PDM_CLK rising edge	tsup		16.1	131.6	-	-	-	Pass	tsup
	Input SDI hold time to PDM_CLK falling edge	thdn		0	18.4	-	-	-	Pass	thdn
	Input SDI setup time to PDM_CLK falling edge	tsun		16.1	130.6	-	-	-	Pass	tsun
Voltage	CLK low level input voltage	VIL_CLK	V	0.8	0	-	0.02	Pass	VIL_CLK	
	CLK high level input voltage	VIH_CLK		2	3.22	-	3.24	Pass	VIH_CLK	
	SDI low level input voltage at rising edge	VIL_SDI		0.8	0.02	-	0.04	Pass	VIL_SDI	
	SDI high level input voltage at rising edge	VIH_SDI		2	3.12	-	3.14	Pass	VIH_SDI	

## I2C Test Report

Operation Mode	Pullup (KΩ)	Power supply (V)	NOTE: Please fill out the power supply first. The test points need to be at the far end of the signal output. Each test item relative to time must be measured at least three times.									
Signal Name	Description	Test item	Unit	Spec limited			Measure			Test Result	Waveform	Remark
				Min	Typical	Max	Min	Mean	Max			
I2C_SCL	Frequency	fCLK	KHz	0		100	98.8	98.8	98.8	Pass	fCLK	This is dictated by external components
	Rise Time of SCL	tR_SCL				1000	-	97		Pass	tR_SCL	
	Fall Time of SCL	tF_SCL				300	-	4.75		Pass	tF_SCL	
	High Time	tHIGH		4		-	4.96	-	-	Pass	tHIGH	
	Low Time	tLOW		4.7		-	5.05	-	-	Pass	tLOW	
I2C_SDA	Rise Time of SDA	tR_SDA	ns			1000	-	107		Pass	tR_SDA	
	Fall Time of SDA	tF_SDA				300	-	4.95		Pass	tF_SDA	
I2C_SCL&I2C_SDA	data valid time	tVD_DAT	us	-		3.45	-	2.075		Pass	tVD_DAT	
	data valid acknowledge time	tVD_ACK		-		3.45	-	0.176		Pass	tVD_ACK	
	Bus Free Time between STOP and START	tBUF		4.7		-	36.3	-	-	Pass	tBUF	
	START Hold Time	tHD_STA		4		-	15	-	-	Pass	tHD_STA	
	START Setup Time	tSU_STA		4.7		-	9.88	-	-	Pass	tSU_STA	
	STOP Setup Time	tSU_STO		4		-	4.97	-	-	Pass	tSU_STO	
	SDA Hold Time	tHD_DAT		0		3.45	1.87	1.955		Pass	tHD_DAT	Slave and Master Default
	SDA Setup Time	tSU_DAT		250		-	2970	-	-	Pass	tSU_DAT	
Signal level	LOW level input voltage of SCL	VIL_SCL	V	-0.5		0.54	0.04	0.049		Pass	VIL_SCL	
	HIGH level input voltage of SCL	VIH_SCL		1.26		2.3	1.76	1.774		Pass	VIH_SCL	
	LOW level input voltage of SDA	VIL_SDA		-0.5		0.54	0.05	0.058		Pass	VIL_SDA	
	HIGH level input voltage of SDA	VIH_SDA		1.26		2.3	1.77	1.783		Pass	VIH_SDA	