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ECE 508
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HW #2

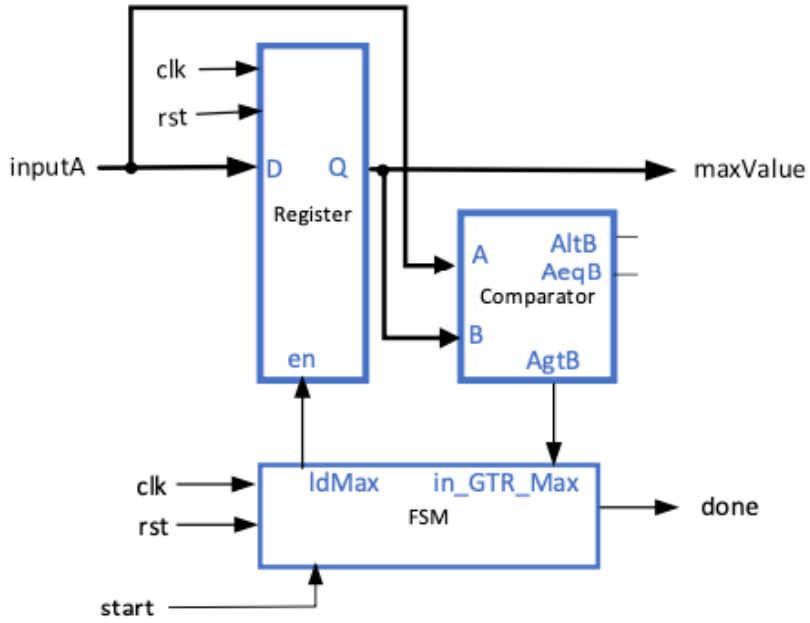

Figure 1: Block Diagram of Device Under Test (DUT) (From Original Spec)

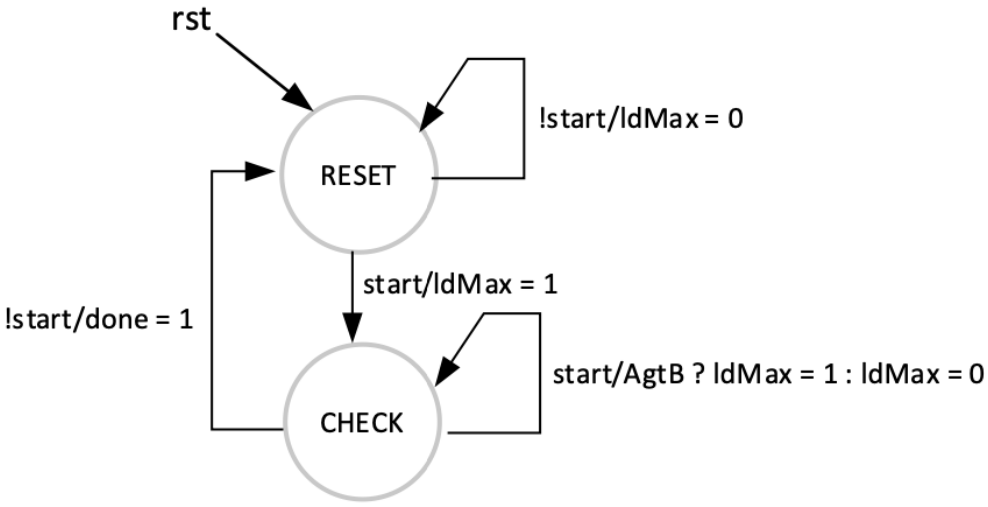

Figure 2: State Machine Given for Problem (From Original Spec)

Present State	Next State		Output ldMax			Output Done	
	Start = 0	Start = 1	Start = 0	Start = 1		Start = 0	Start = 1
RESET	RESET	CHECK	0	1		0	0
CHECK	RESET	CHECK	0	AgtB	!AgtB	1	0
				1	0		

Table 1: State Transition Diagram

Assign RESET to be state 0, and CHECK to be state 1 (This design requires only one flip flop for the state machine as there are only two states)

Present State	Next State		Output ldMax			Output Done	
	Start = 0	Start = 1	Start = 0	Start = 1		Start = 0	Start = 1
0	0	1	0	1		0	0
1	0	1	0	AgtB	!AgtB	1	0
				1	0		

Table 2: State Transition Diagram with State Assignment

From this it easy to create the FSM System Verilog code.

With these state assignments the logic is simple as well (when RESET = 0 and CHECK = 1)

Next State = Start
ldMax = ~State | State & Start & AgtB
Done = State & ~Start

Because of the simplicity of this design, and the flexibility of System Verilog, KMAP reduction checking is unnecessary, and this design as is can simply be implemented.

References:

Specification from canvas for block diagram and state machine diagram ‘ece508f22_hw2.pdf’