EE480 Assignment 1: Average Two 8-Bit Unsigned Binary Integers

Implementor's Notes

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ABSTRACT

This assignment served as an inaugural project for familiarization with verilog. It incorporated writing modules, reference 'oracles' and test benches, as well as methods to exhaustively test all parts.

1. GENERAL APPROACH

There are two operations necessary to complete the task assigned: addition, and division. Luckily, the division is by 2, so we are able to change the scope of valid bits to preform the task.

The addition was accomplished with 8 full adders assembled into one ripple carry adder. In order to round up, a one must be added onto the existing sum before division. This is done by feeding a `1` into the carry in of the ripple carry adder.

Bit slicing was preformed in order to accommodate the division, resulting in only looking at the high 7 bits. This however, limits our range. To ensure we can add numbers who's sum exceeds 255, the carry out from the ripple adder is set as the new MSB.

2. ISSUES

All 65536 test cases passed with no issues.

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