

Figure 3: Pixel generator RTL schematic

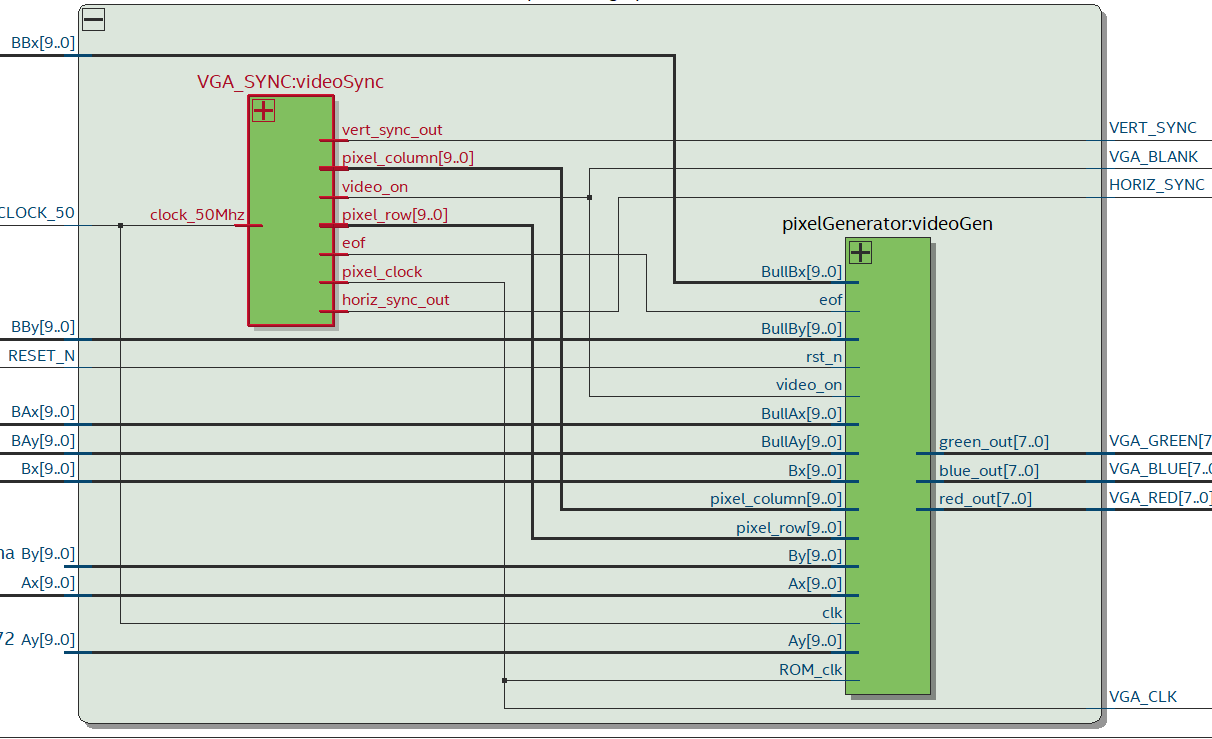


Figure 2: Graphics output RTL schematic

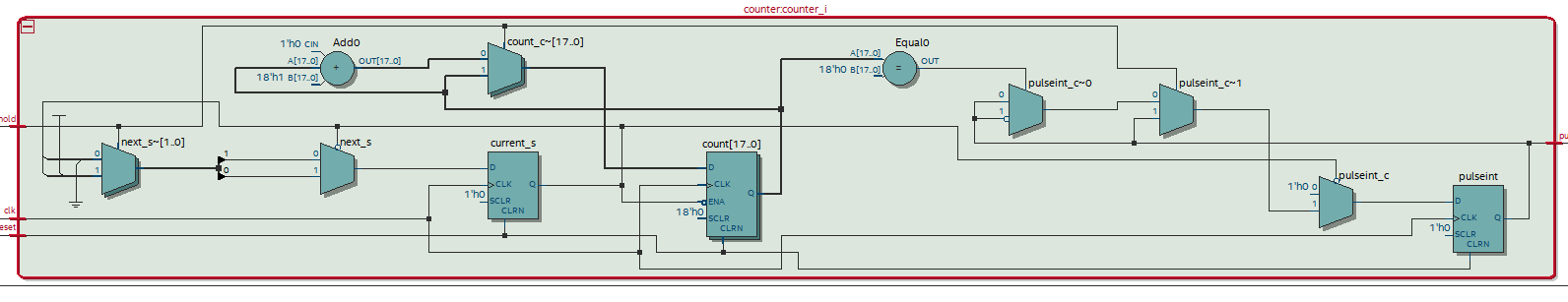


Figure 1: Counter RTL schematic

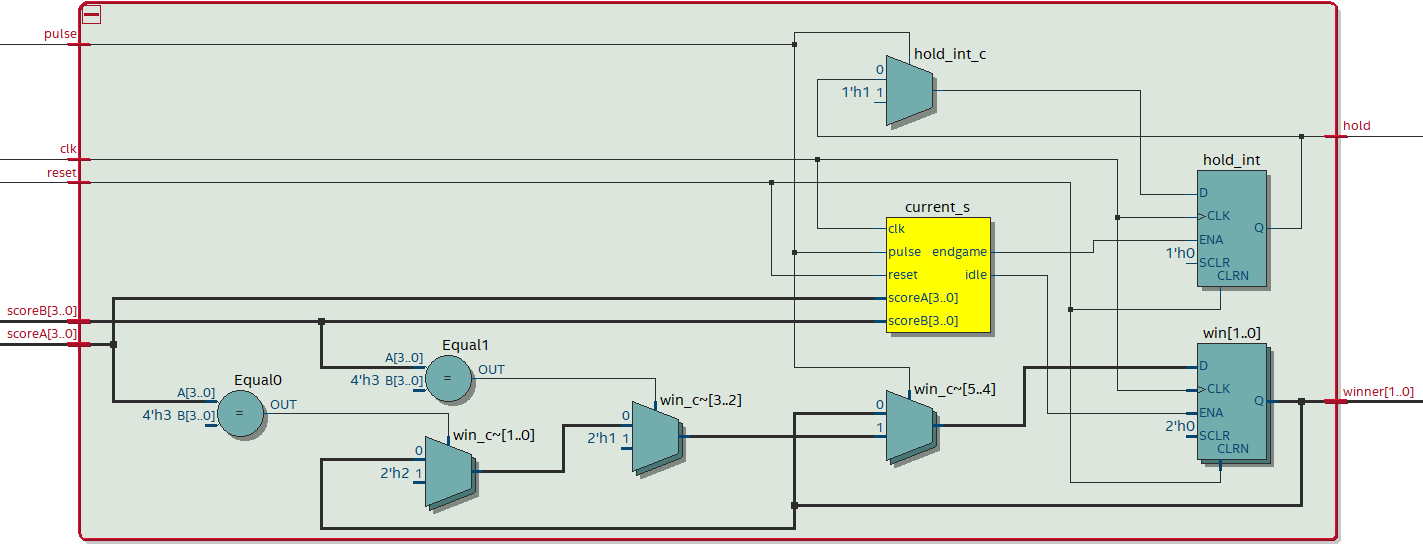


Figure 5: Win logic RTL schematic

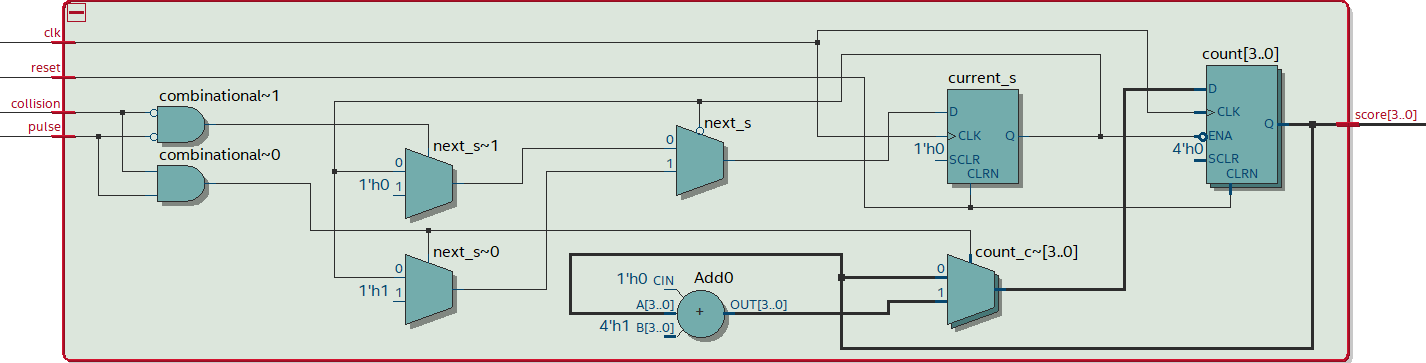


Figure 4: Score component RTL schematic

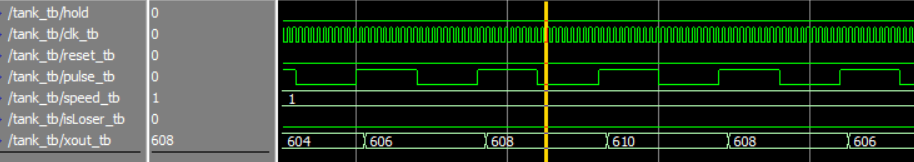


Figure 6: Tank ModelSim wave



Figure 7: Bullet ModelSim wave

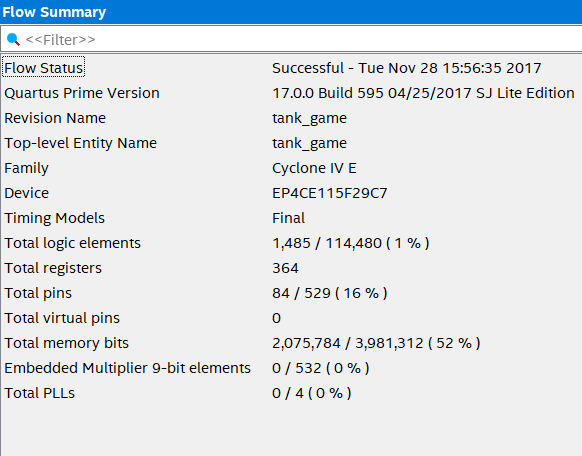


Figure 8: Flow summary showing resource usage