USB Certification for Stellaris® Microcontroller-based USB Peripherals and Embedded Host Systems

Application Note

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Introduction

This application note describes the USB Implementers Forum (USB-IF) certification process for a USB full-speed device and a USB full-speed embedded host system. The Stellaris® family of microcontrollers includes several parts with USB Device and USB Host capability. This application note describes this process using the certification of the Stellaris® LM3S5732 microcontroller as the example.

USB-IF

The Universal Serial Bus (USB) was initially created as a mechanism for connecting peripherals to personal computers, but it has grown into other uses including applications in the embedded world. For products to be USB-compliant, they must meet the USB Specification electrical and functionality requirements per the USB 2.0 standard published by USB-IF. The USB-IF provides a USB Compliance Program to ensure a standard level of acceptability. Products that pass the compliance program requirements are included in the USB Integrators List, which is available only to member companies and includes products meeting the requirements for USB certification. Once a product is in the USB Integrators List, a USB-IF Trademark License Agreement must be submitted for licensing of the USB logo. Information about the Compliance Program can be found at www.usb.org/developers/compliance/.

Products can be tested for compliance by either submitting the product to a USB-IF-sponsored compliance workshop or by submitting the product to a USB-IF-approved independent test lab. A list of approved labs is available at www.usb.org/developers/compliance/labs. For this application, the product was submitted to MCCI Corporation (www.mcci.com).

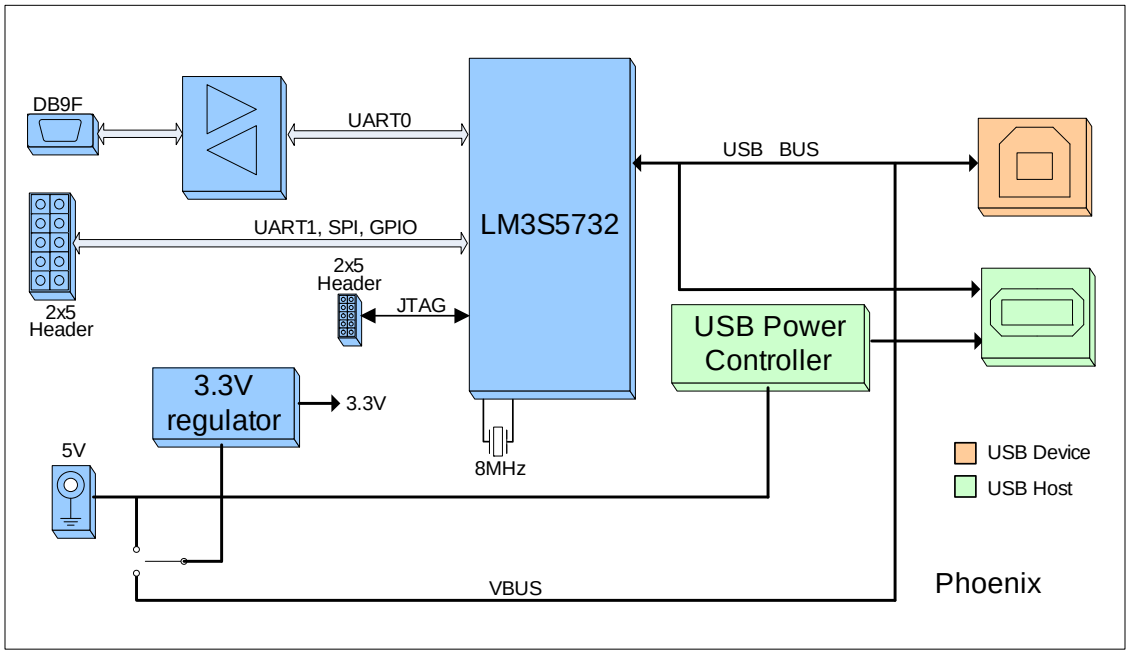
Phoenix USB Test Board

The Phoenix USB test board was built as a platform for silicon certification and board-level certification. In order to certify silicon, the board used to test the silicon must also be certified. All USB-IF requirements are the same for board and silicon certification, with silicon certification requiring an additional checklist. The Phoenix USB test board can be assembled as a USB Device (peripheral) or as a USB Embedded Host.

Block Diagram

The block diagram for the Phoenix USB test board is shown in Figure 1.

Figure 1. Phoenix USB Test Board Block Diagram



The microcontroller used is the Stellaris LM3S5732, which includes 128 Kbytes of Flash memory, 64 Kbytes of SRAM, and a USB 2.0 full-speed host/device controller in an LQFP64 package. An 8 MHz crystal is used to drive an internal PLL to generate all the required clocks for the microcontroller. The board uses 5-VDC power, and a switch selects the power source which can be an external supply or the USB Device bus connector. In addition to the USB port, the Phoenix board includes an RS-232 transceiver and DB9 female connector for a standard 115 kbps serial port. The board also has a JTAG connector for programming and debug and a 2x5 header providing additional I/O signals from the microcontroller.

USB Device

Phoenix USB Device assemblies do not include specific components for USB Host. The system application is a USB to RS-232 serial port bridge. Most personal computers today do not have serial ports, and so this bridge provides an easy way to add a serial port to a PC with an available USB port. After installing the driver, the bridge appears as **USB serial port (COMx)**, with x as the COM port number assigned. See the *"Product Submission Procedure for USB Device"* on page 6 for specific information on submitting a product to the USB-IF. The Phoenix USB Device schematic is shown on page 37. All specific components for USB Host are marked with a red X and are not fitted during board assembly. Note that resistors R4 and R17 are required for USB Device operation due to a silicon errata.

USB Embedded Host

Phoenix USB Host assemblies include a USB power controller, but do not include specific components for USB Device. See the *"Product Submission Procedure for USB Embedded Host"* on page 29 for specific information on submitting a product to the USB-IF. The Phoenix USB Host schematic is shown on page 29. All specific components for USB Device are marked with a red X and are not fitted during board assembly. Note that resistors R3 and R17 are required for USB Host operation due to a silicon errata.

Product Submission Procedure for USB Device

This section describes the submission procedure for USB Device compliance certification. This process has four main steps:

1. Checklist completion
2. Online registration
3. Test lab setup
4. Product testing

Checklist Completion

The first step should be to complete the *USB-Compliance Checklist Peripherals (Excluding Hubs)* form available at www.usb.org/developers/compliance. The checklist provides an assessment of product compliance Any problems at this stage must be resolved to ensure a successful compliance test. Note that all USB connectors, cables, and USB silicon used in the design must be on the Integrators List; otherwise, a checklist must also be provided for any component not on the list.

Online Registration

The product must be registered with the USB-IF at www.usb.org/kcompliance/members. Information about the product is submitted here, including the checklist completed in the previous step. At this stage, an independent test lab is selected. The USB-IF evaluates the application and if accepted, a product test ID (TID) is issued, and the application is sent to the test lab. In some cases, the USB-IF could request additional information before approval.

Test Lab Setup

Once the product application is received by the test lab, they contact the applicant to arrange for lab testing fees and product shipment. Two units are usually shipped with required power supplies, cables, software installation CDs, and documentation with installation instructions. If the unit can be reprogrammed, it is a good idea to ship the programming tools and instructions to avoid long delays if problems are found during testing that could be fixed by reprogramming.

Product Testing

The actual test procedure is described in the *USB-IF Full- and Low-Speed Electrical and Interoperability Compliance Test Procedure* (which can be found at: www.usb.org/developers/docs/USB-IFTestProc1_3.pdf). This document describes test procedures for systems, hubs, and peripherals. The test requirements include:

- Electrical tests
- Interoperability tests
- Functional tests

Recommendation: Read this document and pre-test as much as possible before submitting the product for testing. At a minimum, run the USB command verifier tool (USBCV), which evaluates a USB Device's conformance to the USB Device Framework, on the target device. This tool runs on a Windows PC and requires that the target device connect to a USB 2.0 high-speed hub connected to the host PC. This tool can be found at www.usb.org/developers/tools.

USB Device Test Results

This section provides the Phoenix USB test board results for a USB Device starting with Figure 2 on page 8 through Figure 5 on page 11. Figure 6 on page 12 shows the Phoenix USB Test Board Full-Speed Signal Quality Test Results and Figure 7 on page 13 shows the Phoenix USB Device Full-Speed Signals.

Figure 2. Phoenix USB Test Board Device Framework Results

USB Device Framework (Chapter 9) Tests
NUMBER OF TESTS: 13
RESULT: passed

InitializeTestSuite	
INFO Microsoft Windows XP (Build 2600) INFO Service Pack 3.0 INFO USBCommandVerifier.dll ver 1.3.2.0 INFO TestServices.dll ver 1.3.2.0 INFO StackSwitcher.dll ver 1.3.2.0	
DeviceDescriptorTest_DeviceConfigured	**Passed**
INFO Now Starting Test:Device Descriptor Test (Configuration Index 0) INFO Device descriptor length : 12 INFO Device descriptor type : 1 INFO Major version : 2 INFO Minor version : 0 INFO Device supports different class spec. on different interfaces : 2 INFO Device class code indicates [Communication] Device INFO Device sub class : 0 INFO Device protocol : 0 INFO Device MaxPacketSize0 : 40 INFO Vendor information for VendorID : 1cbe, Luminary Micro Inc. INFO Device ProductID : 2 INFO Device BCD : 100 INFO ENGLISH_US language string descriptor is : Luminary Micro Inc. INFO ENGLISH_US language string descriptor is : Virtual COM Port INFO ENGLISH_US language string descriptor is : 12345678 INFO Number of configurations device supports : 1 INFO Stopping Test [Device Descriptor Test (Configuration Index 0): Number of: Fails (0); Aborts (0); Warnings (0)]	
DeviceDescriptorTest_DeviceAddressed	**Passed**
INFO Now Starting Test:Device Descriptor Test (Configuration Index 0) INFO Device descriptor length : 12 INFO Device descriptor type : 1 INFO Major version : 2 INFO Minor version : 0 INFO Device supports different class spec. on different interfaces : 2 INFO Device class code indicates [Communication] Device INFO Device sub class : 0 INFO Device protocol : 0 INFO Device MaxPacketSize0 : 40 INFO Vendor information for VendorID : 1cbe, Luminary Micro Inc. INFO Device ProductID : 2 INFO Device BCD : 100 INFO ENGLISH_US language string descriptor is : Luminary Micro Inc. INFO ENGLISH_US language string descriptor is : Virtual COM Port INFO ENGLISH_US language string descriptor is : 12345678 INFO Number of configurations device supports : 1 INFO Stopping Test [Device Descriptor Test (Configuration Index 0): Number of: Fails (0); Aborts (0); Warnings (0)]	
ConfigDescriptorTest_DeviceConfigured	**Passed**
INFO Now Starting Test:Configuration Descriptor Test (Configuration Index 0) INFO Configuration descriptor contains descriptor of type : 24 INFO Configuration descriptor contains descriptor of type : 24 INFO Configuration descriptor contains descriptor of type : 24 INFO Number of interface descriptors found 1 INFO Number of alternate interface descriptors found : 0	

Figure 3. Phoenix USB Test Board Device Framework Results (continued)

```
INFO    Number of endpoint descriptors found : 3
INFO    Configuration descriptor length : 9
INFO    Configuration descriptor type : 2
INFO    Configuration descriptor TotalLength : 35
INFO    Configuration descriptor NumInterfaces : 1
INFO    Configuration descriptor ConfigurationValue: 1
INFO    ENGLISH_US           language string descriptor is : Self Powered Configuration
INFO    Configuration descriptor bmAttributes : c0
INFO    Device does not support remote wake up
INFO    Maximum power device requires : 0mA
INFO    Device is SELF-POWERED
INFO    Device is currently SELF POWERED
INFO    Currently remote wakeup is DISABLED
INFO    Stopping Test [ Configuration Descriptor Test (Configuration Index 0):
     Number of: Fails (0); Aborts (0); Warnings (0) ]
```

ConfigDescriptorTest_DeviceAddressed	**Passed**

```
INFO    Now Starting Test:Configuration Descriptor Test (Configuration Index 0)
INFO    Configuration descriptor contains descriptor of type : 24
INFO    Configuration descriptor contains descriptor of type : 24
INFO    Configuration descriptor contains descriptor of type : 24
INFO    Number of interface descriptors found 1
INFO    Number of alternate interface descriptors found : 0
INFO    Number of endpoint descriptors found : 3
INFO    Configuration descriptor length : 9
INFO    Configuration descriptor type : 2
INFO    Configuration descriptor TotalLength : 35
INFO    Configuration descriptor NumInterfaces : 1
INFO    Configuration descriptor ConfigurationValue: 1
INFO    ENGLISH_US           language string descriptor is : Self Powered Configuration
INFO    Configuration descriptor bmAttributes : c0
INFO    Device does not support remote wake up
INFO    Maximum power device requires : 0mA
INFO    Device is SELF-POWERED
INFO    Device is currently SELF POWERED
INFO    Currently remote wakeup is DISABLED
INFO    Stopping Test [ Configuration Descriptor Test (Configuration Index 0):
     Number of: Fails (0); Aborts (0); Warnings (0) ]
```

InterfaceDescriptorTest	**Passed**

```
INFO    Now Starting Test:Interface Descriptor Test (Configuration Index 0)
INFO    Bandwidth check passed
INFO    Testing Interface number : 0 Alternate setting : 0
INFO    Interface descriptor length : 9
INFO    Interface descriptor bDescriptorType : 4
INFO    Interface descriptor bAlternateSetting : 0
INFO    Interface descriptor bNumEndPoints: 3
INFO    Interface descriptor bInterfaceClass reserved for assignment by the USB-IF : 2
INFO    Interface class code indicates [CDC-Control] Interface
INFO    Interface descriptor bInterfaceSubClass : 2
INFO    Device does not use a class-specific protocol on this interface
INFO    ENGLISH_US           language string descriptor is : ACM Control Interface
INFO    Stopping Test [ Interface Descriptor Test (Configuration Index 0):
     Number of: Fails (0); Aborts (0); Warnings (0) ]
```

EndpointDescriptorTest_DeviceConfigured	**Passed**

```
INFO    Now Starting Test:Endpoint Descriptor Test (Configuration Index 0)
INFO    Testing Interface number : 0 Alternate setting : 0
INFO    Endpoint descriptor length : 7
INFO    Endpoint descriptor type : 5
INFO    Endpoint Type : Interrupt, Number : 1, Direction : IN
INFO    Endpoint descriptor bmAttributes : 3
```

Figure 4. Phoenix USB Test Board Device Framework Results (continued)

```
INFO    Endpoint descriptor raw MaxPacketSize : 10
INFO    Endpoint descriptor interval : a
INFO    Endpoint descriptor length : 7
INFO    Endpoint descriptor type : 5
INFO    Endpoint Type : Bulk, Number : 2, Direction : IN
INFO    Endpoint descriptor bmAttributes : 2
INFO    Endpoint descriptor raw MaxPacketSize : 40
INFO    Endpoint descriptor interval : 0
INFO    Endpoint descriptor length : 7
INFO    Endpoint descriptor type : 5
INFO    Endpoint Type : Bulk, Number : 3, Direction : OUT
INFO    Endpoint descriptor bmAttributes : 2
INFO    Endpoint descriptor raw MaxPacketSize : 40
INFO    Endpoint descriptor interval : 0
INFO    Stopping Test [ Endpoint Descriptor Test (Configuration Index 0):
     Number of: Fails (0); Aborts (0); Warnings (0) ]
```

EndpointDescriptorTest_DeviceAddressed	**Passed**

```
INFO    Now Starting Test:Endpoint Descriptor Test (Configuration Index 0)
INFO    Testing Interface number : 0 Alternate setting : 0
INFO    Endpoint descriptor length : 7
INFO    Endpoint descriptor type : 5
INFO    Endpoint Type : Interrupt, Number : 1, Direction : IN
INFO    Endpoint descriptor bmAttributes : 3
INFO    Endpoint descriptor raw MaxPacketSize : 10
INFO    Endpoint descriptor interval : a
INFO    Endpoint descriptor length : 7
INFO    Endpoint descriptor type : 5
INFO    Endpoint Type : Bulk, Number : 2, Direction : IN
INFO    Endpoint descriptor bmAttributes : 2
INFO    Endpoint descriptor raw MaxPacketSize : 40
INFO    Endpoint descriptor interval : 0
INFO    Endpoint descriptor length : 7
INFO    Endpoint descriptor type : 5
INFO    Endpoint Type : Bulk, Number : 3, Direction : OUT
INFO    Endpoint descriptor bmAttributes : 2
INFO    Endpoint descriptor raw MaxPacketSize : 40
INFO    Endpoint descriptor interval : 0
INFO    Stopping Test [ Endpoint Descriptor Test (Configuration Index 0):
     Number of: Fails (0); Aborts (0); Warnings (0) ]
```

HaltEndpointTest	**Passed**

```
INFO    Now Starting Test:Halt Endpoint Test (Configuration Index 0)
INFO    Testing Interface number : 0 Alternate setting : 0
INFO    Testing EndPoint type : Interrupt, Address : 81
INFO    Endpoint is currently not halted
INFO    Endpoint is halted
INFO    Cleared endpoint halt
INFO    Testing EndPoint type : Bulk, Address : 82
INFO    Endpoint is currently not halted
INFO    Endpoint is halted
INFO    Cleared endpoint halt
INFO    Testing EndPoint type : Bulk, Address : 3
INFO    Endpoint is currently not halted
INFO    Endpoint is halted
INFO    Cleared endpoint halt
INFO    Stopping Test [ Halt Endpoint Test (Configuration Index 0):
     Number of: Fails (0); Aborts (0); Warnings (0) ]
```

SetConfigurationTest	**Passed**

```
INFO    Now Starting Test:SetConfiguration Test (Configuration Index 0)
INFO    SetConfiguration with configuration value : 1
```

Figure 5. Phoenix USB Test Board Device Framework Results (continued)

```
INFO    Unconfigured the device
INFO    SetConfiguration with configuration value : 1
INFO    Stopping Test [ SetConfiguration Test (Configuration Index 0):
     Number of: Fails (0); Aborts (0); Warnings (0) ]
```

SuspendResumeTest	**Passed**

```
INFO    Now Starting Test:Suspend/Resume Test (Configuration Index 0)
INFO    Suspended the parent port of the device
INFO    Stopping Test [ Suspend/Resume Test (Configuration Index 0):
     Number of: Fails (0); Aborts (0); Warnings (0) ]
```

RemoteWakeupTestEnabled	**Passed**

```
INFO    Now Starting Test:Remote Wakeup Test (Configuration Index 0)
INFO    The device does not support remote wakeup
INFO    Stopping Test [ Remote Wakeup Test (Configuration Index 0):
     Number of: Fails (0); Aborts (0); Warnings (0) ]
```

RemoteWakeupTestDisabled	**Passed**

```
INFO    Now Starting Test:Remote Wakeup Test (Configuration Index 0)
INFO    The device does not support remote wakeup
INFO    Stopping Test [ Remote Wakeup Test (Configuration Index 0):
     Number of: Fails (0); Aborts (0); Warnings (0) ]
```

EnumerationTest	**Passed**

```
INFO    Now Starting Test:Enumeration Test (repeat 150 times)
INFO    Device speed is Full
INFO    Stopping Test [ Enumeration Test (repeat 150 times):
     Number of: Fails (0); Aborts (0); Warnings (0) ]
```

Summary

```
INFO    Summary Log Counts [ Fails (0); Aborts (0); Warnings (0) ]
```

Figure 6. Phoenix USB Test Board Full-Speed Signal Quality Test Results

Full Speed Signal Quality Test Results for T713_LuminaryMicro_StellarisLM3S5732-rA_T-USBET_UsFs-sqc-01

For details on test setup, methodology, and performance criteria, please consult the signal quality test description at the USB-IF Compliance Program web page.

Required Tests

- Overall result: pass!

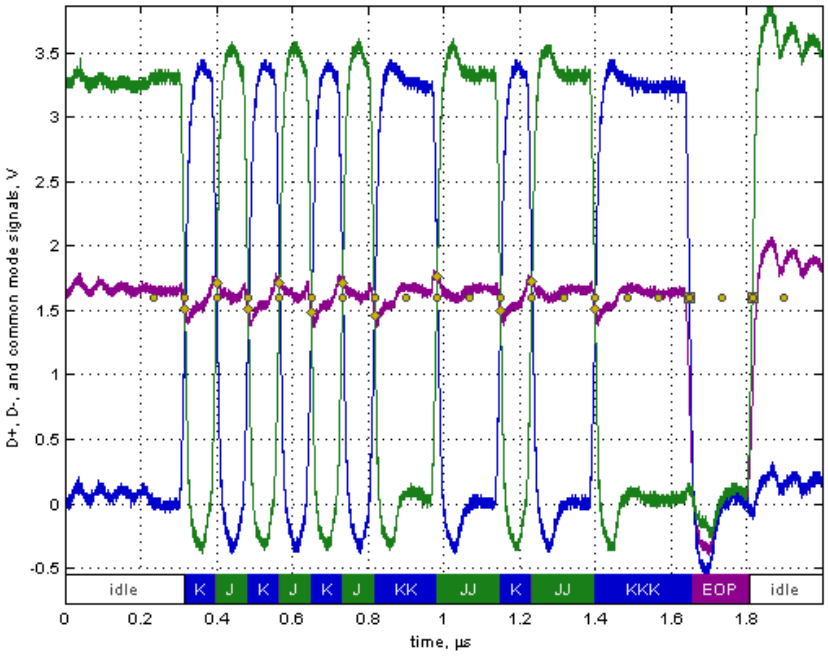
- Signal eye:
  eye passes
- EOP width: 165.35 ns
  EOP width passes
- Measured signaling rate: 12.0031 MHz
  signal rate passes
- Crossover voltage range: 1.46 V to 1.76 V, mean crossover 1.60 V
  (first crossover at 1.52 V, 10 other differential crossovers checked)
  crossover voltages pass
- Consecutive jitter range: -699.634 ps to 656.259 ps, RMS jitter 481.842 ps
  Paired JK jitter range: -158.641 ps to 140.808 ps, RMS jitter 149.990 ps
  Paired KJ jitter range: -310.214 ps to 481.647 ps, RMS jitter 299.756 ps
  jitter passes

Additional Information

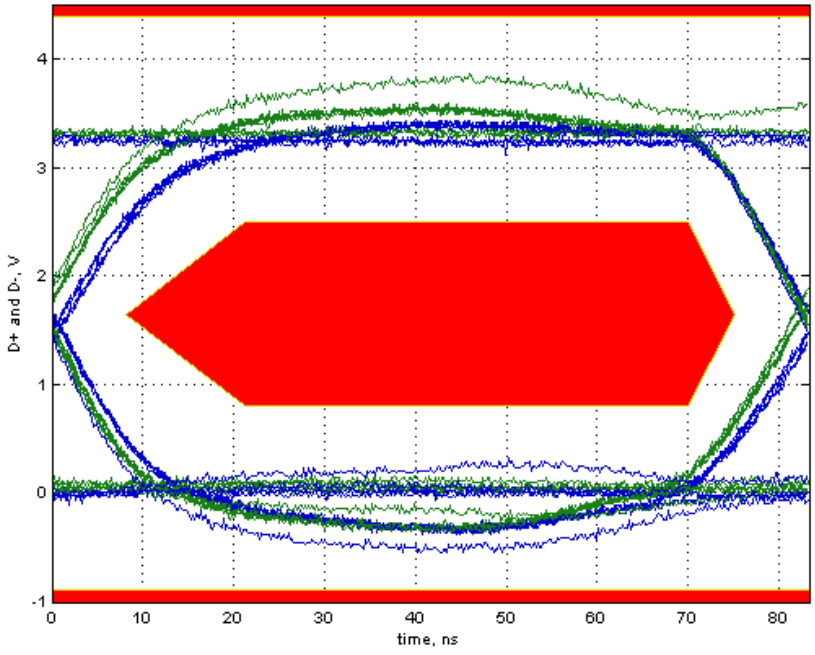
- Rising Edge Rate: 137.80 V/us (Equivalent risetime = 19.16 ns)
  (minimum 132.00 V/us, maximum 660.00 V/us)
- Falling Edge Rate: 137.75 V/us (Equivalent risetime = 19.16 ns)
  (minimum 132.00 V/us, maximum 660.00 V/us)
- Edge Rate Match: 0.04% (limit +/-10%)

Figure 7. Phoenix USB Device Full-Speed Signals

USB Signal Data



USB Data Eye



USB 2.0 Compliance Checklist Sample for Phoenix USB Test Board

The following section contains the specific pages for the USB 2.0 Compliance Checklist as it was completed for the Phoenix USB test board (see Figure 8 on page 15 through Figure 21 on page 28).

Figure 8. Phoenix USB Test Board Compliance Checklist Sample

1 Introduction

This checklist helps designers of USB peripherals to assess their products' compliance with the Universal Serial Bus Specification, Revision 2.0. Unless explicitly stated otherwise, all references to the USB Specification refer to Revision 2.0.

This checklist is also used, in part, to qualify a USB peripheral for the USB-IF Integrators List. This document and other USB compliance tools, including USB Check, are available in the developers section of the USB-IF's website, http://www.usb.org/developers/. The compliance checklists are updated periodically, so developers should check for updates when starting new projects.

Section 5, Recommended Questions, contains questions covering areas not required by the USB Specification. Answering these questions is not a requirement for compliance with the Specification or acceptance to the Integrators List. However, vendors are strongly encouraged to take these questions into consideration when designing their products.

Questions or comments regarding the Integrators List, Compliance Workshop testing results, or checklist submissions should be sent to admin@usb.org. If you have questions regarding the checklist itself, feel it fails to adequately cover an aspect of the USB specification, have found an error, or would like to propose a question, please contact the USB-IF at checklists@usb.org.

1.1 General Notes

All voltages are referenced to the device's USB ground.

2 Mechanical Design and Layout

ID	question
M1	What is the manufacture and model identifier of the connectors or cables used with this peripheral? Manufacturer: Molex USB B connector Model: 67068-8000 If the connectors or cables used in this peripheral are **NOT** listed on the USB Integrators List attach Connector and Cable Assembly checklists covering this peripheral's connectors and cable assemblies.
M2	What is the manufacture and model identifier of the USB silicon used in this peripheral? Manufacturer: Luminary Micro Model: LM3S5732 If the silicon used in this peripheral is **NOT** listed on the USB Integrators List attach a Peripheral Silicon checklist covering this peripheral's USB silicon.

Device vendors are strongly encouraged to review the Connector and Cable Assembly and Peripheral Silicon checklists regardless of whether or not their device's cabling, connectors, and silicon appear on the Integrators List.

ID	question	response	sections in spec
M3	Can the device's data lines withstand voltages between –1.0 and 4.6V	yes ☑ no ☐	7.1.1

Figure 9. Phoenix USB Test Board Compliance Checklist Sample (continued)

	applied with a source impedance of 39Ω ±2% for up to 100ns?		
M4	When tri-stated, can either data line be continuously shorted to V_{BUS}, GND, the other data line, or the connector's shield without damage occurring?	yes☑ no☐	7.1.1
M5	When driving 50% of the time, can either data line be shorted to V_{BUS}, GND, the other data line, or the connector's shield without damage occurring?	yes☑ no☐	7.1.1
M6	Do the D+ and D- traces present a characteristic impedance of 45Ω ±15% to GND and a differential impedance of 90Ω ±15%, between the device's cable connection and termination resistors?	yes☑ no☐	7.1.6
M7	If edge rate control capacitors are used: Are they located between the transciever pins and the device's termination resistors? Is their capacitance less than 75pF and balanced within 10%?	 yes☐ no☐ yes☐ no☐	7.1.6
M8	Are the device's receivers and transmitters within 1ns of its cable connection?	yes☑ no☐	7.1.16
M9	Does the device present sufficient capacitance between V_{BUS} and GND to prevent adverse effects from flyback voltages when its cable is disconnected? (A minimum of 1.0µF is recommended.)	yes☑ no☐	7.2.4.2

2.1 Low-Speed Devices

(not applicable to full-speed devices)

MLS1	Does the device have a captive cable?	yes☐ no☐	7.1.1.2
MLS2	Does the device pull up D-?	yes☐ no☐	7.1.5
MLS3	Does the device, with its captive cable, present a single-ended capacitance between 200 and 450pF on the D+ and D- lines?	yes☐ no☐	7.1.1.2
MLS4	Is the device's signaling rate 1.50Mb/s ±1.5%, even if the device uses spread spectrum clocking?	yes☐ no☐	7.1.11

2.2 Full-Speed Devices

(not applicable to low-speed devices)

MFS1	Does the device's source impedance remain in the shaded areas of Figure 7-4?	yes☑ no☐	7.1.1.1
MFS2	Does the device pull up D+?	yes☑ no☐	7.1.5
MFS3	Is the device's signaling rate 12.000Mb/s ±.25%, even if the device uses spread spectrum clocking?	yes☑ no☐	7.1.11

2.3 Tethered Devices

(not applicable to untethered devices)

Tethered devices are devices with a captive cable.

MT1	Does the captive cable have a series A plug?	yes☐ no☐	6.2
MT2	Does the device pull up the appropriate data line with a 1.5kΩ ±5% resistor attached to a voltage source between 3.0 and 3.6V or with a Thevénin source of at least 900Ω?	yes☐ no☐	7.1.5

2.4 Untethered Devices

(not applicable to tethered devices)

Figure 10. Phoenix USB Test Board Compliance Checklist Sample (continued)

Untethered devices are devices with a detachable cable.

MUT1	Does the device have a series B receptacle?	yes ☑ no ☐	6.2
MUT2	Does the device pull up D+ with a 1.5kΩ ±5% resistor attached to a voltage source between 3.0 and 3.6V?	yes ☑ no ☐	7.1.5
MUT3	Does the device's upstream port present 100pF or less on D+ and D-?	yes ☑ no ☐	7.1.6

3 Device States and Signals

D1	Can the device pull up the appropriate data line to at least 2.0V within 2.5µs?	yes ☑ no ☐	7.1.5
D2	Is the device's pullup active only when V_{BUS} is high?	yes ☑ no ☐	7.1.5
D3	Is the V_{BUS} switching threshold for the device's pullup control between 1.0V and 4.0V?	yes ☑ no ☐	7.1.5
D4	If the device is bus powered, or uses bus power to run any of its components, does it pull up the appropriate data line within 100ms of V_{BUS} exceeding 4.01V?	yes ☑ no ☐	7.1.5
D5	Does the device meet all power-on and connection timing requirements, as illustrated in Figure 7-29?	yes ☑ no ☐	7.1.7.3 7.3.2
D6	Does the device respond to a reset no sooner than 2.5µs and no later than 10ms after the SE0 begins?	yes ☑ no ☐	7.1.7.5
D7	Is the device's reset recovery time less than 10ms?	yes ☑ no ☐	7.1.7.5
D8	At the end of reset is the device in the default state?	yes ☑ no ☐	7.1.7.3 9.1.1
D9	Can the device correctly handle more than one USB RESET with no intervening packets?	yes ☑ no ☐	7.1.7.3
D10	Does the device begin the transition to its suspend state after its bus segment has been idle for 3ms, regardless of the device's state?	yes ☑ no ☐	7.1.7.4
D11	Has the device's power consumption dropped to its suspended value after the hub's upstream bus segment has been idle for 10ms?	yes ☑ no ☐	7.1.7.4
D12	When suspended, does the device recognize any non-idle state on the bus, excluding a reset, as a resume signal?	yes ☑ no ☐	7.1.7.5
D13	When suspended, does the device recognize a reset and act on the signal so that it enters the default state?	yes ☑ no ☐	7.1.7.5 7.1.7.3 9.1
D14	Does the device recognize a K→low-speed EOP→J transition on its upstream port as the end of resume signaling?	yes ☑ no ☐	7.1.7.7
D15	Is the device able to accept a SetAddress() request 10ms after resume is signaled?	yes ☑ no ☐	7.1.7.5
D16	Does the device complete its wakeup within 20ms?	yes ☑ no ☐	7.1.7.5
D17	Can the device function correctly with frame lengths between 995 and 1005µs?	yes ☑ no ☐	7.1.12
D18	Does the device function correctly on tier 6, when subjected to worst-case hub bit skews and delay times?	yes ☑ no ☐	7.1.14 7.1.19
D19	Does the device drive no signals upstream on power up?	yes ☑ no ☐	7.2.1
D20	Does the combination of the device's pullup and the 15kΩ ±5% pulldown resistor at the upstream port yield a voltage between 2.7 and 3.6V when the bus is idle?	yes ☑ no ☐	7.3.2
D21	Does the device complete SetAddress() or a standard request with no data in less than 50ms?	yes ☑ no ☐	7.3.2 9.2.6.3

Figure 11. Phoenix USB Test Board Compliance Checklist Sample (continued)

D22	Does the device deliver the first and all subsequent data packets, except for the last data packet, for a standard request within 500ms?	yes ☑ no ☐	7.3.2 9.2.6.4
D23	Does the device deliver the last data packet for a standard request within 50ms?	yes ☑ no ☐	7.3.2 9.2.6.4
D24	Does the device pass a full Chapter 9 test, as performed by USB Check?	yes ☑ no ☐	Chapters 8 and 9
D25	Does the device implement a default control endpoint 0 for all addresses?	yes ☑ no ☐	9.1.1.4
D26	Are the device's differential *and* single-ended USB signals within spec? Note: This test is especially important if ferrite beads or a common mode choke is used on the USB data lines, as these components often pose a significant signal integrity hazard.	yes ☑ no ☐	7.1.6

Device vendors are strongly encouraged to complete all bus transactions as quickly as is practical. See section 9.2.6.1 for details.

For details on testing USB signals, consult the USB-IF's signal quality test description, which can be downloaded from the USB-IF Compliance Program webpage.

3.1 Low-Speed Devices

(not applicable to full-speed devices)

LS1	Does a low-speed device implement the default control pipe and, at most, two interrupt endpoints?	yes ☐ no ☐	5.3.1.1
LS2	Does the device allow an interpacket delay of at least two low-speed bit times?	yes ☐ no ☐	7.1.18
LS3	Is the device's transaction timeout 16–18 low-speed bit times?	yes ☐ no ☐	7.1.19
LS4	Does the device recognize keep alive strobes and remain awake?	yes ☐ no ☐	11.8.4.1

3.2 Full-Speed Devices

(not applicable to low-speed devices)

FS1	Does the device allow an interpacket delay of at least two full-speed bit times?	yes ☑ no ☐	7.1.18
FS2	Is the device's transaction timeout 16–18 full-speed bit times?	yes ☑ no ☐	7.1.19
FS3	Does the device ignore low-speed packets?	yes ☑ no ☐	8.6.5

3.3 Remote Wakeup

(not applicable to devices which do not support remote wakeup)

W1	Does the device wait at least 5.0ms after its bus segment enters the idle state before sending a remote wakeup?	yes ☐ no ☐	7.1.7.5
W2	Does the device signal remote wakeup by driving K upstream for at least 1ms, but not more than 15m?	yes ☐ no ☐	7.1.7.5
W3	After driving K, does the device immediately tri-state its buffers without driving the bus to any non-K state?	yes ☐ no ☐	7.1.7.5
W4	Does the device send remote wakeups only when configured to do so?	yes ☐ no ☐	9.6.2

Figure 12. Phoenix USB Test Board Compliance Checklist Sample (continued)

4 Operating Voltages and Power Consumption

P1	Does the device source no current to V_{BUS} under any circumstance?	yes ☑ no ☐	7.2.1

4.1 Bus Power Consumption

(applicable to **all** devices, **including self powered devices**)

Note: the current allotted for a device consuming bus power encompasses all current drawn from V_{BUS}, including the power required to drive the device's upstream USB port. For details on testing USB device current consumption, please consult the USB-IF current test description, which can be downloaded from the USB-IF Compliance Program webpage.

4.1.1 Low-Power and Self Powered Devices

(not applicable to high power devices)

LP1	Is the MaxPower field in the device's configuration descriptor 100mA or less?	yes ☑ no ☐	7.2.1.3 9.6.2
LP2	Can the device operate in all states with a steady-state V_{BUS} of 4.35–5.25V?	yes ☑ no ☐	7.2.2
LP3	Can the device operate in all states with a transient V_{BUS} as low as 4.02V?	yes ☑ no ☐	7.2.2
LP4	Does the device draw the amount of current specified in its MaxPower field or less at all times, provided its V_{BUS} is between 4.02 and 5.25V?	yes ☑ no ☐	7.2.1.3
LP5	When the device is suspended, is its average current draw less than 500μA?	yes ☑ no ☐	7.2.3
LP6	If the device's current draw spikes during suspend, is the maximum spike height less than 100mA and is the spike's edge rate less than 100mA/μs for V_{BUS} between 4.02 and 5.25V?	yes ☑ no ☐	7.2.3
LP7	When the device wakes up from suspend, does it limit any inrush currents to 100mA or less?	yes ☑ no ☐	7.2.3
LP8	Does the device limit its inrush current, either by using capacitors smaller than 10μF or by using soft-start circuits, such that no more than 10μF of capacitance is charged by currents higher than 100mA when the device is hot plugged?	yes ☑ no ☐	7.2.4.1 7.2.3
LP9	Does the device draw no inrush current at configuration or when it transitions to its operating mode?	yes ☑ no ☐	7.2.4.1

4.1.2 High Power Devices

(not applicable to low-power and self powered devices)

HP1	Is the MaxPower field in the device's configuration descriptor 500mA or less?	yes ☐ no ☐	7.2.2
HP2	Can the device operate in its unconfigured state with a steady-state V_{BUS} of 4.35–5.25V?	yes ☐ no ☐	7.2.2
HP3	Can the device operate in its unconfigured state with a transient V_{BUS} as low as 4.02V?	yes ☐ no ☐	7.2.2
HP4	While unconfigured, does the device draw 100mA or less at all times, provided its V_{BUS} is between 4.02 and 5.25V?	yes ☐ no ☐	7.2.1.3
HP5	Can the device operate in its configured state with a steady-state V_{BUS} of 4.50–5.25V?	yes ☐ no ☐	7.2.2
HP6	Can the device operate in its configured state with a transient V_{BUS} as low as 4.17V?	yes ☐ no ☐	7.2.2
HP7	While configured, does the device draw the amount of current specified in its MaxPower field or less at all times, provided its V_{BUS} is between 4.02 and 5.25V?	yes ☐ no ☐	7.2.1.3
HP8	If the device does not support remote wakeup, the device is not configured,	yes ☐ no ☐	7.2.3

Figure 13. Phoenix USB Test Board Compliance Checklist Sample (continued)

	or remote wakeup is disabled, is the device's average suspend current draw less than 500µA?		
HP9	If the device supports remote wakeup, remote wakeup is enabled, and the device is configured, is the device's average suspend current draw less than 2.5mA?	yes ☐ no ☐	7.2.3
HP10	If the device's current draw spikes during suspend, is the maximum spike height less than 500mA and the spike's leading edge rate less than 100mA/µs for V_{BUS} between 4.02 and 5.25V?	yes ☐ no ☐	7.2.3
HP11	When the device wakes up from suspend, does it limit any inrush currents to 500mA or less?	yes ☐ no ☐	7.2.3
HP12	Does the device limit its inrush current, either by using capacitors smaller than 10µF or by using soft-start circuits, such that no more than 10µF of capacitance is charged: By currents higher than 100mA when the device is hot plugged? By currents higher than the device's MaxPower at configuration or when the device transitions to its operating mode?	 yes ☐ no ☐ yes ☐ no ☐	7.2.4.1 7.2.3

5 Recommended Questions

R1	Are the device's signal swings matched as closely as possible?	yes ☑ no ☐	7.1.2
R2	If ferrite beads are used in the device's USB connection, are they present on only the V_{BUS} and GND lines?	yes ☑ no ☐	7.1.6
R3	Does the device complete all commands as quickly as is practical?	yes ☑ no ☐	9.2.6.1
R4	If the device is self-powered and does not operate any of its components from bus power, does it only signal an attach when both bus power and external power are available?	yes ☑ no ☐	

Figure 14. Phoenix USB Test Board Compliance Checklist Sample (continued)

6 Explanations

This section should be used to explain any "no" answers or clarify answers on checklist items above. Please key entries to the appropriate checklist question.

M7 - no edge rate capacitors used
2.1 Low-Speed devices - not applicable, device is full speed only
2.3 Tethered devices - not applicable, device is untethered
3.3 Remote wakeup - remote wakeup not supported

Figure 15. Phoenix USB Test Board Compliance Checklist Sample (continued)

USB 2.0 Compliance Checklist — Peripheral Silicon (Excluding Hub Silicon)

LS12	Does the receiver accept an SE0 between 670ns and 1.76µs long, followed by a J, as an EOP?	yes☐ no☐	7.1.13.2
LS13	Does the receiver accept a packet whose first bit has been distorted by as much as ±25ns?	yes☐ no☐	7.1.14
LS14	Does the receiver accept a packet whose last bit has been lengthened by as much as 260ns (dribble bit)?	yes☐ no☐	7.1.14 7.1.9
LS15	Is the receiver data jitter tolerance at least ±141ns for consecutive transitions?	yes☐ no☐	7.1.15
LS16	Is the receiver jitter tolerance for paired transitions at least ±184ns?	yes☐ no☐	7.1.15
LS17	Is the device's turn-around time between two and 6.5 low-speed bit times, or 7.5 bit times if the device has a fixed cable?	yes☐ no☐	7.1.18
LS18	Is the time-out period 16–18 low-speed bit times?	yes☐ no☐	7.1.19
LS19	Is D- between 2.7 and 3.6V and D+ between 0.0 and 0.3V when the bus is idle?	yes☐ no☐	7.2.3

Note: the low-speed receiver jitter tolerances listed here do not apply to hosts and hubs. Consult section 7.1.15 for host and hub jitter requirements.

2.2 Full-Speed Ports

(applicable to any USB port which can operate at 12Mb/s)

FS1	With series termination resistors, does the device's source impedance remain in the shaded areas of Figure 7-3?	yes☑ no☐	7.1.1.1
FS2	Are data line rise times between 4.0 and 20ns when driving into a single-ended 50pF load?	yes☑ no☐	7.1.2
FS3	Are data line fall times between 4.0 and 20ns when driving into a single-ended 50pF load?	yes☑ no☐	7.1.2
FS4	Are the rise and fall times matched to within 10% for J→K transitions?	yes☑ no☐	7.1.2
FS5	Are the rise and fall times matched to within 10% for K→J transitions?	yes☑ no☐	7.1.2
FS6	Is a SE0 less than 14ns long ignored at all transitions in a bitstream?	yes☑ no☐	7.1.4
FS7	Is a SE1 less than 8ns long ignored at all transitions in a bitstream?	yes☑ no☐	
FS8	Does the device drive the J state at the end of an EOP for complete full-speed bit time?	yes☑ no☐	7.1.7
FS9	If the device tracks the K→low-speed EOP→J transition on its upstream port at the end of resume, does it correctly handle the low-speed EOP?	yes☑ no☐	7.1.7.5
FS10	Is the transmission data rate between 11.97 and 12.03Mb/s?	yes☑ no☐	7.1.11
FS11	Is the differential driver jitter for consecutive transitions less than ±2.0ns?	yes☑ no☐	7.1.13.1
FS12	Is the differential driver jitter for paired transitions less than ±1.0ns?	yes☑ no☐	7.1.13.1
FS13	Is the EOP width between 160ns and 175ns at the transmitter?	yes☑ no☐	7.1.13.2
FS14	Does the device accept an SE0 between 82ns and 250ns long, followed by a J, as an EOP?	yes☑ no☐	7.1.13.2 7.1.14
FS15	Does the receiver accept a packet whose first bit has been distorted by as much as ±25ns?	yes☑ no☐	7.1.14
FS16	Does the receiver accept a packet whose last bit has been lengthened by as much as 75ns?	yes☑ no☐	7.1.14 7.1.9
FS17	Is the receiver data jitter tolerance at least ±20.0 ns for consecutive transitions?	yes☑ no☐	7.1.15
FS18	Is the receiver jitter tolerance for paired transitions at least ±12.0 ns?	yes☑ no☐	7.1.15
FS19	Is the device's turn-around time between two and 6.5 full-speed bit times, or 7.5 bit times if the device has a fixed cable?	yes☑ no☐	7.1.18
FS20	Is the time-out period 18 full-speed bit times?	yes☑ no☐	7.1.19

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Figure 16. Phoenix USB Test Board Compliance Checklist Sample (continued)

FS21	Is D+ between 2.7 and 3.6V and D- between 0.0 and 0.3V when the bus is idle?	yes ☑ no ☐	7.2.3

3 Signaling Protocol and Error Handling

3.1 Bitstreams

B1	Is the possibility of both D+ and D- registering as NIB 1 during bus transitions accounted for?	yes ☑ no ☐	7.1.2 7.1.13.1
B2	Is the USB signaling either full-speed or low-speed but not both?	yes ☑ no ☐	7.1.5
B3	Does the sense of USB signaling correspond to the signaling speed?	yes ☑ no ☐	7.1.7
B4	Is the bitstream on the bus NRZI encoded?	yes ☑ no ☐	7.1.8
B5	Is bit stuffing performed on all data transmitted, including CRCs, prior to NRZI encoding?	yes ☑ no ☐	7.1.9 8.3.5
B6	Is bit stuffing performed even if the stuffed bit follows the last bit of a packet?	yes ☑ no ☐	7.1.9
B7	Is NRZI to NRZ decoding done before bit unstuffing?	yes ☑ no ☐	7.1.9
B8	Is bit unstuffing performed on all received data, including CRCs?	yes ☑ no ☐	7.1.9 8.3.5
B9	Is bit unstuffing done before the bitstream is parsed?	yes ☑ no ☐	7.1.9

3.2 Fields

A field is one of:

address	7 bit field
data	0 to 1023 byte field
data CRC	16 bit field
endpoint	4 bit field
EOP	3 bit field with NIB value 00J
frame number	11 bit field
PID	8 bit field, whose types are listed in section 8.3.1
SYNC	8 bit field with NZB value 00000001
token CRC	5 bit field

F1	Is the SYNC field, as measured on the bus wires, correct (NIB KJKJKJKK)?	yes ☑ no ☐	8.2
F2	Are all PIDs used among those listed in Table 8-1?	yes ☑ no ☐	8.3.1
F3	Are the PID check bits the ones complement of the packet type field?	yes ☑ no ☐	8.3.1
F4	Are the CRC generator's contents inverted and sent to the checker MSb first?	yes ☑ no ☐	8.3.5
F5	Is the token CRCs generated with the polynomial NZB 00101 on the ADDR and ENDP fields of IN, SETUP, and OUT tokens?	yes ☑ no ☐	8.3.5.1
F6	If all bits are received without error, does the CRC computation on a token or SOF leave a residual of NZB 01100 at the EOP?	yes ☑ no ☐	8.3.5.1
F7	Is the data CRC generated with the polynomial NZB 1000000000000101 on	yes ☑ no ☐	8.3.5.2

Figure 17. Phoenix USB Test Board Compliance Checklist Sample (continued)

setup0	*out1 out0 out1 ... out0/1*	in1
setup0	*in1 in0 in1 ... in0/1*	out1
setup0	in1	

Transactions in italics constitute the data stage. The suffix of 0 or 1 indicates the data PID used in the transaction.

TF1	Does the data stage always start with a data1 PID?	yes☑ no☐	8.5.2
TF2	Are all the transactions of the data stage in the same direction?	yes☑ no☐	8.5.2
TF3	Is there status stage's direction opposite that of the data stage?	yes☑ no☐	8.5.2
TF4	Is the data packet used in the status stage zero bytes in length?	yes☑ no☐	8.5.2

4 Recommended Questions

4.1 Device Robustness

4.1.1 Bitstreams

RB1	Is a single ended NIB 1 more than one bit time long ignored?	yes☑ no☐	
RB2	Does an agent ignore a truncated (up to 90%) first bit of the sync field without impacting the rest of the bitstream?	yes☑ no☐	
RB3	Is the state of the differential receiver ignored during single ended signaling?	yes☑ no☐	
RB4	Does the target reject bitstreams less than one bit time long without impacting future transactions?	yes☑ no☐	
RB5	Does the target adjust to the difference in frequency and phase between incoming clock and its internal clock?	yes☑ no☐	
RB6	Is a packet with a bit-stuff error rejected by the target?	yes☑ no☐	
RB7	Is a bitstream, which is not part of a packet, with bit stuff error ignored by the target?	yes☑ no☐	
RB8	Does the target reject packets with bit stuff error at the last bit of the packet?	yes☑ no☐	

4.1.2 Fields

RF1	Is the sync field recognized as valid even if the first two bits of it are corrupted? (Only the last 3 bits actually need to be decoded.)	yes☑ no☐	
RF1	Is a packet with packet type not listed in Table 8-1 ignored by the target	yes☑ no☐	
RF2	Is a packet with a corrupt PID (PID check error) ignored by the target?	yes☑ no☐	
RF3	Is a token with a bad CRC ignored by the target?	yes☑ no☐	
RF4	Is a CRC error on a data packet recognized by the target?	yes☑ no☐	

4.1.3 Packets

RP1	Is a token whose address field doesn't match any address in the device ignored by the device?	yes☑ no☐	
RP2	Is a token whose endpoint field doesn't match any endpoint in the address ignored by the device?	yes☑ no☐	
RP3	Is a token which doesn't match the direction of its target endpoint ignored	yes☑ no☐	

Figure 18. Phoenix USB Test Board Compliance Checklist Sample (continued)

	the data field of a data packet?		
F8	If all bits are received without error, does the CRC computation on the data field leave a residual of NZB 1000000000001101 at the EOP?	yes ☑ no ☐	8.3.5.2

3.3 Packets

A packet can be one of the following:

packet	fields comprising packet
data	SYNC PID data data CRC EOP
handshake	SYNC PID EOP
PRE	SYNC PID
SOF	SYNC PID frame number token CRC EOP
token	SYNC PID endpoint token CRC EOP

P1	Are all token packets 32 bits long and followed by an EOP?	yes ☑ no ☐	8.4.1
P2	Are all token packets of the form SYNC PID address endpoint token CRC EOP?	yes ☑ no ☐	8.4.1
P3	Are all data packets an integral number of bytes long (4 to 1027) excluding the EOP?	yes ☑ no ☐	8.4.3
P4	Is the data packet constituted as sync followed by PID followed by 0 to 1023 bytes of data followed by data CRC followed by EOP	yes ☑ no ☐	8.4.3
P5	Are all handshake packets 16 bits + EOP?	yes ☑ no ☐	8.4.4
P6	Are all handshake packets of the form SYNC PID EOP?	yes ☑ no ☐	8.4.4
P7	Is the data payload of a low-speed packet limited to a maximum of 8 bytes?	yes ☑ no ☐	8.6.5
P8	Is the PRE packet 16 bits long?	yes ☑ no ☐	8.6.5
P9	Does the PRE packet consist of only a SYNC followed by a PID?	yes ☑ no ☐	8.6.5

3.4 Transactions

Transactions are sets of packets used for unidirectional data transfer. Transactions are discussed in detail in section 8.5 of the USB Specification.

TA1	Does an isochronous endpoint synthesize frame markers to replace SOFs which may be lost due to bus error?	yes ☑ no ☐	5.10.6
TA2	Do handshakes conform to order of precedence described in section 8.4.5?	yes ☑ no ☐	8.4.5
TA3	Does the generated packet comply with the flows show in Figure 8-9, 8-11, 8-13, or 8-14, as appropriate?	yes ☑ no ☐	8.5 8.6.5
TA4	Is an unsuccessful (NAKed or timed-out in non-token phase) transaction retried?	yes ☑ no ☐	8.6
TA5	Does the retried transaction use the same data PID as the original transaction?	yes ☑ no ☐	8.6

3.5 Transfers

Transfers are data structures used by control endpoints. Each transfer is made up of setup and status stages, possibly with a data stage. Transfers can be one of:

Figure 19. Phoenix USB Test Board Compliance Checklist Sample (continued)

setup0	*out1 out0 out1 ... out0/1*	in1
setup0	*in1 in0 in1 ... in0/1*	out1
setup0	in1	

Transactions in italics constitute the data stage. The suffix of 0 or 1 indicates the data PID used in the transaction.

TF1	Does the data stage always start with a data1 PID?	yes☑ no☐	8.5.2
TF2	Are all the transactions of the data stage in the same direction?	yes☑ no☐	8.5.2
TF3	Is there status stage's direction opposite that of the data stage?	yes☑ no☐	8.5.2
TF4	Is the data packet used in the status stage zero bytes in length?	yes☑ no☐	8.5.2

4 Recommended Questions

4.1 Device Robustness

4.1.1 Bitstreams

RB1	Is a single ended NIB 1 more than one bit time long ignored?	yes☑ no☐	
RB2	Does an agent ignore a truncated (up to 90%) first bit of the sync field without impacting the rest of the bitstream?	yes☑ no☐	
RB3	Is the state of the differential receiver ignored during single ended signaling?	yes☑ no☐	
RB4	Does the target reject bitstreams less than one bit time long without impacting future transactions?	yes☑ no☐	
RB5	Does the target adjust to the difference in frequency and phase between incoming clock and its internal clock?	yes☑ no☐	
RB6	Is a packet with a bit-stuff error rejected by the target?	yes☑ no☐	
RB7	Is a bitstream, which is not part of a packet, with bit stuff error ignored by the target?	yes☑ no☐	
RB8	Does the target reject packets with bit stuff error at the last bit of the packet?	yes☑ no☐	

4.1.2 Fields

RF1	Is the sync field recognized as valid even if the first two bits of it are corrupted? (Only the last 3 bits actually need to be decoded.)	yes☑ no☐	
RF1	Is a packet with packet type not listed in Table 8-1 ignored by the target	yes☑ no☐	
RF2	Is a packet with a corrupt PID (PID check error) ignored by the target?	yes☑ no☐	
RF3	Is a token with a bad CRC ignored by the target?	yes☑ no☐	
RF4	Is a CRC error on a data packet recognized by the target?	yes☑ no☐	

4.1.3 Packets

RP1	Is a token whose address field doesn't match any address in the device ignored by the device?	yes☑ no☐	
RP2	Is a token whose endpoint field doesn't match any endpoint in the address ignored by the device?	yes☑ no☐	
RP3	Is a token which doesn't match the direction of its target endpoint ignored	yes☑ no☐	

Figure 20. Phoenix USB Test Board Compliance Checklist Sample (continued)

	by the device?		
RP4	Is a SETUP token to a unidirectional endpoint ignored by the device?	yes ☑ no ☐	
RP5	Is every endpoint capable of handling zero length data packets in its assigned directions?	yes ☑ no ☐	
RP6	Does an ISO endpoint use a zero length data packet if fresh frame data is not available?	yes ☑ no ☐	
RP7	Is a packet whose length doesn't match the standard length for the packet type rejected by target?	yes ☑ no ☐	
RP8	Does the measurement of packet length take into account the possibility of jitter and hub repeater skews in the EOP?	yes ☑ no ☐	
RP9	Is a bitstream that does not constitute a valid packet rejected by the target?	yes ☑ no ☐	
RP10	Are low-speed packets received by full-speed upstream ports ignored?	yes ☑ no ☐	8.6.5

4.1.4 Transactions

RTA1	Do all pipes in the device return to normal operation when the device resumes from suspend?	yes ☑ no ☐	
RTA2	Is a packet which doesn't fit the current phase of a transaction rejected by the target?	yes ☑ no ☐	
RTA3	Does the receipt of a token always start a new transaction and end a pending transaction?	yes ☑ no ☐	
RTA4	Is a data packet with same PID as the previous data packet to an endpoint ignored, other than ACKing the data packet?	yes ☑ no ☐	
RTA5	Does a time-out or error in any phase cause the transaction to be terminated?	yes ☑ no ☐	
RTA6	Is a transaction always started with a token?	yes ☑ no ☐	
RTA7	Is the data toggle implemented independently for each unidirectional endpoint?	yes ☑ no ☐	
RTA8	Does an isochronous data source ignore a handshake without impacting subsequent transactions?	yes ☑ no ☐	
RTA9	Can consecutive packets in the same direction be handled , provided there are two or more bit times of interpacket gap between each packet?	yes ☑ no ☐	

4.1.5 Transfers

RTF1	Does the receipt of a nonzero length data packet in the status stage cause the transfer to be terminated with an error indication?	yes ☑ no ☐	

Figure 21. Phoenix USB Test Board Compliance Checklist Sample (continued)

5 Explanations

This section should be used to explain any "no" answers or clarify answers on checklist items above. Please key entries to the appropriate checklist question.

Section 2.1 - Low Speed Ports is non-applicable. USB Device only works in full speed.

Product Submission Procedure for USB Embedded Host

This section describes the submission procedure for USB Embedded Host compliance certification. There are four main steps in this process:

1. Checklist completion
2. Online registration
3. Test lab setup
4. Test requirements

Checklist Completion

The USB Compliance Checklist for Systems, available at www.usb.org/developers/compliance must be submitted. The checklist provides an assessment of product compliance, and any problems at this stage must be resolved to ensure a successful compliance test. Note that USB connectors and cables used must be in the Integrator's List, otherwise a checklist must also be provided for the corresponding component not on the list. No additional checklist is required for silicon certification.

Online Registration

The product must be registered with the USB-IF at www.usb.org/kcompliance/members. Information about the product is submitted here, including the checklist completed in the previous step. An additional requirement is the submission of a Targeted Peripheral List (TPL), which is a list of the specific devices that the USB Embedded Host supports (see Table 1 on page 30). The USB-IF will evaluate the application and if accepted, a product test ID (TID) is issued and the application is sent to the test lab. In some cases, the USB-IF could request additional information before approval.

Test Lab Setup

Once the product application is received by the test lab, they contact the applicant to arrange for lab testing fees and product shipment. Two units are usually shipped with required power supplies, cables, software installation CDs, and documentation with installation instructions. If the unit can be reprogrammed, it is a good idea to ship the programming tools and instructions to avoid long delays if problems are found during testing that could be fixed by reprogramming.

Test Requirements

The test requirements are described in two documents:

- *Requirements and Recommendations for USB Products with Embedded Hosts and/or Receptacles*
- *USB-IF Embedded Host Compliance Plan*

A USB Embedded Host must source at least 8 mA on each downstream port. The Phoenix test board supports 100 mA on its downstream port.

USB Embedded Host Targeted Peripheral List

Embedded host systems only support a limited number of USB Devices as defined in the Targeted Peripheral List (TPL). The Phoenix USB Embedded Host has support for a USB low-speed and a USB full-speed mouse, with mouse X/Y delta movement and button press/release data transmitted over the serial port. Table 1 shows the targeted peripheral list for the Phoenix USB Embedded Host.

Table 1. Targeted Peripheral List for Phoenix USB Embedded Host

Class Name	Description	Class Code	Sub Class Code	Protocol	Specs Supported
HID	Supports USB mouse	03h	01h	02h	FS, LS
Devices Tested					
Manufacturer	Model	VendorID	ProductID	Description	Speed
Logitech	G5 laser mouse	46Dh	C049h	USB gaming mouse	FS

USB Embedded Host Test Results

This section provides the Phoenix USB test board results for a USB Embedded Host starting with Figure 22 on page 31 through Figure 23 on page 32. Figure 24 on page 33 shows the Phoenix USB Embedded Host Full-Speed Signals, Figure 25 on page 34 shows the Phoenix USB Test Board Embedded Host Low-Speed Test Results, and Figure 26 on page 35 shows the Phoenix USB Embedded Host Low-Speed Signals.

Figure 22.Phoenix USB Test Board Embedded Host Full-Speed Test Results

MCCI USB-IF Compliance Test Report

Full Speed Host Compliance Test Checklist

USB Silicon	result	notes
Vendor	PASS	Luminary Micro
Model	PASS	LM3S5732
Hardware	**result**	**notes**
Downstream Connection	PASS	A socket
User Interface	PASS	Hyperterminal Debug window
Maximum Power	**result**	**notes**
Power Source	PASS	device powers on

Signal Quality	Low	Full	High	notes
Host - Downstream - Port 1	PASS	PASS	N/A	

Interoperability

Host Interoperability		
Enum & Op - General	PASS	
Goldtree Op	PASS	
Hot Detach & Reattach	PASS	
Cold Boot	PASS	
Target Device Enumeration	PASS	
Target Device Operation	PASS	
Hot Attach & Reattach	PASS	
Power Cycle OTG DUT	PASS	
Enumerate 5 Hubs	PASS	

Target Peripheral List

Mice	PASS	Logitech, Kensinton, Microsoft Tested

Figure 23.Phoenix USB Test Board Embedded Host Full-Speed Test Results (continued)

Full Speed DS Hub Signal Quality Test
Results for T745_LuminaryMicro_LM3S5732_rA_USBET_fsu

For details on test setup, methodology, and performance criteria, please consult the signal quality test description at the USB-IF Compliance Program web page.

Required Tests

- Overall result: pass!

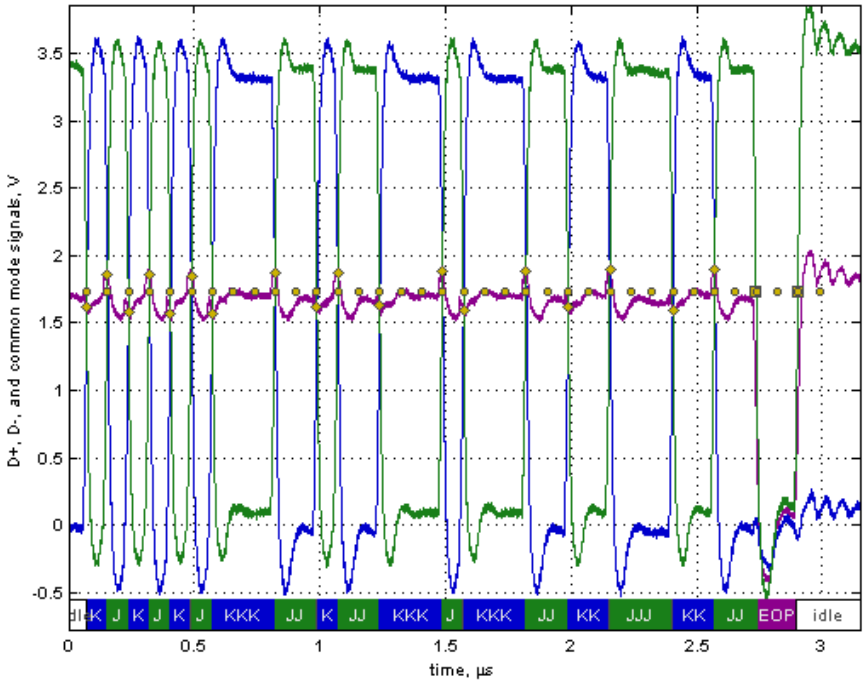
- Signal eye:
  eye passes
- EOP width: 166.85 ns
  EOP width passes
- Measured signaling rate: 12.0009 MHz
  signal rate passes
- Crossover voltage range: 1.57 V to 1.90 V, mean crossover 1.74 V
  (first crossover at 1.61 V, 17 other differential crossovers checked)
  crossover voltages pass
- Consecutive jitter range: -376.136 ps to 465.019 ps, RMS jitter 259.113 ps
  Paired JK jitter range: -288.141 ps to 457.097 ps, RMS jitter 254.084 ps
  Paired KJ jitter range: -99.747 ps to 225.611 ps, RMS jitter 127.087 ps
  jitter passes

Additional Information

- Rising Edge Rate: 133.45 V/us (Equivalent risetime = 19.78 ns)
  (minimum 132.00 V/us, maximum 660.00 V/us)
- Falling Edge Rate: 147.82 V/us (Equivalent risetime = 17.86 ns)
  (minimum 132.00 V/us, maximum 660.00 V/us)
- Edge Rate Match: 9.73% (limit +/-10%)

Figure 24.Phoenix USB Embedded Host Full-Speed Signals

Signal Data



Data Eye

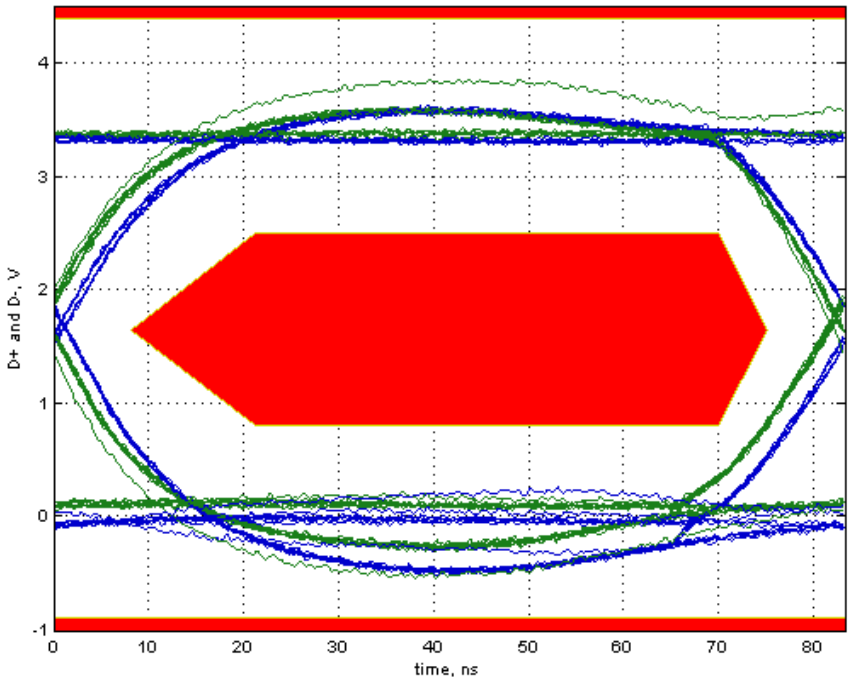


Figure 25.Phoenix USB Test Board Embedded Host Low-Speed Test Results

Low Speed DS Hub Signal Quality Test Results for T745_LuminaryMicro_LM3S5732_rA_USBET_lsu

For details on test setup, methodology, and performance criteria, please consult the signal quality test description at the USB-IF Compliance Program web page.

Required Tests

- Overall result: pass!

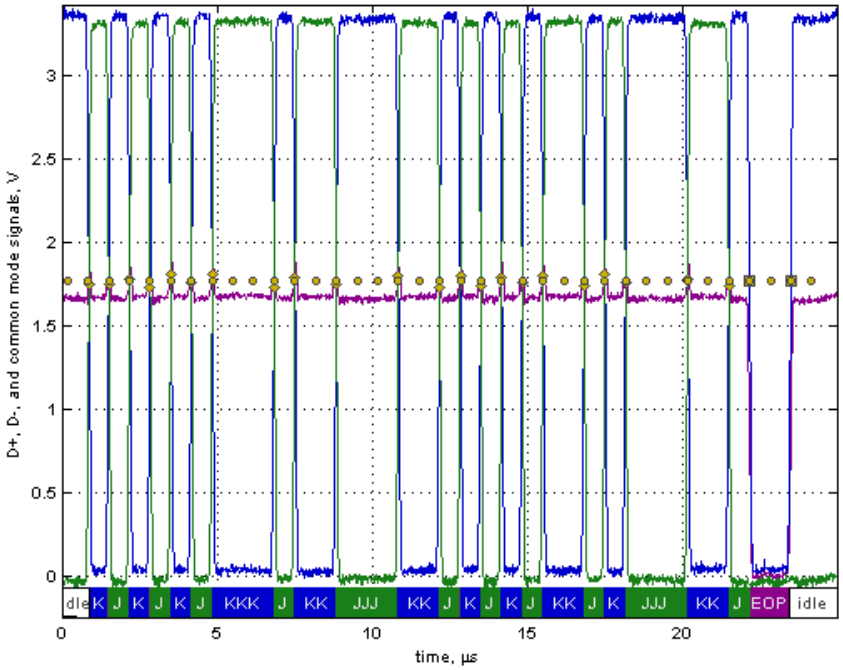
- Signal eye:
  eye passes
- EOP width: 1.33 µs
  EOP width passes
- Measured signaling rate: 1.4994 MHz
  signal rate passes
- Crossover voltage range: 1.73 V to 1.81 V, mean crossover 1.77 V
  (first crossover at 1.75 V, 21 other differential crossovers checked)
  crossover voltages pass
- Consecutive jitter range: -7.652 ns to 5.805 ns, RMS jitter 3.928 ns
  Paired JK jitter range: -0.883 ns to 1.945 ns, RMS jitter 1.177 ns
  Paired KJ jitter range: -2.259 ns to 2.254 ns, RMS jitter 1.705 ns
  jitter passes

Additional Information

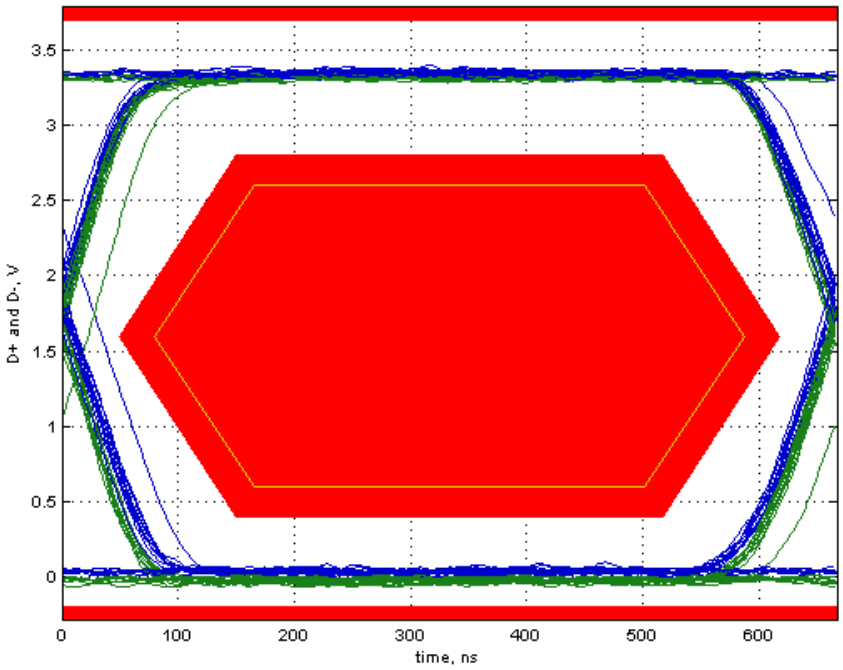
- Rising Edge Rate: 23.41 V/us (Equivalent risetime = 112.76 ns)
  (minimum 8.80 V/us, maximum 35.20 V/us)
- Falling Edge Rate: 22.33 V/us (Equivalent risetime = 118.21 ns)
  (minimum 8.80 V/us, maximum 35.20 V/us)
- Edge Rate Match: 4.83% (limit +/-20%)

Figure 26.Phoenix USB Embedded Host Low-Speed Signals

Signal Data

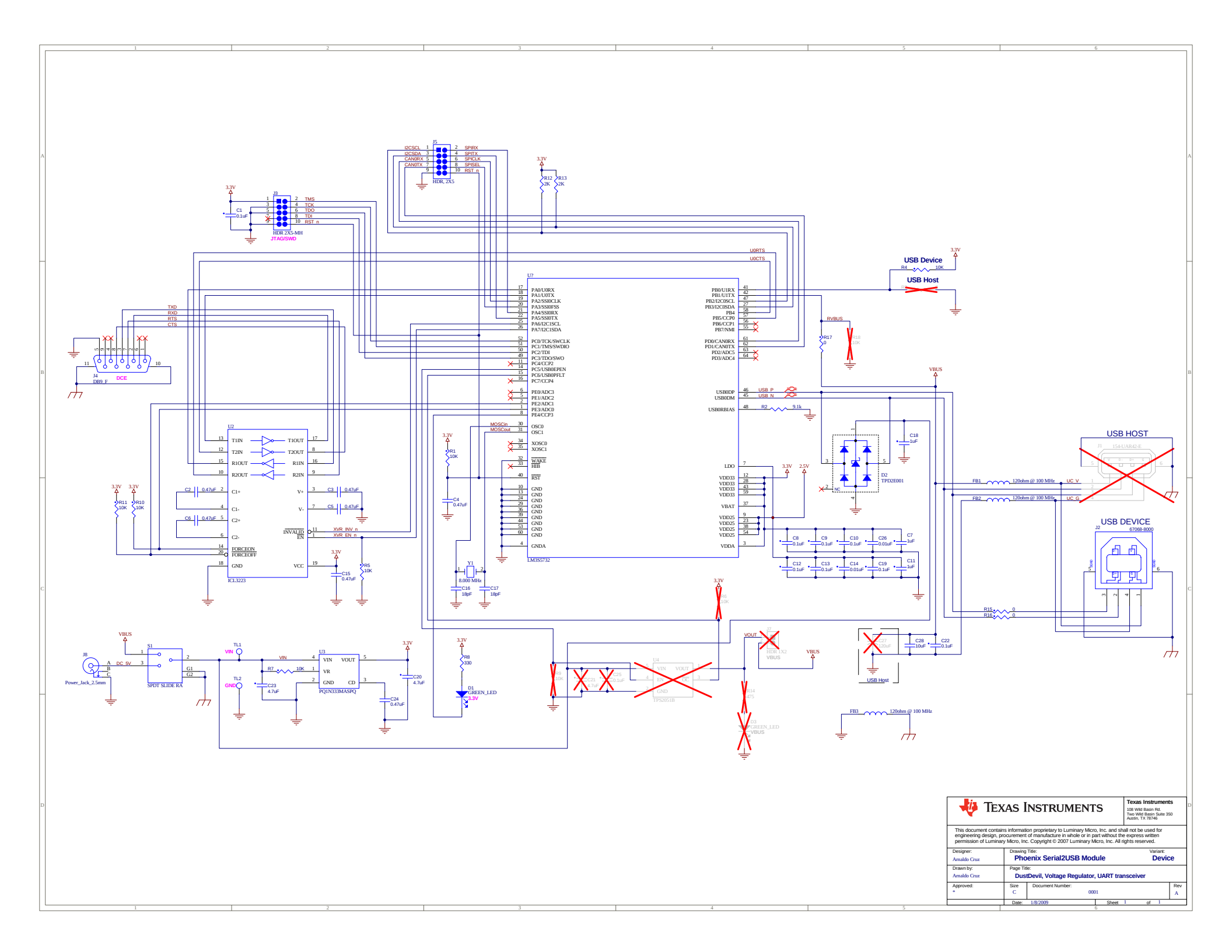


Data Eye



Schematics

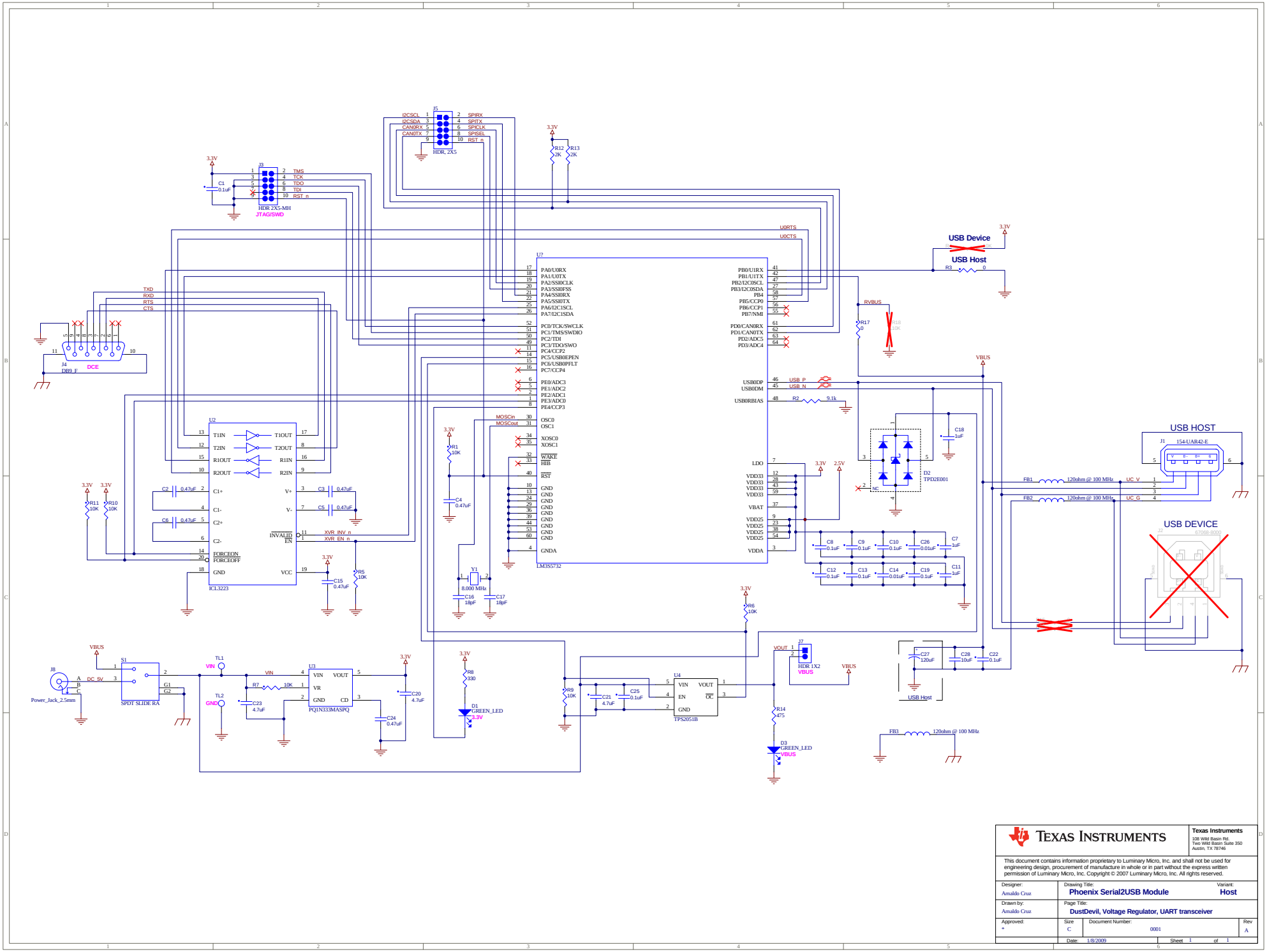
This section contains the schematic diagrams for the Stellaris USB Embedded Host and USB Device:



TEXAS INSTRUMENTS

Texas Instruments
108 Wild Basin Rd.
Two Wild Basin Suite 350
Austin, TX 78746

Designer: Arnaldo Cruz	Drawing Title: Phoenix Serial2USB Module	Variant: Device
Drawn by: Arnaldo Cruz	Page Title: DustDevil, Voltage Regulator, UART transceiver	
Approved: *	Size: C / Document Number: 0001	Rev: A
	Date: 1/8/2009	Sheet 1 of 1



TEXAS INSTRUMENTS

Texas Instruments
108 Wild Basin Rd
Two Wild Basin Suite 350
Austin, TX 78746

Designer: Arnaldo Cruz	Drawing Title: **Phoenix Serial2USB Module**	Variant: **Host**
Drawn by: Arnaldo Cruz	Page Title: **DustDevil, Voltage Regulator, UART transceiver**	
Approved: *	Size: C / Document Number: 0001	Rev: A
	Date: 1/8/2009	Sheet 1 of 1

Conclusion

The Stellaris family of ARM Cortex-M3 microcontrollers includes a range of parts with USB 2.0 Full-Speed Host and Device capabilities. USB hardware features are complemented by comprehensive USB driver software available in StellarisWare®. Certifying a USB Device or USB Embedded Host board is straightforward when using USB-certified Stellaris microcontrollers.

References

Documents used in the generation of this application note include:

- *Stellaris® LM3S5732 Microcontroller Data Sheet,* Publication Number DS-LM3S*5732*
- *StellarisWare® Driver Library User's Manual*, publication number SW-DRL-UG
- *USB Compliance Checklist, Peripherals (Excluding Hubs)*, Checklist Version 1.08, November 28, 2001
- *USB Compliance Checklist, Peripheral Silicon (Excluding Hubs)*, Checklist Version 1.08, December 18, 2001
- *USB Compliance Checklist Systems*, Checklist Version 1.05, October 5, 2001
- *Requirements and Recommendations for USB Products with Embedded Hosts and/or Multiple Receptacles*, Revision 1.0, July 8, 2004
- *USB-IF Embedded Host Compliance Plan*, Revision 1.0, August 2006

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