Configuring Stellaris® Microcontrollers with Pin Multiplexing

With Examples Using the LM3S9B90 and LM3S9790 Devices

Application Note

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Table of Contents

Introduction

The fourth generation of the Stellaris® family of microcontrollers provides system designers with a great deal of control over the placement and selection of peripheral module signals that are alternate functions for GPIO signals. The LM3S9B90 and LM3S9790 microcontrollers are all pin compatible and have 60 pins that can be used for peripheral functions or as GPIOs. Using a unique pin multiplexing implementation, these 60 pins can be customized to provide the best possible signal combination and placement for each individual system design. The remaining 40 pins are power and ground pins, crystal inputs, and a few other functions (Hibernation module signals, USB and Ethernet I/O signals, and BIAS inputs) that require fixed pin location and function.

This application note provides an overview of the pin muxing implementation, an explanation of how a system designer defines a pin configuration, and six examples of the pin configuration process using the LM3S9B90 microcontroller. Although the LM3S9B90 is used to illustrate these concepts, any of the microcontrollers mentioned above can be configured in the same manner.

Pin Muxing Overview

Most of the GPIO pins default to GPIO signals at reset, with the following exceptions:

- JTAG/SWD signals needed at power up for the debugger
- UART0 Rx/Tx signals needed to allow the Stellaris Boot Loader to operate from ROM
- SSI0 Clk/Fss/Rx/Tx signals needed to allow the Stellaris Boot Loader to operate from ROM
- I^2C SCL/SDA signals needed to allow the Stellaris Boot Loader to operate from ROM

Users can select one from up to 9 possible alternate functions for each pin using the **GPIO PORT CONTROL** registers. The data sheet for the specific device has a table in the General Purpose Input/ Outputs (GPIOs) chapter that shows all the possible functions for each GPIO pin.

To configure a GPIO pin to an alternate function, follow these steps:

1. Enable the clock to the appropriate GPIO port using the `SysCtlPeripheralEnable` function.
2. Enable the clock to the peripherals using the `SysCtlPeripheralEnable` function.
3. Configure the pins to the appropriate function using the `GPIOPinConfigure` function.
4. Configure the signal attributes using the `GPIOPinTypexxx` function to configure the pins for specific peripheral function.

Pin Allocation

To decide how to distribute the signals on the device, make a list of the signals needed in the system. Three factors to keep in mind when allocating signals are:

- The number of possible pin assignments for each signal. Some signals can only be assigned to one pin, while others can be assigned to up to ten pins.

- Some signals should be assigned to the same GPIO port so that they can be accessed in a single write, for example, when using both `PWM2` and `PWM3` for bit banging.
- Some signals with similar functions are fungible. For example, if you need 4 CCP signals, you can choose any of the 4 `CCPx` signals; if you need 1 Fault signal, you can choose any of the `Faultx` signals.

To begin pin allocation, first assign the signals that have only one available location, then assign the ones that have two, then three, and so on, bearing in mind the factors listed above. Once the pins have been allocated, then write the code to properly configure the GPIOs for the signal selections.

Table 1 shows the possible pin assignments for each signal on the LM3S9B90 and LM3S9790 microcontrollers.

Table 1. Possible Pin Assignments for the LM3S9B90 and LM3S9790 Microcontrollers

Number of Possible Assignments	Signal Name	GPIO
1	CAN1Rx	PF0
	CAN1Tx	PF1
	EPI0S0	PH3
	EPI0S1	PH2
	EPI0S2	PC4
	EPI0S3	PC5
	EPI0S4	PC6
	EPI0S5	PC7
	EPI0S6	PH0
	EPI0S7	PH1
	EPI0S8	PE0
	EPI0S9	PE1
	EPI0S10	PH4
	EPI0S11	PH5
	EPI0S12	PF4
	EPI0S13	PG0
	EPI0S14	PG1
	EPI0S15	PF5
	EPI0S16	PJ0
	EPI0S17	PJ1

Table 1. Possible Pin Assignments for the LM3S9B90 and LM3S9790 Microcontrollers (Continued)

Number of Possible Assignments	Signal Name	GPIO
1 (cont.)	EPI0S18	PJ2
	EPI0S19	PD4
	EPI0S20	PD2
	EPI0S21	PD3
	EPI0S22	PB5
	EPI0S23	PB4
	EPI0S24	PE2
	EPI0S25	PE3
	EPI0S26	PH6
	EPI0S27	PH7
	EPI0S28	PD5
	EPI0S29	PD6
	EPI0S30	PD7
	EPI0S31	PG7
	I2C0SCL	PB2
	I2C0SDA	PB3
	I2S0RXSCK	PD0
	I2S0RXWS	PD1
	I2S0TXMCLK	PF1
	LED0	PF3
	LED1	PF2
	NMI	PB7
	SSI0Clk	PA2
	SSI0Fss	PA3
	SSI0Rx	PA4
	SSI0Tx	PA5
	TCK/SWCLK	PC0
	TMS/SWDIO	PC1
	TDI	PC2

Table 1. Possible Pin Assignments for the LM3S9B90 and LM3S9790 Microcontrollers (Continued)

Number of Possible Assignments	Signal Name	GPIO
1 (cont.)	TDO/SWO	PC3
	U0Rx	PA0
	U0Tx	PA1
	U1DSR	PF0
	U1DTR	PD7
	U1RI	PD4
	U1RTS	PF1
2	C2o	PC6, PE7
	I2S0RXMCLK	PA3, PD5
	I2S0RXSD	PA2, PD4
	I2S0TXSD	PE5, PF0
3	I2S0TXSCK	PA4, PB6, PD6
	I2S0TXWS	PA5, PD7, PE4
	SSI1Clk	PE0, PF2, PH4
	SSI1Fss	PE1, PF3, PH5
	SSI1Rx	PE2, PF4, PH6
	SSI1TX	PE3, PF5, PH7
	U1CTS	PA6, PD0, PE6
	U1DCD	PA7, PD1, PE7
4	CAN0Rx	PA4, PA6, PB4, PD0
	CAN0Tx	PA5, PA7, PB5, PD1
	I2C1SCL	PA0, PA6, PG0, PJ0
	I2C1SDA	PA1, PA7, PG1, PJ1
	U2Rx	PB4, PD0, PD5, PG0
	U2Tx	PD1, PD6, PE4, PG1
5	C0o	PB5, PB6, PC5, PD7, PF4
	C1o	PC5, PC7, PE6, PF5, PH2
	CCP4	PA7, PC4, PC7, PD5, PE2
	CCP6	PB5, PD0, PD2, PE1, PH0

Table 1. Possible Pin Assignments for the LM3S9B90 and LM3S9790 Microcontrollers (Continued)

Number of Possible Assignments	Signal Name	GPIO
5 (cont.)	CCP7	PB6, PD1, PD3, PE3, PH1
	USB0EPEN	PA6, PB2, PC5, PG0, PH3
6	CCP5	PB5, PB6, PC4, PD2, PE5, PG7
	U1Rx	PA0, PB0, PB4, PC6, PD0, PD2
	U1Tx	PA1, PB1, PB5, PC7, PD1, PD3
7	CCP1	PA6, PB1, PB6, PC4, PC5, PD7, PE3
	USB0PFLT	PA7, PB3, PC6, PC7, PE0, PH4, PJ1
8	CCP3	PA7, PB2, PC5, PC6, PD4, PE0, PE4, PF1
9	CCP0	PB0, PB2, PB5, PC6, PC7, PD3, PD4, PF4, PJ2
	CCP2	PB1, PB5, PC4, PD1, PD5, PE1, PE2, PE4, PF5

Examples

Table 1-1 summarizes the examples in this application note. The code for these examples can be found at the www.luminarymicro.com/products/software_updates.html web site. If your application matches or is a subset of one of these examples, you can simply use the code for that example, modifying it to remove any unneeded signals. If your application requires additional or different signals that have several possible pin assignments, you may be able to easily modify one of the following examples to meet your requirements. However, if the additional signals your application requires have few possible pin assignments, it is usually easiest to start from scratch with the pin assignments following the described in the Pin Allocation section.

The code to create the examples implements Steps 1 and 3 described in the Pin Muxing Overview. Steps 2 and 4 are outside the scope of this example and are not included in the code.

Table 1-1. Example Configurations

Example	Ethernet	USB	EPI[a]	HIB	CAN	UART	I^2C	SSI	I^2S	ADC	Ext Ref	Timer	CCP
1	Y	Host	N	Y	1	3	2	2	0	16	Y	4	8
2	Y	OTG	N	Y	1	2	2	2	1	4	Y	4	7
3	Y	OTG	N	Y	0	2[b]	2	2	0	0	N	4	0
4	Y	OTG	HB	Y	2	1	1	1	0	4	Y	4	0
5	Y	OTG	GP	Y	0	1	1	0	1	4	Y	4	0

a.N = no EPI interface, HB = Host-Bus interface, GP = General-Purpose interface
b.UART1 uses modem controls

Example 1

The first example uses the LM3S9B90 device with the modules and signals shown in Table 1-2.

Table 1-2. Example 1 Module and Signal List

Module	Signals	Notes
Ethernet	LED0, LED1	Remaining signals have fixed locations.
USB Host	USB0PFLT, USB0EPEN	Remaining signals have fixed locations.
Hibernate		Signals have fixed locations.
CAN	CAN0Rx, CAN0Tx	
UART	U0Rx, U0Tx, U1Rx, U1Tx, U2Rx, U2Tx	
I^2C	I2C0SCL, I2C0SDA, I2C1SCL, I2C1SDA	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx, SSI1Clk, SSI1Fss, SSI1Rx, SSI1Tx	
ADC	AIN[15:0], VREFA	PB[5:4], PD[7:0], PE[7:2], and PB6 used as analog functions
4 Timers, 8 CCP inputs	CCP0, CCP1, CCP2, CCP3, CCP4, CCP5, CCP6, CCP7	
System Control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only 1 available pin assignment:

- Port A - U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B - I2C0SCL (PB2), I2C0SDA (PB3), NMI (PB7)
- Port C - TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3)
- Port F - LED1 (PF2), LED0 (PF3)

Step 2: Assign signals with 2 available pin assignments:

- This configuration does not use any of the pins with 2 possible pin assignments.

Step 3: Assign signals with 3 available pin assignments:

- Port H - SSI1Clk (PH4), SSI1Fss (PH5), SSI1Rx (PH6), SSI1Tx (PH7)

Step 4: Assign signals with 4 available pin assignments:

- Port A - CAN0Rx (PA6), CAN0Tx (PA7)
- Port G - U2Rx (PG0), U2Tx (PG1)
- Port J - I2C1SCL (PJ0), I2C1SDA (PJ1)

Step 5: Assign signals with 5 available pin assignments:

- Port C - CCP4 (PC4)
- Port H - CCP6 (PH0), CCP7 (PH1), USB0EPEN (PH3)

Step 6: Assign signals with 6 available pin assignments:

- Port C - U1Rx (PC6), U1Tx (PC7)
- Port G - CCP5 (PG7)

Step 7: Assign signals with 7 available pin assignments:

- Port C - CCP1 (PC5)
- Port E - USB0PFLT (PE0)

Step 8: Assign signals with 8 available pin assignments:

- Port F - CCP3 (PF1)

Step 9: Assign signals with 9 available pin assignments:

- Port E - CCP2 (PE1)
- Port F - CCP0 (PF4)

Table 1-3 shows the final pin assignments for Example 1. “NA” appears in a column when a pin is not available on the microcontroller. “-” appears in a column when a pin is not used for an analog or alternate digital function.

Table 1-3. Final Pin Assignments for Example 1

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	-	TCK/ SWCLK	AIN15	USB0PFLT	-	U2Rx	CCP6	I2C1SCL
1	U0Tx	-	TMS/ SWDIO	AIN14	CCP2	CCP3	U2Tx	CCP7	I2C1SDA
2	SSI0Clk	I2C0SCL	TDI	AIN13	AIN9	LED1	NA	-	-
3	SSI0Fss	I2C0SDA	TDO/ SWO	AIN12	AIN8	LED0	NA	USB0EPEN	NA
4	SSI0Rx	AIN10	CCP4	AIN7	AIN3	CCP0	NA	SSI1Clk	NA
5	SSI0Tx	AIN11	CCP1	AIN6	AIN2	-	NA	SSI1Fss	NA
6	CAN0Rx	VREFA	U1Rx	AIN5	AIN1	NA	NA	SSI1Rx	NA
7	CAN0Tx	NMI	U1Tx	AIN4	AIN0	NA	CCP5	SSI1Tx	NA

Example 2

The second example uses the LM3S9B90 device with the modules and signals shown in Table 1-4.

Table 1-4. Example 2 Module and Signal List

Module	Signals	Notes
Ethernet	LED0, LED1	Remaining signals have fixed locations.
USB OTG	USB0PFLT, USB0EPEN	USB0ID and USB0VBUS use PB0 and PB1 as analog functions, remaining signals have fixed locations.
Hibernate		Signals have fixed locations.
CAN	CAN0Rx, CAN0Tx	
UART	U0Rx, U0Tx, U1Rx, U1Tx	
I^2C	I2C0SCL, I2C0SDA, I2C1SCL, I2C1SDA	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx, SSI1Clk, SSI1Fss, SSI1Rx, SSI1Tx	
I^2S	I2S0RXMCLK, I2S0RXSCK, I2S0RXSD, I2S0RXWS, I2S0TXMCLK, I2S0TXSCK, I2S0TXSD, I2S0TXWS	
ADC	AIN[3:0], VREFA	PE[7:4] and PB6 used as analog functions
4 Timers, 7 CCP inputs	CCP0, CCP1, CCP2, CCP3, CCP4, CCP5, CCP6	
System Control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only 1 available pin assignment:

- Port A - U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B - I2C0SCL (PB2), I2C0SDA (PB3), NMI (PB7)
- Port C - TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3)
- Port D - I2S0RXSCK (PD0), I2S0RXWS (PD1)
- Port F - I2S0TXMCLK (PF1), LED1 (PF2), LED0 (PF3)

Step 2: Assign signals with 2 available pin assignments:

- Port D - I2S0RXSD (PD4), I2S0RXMCLK (PD5)
- Port F - I2S0TXSD (PF0)

Step 3: Assign signals with 3 available pin assignments:

- Port D - I2S0TXSCK (PD6), I2S0TXWS (PD7)
- Port E - SSI1Clk (PE0), SSI1Fss (PE1), SSI1Rx (PE2), SSI1Tx (PE3)

Step 4: Assign signals with 4 available pin assignments:

- Port A - CAN0Rx (PA6), CAN0Tx (PA7)
- Port G - I2C1SCL (PG0), I2C1SDA (PG1)

Step 5: Assign signals with 5 available pin assignments:

- Port C - USB0EPEN (PC5), CCP4 (PC7)
- Port H - CCP6 (PH0)

Step 6: Assign signals with 6 available pin assignments:

- Port B - U1Rx (PB4), U1Tx (PB5)
- Port D - CCP5 (PD2)

Step 7: Assign signals with 7 available pin assignments:

- Port C - CCP1 (PC4)
- Port H - USB0PFLT (PH4)

Step 8: Assign signals with 8 available pin assignments:

- Port C - CCP3 (PC6)

Step 9: Assign signals with 9 available pin assignments:

- Port D - CCP0 (PD3)
- Port F - CCP2 (PF5)

Table 1-5 shows the final pin assignments for Example 2. “NA” appears in a column when a pin is not available on the microcontroller. “-” appears in a column when a pin is not used for an analog or alternate digital function.

Table 1-5. Final Pin Assignments for Example 2

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	USB0ID	TCK/ SWCLK	I2S0RXSCK	SSI1Clk	I2S0TXSD	I2C1SCL	CCP6	-
1	U0Tx	USB0VBUS	TMS/ SWDIO	I2S0RXWS	SSI1Fss	I2S0TXMCLK	I2C1SDA	-	-
2	SSI0Clk	I2C0SCL	TDI	CCP5	SSI1Rx	LED1	NA	-	-
3	SSI0Fss	I2C0SDA	TDO/ SWO	CCP0	SSI1Tx	LED0	NA	-	NA
4	SSI0Rx	U1Rx	CCP1	I2S0RXSD	AIN3	-	NA	USB0PFLT	NA
5	SSI0Tx	U1Tx	USB0EPEN	I2S0RXMCLK	AIN2	CCP2	NA	-	NA

Table 1-5. Final Pin Assignments for Example 2 (Continued)

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
6	CAN0Rx	VREFA	CCP3	I2S0TXSCK	AIN1	NA	NA	-	NA
7	CAN0Tx	NMI	CCP4	I2S0TXWS	AIN0	NA	-	-	NA

Example 3

The third example uses the LM3S9B90 device with the modules and signals shown in Table 1-6.

Table 1-6. Example 3 Module and Signal List

Module	Signals	Notes
Ethernet	LED0, LED1	Remaining signals have fixed locations.
USB OTG	USB0PFLT, USB0EPEN	USB0ID and USB0VBUS use PB0 and PB1 as analog functions, remaining signals have fixed locations.
Hibernate		Signals have fixed locations.
UART	U0Rx, U0Tx, U1Rx, U1Tx, U1CTS, U1DCD, U1DSR, U1DTR, U1RI, U1RTS	
I^2C	I2C0SCL, I2C0SDA, I2C1SCL, I2C1SDA	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx, SSI1Clk, SSI1Fss, SSI1Rx, SSI1Tx	
4 Timers		No signals.
System Control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only 1 available pin assignment:

- Port A - U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B - I2C0SCL (PB2), I2C0SDA (PB3), NMI (PB7)
- Port C - TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3)
- Port D - U1RI (PD4), U1DTR (PD7)
- Port F - U1DSR (PF0), U1RTS (PF1), LED1 (PF2), LED0 (PF3)

Step 2: Assign signals with 2 available pin assignments:

- This configuration does not use any of the pins with 2 possible pin assignments.

Step 3: Assign signals with 3 available pin assignments:

- Port A - U1CTS (PA6), U1DCD (PA7)

- Port E - SSI1Clk (PE0), SSI1Fss (PE1), SSI1Rx (PE2), SSI1Tx (PE3)

Step 4: Assign signals with 4 available pin assignments:
- Port G - I2C1SCL (PG0), I2C1SDA (PG1)

Step 5: Assign signals with 5 available pin assignments:
- Port C - USB0EPEN (PC5)

Step 6: Assign signals with 6 available pin assignments:
- Port B - U1Rx (PB4), U1Tx (PB5)

Step 7: Assign signals with 7 available pin assignments:
- Port C - USB0PFLT (PC6)

Step 8: Assign signals with 8 available pin assignments:
- This configuration does not use the pin with 8 possible pin assignments.

Step 9: Assign signals with 9 available pin assignments:
- This configuration does not use any of the pins with 9 possible pin assignments.

Table 1-7 shows the final pin assignments for Example 3. “NA” appears in a column when a pin is not available on the microcontroller. “-” appears in a column when a pin is not used for an analog or alternate digital function.

Table 1-7. Final Pin Assignments for Example 3

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	USB0ID	TCK/ SWCLK	-	SSI1Clk	U1DSR	I2C1SCL	-	-
1	U0Tx	USB0VBUS	TMS/ SWDIO	-	SSI1Fss	U1RTS	I2C1SDA	-	-
2	SSI0Clk	I2C0SCL	TDI	-	SSI1Rx	LED1	NA	-	-
3	SSI0Fss	I2C0SDA	TDO/ SWO	-	SSI1Tx	LED0	NA	-	NA
4	SSI0Rx	U1Rx	-	U1RI	-	-	NA	-	NA
5	SSI0Tx	U1Tx	USB0EPEN	-	-	-	NA	-	NA
6	U1CTS	-	USB0PFLT	-	-	NA	NA	-	NA
7	U1DCD	NMI	-	U1DTR	-	NA	-	-	NA

Example 4

The fourth example uses the LM3S9B90 device with the modules and signals shown in Table 1-8.

Table 1-8. Example 4 Module and Signal List

Module	Signals	Notes
Ethernet	LED0, LED1	Remaining signals have fixed locations.
USB OTG	USB0PFLT, USB0EPEN	USB0ID and USB0VBUS use PB0 and PB1 as analog functions, remaining signals have fixed locations.
EPI interface to Host Bus	EPI0S[31:0]	
Hibernate		Signals have fixed locations.
CAN	CAN0Rx, CAN0Tx, CAN1Rx, CAN1Tx	
UART	U0Rx, U0Tx	
I^2C	I2C0SCL, I2C0SDA	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx	
ADC	AIN[3:0], VREFA	PE[7:4] and PB6 used as analog functions.
4 Timers		No signals.
System Control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with 1 available pin assignment:

- Port A - U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B - I2C0SCL (PB2), I2C0SDA (PB3), EPI0S23 (PB4), EPI0S22 (PB5), NMI (PB7)
- Port C - TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3), EPI0S2 (PC4), EPI0S3 (PC5), EPI0S4 (PC6), EPI0S5 (PC7)
- Port D - EPI0S20 (PD2), EPI0S21 (PD3), EPI0S19 (PD4), EPI0S28 (PD5), EPI0S29 (PD6), EPI0S30 (PD7)
- Port E - EPI0S8 (PE0), EPI0S9 (PE1), EPI0S24 (PE2), EPI0S25 (PE3)
- Port F - CAN1Rx (PF0), CAN1Tx (PF1), LED1 (PF2), LED0 (PF3), EPI0S12 (PF4), EPI0S15 (PF5)
- Port G - EPI0S13 (PG0), EPI0S14 (PG1), EPI0S31 (PG7)

- Port H - EPI0S6 (PH0), EPI0S7 (PH1), EPI0S1 (PH2), EPI0S0 (PH3), EPI0S10 (PH4), EPI0S11 (PH5), EPI0S26 (PH6), EPI0S27 (PH7)
- Port J - EPI0S16 (PJ0), EPI0S17 (PJ1), EPI0S18 (PJ2)

Step 2: Assign signals with 2 available pin assignments:

- This configuration does not use any of the pins with 2 possible pin assignments.

Step 3: Assign signals with 3 available pin assignments:

- This configuration does not use any of the pins with 3 possible pin assignments.

Step 4: Assign signals with 4 available pin assignments:

- Port D - CAN0Rx (PD0), CAN0Tx (PD1)

Step 5: Assign signals with 5 available pin assignments:

- Port A - USB0EPEN (PA6)

Step 6: Assign signals with 6 available pin assignments:

- This configuration does not use any of the pins with 6 possible pin assignments.

Step 7: Assign signals with 7 available pin assignments:

- Port A - USB0PFLT (PA7)

Step 8: Assign signals with 8 available pin assignments:

- This configuration does not use the pin with 8 possible pin assignments.

Step 9: Assign signals with 9 available pin assignments:

- This configuration does not use any of the pins with 9 possible pin assignments.

Table 1-9 shows the final pin assignments for Example 4. “NA” appears in a column when a pin is not available on the microcontroller. “-” appears in a column when a pin is not used for an analog or alternate digital function.

Table 1-9. Final Pin Assignments for Example 4

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	USB0ID	TCK/ SWCLK	CAN0Rx	EPI0S8	CAN1Rx	EPI0S13	EPI0S6	EPI0S16
1	U0Tx	USB0VBUS	TMS/ SWDIO	CAN0Tx	EPI0S9	CAN1Tx	EPI0S14	EPI0S7	EPI0S17
2	SSI0Clk	I2C0SCL	TDI	EPI0S20	EPI0S24	LED1	NA	EPI0S1	EPI0S18
3	SSI0Fss	I2C0SDA	TDO/ SWO	EPI0S21	EPI0S25	LED0	NA	EPI0S0	NA

Table 1-9. Final Pin Assignments for Example 4 (Continued)

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
4	SSI0Rx	EPI0S23	EPI0S2	EPI0S19	AIN3	EPI0S12	NA	EPI0S10	NA
5	SSI0Tx	EPI0S22	EPI0S3	EPI0S28	AIN2	EPI0S15	NA	EPIS011	NA
6	USB0EPEN	VREFA	EPI0S4	EPI0S29	AIN1	NA	NA	EPI026	NA
7	USB0PFLT	NMI	EPI0S5	EPI0S30	AIN0	NA	EPI0S31	EPI027	NA

Example 5

The fifth example uses the LM3S9B90 device with the modules and signals shown in Table 1-10.

Table 1-10. Example 5 Module and Signal List

Module	Signals	Notes
Ethernet	LED0, LED1	Remaining signals have fixed locations.
USB OTG	USB0PFLT, USB0EPEN	USB0ID and USB0VBUS use PB0 and PB1 as analog functions, remaining signals have fixed locations.
EPI interface in General-Purpose mode	EPI0S[31:0]	
Hibernate		Signals have fixed locations.
UART	U0Rx, U0Tx	
I^2C	I2C0SCL, I2C0SDA	
I^2S	I2S0RXMCLK, I2S0RXSCK, I2S0RXSD, I2S0RXWS, I2S0TXMCLK, I2S0TXSCK, I2S0TXSD, I2S0TXWS	
ADC	AIN[3:0], VREFA	PE[7:4] and PB6 used as analog functions.
4 Timers		No signals.
System Control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only 1 available pin assignment:

- Port A - U0Rx (PA0), U0Tx (PA1)
- Port B - I2C0SCL (PB2), I2C0SDA (PB3), EPI0S23 (PB4), EPI0S22 (PB5), NMI (PB7)
- Port C - TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3), EPI0S2 (PC4), EPI0S3 (PC5), EPI0S4 (PC6), EPI0S5 (PC7)

- Port D - I2S0RXSCK (PD0), I2S0RXWS (PD1), EPI0S20 (PD2), EPI0S21 (PD3), EPI0S19 (PD4), EPI0S28 (PD5), EPI0S29 (PD6), EPI0S30 (PD7)
- Port E - EPI0S8 (PE0), EPI0S9 (PE1), EPI0S24 (PE2), EPI0S25 (PE3)
- Port F - I2S0TXMCLK (PF1), LED1 (PF2), LED0 (PF3), EPI0S12 (PF4), EPI0S15 (PF5)
- Port G - EPI0S13 (PG0), EPI0S14 (PG1), EPI0S31 (PG7)
- Port H - EPI0S6 (PH0), EPI0S7 (PH1), EPI0S1 (PH2), EPI0S0 (PH3), EPI0S10 (PH4), EPI0S11 (PH5), EPI0S26 (PH6), EPI0S27 (PH7)
- Port J - EPI0S16 (PJ0), EPI0S17 (PJ1), EPI0S18 (PJ2)

Step 2: Assign signals with 2 available pin assignments:

- Port A - I2S0RXSD (PA2), I2S0RXMCLK (PA3)
- Port F - I2S0TXSD (PF0)

Step 3: Assign signals with 3 available pin assignments:

- Port A - I2S0TXSCK (PA4), I2S0TXWS (PA5)

Step 4: Assign signals with 4 available pin assignments:

- This configuration does not use any of the pins with 4 possible pin assignments.

Step 5: Assign signals with 5 available pin assignments:

- Port A - USB0EPEN (PA6)

Step 6: Assign signals with 6 available pin assignments:

- This configuration does not use any of the pins with 6 possible pin assignments.

Step 7: Assign signals with 7 available pin assignments:

- Port A - USB0PFLT (PA7)

Step 8: Assign signals with 8 available pin assignments:

- This configuration does not use the pin with 8 possible pin assignments.

Step 9: Assign signals with 9 available pin assignments:

- This configuration does not use any of the pins with 9 possible pin assignments.

Table 1-11 shows the final pin assignments for Example 5. “NA” appears in a column when a pin is not available on the microcontroller. “-” appears in a column when a pin is not used for an analog or alternate digital function.

Table 1-11. Final Pin Assignments for Example 5

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	USB0ID	TCK/ SWCLK	I2S0RXSCK	EPI0S8	I2S0TXSD	EPI0S13	EPI0S6	EPI0S16

Table 1-11. Final Pin Assignments for Example 5 (Continued)

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
1	U0Tx	USB0VBUS	TMS/ SWDIO	I2S0RXWS	EPI0S9	I2S0TXMCLK	EPI0S14	EPI0S7	EPI0S17
2	I2S0RXSD	I2C0SCL	TDI	EPI0S20	EPI0S24	LED1	NA	EPI0S1	EPI0S18
3	I2S0RXMCLK	I2C0SDA	TDO/ SWO	EPI0S21	EPI0S25	LED0	NA	EPI0S0	NA
4	I2S0TXSCK	EPI0S23	EPI0S2	EPI0S19	AIN3	EPI0S12	NA	EPI0S10	NA
5	I2S0TXWS	EPI0S22	EPI0S3	EPI0S28	AIN2	EPI0S15	NA	EPI0S11	NA
6	USB0EPEN	VREFA	EPI0S4	EPI0S29	AIN1	NA	NA	EPI0S26	NA
7	USB0PFLT	NMI	EPI0S5	EPI0S30	AIN0	NA	EPI0S31	EPI027	NA

Conclusion

The pin muxing capabilities of the Stellaris Tempest-class microcontrollers are highly flexible and easy to implement using the functions provided by the StellarisWare™ Peripheral Driver Library. A system designer can choose the most efficient pin configuration targeted for specific system requirements.

References

Documents used in the generation of this application note include:

- *Stellaris® LM3S9B90 Microcontroller Data Sheet*, Publication Number DS-LM3S9B90
- *Stellaris® Peripheral Driver Library User's Guide* – An element of each StellarisWare® Firmware Development Package downloadable from http://www.luminarymicro.com/products/software_updates.html

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