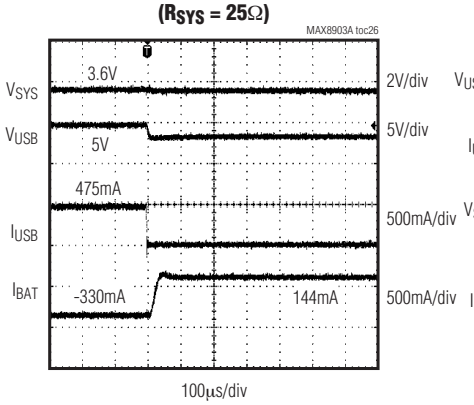
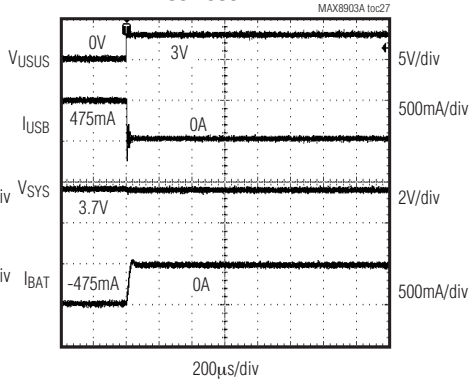
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

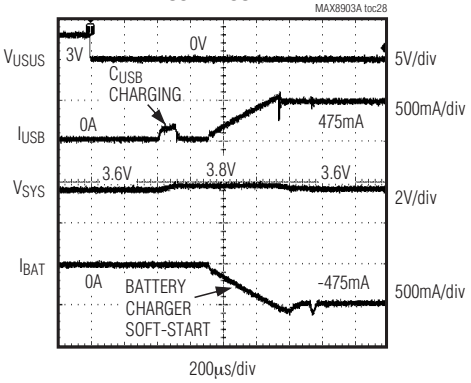
USB DISCONNECT WITH NO DC (R_{SYS} = 25Ω)



USB SUSPEND



USB RESUME



Pin Description

PIN	NAME	FUNCTION
1, 2	PG	Power Ground for Step-Down Low-Side Synchronous n-Channel MOSFET. Both PG pins must be connected together externally.
3, 4	DC	DC Power Input. DC is capable of delivering up to 2A to SYS. DC supports both AC adapter and USB inputs. The DC current limit is set through DCM, IUSB, or IDC depending on the input source used. See Table 2. Both DC pins must be connected together externally. Connect at least a 4.7µF ceramic capacitor from DC to PG.
5	DCM	Current-Limit Mode Setting for the DC Power Input. When logic-high, the DC input current limit is set by the resistance from IDC to GND. When logic-low, the DC input current limit is internally programmed to 500mA or 100mA, as set by the IUSB logic input. There is an internal diode from DCM (anode) to DC (cathode) as shown in Figure 1.
6	BST	High-Side MOSFET Driver Supply. Bypass BST to LX with a 0.1µF ceramic capacitor.
7	IUSB	USB Current-Limit Set Input. Drive IUSB logic-low to set the USB current limit to 100mA. Drive IUSB logic-high to set the USB current limit to 500mA.
8	$\overline{DOK}$	DC Power-OK Output. Active-low open-drain output pulls low when a valid input is detected at DC. $\overline{DOK}$ is still valid when the charger is disabled ($\overline{CEN}$ high).
9	VL	Logic LDO Output. VL is the output of an LDO that powers the MAX8903_ internal circuitry and charges the BST capacitor. Connect a 1µF ceramic capacitor from VL to GND.
10	CT	Charge Timer Set Input. A capacitor (C_{CT}) from CT to GND sets the fast-charge and prequal fault timers. Connect to GND to disable the timer.
11	IDC	DC Current-Limit Set Input. Connect a resistor (R_{IDC}) from IDC to GND to program the current limit of the step-down regulator from 0.5A to 2A when DCM is logic-high.
12	GND	Ground. GND is the low-noise ground connection for the internal circuitry.

Pin Description (continued)

PIN	NAME	FUNCTION
13	ISET	Charge Current Set Input. A resistor (R_{ISET}) from ISET to GND programs the fast-charge current up to 2A. The prequal charge current is 10% of the fast-charge current.
14	$\overline{CEN}$	Charger Enable Input. Connect $\overline{CEN}$ to GND to enable battery charging when a valid source is connected at DC or USB. Connect to VL, or drive high to disable battery charging.
15	USUS	USB Suspend Input. Drive USUS logic-high to enter USB suspend mode, lowering USB current to 115µA, and internally shorting SYS to BAT.
16	THM	Thermistor Input. Connect a negative temperature coefficient (NTC) thermistor from THM to GND. Connect a resistor equal to the thermistor +25°C resistance from THM to VL. Charging is suspended when the thermistor is outside the hot and cold limits. Connect THM to GND to disable the thermistor temperature sensor.
17	USB	USB Power Input. USB is capable of delivering 100mA or 500mA to SYS as set by the IUSB logic input. Connect a 4.7µF ceramic capacitor from USB to GND.
18	$\overline{FLT}$	Fault Output. Active-low, open-drain output pulls low when the battery timer expires before prequal or fast-charge completes.
19	$\overline{UOK}$	USB Power-OK Output. Active-low, open-drain output pulls low when a valid input is detected at USB. $\overline{UOK}$ is still valid when the charger is disabled ($\overline{CEN}$ high).
20, 21	BAT	Battery Connection. Connect to a single-cell Li+ battery. The battery charges from SYS when a valid source is present at DC or USB. BAT powers SYS when neither DC nor USB power is present, or when the SYS load exceeds the input current limit. Both BAT pins must be connected together externally.
22	$\overline{CHG}$	Charger Status Output. Active-low, open-drain output pulls low when the battery is in fast-charge or prequal. Otherwise, $\overline{CHG}$ is high impedance.
23, 24	SYS	System Supply Output. SYS connects to BAT through an internal 50mΩ system load switch when DC or USB are invalid, or when the SYS load is greater than the input current limit. When a valid voltage is present at DC or USB, SYS is limited to V_{SYSREG}. When the system load (I_{SYS}) exceeds the DC or USB current limit, SYS is regulated to 50mV below BAT, and both the powered input and the battery service SYS. Bypass SYS to GND with an X5R or X7R ceramic capacitor. See Table 6 for the minimum recommended SYS capacitor (C_{SYS}). Both SYS pins must be connected together externally.
25, 26	CS	70mΩ Current-Sense Input. Connect the step-down inductor from LX to CS. When the step-down regulator is on, there is a 70mΩ current-sense MOSFET from CS to SYS. When the step-down regulator is off, the internal CS MOSFET turns off to block current from SYS back to DC.
27, 28	LX	Inductor Connection. Connect the inductor between LX and CS. Both LX pins must be connected together externally.
—	EP	Exposed Pad. Connect the exposed pad to GND. Connecting the exposed pad does not remove the requirement for proper ground connections to the appropriate pins.