A Design Methodology for Fault-Tolerant Embedded Neuromorphic Computing (Author's Note)

ACM Reference Format:
. 2018. A Design Methodology for Fault-Tolerant Embedded Neuromorphic Computing (Author's Note). In *DAC '22: ACM Design Automation Conference, July 10–14, 2022, San Francisco, CA.* ACM, New York, NY, USA, 4 pages. https://doi.org/10.1145/1122445.1122456

1 SIMULATION PARAMETERS

1.1 Astrocyte Simulation Parameters (Sec. 4)

Table 1 reports the simulation parameters obtained from [2]. We model these parameters in Brian 2 simulator [3] to explore the self-repair property of an astrocyte.

Table 1: Astrocyte simulation parameters [2].

Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
τ_{AG}	$10s$	r_{AG}	$0.8\mu Ms^{-1}$	τ_{Glu}	$100ms$	r_{Glu}	$10\mu Ms^{-1}$
t_{Ca}	$0.3\mu M$	τ_{eSP}	$40s$	m_{eSP}	$55,000$	K_{AG}	-4000

1.2 Fault Modeling Parameters (Sec. 2)

Table 2: Fault modeling parameters [4].

Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
I_{cell}	$100\mu A$	R_{cell}	$10K\Omega$	l	$120nm$	V	$V = 4 \times 10^{-14} cm^3$
T_{amb}	$300K$	γ	1000	m_{eSP}	$55,000$	C	$1.25JK^{-1}cm^{-3}$

The parameters related to logic failures are adjusted to obtain an MTTF of 2 years.

2 IMPLEMENTATION DETAILS

In this section, we describe the implementation details.

2.1 Astrocyte Design

Figure 4 shows the block diagram of a digital astrocyte [1] implemented using a reduced fixed-point representation while still maintaining physiologically realistic precision. The proposed design is synthesized on three different Xilinx FPGA boards — VC707, VCU128 and ML605.

The designed structure is a parallel architecture that takes less processing time. The output provider unit (OPU) generates the retrograde feedback signal that facilitates frequency restoration at a faulty synaptic site. The frequency reconstruction error can be controlled by choosing the right astrocyte coupling coefficients.

DAC '22, July 10–14, 2022, San Francisco, CA

ACM ISBN 978-1-4503-XXXX-X/18/06…$15.00
https://doi.org/10.1145/1122445.1122456

We use the piece-wise linear model to create efficient FPGA-based architecture. The number of bits used for particular variables is determined by the required precision, processing performance, and resource use. We use a 42-bit fixed point with 2 bit used for sign, 20 bits for integer, and 20 bits for fractional components.

The role of an astrocyte in regulating and modulating the excitation current of a neurons can be seen in Fig. 1.

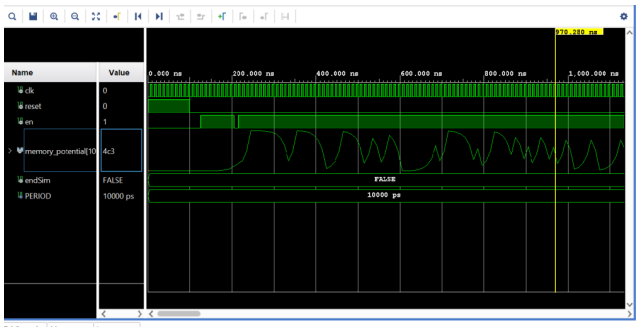

Figure 1: Memory potential.

A key element of the design is the piece-wise linear approximation function, which is illustrated in Figure 2.

FPGA illustrated acceptable performance with a very low error value between the proposed hardware and simulation results.

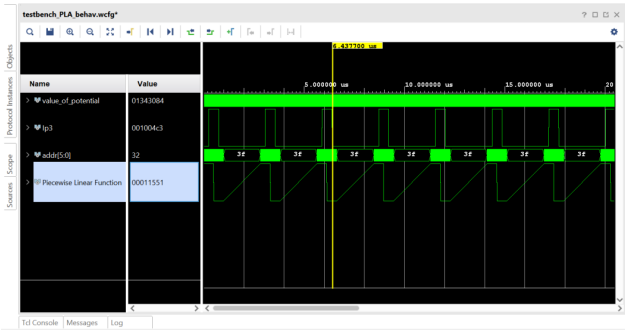

Figure 2: Piece-Wise Linear Approximation Function.

Figure 3 shows the area of the proposed design implemented on the three FPGA development boards. In the submitted paper, we show only the results for VCU128 board.

Tech	XC7VX485T-2	XC6VLX240-1	XCVU37P-L2
Operation Frequency	100MHz	100MHz	100MHz
BRAM	4	5	3
DSP48E	4	4	4
FF	2,368	2,539	2,226
Slice	670	719	354
LUT	1,345	1,804	1,291
Power	0.538 W	0.321 W	3,242 W

Figure 3: Astrocyte implementation on three boards.

The power consumption of astrocyte design is shown in Figure 5, distributed into clocks, signals, logic, DSP, BRAM, MMCM, and I/O.

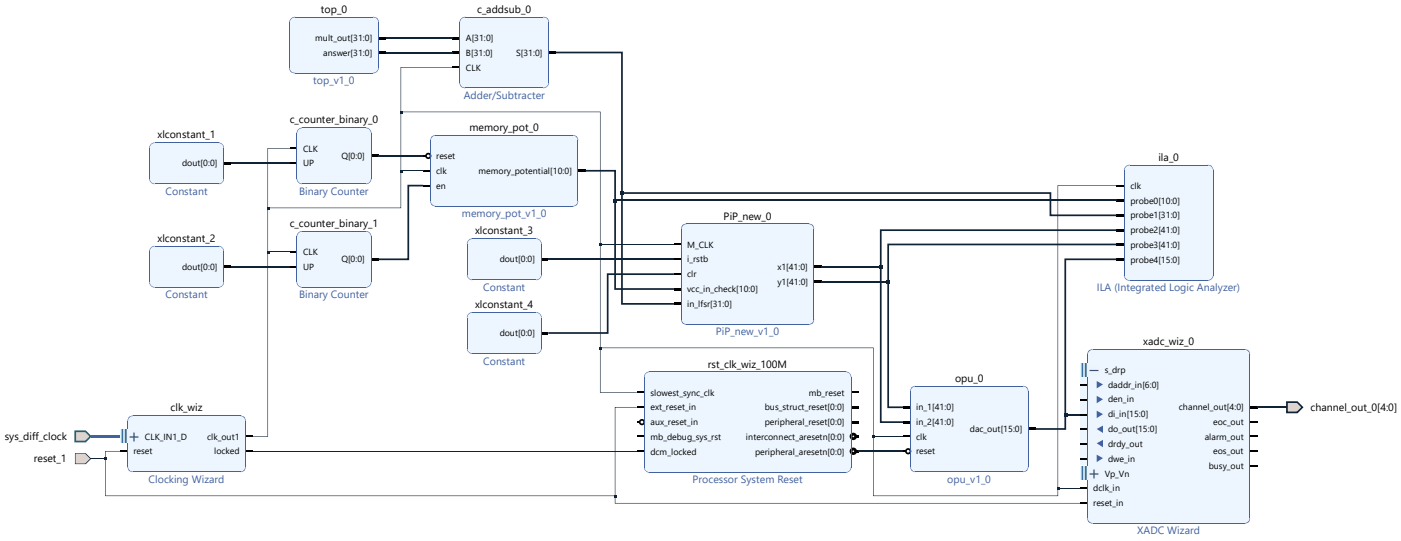

Figure 4: Block designs of an astrocyte.

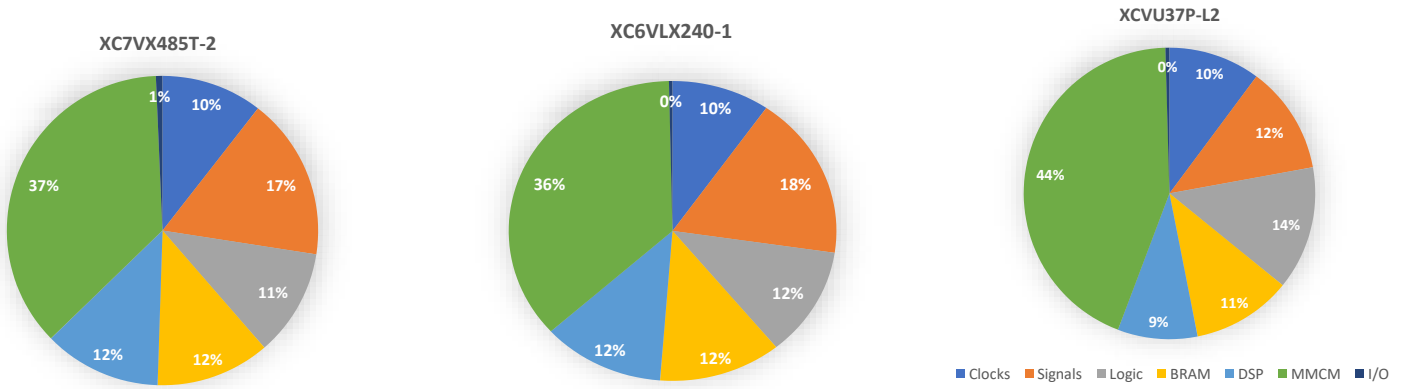

Figure 5: Power consumption of astrocyte, distributed into clocks, signals,BRAMs,DSPs,MMCM, and I/Os.

2.2 Crossbar and μBrain Designs

2.2.1 Crossbar Design. Figure 6 shows the area of the crossbar design implemented on the three FPGA development boards. In the submitted paper, we show only the results for VCU128 board.

Tech	XC7VX485T-2	XC6VLX240-1	XCVU37P-L2
BRAM	32	32	32
DSP48E	0	0	0
FF	86	96	70
Slice	78	86	86
LUT	76	80	74
Power	4.644 W	4.637 W	9.812 W

Figure 6: Crossbar implementation on three boards.

Figure 7 shows the schematic of a crossbar core on FPGA.

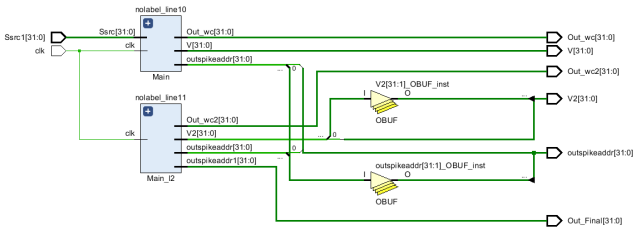

Figure 7: Crossbar schematic on FPGA.

2.2.2 μBrain Design. Figure 8 shows the area of the μBrain design implemented on the three FPGA development boards. In the submitted paper, we show only the results for VCU128 board.

Tech	XC7VX485T-2	XC6VLX240-1	XCVU37P-L2
BRAM	48	48	48
DSP48E	0	0	0
FF	129	144	105
Slice	117	129	129
LUT	114	120	111
Power	4.644 W	4.637 W	9.554 W

Figure 8: μBrain implementation on three boards.

Figure 9 shows the schematic of a μBrain core on FPGA.

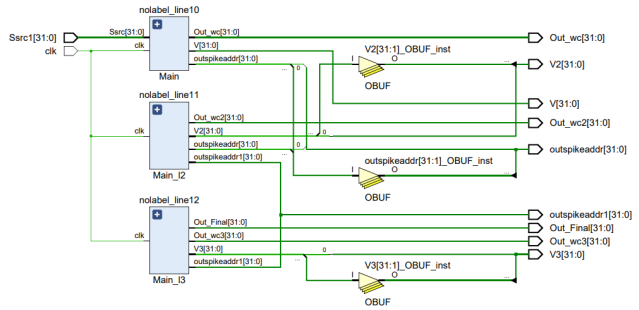

Figure 9: μBrain schematic on FPGA.

REFERENCES

[1] S. Haghiri *et al.*, "Digital FPGA implementation of spontaneous astrocyte signalling," *IJCTA*, 2020.

[2] J. Liu *et al.*, "Exploring self-repair in a coupled spiking astrocyte neural network," *TNNLS*, 2018.

[3] M. Stimberg *et al.*, "Modeling neuron–glia interactions with the Brian 2 simulator," in *Computational Glioscience*, 2019.

[4] T. Titirsha *et al.*, "Endurance-aware mapping of spiking neural networks to neuromorphic hardware," *TPDS*, 2021.