RV32I R-Type Design
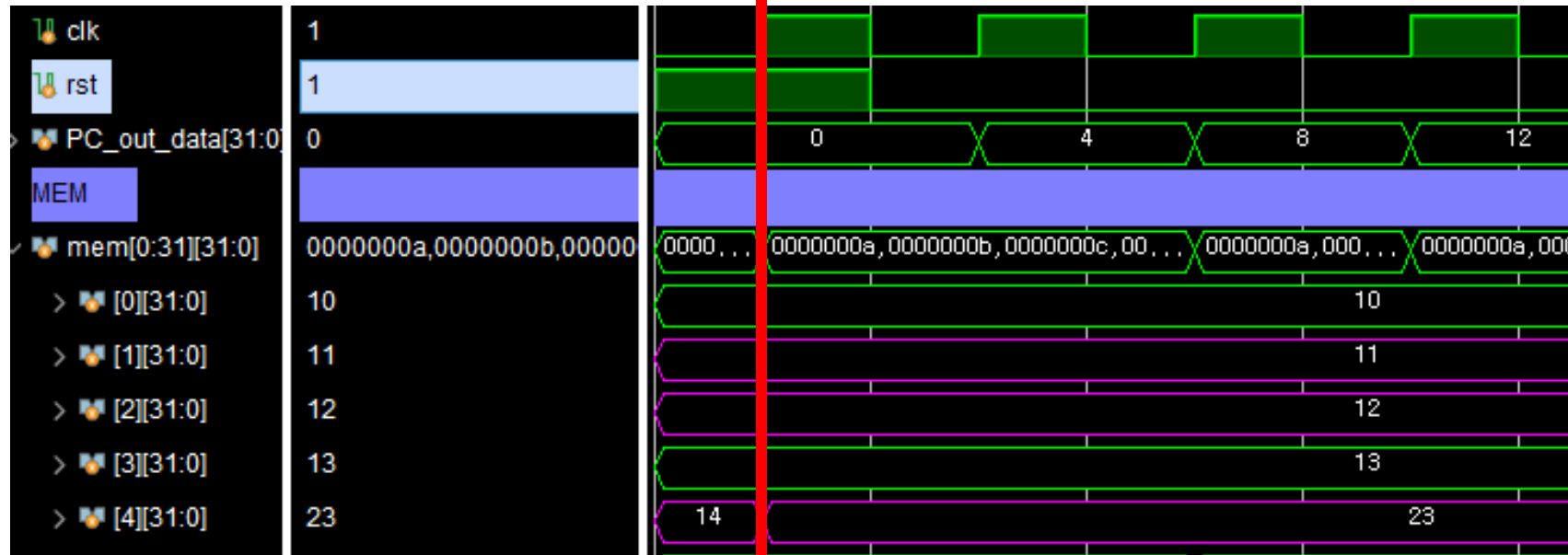
대한상공회의소 AI 시스템반도체 설계 2기

최현우

Add x4, x2, x1
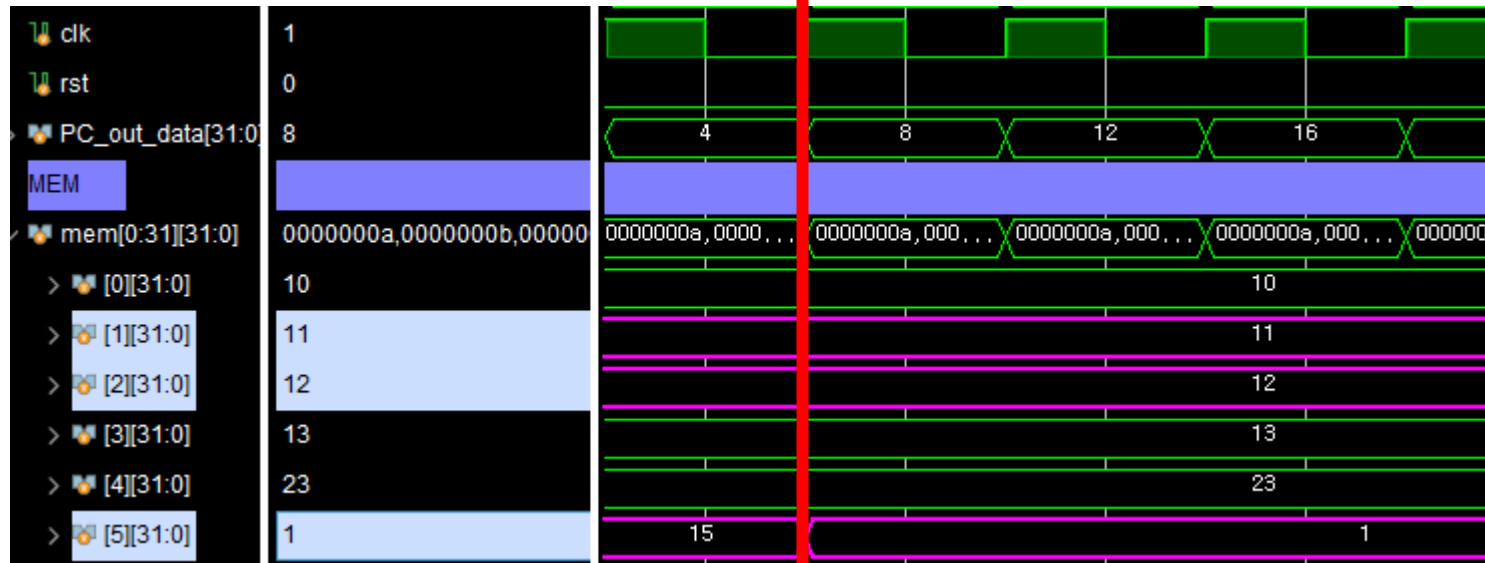

X2 = 12

X1 = 11
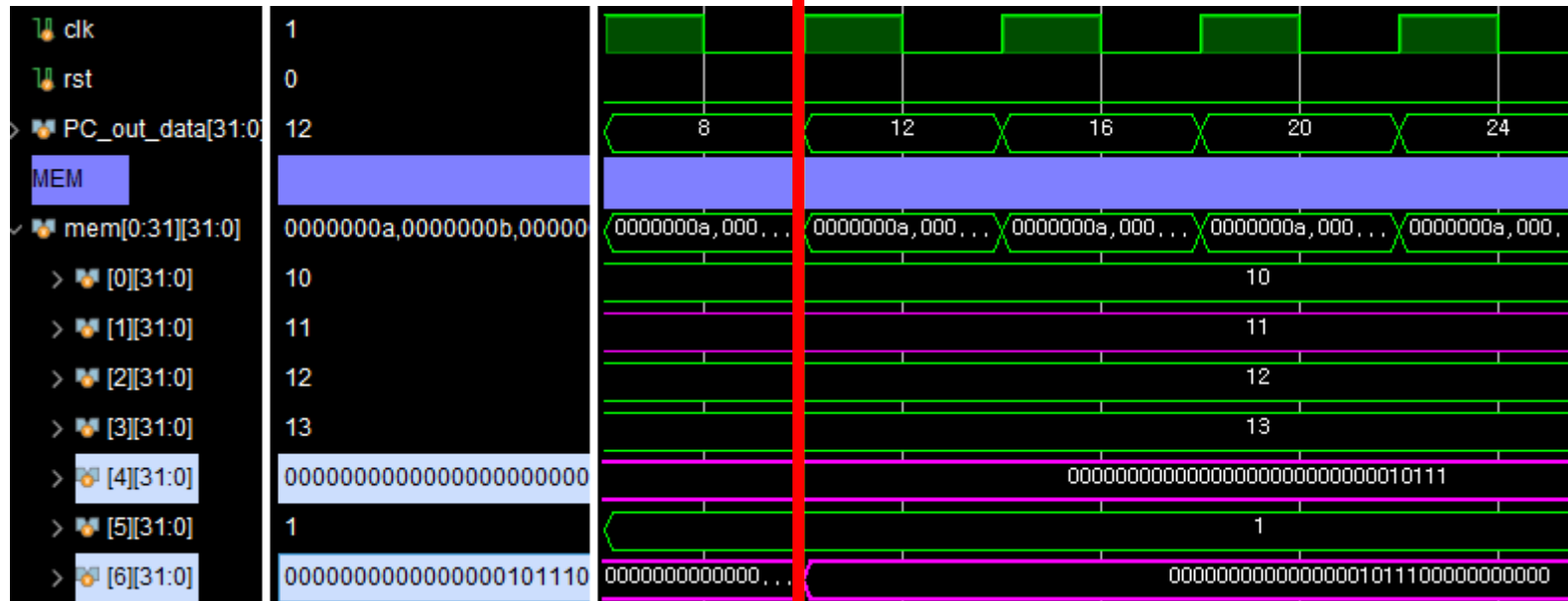
X4 = 23

sub x5, x2, x1

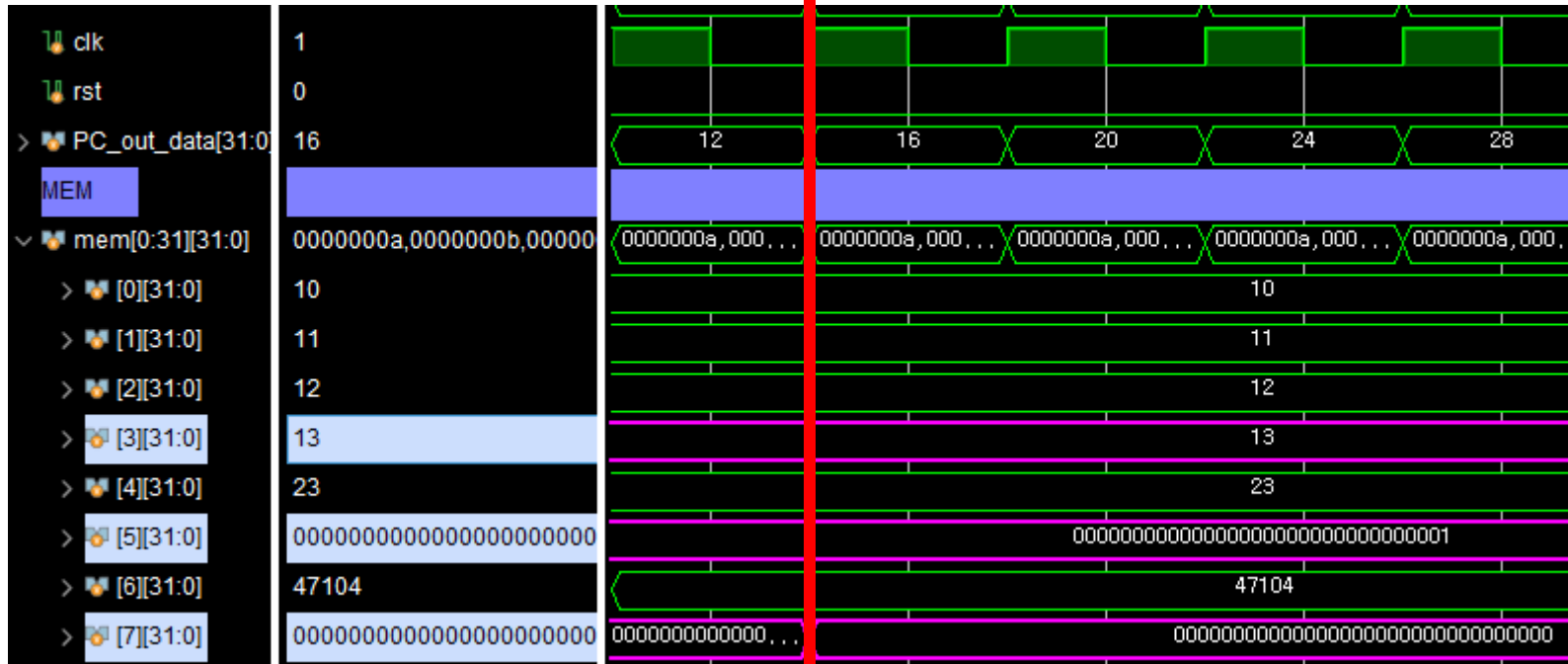X2 = 12

X1 = 11

X5 = 1

sll x6, x4, x1

X4 = 32'b0000_0000_0000_0000_0000_0000_0001_0111

X1 = 32'd11

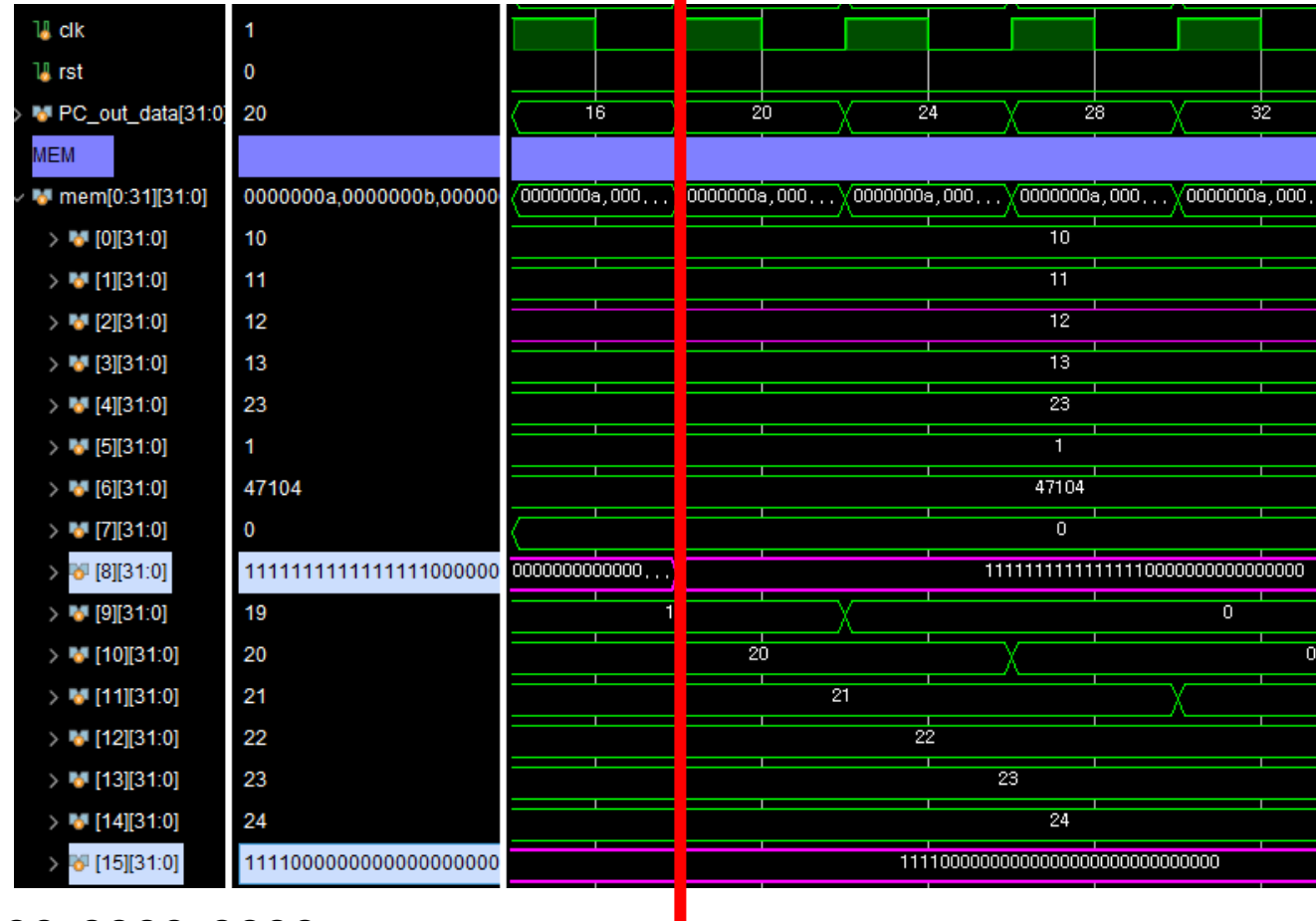X6 = 32'b0000_0000_0000_0000_1011_1000_0000_0000

srl x7, x5, x3

X5 = 32'b0000_0000_0000_0000_0000_0000_0000_0001

X3 = 32'd13

X7 = 32'b0000_0000_0000_0000_0000_0000_0000_0000
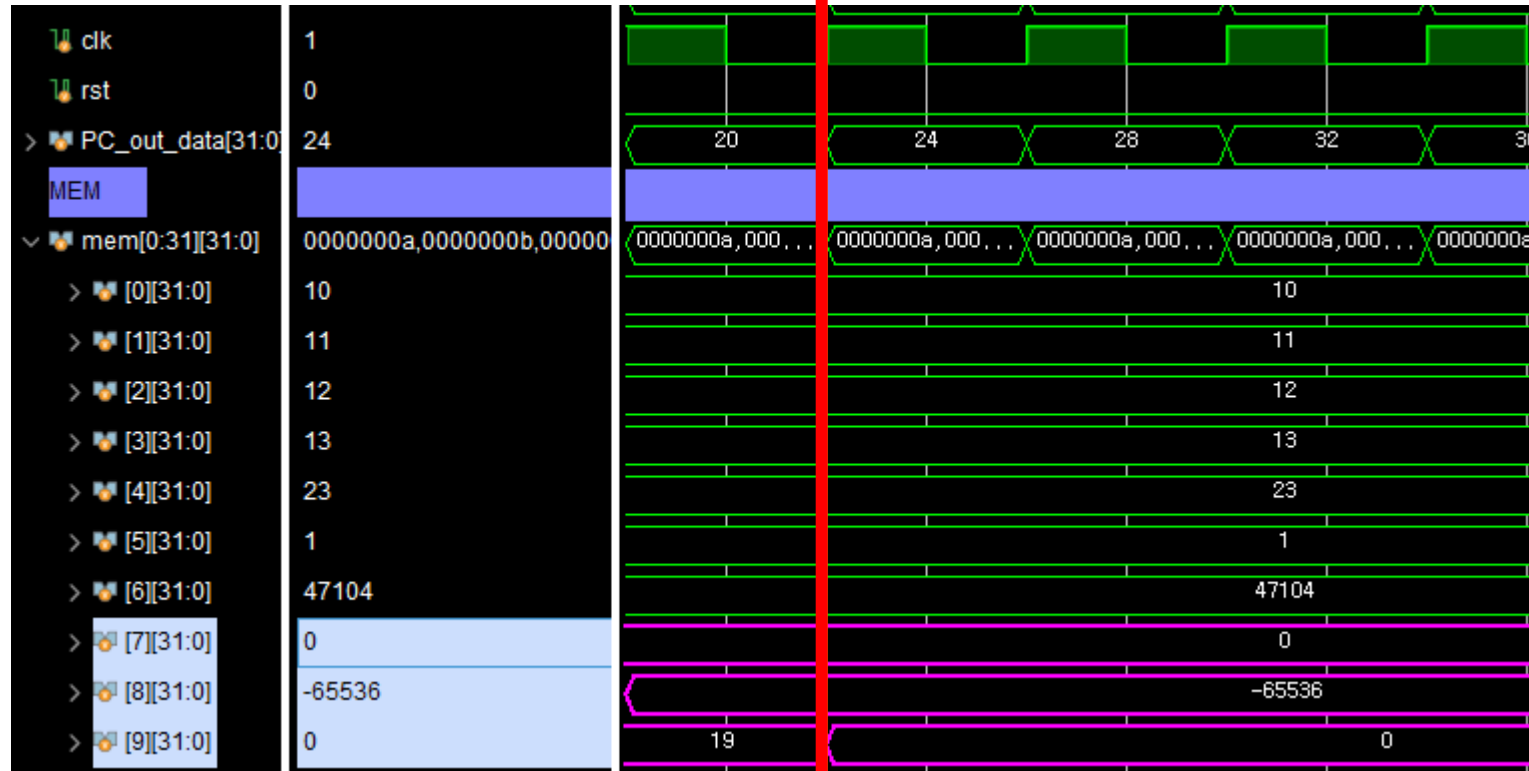
sra x8, x15, x2

X15 = 32'b1111_0000_0000_0000_0000_0000_0000_0000

X2 = 32'd12

X8 = 32'b1111_1111_1111_1111_0000_0000_0000_0000
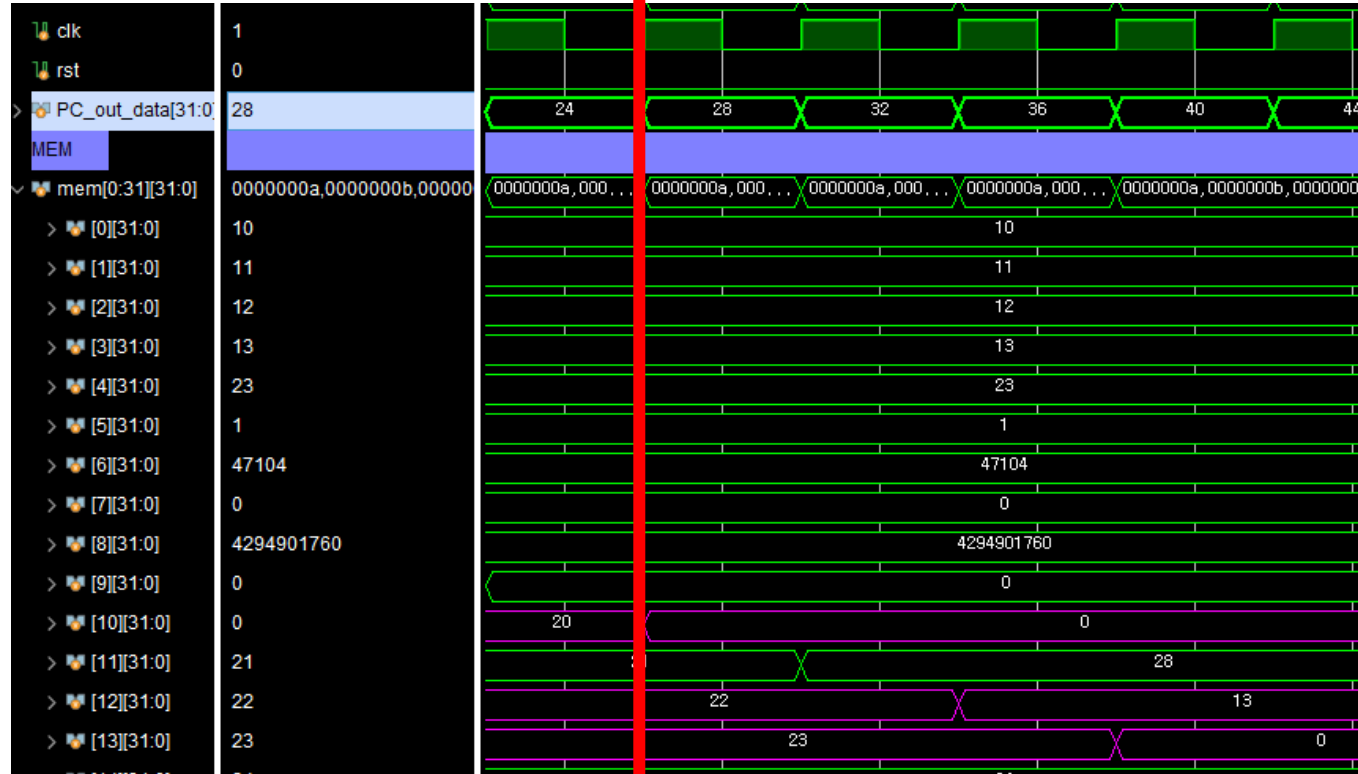
slt x9, x7, x8

X7 = 32'd0

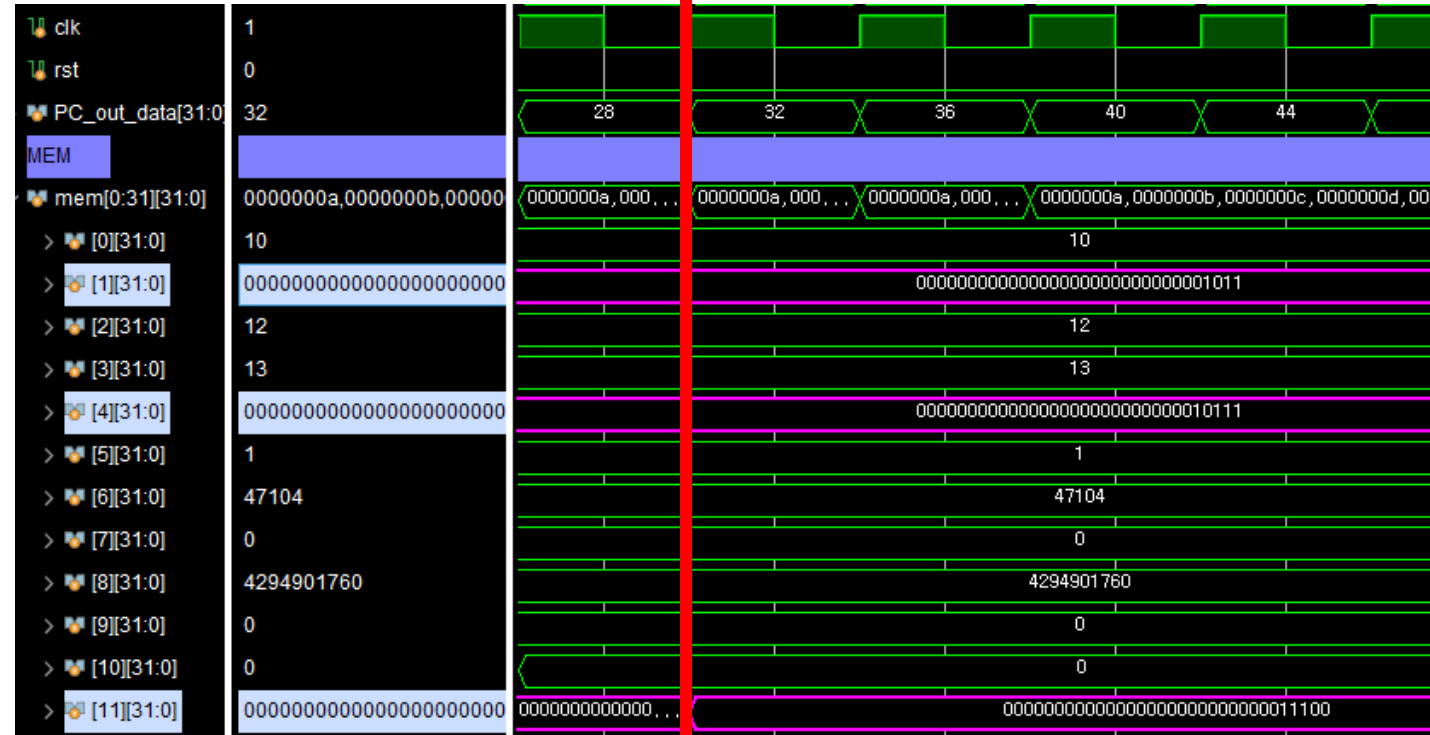X8 = -32'd65536

X9 = 32'd0

sltu x10, x13, x12

X13 = 32'd23

X12 = 32'd22

X10 = 32'd0

xor x11, x4, x1

X4 = 32'b0000_0000_0000_0000_0000_0000_0001_0111

X1 = 32'b0000_0000_0000_0000_0000_0000_0000_1011

X11 = 32'b0000_0000_0000_0000_0000_0000_0001_1100

or x12, x2, x3

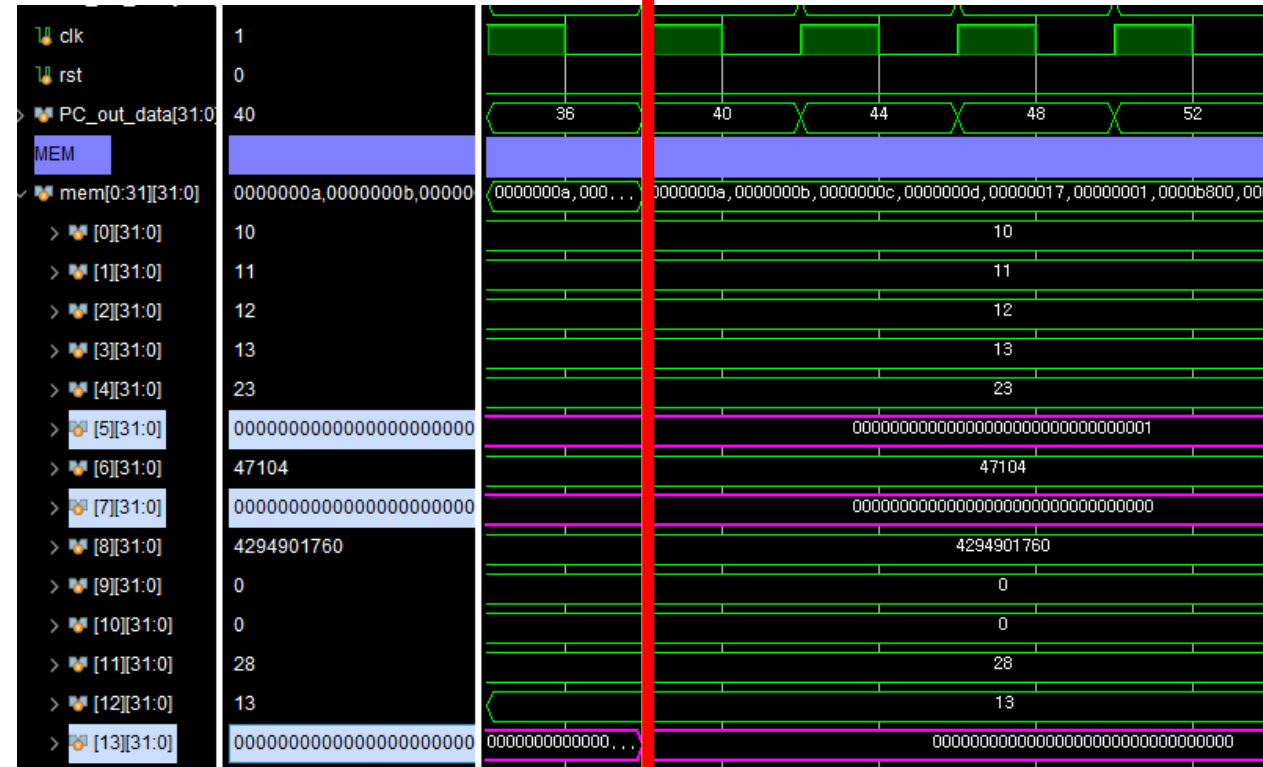X2 = 32'b0000_0000_0000_0000_0000_0000_0000_1100

X3 = 32'b0000_0000_0000_0000_0000_0000_0000_1101

X12 = 32'b0000_0000_0000_0000_0000_0000_0000_1101

and x13, x5, x7

X5 = 32'b0000_0000_0000_0000_0000_0000_0000_0001

X7 = 32'b0000_0000_0000_0000_0000_0000_0000_0000

X13 = 32'b0000_0000_0000_0000_0000_0000_0000_0000