------------------------------------1

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity projeto\_3\_1 is

Port ( A : in BIT\_VECTOR (0 to 2);

SEL : in BIT;

Z : out BIT\_VECTOR (0 to 2));

end projeto\_3\_1;

architecture Behavioral of projeto\_3\_1 is

begin

process (A,SEL)

begin

if (SEL = '0') then Z<= A;

elsif(SEL = '1') then Z<= not(A);

end if;

end process;

end Behavioral;

---------------------------------------2

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity project\_3\_2 is

Port ( num1 : in BIT;

num2 : in BIT;

o : out BIT);

end project\_3\_2;

architecture Behavioral of project\_3\_2 is

begin

process (num1,num2)

begin

if(num1 = num2) then o <='1';

else o <='0';

end if;

end process;

end Behavioral;

---------------------------------------3