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| pinout_diagram**General Description**  Silego SLG~~~~~ is a low power and small form device. The SoC is housed in a PACKAGE\_SIZE PACKAGE package which is optimal for using with small devices.  **Features**   * Low Power Consumption * Pb-Free / RoHS Compliant * Halogen-Free * PACKAGE Package   **Output Summary**   * OUTPUT\_SUMMARY | **Pin Configuration** |

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Block Diagram

Pin Configuration

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| **Pin #** | **Pin Name** | **Type** | **Pin Description** | **Internal**  **Resistor** |
|  |  |  |  |  |

Ordering Information

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| --- | --- |
| **Part Number** | **Package Type** |
| SLG~~~~~[V/M] | [V/M] = PACKAGE |
| SLG~~~~~[V/M]TR | [V/M]TR = PACKAGE - Tape and Reel (3k units) |

Absolute Maximum Conditions

|  |  |  |  |
| --- | --- | --- | --- |
| **Parameter** | **Min.** | **Max.** | **Unit** |
| VDDto GND | -0.3 | VDD\_MAX | V |
| Voltage at input pins | -0.3 | VDD\_MAX | V |
| Current at input pin | -1.0 | 1.0 | mA |
| Storage temperature range | -65 | 125 | °C |
| Junction temperature | -- | 150 | °C |
| ESD Protection (Human Body Model) | 2000 | -- | V |
| ESD Protection (Charged Device Model) | ESD\_CDM | -- | V |
| Moisture Sensitivity Level | 1 | |  |

Electrical Characteristics

(@ 25° C, unless otherwise stated)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Condition/Note** | **Min.** | **Typ.** | **Max.** | **Unit** |
| VDD | Supply Voltage | -- | vddMin | vddTyp | vddMax | V |
| TA | Operating Temperature | -- | tempMin | tempTyp | tempMax | °C |
| IQ | Quiescent Current | Static inputs and floating outputs | -- | I\_Q | -- | µA |
| VO | Maximal Voltage Applied to any PIN in High-Impedance State | -- | -- | -- | VDD | V |
| IO | Maximal Average or DC Current (note 1) | Per Each Chip Side | -- | -- | 90 | mA |

1. Guaranteed by design

I2C Chip Address

|  |  |  |
| --- | --- | --- |
| **HEX** | **BIN** | **DEC** |
| HEX | BIN | DEC |

Description

Truth Tables

Timing Diagram

Typical Application Circuit

Functionality Waveforms

with external 5kΩ pull up resistor

Channel 1 (yellow/top line) –

Channel 2 (light blue/2nd line) –

Channel 3 (magenta /3rd line) –

Channel 4 (blue/bottom line) –

D0 –

D1 –

D2 –

D3 –

D4 –

D5 –

D6 –

D7 –

D8 –

D9 –

D10 –

D11 –

D12 –

D13 –

D14 –

D15 –

PIN#01 (PIN1)

PIN#02 (PIN2)

PIN#03 (PIN3)

PIN#04 (PIN4)

PIN#05 (PIN5)

PIN#06 (PIN6)

PIN#07 (PIN7)

PIN#08 (PIN8)

PIN#09 (PIN9)

PIN#10 (PIN10)

PIN#11 (PIN11)

PIN#12 (PIN12)

PIN#13 (PIN13)

PIN#14 (PIN14)

PIN#15 (PIN15)

PIN#16 (PIN16)

PIN#17 (PIN17)

PIN#18 (PIN18)

PIN#19 (PIN19)

PIN#20 (PIN20)

PIN#21 (PIN21)

PIN#22 (PIN22)

PIN#23 (PIN23)

PIN#24 (PIN24)

PIN#25 (PIN25)

PIN#26 (PIN26)

PIN#27 (PIN27)

PIN#28 (PIN28)

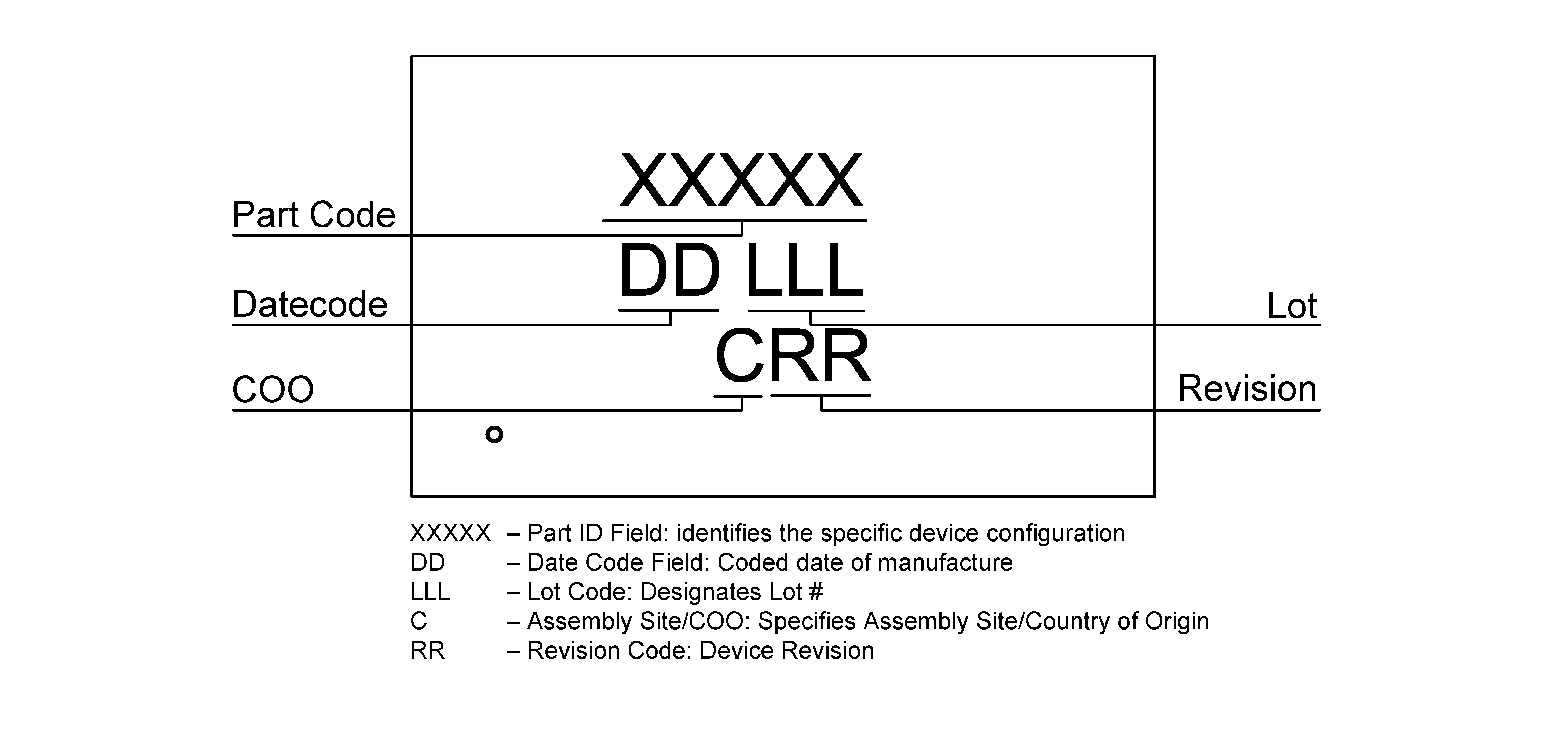
PIN#29 (PIN29)

PIN#30 (PIN30)

PIN#31 (PIN31)

PIN#32 (PIN32)

Package Top Marking



|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Datasheet Revision** | **Programming Code Number** | **Locked Status** | **Part Code** | **Revision** | **Date** |
| DS\_REV\_ALT | PATTERN\_ID | NVM\_LOCK | TM\_PART\_CODE | TM\_REVISION | DATE |

Lock coverage for this part is indicated by √, from one of the following options:

|  |  |
| --- | --- |
|  | Unlocked |

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

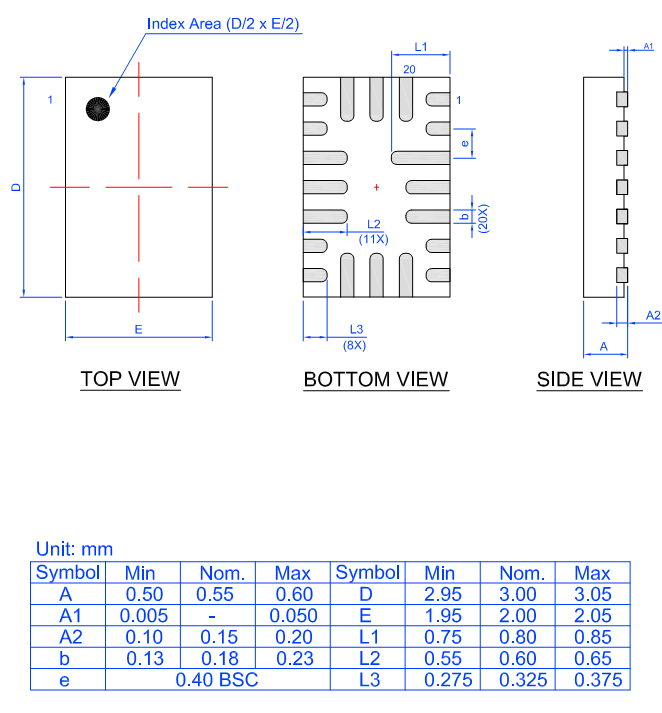
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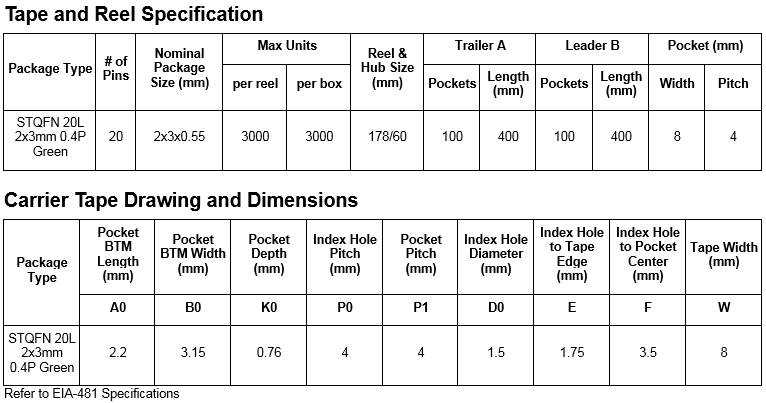
Package Drawing and Dimensions

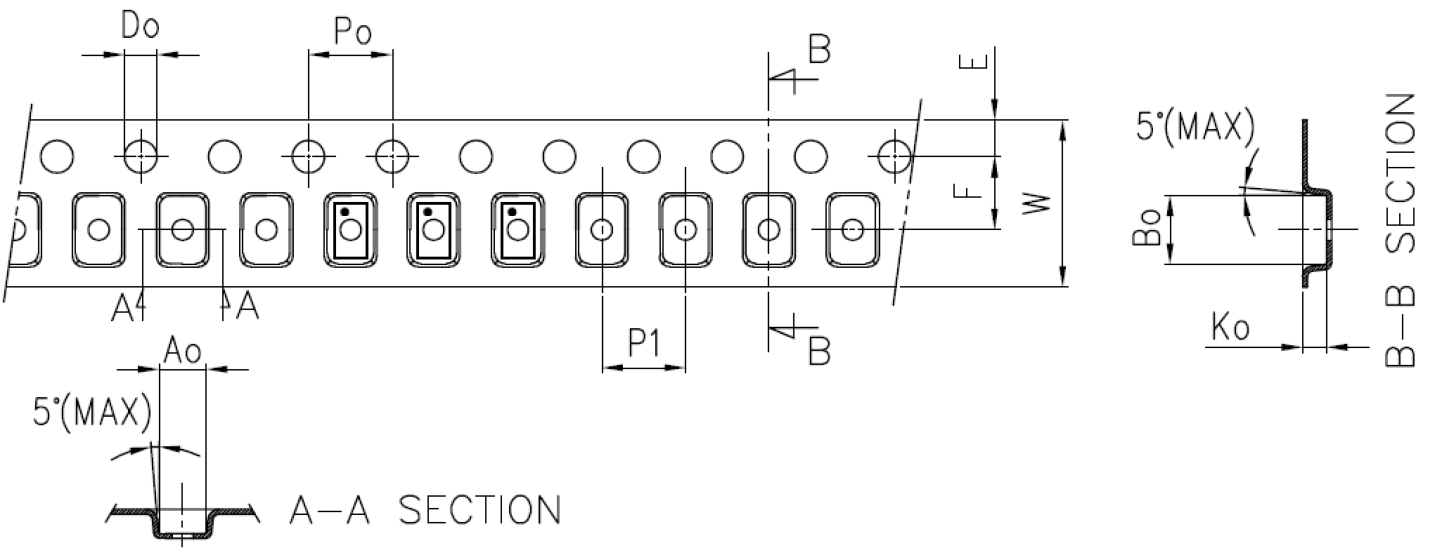
**PIN\_COUNT Lead PACKAGE\_ALT Package**

**JEDEC MO-220**

**IC Net Weight: NET\_WEIGHT**



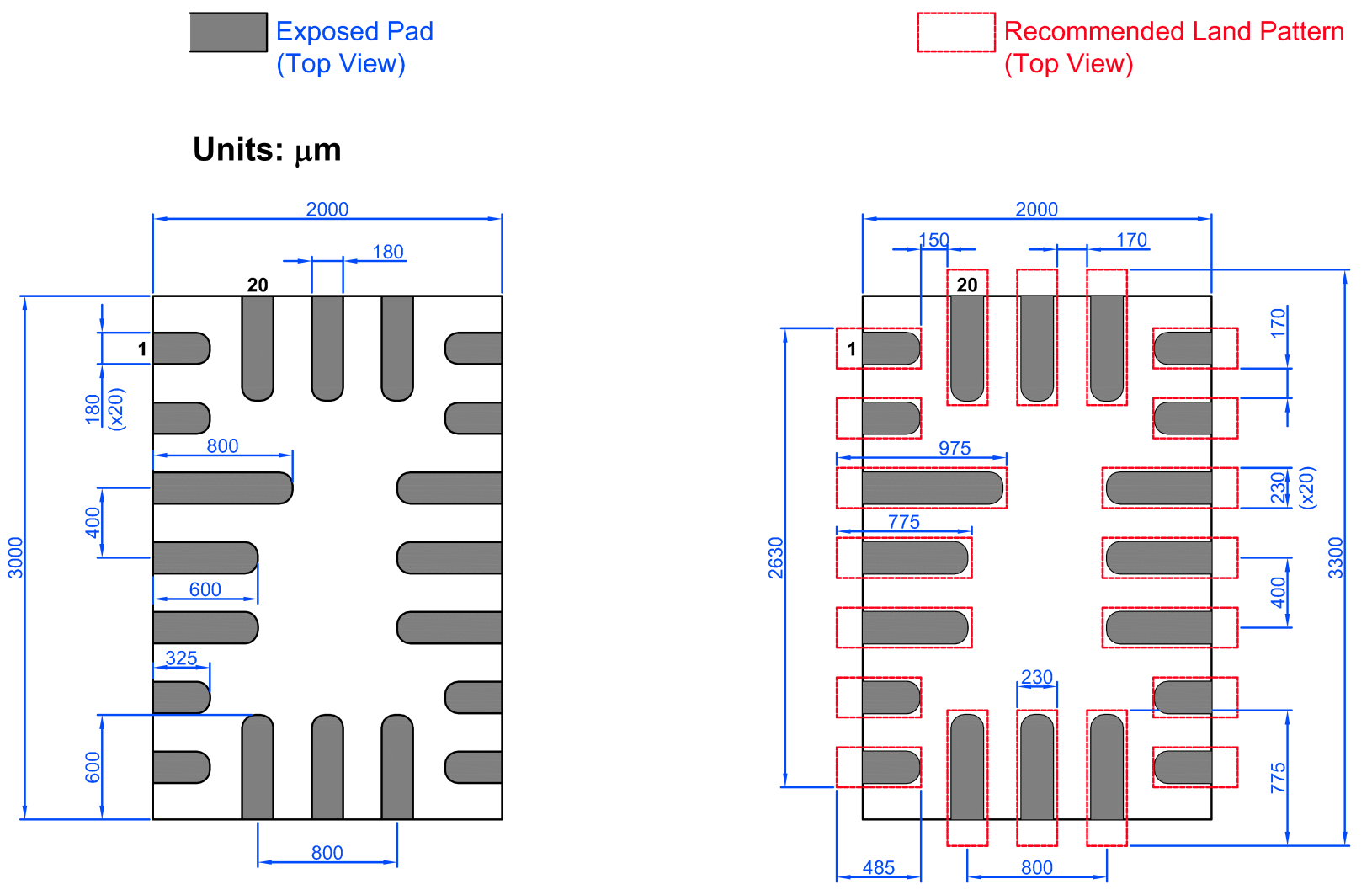




**Recommended Reflow Soldering Profile**

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.3 mm3 (nominal). More information can be found at [www.jedec.org](http://www.jedec.org).

Recommended Land Pattern



Datasheet Revision History

|  |  |  |
| --- | --- | --- |
| **Date** | **Version** | **Change** |
|  |  |  |

Silego Website & Support

**Silego Technology Website**

Silego Technology provides online support via our website at [http://www.silego.com/](http://www.silego.com/.This).This website is used as a means to make files and information easily available to customers.

For more information regarding Silego Green products, please visit:

<http://greenpak.silego.com/>

<http://greenpak2.silego.com/>

<http://greenpak3.silego.com/>

<http://greenfet.silego.com/>

<http://greenfet2.silego.com/>

<http://greenclk.silego.com/>

Products are also available for purchase directly from Silego at the Silego Online Store at <http://www.silego.com/>

**Silego Technical Support**

Datasheets and errata, application notes and example designs, user guides, and hardware support documents and the latest software releases are available at the Silego website or can be requested directly at [info@silego.com.](mailto:info@silego.com.)

For specific GreenPAK design or applications questions and support please send e-mail requests to [GreenPAK@silego.com](mailto:GreenPAK@silego.com)

Users of Silego products can receive assistance through several channels:

**Online Training**

Silego Technology has live training assistance and sales support available at <http://www.silego.com/>. Please contact us to schedule a 1 on 1 training session with one of our application engineers.

**Contact Your Local Sales Representative**

Customers can contact their local sales representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. More information regarding your local representative is available at the Silego website or send a request to [info@silego.com](mailto:info@silego.com)

**Contact Silego Directly**

Silego can be contacted directly via e-mail at [info@silego.com](mailto:info@silego.com) or user submission form, located at the following URL:

<http://support.silego.com/>

**Other Information**

The latest Silego Technology press releases, listing of seminars and events, listings of worldwide Silego Technology offices and representatives are all available at <http://www.silego.com/>

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