MODULE CONFIGURATIONS

Non-ECC

V/I Part Number	Capacity	Module Configuration	Device Configuration	Module Height (in.)	Module Ranks	Performance	CAS Latency
VR4CU166428C(*)H	128MB	16M x 64	16M x 8 bit (8)	1.25	1	PC2100	CL2.5
VR4CU166428C(*)K	128MB	16M x 64	16M x 8 bit (8)	1.25	1	PC2700	CL2.5
VR4CU166428C(*)P	128MB	16M x 64	16M x 8 bit (8)	1.25	1	PC3200	CL3
VR4CU326428C(*)H	256MB	32M x 64	16M x 8 bit (16)	1.25	2	PC2100	CL2.5
VR4CU326428C(*)K	256MB	32M x 64	16M x 8 bit (16)	1.25	2	PC2700	CL2.5
VR4CU326428C(*)P	256MB	32M x 64	16M x 8 bit (16)	1.25	2	PC3200	CL3
VR4CU326428D(*)H	256MB	32M x 64	32M x 8 bit (8)	1.25	1	PC2100	CL2.5
VR4CU326428D(*)K	256MB	32M x 64	32M x 8 bit (8)	1.25	1	PC2700	CL2.5
VR4CU326428D(*)P	256MB	32M x 64	32M x 8 bit (8)	1.25	1	PC3200	CL3
VR4CU646428D(*)H	512MB	64M x 64	32M x 8 bit (16)	1.25	2	PC2100	CL2.5
VR4CU646428D(*)K	512MB	64M x 64	32M x 8 bit (16)	1.25	2	PC2700	CL2.5
VR4CU646428D(*)P	512MB	64M x 64	32M x 8 bit (16)	1.25	2	PC3200	CL3
VR4CU646428E(*)H	512MB	64M x 64	64M x 8 bit (8)	1.25	1	PC2100	CL2.5
VR4CU646428E(*)K	512MB	64M x 64	64M x 8 bit (8)	1.25	1	PC2700	CL2.5
VR4CU646428E(*)P	512MB	64M x 64	64M x 8 bit (8)	1.25	1	PC3200	CL3
VR4CU286428E(*)H	1GB	128M x 64	64M x 8 bit (16)	1.25	2	PC2100	CL2.5
VR4CU286428E(*)K	1GB	128M x 64	64M x 8 bit (16)	1.25	2	PC2700	CL2.5
VR4CU286428E(*)P	1GB	128M x 64	64M x 8 bit (16)	1.25	2	PC3200	CL3
VR4CU566428F(*)H	2GB	256M x 64	128M x 8 bit (16)	1.25	2	PC2100	CL2.5
VR4CU566428F(*)K	2GB	256M x 64	128M x 8 bit (16)	1.25	2	PC2700	CL2.5
VR4CU566428F(*)P	2GB	256M x 64	128M x 8 bit (16)	1.25	2	PC3200	CL3

Note: 1. (*) indicates device package: T= TSOP, B= FBGA.
2. Module height for FBGA versions is 1.0 inches (25.4mm).

ECC

V/I Part Number	Capacity	Module Configuration	Device Configuration	Module Height (in.)	Module Ranks	Performance	CAS Latency
VR4CU167228C(*)H	128MB	16M x 72	16M x 8 bit (9)	1.25	1	PC2100	CL2.5
VR4CU167228C(*)K	128MB	16M x 72	16M x 8 bit (9)	1.25	1	PC2700	CL2.5
VR4CU167228C(*)P	128MB	16M x 72	16M x 8 bit (9)	1.25	1	PC3200	CL3
VR4CU327228C(*)H	256MB	32M x 72	16M x 8 bit (18)	1.25	2	PC2100	CL2.5
VR4CU327228C(*)K	256MB	32M x 72	16M x 8 bit (18)	1.25	2	PC2700	CL2.5
VR4CU327228C(*)P	256MB	32M x 72	16M x 8 bit (18)	1.25	2	PC3200	CL3
VR4CU167228C(*)H	128MB	16M x 72	16M x 8 bit (9)	1.25	1	PC2100	CL2.5
VR4CU167228C(*)K	128MB	16M x 72	16M x 8 bit (9)	1.25	1	PC2700	CL2.5
VR4CU167228C(*)P	128MB	16M x 72	16M x 8 bit (9)	1.25	1	PC3200	CL3
VR4CU327228C(*)H	256MB	32M x 72	16M x 8 bit (18)	1.25	2	PC2100	CL2.5
VR4CU327228C(*)K	256MB	32M x 72	16M x 8 bit (18)	1.25	2	PC2700	CL2.5
VR4CU327228C(*)P	256MB	32M x 72	16M x 8 bit (18)	1.25	2	PC3200	CL3

ECC (cont'd)

V/I Part Number	Capacity	Module Configuration	Device Configuration	Module Height (in.)	Module Ranks	Performance	CAS Latency
VR4CU327228D(*)G	256MB	32M x 72	32M x 8 bit (9)	1.25	1	PC2100	CL2
VR4CU327228D(*)H	256MB	32M x 72	32M x 8 bit (9)	1.25	1	PC2100	CL2.5
VR4CU327228D(*)K	256MB	32M x 72	32M x 8 bit (9)	1.25	1	PC2700	CL2.5
VR4CU327228DTK01	256MB	32M x 72	32M x 8 bit (9)	1.125	1	PC2700	CL2.5
VR4CU327228D(*)P	256MB	32M x 72	32M x 8 bit (9)	1.125	1	PC3200	CL3
VR4CU647228D(*)H	512MB	64M x 72	32M x 8 bit (18)	1.25	2	PC2100	CL2.5
VR4CU647228D(*)K	512MB	64M x 72	32M x 8 bit (18)	1.25	2	PC2700	CL2.5
VR4CU647228D(*)P	512MB	64M x 72	32M x 8 bit (18)	1.25	2	PC3200	CL3
VR4CU647228DTP01	512MB	64M x 72	32M x 8 bit (18)	1.125	2	PC3200	CL3
VR4CU647228E(*)H	512MB	64M x 72	64M x 8 bit (9)	1.25	1	PC2100	CL2.5
VR4CU647228E(*)K	512MB	64M x 72	64M x 8 bit (9)	1.25	1	PC2700	CL2.5
VR4CU647228ETK01	512MB	64M x 72	64M x 8 bit (9)	1.125	1	PC2700	CL2.5
VR4CU647228E(*)P	512MB	64M x 72	64M x 8 bit (9)	1.25	1	PC3200	CL3
VR4CU287228E(*)H	1GB	128M x 72	64M x 8 bit (18)	1.25	2	PC2100	CL2.5
VR4CU287228E(*)K	1GB	128M x 72	64M x 8 bit (18)	1.25	2	PC2700	CL2.5
VR4CU287228ETK01	1GB	128M x 72	64M x 8 bit (18)	1.125	2	PC2700	CL2.5
VR4CU287228E(*)P	1GB	128M x 72	64M x 8 bit (18)	1.125	2	PC3200	CL3
VR4CU567228F(*)H	2GB	256M x 72	128M x 8 bit (18)	1.25	2	PC2100	CL2.5
VR4CU567228F(*)K	2GB	256M x 72	128M x 8 bit (18)	1.25	2	PC2700	CL2.5
VR4CU567228F(*)P	2GB	256M x 72	128M x 8 bit (18)	1.25	2	PC3200	CL3

Note: 1. (*) indicates device package: T= TSOP, B= FBGA.
2. Module height for FBGA versions is 1.0 inches (25.4mm).

Features

- Single Power Supply: 2.5V ± 0.2V (266MHz, 333MHz) or 2.6V ± 0.1V (400MHz)
- Double Data Rate architecture; two data transfers per clock cycle.
- Source-synchronous data strobes.
- Differential clock inputs (CLK, #CLK).
- MRS cycle with address key programs.
  - Read CAS latency
  - Burst Length (2, 4, and 8)
  - Burst type (Sequential & Interleave)
- All inputs except Data & DM are sampled at the positive edge of the system clock.
- Auto & Self-Refresh.
- 4k/15.625us (128Mbit) and 8k/8.125us (256Mb, 512Mb, 1Gb) average Refresh Period.
- Serial Presence Detect with EEPROM.
- RoHS Compliant* (see last page)

PIN CONFIGURATIONS

Pin		Pin		Pin		Pin		Pin		Pin		Pin		Pin	
1	VREF	24	DQ17	47	†DQS8	70	VDD	93	GND	116	GND	139	GND	162	DQ47
2	DQ0	25	DQS2	48	A0	71	*#CS2	94	DQ4	117	DQ21	140	† DM8	163	* #CS3
3	GND	26	GND	49	† CB2	72	DQ48	95	DQ5	118	A11	141	A10	164	VDDQ
4	DQ1	27	A9	50	GND	73	DQ49	96	VDDQ	119	DM2	142	† CB6	165	DQ52
5	DQS0	28	DQ18	51	† CB3	74	GND	97	DM0	120	VDD	143	VDDQ	166	DQ53
6	DQ2	29	A7	52	BA1	75	#CLK2	98	DQ6	121	DQ22	144	† CB7	167	¶ A13
7	VDD	30	VDDQ	53	DQ32	76	CLK2	99	DQ7	122	A8	145	GND	168	VDD
8	DQ3	31	DQ19	54	VDDQ	77	VDDQ	100	GND	123	DQ23	146	DQ36	169	DM6
9	NC	32	A5	55	DQ33	78	DQS6	101	NC	124	GND	147	DQ37	170	DQ54
10	*#RST	33	DQ24	56	DQS4	79	DQ50	102	NC	125	A6	148	VDD	171	DQ55
11	GND	34	GND	57	DQ34	80	DQ51	103	NC	126	DQ28	149	DM4	172	VDDQ
12	DQ8	35	DQ25	58	GND	81	GND	104	VDDQ	127	DQ29	150	DQ38	173	NC
13	DQ9	36	DQS3	59	BA0	82	*VDDID	105	DQ12	128	VDDQ	151	DQ39	174	DQ60
14	DQS1	37	A4	60	DQ35	83	DQ56	106	DQ13	129	DM3	152	GND	175	DQ61
15	VDDQ	38	VDD	61	DQ40	84	DQ57	107	DM1	130	A3	153	DQ44	176	GND
16	CLK1	39	DQ26	62	VDDQ	85	VDD	108	VDD	131	DQ30	154	#RAS	177	DM7
17	#CLK1	40	DQ27	63	#WE	86	DQS7	109	DQ14	132	GND	155	DQ45	178	DQ62
18	GND	41	A2	64	DQ41	87	DQ58	110	DQ15	133	DQ31	156	VDDQ	179	DQ63
19	DQ10	42	GND	65	#CAS	88	DQ59	111	** CKE1	134	† CB4	157	#CS0	180	VDDQ
20	DQ11	43	A1	66	GND	89	GND	112	VDDQ	135	† CB5	158	** #CS1	181	SA0
21	CKE0	44	† CB0	67	DQS5	90	NC	113	* BA2	136	VDDQ	159	DM5	182	SA1
22	VDDQ	45	† CB1	68	DQ42	91	SDA	114	DQ20	137	CLK0	160	GND	183	SA2
23	DQ16	46	VDD	69	DQ43	92	SCL	115	§ A12	138	#CLK0	161	DQ46	184	VDDSPD

* Pins are not used in this module
** Pins are not connected or used on single rank modules
† Pins are not connected or used on non-ECC (64 bit) modules.
§ Pin is not used on modules based on 128Mbit devices (Cxx at end of PN).
¶ Pin is used on modules based on 1Gbit devices (Fxx at end of PN)

ADDRESSING

DDR Device →	128Mbit (Cxx suffix)	256Mbit (Dxx suffix)	512Mbit (Exx suffix)	1Gbit (Fxx suffix)
Row address	A0 ~ A11	A0 ~ A12	A0 ~ A12	A0 ~ A13
Column address	A0 ~ A9	A0 ~ A9	A0 ~ A9, A11	A0 ~ A9, A11
Device banks	BA0 ~ BA1 (4)	BA0 ~ BA1 (4)	BA0 ~ BA1 (4)	BA0 ~ BA1 (4)
Refresh Count	4k	8k	8k	8k

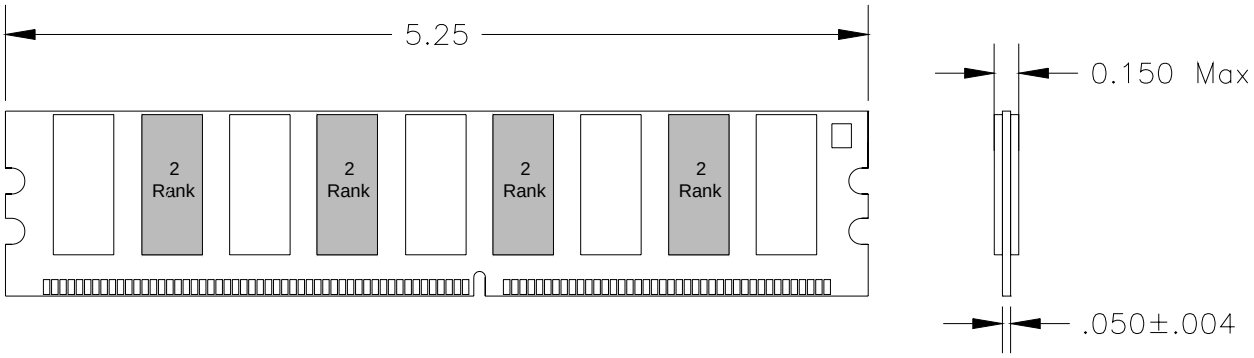
PIN FUNCTION DESCRIPTION

SIGNAL	FUNCTION	DIRECTION	DESCRIPTION
A0 ~ An	Address	Input	Provides row / column addresses on the rising edge of CLK. During a PRECHARGE command, a VIH level on A10 precharges all device banks and a VIL level precharges one bank selected by BA0~BAn. During a MRS command, address lines provide the op code.
BA0 ~ BAn	Bank Select Address	Input	Selects device bank that a command is applied to.
CLK0 ~ CLK2, #CLK0 ~ #CLK2	Master Clock	Input	Differential module clock used to sample address, control, and data lines. The timing reference point for address and control is the positive edge of CLK; output data and DQS are defined by CLK and #CLK crossing.
CKE0, CKE1	Clock Enable	Input	Disables (low) or activates (high) internal device clocks, inputs, and buffers. Provides power savings during Precharge Power-Down, Self-Refresh, and Active Power-Down operations. CKE enters and exits all modes synchronously except for output buffer disable and Self-Refresh exit which are asynchronous. CKE must be kept high for Read and Write operations.
#CS0, #CS1	Chip Select	Input	Command bit used to enable (low) or mask (high) incoming commands on the positive clock edge.
#CAS, #RAS, #WE	Command bits	Input	Define the command being entered on the positive clock edge.
DQ0 ~ DQ63	Data input/output	Bi-directional	Data inputs / outputs.
CB0 ~ CB7	Check Bit	Bi-directional	ECC check bits.
DQS0 ~ DQS8	Data Strobe	Bi-directional	Source-synchronous signal, edge-aligned output with read data and center-aligned input with write data.
DM0 ~ DM8	Data Mask	Input	Masks write data if high. Sampled on both the rising and falling edges of the DQS.
#RST	Reset	Input	Asynchronously sets register outputs low during initialization.
SDA	EEPROM Data	Bi-directional	Transfers serial address and data to/from the SPD EEPROM. Open drain, requires external pullup to VDDSPD.
SCL	EEPROM Clock	Input	Clock signal for the SPD EEPROM. Requires external pullup to VDDSPD.
SA0 ~ SA2	EEPROM Select	Input	Tied to either GND or VDDSPD on the motherboard to configure the SPD EEPROM address range.
VREF	Reference Supply	Power Input	SDRAM reference I/O power supply.
VDDQ	I/O Supply Voltage	Power Input	Power supply voltage for data and DQS buffers.
VDDSPD	SPD power	Power Input	SPD EEPROM power, 2.2 to 5.5V.
VDDID	VDD Identification Flag	Output	A no connect / open indicates that VDD = VDDQ.
VDD/GND	Power Supply/ Ground	Power Input	Module power / ground supply
NC	N/A	N/A	No Connection

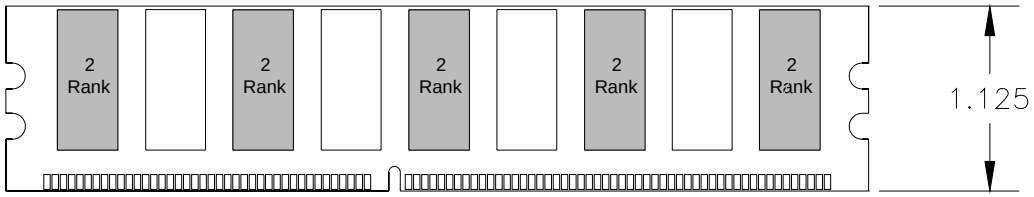
MECHANICAL OUTLINE, 1.125” HIGH MODULE

All dimensions are in inches. Tolerance is +/- 0.005, unless otherwise specified.

FRONT



BACK

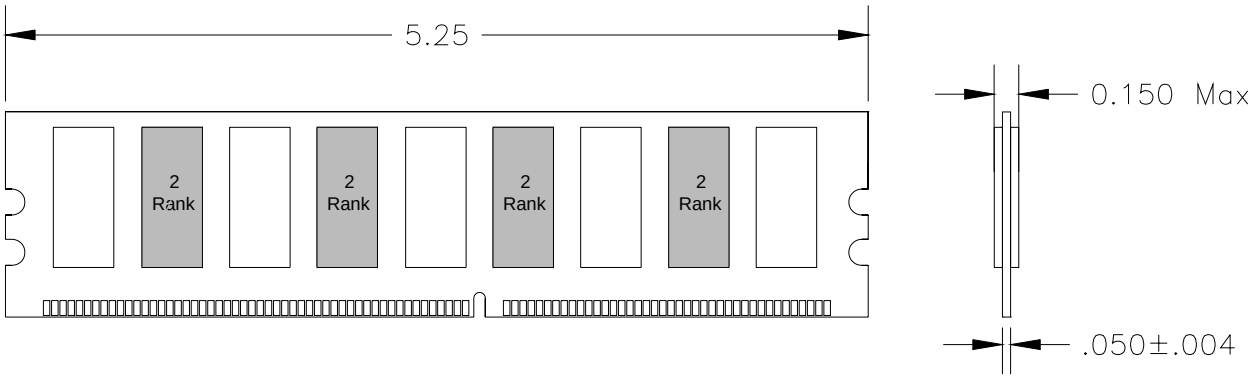


MD_00981_a

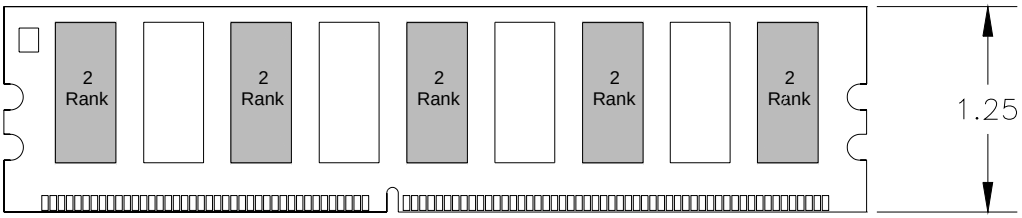
MECHANICAL OUTLINE, 1.25” HIGH MODULE

All dimensions are in inches. Tolerance is +/- 0.005, unless otherwise specified.

FRONT



BACK

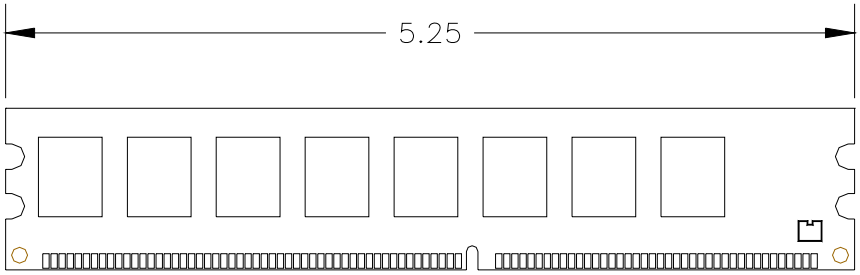


MD_00927_a

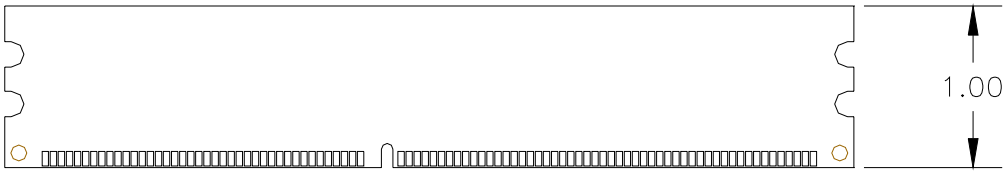
MECHANICAL OUTLINE, 1.0” HIGH MODULE

All dimensions are in inches. Tolerance is +/- 0.005, unless otherwise specified.

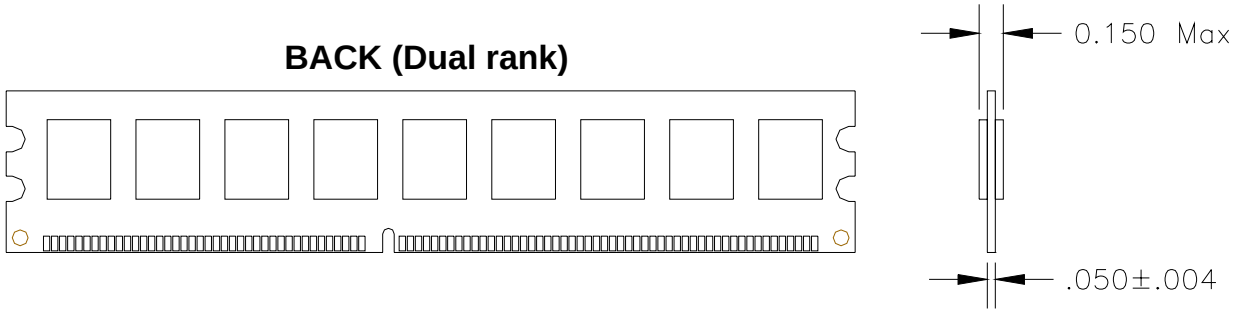
FRONT



BACK (Single rank)

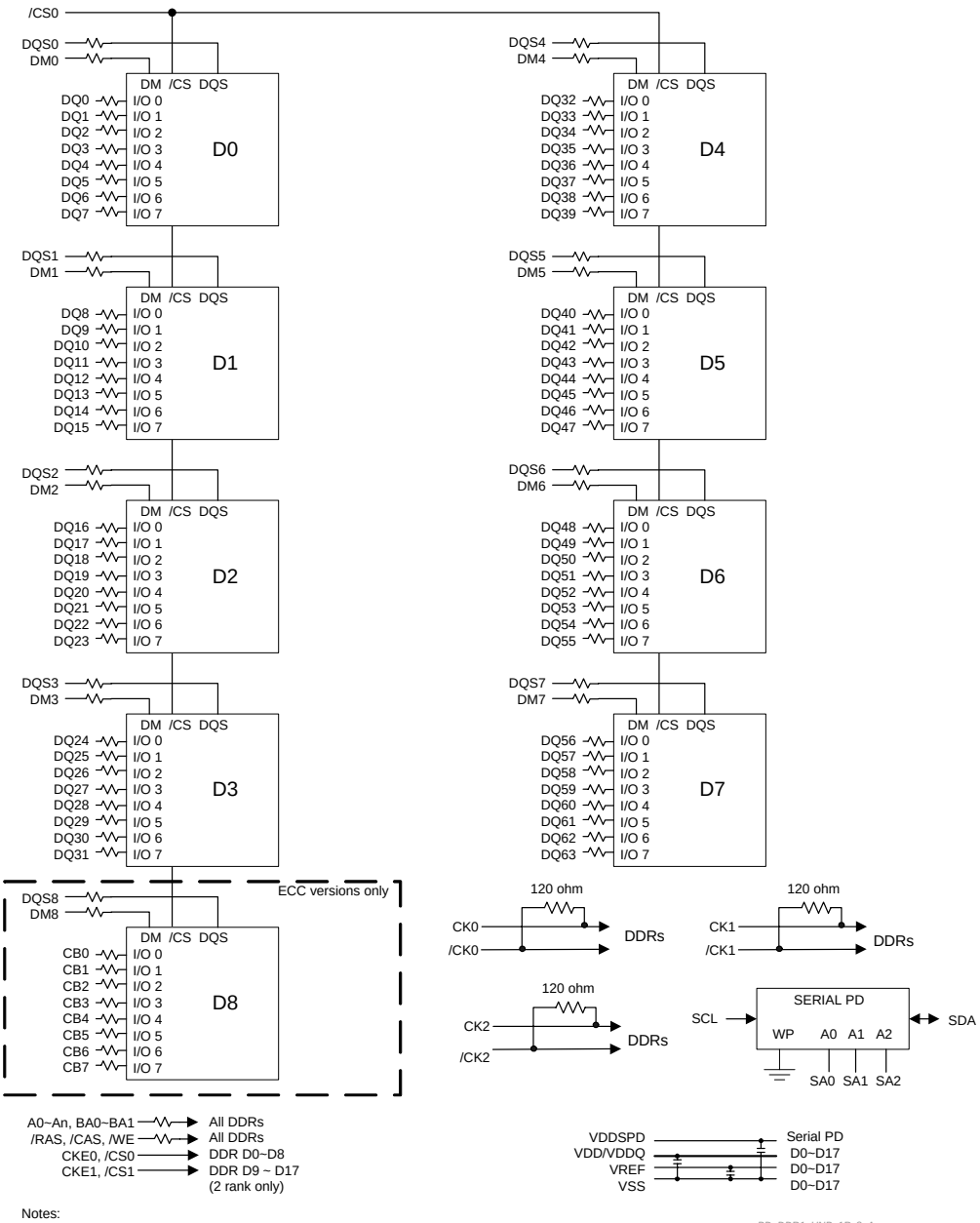


BACK (Dual rank)



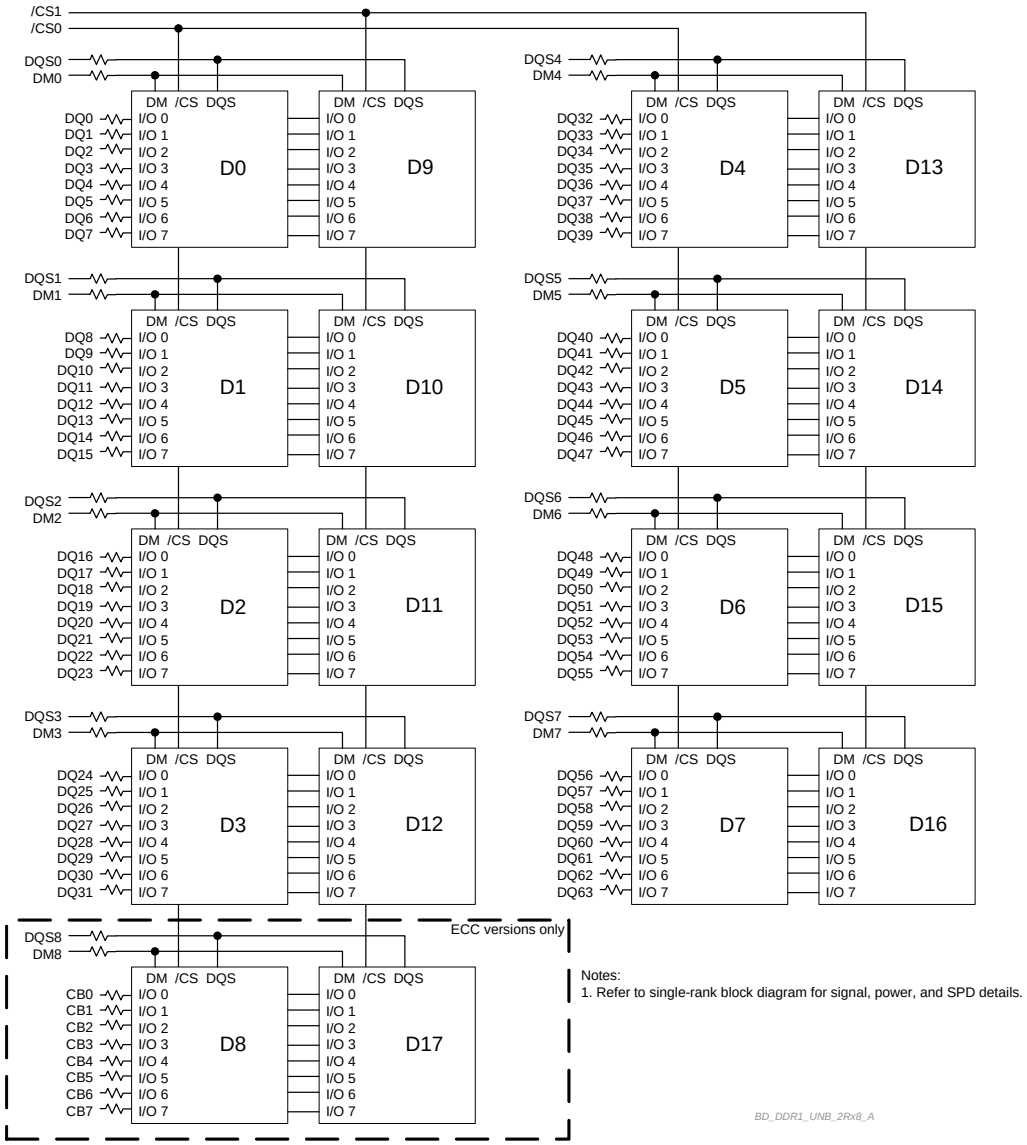
MD_01036_a

FUNCTIONAL BLOCK DIAGRAM SINGLE RANK



Notes:
1. Unless otherwise noted, resistor values are 22 Ohms +/- 5% on DQ, CB, and DM and 3 Ohms +/- 5% on address/control.

FUNCTIONAL BLOCK DIAGRAM DUAL RANK



Notes:
1. Refer to single-rank block diagram for signal, power, and SPD details.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to GND	Vin, Vout	-0.5 ~ 3.6	V
Voltage on VCC supply relative to GND	VDD, VDDQ	-1.0 ~ 3.6	V
Storage temperature	TSTG	-55 ~ +150	°C
Power dissipation	PD	1.5 x number of devices	W
Short circuit current	Ios	50	mA

Note:

1. Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.
2. Functional operation should be restricted to recommended operating condition.
3. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS (SSTL_2)

Recommended operating conditions (Voltages referenced to GND, TA = 0 to 70°C)

Parameter			Symbol	Min.	Max.	Unit
Operating Temperature			TOPR	0	70	ºC
Supply voltage		266, 333	VDD	2.3	2.7	V
		400	VDD	2.5	2.7	V
Supply voltage for DQ, DQS		266, 333	VDDQ	2.3	2.7	V
		400	VDDQ	2.5	2.7	V
Input reference voltage			VREF	0.49 x VCCQ	0.51 x VCCQ	V
EEPROM Supply Voltage			VDDSPD	1.7	3.6	V
Termination voltage (system)			VTT	VREF - 0.04	VREF + 0.04	V
Input high voltage			VIH	VREF + 0.15	VCCQ + 0.3	V
Input low voltage			VIL	-0.3	VREF - 0.15	V
Input leakage current, Non-ECC	(A0 ~ An, BA0 ~ BAn)	Single Rank	IIL(1)	-16	16	µA
		Dual Rank		-32	-32	
	(#CS0, *#CS1, CKE0, *CKE1)	Single Rank	IIL(2)	-16	16	µA
		Dual Rank				
	(#RAS, #CAS, #WE)	Single Rank	IIL(3)	-16	16	µA
		Dual Rank		-32	-32	
Input leakage current, ECC	(A0 ~ An, BA0 ~ BAn)	Single Rank	IIL(1)	-18	18	µA
		Dual Rank		-36	-36	
	(#CS0, *#CS1, CKE0, *CKE1)	Single Rank	IIL(2)	-18	18	µA
		*Dual Rank				
	(#RAS, #CAS, #WE)	Single Rank	IIL(3)	-18	18	µA
		Dual Rank		-36	36	
Output leakage current		Single Rank	IOL	-5	-5	µA
		Dual Rank		-10	10	

*Used in dual rank module only

CAPACITANCE (VDD = 2.5V, TA = 0 to 70ºC)

Parameter	Symbol	Min		Max		Unit
		Single Rank	Dual Ranks	Single Rank	Dual Ranks	
Input capacitance, Non-ECC (A0 ~ An, BA0 ~ BAn)	CIN1	17	29	29	53	pF
Input capacitance, Non-ECC (#RAS, #CAS, #WE)	CIN2	17	29	29	53	pF
Input capacitance, Non-ECC (CKE0, *CKE1)	CIN3	17		29		pF
Input capacitance, Non-ECC (#CS0, *#CS1)	CIN4	17		29		pF
Input capacitance, ECC (A0 ~ An, BA0 ~ BAn)	CIN1	18.5	32	32	59	pF
Input capacitance, ECC (#RAS, #CAS, #WE)	CIN2	18.5	32	32	59	pF
Input capacitance, ECC (CKE0, *CKE1)	CIN3	18.5		32		pF
Input capacitance, ECC (#CS0, *#CS1)	CIN4	18.5		32		pF
Input capacitance (CLK0, #CLK0 ~ CLK2, #CLK2)	CIN5a	9.5	14	14	23	pF
Input capacitance (DQS0 ~ DQS7, DM0 ~ DM7)	CIN6	8.5	12	10	15	pF
Data input/output capacitance (DQ0 ~ DQ63, CB0 ~ CB7)	COUTa	8.5	12	10	15	pF

*Used in dual rank module only

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted, TA = 0 to 70 °C)

Parameter	Symbol	Test Condition	Unit	Note
Operating Current (one bank; active / precharge)	IDD0	tRC = tRC(min); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle.	mA	1, 2
Operating Current (one bank; active / read / precharge)	IDD1	Burst Length = 4; tRC = tRC(min); IO = 0 mA; address and control inputs changing once per clock cycle	mA	1, 2
Precharge Standby (Power-down mode)	IDD2P	CKE ≤ VIL(max)	mA	1, 3
Idle Standby Current	IDD2F	CKE ≥ VIH(min); CS ≥ VIH(min); all banks idle; address and control inputs changing once per clock cycle	mA	1, 3
Active Power-down Standby Current (one bank active; power-down mode)	IDD3P	CKE ≤ VIL(max)	mA	1, 3
Active Standby Current (one bank; active / precharge)	IDD3N	CKE ≥ VIH(min); CS ≥ VIH(min); tRC = tRAS(max); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	mA	1, 3
Operating Current (Burst read)	IDD4R	One bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; IO = 0mA	mA	1, 2
Operating Current (Burst write)	IDD4W	One bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle	mA	1, 2
Auto-Refresh Current	IDD5	tRC = tRFC(min)	mA	1, 3
Self Refresh Current	IDD6	CKE ≤ 0.2V	mA	1, 3
Operating Current (Four Bank Operation)	IDD7	Four bank interleaving with BL=4	mA	1, 2

Note: 1. Calculated values are from component data. Currents are for DDR SDRAM components only.
2. Active rank is in the IDD current mode shown, all other ranks are in IDD2P Precharge Power-Down Standby Current mode.
3. All ranks are in the same IDD current mode.

IDD CHARACTERISTICS- SINGLE RANK 128Mb, Non-ECC

Symbol	VR4CU16642C(*)H PC2100 CL2.5	VR4CU166428C(*)K PC2700 CL2.5	VR4CU166428C(*)P PC3200 CL3 (3-3-3)	Unit
IDD0	600	680	800	mA
IDD1	800	880	1000	mA
IDD2P	24	24	24	mA
IDD2F	160	176	240	mA
IDD3P	200	200	200	mA
IDD3N	280	320	320	mA
IDD4R	960	1120	1280	mA
IDD4W	1000	1160	1360	mA
IDD5	1240	1320	1440	mA
IDD6	16	16	16	mA
IDD7	2000	2400	2800	mA

IDD CHARACTERISTICS- DUAL RANK 128Mb, Non-ECC

Symbol	VR4CU326428C(*)H PC2100 CL2.5	VR4CU326428C(*)K PC2700 CL2.5	VR4CU326428C(*)P PC3200 CL3 (3-3-3)	Unit
IDD0	624	704	824	mA
IDD1	824	904	1024	mA
IDD2P	48	48	48	mA
IDD2F	320	352	480	mA
IDD3P	400	400	400	mA
IDD3N	560	640	640	mA
IDD4R	984	1144	1304	mA
IDD4W	1024	1184	1384	mA
IDD5	1264	1344	1464	mA
IDD6	32	32	32	mA
IDD7	2024	2424	2824	mA

IDD CHARACTERISTICS- SINGLE RANK 256Mb, Non-ECC

Symbol	VR4CU326428D(*)H PC2100 CL2.5	VR4CU326428D(*)K PC2700 CL2.5	VR4CU326428D(*)P PC3200 CL3 (3-3-3)	Unit
IDD0	640	720	840	mA
IDD1	840	920	1040	mA
IDD2P	24	24	32	mA
IDD2F	200	240	240	mA
IDD3P	240	280	400	mA
IDD3N	360	440	520	mA
IDD4R	1080	1200	1360	mA
IDD4W	1080	1200	1360	mA
IDD5	1280	1360	1440	mA
IDD6	24	24	24	mA
IDD7	2000	2240	2400	mA

IDD CHARACTERISTICS- DUAL RANK 256Mb, Non-ECC

Symbol	VR4CU646428D(*)H PC2100 CL2.5	VR4CU646428D(*)K PC2700 CL2.5	VR4CU646428D(*)P PC3200 CL3 (3-3-3)	Unit
IDD0	664	744	872	mA
IDD1	864	944	1072	mA
IDD2P	48	48	64	mA
IDD2F	400	480	480	mA
IDD3P	480	560	800	mA
IDD3N	720	880	960	mA
IDD4R	1104	1224	1392	mA
IDD4W	1104	1224	1392	mA
IDD5	2560	2720	2880	mA
IDD6	48	48	48	mA
IDD7	2024	2264	2432	mA

IDD CHARACTERISTICS- SINGLE RANK 512Mb, Non-ECC

Symbol	VR4CU646428E(*)H PC2100 CL2.5	VR4CU646428E(*)K PC2700 CL2.5	VR4CU646428E(*)P PC3200 CL3 (3-3-3)	Unit
IDD0	760	840	960	mA
IDD1	1000	1080	1200	mA
IDD2P	40	40	40	mA
IDD2F	240	240	240	mA
IDD3P	240	240	360	mA
IDD3N	360	360	480	mA
IDD4R	1000	1120	1240	mA
IDD4W	1040	1200	1400	mA
IDD5	1560	1640	1760	mA
IDD6	40	40	40	mA
IDD7	2600	2880	3080	mA

IDD CHARACTERISTICS- DUAL RANK 512Mb, Non-ECC

Symbol	VR4CU286428E(*)H PC2100 CL2.5	VR4CU286428E(*)K PC2700 CL2.5	VR4CU286428E(*)P PC3200 CL3 (3-3-3)	Unit
IDD0	800	880	1000	mA
IDD1	1040	1120	1240	mA
IDD2P	80	80	80	mA
IDD2F	480	480	480	mA
IDD3P	480	480	720	mA
IDD3N	720	720	960	mA
IDD4R	1040	1160	1280	mA
IDD4W	1080	1240	1440	mA
IDD5	3120	3280	3520	mA
IDD6	80	80	80	mA
IDD7	2640	2920	3120	mA

IDD CHARACTERISTICS- SINGLE RANK 1Gb, Non-ECC

Symbol	VR4CU286428F(*)H PC2100 CL2.5	VR4CU286428F(*)K PC2700 CL2.5	VR4CU286428F(*)P PC3200 CL3	Unit
IDD0	800	920	960	mA
IDD1	960	1080	1120	mA
IDD2P	120	120	120	mA
IDD2F	240	280	280	mA
IDD3P	240	240	240	mA
IDD3N	520	560	560	mA
IDD4R	1040	1200	1360	mA
IDD4W	1040	1200	1360	mA
IDD5	1840	1920	2000	mA
IDD6	120	120	120	mA
IDD7	2400	2640	2880	mA

IDD CHARACTERISTICS- DUAL RANK 1Gb, Non-ECC

Symbol	VR4CU566428F(*)H PC2100 CL2.5	VR4CU566428F(*)K PC2700 CL2.5	VR4CU566428F(*)P PC3200 CL3	Unit
IDD0	920	1040	1080	mA
IDD1	1080	1200	1240	mA
IDD2P	240	240	240	mA
IDD2F	480	560	560	mA
IDD3P	480	480	480	mA
IDD3N	1040	1120	1120	mA
IDD4R	1160	1320	1480	mA
IDD4W	1160	1320	1480	mA
IDD5	3680	3840	4000	mA
IDD6	240	240	240	mA
IDD7	2520	2760	3000	mA

IDD CHARACTERISTICS- SINGLE RANK 128Mb, ECC

Symbol	VR4CU167228C(*)H PC2100 CL2.5	VR4CU167228C(*)K PC2700 CL2.5	VR4CU167228C(*)P PC3200 CL3 (3-3-3)	Unit
IDD0	675	765	900	mA
IDD1	900	990	1125	mA
IDD2P	27	27	27	mA
IDD2F	180	198	270	mA
IDD3P	225	225	225	mA
IDD3N	315	360	360	mA
IDD4R	1080	1260	1440	mA
IDD4W	1125	1305	1530	mA
IDD5	1395	1485	1620	mA
IDD6	18	18	18	mA
IDD7	2250	2700	3150	mA

IDD CHARACTERISTICS- DUAL RANK 128Mb, ECC

Symbol	VR4CU327228C(*)H PC2100 CL2.5	VR4CU327228C(*)K PC2700 CL2.5	VR4CU327228C(*)P PC3200 CL3 (3-3-3)	Unit
IDD0	702	792	927	mA
IDD1	927	1017	1152	mA
IDD2P	54	54	54	mA
IDD2F	360	396	540	mA
IDD3P	450	450	450	mA
IDD3N	630	720	720	mA
IDD4R	1107	1287	1467	mA
IDD4W	1152	1332	1557	mA
IDD5	1422	1512	1647	mA
IDD6	36	36	36	mA
IDD7	2277	2727	3177	mA

IDD CHARACTERISTICS- SINGLE RANK 256Mb, ECC

Symbol	VR4CU327228D(*)H PC2100 CL2.5	VR4CU327228D(*)K PC2700 CL2.5	VR4CU327228D(*)P PC3200 CL3 (3-3-3)	Unit
IDD0	720	810	945	mA
IDD1	945	1035	1170	mA
IDD2P	27	27	36	mA
IDD2F	225	270	270	mA
IDD3P	270	315	450	mA
IDD3N	405	495	585	mA
IDD4R	1215	1350	1530	mA
IDD4W	1215	1350	1530	mA
IDD5	1440	1530	1620	mA
IDD6	27	27	27	mA
IDD7	2250	2520	2700	mA

IDD CHARACTERISTICS- DUAL RANK 256Mb, ECC

Symbol	VR4CU647228D(*)H PC2100 CL2.5	VR4CU647228D(*)K PC2700 CL2.5	VR4CU647228D(*)P PC3200 CL3 (3-3-3)	Unit
IDD0	747	837	981	mA
IDD1	972	1062	1206	mA
IDD2P	54	54	72	mA
IDD2F	450	540	540	mA
IDD3P	540	630	900	mA
IDD3N	810	990	1080	mA
IDD4R	1242	1377	1566	mA
IDD4W	1242	1377	1566	mA
IDD5	2880	3060	3240	mA
IDD6	54	54	54	mA
IDD7	2277	2547	2736	mA

IDD CHARACTERISTICS- SINGLE RANK 512Mb, ECC

Symbol	VR4CU647228E(*)H PC2100 CL2.5	VR4CU647228E(*)K PC2700 CL2.5	VR4CU647228E(*)P PC3200 CL3 (3-3-3)	Unit
IDD0	855	945	1080	mA
IDD1	1125	1215	1350	mA
IDD2P	45	45	45	mA
IDD2F	270	270	270	mA
IDD3P	270	270	405	mA
IDD3N	405	405	540	mA
IDD4R	1125	1260	1395	mA
IDD4W	1170	1350	1575	mA
IDD5	1755	1845	1980	mA
IDD6	45	45	45	mA
IDD7	2925	3240	3465	mA

IDD CHARACTERISTICS- DUAL RANK 512Mb, ECC

Symbol	VR4CU287228E(*)H PC2100 CL2.5	VR4CU287228E(*)K PC2700 CL2.5	VR4CU287228E(*)P PC3200 CL3 (3-3-3)	Unit
IDD0	900	990	1125	mA
IDD1	1170	1260	1395	mA
IDD2P	90	90	90	mA
IDD2F	540	540	540	mA
IDD3P	540	540	810	mA
IDD3N	810	810	1080	mA
IDD4R	1170	1305	1440	mA
IDD4W	1215	1395	1620	mA
IDD5	3510	3690	3960	mA
IDD6	90	90	90	mA
IDD7	2970	3285	3510	mA

IDD CHARACTERISTICS- SINGLE RANK 1Gb, ECC

Symbol	VR4CU287228F(*)G PC2100 CL2	VR4CU287228F(*)H PC2100 CL2.5	VR4CU287228F(*)K PC2700 CL2.5	VR4CU287228F(*)P PC3200 CL3	Unit
IDD0	900	900	1035	1080	mA
IDD1	1080	1080	1215	1260	mA
IDD2P	135	135	135	135	mA
IDD2F	270	270	315	315	mA
IDD3P	270	270	270	270	mA
IDD3N	585	585	630	630	mA
IDD4R	1170	1170	1350	1530	mA
IDD4W	1170	1170	1350	1530	mA
IDD5	2070	2070	2160	2250	mA
IDD6	135	135	135	135	mA
IDD7	2700	2700	2970	3240	mA

IDD CHARACTERISTICS- DUAL RANK 1Gb, ECC

Symbol	VR4CU567228F(*)G PC2100 CL2	VR4CU567228F(*)H PC2100 CL2.5	VR4CU567228F(*)K PC2700 CL2.5	VR4CU567228F(*)P PC3200 CL3	Unit
IDD0	1035	1035	1170	1215	mA
IDD1	1215	1215	1350	1395	mA
IDD2P	270	270	270	270	mA
IDD2F	540	540	630	630	mA
IDD3P	540	540	540	540	mA
IDD3N	1170	1170	1260	1260	mA
IDD4R	1305	1305	1485	1665	mA
IDD4W	1305	1305	1485	1665	mA
IDD5	4140	4140	4320	4500	mA
IDD6	270	270	270	270	mA
IDD7	2835	2835	3105	3375	mA

AC OPERATING TEST CONDITIONS (VDD=2.5V, VDDQ=2.5V, TA=0 to 70°C)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH	VREF + 0.31	-	V	1
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL	-	VREF – 0.31	V	2
Input Differential Voltage, CLK and #CLK inputs	VID	0.7	VDDQ + 0.6	V	3
Input Crossing Point Voltage, CLK and #CLK inputs	VIX	0.5*VDDQ - 0.2	0.5*VDDQ + 0.2	V	4

Note: 1. VIH(max) = 4.2V. The overshoot voltage duration is ≤ 3 ns at VDD.
2. VIL(min) = -1.5V. The undershoot voltage duration is ≤ 3 ns at GND.
3. VID is the magnitude of the difference between the input levels on CLK and on #CLK.
4. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the DC level of the same.

AC Timing Parameters & Specifications

Symbol	Parameter		PC3200 CL=3.0		PC2700 CL=2.5		PC2100 CL=2.5		Unit
			Min	Max	Min	Max	Min	Max	
tRC	Row cycle time		55		60		65		ns
tRFC	Refresh row cycle time	128 Mb, 256Mb, 512Mb	70		72		75		ns
		1Gbit only	120		120		120		ns
tRAS	Row active time		40	70K	42	70K	45	120K	ns
tRCD	RAS to CAS delay		15		18		20		ns
tRP	Row precharge time		15		18		20		ns
tRRD	Row active to Row active delay		10		12		15		ns
tWR	Write recovery time		15		15		15		ns
tWTR	Last data in to Read command		2		1		1		tCK
tCK	Clock cycle time	CL=2	-	-	-	-	10	12	
		CL=2.5	6	12	6	12	7.5	12	ns
		CL=3.0	5	10	-	-	-	-	
tCH	Clock high level width		0.45	0.55	0.45	0.55	0.45	0.55	tCK
tCL	Clock low level width		0.45	0.55	0.45	0.55	0.45	0.55	tCK
tDQSCK	DQS-out access time from CK/CK		-0.55	+0.55	-0.6	+0.6	-0.75	+0.75	ns
tAC	Output data access time from CK/CK		-0.65	+0.65	-0.7	+0.7	-0.75	+0.75	ns
tDQSQ	Data strobe edge to ouput data edge		-	0.4	-	0.45	-	0.5	ns
tRPRE	Read Preamble		0.9	1.1	0.9	1.1	0.9	1.1	tCK
tRPST	Read Postamble		0.4	0.6	0.4	0.6	0.4	0.6	tCK
tDQSS	CK to valid DQS-in		0.72	1.25	0.75	1.25	0.75	1.25	tCK
tWPRES	DQS-in setup time		0		0		0		ns
tWPRE	DQS-in hold time		0.25		0.25		0.25		tCK
tDSS	DQS falling edge to CK rising-setup time		0.2		0.2		0.2		tCK
tDSH	DQS falling edge from CK rising-hold time		0.2		0.2		0.2		tCK
tDQSH	DQS-in high level width		0.35		0.35		0.35		tCK
tDQSL	DQS-in low level width		0.35		0.35		0.35		tCK
tIS	Address and Control Input setup time(fast)		0.6		0.75		0.9		ns
tIH	Address and Control Input hold time(fast)		0.6		0.75		0.9		ns
tIS	Address and Control Input setup		0.7		0.8		1.0		ns
tIH	Address and Control Input hold time(slow)		0.7		0.8		1.0		ns
tHZ	Data-out high impedence time from CK/CK		-	+0.65	-	+0.7	-	+0.75	ns
tLZ	Data-out low impedence time from CK/CK		-0.65	+0.65	-0.7	+0.7	-0.75	+0.75	ns
tMRD	Mode register set cycle time		10		12		15		ns
tDS	DQ & DM setup time to DQS		0.4		0.45		0.5		ns
tDH	DQ & DM hold time to DQS		0.4		0.45		0.5		ns
tIPW	Control & Address input pulse width		2.2		2.2		2.2		ns
tDIPW	DQ & DM input pulse width		1.75		1.75		1.75		ns
tXSNR	Exit self refresh to non-Read command		75		75		75		ns
tXSRD	Exit self refresh to read command		200		200		200		tCK
tREFI	Refresh interval time			7.8		7.8		7.8	µs
tQH	Output DQS valid window		tHP-tQHS	-	tHP-tQHS	-	tHP-tQHS	-	ns
tQHS	Data hold skew factor			0.5		0.55		0.75	ns
tWPST	DQS write postamble time		0.4	0.6	0.4	0.6	0.4	0.6	tCK

REVISION HISTORY

Revision	Release Date	Description of Change	Checked By (Full Name)
A	November 25, 2006	Initial Release of DDR1 UDIMM family spec: - Consolidated all DDR1 UDIMM specs - Removed PC1600 data - Corrected block diagram and updated mech dwg - Checked and updated values, added 1Gbit	Ken Ishiguro Brian Ouellette
A1	March 2, 2007	Add VR4CU647228ETK01 to configuration table, correct VR4CU647228E(*)K height to 1.25”	Brian Ouellette
A2	February 2, 2009	Change header and footer to Viking Modular Solutions	Brian Ouellette
A3	October 27, 2009	Correct VR4CU647228D(*)P height to 1.25”	Brian Ouellette

STATEMENT OF COMPLIANCE

Viking Modular Solutions(tm), Sanmina-SCI Corporation ("Viking") shall use commercially reasonable efforts to provide components, parts, materials, products and processes to Customer that do not contain: (i) lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) above 0.1% by weight in homogeneous material or (ii) cadmium above 0.01% by weight of homogeneous material, except as provided in any exemption(s) from RoHS requirements (including the most current version of the "Annex" to Directive 2002/95/EC of 27 January, 2003), as codified in the specific laws of the EU member countries. Viking strives to obtain appropriate contractual protections from its suppliers in connection with the RoHS Directives.