Machine Learning Assisted Validation, Off and On-Line Test and Tuning of Advanced Mixed-Signal/RF Circuits and Systems

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Overview

Future real-time mixed-signal/RF/DSP/control systems: *the need for self-awareness*

- Self aware: Dynamically adapt to operating environment and health (failure conditions)

Objective: Minimize power, maximize reliability/error resilience

Machine Learning Assisted Validation of Mixed-Signal Systems

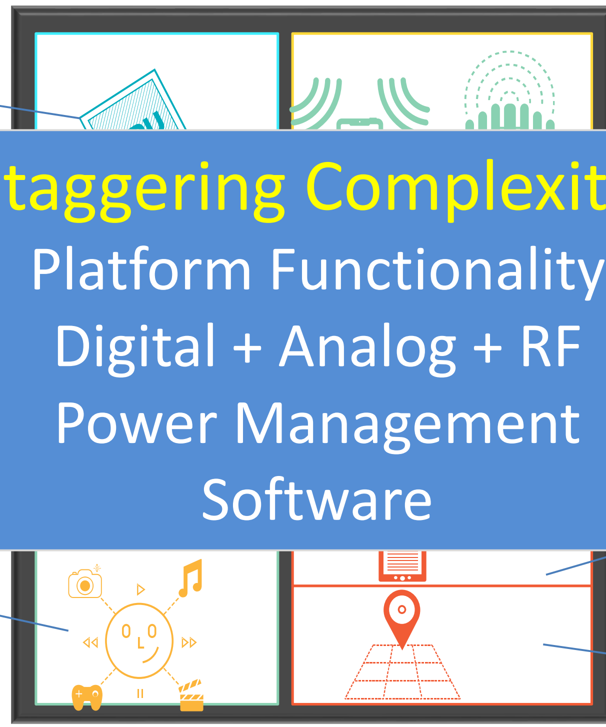
S602A – Qualcomm's automotive SoCs must meet automotive temperature, quality and reliability requirements

Quad Core Krait CPU
up to 1.5 GHz

Adreno GPU
(400MHz)

DSP core

Connectivity: Wi-Fi, BT, PCIe, USB, SATA, SPI



Staggering Complexity!

Platform Functionality

Digital + Analog + RF

Power Management

Software

Multimedia Frameworks:
DTS-HD and Dolby audio
Gesture Support

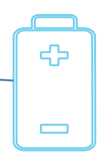
Sensor Core

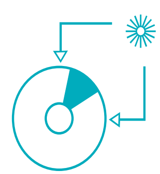
Camera and video engines with compression, decompression and image processing

Multi-display support (Center Stack, Rear Seat, Instrument Cluster): HDMI, LVDS, CSI, DSI…

Global Navigation Satellite Subsystem

Power Management (dynamic, adaptive)





HLOS / Software
Android, Linux, QNX

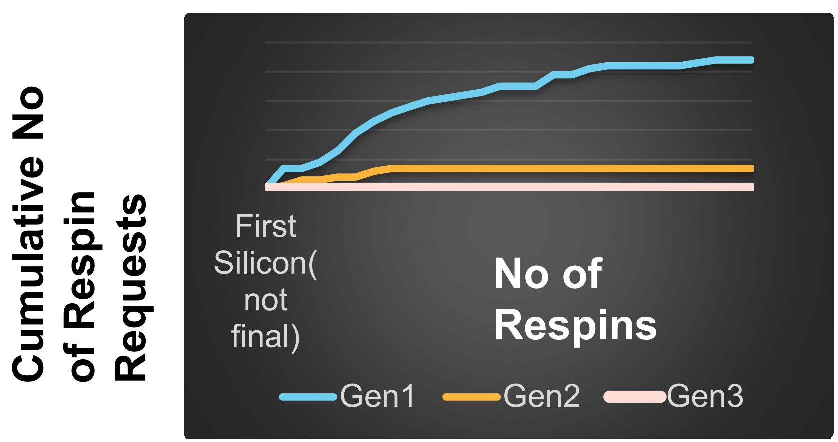
Quality &
Reliability

Bad News: Complexity Makes Design Bugs Inevitable!

Verification complexity is increasing exponentially with design size: Logic bugs, Electrical bugs

- **System-level simulation bottlenecks (billions of cycles at 1000 cycles/second)**
- **Verification bottlenecks**
  - **Manually generated assertions requiring combinatorial search**
  - **Inability to verify physics-based electrical interactions between devices (electrical bugs)**
- **No golden DUT! Do not where, when and how the bug will manifest!**

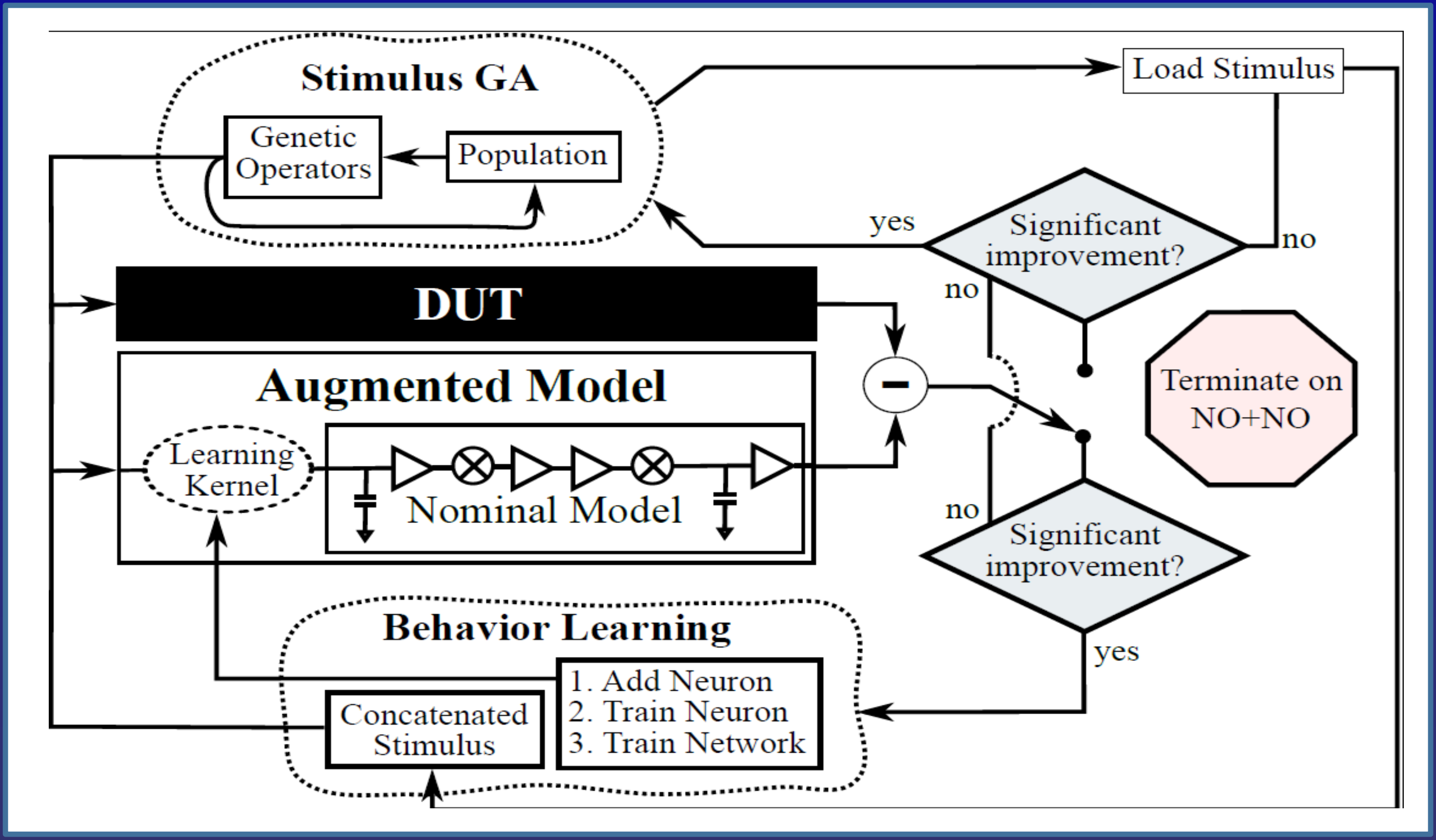
Increasing numbers of bugs are escaping into silicon !

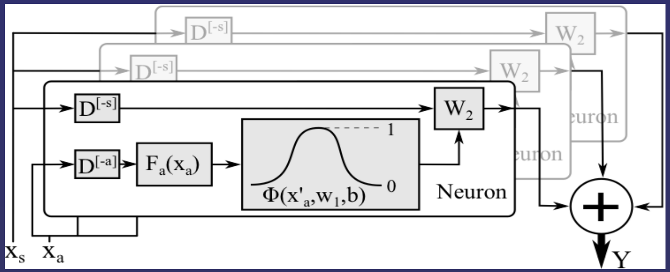


> 7 respins for advanced SoCs

Source: Qualcomm

Approach 1: Adversarial Test Generation Vs. Behavior Learning



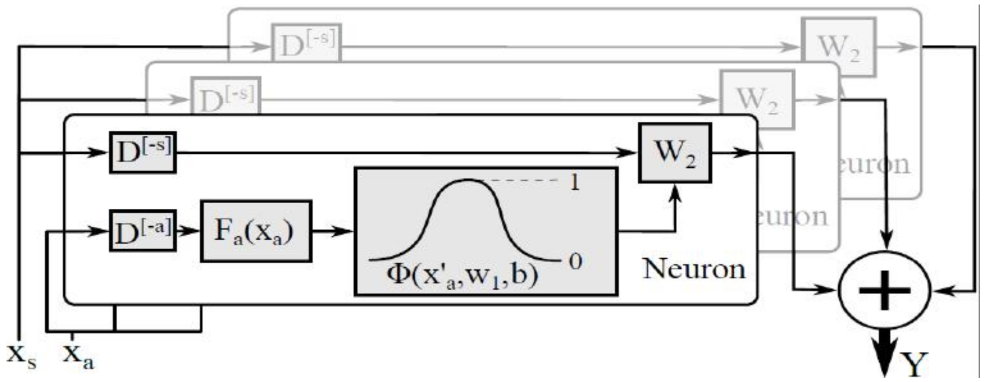


Sparse Weiner learning kernel

Recurrent neural networks can be used

Learning Agent Example: Incorporating memory

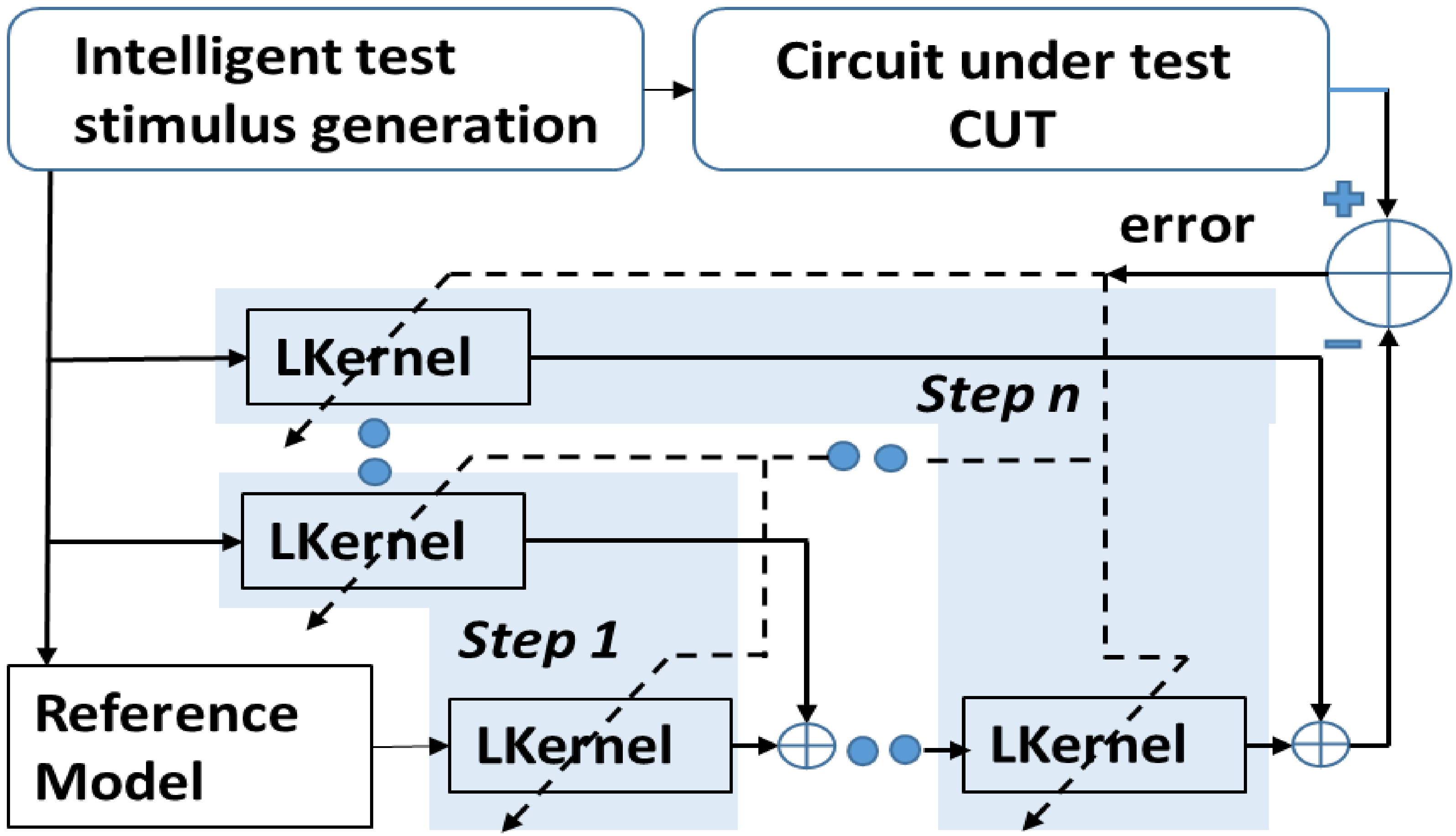
- Combine Radial Basis Neurons into a Weiner filter structure
- Employ nonlinear activation functions chosen on a per-neuron basis
- Highly parametric: sparse number of delay taps



When extracting data from hardware, internal circuit nodes may not be externally observable, so training is based on only observable signals !

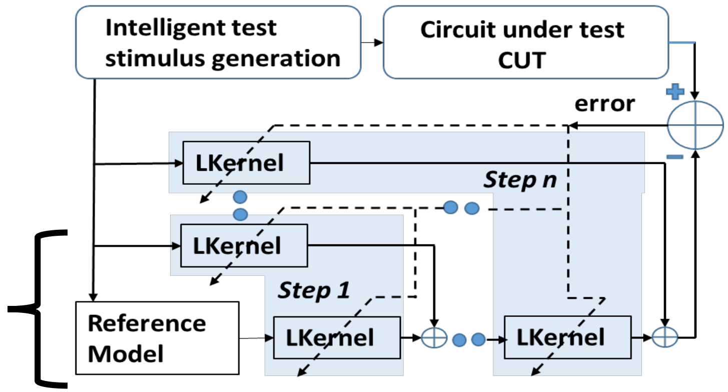
Can use Volterra filters, Recurrent neural networks, etc !

Per Iteration Kernel Update

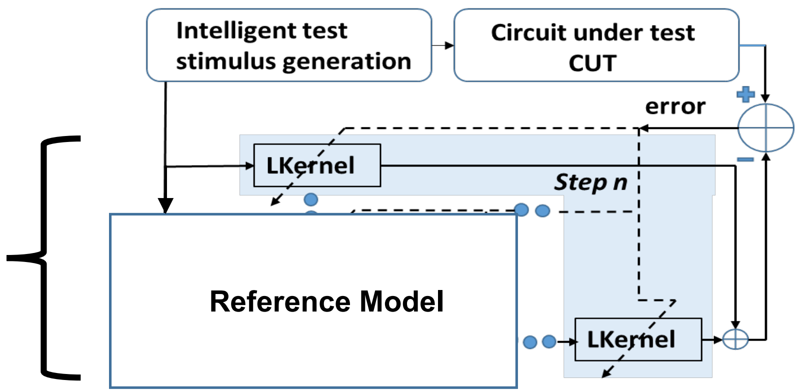


Per Iteration Kernel Update

T1



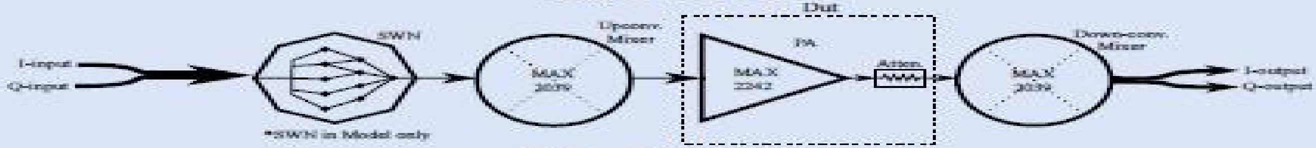
T1 - Tk



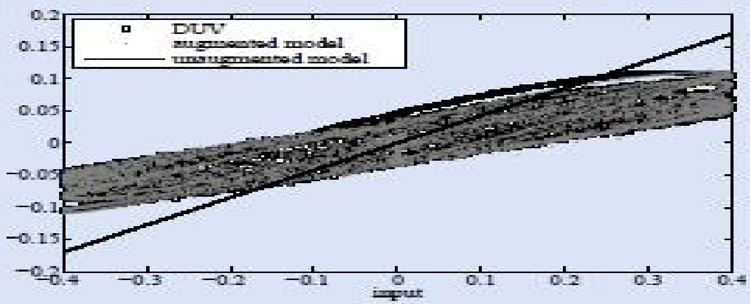
Experimental Validation

Experiment:

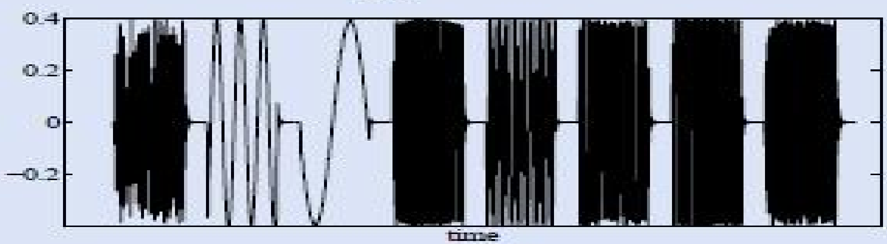
The Model:



The Silicon:
MAX 2242

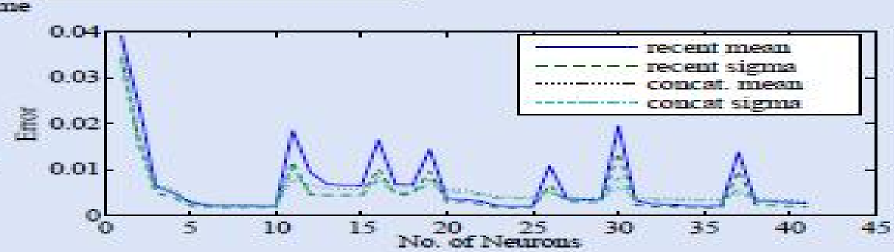


The MAX2242 was found to behave very divergently when compared to our very simplistic, unaugmented, linear model

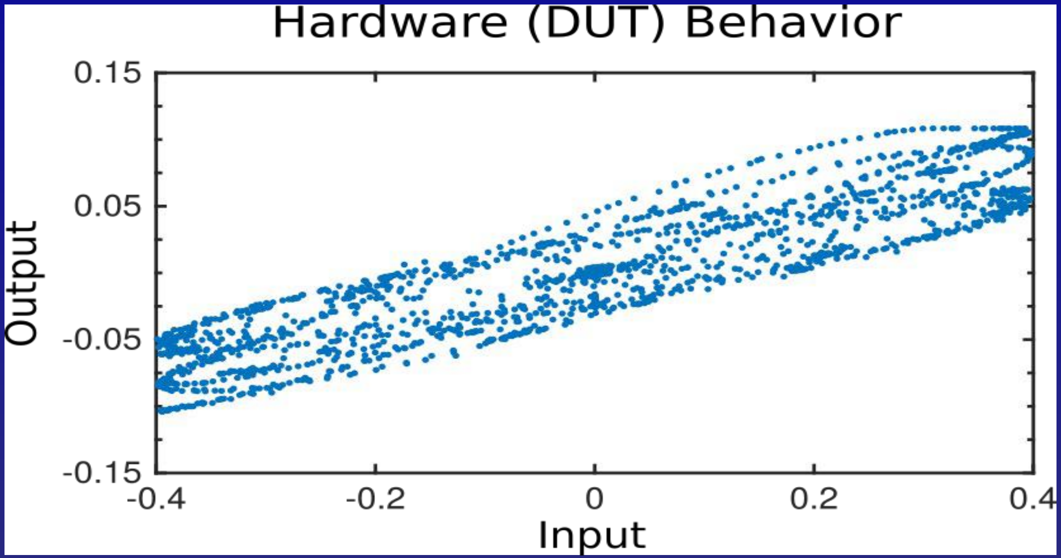


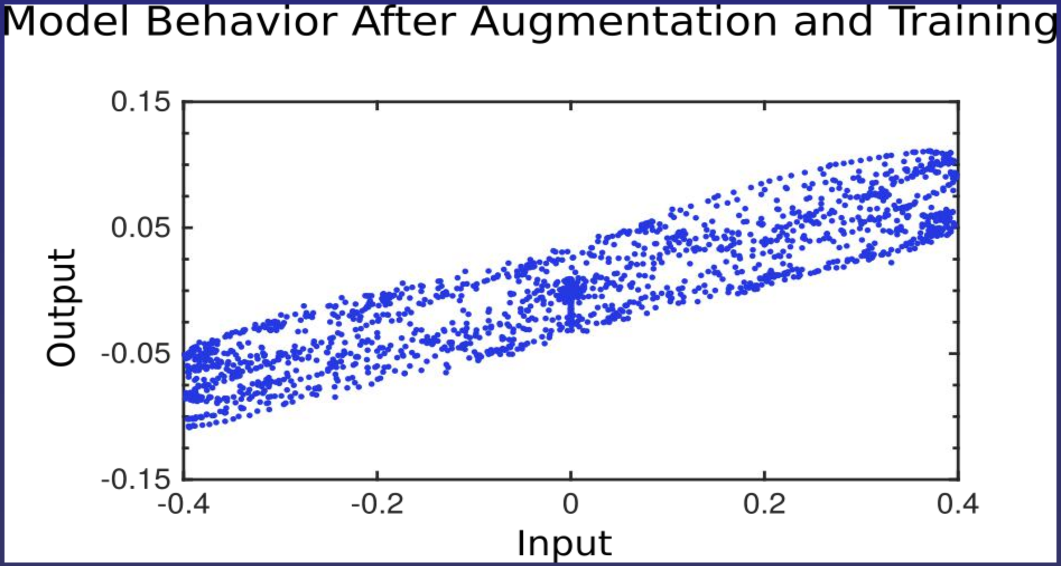
Using a single SWN network of 40 neurons built in 8 stimulus iterations…

the augmented model achieved an order of magnitude improvement in error vs. the MAX 2422



Experimental Results: Maxim MAX2242 RF PA



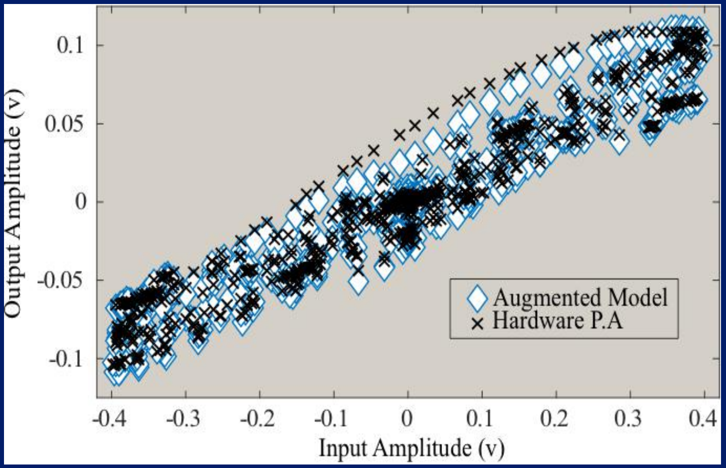


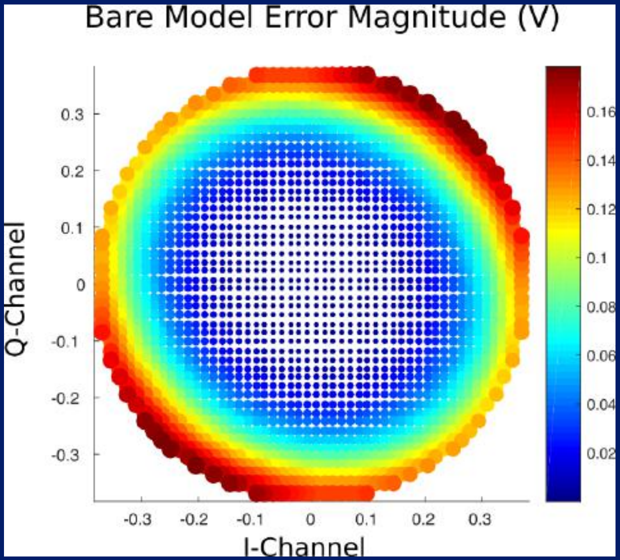
Captures hysteresis and memory effects automatically

Augmenting Behavioral Models

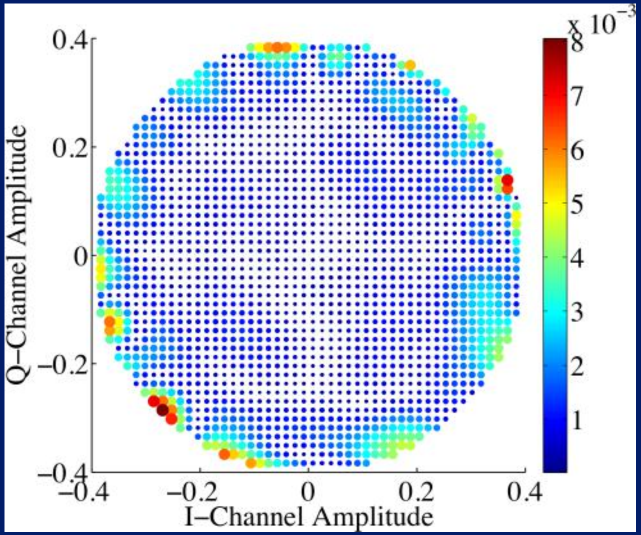
Network was able to learn:

- "Memory" effects
- AM-PM behavior
- AM-AM behavior



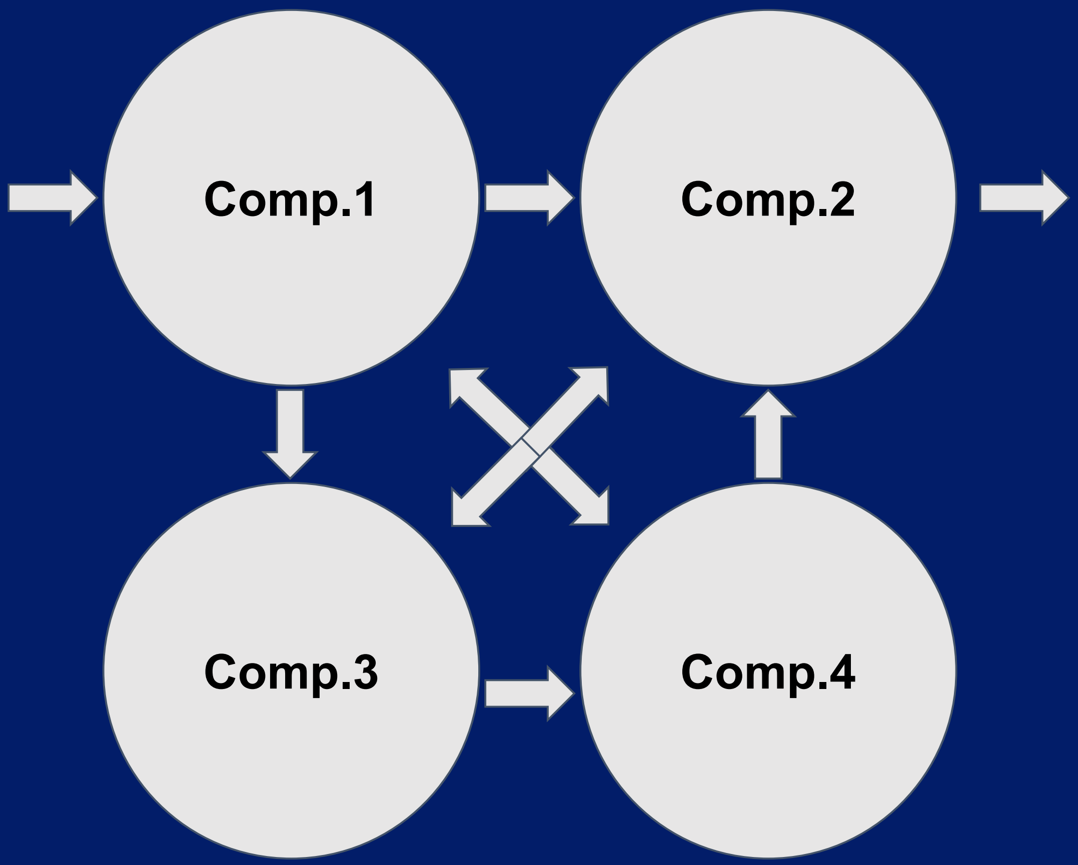


Several orders of magnitude behavior correction!

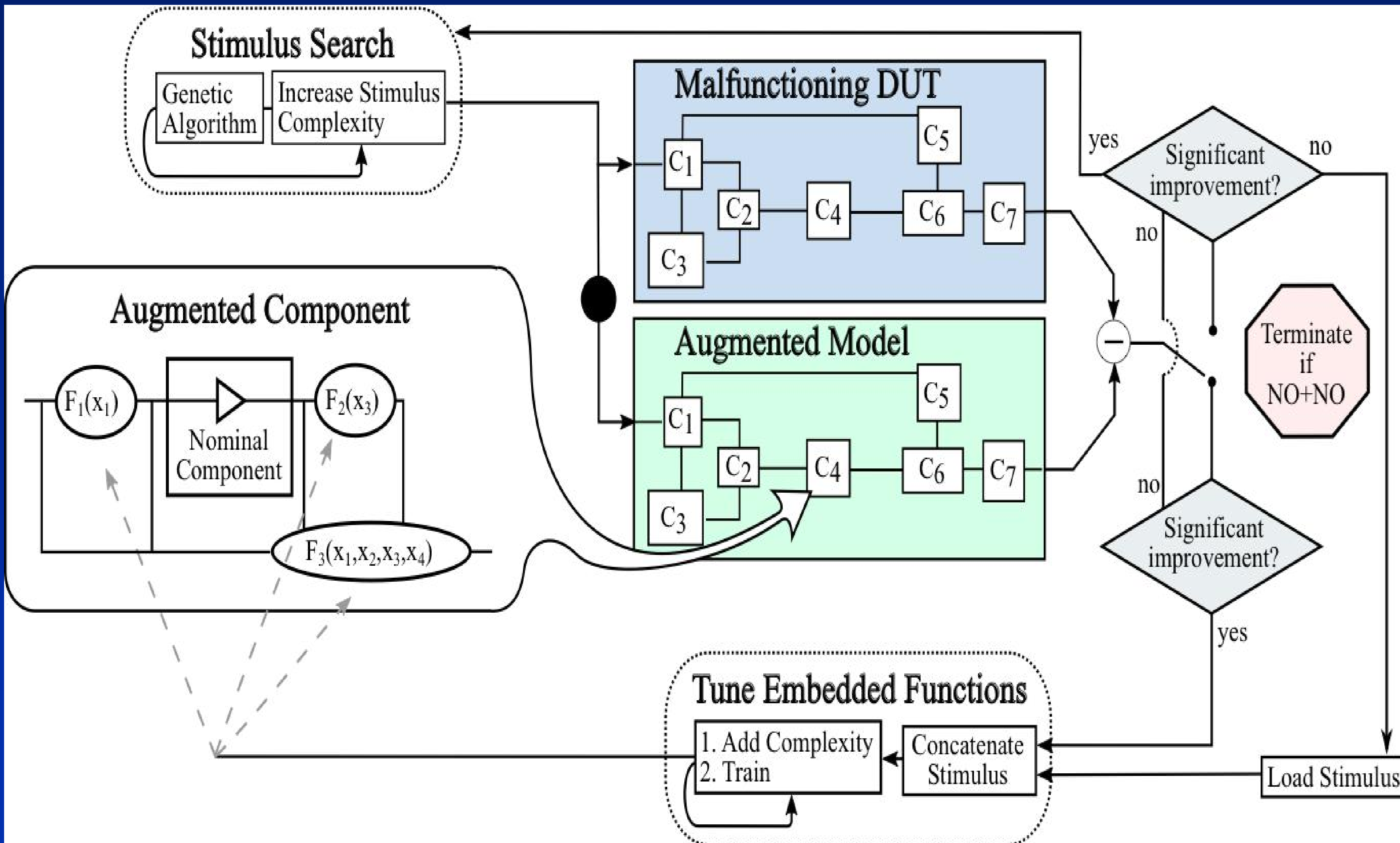


The Diagnosis Problem

- System is failing
- Which comp. is responsible?

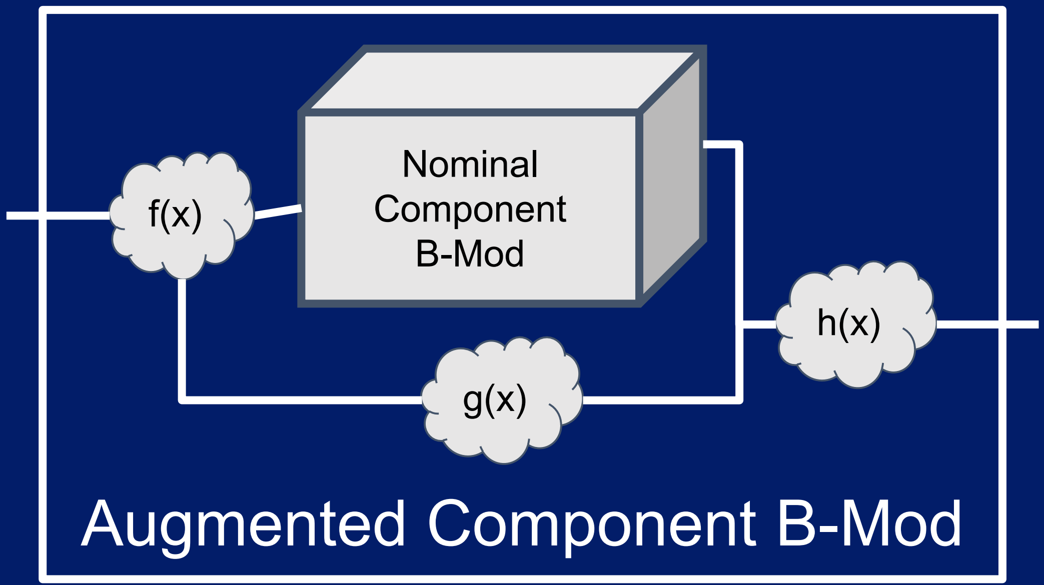


Diagnosis of Static Design Bugs



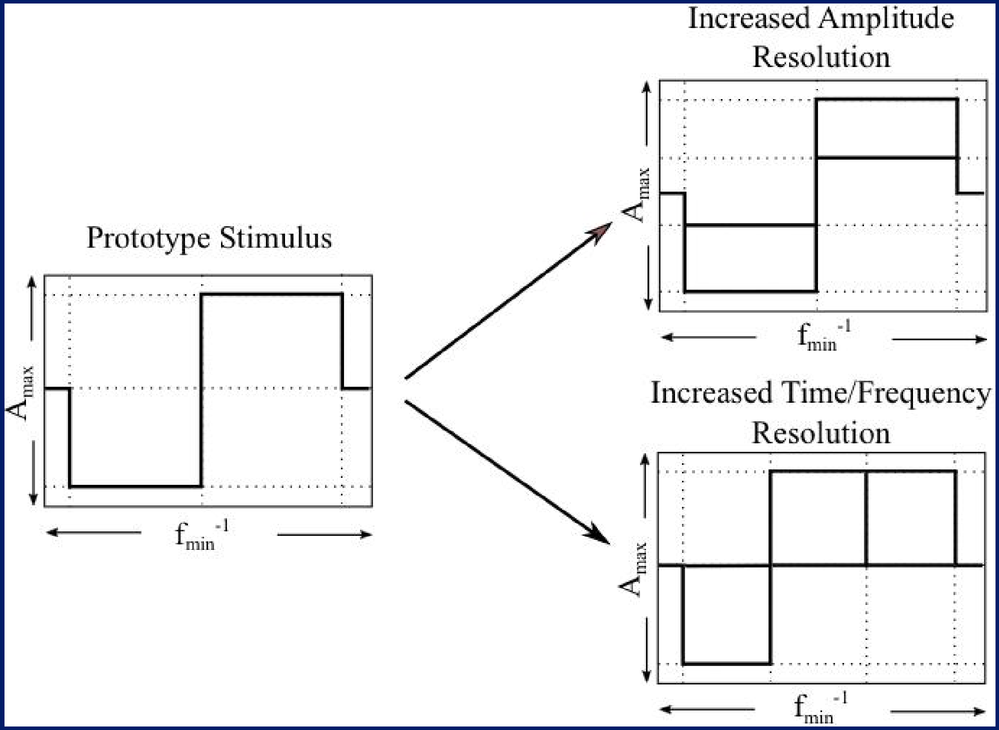
Augmenting Behavioral Models

Systematically impart additional behaviors to arbitrary B-Mods



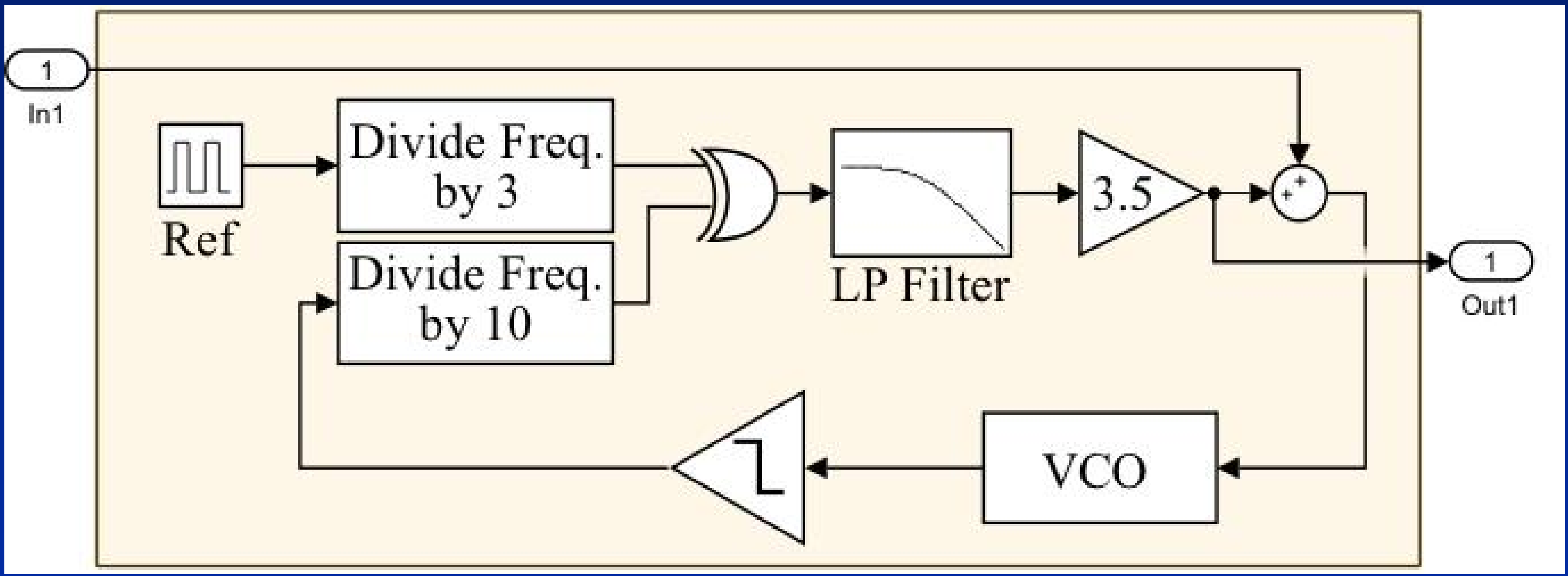
Stimulating Errant Behavior

- Operational space must be searched to discover design/manufacture bugs
- Huge space to search (stoch.)
- Algorithm requires determinism



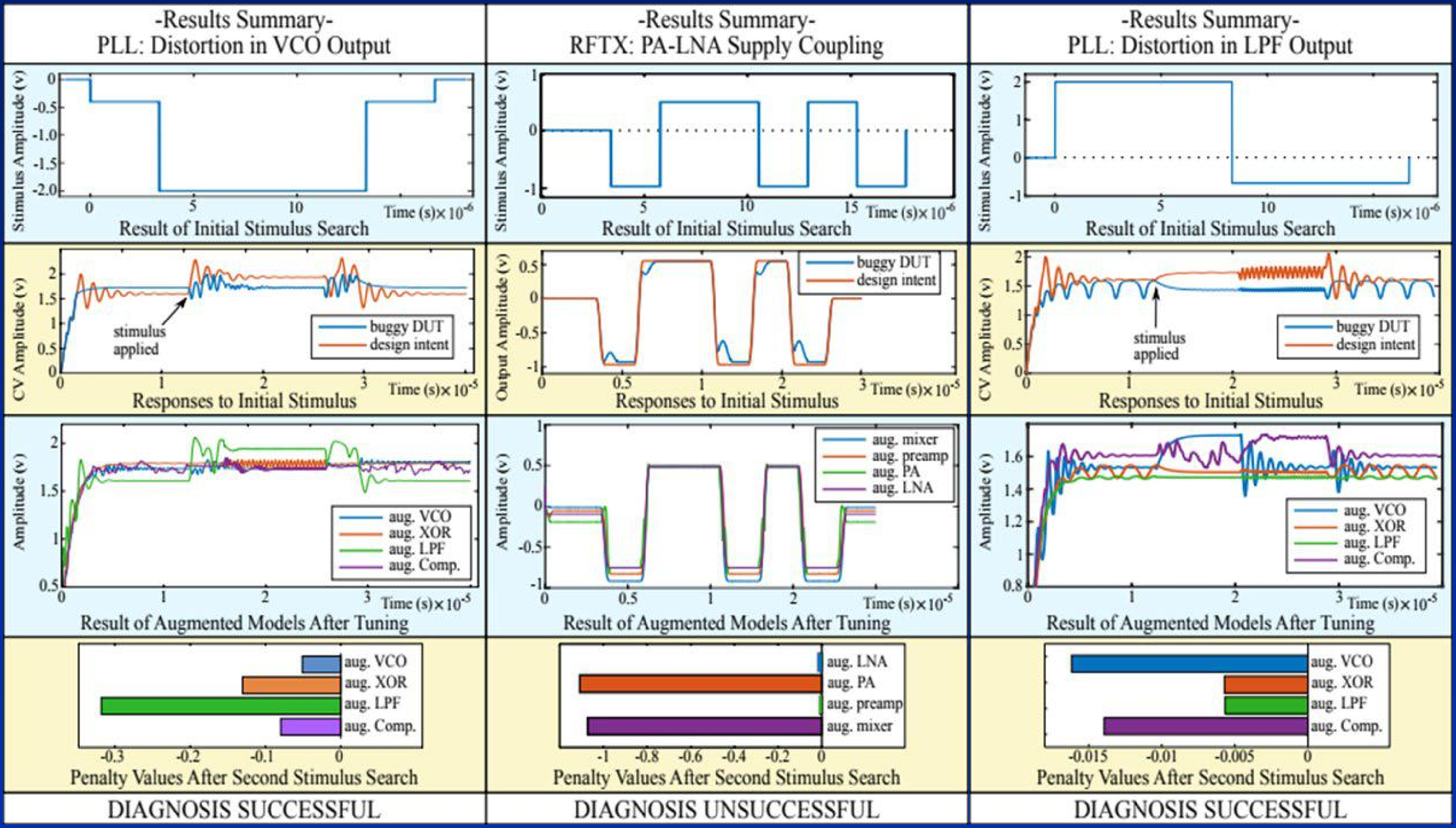
Stimulus complexity (search space) increases deterministically

PLL Experiments



- System stimulated by summing LP signal at VCO input
- System observed immediately prior to summing

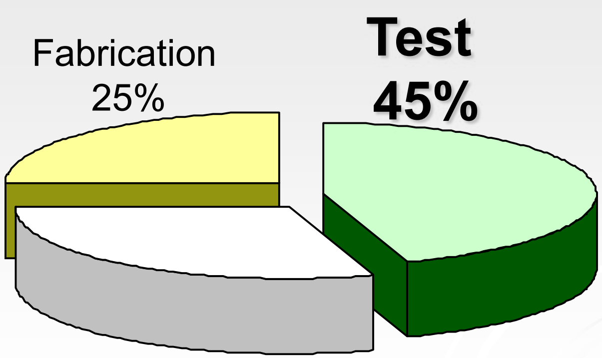
PLL Experiments

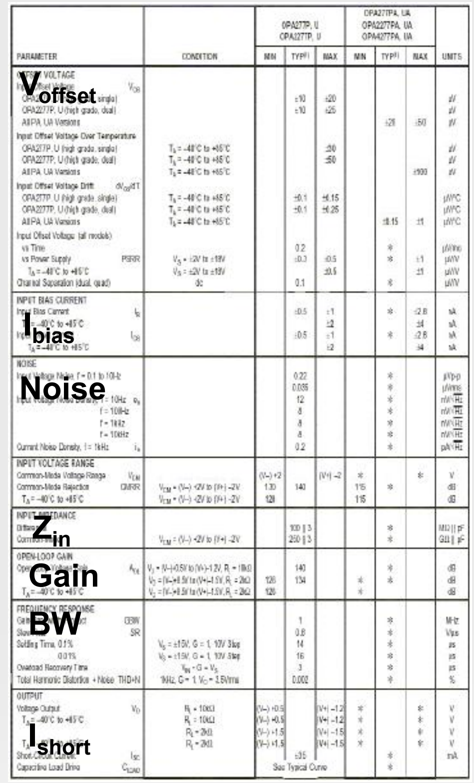


Adaptation Based on Off-Line Test Response Analysis: *Post-Manufacture*

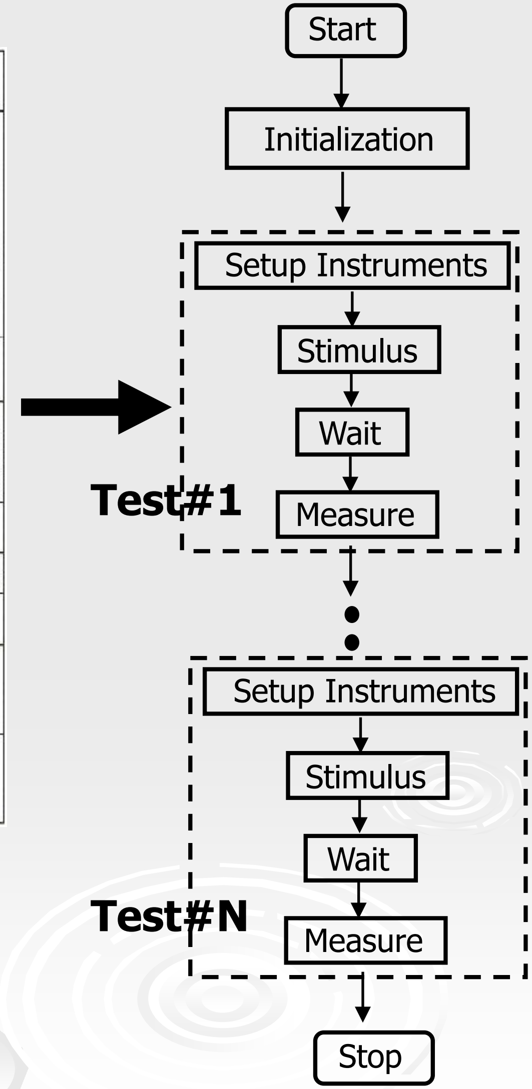
State of the Art: Mixed-Signal SoCs

- Specification Tests
- Each test requires a different setup
  - Total testing time
  - ATE complexity
  - Load board complexity
- Test cost up 30%- 45%*



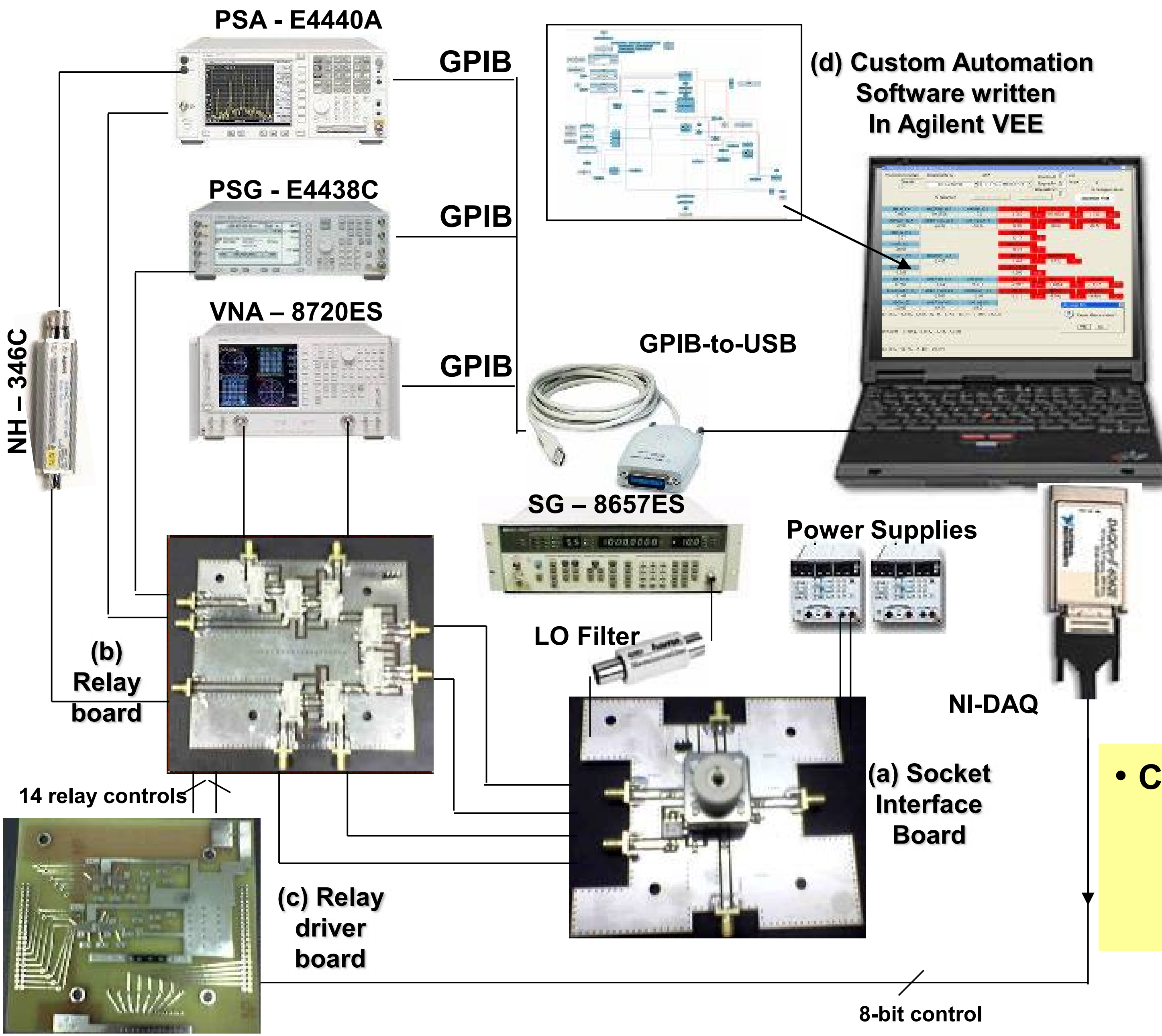


Datasheet



*R. Tummala, Fundamentals of Microsystems Packaging, 2001.

Standard Specification Tests



- 541 ICs
- 13 specifications
- 7 test setups

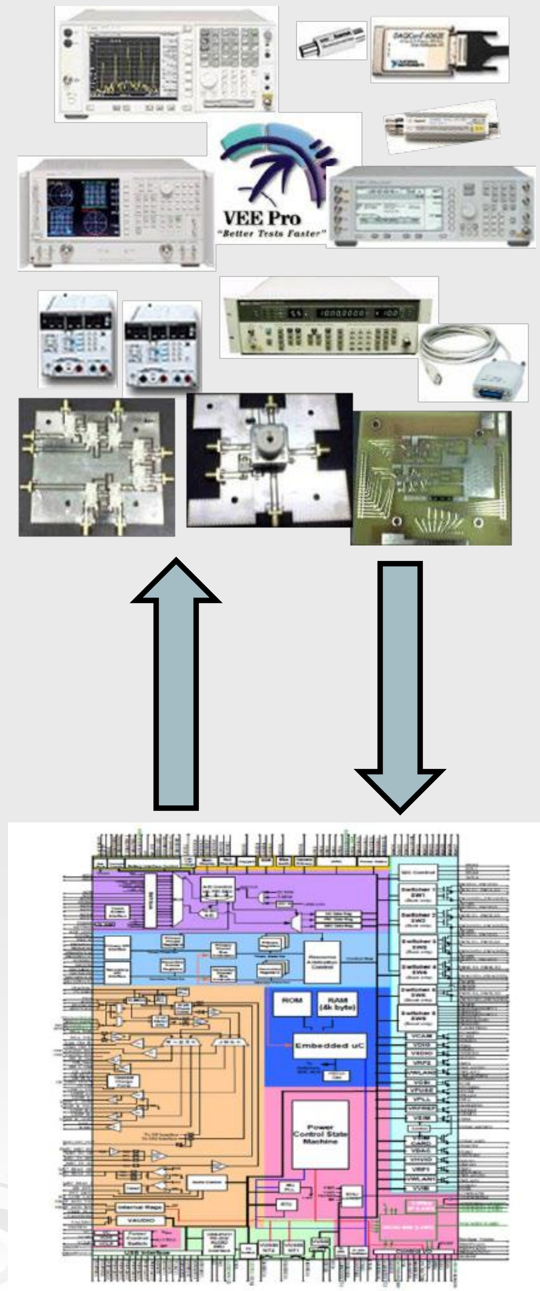
- Custom designed
  - ✓ Socket Board
  - ✓ Relay Board
  - ✓ Relay Driver Board
  - ✓ Control Software

Key Issues:

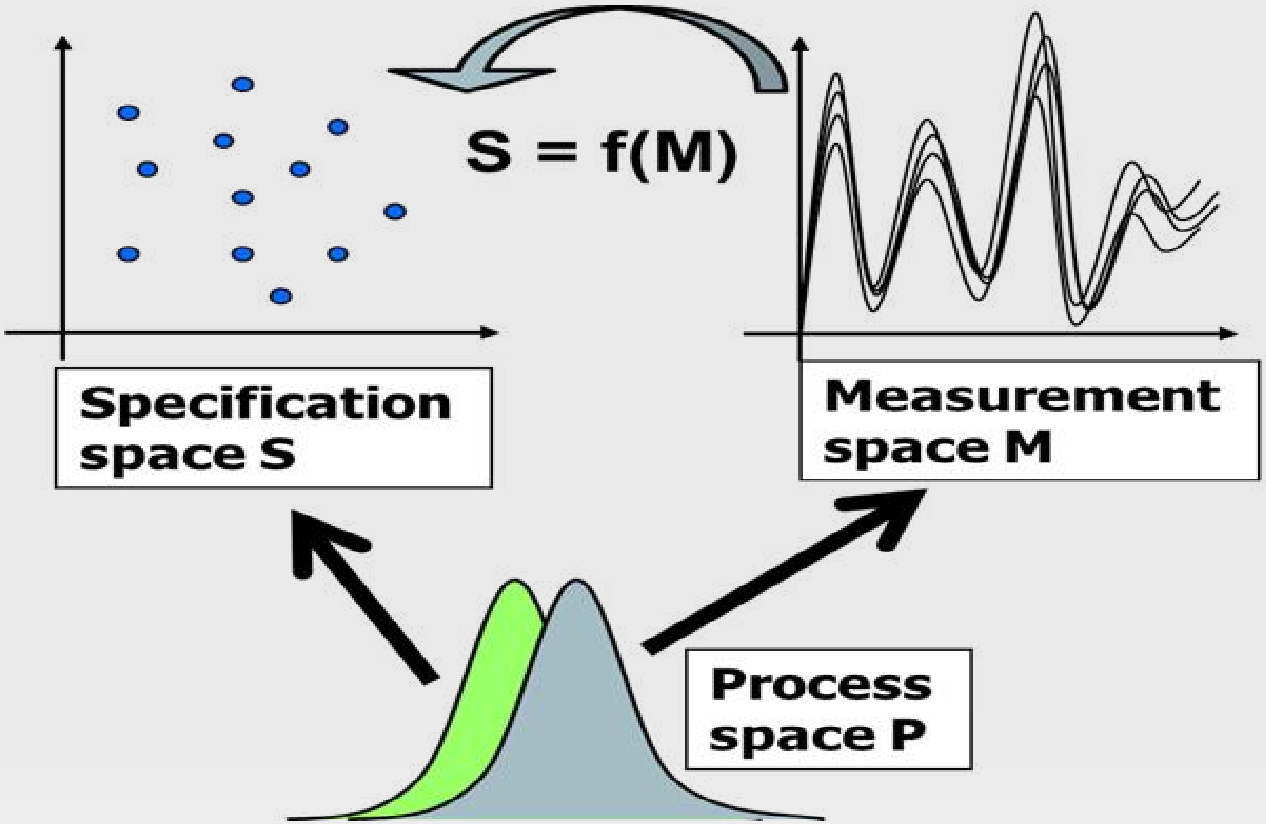
Manufacturing test time: Relay settling time >> actual test time ! Test multiple specs.

Built-in test of complex specifications: Difficult to place test instruments and circuitry on-chip for multiple specifications !

Post-manufacture and field performance tuning: Tune *multiple* specs while minimizing power ? Need to tune devices *without extended test costs*.

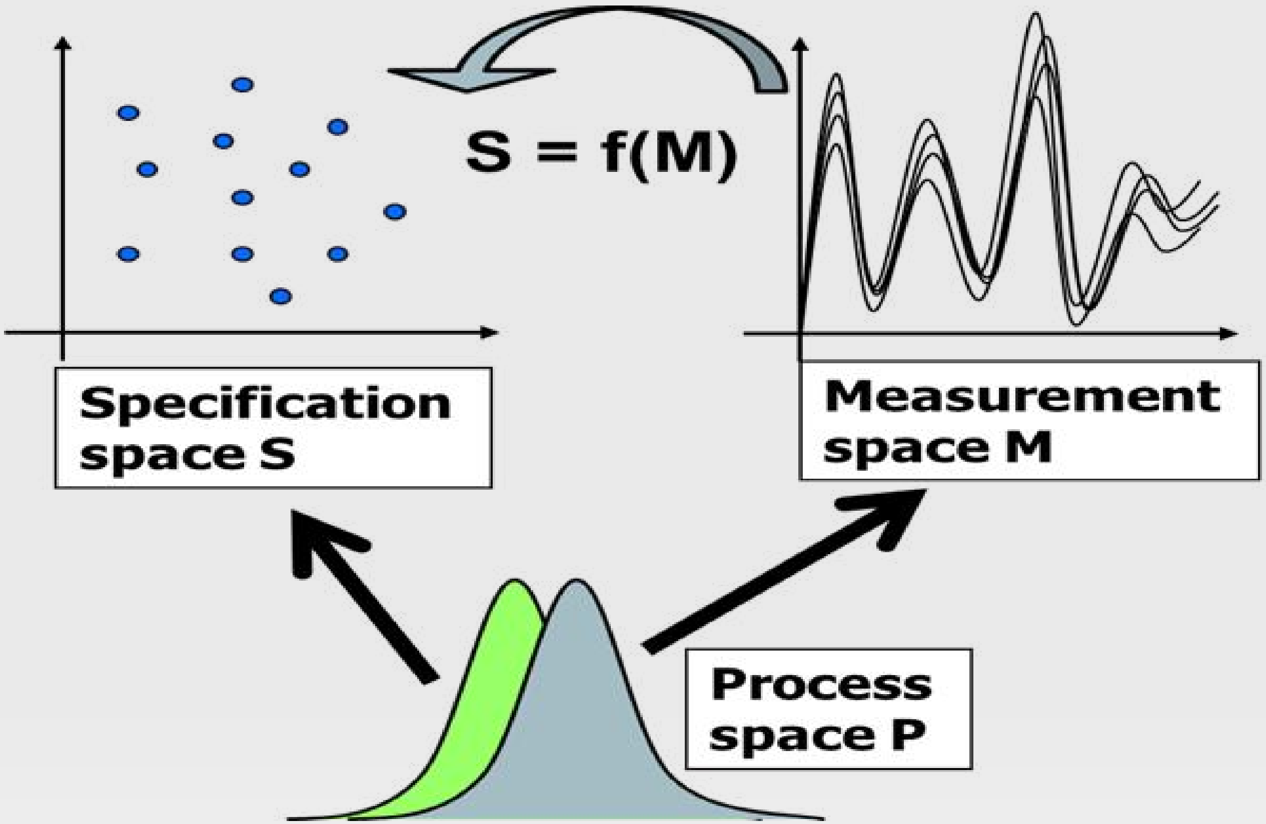


Alternate Tests: Key Principles



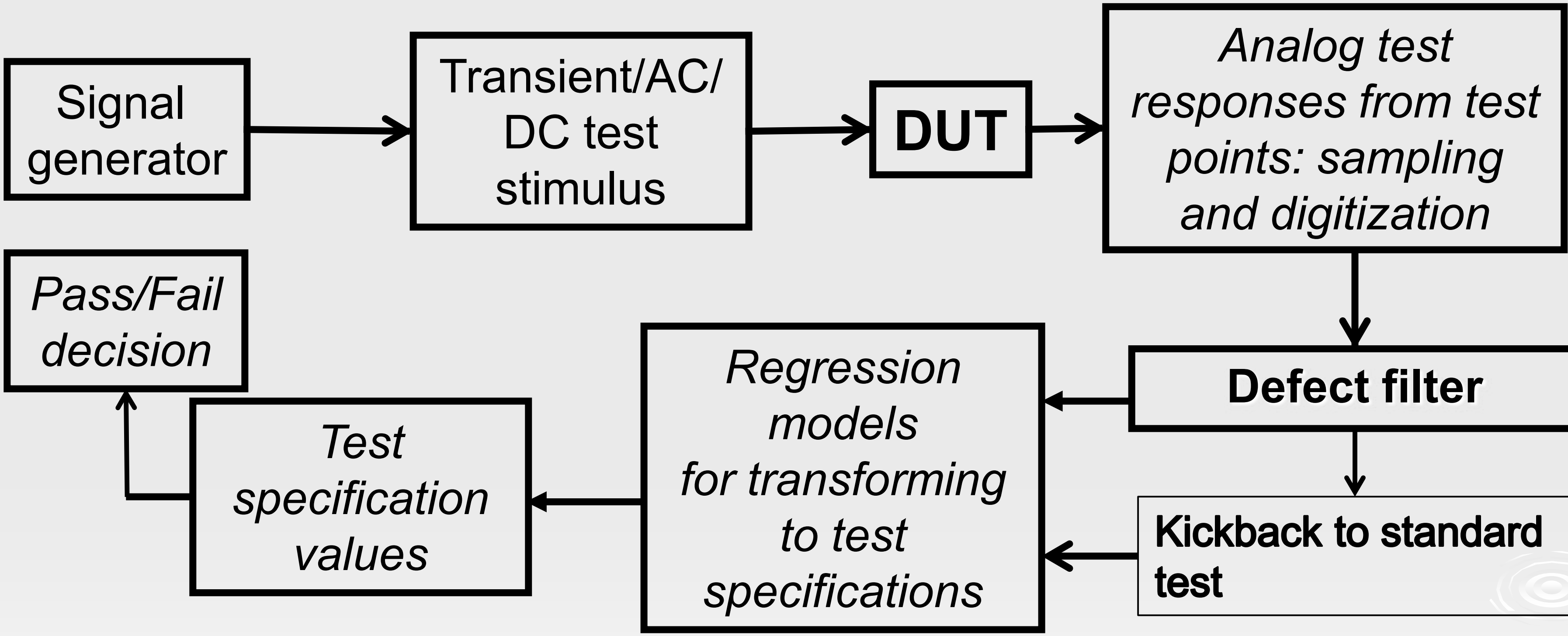
- **The mapping *S=f(M)* is derived using nonlinear regression (multiple adaptive regression splines: MARS)**

Alternate Tests: Key Principles

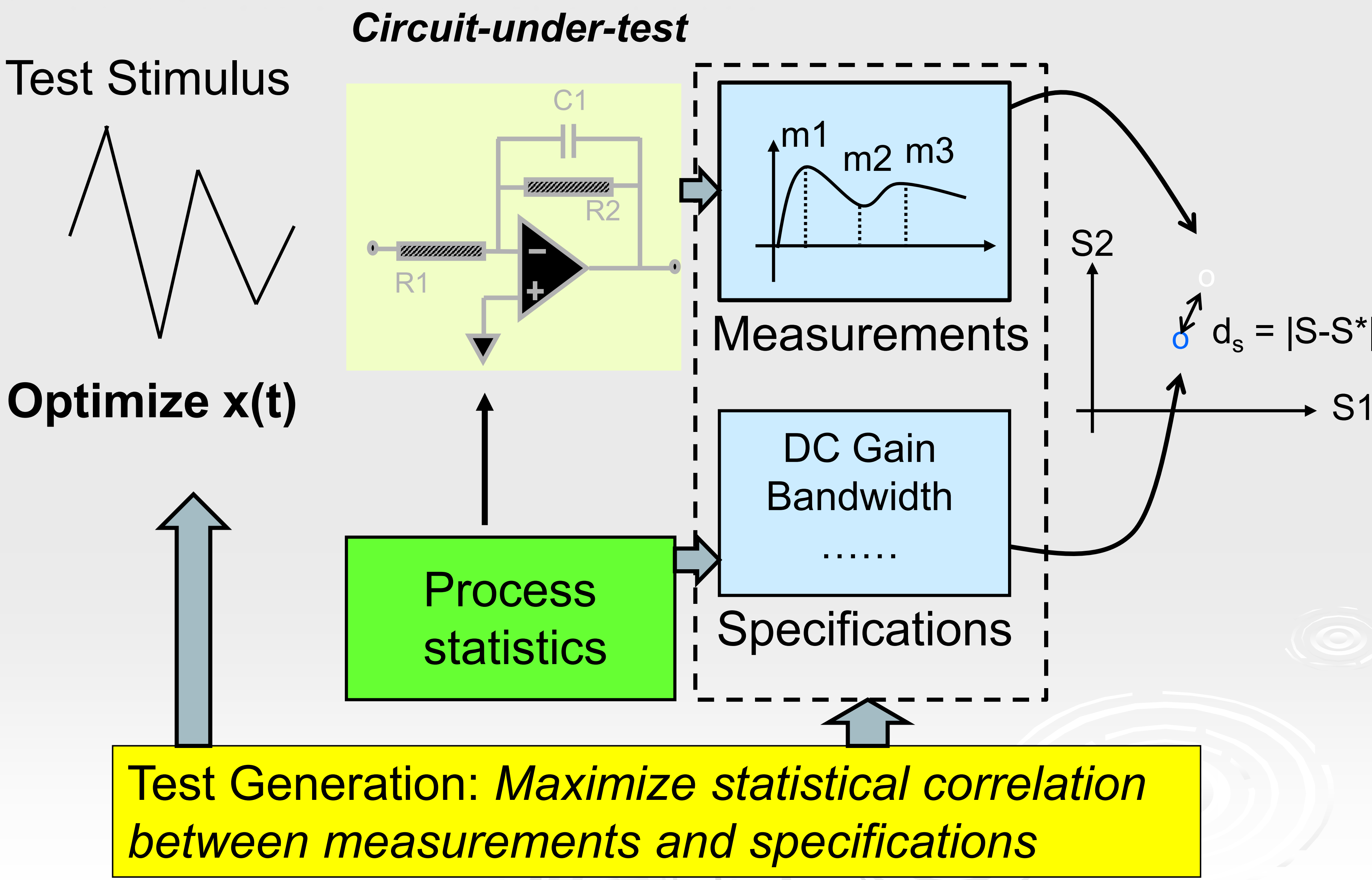


- The mapping *S=f(M)* is derived using nonlinear regression (multiple adaptive regression splines: MARS)

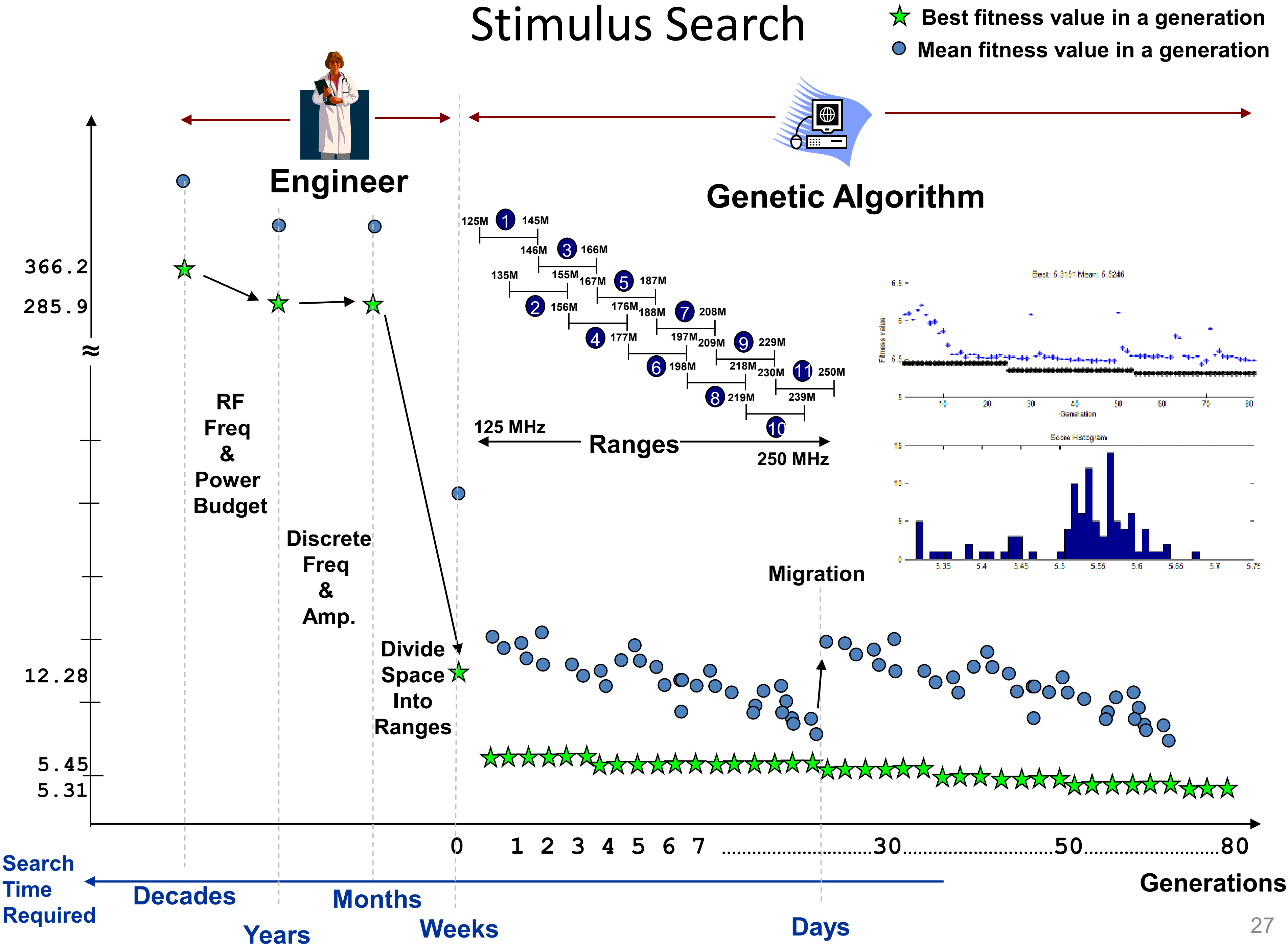
Signature Test Methodology



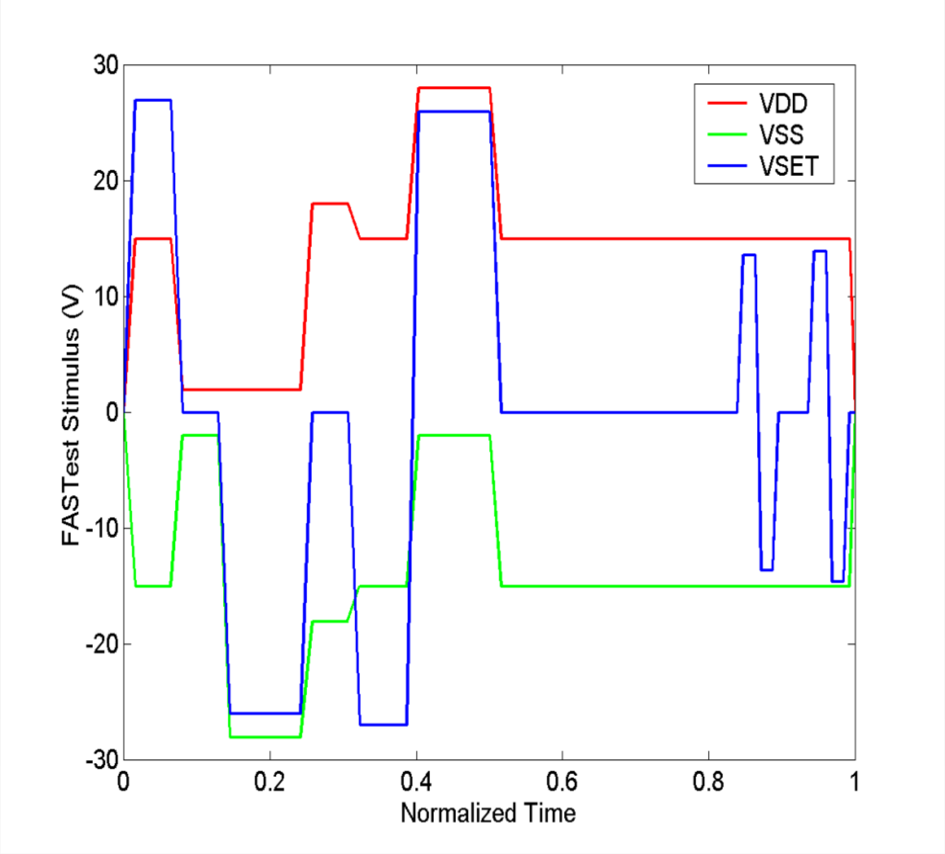
Test Stimulus Generation

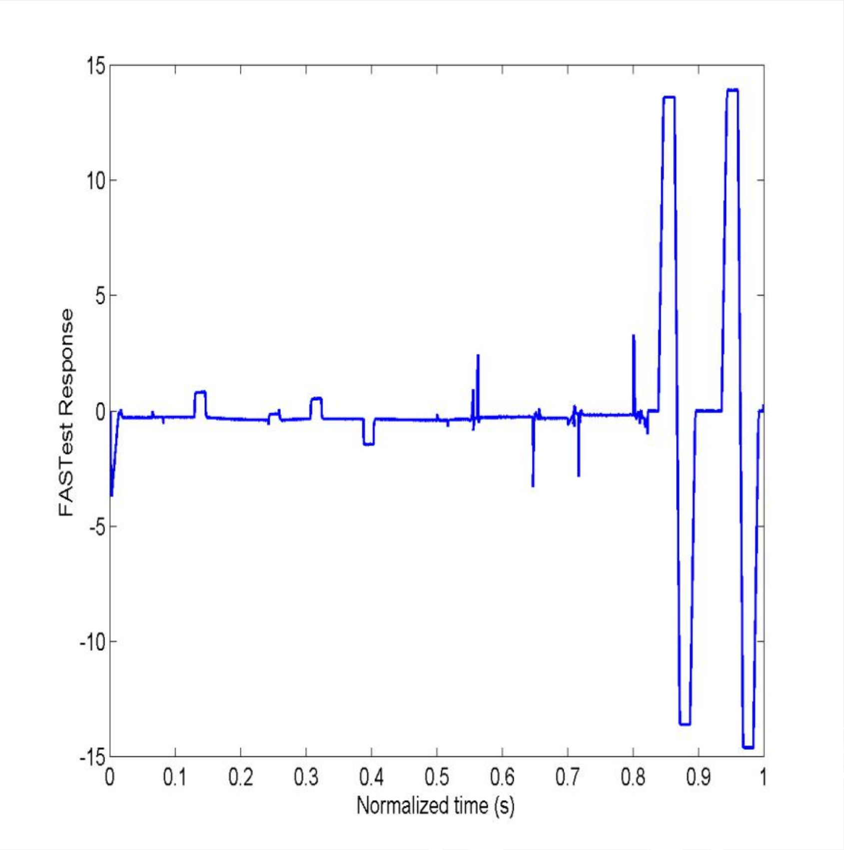


Stimulus Search



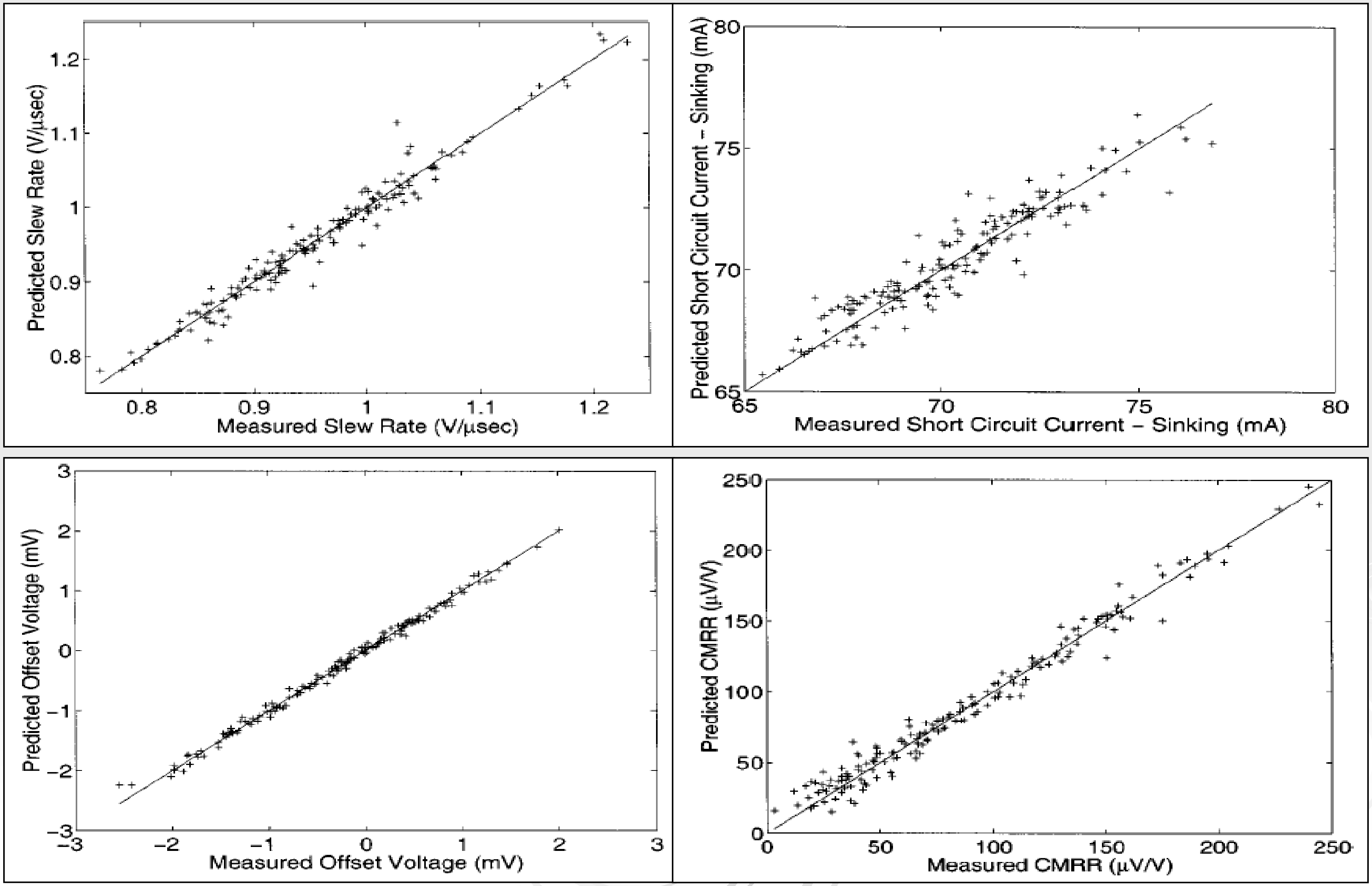
TI Precision Opamp





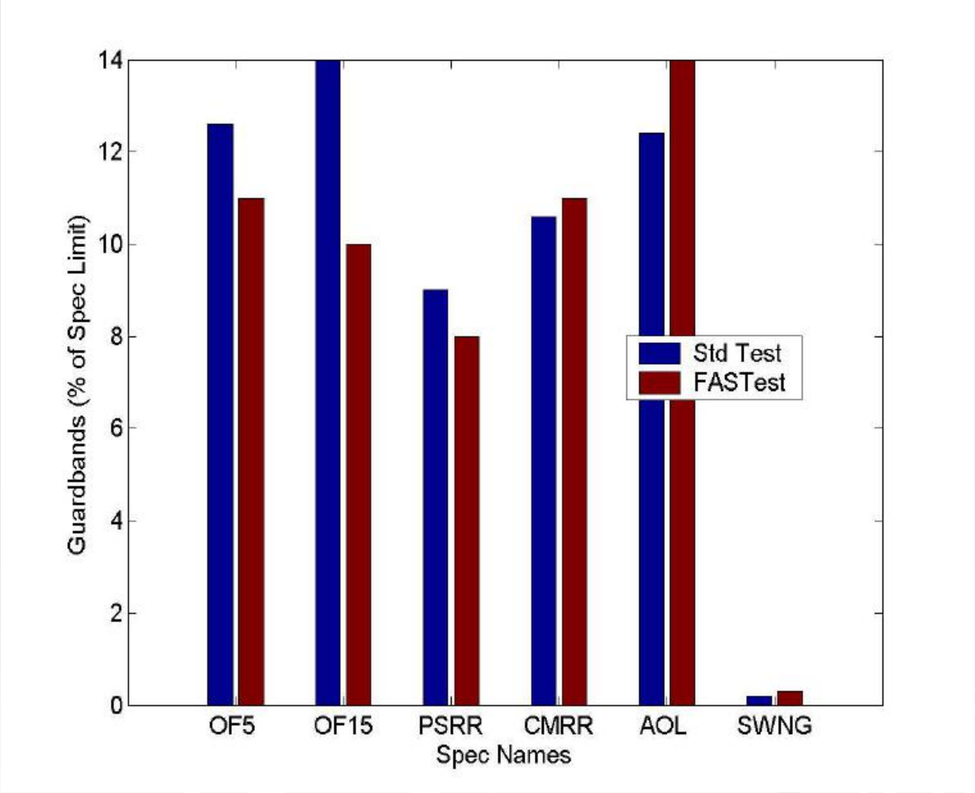
>3X test time reduction

Alternate Test: Performance

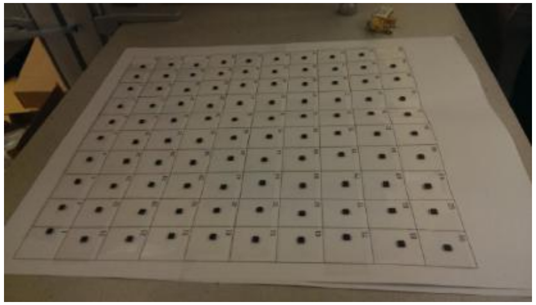


Capability Study (Guardbands)

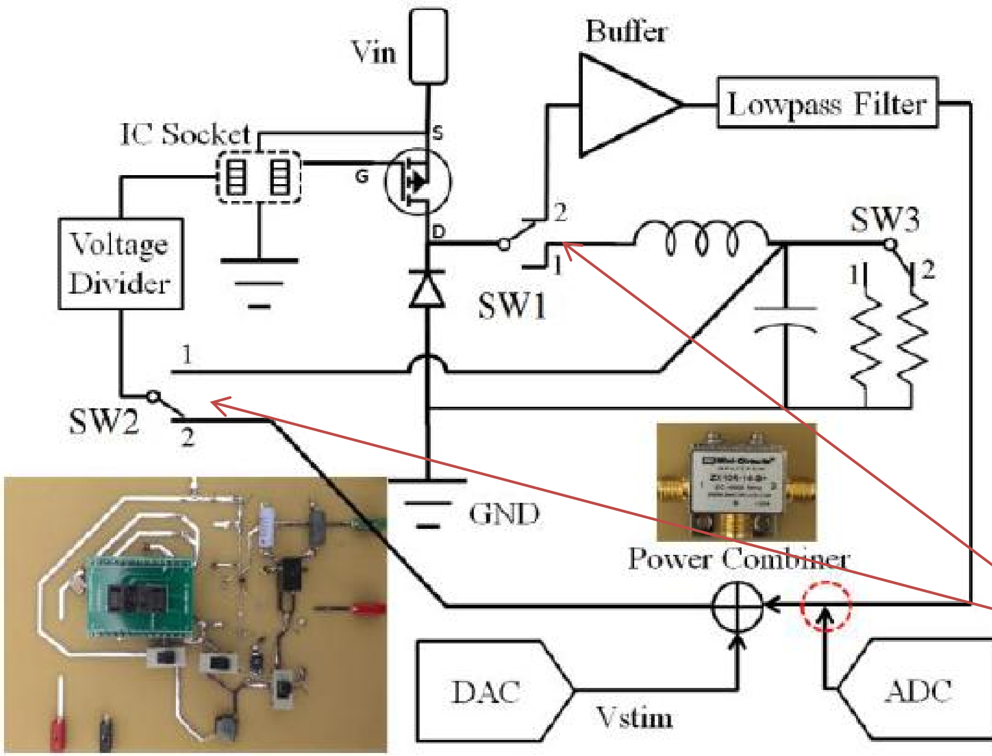
- For most specs, identical or better guardbands resulted

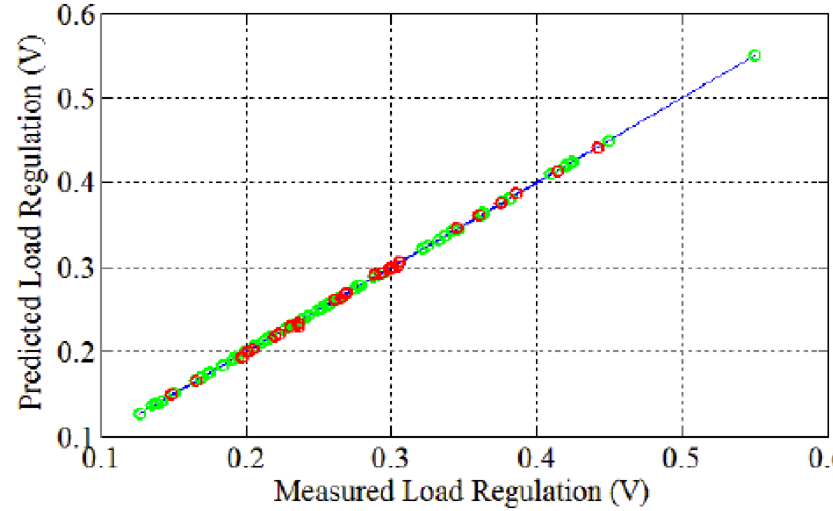


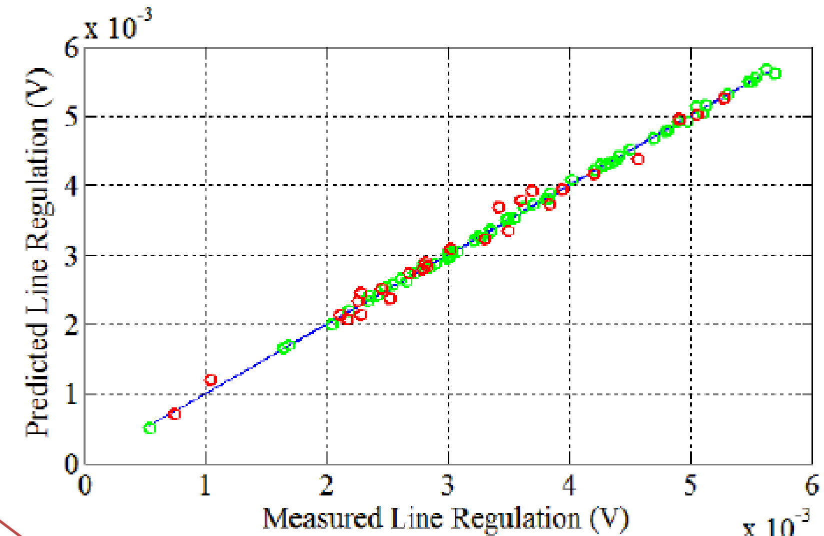
Hysteretic Buck Converter



100 chips (LM3485)

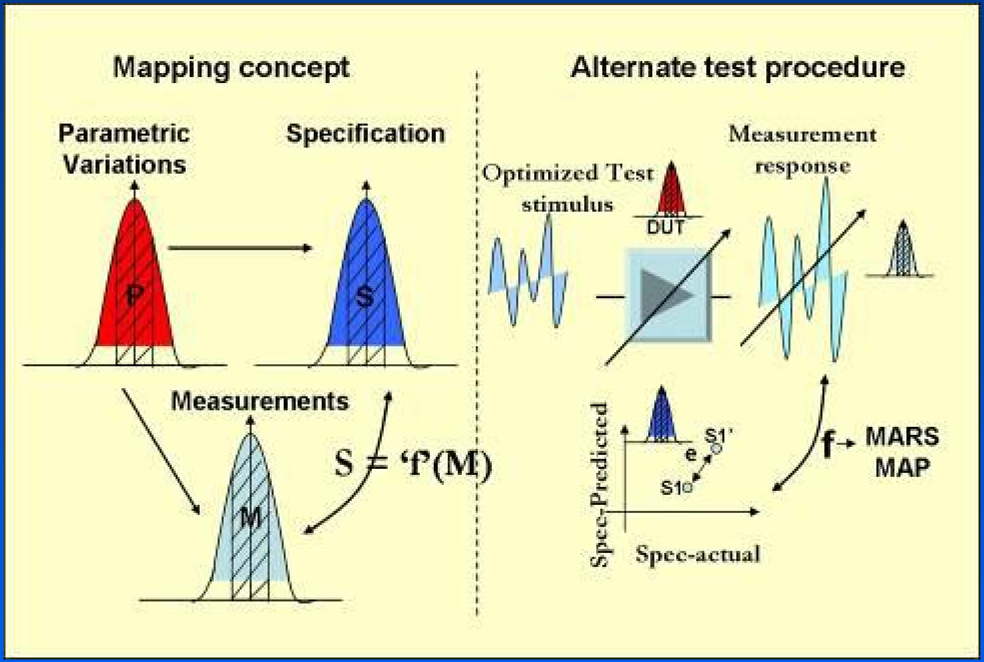






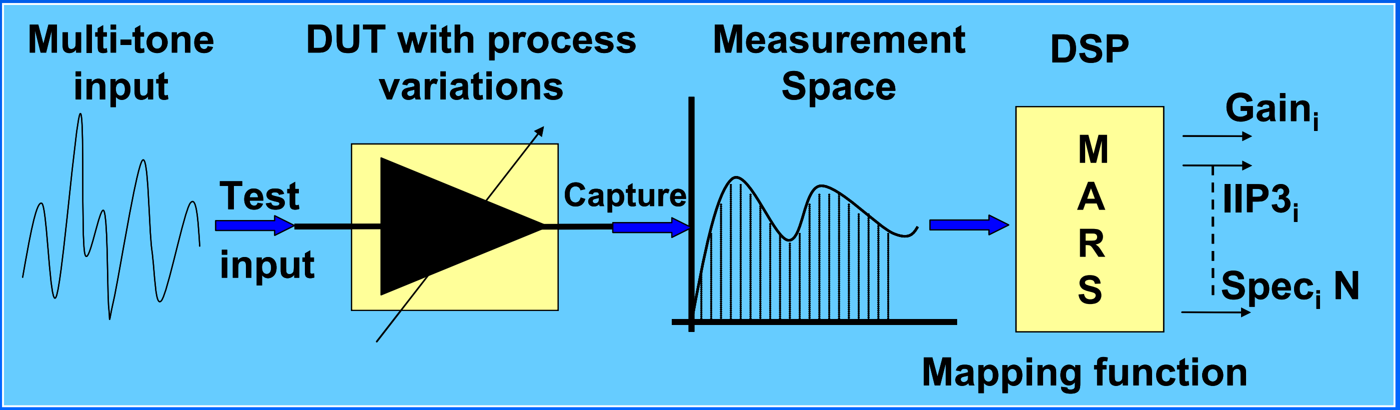
SW1 and SW2 in positions 2 for proposed test and position 1 for conventional test

BIST for Multiple Specs

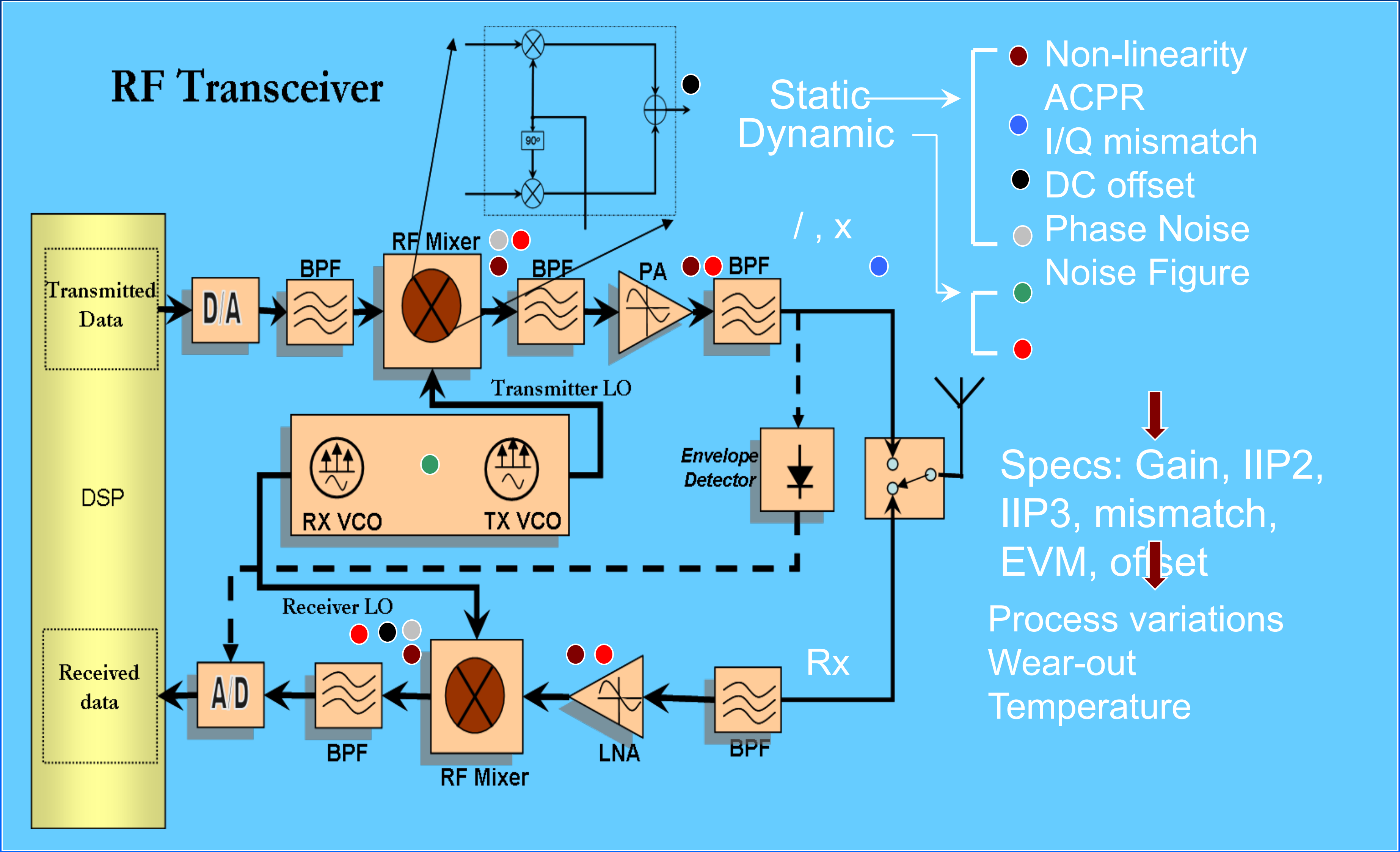


SIGNATURE TEST !

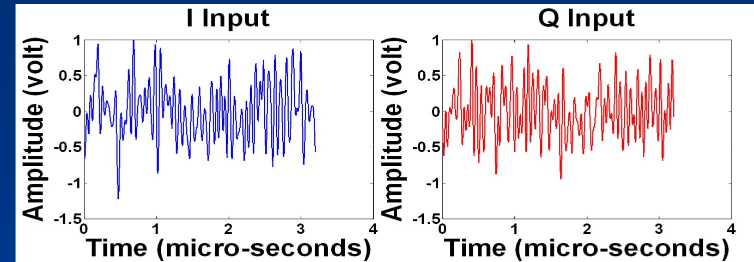
Production Phase

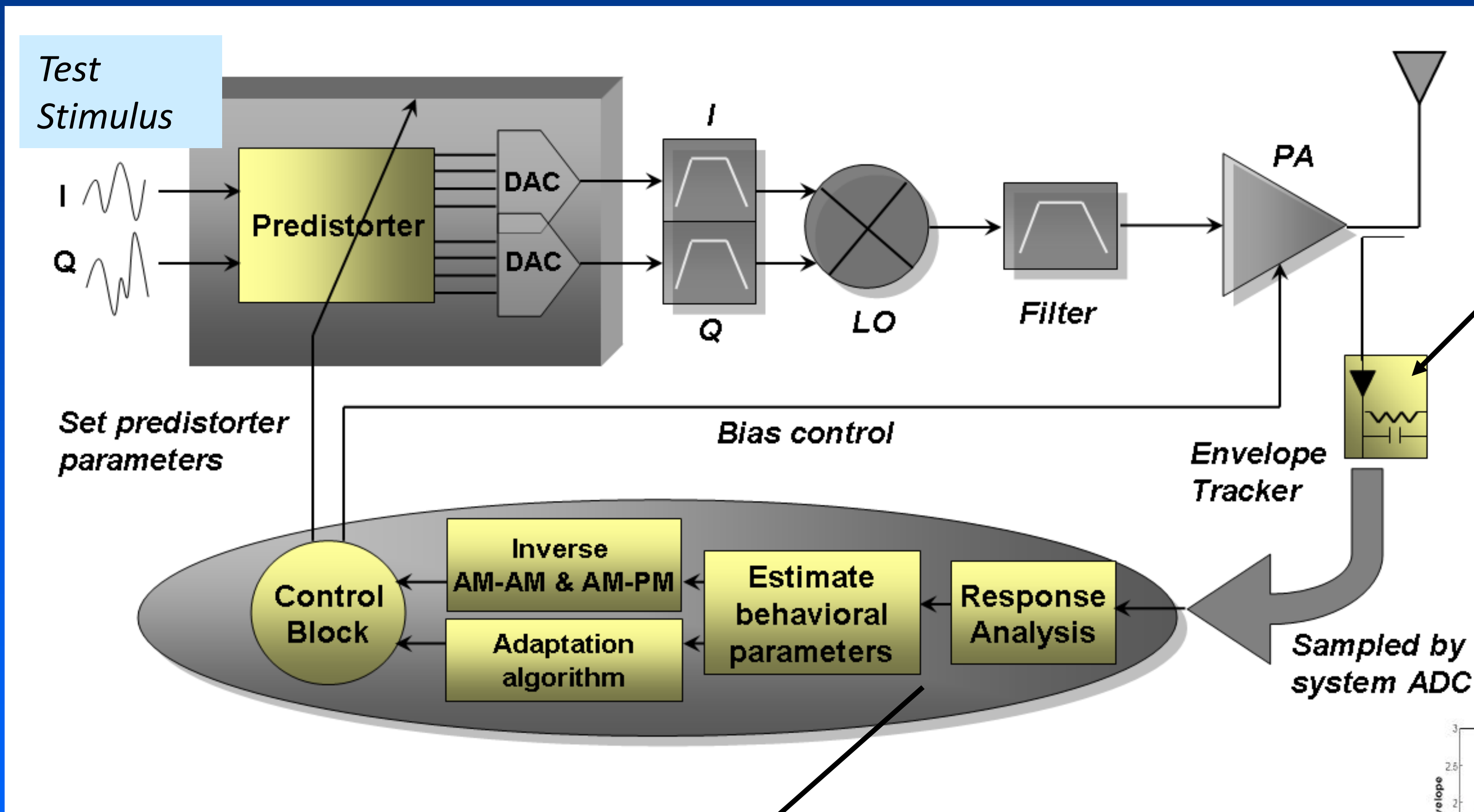


RF Transceiver Non-idealities



Signature-BIST: Overview

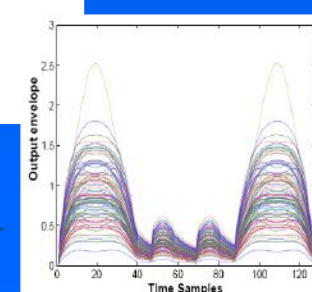




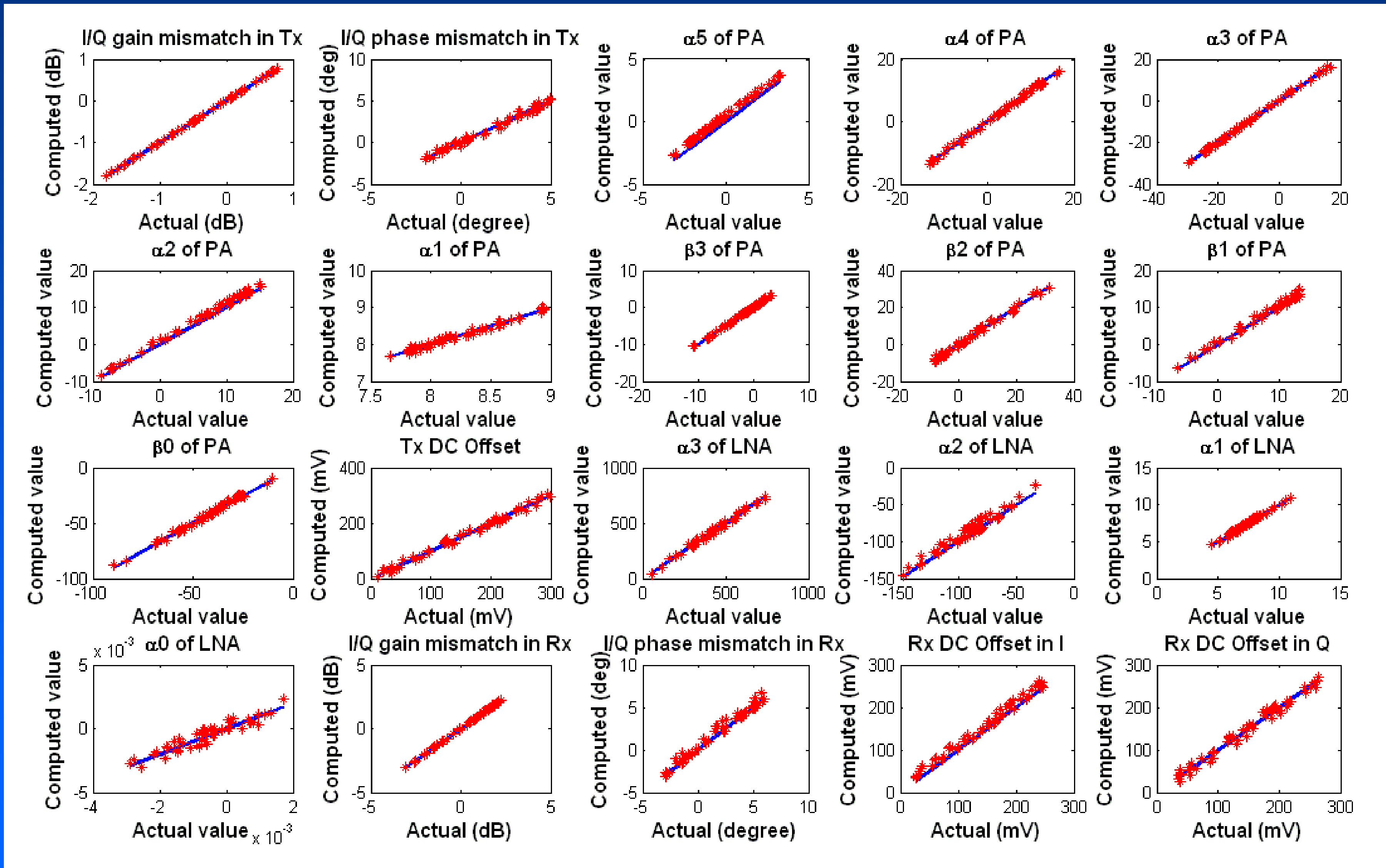
RF to low-frequency conversion

Diagnosis

Envelope response

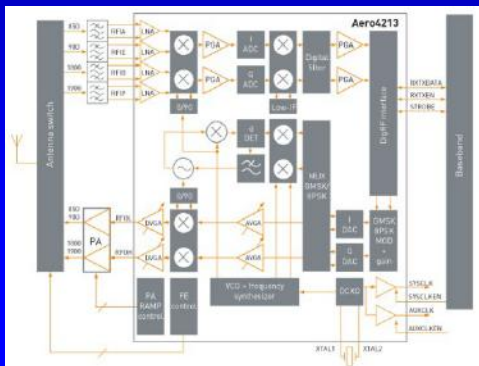


Signature Based Model Parameter Estimation



Current State-of-Art: Tuning

Phase1: Characterization



RF Module level specification testing

Bench →

§1 , §2

Trimming

Tester →

§3

Phase2: Production

Trimming

Calibration

RF System level specification testing

Fabrication

Characterization

Design

Trimming

Production test

Process

Trimming
&
Calibration

- Expensive !
- Impacts time to market

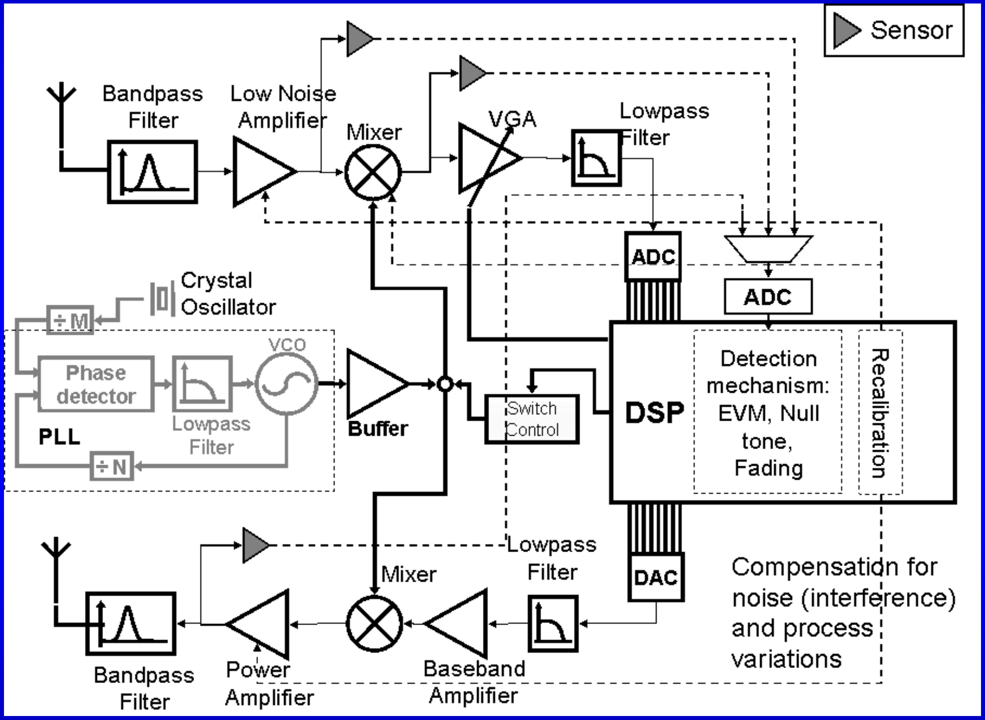
§ 1. Texas Instruments, stack and rack bench equipments

§ 2. Lee, K. et.al, "The Impact of semiconductor technology scaling on CMOS RF and Digital Circuits for Wireless Applications", IEEE Trans. Elec. Devices, July 2006

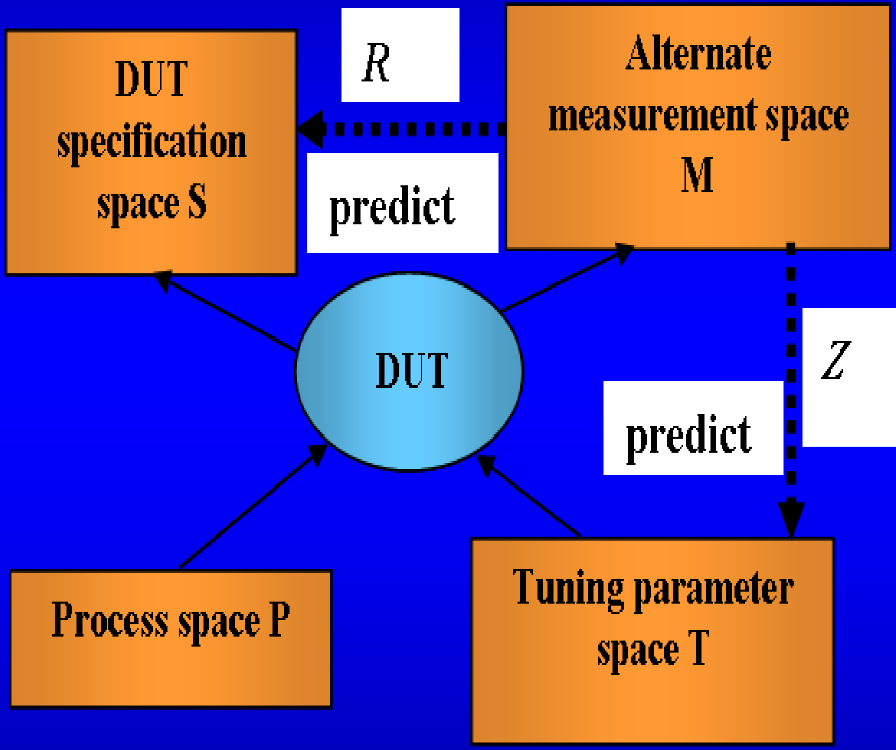
§ 3. Advantest tester

Tuning: Learning Driven

Tuning Architecture

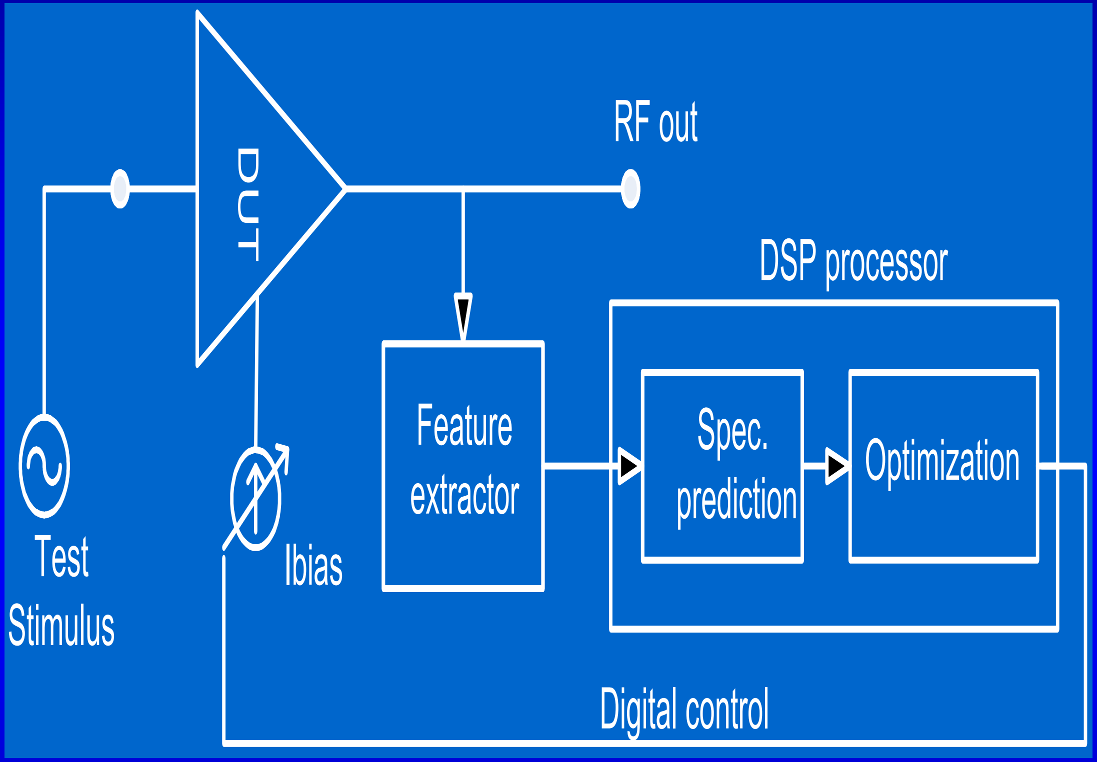


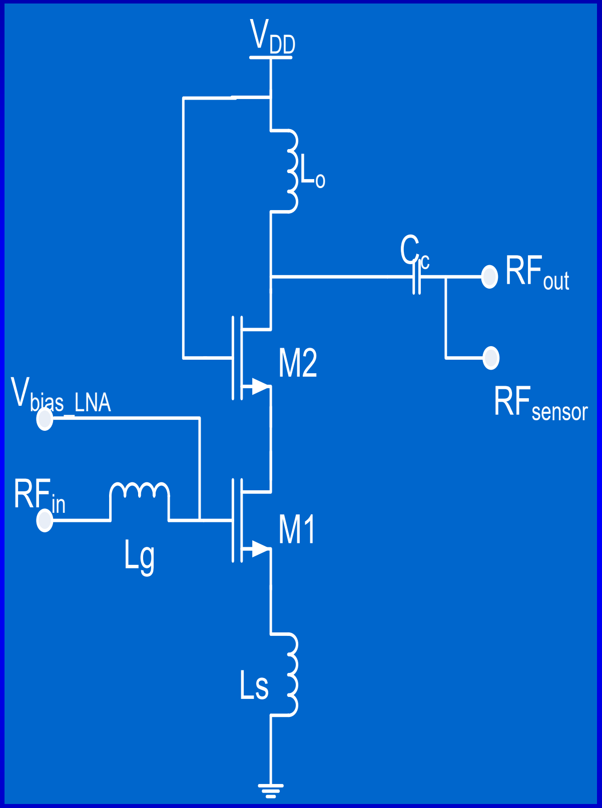
Supervised Learning



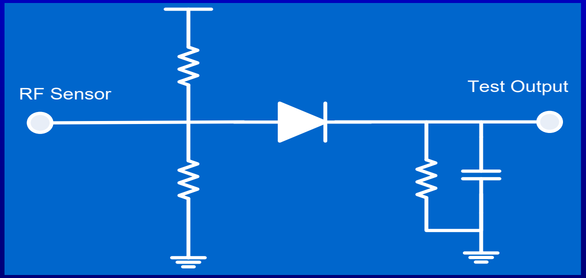
- Ability to tune for multiple specs using *single data acquisition*
- Ability to perform *near optimal tuning*
- *Minimal on-chip hardware* overhead

Learning driven tuning algorithms

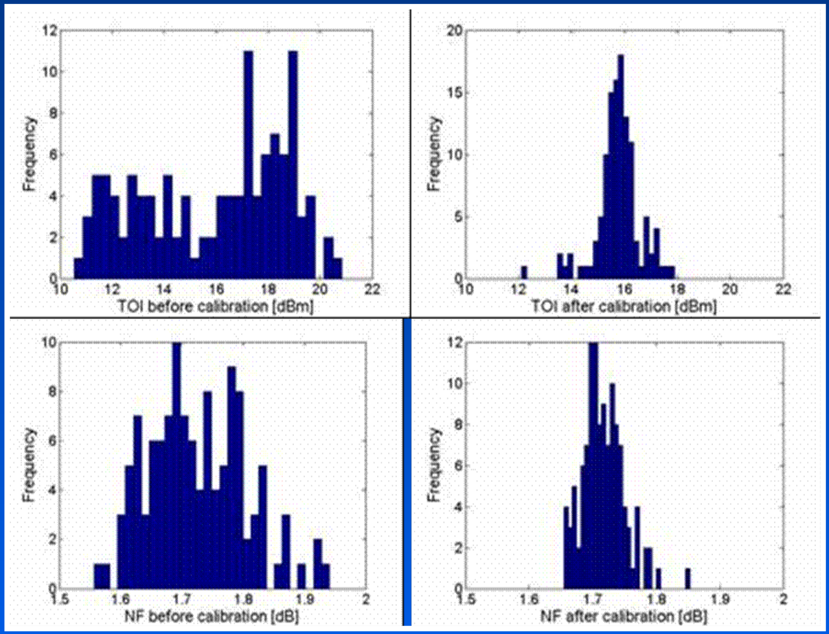


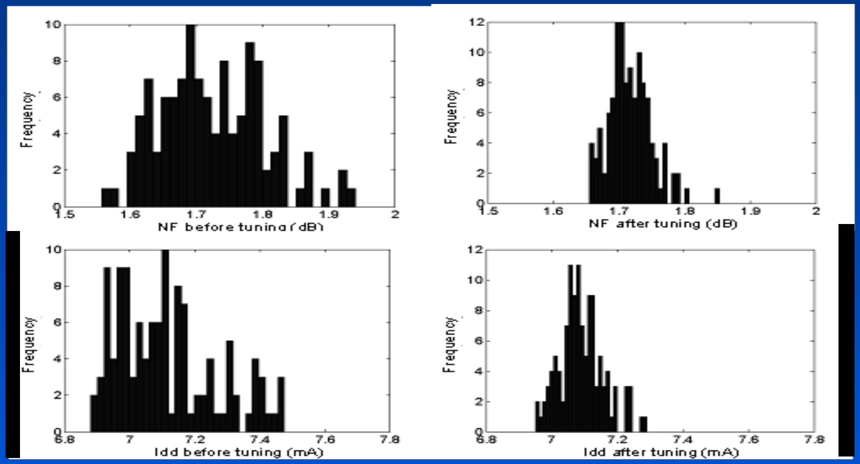


Need accurate learning algorithms!



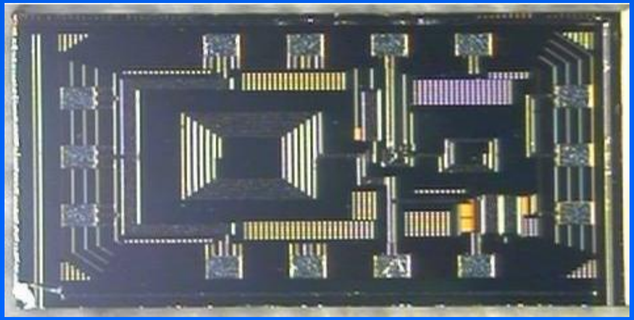
Can predict optimal tuning knob values from DUT response: One-shot tuning !





NF (top) and Idd (bottom) before tuning.

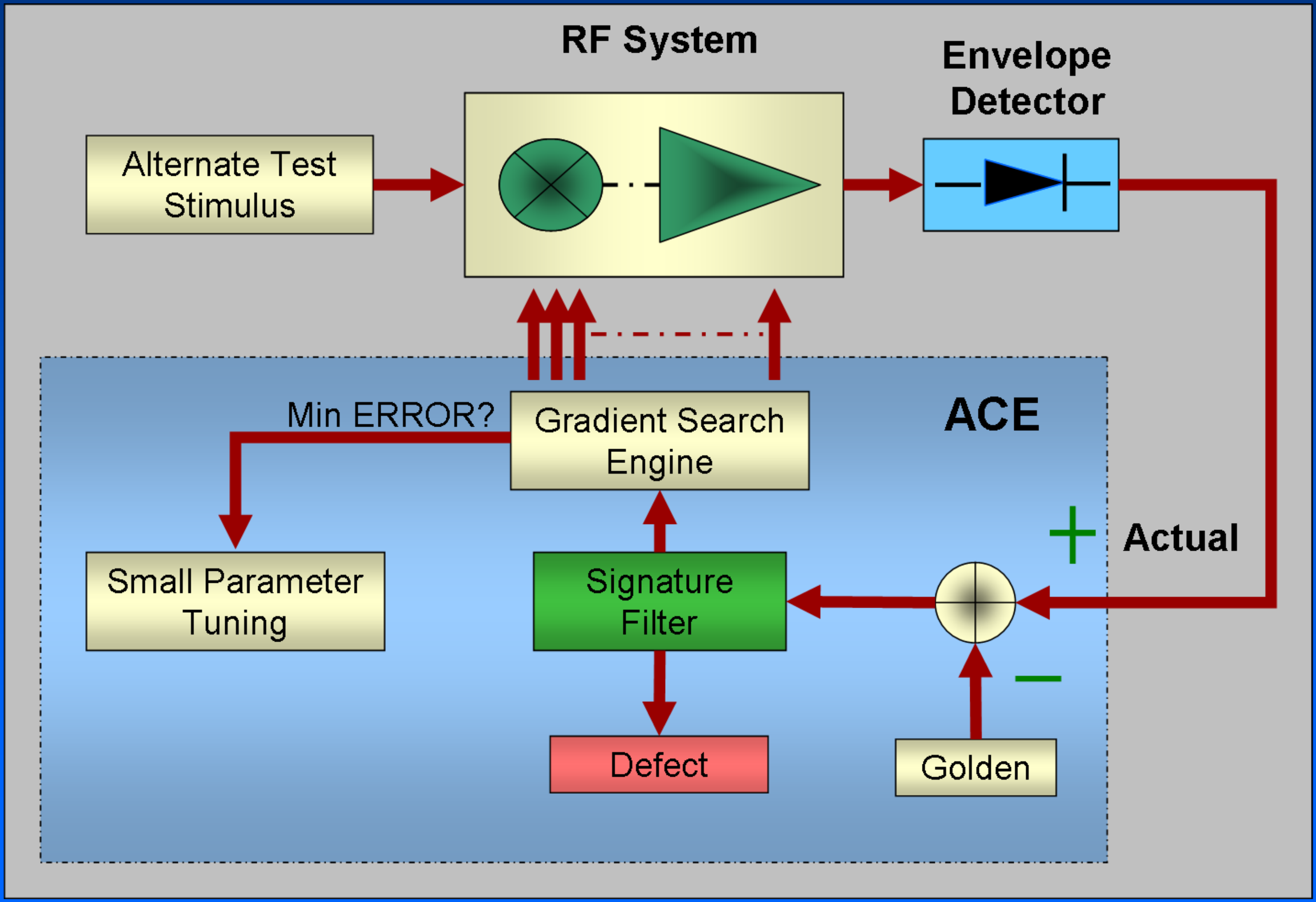
NF (top) and Idd (bottom) after tuning



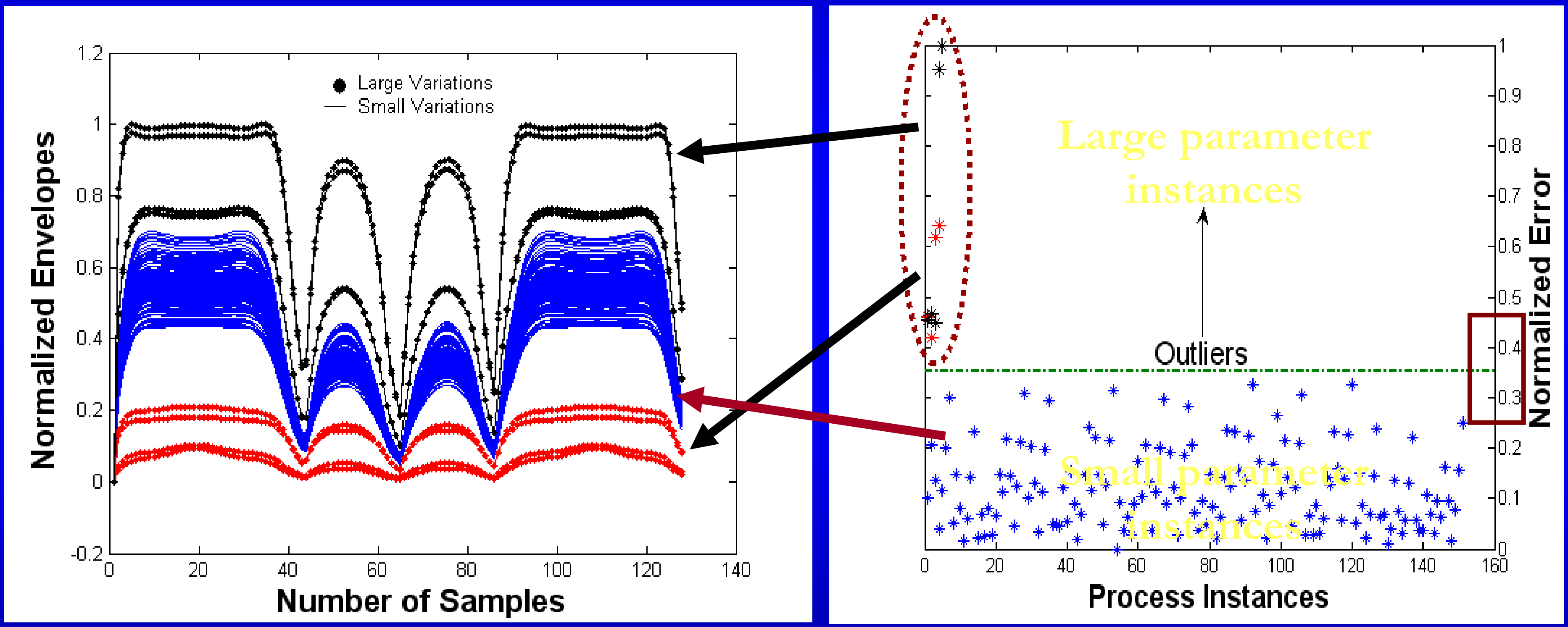
Self-healing LNA !

70% to 99% yield improvement

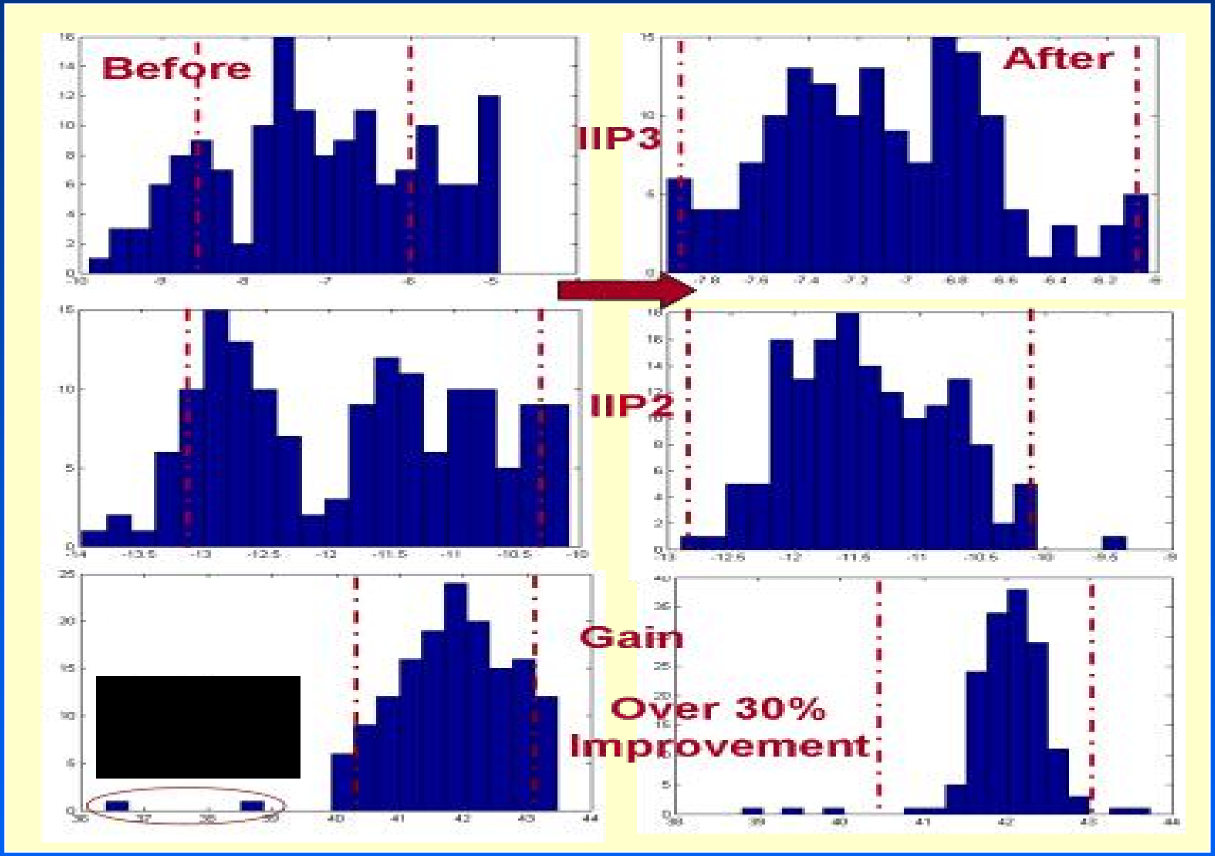
Parameter Tuning: Iterative



Experimental Results: Test Response to Tuning

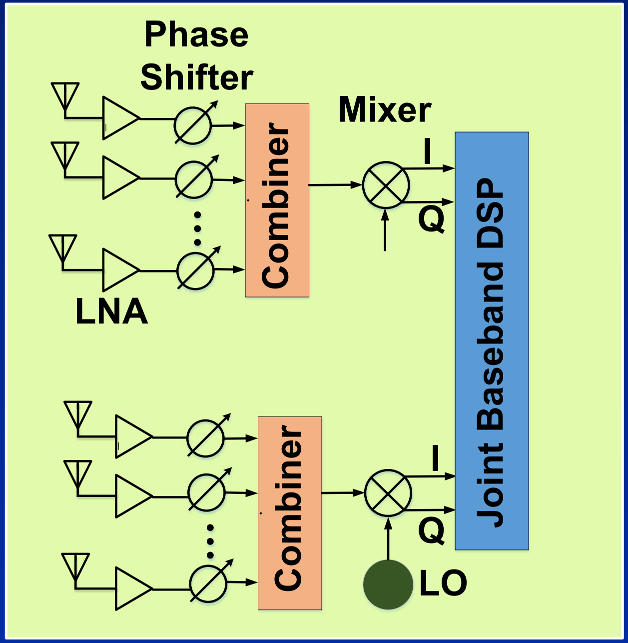


Experimental Results: Iterative Tuning



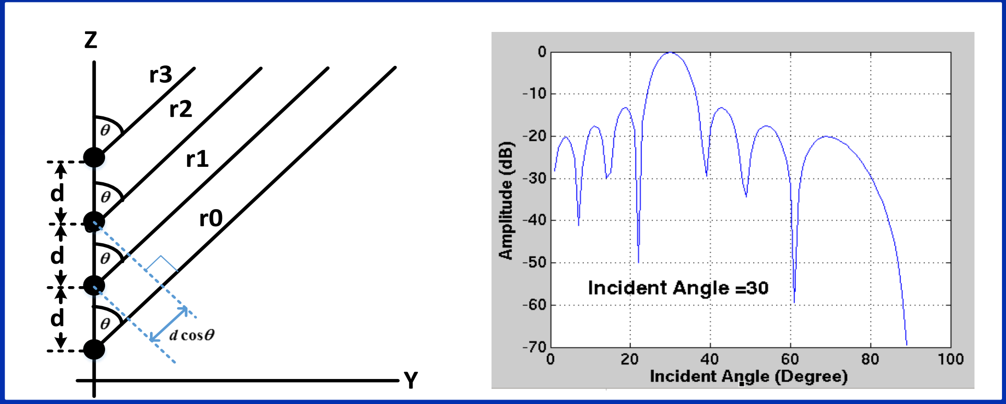
- 207 possible knob combinations (P1) for yield recovery
- Power conscious knob combination (P1) : 0.5724W
- Converged Knob combination (P1) : 0.5724W

Concurrent Built In Test and Tuning of Beamforming MIMO Systems Using Learning Assisted Performance Optimization



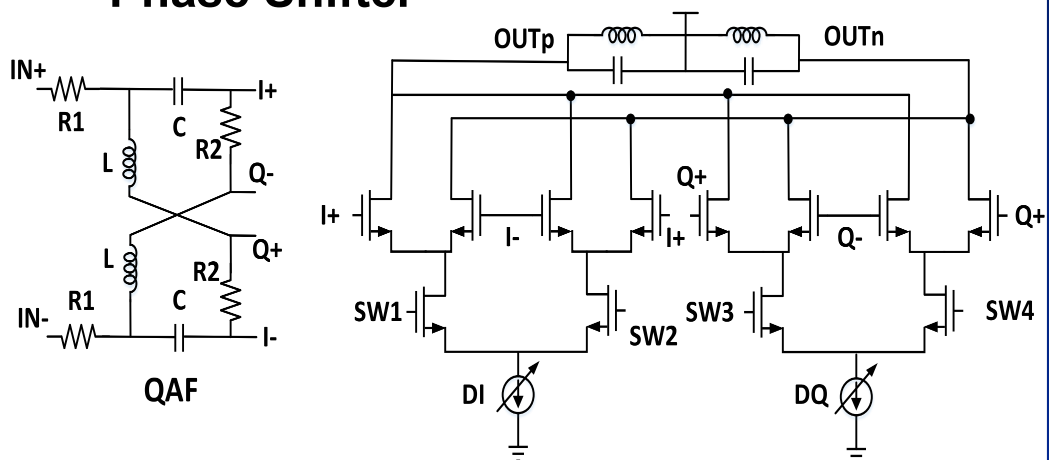
MIMO Test Challenges

1) Decoupling of test results for individual antenna-RF chains from combined signals
2) *Concurrently test all mixed-signal/RF components in all the RF chains* with the least test cost
3) Test and calibrate for all beam steering angles



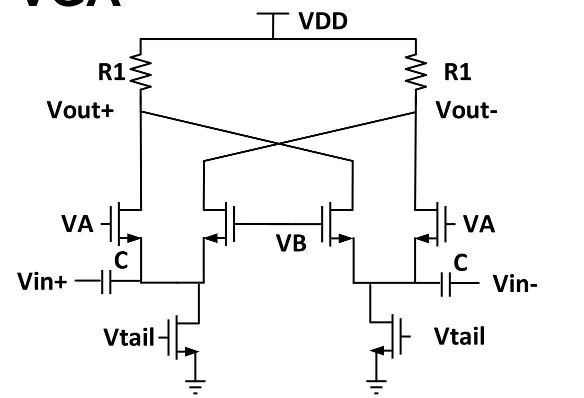
Tuning Bits

Phase Shifter

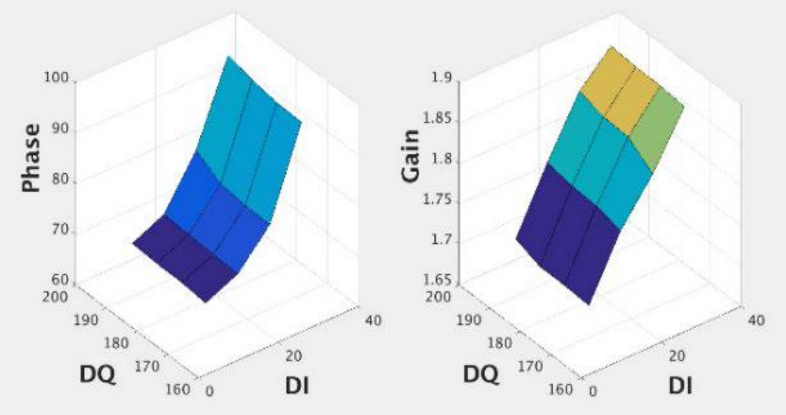


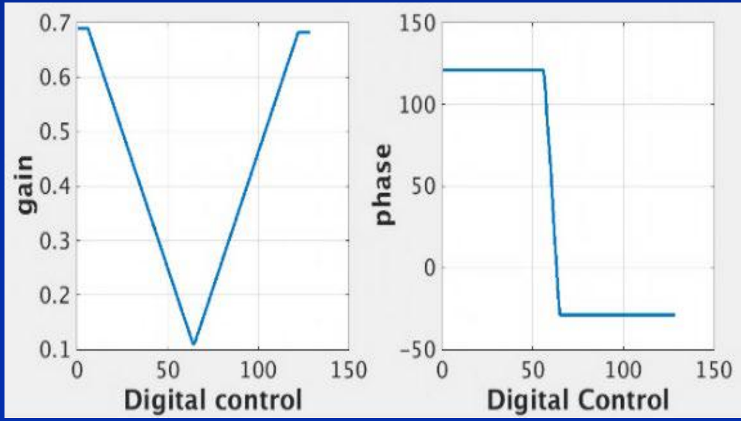
Coarse Bits : SW1-4, MSB 4 bits of DI,DQ
Fine Bits: LSB 4 bits of DI,DQ

VGA

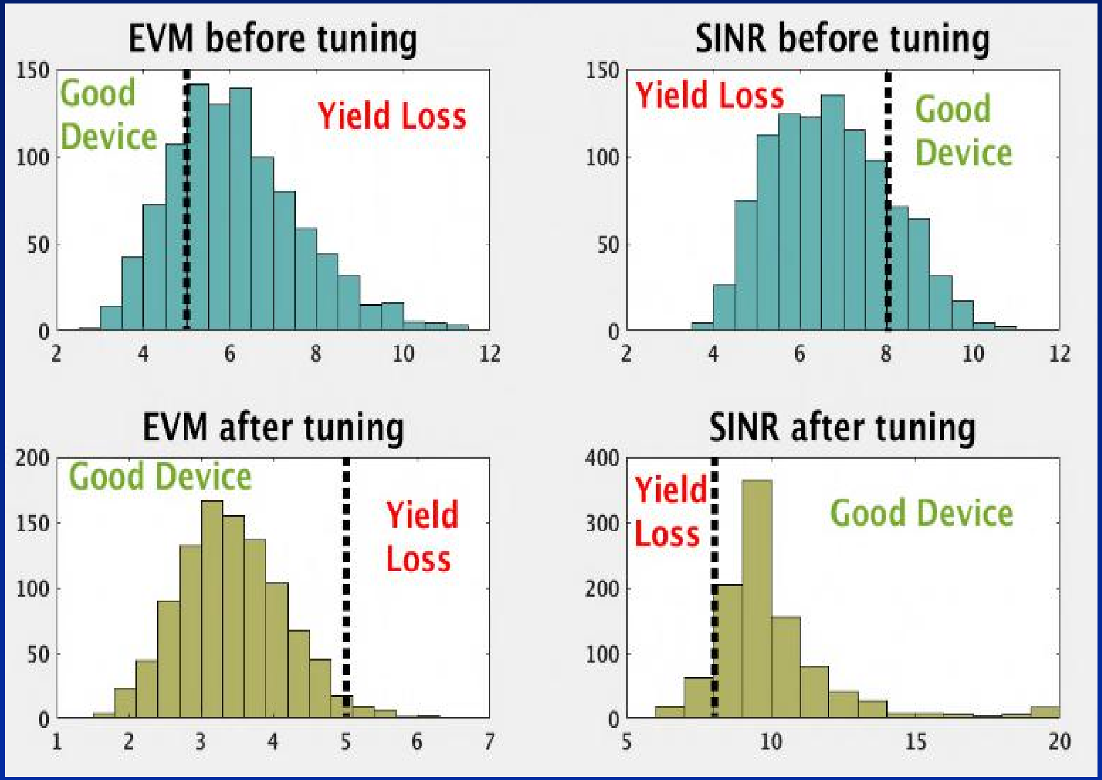


Coarse Bits : MSB 4 bits of VA
Fine Bits : LSB 4 bits of VA





Efficacy of Proposed Tuning Methodology



- ***Yield improvement : 11% to 88%***

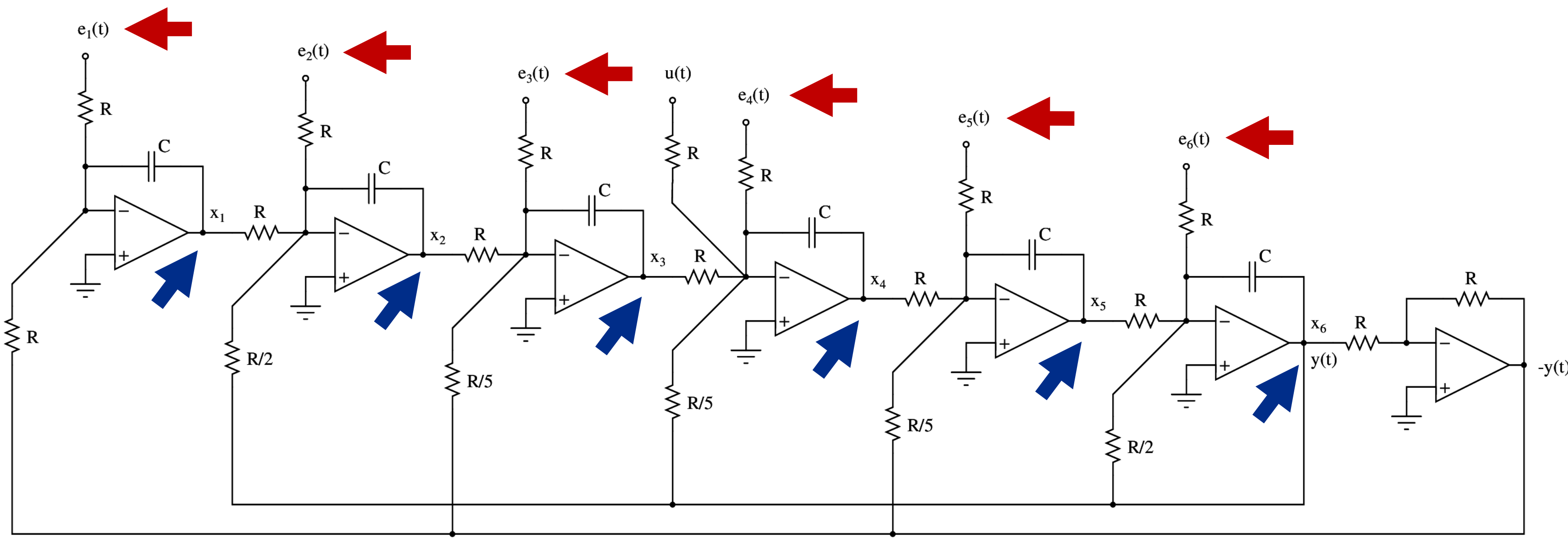
(acceptance criteria: EVM 5% SINR 8dB)

- **256 bits tuned simultaneously**
- **Average tuning optimization process takes 2.5 ms in MATLAB.**

Adaptation Based on Algorithmic Circuit-Level Encodings: *Circuits in the Field*

Case Study

6th Order Band-Pass Butterworth Filter



Specification	Value
Frequency	100 MHz
Band Pass Gain	1 V/V
Quality Factor	1
Band Pass	100 MHz

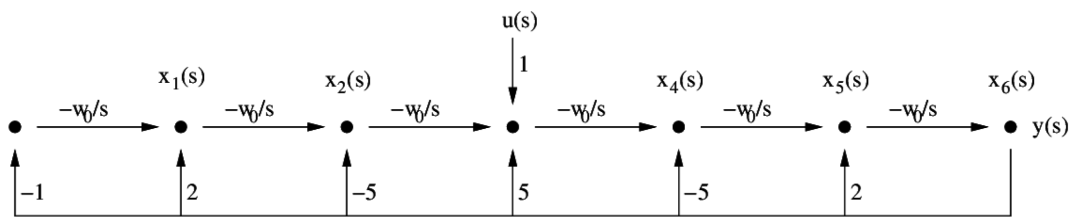
$$H(s) = \frac{-\frac{s^3}{\omega_0^3}}{\frac{s^6}{\omega_0^6} + 2\frac{s^5}{\omega_0^5} + 5\frac{s^4}{\omega_0^4} + 5\frac{s^3}{\omega_0^3} + 5\frac{s^2}{\omega_0^2} + 2\frac{s}{\omega_0} + 1}$$

6 STATES TO CHECK: $x_1, \ldots, x_6$

6 ERROR SIGNALS: $e_1, \ldots, e_6$

Case Study

State Space Representation



BAND-PASS FILTER SIGNAL FLOW GRAPH DESCRIPTION

$$-\frac{s}{\omega_0}\begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & -1 \\ 1 & 0 & 0 & 0 & 0 & 2 \\ 0 & 1 & 0 & 0 & 0 & -5 \\ 0 & 0 & 1 & 0 & 0 & 5 \\ 0 & 0 & 0 & 1 & 0 & -5 \\ 0 & 0 & 0 & 0 & 1 & 2 \end{bmatrix}}_{\text{SYSTEM MATRIX } (A)} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \\ 0 \\ 0 \end{bmatrix} u(s)$$

BAND-PASS FILTER STATE SPACE DESCRIPTION

INPUT SIGNAL (*u*)

STATE VECTOR (*X*)

INPUT MATRIX (*B*)

Analog Checksums

Redundant States

Consider a state space system… $sX = AX + BU$

$$s\underbrace{\begin{bmatrix} x_1 \\ \vdots \\ x_n \end{bmatrix}}_{X} = \underbrace{\begin{bmatrix} a_{11} & \cdots & a_{1n} \\ \vdots & \ddots & \vdots \\ a_{n1} & \cdots & a_{nn} \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} x_1 \\ \vdots \\ x_n \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} b_{11} & \cdots & b_{1p} \\ \vdots & \ddots & \vdots \\ b_{n1} & \cdots & b_{np} \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} u_1 \\ \vdots \\ u_p \end{bmatrix}}_{U}$$

And a set of scalars… $\alpha = [\alpha_1, \alpha_2, \ldots, \alpha_n]$ ← **CODING VECTOR**

Extend the system with a new redundant state being a linear combination of $x_1, \ldots, x_n$**…**

$$s\begin{bmatrix} x_1 \\ \vdots \\ x_n \\ \hline x_r \end{bmatrix} = \left[\begin{array}{ccc|c} a_{11} & \cdots & a_{1n} & 0 \\ \vdots & \ddots & \vdots & \vdots \\ a_{n1} & \cdots & a_{nn} & 0 \\ \hline (\alpha A)_1 & \cdots & (\alpha A)_n & 0 \end{array}\right] \begin{bmatrix} x_1 \\ \vdots \\ x_n \\ \hline x_r \end{bmatrix} + \begin{bmatrix} b_{11} & \cdots & b_{1p} \\ \vdots & \ddots & \vdots \\ b_{n1} & \cdots & b_{np} \\ \hline (\alpha B)_1 & \cdots & (\alpha B)_p \end{bmatrix} \begin{bmatrix} u_1 \\ \vdots \\ u_p \end{bmatrix}$$

REDUNDANT STATE

Error Signal Generation

Error signal is defined as…

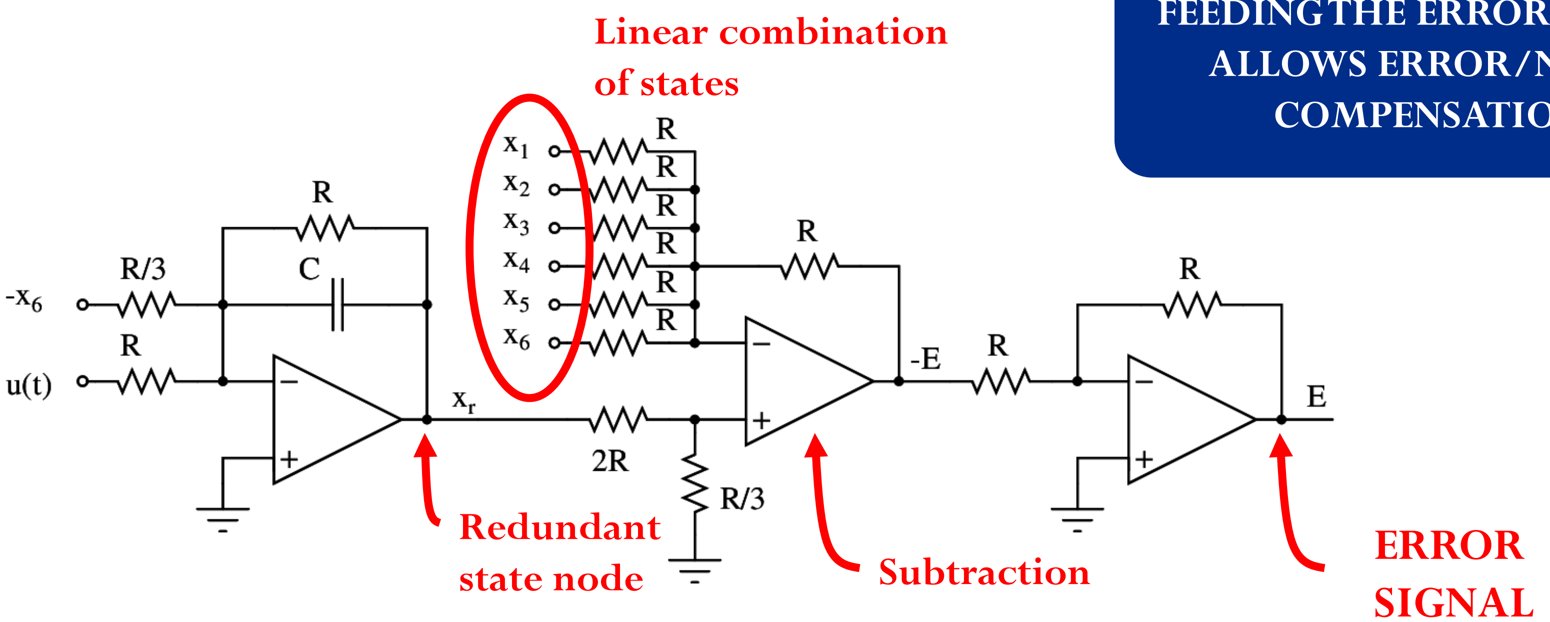
$$E = \alpha X - x_r$$

And we already know the expression for the redundant state…

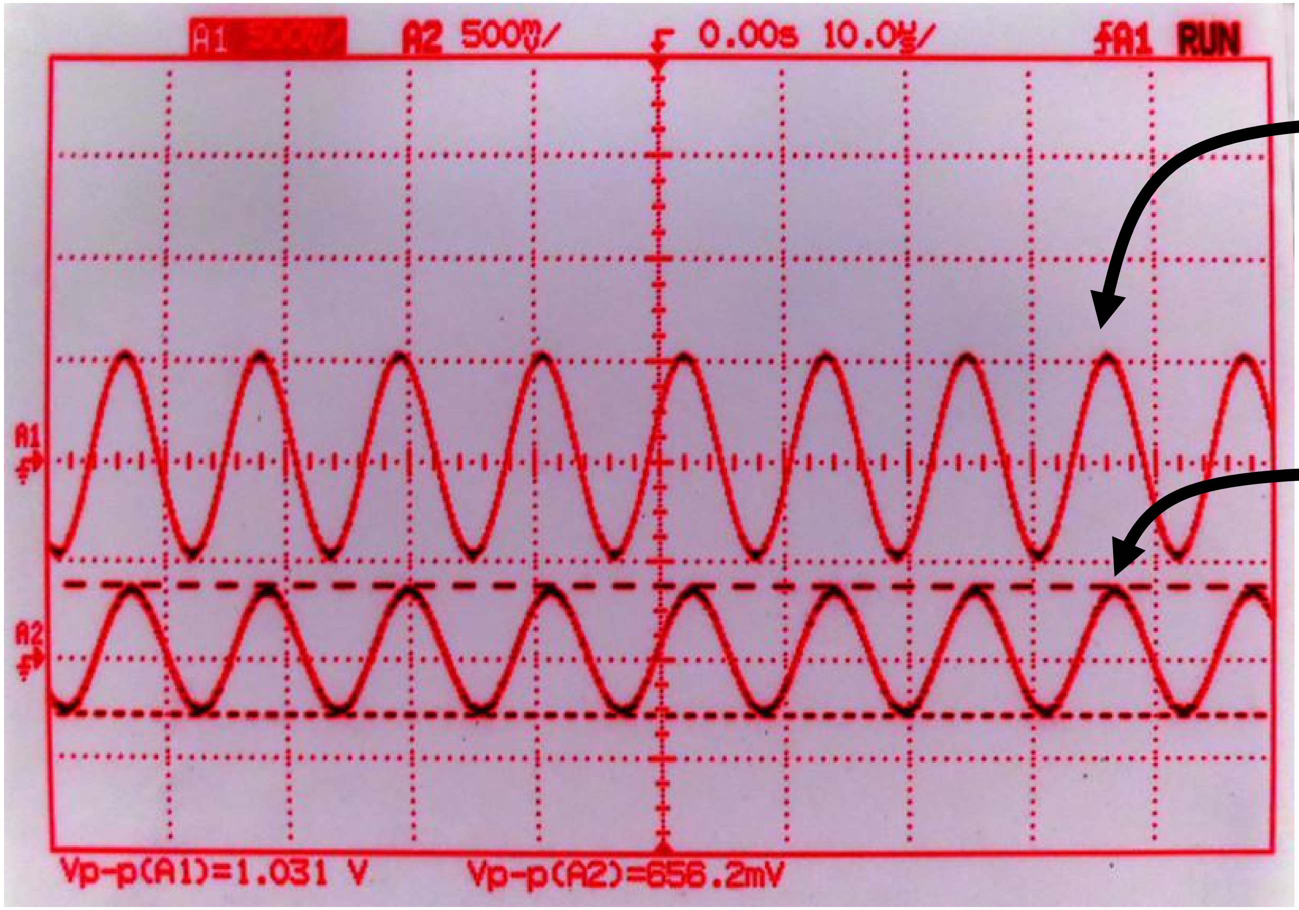
$$-\frac{s}{\omega_0} x_r = 3(-x_6) + x_r + u(s)$$

We just need an integration, a linear combination and a subtraction…

FEEDING THE ERROR SIGNAL ALLOWS ERROR/NOISE COMPENSATION



Input-Output
With No Perturbation

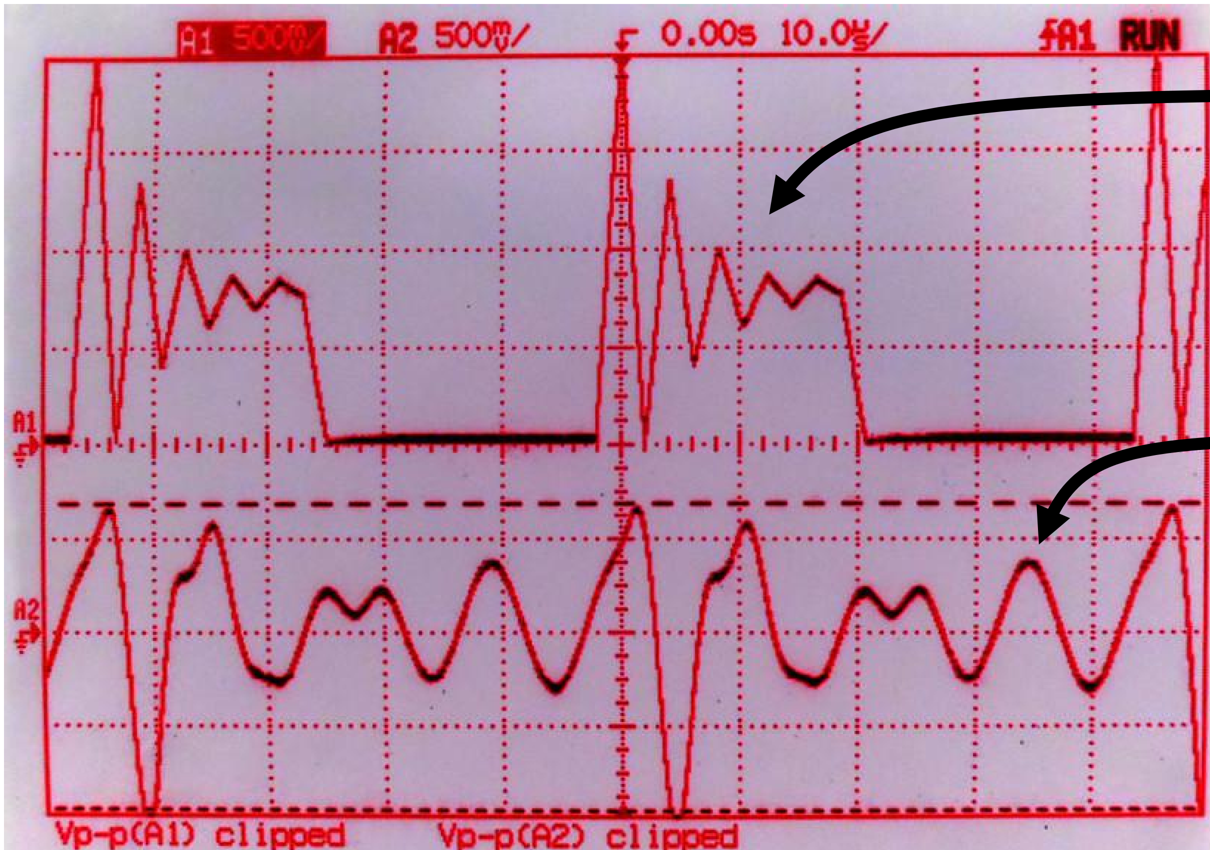


PURE SINUSOIDAL INPUT SIGNAL

PURE SINUSOIDAL RESPONSE

Perturbed Output

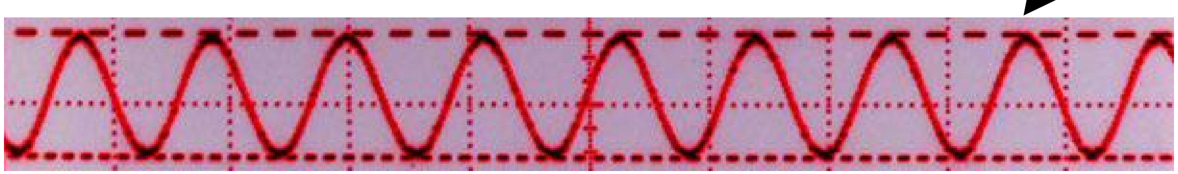
Before Compensation



INJECTED PERTURBATION SIGNAL AT STATE 3

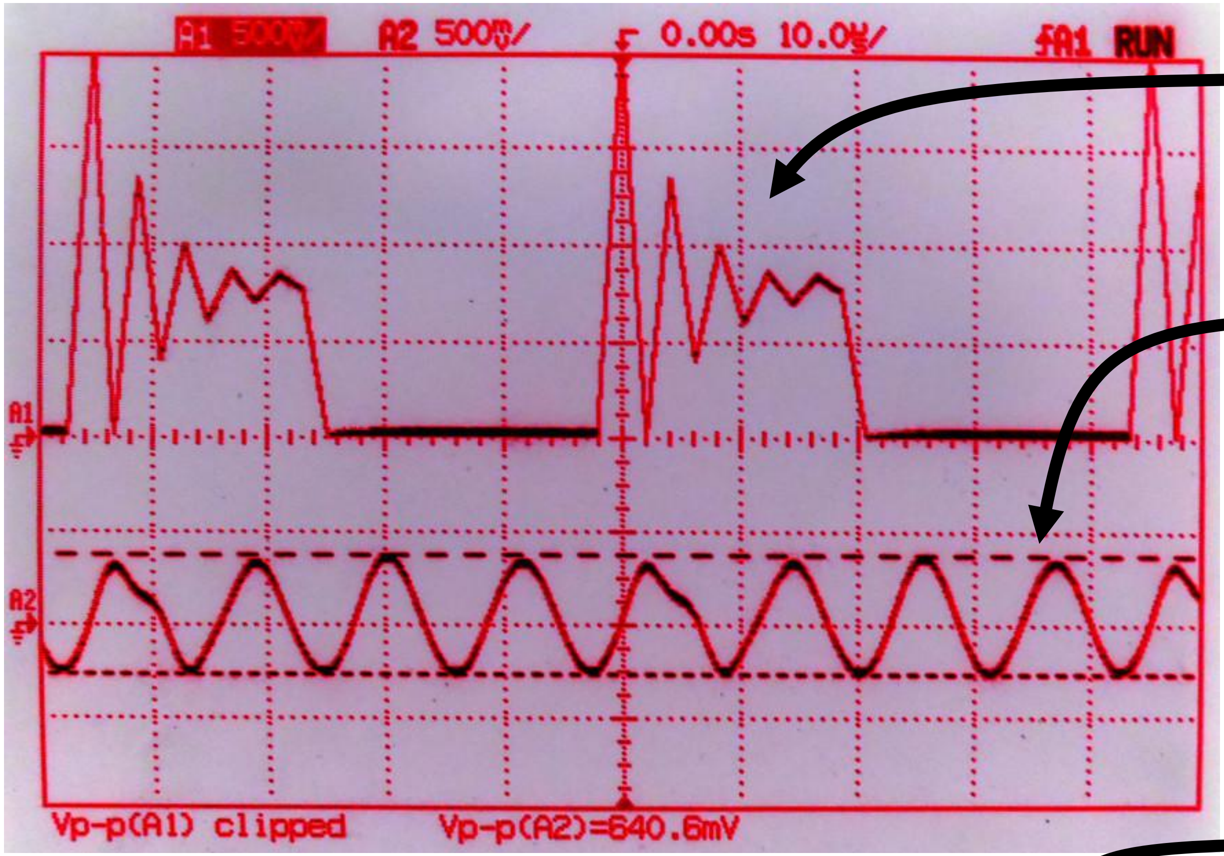
HIGHTLY PERTURBED FILTER RESPONSE

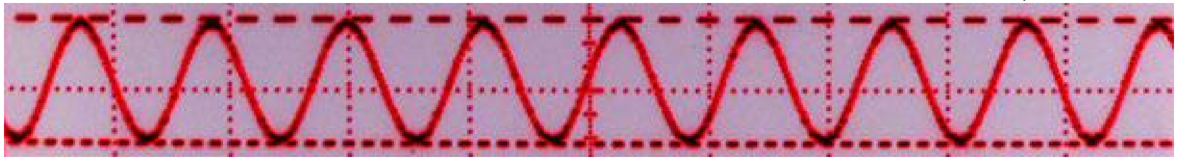
HOW IT SHOULD LOOK LIKE IF NO PERTURBATION WAS INJECTED



Compensated Output

After Compensation





INJECTED PERTURBATION SIGNAL AT STATE 3

FILTER RESPONSE WHEN ERROR/NOISE COMPENSATION IS APPLIED

ALMOST PERFECT COMPENSATION IS ACHIEVED

HOW IT SHOULD LOOK LIKE IF NO PERTURBATION WAS INJECTED

Future Work

- Exciting road ahead
  - Large scale sensor networks
  - Self-driven vehicles
  - Drones
  - Personal robots

Adapt in real-time to working environment, electro-mechanical degradation and failures

Questions