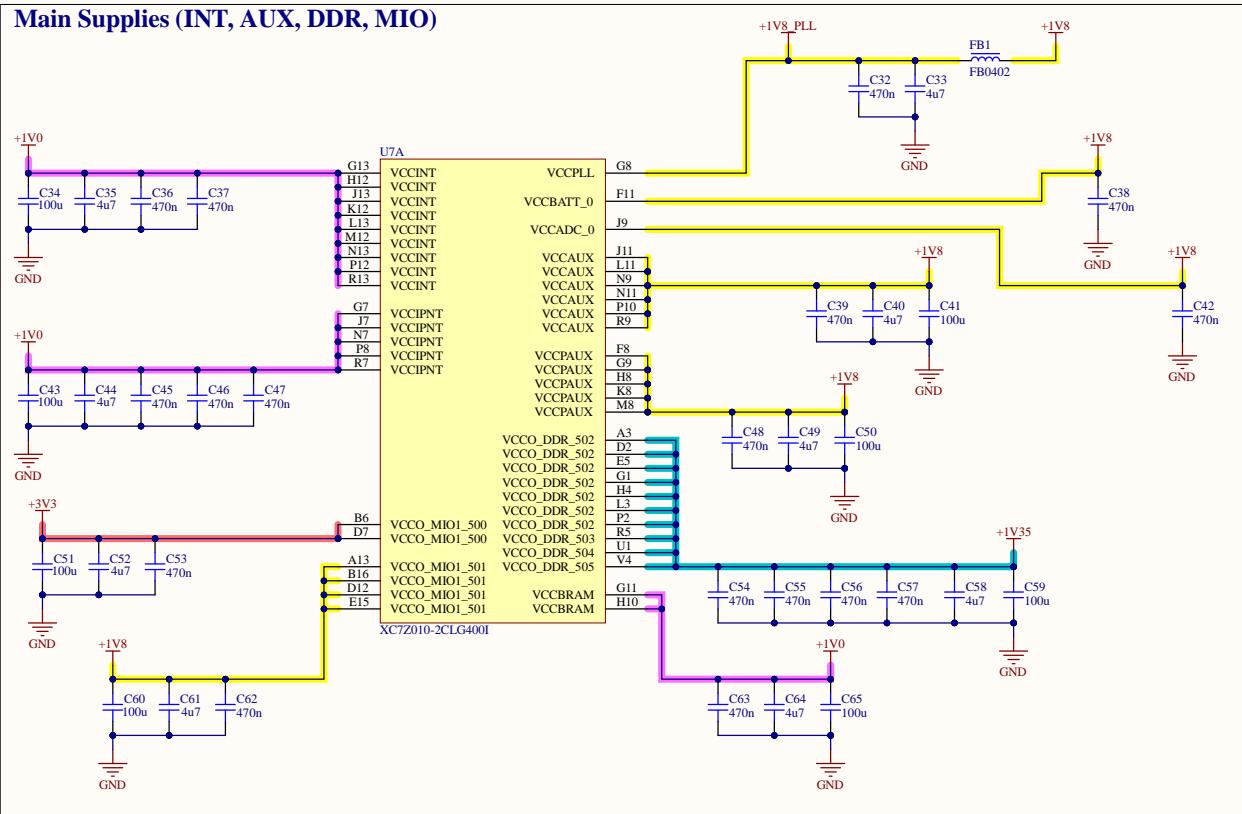
Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾ (Cont'd)

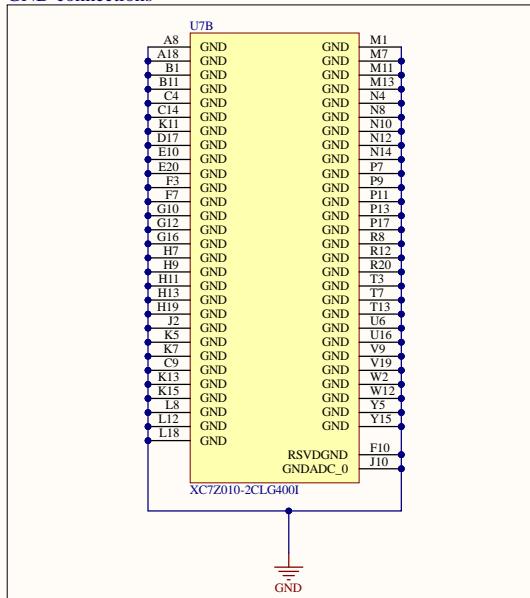
Symbol	Description	Min	Typ	Max	Units
$V_{PIN}^{(4)}$	PS DDR and MIO I/O input voltage	-0.20	-	$V_{CCO_DDR} + 0.20$	V
PL					
$V_{CCINT}^{(5)}$	PL internal supply voltage	0.95	1.00	1.05	V
	PL -1LI (0.95V) internal supply voltage	0.92	0.95	0.98	V
V_{CCAUX}	PL auxiliary supply voltage	1.71	1.80	1.89	V
$V_{CCBRAM}^{(8)}$	PL block RAM supply voltage	0.95	1.00	1.05	V
	PL -1LI (0.95V) block RAM supply voltage	0.92	0.95	0.98	V
$V_{CCO}^{(6)(7)}$	PL supply voltage for HR I/O banks	1.14	-	3.465	V
	I/O input voltage	-0.20	-	$V_{CCO} + 0.20$	V
$V_{IN}^{(4)}$	I/O input voltage (when $V_{CCO} = 3.3V$) for V_{REF} and differential I/O standards except TMDS_33 ⁽⁸⁾	-0.20	-	2.625	V
$I_{IN}^{(9)}$	Maximum current through any (PS or PL) pin in a powered or unpowered bank when forward biasing the clamp diode	-	-	10	mA
$V_{CCBAT}^{(10)}$	Battery voltage	1.0	-	1.89	V
GTP Transceiver (XC7Z012S and XC7Z010 Only)					
$V_{MGTAVCC}^{(11)}$	Analog supply voltage for the GTP transmitter and receiver circuits	0.97	1.0	1.03	V
$V_{MGTAVTT}^{(11)}$	Analog supply voltage for the GTP transmitter and receiver termination circuits	1.17	1.2	1.23	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
Temperature					

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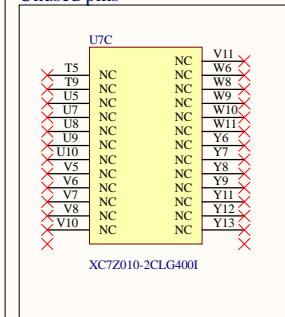
Main Supplies (INT, AUX, DDR, MIO)



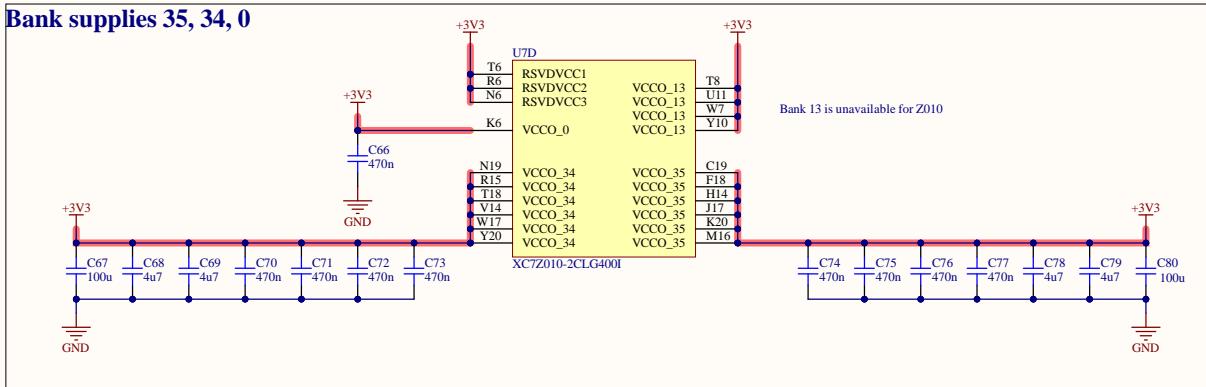
GND connections



Unused pins

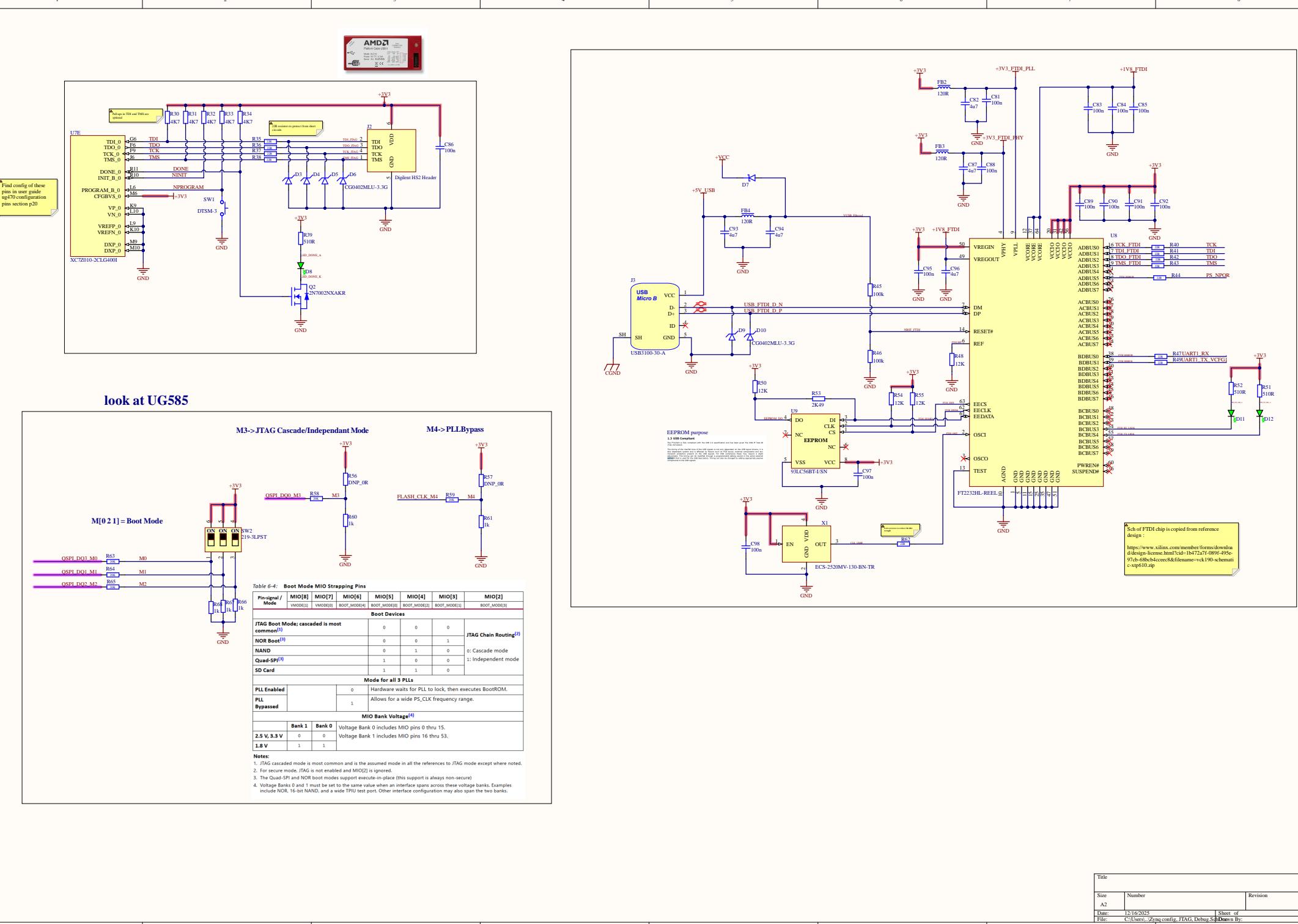


Bank supplies 35, 34, 0

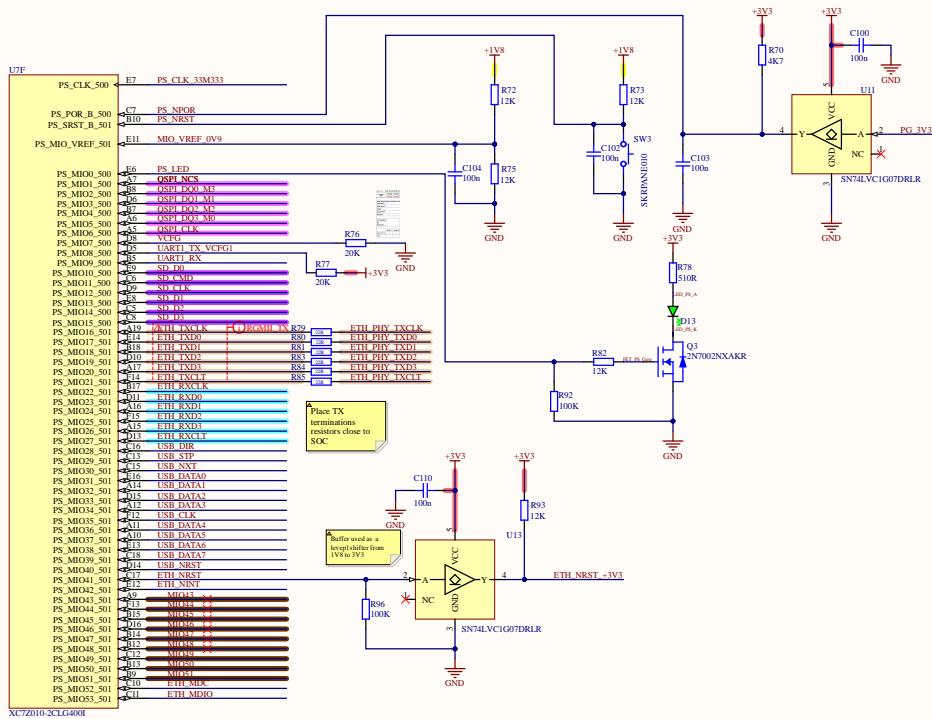


Bank 13 is unavailable for

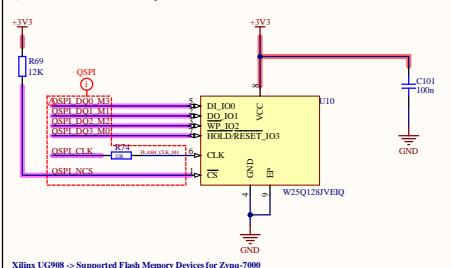
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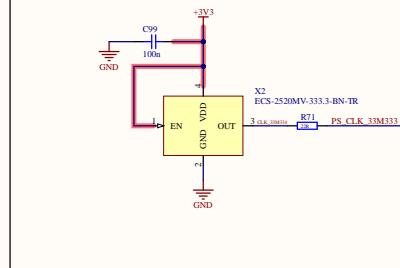
Processing system (bank 500 & 501)



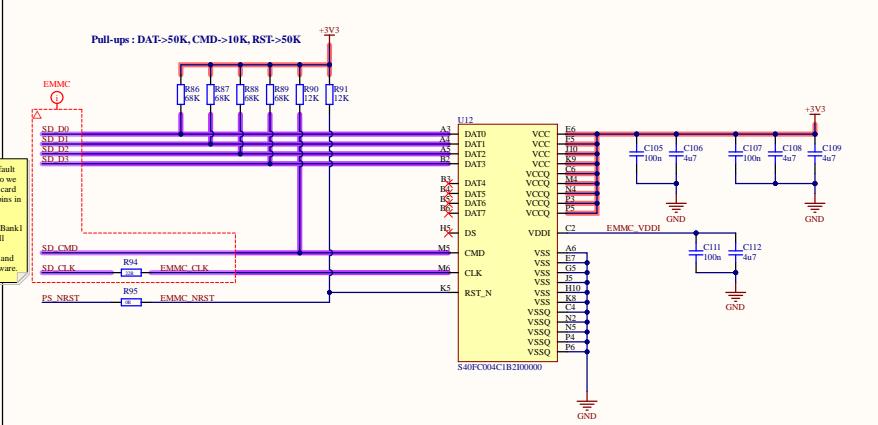
QSPI Flash memory 128MBit



PS CLOCK 33.3MHz



EMMC Memory

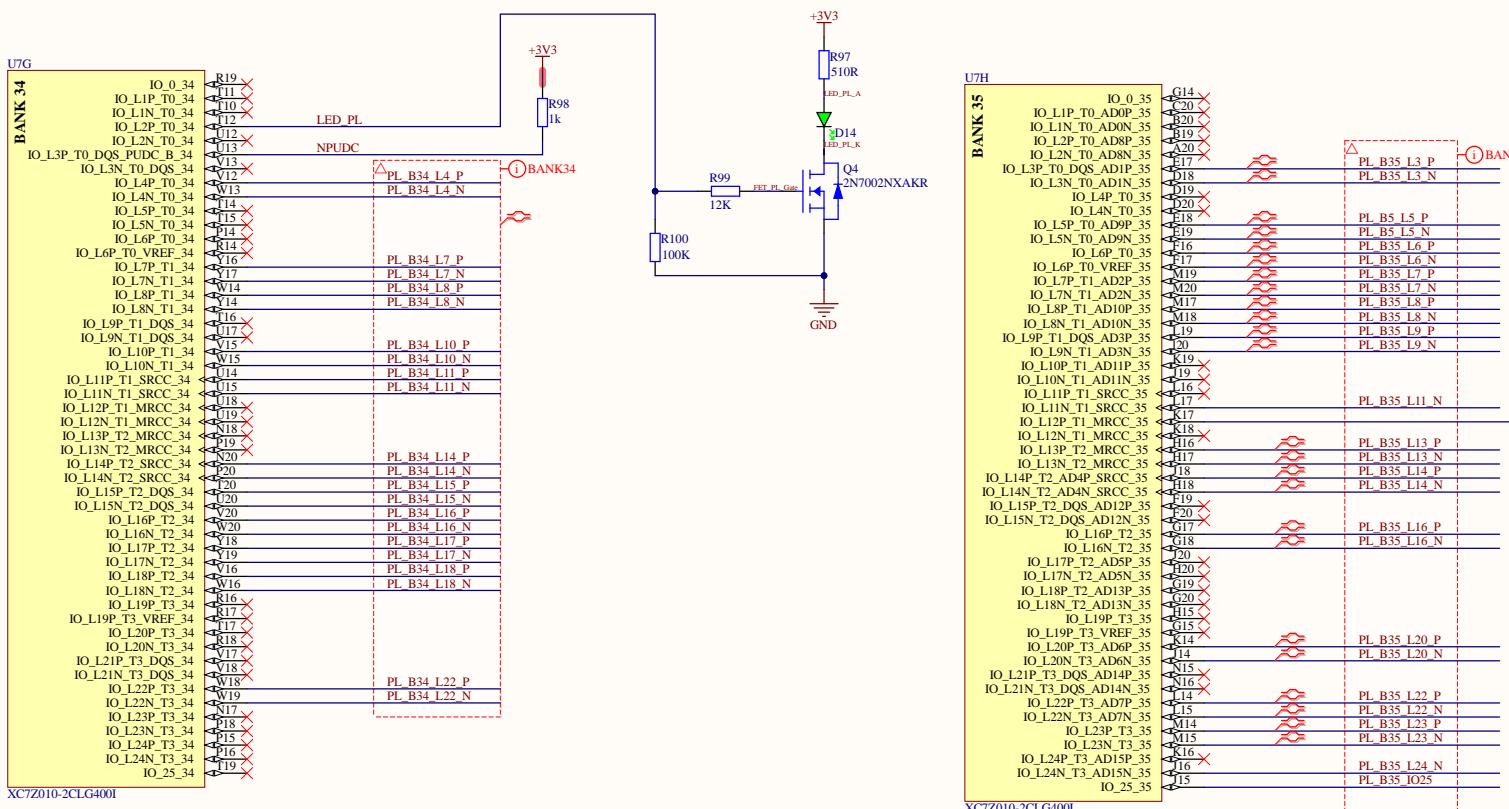


See: "Recommended PCB Routing Guidelines for SHM_eMMC"

https://www.skyhighmemory.com/download/applicationNotes/Recommended_PCB_Routing_Guidelines_for_SHM_eMMC.pdf

Processing system pinout isn't flexible so you have to figure out each pin config

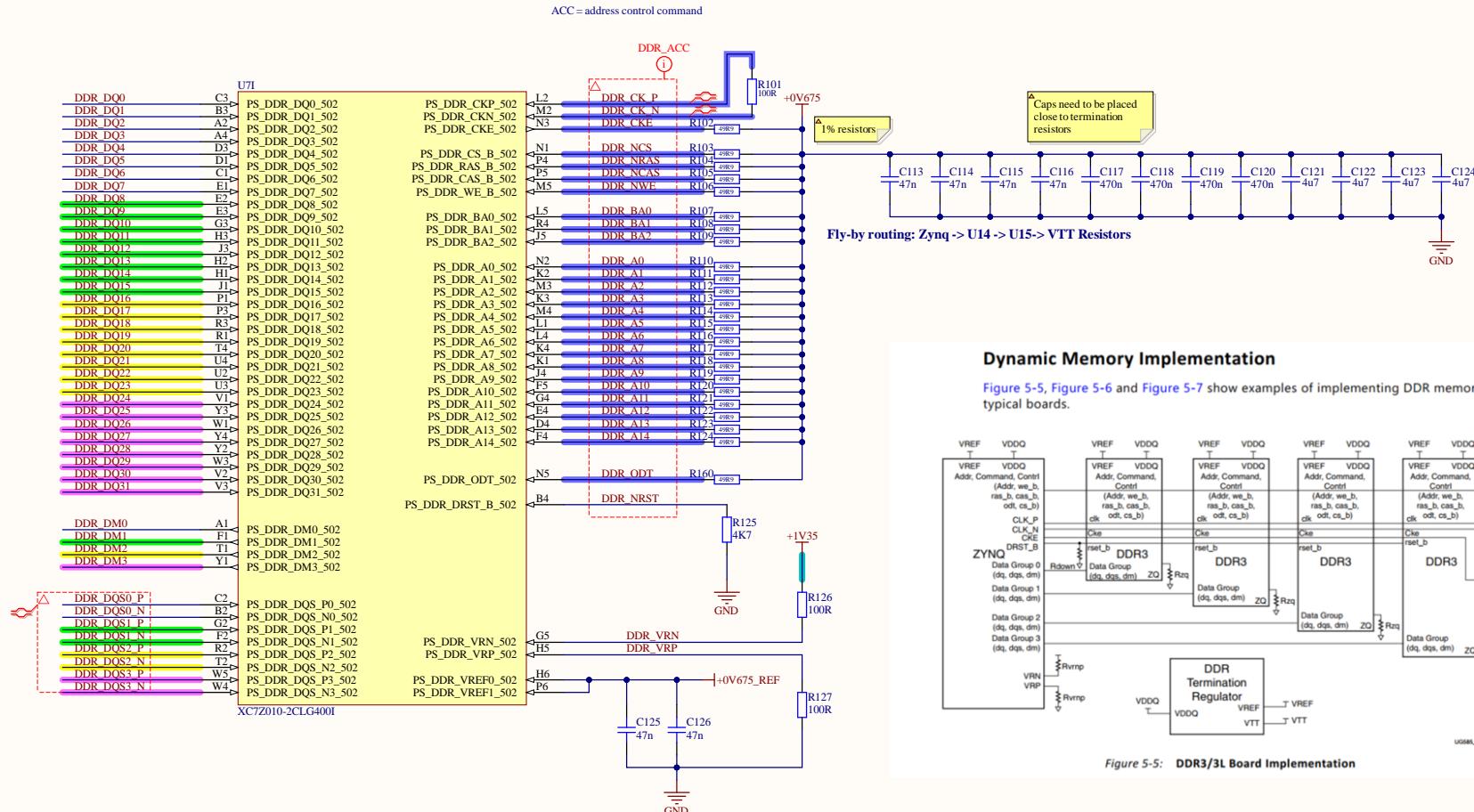
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A
FPGA (PL) pinout is so flexible so assigning pins not a problem

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Zynq DDR Interface & Termination



Dynamic Memory Implementation

Figure 5-5, Figure 5-6 and Figure 5-7 show examples of implementing DDR memory on typical boards.

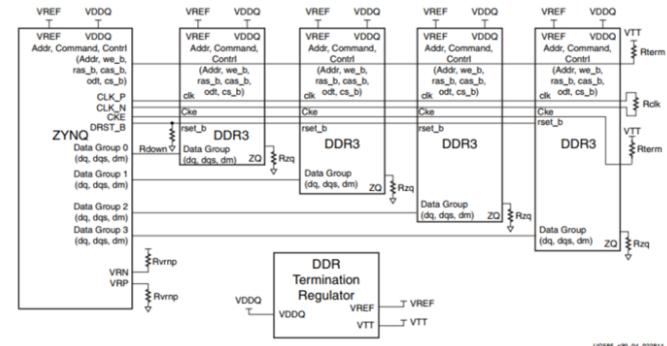
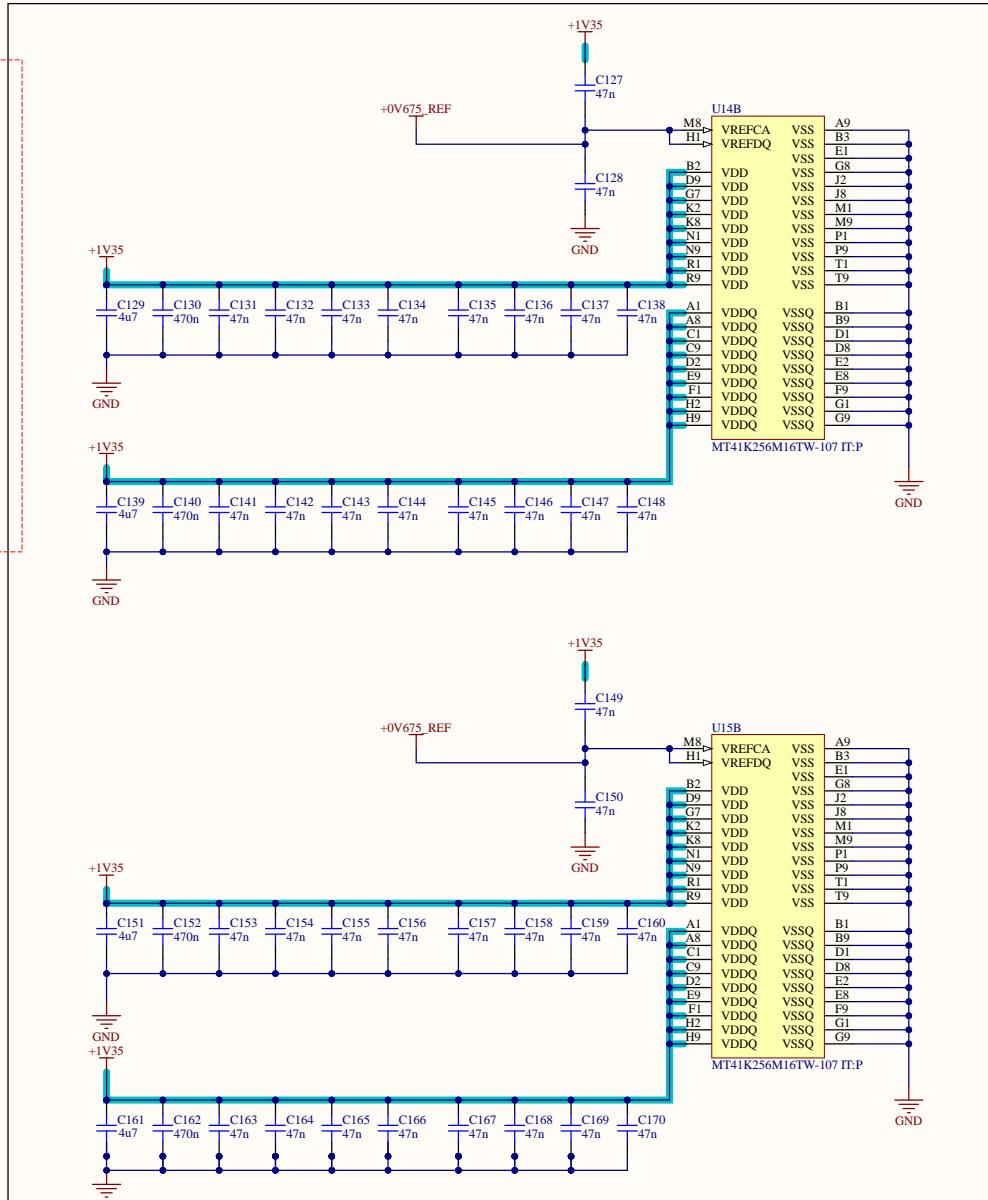
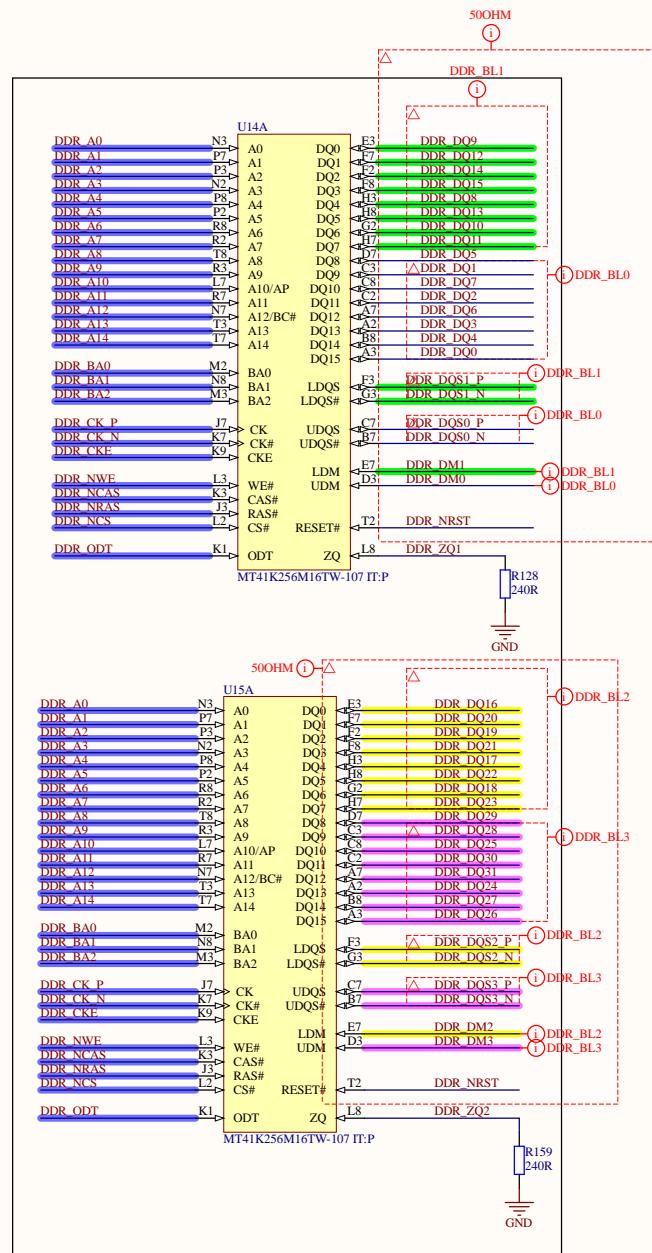


Figure 5-5: DDR3/3L Board Implementation

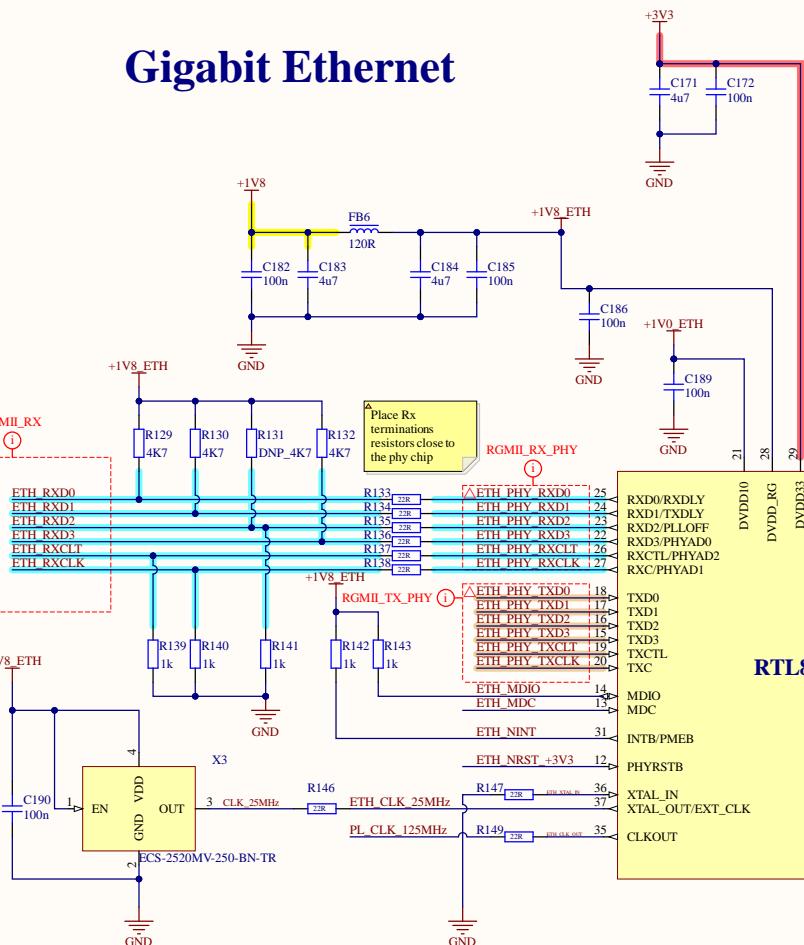
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1GB DDR3L Modules



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Gigabit Ethernet



Ethernet Clock (25 MHz) Ethernet PHY & RJ45 Connector
 $f(CLK) = 25$ MHz for RGMII

Table 9. Power and Ground			
Pin No.	Pin Name	Type	Description
29	DVDD33	P	Digital Power, 3.3V.
28	DVDD_RG	P	Digital I/O Pad Power. When pulling high CFG_EXT [10] during Hardware Configuration (External Power mode), connect this pin to the external power source for 3.3/2.5/1.8/1.5V RGMM I/O.
21	DVDD10	P	Digital Core Power, 1.0V.
11, 40	AVDD33	P	Analog Power, 3.3V.
3, 38	AVDD10	P	Analog Core Power, 1.0V.
41	GND	G	Ground.
			Exposed Pad (E-Pad) is Analog and Digital Ground (see section 11 Mechanical Dimensions, note 54).

Table 2. Clock

Pin No.	Pin Name	Type	Description
36	XTAL_IN	I	25MHz Crystal Input. Connect to GND if an external 25MHz oscillator drives XTAL_OUT/EXT_CLK.
37	XTAL_OUT/E XT_CLK	O	25MHz Crystal Output If a 25MHz oscillator is used, connect XTAL_OUT/EXT_CLK to the oscillator's output (see section 10.3, page 58 for clock source specifications).
35	CLKOUT	O	125/25MHz Reference Clock Generated from Internal PLL. This pin should be kept floating if this clock is not used by MAC.

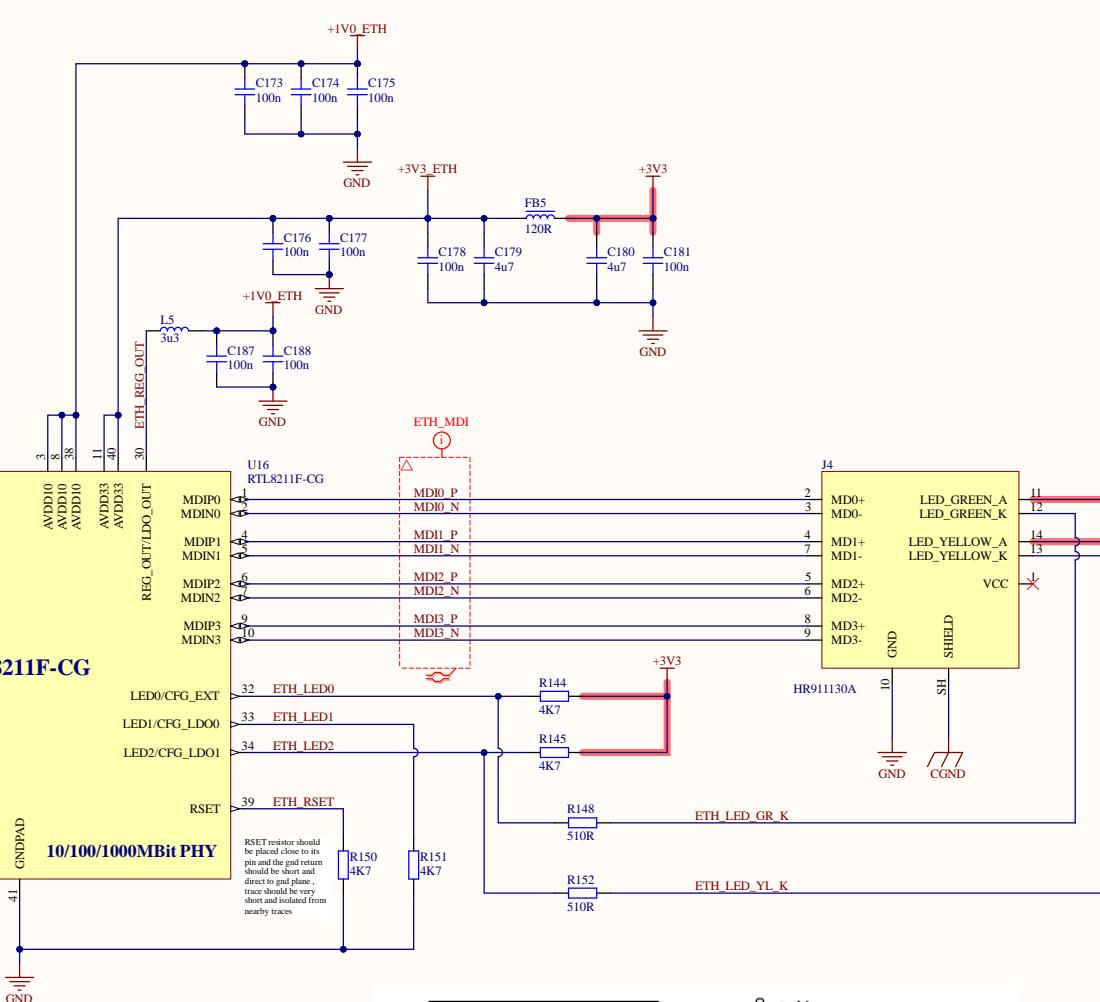
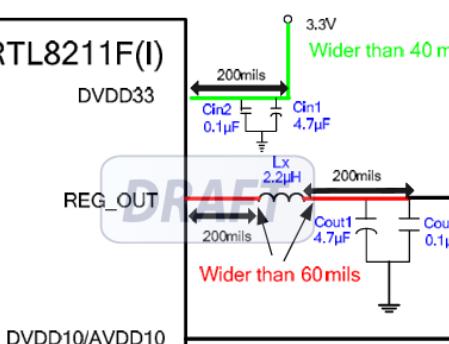


Figure 10. Switching Regulator



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USB 2.0 High-Speed (OTG)

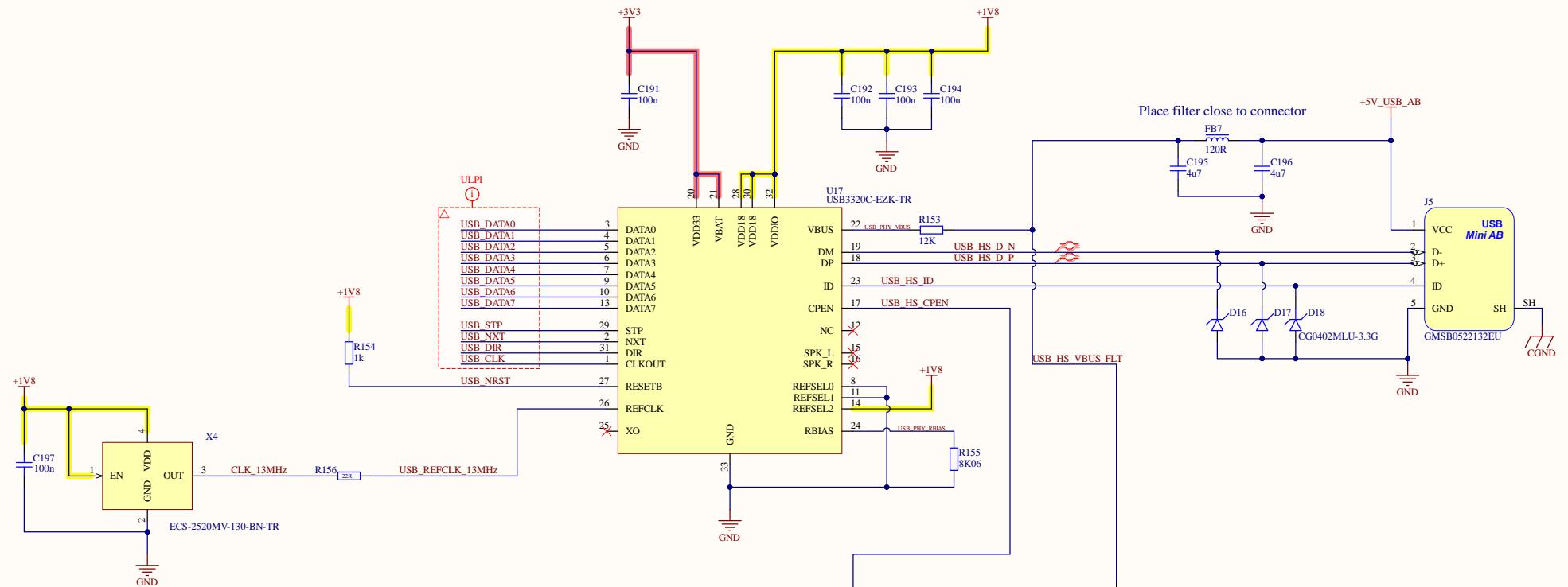
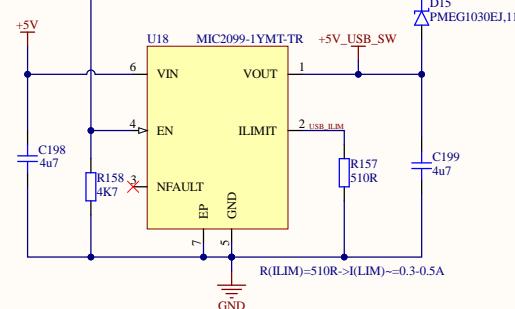
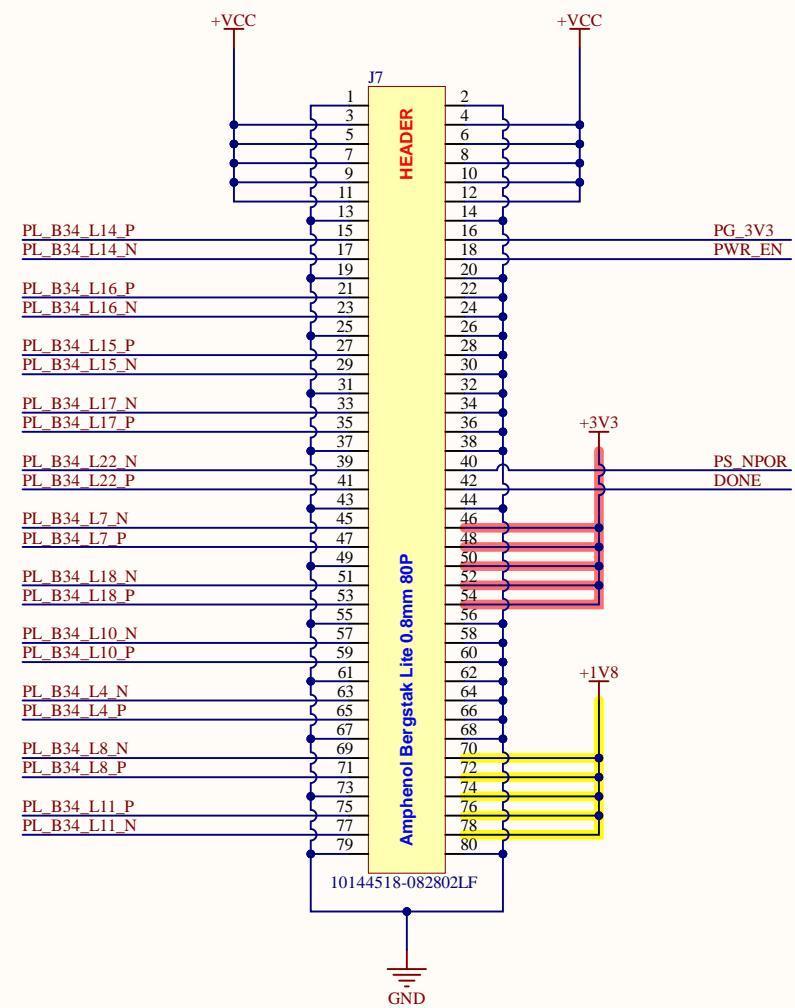
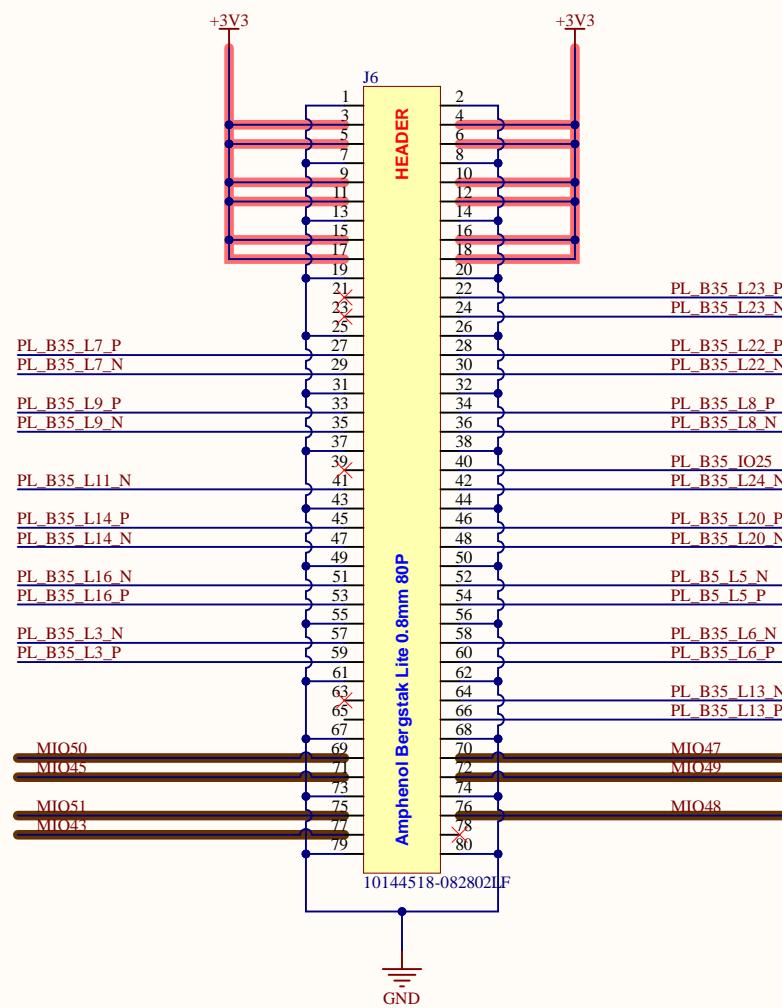


TABLE 5-10: CONFIGURATION TO SELECT REFERENCE CLOCK FREQUENCY

Configuration Pins			Description
REFSEL[2]	REFSEL[1]	REFSEL[0]	Reference Frequency
0	0	0	52 MHz
0	0	1	38.4 MHz
0	1	0	12 MHz
0	1	1	27 MHz
1	0	0	13 MHz
1	0	1	19.2 MHz
1	1	0	26 MHz
1	1	1	24 MHz

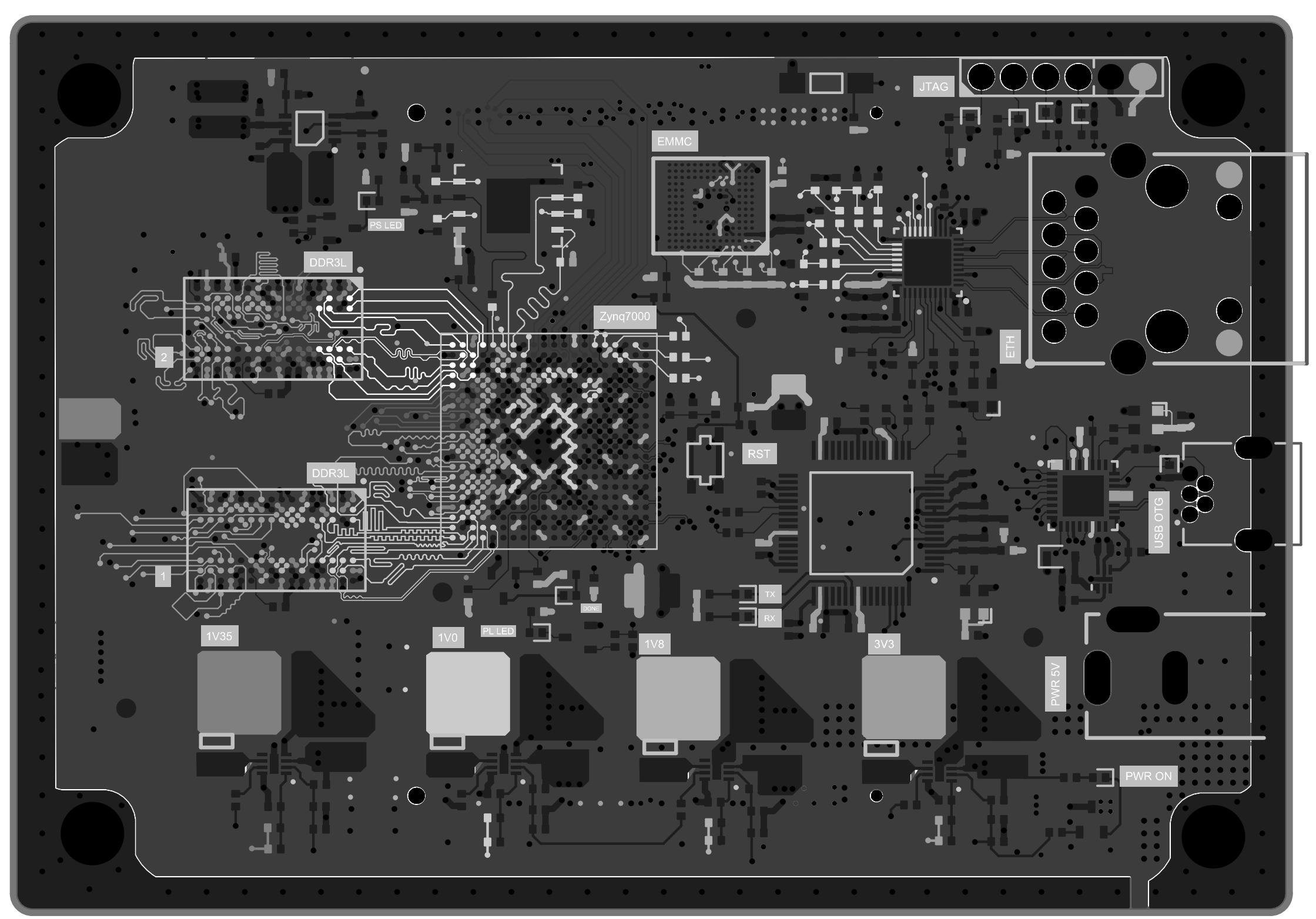


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Board Stack Report