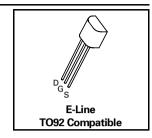
P-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ZVP3306A

ISSUE 2 - MARCH 94

FEATURES

- * 60 Volt V_{DS}
- * $R_{DS(on)} = 14\Omega$



ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V _{DS}	-60	V
Continuous Drain Current at T _{amb} =25°C	I _D	-160	mA
Pulsed Drain Current	I _{DM}	-1.6	А
Gate Source Voltage	V_{GS}	± 20	V
Power Dissipation at T _{amb} =25°C	P _{tot}	625	mW
Operating and Storage Temperature Range	T _j :T _{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated).

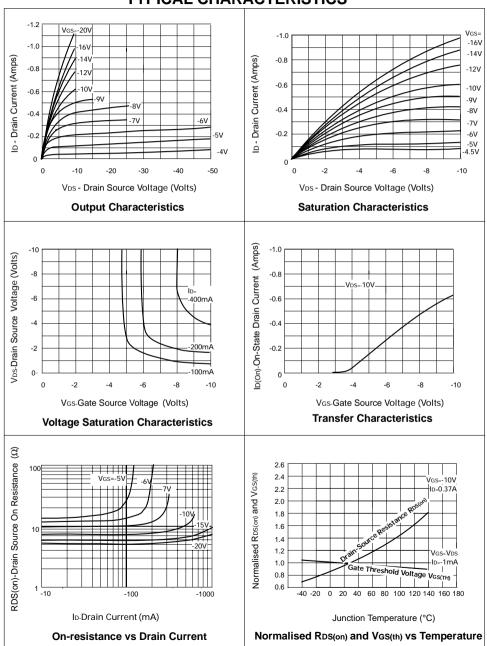
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.	
Drain-Source Breakdown Voltage	BV _{DSS}	-60		V	I _D =-1mA, V _{GS} =0V	
Gate-Source Threshold Voltage	V _{GS(th)}	-1.5	-3.5	V	ID=-1mA, V _{DS} = V _{GS}	
Gate-Body Leakage	I _{GSS}		20	nA	V_{GS} =± 20V, V_{DS} =0V	
Zero Gate Voltage Drain Current	I _{DSS}		-0.5 -50	μ Α μ Α	V _{DS} =-60 V, V _{GS} =0 V _{DS} =-48 V, V _{GS} =0V, T=125°C(2)	
On-State Drain Current(1)	I _{D(on)}	-400		mA	V _{DS} =-18 V, V _{GS} =-10V	
Static Drain-Source On-State Resistance (1)	R _{DS(on)}		14	Ω	V _{GS} =-10V,I _D =-200mA	
Forward Transconductance (1)(2)	g _{fs}	60		mS	V _{DS} =-18V,I _D =-200mA	
Input Capacitance (2)	C _{iss}		50	pF	V _{DS} =-18V, V _{GS} =0V, f=1MHz	
Common Source Output Capacitance (2)	C _{oss}		25	pF		
Reverse Transfer Capacitance (2)	C _{rss}		8	pF		
Turn-On Delay Time (2)(3)	t _{d(on)}		8	ns	V _{DD} ≈-18V, I _D =-200mA	
Rise Time (2)(3)	t _r		8	ns		
Turn-Off Delay Time (2)(3)	t _{d(off)}		8	ns		
Fall Time (2)(3)	t _f		8	ns		

⁽¹⁾ Measured under pulsed conditions. Width=300µs. Duty cycle ≤2%

⁽²⁾ Sample test.

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TYPICAL CHARACTERISTICS



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TYPICAL CHARACTERISTICS

