

## Specifications

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The CALI box is intended to digitize up to 4 sensors, and transmit continuously their digitized signals via an Ethernet network (more precisely under UDP).

It contains 2 cards:

One ADC card, designed by Bernard PAUL<sup>(\*)</sup>.

One FPGA card including a microprocessor communicating via Ethernet : initial design Sébastien L'HENORET with Philippe VENAULT<sup>(\*)</sup>, final setup Michel GROS<sup>(\*)</sup>.

Production: Didier JOURDE.

Project manager: Michel GROS (michel.gros@cea.fr).

### **1. ADC card: 4 channels**

- For each channel:
  - 16 bits ADC polarized at  $\pm 1,25V$ ;
  - Programmable gain:
    - x1, for input  $\pm 1,25V$  (corresponding to  $38,15 \mu V/ADU$ ),
    - x1.5, for input  $\pm 0,833V$  (corresponding to  $25,43 \mu V/ADU$ );
  - Sampling at 10 MHz;
  - Anti-aliasing filter, resulting in 5MHz as the best signal sampling frequency;
  - Single or differential inputs;
  - AC/DC input (jumpers selection);
  - Gain before digitization: x1, x4/3, x2, x4 (jumpers selection);
- External clock outputs and input for the time synchronization between several boxes (not yet operational).

### **2. FPGA card: a commercial Xilinx mezzanine**

- Large FPGA including a PPC emulation;
- Programming language: VHDL (pure FPGA) and C (PPC emulation);
- Communication:
  - 1 serial port RS232;
  - 1 Ethernet port RJ45;
  - 1 USB port (not programmed);
  - Control writes under TCP, Data readout under UDP;
- Power supply: 5V DC;
- 4 front LED.

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## Performances

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- Throughput: 320Mbits/s (@ 5MS/s) ;
- IP address: 192.168.2.x (suited to a private acquisition network); 169.254.123.x is also available;
- Selection of the ADC data to be transmitted (1 to 4 of the 4 ADCs);
- Selection of the data rate:
  - Fundamental clock: 100 MHz;
  - Sampling rate: nearest from 10 MHz as possible (anti-aliasing filter);\
  - Completed by a smoothing by a power of 2.
  - Example: goal = 1 MHz:
    - The sampling divider is set to 12 and the smoothing factor is set to 8;
    - This gives a data rate of 100/96 MHz;
    - The combination is to be computed by the readout software.
- Noise:
  - Less than 1 ADU at 1 MHz;
  - Varies as the square root of the data rate.

## Connectors

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Input #4+  
Input #4-  
Input #3+  
Input #3-  
Synchro  
Synchro  
Synchro  
Synchro  
Input #2+  
Input #2-  
Input #1+  
Input #1-



Power input, 5V DC  
LEDs  
USB Connector  
Ethernet Connector  
RS232 Connector

**Input side** (14 SMA connectors)

**Computer side** (various computer ports)

## Signal Input Jumpers

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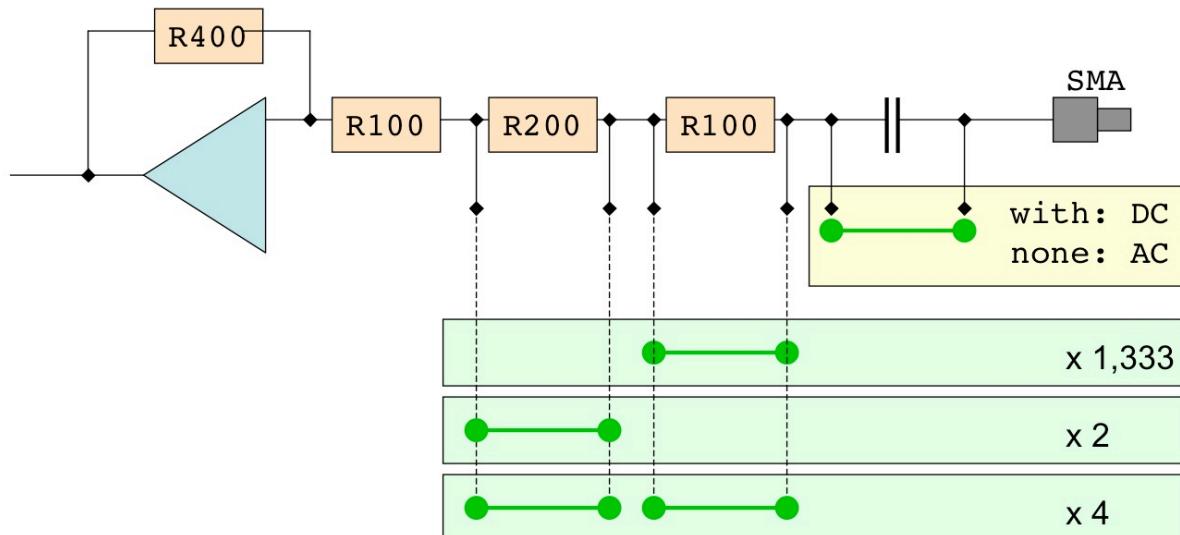
### 1. Definition

For each input connector, there are 3 removable jumpers. With the differential mode, up to 6 jumpers per signal may be necessary.

A first jumper allows choosing between a DC and an AC input.

The 2 other ones allow modifying the input amplifier gain. The actual gain is the ratio between the feedback resistor and the amplifier input resistor. The available gain values are therefore 1, 4/3, 2 and 4, depending upon the involved resistors.

The rules concerning these jumpers are recalled in the following diagram. A suggestion is to glue a copy of it on one of the box sides.



### 2. Opening and closing the box

For any of these operations, **take a full care of the main power connector**: it is very fragile. Unscrew (as possible) and, above all, **screw it by hand only!**

There is an easiest way to open the box:

- 1) Go to the *computer side* (see page 4) and remove by hand the hexagonal nut which holds the main power connector;

- 2) Remove, with a 5mm wrench, the 2 hexagonal screws that hold the RS232 connector;
- 3) Go to the *input side* (see page 4) and remove the 4 cruciform screws that hold the plate;
- 4) You can push on the RS232 connector to extract the cards together with the input side plate remaining fixed by the 14 SMA connectors.

To close the box, do the same in the reverse order, and don't forget to handle the main power nut by hand.

### **3. Connecting in single input mode**

The way to connect the input signal, when it comes in the single (not differential) mode, is the following:

- 1) The signal can be plugged to either only the connector + or the connector -; with the signal plugged to the connector +, an increase of the signal (typically an event) will be seen as a positive event in the software.
- 2) However, the gain jumpers for the unplugged connector have a role in the digitized signal. Here is a table of typical baseline values for the 16 combinations of the gain jumpers, assuming a connection on +:

CALI #7	+, Gain 1	+, Gain 1.33	+, Gain 2	+, Gain 4
-, Gain 1	32000	25000	15000	0
-, Gain 1.33	<b>-25000</b>	32000	22000	<b>5000</b>
-, Gain 2	-15000	<b>-25000</b>	32000	15000
-, Gain 4	0	-5000	<b>-15000</b>	32000

The data are obviously useless whenever the baseline is near to saturation (i.e. 32000), but also, in the case of the CALI #7, when it is at 0. This means that the best combinations of the jumpers for this box are (green colour in this table):

- Gain 1: + with gain 1, - with gain 1.33
- Gain 1.33: + with gain 1.33, - with gain 2
- Gain 2: + with gain 2, - with gain 4
- Gain 4: + with gain 4, - with gain 1.33

For any new box, a check should be done with the requested gain on the input side, by changing the gain on the empty side (the box remaining open during the check!) until the baseline is reasonable.

## Software use (version 8)

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### **1. Network addresses**

The MAC address of the box serial number  $n$  is  $0x000A35000100 + n$ .

The IP configuration depends on the DIP switches (located inside of the box) settings at the card power-on time. Only the switches 1 to 3 are taken into account.

With the settings of 3..1 equal to 000 (highly recommended), the default addresses are pretty well fitted to a local acquisition network:

<b>CALI #n</b>			
<b>Switches 3:1</b>	<b>IP Address</b>	<b>NetMask</b>	<b>GateWay</b>
000	192.168.2.n	255.255.248.0	192.168.0.1

*With the others combinations of the DIP switches, the default addresses are defined as follows:*

<b>CALI #n</b>			
<b>Switches 3:1</b>	<b>IP Address</b>	<b>NetMask</b>	<b>GateWay</b>
001	169.254.123.80+n	255.255.0.0	169.254.123.1
010	132.166.15.131+n	255.255.0.0	132.166.59.254
011	See below	See below	See below

*The DIP switches position “010” (addresses 132.166.15.131+n) fits exclusively to the CEA Saclay’s network.*

*In case of DIP switches set to “011”, the user has to define itself the various addresses (IP, Net mask and Gateway) via a RS232 terminal connected to the board.*

Once the card has booted with any of these configurations, the addresses can be, anyway, dynamically changed by sending commands via the TCP input link (see below).

### **2. Commands to CALI**

Slow control access is made via a TCP link. Commands and responses are text strings. Several registers can be read and written (see below). In case of a read command, the response (register value) is sent via a TCP packet to the host. In case of a wrong command syntax, a TCP packet is sent to the host with “Err0” as the data. For all commands, debug information is sent to the serial port (RS232) of the board.

The readout link is an UDP link. The UDP port can be changed by a specific command (see below).

## 2.1/ Command definition

**Register write:** “w <register address> <data>”

Both parameters are hexadecimal values.

Example: “w 1 64”: write value 0x64 to register 0x1.

**Register read:** “r <register address>”

Both parameters are hexadecimal values.

Example: “r 1”: read value of register 0x1.

**UDP setup :** “p <udp port> <max frames> ”

The port is in decimal, and the maximum frame amount (24 bits wide) is expressed in hexadecimal.

Example: “p 5001 10000” closes the previous UDP connection and initiates a new UDP connection (with the host which sent this command) at the port 5001 for a maximum amount of 65536 frames.

**IP address:** “i <IP Address>”.

The parameter is in decimal form.

Example: “i 132.166.15.140”: change the previous IP address of the board to “132.166.15.140”.

No board reset or board power-up has to be applied for updating parameters.

**Net mask:** “n <Netmask value>”.

The parameter is in decimal form.

Example: “n 255.0.0.0”: change the previous net mask value to “255.0.0.0”.

No board reset or board power-up has to be applied for updating parameters.

**Gateway:** “g <Gateway value>”.

The parameter is in decimal form.

Example: “g 132.166.59.255”: change previous the gateway value to “132.166.59.255”.

No board reset or board power-up has to be applied for updating parameters.

## 2.2/ Registers list

Address	Width	Access	Description	Default
0x0	8	R/W	Acquisition control	0x1
0x1	2	R/W	Start/Stop command	0x0
0x2	24	R/W	Number of UDP frame to send	0xA
0x3	32	R/W	Number of Word in UDP frame	0x3C
0x4	32	R/W	System clock divider (for sampling clock)	0x64
0x5	16	R/W	ADC control	0x0
0x6	8	R/W	Average Sample Number	0x0
0x7	16	R/W	Data for external device control	0x0
0x8	32	R/W	Debug control	0x0
0x9	8	R	Software release	8
0xA to 0xF		R/W	Not used	

## 2.3/ Registers definition

### Register 0x0 : Acquisition control

- Bit 0 : Channel 1 enable
- Bit 1 : Channel 2 enable
- Bit 2 : Channel 3 enable
- Bit 3 : Channel 4 enable
- Bit 4: Master/Slave configuration (Master = ‘0’, Slave = ‘1’). Default value is ‘0’ (Master configuration).
  - In Master configuration,
    - the system runs with the onboard clock;
    - the acquisition start comes from Ethernet TCP commands (see below);
    - The onboard clock is sent to an external differential SMA output, “CKOUT” (in the front panel of the board), to provide its running clock for the slave CALI boards;
    - the master start signal is sent to another differential SMA output, “SYNCIN” (on the front panel of the board also), to allow the slave CALI boards to start the acquisition at the same time.
  - In Slave configuration,
    - the system runs with the master clock, incoming in “CKEXT”;
    - the acquisition start comes from the master signal, incoming in “SYNCIN”.

- Bit 5: Firmware reset. If a firmware reset command is sent, the reset is automatically de-asserted.
- Bit 6: Frame ID reset. This command resets to the value 1 the UDP frame ID to send. If a frame ID reset command is sent, the reset is automatically de-asserted.
- Bit 7: Not used yet

### **Register 0x1 : Start/Stop command**

- Bit 0: Start (Start = ‘1’; Stop = ‘0’). If “Start” is asserted, UDP frames are sent to the host according to the maximum number of frames defined in register 0x2. If “Start” is asserted before the number of UDP frames to send has not been reached, acquisition continues with an UDP frames counter reset to 0.
- Bit 1: Stop (Start = ‘0’; Stop = ‘1’). If “Stop” is asserted, acquisition is stopped even if the number of UDP frames to send has not been reached.

### **Register 0x2 : Number of UDP frame to send**

- Bit 0 to 23: Maximum number of UDP frames to send. When this number is reached, the acquisition is stopped. The acquisition can be stopped also before the number of frames has been reached, by sending “Stop” command (register 0x1) or writing “0” for number of frames into this register.

### **Register 0x3 : Number of Word in UDP frame**

- Bit 0 to 31: Number of ADC word in each UDP frame. This value represents the number of ADC data word (16 bits) in each UDP sent packet, divided by 12 (!?). The default value is 0x3C = 60, which means that  $60 \times 12 = 720$  words (1440 bytes) will be sent by UDP frame. The maximum value is 0x3C=60 (default value) because, up to now, no JUMBO frame is supported by the board. As long as JUMBO frame is not supported, the value should not be greater than the default value (to prevent IP packets from being fragmented). To optimize the Ethernet throughput, the value of this register should not be changed from the default value (0x3C).

### **Register 0x4 : System clock divider (for sampling clock)**

- Bit 0 to 31: Divider value to provide ADC sampling clock from 100 MHz system clock. This value must be even, i.e. 0x64 or 0x65 will lead to the same frequency. The default value is 0x64=100 ( $100\text{MHz}/100 = 1\text{ MHz}$ ). The ADC clock frequency range is from 1 Hz to 50 MHz.

## Register 0x5 : ADC control

- Bit 0 to 3: ADC1 control;
  - Bit 4 to 7: ADC2 control;
  - Bit 8 to 11: ADC3 control;
  - Bit 12 to 15: ADC4 control;

For each ADC:

- Bit 3 : Digital output randomization, active high;
  - Bit 2 : Programmable gain amplifier ('0' → G = 1, Range = 2.5Vpp)  
('1' → G = 1.5, Range = 1.667Vpp);
  - Bit 1 : Internal dither enable, active high;
  - Bit 0 : Power shutdown, active high.

## Register 0x6 : Average Word Number

- Bit 0 to 7: Number of samples to take into account for averaging ADC data. This value must be a power of 2 (2, 4, 8, 16, 32, 64 and 128). Otherwise, the value 0x2 will be taken by the system. Writing a value different from 0x0 into this register enables the average process. If the value is 0x0, no average operation is applied.

### **Register 0x7 : Data for external device control**

- Bit 0 to 15: Data for external device control: This register data is sent to the 16-bits external debug port to control an optional external device. To do this, the switch control value of the debug port (register 0x8) has to be 0x0 to drive this register value to the external debug port.

## Register 0x8 : Debug control

- Bit 0 to 15: Debug port control: This value controls the switch driving several logic internal signals and bus to external 16-pin debug port.
  - Bit 16 to 23 : ADC data in choice
    - 0x0 : Normal Operation : Data from external ADC
    - 0x1: Fixed pattern data: “0x1” for channel 1, “0x2” for channel 2, ...
    - 0x2 : Counter data : data from ADC sampling clock linear counter
  - Bit 24 to 31 : LED control. This value controls a switch to drive different logic internal signals to the 4 front panel LED.

### Register 0x9 : Software release

- Bit 0 to 7: This value corresponds to the processor software version and is only readable. It is fixed at program compilation.

## 3. Read data packet (UDP)

The default amount of data in an UDP packet is fixed to 1456 bytes. This includes 16 bytes for a frame header and 1440 bytes of ADC samples. Note that the number of channels for which there are samples depend on register 0x3 value. However, the header size is fixed.

The table below represents the UDP date packet sent by CALI in acquisition when all channels are activated.

Ethernet/IP/UDP header				
Timestamp (MSB 32 bits of 64)				
Timestamp (LSB 32 bits of 64)				
Frame ID (24 bits)				Soft version (8 bits)
Channel 1 Status	Channel 2 Status	Channel 3 Status	Channel 4 Status	
ADC1 Sample 0	ADC2 Sample 0	ADC3Sample 0	ADC4 Sample 0	
ADC1 Sample 1	ADC2 Sample 1	ADC3 Sample 1	ADC4 Sample 1	
...				
ADC1 Sample 178	ADC2 Sample 178	ADC3 Sample 178	ADC4 Sample 178	
ADC1 Sample 179	ADC2 Sample 179	ADC3 Sample 179	ADC4 Sample 179	

The next table represents the UDP date packet sent by CALI in acquisition when only the first channel is activated.

Ethernet/IP/UDP header				
Timestamp (MSB 32 bits of 64)				
Timestamp (LSB 32 bits of 64)				
Frame ID (24 bits)				Soft Release (8 bits)
Channel 1 Status	Channel 2 Status	Channel 3 Status	Channel 4 Status	
ADC1 Sample 0	ADC1 Sample 1	ADC1Sample 2	ADC1 Sample 3	
ADC1 Sample 4	ADC1 Sample 5	ADC1Sample 6	ADC1 Sample 7	
...				
ADC1 Sample 712	ADC1 Sample 713	ADC1Sample 714	ADC1 Sample 715	
ADC1 Sample 716	ADC1 Sample 717	ADC1Sample 719	ADC1 Sample 720	

The 64-bits Timestamp is the sample counter, and the “Frame ID” is the UDP frame counter.

#### *Channel Status:*

- Bit 0: FIFO Read Error
- Bit 1: FIFO Write Error
- Bit 2: FIFO Full
- Bit 3: FIFO Empty

- Bit 4: FIFO Almost Full
- Bit 5 : FIFO Almost Empty
- Bit 6: ADC Overflow
- Bit 7: Channel Enable

“*FIFO Almost Full*” indicates to the host that no more ADC sample can be taken into account because ADC sampling frequency is too high compared to the Ethernet board link throughput. In this case, the ADC samples read by the host are no more guaranteed to be time coherent. User should decrease the ADC sampling clock frequency or disable channels.

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