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Demonstration of recycling process for GaN substrates using laser slicing technique towards cost reduction of GaN vertical power MOSFETs

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To address the issue of the high cost of GaN substrates, a recycling process for GaN substrates using a laser slicing technique was investigated. The channel properties of lateral MOSFETs and the reverse characteristics of vertical PN diodes, which represent the main components of vertical power devices, exhibited no degradation either before and after laser slicing or due to the overall GaN substrate recycling process. This result indicates that the proposed recycling process is an effective method for reducing the cost of GaN substrates and has the potential to encourage the popularization of GaN vertical power devices. © 2024 The Author(s). Published on behalf of The Japan Society of Applied Physics by IOP Publishing Ltd

Gallium nitride (GaN) is receiving increased attention as a post-silicon (Si) material for reducing the on-resistance of power devices as its critical electric field is ten times higher than Si.[1–3] In particular, GaN vertical devices are recognized as being potentially suitable for high power applications such as in-vehicle inverters that control main motors.[4] To date, numerous device structures such as current aperture vertical electron transistors,[5–7] semipolar gate structure transistors,[8,9] junction FETs,[10–13] fin FETs,[14,15] planar-gate MOSFETs,[16–20] and trench-gate MOSFETs[21–31] have been investigated to experimentally demonstrate the advantage of GaN-based vertical power devices. The results of these experiments are also competitive against silicon carbide (SiC), another post-Si material with high potential. For instance, the MOS channel mobilities of GaN, which are one of the key properties that determine the performance of vertical power devices, are 173–266 $cm^2V^{-1}s^{-1}$.[16,19,26] These values are twice as high as SiC (80–125 $cm^2V^{-1}s^{-1}$).[32–34]

However, reducing device chip cost is one of the critical issues for the popularization of GaN vertical power devices. Although the cost of fabricating GaN devices is expected to be lower than that of SiC, owing to the low process temperature, the high cost of GaN substrates is a crucial issue. To address this issue, a recycling process for GaN substrates using a laser slicing technique has been developed.[35–38]

Figure 1 shows an overview of the GaN substrate recycling process. The thicknesses described in the figure represent the design values of the experiment in this study. The recycling process is as follows. After preparation of a new GaN substrate (No. 1 in Fig. 1), metalorganic vapor phase epitaxy (MOVPE) to grow the desired epitaxial layer structure (No. 2) and device fabrication (No. 3) are implemented in the conventional way. After device fabrication, a laser with a wavelength of 532 nm is irradiated onto the GaN substrate from the N-face and GaN is decomposed into metallic Gallium (Ga) and nitrogen gas at the focal plane by two-photon absorption (No. 4). The depth of the focal plane can be adjusted to obtain thin device chips with a specific thickness. For instance, the focus depth can be set to 65 μm from the surface of the GaN substrate considering the grinding and polishing of the N-face by 15 μm, resulting in 50-μm-thick device chips. After laser irradiation, the GaN substrate is separated into an upper side (thin device chips) and a lower side (GaN substrate without devices) at the GaN decomposition plane (No. 5). The combination of consecutive steps No. 4 and No. 5 is called "laser slicing." The Ga-face of the GaN substrate and the N-faces of the device chips, namely, the separation planes, are ground and polished to obtain smooth surfaces (Nos. 6 and 10). The thin device chips are mounted to packages after metal deposition on the N-face (No. 11). In contrast, chemical mechanical polishing (CMP) is applied to the Ga-face of the GaN substrate (No. 7) for the following hydride vapor phase epitaxy (HVPE) process. In order to make the Ga-face ready for the epitaxial growth, the Ga-face of the GaN substrate after CMP should be atomically flat (RMS $\leqq$ 0.5 nm), which is equivalent to a new substrate. The thickness of the GaN layer grown by HVPE is approximately 90 μm (No. 8), which is designed to restore the original substrate thickness. After further Ga-face CMP (No. 9), the GaN substrate can be considered as a new GaN substrate. It is indispensable to avoid wafer cracks for the success of the recycling process. To avoid wafer cracks, the suppression of the wafer warp caused by thinning wafer thickness is necessary. In particular, the amount of Ga-face grinding and polishing after separation should be minimized.

Tanaka et al. has reported that GaN high electron mobility transistors exhibit similar electrical properties before and after laser slicing to a thickness of 50 μm[35] and that a 8-μm-thick epitaxial layer could be successfully grown on the GaN substrate after laser slicing.[36] However, the electrical properties of the devices on a recycled wafer, which are essential to demonstrate the recyclability of a GaN substrate, have yet to be investigated.

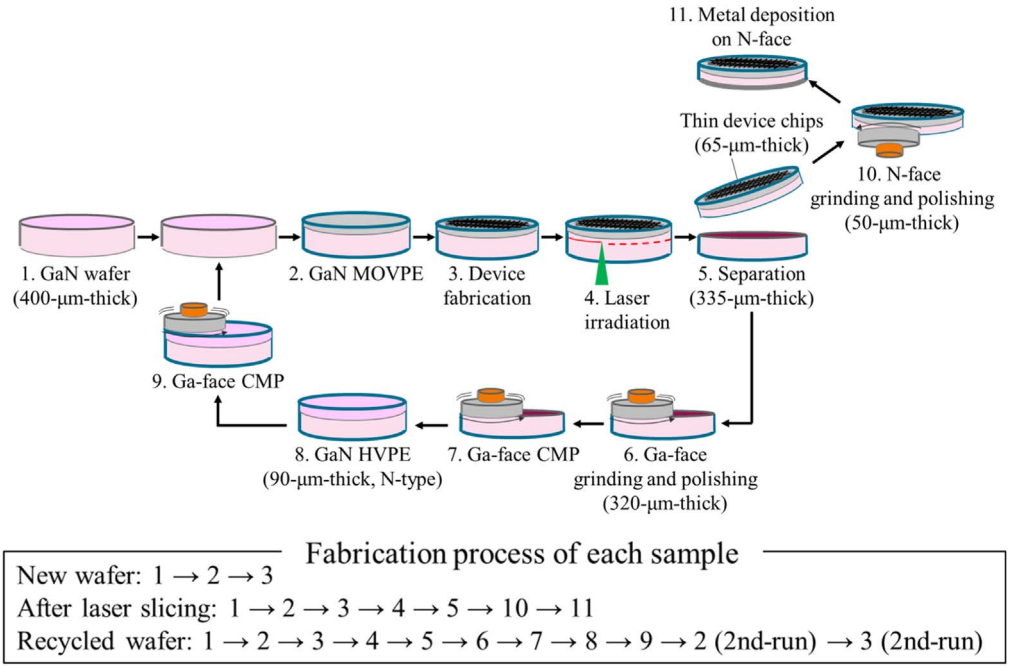

Fig. 1. Overview of the GaN substrate recycling process and the fabrication process of each sample: new wafer (before laser slicing), after laser slicing, and recycled wafer.

Before applying this method to vertical power devices, the effects of the laser slicing on the MOS channel and vertical PN junction structures must be investigated. This study examined the feasibility of this recycling process with vertical power devices by fabricating lateral MOSFETs and vertical PN diodes. First, the impact of the laser slicing process was investigated by comparing the electrical properties before and after laser slicing of a new wafer. Second, the feasibility of the overall GaN substrate recycling process was verified by comparing the electrical properties of new and recycled wafers.

Figure 2 shows cross-sections of the fabricated lateral MOSFET and vertical PN diode. These two structures were fabricated on the same wafer. The fabrication process is as follows. The layered structure on the 2-inch n^+-GaN substrate consisting of a 4 μm thick n-type drift layer and a 2 μm thick p-type body layer grown by MOVPE with designed doping concentrations of $1 \times 10^{17}\,cm^{-3}$ and $5 \times 10^{17}\,cm^{-3}$, respectively. Using a 100 nm thick SiO_2 through capping layer, the n^+ source regions of the lateral MOSFETs were formed by Si ion implantation with a dosage of $3 \times 10^{15}\,cm^{-2}$ and an acceleration energy of 60 keV, and a dosage of $5 \times 10^{14}\,cm^{-2}$ and an acceleration energy of 70 keV, respectively. Activation annealing was then performed at 1050 °C in an N_2 ambient atmosphere for 5 min, which simultaneously activated the p-type body layer. After removing the SiO_2 through the capping layer and the resist patterning mask, negative beveled-mesa structures were fabricated by inductively coupled plasma reactive ion etching as the edge terminations of the vertical PN diodes. The bevel angle and the depth were approximately 6° and 3 μm, respectively. Then, a 100 nm thick SiO_2 film was deposited as the gate oxide layer by plasma CVD and annealed at 800 °C in an N_2 ambient atmosphere for 5 min. A 160 nm thick Ni film was sputtered to form the gate, source, and drain electrodes of the lateral MOSFETs and the anode electrode of the vertical PN diodes simultaneously. Finally, a 500 nm thick Al film was sputtered to form the backside cathode electrode of the vertical PN diodes.

The I_d–V_g and I_g–V_g characteristics of the lateral MOSFETs and the reverse I-V characteristics of the vertical PN diodes were measured. These characteristics correspond

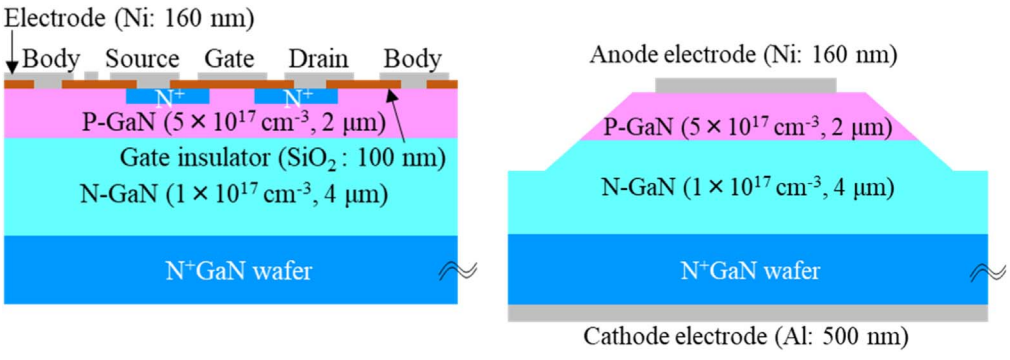

Fig. 2. Cross-sections of the fabricated devices: (a) lateral MOSFET and (b) vertical PN diode.

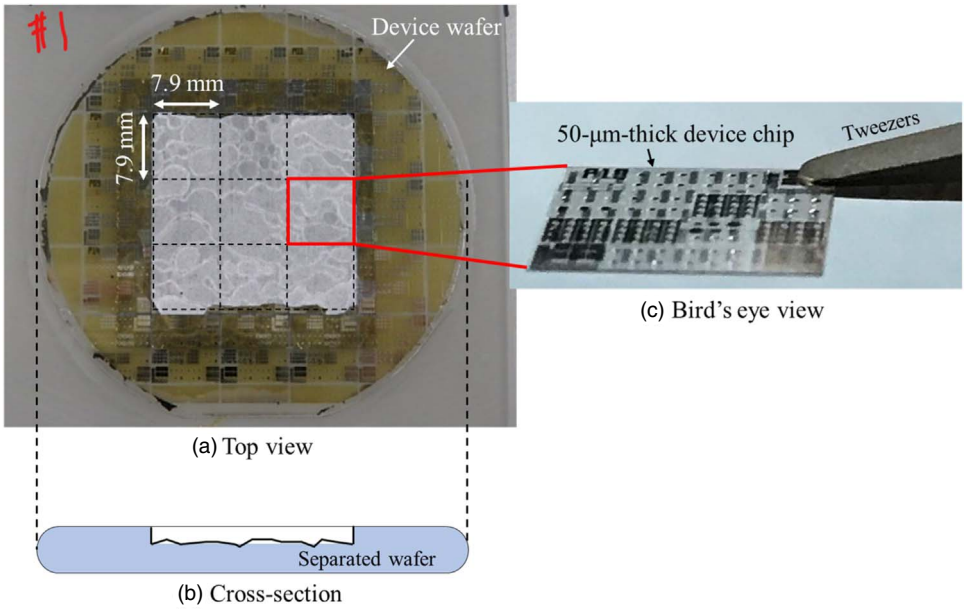

Fig. 3. (a) Top view, (b) cross-section of GaN substrate directly after laser slicing, and (c) bird's eye view of the 50-μm-thick device chip.

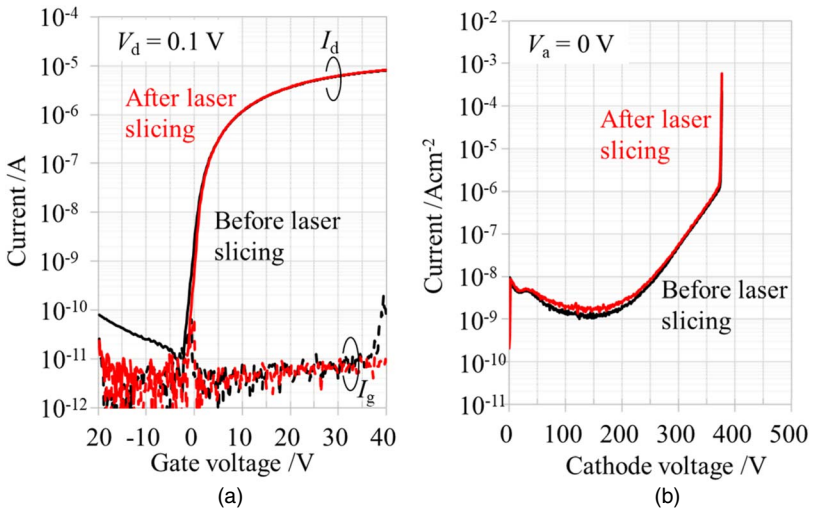

Fig. 4. (a) I_d–V_g and I_g–V_g curves of lateral MOSFET and (b) reverse curves of vertical PN diode before and after laser slicing.

to the on-state and off-state of a vertical power MOSFET, respectively. The characteristics of the lateral MOSFETs were measured under the following conditions: $V_d = 0.1$ V, $V_s = 0$ V, and $V_g = -20$ to 40 V at 300 K. In contrast, the characteristics of the vertical PN diodes were measured under the following conditions: $V_a = 0$ V, $V_c = 0$ V to the voltage when $I_c = 1 \times 10^{-6}$ A at 300 K.

Figure 3 shows a top view and a cross-section of the GaN substrate directly after laser slicing, and a bird's eye view of the 50 μm-thick device chip. The separated area was approximately 23.7 mm square, large enough to obtain nine thin device chips from one substrate in this experiment. The metallic Ga color and the morphology of the nitrogen gas bubble existed on the separated area of the substrate.

Figure 4 shows the I_d–V_g and I_g–V_g curves of a lateral MOSFET and the reverse curves of a vertical PN diode before and after laser slicing. The fabrication process of the samples before (new wafer) and after laser slicing are described in the lower part of Fig. 1. It should be noted that the curves were measured from the same lateral MOSFET and vertical PN diode before and after laser slicing. The black lines and the red lines represent the curves before and after laser slicing, respectively. The solid lines and the dashed lines in Fig. 4(a) represent the I_d–V_g and the I_g–V_g curves, respectively. No apparent changes in characteristics occurred due to laser slicing, indicating that the devices are virtually unaffected by laser slicing, such as due to application of the heat generated by the laser onto the device surface and the stress of the separation process. The leakage current of a vertical PN diode in the voltage range of less than 100 V originated from transient current, i.e., the hole emission current of carbon-related defects (C_N).[39]

Table I shows the averages and standard deviations (σ) of the characteristic values extracted from the measured curves before and after laser slicing. The characteristic values of the lateral MOSFETs were defined as follows. The threshold voltage was defined as the V_g when $I_d = 1 \times 10^{-9}$ A. The drain leakage current was defined as the I_d when $V_g = -15$

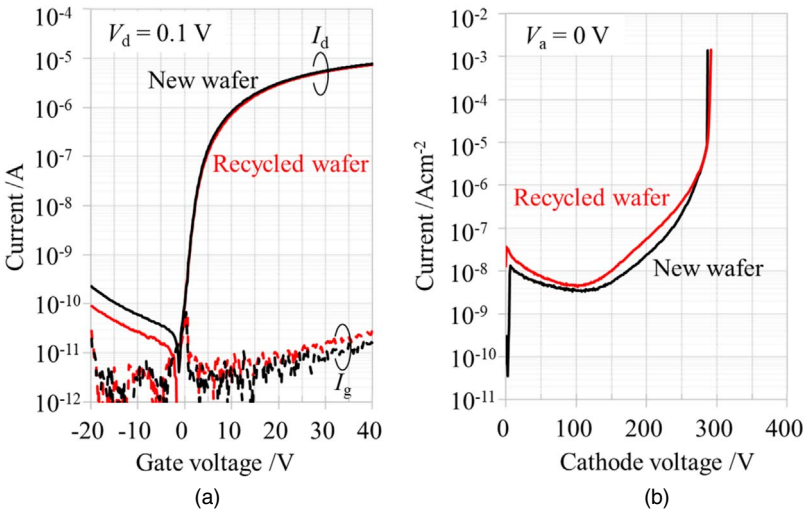

Fig. 5. (a) I_d–V_g and I_g–V_g curves of lateral MOSFETs and (b) reverse curves of vertical PN diodes fabricated on new and recycled wafers.

Table I. Averages and standard deviations (σ) of the characteristic values extracted from the measured curves before and after laser slicing.

Characteristics	Before laser slicing (n = 55) Average	σ	After laser slicing (n = 55) Average	σ
(a) Lateral MOSFETs				
Drain leakage current/A @$V_g = -15$ V	8.8×10^{-11}	3.6×10^{-11}	3.0×10^{-12}	2.0×10^{-12}
Gate leakage current/A @$V_g = 40$ V	1.9×10^{-11}	1.7×10^{-11}	7.7×10^{-12}	2.2×10^{-12}
Threshold voltage/V @$I_d = 1 \times 10^{-9}$ A	−0.1	0.5	0.0	0.8
Channel mobility/cm^{2}V^{-1}s^{-1} @max	73.8	2.3	79.2	4.2
Characteristics	**Before laser slicing (n = 62) Average**	**σ**	**After laser slicing (n = 62) Average**	**σ**
(b) Vertical PN diodes				
Blocking voltage/V @$I_c = 1 \times 10^{-7}$ A	369.9	21.7	367.9	23.0
Leakage current/Acm^{-2} @$V_c = 100$ V	2.0×10^{-9}	1.7×10^{-9}	3.3×10^{-9}	4.7×10^{-9}

V. The gate leakage current was defined as the I_g when $V_g = 40$ V. The channel mobility was calculated as the maximum field-effect mobility obtained from Eq. (1).

$$\mu_{FE} = \frac{\partial I_d}{\partial V_g} \frac{L}{W} \frac{1}{C_{ox}} \frac{1}{V_d}, \quad (1)$$

where, the channel length (L) and channel width (W) were 100 μm, the gate oxide capacitance per unit area (C_{ox}) was 3.5×10^{-8} Fcm^{-2}, and $V_d = 0.1$ V, respectively. For the vertical PN diodes, the blocking voltage (BV) was defined as the V_c when $I_c = 1 \times 10^{-7}$ A, and the leakage current was defined as the I_c when $V_c = 100$ V, respectively. The results show that the characteristics of both devices exhibit no degradation due to laser slicing, and that laser slicing is a stable process capable of separating the upper device chips and lower substrate.

Next, the entire GaN substrate recycling process was verified. The fabrication processes for new and recycled wafers are described in the lower part of Fig. 1. These processes (MOVPE growth as well as the device fabrication process) were conducted simultaneously for both wafers. In other words, the same wafer was not used before and after the recycling process. It should be noted that the wafers were purchased from the same manufacturer.

Figure 5 shows the I_d–V_g and the I_g–V_g curves of the lateral MOSFETs and the reverse curves of the vertical PN diodes fabricated on the new and recycled wafers. Both the lateral MOSFETs and vertical PN diodes exhibited similar characteristics on the new and recycled wafers. The difference in the gate leakages of the lateral MOSFETs before and after the recycling process is considered to be caused by the variation of the quality of the gate insulator. Table II shows the results for the devices on the new and recycled wafers. The results show that the characteristics exhibit no critical degradation after the GaN substrate recycling process, demonstrating that a recycled GaN substrate can be used in the same way as a new substrate.

In summary, this study demonstrated the feasibility of the laser slicing technique to reduce the cost of vertical GaN power devices. Lateral MOSFETs and vertical PN diodes were fabricated as test devices and the effects of laser slicing and the use of recycled wafers on the electrical properties of these devices were investigated. Virtually no differences occurred in electrical characteristics before and after laser slicing, which indicates that laser slicing has no impact on performance, such as due to application of the heat generated by the laser onto the device surface and the stress applied during the separation process. The characteristics of the devices on new and recycled wafers were almost the same, showing that a recycled GaN substrate can be used in the same way as a new substrate. By conducting this recycling process a sufficient number of times, the practical cost of GaN substrates can be dramatically reduced, indicating that this GaN substrate recycling process is a potentially effective method for encouraging the popularization of GaN vertical power devices.

Table II. Averages and standard deviations (σ) of the characteristic values extracted from the measured curves on new and recycled wafers.

Characteristics	New wafers (n = 89)		Recycled wafers (n = 94)	
	Average	σ	Average	σ
	(a) Lateral MOSFETs			
Drain leakage current/A @$V_g = -15$ V	8.4×10^{-11}	3.1×10^{-11}	1.5×10^{-10}	2.9×10^{-10}
Gate leakage current/A @$V_g = 40$ V	3.1×10^{-10}	5.1×10^{-10}	6.9×10^{-11}	6.9×10^{-11}
Threshold voltage/V @$I_d = 1 \times 10^{-9}$ A	0.8	0.9	0.0	0.5
Channel mobility/$cm^2V^{-1}s^{-1}$ @max	76.4	6.1	75.6	4.1
Characteristics	New wafers (n = 177)		Recycled wafers (n = 177)	
	Average	σ	Average	σ
	(b) Vertical PN diodes			
Blocking voltage/V @$I_c = 1 \times 10^{-7}$ A	283.7	16.2	283.0	15.8
Leakage current/Acm^{-2} @$V_c = 100$ V	3.8×10^{-7}	3.0×10^{-6}	2.8×10^{-7}	2.0×10^{-6}

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