Intra-Operation Dynamic Voltage Scaling

Maximizing Peripheral Performance and Minimizing Energy Consumption

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*Abstract*—Embedded peripherals are often specified with a range of performance characteristics that are affected by their supply voltage. Typically the peripheral supply voltage is static and therefore both power consumption and performance traits are known at design-time. With Intra-Operation Dynamic Power Management (IODVS), we focus on reducing the power consumption of peripheral devices by dynamically modulating supply voltage as they perform specified operations. IODVS is designed to have minimal impact on CPU utilization through the use of peripheral power profiles (PPP) that designate an ideal voltage on a per-state basis. Any peripheral operation seamlessly flows through the pre-determined states and the device driver modulates the supply voltage upon each transition. IODVS is unique in that during high-performance states such as data-transmission, peripherals can have the high supply voltage they demand. Likewise, during low-performance states such as mandatory delays, the system can decrease domain voltage thus reducing power consumption without affecting performance or correctness. We demonstrate this method on various common peripherals and have found energy savings of up to 40%.

Keywords—DVS; DPM

# Introduction

Consider an embedded system where the supply voltage to an application MCU is decoupled from the supply voltage of the peripherals that it is controlling. This is becoming more common as modern MCU applications take advantage of Dynamic Voltage and Frequency Scaling (DVFS) and, in effect, IODVS is a natural extension of DVFS to the peripheral domain. The same modulation techniques (DAC, PWM, etc.) that a MCU may use to control its own voltage can be used to control peripheral voltages. We have found that energy can be saved by lowering the domain voltage during timeframes where low-performance is allowed such as mandatory wait periods and where the application of traditional DPM techniques would adversely affect operation of either the device or the system.

The Microchip SPI EEPROM [[1](" \l "Mic10)] is a typical peripheral device. A write operation to the device (with an optional write-verification stage) has the following specifications regarding state transitions and timings:

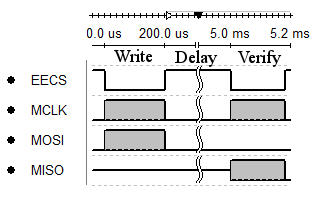


Figure 1: A SPI EEPROM Write / Verify Cycle

Both the read and write operations are voltage/frequency dependent in that the 25AA512 can communicate at 20MHz while above 4.5v, 10MHz while above 3.3v and 2MHz while above 1.8v. It follows that one should communicate between the two domains at matched voltages thereby maximizing data transfer while minimizing energy delay product (EDP). The maximum benefit of IODVS can be realized during the longest portion of the transaction: the delay. By decreasing the supply voltage to 1.8v during the delay state, the energy cost of the delay is decreased by 58%.

The IODVS technique is applicable to many peripherals and this investigation considered the peripherals listed in Figure 1 as a representative sample:

1. Typical External Peripherals

|  |  |  |
| --- | --- | --- |
|  | Honeywell HIH-6130 I2C  Temperature / Humidity Sensor | Vmax: 5.5V  Vmin: 2.3V |
| Microchip MCP 25AA512  512Kbit (64KB) SPI EEPROM | Vmax: 5.5V  Vmin: 1.8V |
| Numonyx M25PX16  16Mbit (2MB) SPI Serial Flash | Vmax: 3.6V  Vmin: 2.3V |
| SwissBit S-200u  512MB (SPI Mode) SD Card | Vmax: 3.6V  Vmin: 2.7V (Operating)  Vmin: 2.0V (Idle/Ready) |

Enabling IODVS requires only an adjustable power supply. An adjustable linear regulator could be used; however in that case one would realize only the benefits of decreased current consumption. This experiment made use of the TPS62240 adjustable switched mode power supply (SMPS) in order to maximize efficiency gains. Peripheral domain voltage modulation is accomplished via DAC output on the STM32F205 MCU signaling into the resistive feedback circuit on the SMPS. In order to measure the results of IODVS, the domain is outfitted with current sense circuitry on both the input to the SMPS and the output to the domain.

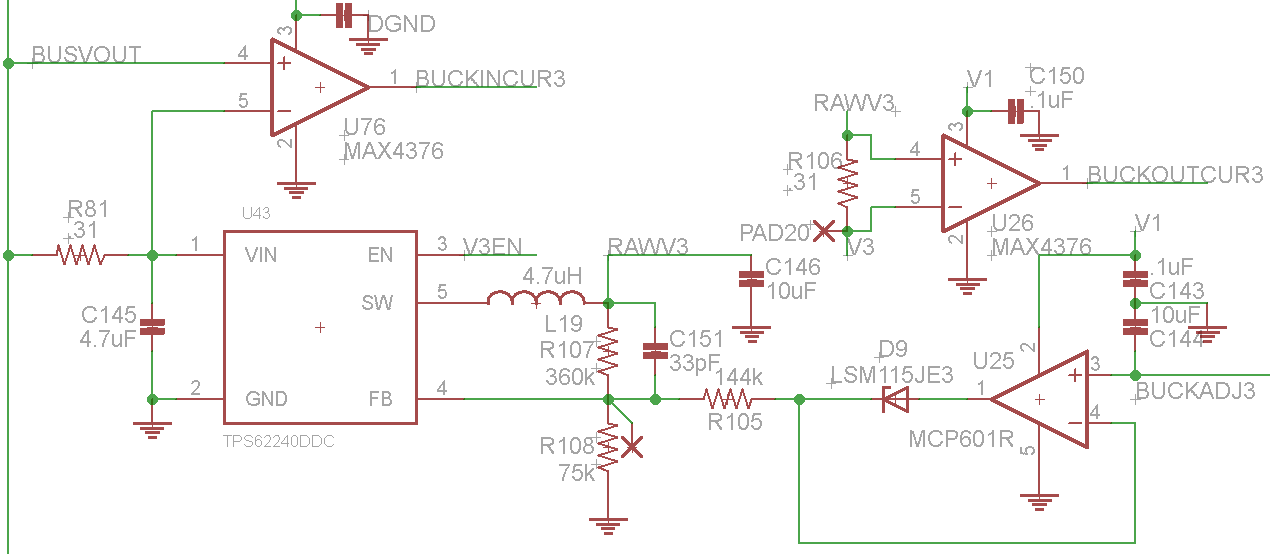


Figure 2: Peripheral Domain SMPS, Control and Current Sense Circuitry

IODVS is thoroughly tested on each of the four sample peripherals by conducting 1000 pseudo-random tests on each device. The output is analyzed and if any particular operation fails then the test is considered a failure and the PPP is increased (voltage slack is decreased) until all tests complete as expected.

# Related Work

Dynamic Power Management (DPM) and Dynamic Voltage Scaling (DVS) implementations seek to maximize energy efficiency in an embedded system when scheduling the use of external peripherals. DPM policies tend to focus on strict power-state relationships [[2](#Bro03)] while DVS policies tend to incorporate a linear power-performance relationship [[3](#Jej04)]. Most DPM implementations focus on optimal scheduling techniques such that peripherals emerge from shutdown just in time for access by tasks. Generally, the approaches to date can be categorized as a combination of either online [[4](#Hui06)] or offline [[5](#Kum08)] and deterministic [[6](#Swa03)] or probabilistic [[7](#Ira02)].

Offline analysis can aid in the implementation of DPM by analyzing the CFG of a task to determine when a peripheral is likely to be accessed [[5](#Kum08)]. Similar data can be realized online by profiling a task and determining which paths lead to a peripheral access [[8](#You10)]. Both methods enhance the accuracy of predictions regarding the optimal peripheral wakeup time. In fact, all methods must evaluate the cost/benefit of peripheral deactivation with respect to the energy savings gleaned versus the time spent reactivating the device when next needed. This equality is commonly known as the breakeven time [[9](#Edw09)].

Some peripherals provide multiple performance/power states. As such, Mode Dependence Graphs were developed in order to accurately quantify the breakeven time between states [[10](#Dex02)]. Approaches have been explored with respect to optimally scheduling devices with multiple power saving states and in systems where multiple tasks share a common resource (inter-task DPM). Naturally, the decrease in voltage margin along with the decrease in available task slack time also decreases the ability to detect and correct errors as they occur [[11](#Dak06)].

The CADVS technique [[12](#Hor11)] is similar to IODVS in that an adjustable regulator is used to operate an embedded system at its minimum voltage requirements. IODVS extends the technique into multiple voltage domains and operates at a much finer granularity. DPM techniques tend to achieve break-even times on the order of 10’s to 100’s of ms, while IODVS is shown to be effective at least 5ms intervals. The technique is different in that we seek to decrease the energy cost of performing peripheral operations as they are performed.

# Assumptions

Create a completely controllable buck power supply via analog input through a DAC. The power source will be supplying voltage for multiple peripherals on a domain separate from the MCU. All digital transactions between the MCU and the peripheral domain will be made at the same voltage. The cost of level translation or isolation is too great to warrant implementation. Also, various sources have cited that the lowest EDP of communication occurs at matched voltage/frequencies. Thus we are left with intra-operation voltage modulation as our means of decreasing energy consumption.

# Methods and Materials

The peripheral power supply (PPS) is outfitted with current sense resistors and amplifiers on both the input to the PPS and the output to the peripheral domain. These signals, along with the input voltage to the PPS and the output voltage from the PPS are fed into the ADC of the STM32F205 microcontroller and sampled at 1MSPS. The MCU has 3 simultaneously sampling ADCs which allows for simultaneous measurement of the output voltage, input current and output current.

Peripheral operations are broken up into states as per an intrinsic state transition diagram. For example, in order to write to EEPROM, the MCU must issue the write command and write the data, wait for a specified delay period and then read the data back in order to verify a correct write. Therefore, the states are delineated as Idle, Writing, Waiting and Verifying.

Each peripheral operation is associated with a specific voltage. For instance, as per our assumptions, data transfers must occur at equal voltages between the domain and MCU. Therefore the Writing and Verifying states voltage must equal that of the MCU (3.3v). This leaves the Idle and Waiting states free for energy optimization. Special care was taken to guarantee that the pins connecting the MCU to peripheral devices were changed to input mode upon transitions into the Idle/Wait states. This ensured that the peripherals were not inadvertently being powered from port pins on the MCU.

The set of states and associated voltages creates a power profile per peripheral. Each test designates a power profile to use. Peripheral memory was tested with random data and across random memory addresses. Tests were run 1000x and the results were averaged. If any test failed to complete the operation successfully then the test-set was considered to have failed.

# Results

All test results were measured entirely in-system using the 3 simultaneously sampling ADC converters. The converters are triggered from a timer overflow using a reload value that allows for a complete buffer fill roughly corresponding to the expected length of the test. For example, the duration of the SDCard test was approximately 15ms with a buffer size of 10240 samples yielded 1.465us per sample (or a sample rate of 683KHz). Upon an ADC trigger, the state of the peripheral is stored synchronously with the sample. Each test data set was retrieve by MATLAB upon completion and is composed of:

* Time Scale
* 10240 12-bit ADC Samples per channel
* Output Voltage
* Input Current
* Output Current
* 10240 State Samples (state of the device: reading/writing/etc)
* Bit Resolution (ADC sample 🡪 Current or Voltage value)

One immediately notices the effects of domain capacitance. The domain voltage changes at a rate corresponding to Equation 1. This is most noticeable as the voltage transitions from high to low because the power supply has a high current drive capability, but no current sink circuitry. This is a benefit to IODVS in that peripheral performance is unaffected by higher-than-necessary voltage in the states of concern.

|  |  |
| --- | --- |
|  | Equation 1 |
|  | Equation 2 |

Likewise, on low to high transitions, the output current of the power supply spikes in order to charge the domain as quickly as possible via Equation 2. This is also beneficial to IODVS in that it allows for very fast transitions from the wait states to the communication states.

## Microchip MCP25AA512 SPI EEPROM

IODVS uses peripheral power profiles (PPP) correlate peripheral voltages with internal state. The standard PPP indicates that all states (writing/waiting/verifying/etc) should have 3.3V applied to the peripheral. The 1.8VIW (1.8V Idle/Wait) profile indicates that the EEPROM should have 1.8V applied during the idle and waiting states and 3.3V applied on all others. Figure 4 provides a comparison of both the standard PPP and the 1.8VIW profiles enabled by IODVS.

The state transition diagram of Figure 3 is known a-priori and is followed throughout the tests illustrated in Figure 4. The test begins with the powered up and having been idle for approximately 100ms. The delay ensures that any other devices on the domain have completed their power-on-reset routines and this effect is discussed further in the future work section.

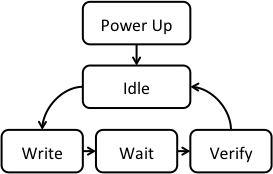


Figure 3: EEPROM Write Procedure

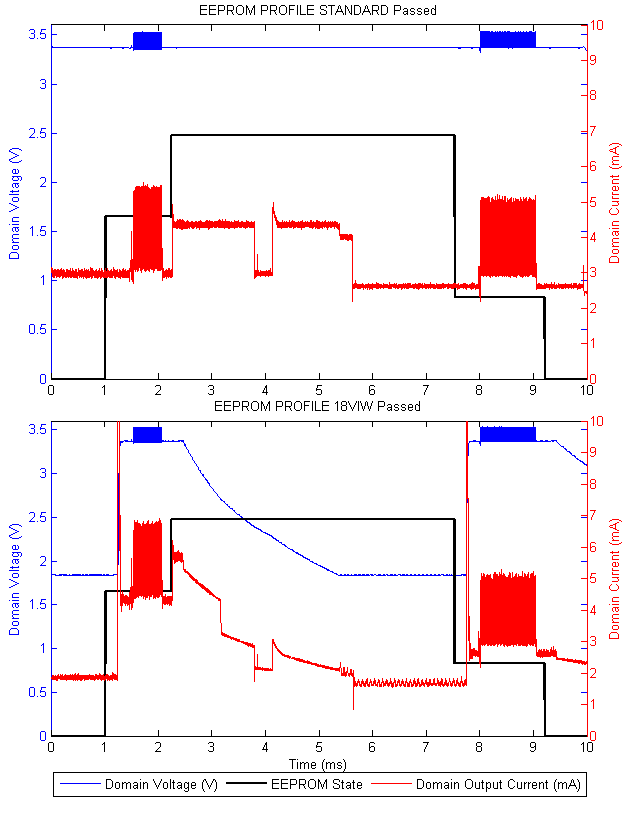


Figure 4: EEPROM Test Results

1. EEPROM Energy Consumption

|  |  |  |  |
| --- | --- | --- | --- |
| State | Static (uJ) | IODVS (uJ) | Delta |
| Idle | 10.24 | 3.49 | -65.91% |
| Write | 13.79 | 17.85 | 29.47% |
| Wait | 64.59 | 33.71 | -47.80% |
| Verify | 17.58 | 17.40 | -1.02% |
| Idle | 8.81 | 7.96 | -9.57% |
| **Total** | **115.02** | **80.43** | **-30.07%** |

The effects of IODVS are immediately noticeable during the Idle and Wait states. The energy consumption during these states decreased 66% and 48% respectively. Energy consumption during the Write state appears to have increased by 30%. This is primarily due to the energy required to charge the domain to 3.3V which is required to complete the transaction. Note that although the current measurement appears to clip the graph in Figure 4, that the current spike was indeed measured to be approximately 15mA and the data was analyzed accordingly.

## Numonyx M25PX16 Serial Flash

Serial flash [[13](#Mic12)] modules have a somewhat more complicated state transition diagram than EEPROM. Serial flash chips can only write zeroes to their memory locations. At a simplistic level, this requirement necessitates a complete erase of a subsector before modifying any memory within it. The M25PX16 supports a minimum of 4KB (sub-sector) erase and a maximum of 256B (page) sequential writes. In order to perform a read-modify-write operation, the transition diagram shown in Figure 5 is followed wherein a 4KB sub-sector is erased and 16 page writes follow.

As the test begins, the chip is in the Idle state; it does not require an initialization routine to function. The specified sub-sector of memory is read into cache and modified with the data to be written while the sub-sector erase operation is ongoing. Note that cross-subsector writes were not evaluated because that would simply require two sequences to occur sequentially. Upon completion of the erase cycle, the modified data are written back to the flash module one page at a time. The writes cause a series of alternating “write-wait” states and the corresponding voltage/state changes are evident in Figure 6.

|  |  |  |  |
| --- | --- | --- | --- |
| State | Static (uJ) | IODVS (uJ) | Delta |
| Idle | 10.73 | 5.63 | -47.58% |
| Read | 71.51 | 72.36 | 1.19% |
| Erase | 2.47 | 2.47 | -0.13% |
| Write\* | 89.48 | 99.16 | 10.82% |
| Wait\* | 574.84 | 365.75 | -36.37% |
| Verify | 83.78 | 52.77 | -37.02% |
| Idle | 38.92 | 38.20 | -1.85% |
| **Total** | **2666.18** | **1614.57** | **-39.44%** |

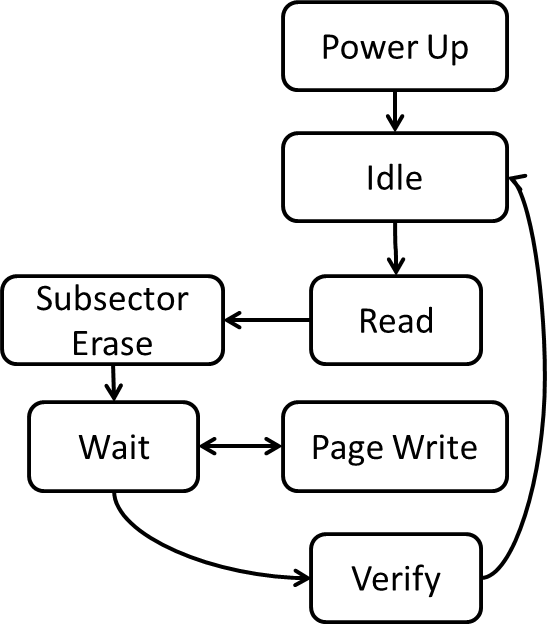


Figure 5: Serial Flash Read-Modify-Write Procedure

Table III summarizes the energy saved through the use of IODVS. As expected, the most significant savings are found in the Idle and Wait states and some small increase is seen in the active states.

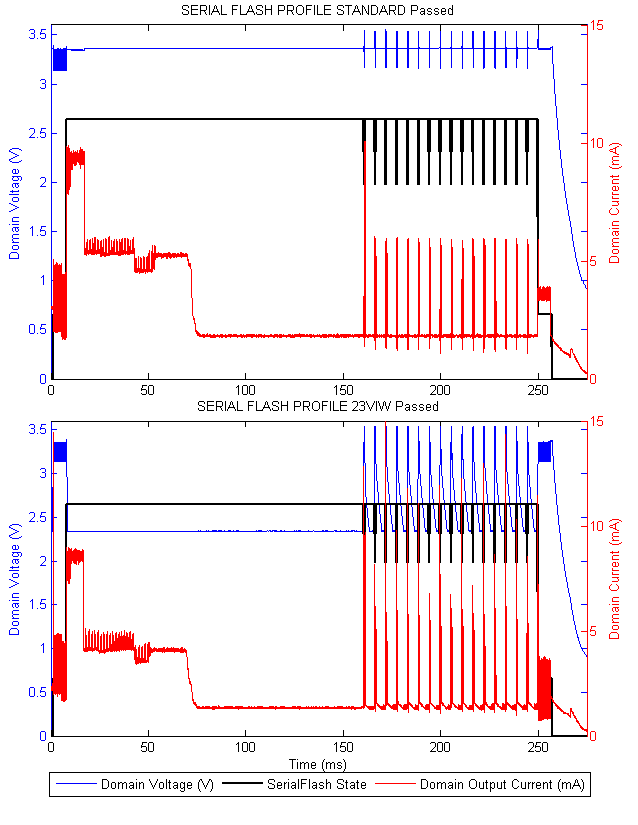


Figure 6: Serial Flash Test Results

1. Serial Flash Test Results

\*Sequential writes and waits combined

## Swissbit S-200U 512MB Micro-SD Memory Card

The SD Card protocol heavily relies on polling the peripheral device. As such, there is not much opportunity to apply IODVS like what was shown for the EEPROM and serial flash cases. However, it is very beneficial to apply IODVS to the SD Card after the device has completed its initialization routine.

An SD Card must be initialized before use, the test fixture communicates with the device via SPI and the initialization process takes approximately 200ms. Therefore, when the device is not in use, it can transition to the low-power 2.7V “Initialized” state, rather than undergoing a complete power-cycle as would be typical with DPM.

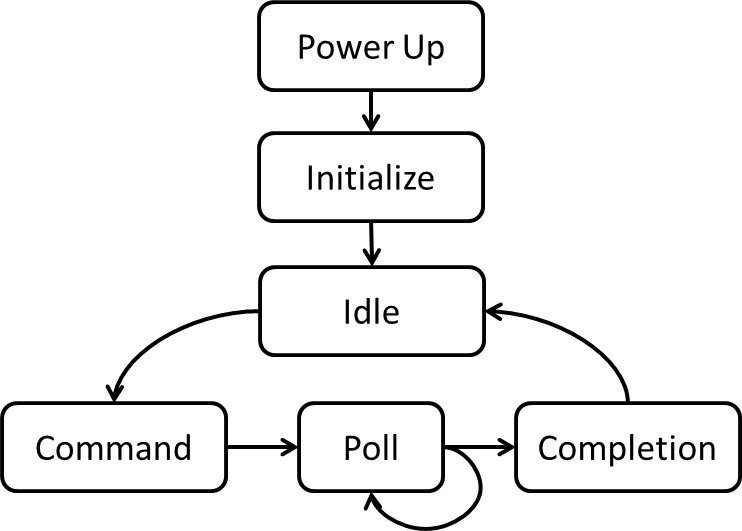
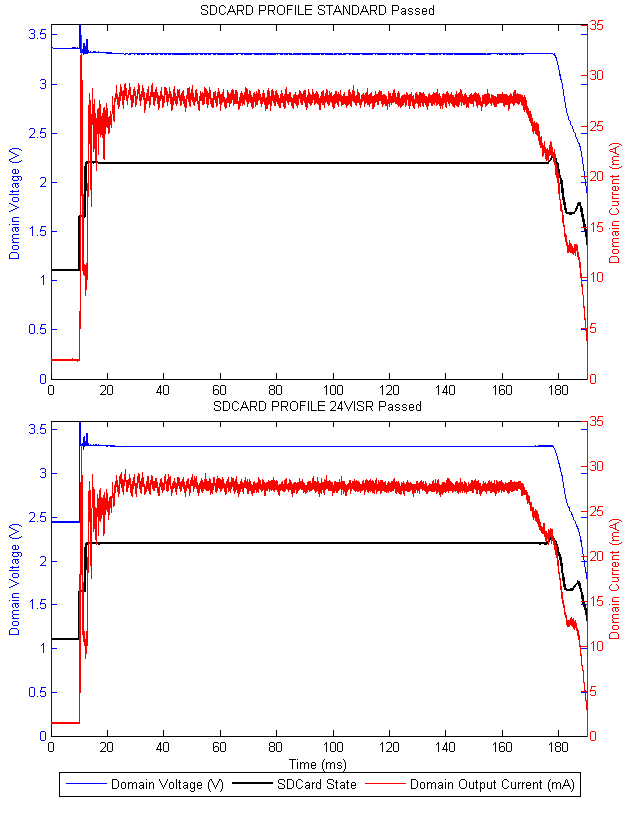


Figure 7: SD Card Measurement Procedure

Thus, the benefits of IODVS with respect to the SD Card are highly dependent on duty cycle. It is shown that the initialized current consumption of the device is reduced by 30% while all other states have no change. Therefore, by using IODVS, the response time of the device is decreased when measured against DPM techniques and the power consumption of the devices is decreased when compared to the static-voltage case.

The SD Card has the highest current consumption of the devices tested and as such causes high droop in domain voltage when active. Decreasing this voltage sag while maintaining or decreasing domain capacitance would increase the efficacy of IODVS and this is further discussed in the future work section.



1. SwissBit SD Card Test Results

|  |  |  |  |
| --- | --- | --- | --- |
| State | Static | IODVS | Delta |
| Idle | 3.10 | 1.16 | -62.52% |
| Write | 3.80 | 4.45 | 17.08% |
| Wait | 18.09 | 8.90 | -50.79% |
| Verify | 4.97 | 6.05 | 21.73% |
| Idle | 2.73 | 2.73 | -0.11% |
| Total | 32.6852 | 23.2879 | -28.75% |

* Use either SI (MKS) or CGS as primary units. (SI units are encouraged.) English units may be used as secondary units (in parentheses). An exception would be the use of English units as identifiers in trade, such as “3.5-inch disk drive”.
* Avoid combining SI and CGS units, such as current in amperes and magnetic field in oersteds. This often leads to confusion because equations do not balance dimensionally. If you must use mixed units, clearly state the units for each quantity that you use in an equation.
* Do not mix complete spellings and abbreviations of units: “Wb/m2” or “webers per square meter”, not “webers/m2”. Spell out units when they appear in text: “. . . a few henries”, not “. . . a few H”.
* Use a zero before decimal points: “0.25”, not “.25”. Use “cm3”, not “cc”. (*bullet list*)

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The equations are an exception to the prescribed specifications of this template. You will need to determine whether or not your equation should be typed using either the Times New Roman or the Symbol font (please no other font). To create multileveled equations, it may be necessary to treat the equation as a graphic and insert it into the text after your paper is styled.

Number equations consecutively. Equation numbers, within parentheses, are to position flush right, as in (1), using a right tab stop. To make your equations more compact, you may use the solidus ( / ), the exp function, or appropriate exponents. Italicize Roman symbols for quantities and variables, but not Greek symbols. Use a long dash rather than a hyphen for a minus sign. Punctuate equations with commas or periods when they are part of a sentence, as in

*a**b* 

Note that the equation is centered using a center tab stop. Be sure that the symbols in your equation have been defined before or immediately following the equation. Use “(1)”, not “Eq. (1)” or “equation (1)”, except at the beginning of a sentence: “Equation (1) is . . .”

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* The subscript for the permeability of vacuum **0, and other common scientific constants, is zero with subscript formatting, not a lowercase letter “o”.
* In American English, commas, semi-/colons, periods, question and exclamation marks are located within quotation marks only when a complete thought or name is cited, such as a title or full quotation. When quotation marks are used, instead of a bold or italic typeface, to highlight a word or phrase, punctuation should appear outside of the quotation marks. A parenthetical phrase or statement at the end of a sentence is punctuated outside of the closing parenthesis (like this). (A parenthetical sentence is punctuated within the parentheses.)
* A graph within a graph is an “inset”, not an “insert”. The word alternatively is preferred to the word “alternately” (unless you really mean something that alternates).
* Do not use the word “essentially” to mean “approximately” or “effectively”.
* In your paper title, if the words “that uses” can accurately replace the word “using”, capitalize the “u”; if not, keep using lower-cased.
* Be aware of the different meanings of the homophones “affect” and “effect”, “complement” and “compliment”, “discreet” and “discrete”, “principal” and “principle”.
* Do not confuse “imply” and “infer”.
* The prefix “non” is not a word; it should be joined to the word it modifies, usually without a hyphen.
* There is no period after the “et” in the Latin abbreviation “et al.”.
* The abbreviation “i.e.” means “that is”, and the abbreviation “e.g.” means “for example”.

An excellent style manual for science writers is [7].

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#### Change number of columns: Select the “Columns” icon from the MS Word Standard toolbar and then select “1 Column” from the selection palette.

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Component heads identify the different components of your paper and are not topically subordinate to each other. Examples include Acknowledgments and References and, for these, the correct style to use is “Heading 5”. Use “figure caption” for your Figure captions, and “table head” for your table title. Run-in heads, such as “Abstract”, will require you to apply a style (in this case, italic) in addition to the style provided by the drop down menu to differentiate the head from the text.

Text heads organize the topics on a relational, hierarchical basis. For example, the paper title is the primary text head because all subsequent material relates and elaborates on this one topic. If there are two or more sub-topics, the next level head (uppercase Roman numerals) should be used and, conversely, if there are not at least two sub-topics, then no subheads should be introduced. Styles named “Heading 1”, “Heading 2”, “Heading 3”, and “Heading 4” are prescribed.

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| Table Head | Table Column Head | | |
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1. Sample of a Table footnote. (*Table footnote*)
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The preferred spelling of the word “acknowledgment” in America is without an “e” after the “g”. Avoid the stilted expression “one of us (R. B. G.) thanks ...”. Instead, try “R. B. G. thanks...”. Put sponsor acknowledgments in the unnumbered footnote on the first page.

##### References

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Number footnotes separately in superscripts. Place the actual footnote at the bottom of the column in which it was cited. Do not put footnotes in the reference list. Use letters for table footnotes.

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For papers published in translation journals, please give the English citation first, followed by the original foreign-language citation [6].

1. G. Eason, B. Noble, and I. N. Sneddon, “On certain integrals of Lipschitz-Hankel type involving products of Bessel functions,” Phil. Trans. Roy. Soc. London, vol. A247, pp. 529–551, April 1955. *(references)*

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To have non-visible rules on your frame, use the MSWord “Format” pull-down menu, select Text Box > Colors and Lines to choose No Fill and No Line.

1. J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68–73.
2. I. S. Jacobs and C. P. Bean, “Fine particles, thin films and exchange anisotropy,” in Magnetism, vol. III, G. T. Rado and H. Suhl, Eds. New York: Academic, 1963, pp. 271–350.
3. K. Elissa, “Title of paper if known,” unpublished.
4. R. Nicole, “Title of paper with only first word capitalized,” J. Name Stand. Abbrev., in press.
5. Y. Yorozu, M. Hirano, K. Oka, and Y. Tagawa, “Electron spectroscopy studies on magneto-optical media and plastic substrate interface,” IEEE Transl. J. Magn. Japan, vol. 2, pp. 740–741, August 1987 [Digests 9th Annual Conf. Magnetics Japan, p. 301, 1982].
6. M. Young, The Technical Writer’s Handbook. Mill Valley, CA: University Science, 1989.