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Piezoelectric-powered wireless sensor system with regenerative transmit mode

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Abstract: This work shows the first, piezoelectric energy harvester powered wireless sensor system, made using commercial off the shelf components, which is capable of continuous operation at an acceleration of 120 mg (1.17 m/s^2) at 77 Hz, which is comparable to a small microwave oven. The authors' results show that a highly deployable system can be realised without the need for custom electronics or devices. By using different operating parameters of the onboard peripheral interface controller (PIC) processor and selectively activating components only when they are required, the system awake time can be increased by over 49 times from that of an unoptimised system. This method also allows the onboard storage to recharge during the awake period and, above a certain acceleration, can lead to continuous operation without the need for a charging sleep period. It can also operate at an acceleration of only 40 mg with a system duty cycle of 5%.

1 Introduction

The size, cost and power consumption of electronic devices has fallen considerably in recent years and has enabled the use of wireless sensors for environmental monitoring. These systems have limited deployability by the use of an onboard battery, which has a finite amount of stored energy and will eventually need to be replaced or recharged. To overcome this, many techniques have been developed to convert ambient environmental energy into electrical energy. This type of energy harvesting produces very low power levels, and so this energy is temporarily stored on a capacitor, or secondary battery, for later transfer to a dependent circuit.

Solar energy is the most established energy harvesting technique and is now a well-developed technology used in small-scale sensor systems [1], domestic power installations and satellites. However, solar cells require a light source and will not work in environments where there is limited or no light. In many environments other forms of energy are available, including vibrational, thermal and radioisotopic sources. In a typical industrial setting, vibrational energy can be abundant and energy harvesters have been developed that are able to convert this kinetic energy into an AC electrical signal. The three methods for this conversion are electromagnetic, electrostatic and piezoelectric conversion, each has been extensively researched and examples of effective converters are reported in the literature [2–4].

Piezoelectric conversion is the most developed of these techniques, with companies now selling energy harvesters which can be used as small-scale power sources. Piezoelectric devices are usually characterised by their relatively large output voltage and small current. This low-output current means that the output needs to be rectified and stored in a battery or capacitor before it is useful in a circuit. This leads to intermittent operation, with periods of inactivity while the voltage on the storage medium is insufficient for circuit operation; hereon, this is referred to as the sleep period. When there is enough stored energy, the circuit can perform a series of operations until the stored energy is depleted to a preset level, at which point the system returns to the sleep mode, this is referred to as the awake period. The duty ratio of the system is determined predominately by the acceleration experienced by the piezoelectric harvester and the predetermined awake/sleep voltages, maximising this ratio is of key importance to the development of an energy harvester-powered system and is the main focus of this paper.

This work will present a reliable, piezoelectric powered, wireless sensor system that can be realised from commercially available components to work at low acceleration. With careful design of the system, it is shown that the awake period can be increased significantly and that above a certain acceleration the system can operate continuously. The design process is presented, which includes a brief discussion on the system electronics, the piezoelectric effect and detailed discussion of the considered regulator topologies. The results section presents comparisons of three rectifier circuits and undertakes an extensive analysis of the energy consumption during different operating modes. Finally, the results show that a base station is able to receive and display sensor data in real time.

2 Design

2.1 System overview

This system comprises a Mide piezoelectric energy harvester, rectification and storage, PIC16F690 micro controller, light

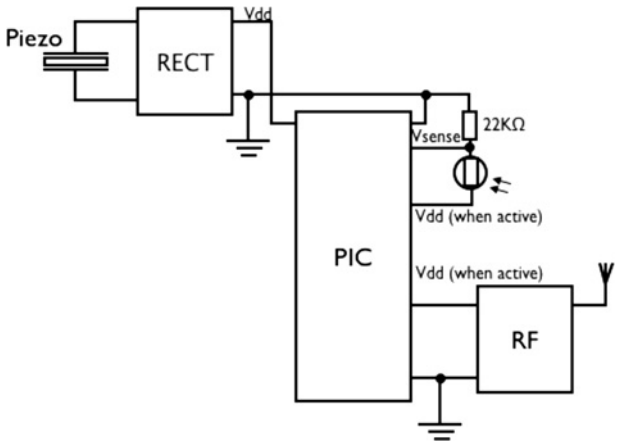

Fig. 1 *System diagram of the final sensor system*

sensor and a 433 MHz amplitude modulation (AM) transmitter. A schematic of the system is shown in Fig. 1.

2.2 Piezoelectric converter

When pressure is exerted on a piezoelectric device, its crystal structure is deformed and an electric field is generated across the material. This electric field is caused by the creation of dipole pairs throughout the material leading to an overall electric field [5]. This effect can be used to generate electrical power if the piezoelectric material is connected to an external load. The output voltage is proportional to the input stress, and so maximising the stress induced is key to maximising the output power.

If the material is formed into a cantilever structure, where one end is clamped and the other is free to move, then vibrations at the clamped end will make the cantilever oscillate [6]. The system is a mechanical filter that has a resonant frequency dependent on its mechanical properties. At resonance, the free end is oscillating with peak displacement and so the strain across the piezoelectric layer is maximised. To maximise the output power this resonant frequency should match the fundamental frequency of the environment in which the system is deployed.

A MIDE V21B Volture energy harvester [7] with a tip mass of 4 g was used as the energy harvester. The data sheet indicated that this mass would result in a resonant frequency of less than 100 Hz, brief experimental validation placed this at 77 Hz. The device is a bi-morph structure with two piezoelectric layers separated by a metallic shim. Both the piezoelectric layers are made of lead zirconate titanate, which is one of the most common piezoelectric materials, because of its high piezoelectric constants. The layers are poled in the same direction and so are used in parallel. Using piezoelectric bi-morphs in parallel, rather than series, reduces the potential output voltage but increases the current output. These devices have a high electromechanical coupling coefficient and a low mechanical Q factor, and thus they have a wider bandwidth than other, similar, devices. This is important when deploying a system as having the widest possible bandwidth will help compensate for fluctuations in the frequency of environmental vibrations.

2.3 Rectification

As the power output from a piezoelectric harvester is small, selecting the correct regulator circuit is important. Typically a four-diode full-wave rectifier, shown in Fig. 2*a*, would be used; however, this circuit reduces the voltage by twice the voltage drop of the diodes used. This topology has been used successfully in rectifying the output from a piezoelectric bimorph for storage on a capacitor [6]. An alternative to this circuit is the voltage doubler, as shown in Fig. 2*b*, which uses two diodes and a small capacitor to double and rectify the voltage output from the energy harvester. While both circuits are capable of rectifying the output from a piezoelectric energy harvester, results will show that the full-wave rectifier has a higher current output, while the doubler has a higher-voltage output.

The full-wave rectifier is well documented [8] but the voltage doubler requires some further explanation. With reference to Fig. 2*b*, D_1 blocks the signal path to ground and so stores the negative half of the signal on the intermediate capacitor C_{in}. When the signal is positive, half a cycle later, the polarity on C_{in} is reversed and the positive signal is summed with the existing voltage on C_{in}. When the addition of these two voltages is greater than $V_{C_{store}} + V_{diode}$, diode D_2 starts conducting and the charge is transferred to C_{store} [9]. It is this stored voltage that will be V_{dd} to the dependent system. Previous modelling by Ferrari *et al.* has shown that the increase in stored voltage for each input cycle is dependent on the ratio of the capacitors C_{store} and C_{in} [10]. To maximise this ratio a 1 mF capacitor was chosen as the storage capacitor, although this is not a super capacitor, which are common in energy harvester powered systems, it does have very low leakage and, because of its relatively small capacitance, will not take as long to charge. By using a smaller capacitance the system will be dependent on careful use of the stored energy during the awake period. The input capacitor was set to 1 μF to maximise the capacitance ratio. In reality this capacitor is not necessary as it is in series with the piezoelectric capacitance, C_p, measured to be 56 nF, measured with a 200 kHz impedance analyser bridge as it shows minimal capacitance variation with frequency. So the effective capacitance will fall to the value of C_p in accordance with (1).

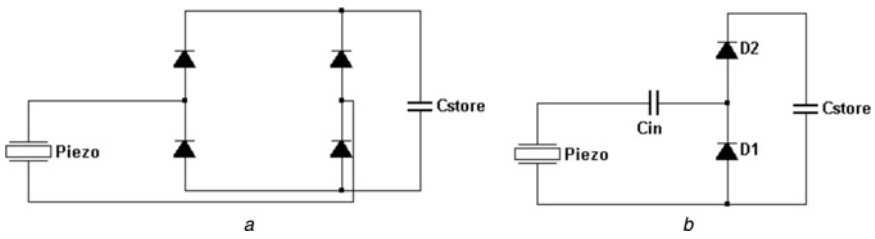

Fig. 2 *Circuit topologies*

a Rectifier
b Multiplier

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The capacitor was left in for testing purposes, as when testing the regulator from a function generator this capacitor is needed as there is no C_p.

$$C_{\text{eff}} = \frac{1}{(1/C_{\text{in}}) + (1/C_p)} \quad (1)$$

The results section compares the performance of the voltage doubler circuit against a full-wave rectifier. The voltage doubler was chosen as the system regulator because of the voltage increase in comparison to the full-wave rectifier circuit. For instance, when the acceleration falls to a point where the energy harvester output is less than 1.4 V the full-wave rectifier will not produce an output, the voltage doubler, however, will still theoretically produce 2.1 V. This slightly increases the bandwidth of the system allowing it to run at frequencies slightly off resonance.

2.4 Sensor system

With such a small output current from the energy harvester, it is important to maximise the overall system efficiency. For instance, there is little need to have communications circuitry active while the system is sampling a sensor, and in some cases it is worth sacrificing speed of operation for the associated current reduction [11]. Hence, careful consideration of the energy requirements of every operation performed by the sensor system is required.

The system electronics have been designed around a PIC microprocessor, which can be placed into a low-power sleep mode to enable to capacitor to charge up. This method relies on the PIC drawing less current in sleep mode than the energy harvester produces, therefore allowing the capacitor to charge [3]. This method has been chosen over a hardware-controlled approach that uses an electronic switch, in the form of a comparator, to isolate the dependent circuitry during capacitor charging.

The comparator circuit has the benefit of hardware-determined voltage thresholds for activating and deactivating the dependent circuitry, and has been shown to provide very stable operation with low sleep mode leakage [10], a trade-off to this however is a loss of deployability. As the switching thresholds are set by the hardware they can only be changed by swapping components, as such, a change in the chosen deployment environment would lead to a system redesign for different operating points. One advantage of the PIC approach is that the operating points can be changed programatically within the embedded software and the circuit elements can be selectively activated and deactivated depending on the functionality required. Both methods have been successfully implemented and discussed previously [3, 9] and so the focus of this paper is on maximising the efficiency during the awake period.

The algorithm shown in Fig. 3 was implemented in the final design using a PIC16F690 as the main system controller. The aim was to minimise the energy burden of the system by using two different clock modes and only activating subsystems when absolutely necessary. There are several internal clock options in the PIC16F690 and each have different current requirements. According to the device data sheet the 31 kHz internal oscillator draws significantly less current than the full-speed 8 MHz one, however, it takes longer to perform operations. Hence, there is a trade-off between the current consumption of a given set of operations and the speed at which they can be executed.

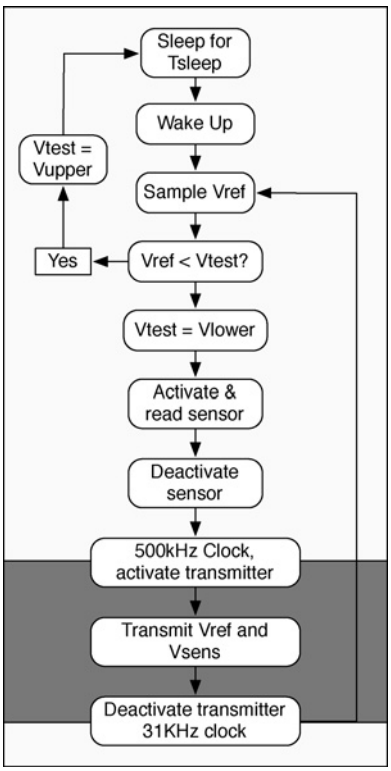

Fig. 3 *Operation algorithm, the light area indicates low-power 31 kHz operation and the dark area indicates 500 kHz operation*

When transmitting, however, there is a minimum required clock frequency to obtain an accurate baud rate for wireless transmission of the sensor data. The system uses a standard 9600 baud rate for data transmission and on the 16F690 the minimum clock frequency that this can be obtained at is 500 kHz. The system needs to switch its internal clock to 500 kHz when transmitting data, faster than this would not speed up the transmission time as there would be more idle clock cycles as the data is transmitted. The 500 kHz clock frequency increases the current consumption of the PIC, but it is considerably less than the 8 MHz full-speed clock.

To determine whether there is sufficient stored energy to perform the required operations, the built-in internal voltage reference of the PIC is used to determine the voltage stored on the capacitor. The stored voltage cannot be sampled directly as it is also the system V_{dd} and so will always return the value 1024, independent of the V_{dd}. Instead, the PICs internal voltage reference, V_{ref}, is sampled as a fraction of V_{dd} and used to determine the stored voltage level, according to the specifications this internal reference is 0.6 V. Once activated the reference is sampled with a 10-bit analogue-to-digital converter and then subtracted from a stored constant. The constants are the upper, V_{upper}, and lower, V_{lower}, operating limits. Prior to subtraction, the two least significant bits are removed from the word to so that the PIC can process the data considerably quicker and more efficiently, leading to a resolution of 8 bits.

As previously mentioned V_{ref} is sampled as a fraction of V_{dd}. If V_{dd} is small then V_{ref} will be large as it takes up a large portion of full range, as V_{dd} changes V_{ref} will change inversely in accordance with (2).

$$V_{\text{refsample}} = \frac{0.6}{V_{dd}} * 256 \quad (2)$$

Depending on whether the PIC is in the awake mode or sleep mode will determine if this sampled value is subtracted from V_{upper} or V_{lower}. If the system is in sleep mode, then the PIC will wake up, sample V_{ref} and subtract the sampled value from V_{upper}. If the result is negative then the turn on threshold has not been reached as V_{dd} is too low, the PIC will return to sleep. Once the result is positive the system will wake up and perform the desired operations.

When the system is in the awake mode it will sample V_{ref} once per cycle and subtract it from V_{lower}. When this subtraction returns a negative result, the system will go back to sleep because V_{dd} has fallen to a point where V_{ref} is once again a large fraction of V_{dd}. Equation (2) has been used to set the values of V_{upper} to 63 and V_{lower} to 75, these equate to 2.43 and 2.04 V, respectively. For system efficiency and processing speed this system is not programmed to process floating points, and so some accuracy is lost in this conversion process, this is primarily a problem at higher operating voltages. At around $V_{dd} = 10$ V a one bit change in the the sampled value of V_{ref} equates to 0.5 V of V_{dd}, this is an unlikely operating voltage but not unrealistic for higher-power sensors. Between the operating points of this system, however, the resolution is 25 values per volt, and this is enough to change the threshold constants to suit a range of environments.

3 Data transmission and receiver

During the awake period V_{dd} decreases, and so any sensor reading needs to be accompanied by knowledge of V_{ref} taken at the same time, otherwise it would not be possible to convert the sensor reading back into a voltage. The data are transmitted with an 433 MHz AM transmitter to a remote base station. This transmitter has no flow control and so transmitting two paired readings, V_{ref} and V_{sense}, and receiving them in the correct order is problematic if the channel is assumed to be imperfect. A transceiver would remove this issue but has a substantially higher energy burden. To reduce the chance of receiving data incorrectly, a series of synchronisation bytes is sent either side of the readings, V_{ref} and V_{sample}. The remote system, running an Objective-C application, disregards data not matching this pattern and so reduces the likelihood of receiving corrupted data. This application presents the received data as a live reading and is able to store the values of V_{dd}, V_{sense} and relative light intensity for later analysis.

4 Results and discussion

4.1 Rectifier

Choosing the correct components to use in the power regulation circuitry is vital to the efficiency of the overall system and maximising the awake time. With this in mind it was decided to compare the performance of standard silicon diodes against silicon carbide Schottky diodes. It has been noted in the literature [12] that components with low-leakage currents is as important a low turn on voltages [3] in order to minimise power loss. Silicon carbide is a wide band gap semiconductor that has a room-temperature intrinsic carrier concentration of 8.1×10^{-9} cm^{-3} compared to that of silicon which is 1.45×10^{10} cm^{-3}, calculated using (3). Hence, silicon carbide diodes have a much lower reverse leakage current than silicon devices; however, they also have a larger forward voltage drop [13].

$$n_i = N_C N_V^{1/2} (\exp^{-E_g/2K_B T}) \tag{3}$$

To test the effect of these diodes in the power rectification, four circuit topologies were fabricated and tested. The topologies were for both silicon and silicon carbide full-wave rectifiers and voltage multipliers. Results from the tests carried out on the diodes and circuits are shown in Table 1. Fig. 4 shows a comparison between the I-V characteristics of a silicon carbide Schottky and a silicon diode. It is clear that the silicon device has a lower turn on voltage, but, as the first column in Table 1 shows, the silicon device has a reverse leakage current 100 times larger than the silicon carbide devices.

Fig. 5 shows the charge profile of a 1 mF capacitor when charged from the rectified output of a Mide piezoelectric energy harvester that is driven with an acceleration of 130 mg(1.27 m/s^2) at resonance. The system was tested with each rectifier topology and the four charge profiles highlight clear differences between not only the diodes but also the circuits. The full-wave rectifier charges the storage capacitor around 1.3 times quicker than either of the multipliers. This is expected because the full-wave rectifier doubles the input frequency. However, the charging is not twice as fast, this is likely to be caused by the difference in diode voltage drop between the topologies. The silicon circuits charge the capacitor faster than the corresponding silicon carbide version, this is probably by the difference in the diode voltage drops. This voltage drop difference reduces the charging current by 4.4 μA for the doubler circuit and 4.8 μA for the rectifier. The data in Fig. 5 show that this has a noticeable effect on the charge rate.

Table 1 Regulator current and power comparison

	Diode leakage at −5 V, nA	I_{OUT}, μA	P_{OUT}, μW	Charge time to 2.5 V, s
Si rectifier	5	42.9	53.4	57.9
SiC rectifier	0.05	38.1	47.1	65.3
Si doubler	5	31.9	39.7	77.9
SiC doubler	0.05	27.9	34.2	90.5

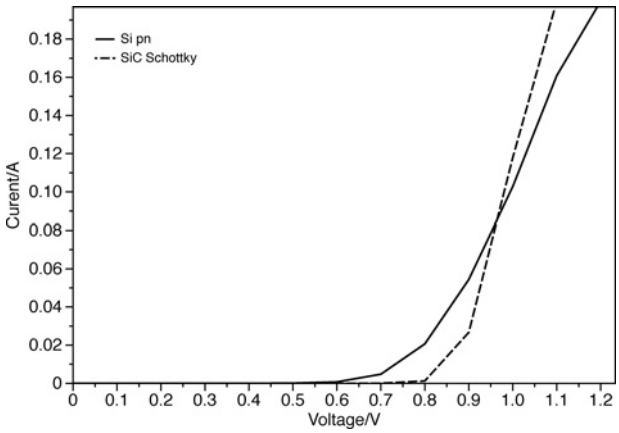

Fig. 4 *Forward IV characteristic comparison between a silicon diode and a silicon carbide Schottky diode*

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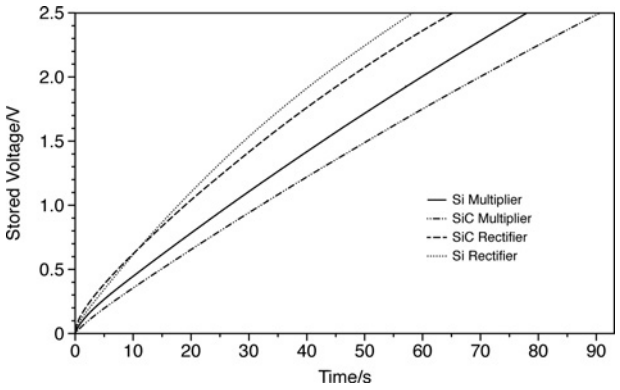

Fig. 5 *1 mF capacitor charge profile at 130 mg (1.27 m/s^2) comparison for Si and SiC full-wave rectifiers and doublers*

The SiC Schottky diode leakage is 100 times lower than that of the silicon diode. However, the slower charge rate offered by the SiC multiplier and the fact that the PIC sleep current is much more than either of the diodes leakage means that in this system there is no gain from using the lower-leakage SiC diodes. When this system is in sleep mode the PIC is still drawing energy from the storage capacitor and as such it is important that the storage element has a net positive input current to stop it being completely depleted, as such using the silicon diodes is a better option. In a system where the electronics is isolated from the storage capacitor during the off-mode, using diodes with the lowest leakage possible is a more suitable option, as it will minimise the leakage from the storage capacitor back into the energy harvester during times of low-energy harvester output.

4.2 Transmission characterisation

Initially the PIC was run with an 8 MHz clock and an input acceleration of 100 mg (0.981 m/s^2). The stored voltage on C_{store} was sampled every 50 ms by an NI DAQ 6033 buffered by a Keithley 6517A electrometer with an input impedance of 200 TΩ. For an 8 MHz clock, the awake period lasted 0.9 s and drew an average current of 0.46 mA. Comparing this to the data shown in Fig. 6, it is clear that a significant improvement is achieved by using two clock frequencies and disabling the transmitter when it is not needed. The average discharge current for the awake period is now 9.3 μA and the average power is reduced to 21 μW. By using two clock frequencies the system's awake time is now 49 times longer than without using two clock frequencies. Given that the total charge time is 20.84 s, the duty ratio of this system has been improved from 0.04 to 3.15. Compared to similar work by Ferrari [14] where the charge and discharge times at 0.5 g input acceleration are 17 s and less than 1 s, respectively, this is a considerable improvement. It is also interesting to note that similar work by Colomer-Farrarons [15], where custom electronics were used, is able to achieve a system with a sleep time of 60 ms and an awake time of 10 ms with an input acceleration of 0.7 g but is unable to have a duty cycle greater than one such as the system presented in this work.

This large increase in duty cycle is a result of the low current draw of the lower-frequency clock operations. The data in Fig. 6 show the stored voltage for a single sleep/awake cycle for the system when the dual-clock system is employed. In the awake period it can be seen that the stored voltage periodically increases before a rapid decrease. The increase in stored voltage is a result of the low-frequency clock drawing less current that the energy harvester is producing, and so leading to a net positive energy flow into the capacitor. This leads to the creation of two distinct operating modes in the awake period, the low-power sample mode and higher-power transmit mode.

Analysing the individual sample/transmit pairs, depicted in Fig. 6 insert, during the awake period in Fig. 6 results in the data shown in Fig. 7. This graph shows the stored voltage change during every fifth sample/transmit cycle, where the voltage data have been normalised to the initial stored voltage at the start of each sample period. It can be seen that as V_{dd} decreases, the current consumed by the system reduces. The current draw from the system in the sample mode is less than the current output from the energy harvester and so the capacitor is able to recharge in this mode. The system is still depleting the stored energy and V_{dd} still crosses V_{lower}, forcing the PIC back into sleep mode. This happens because the energy required for a transmission is never completely balanced by the sample period recharge. However, the data do indicate that there will be a balance point where the energy consumed in the transmission phase will be equalled by the sample period recharge. To test this, several accelerations were used to drive the energy harvester, the results for which are shown in Fig. 8.

Fig. 8 shows the charge and discharge profile for the storage capacitor at three accelerations. At 50 mg the charge time is longer than the discharge time (duty cycle less than 1), at 100 mg the discharge is time is longer than the

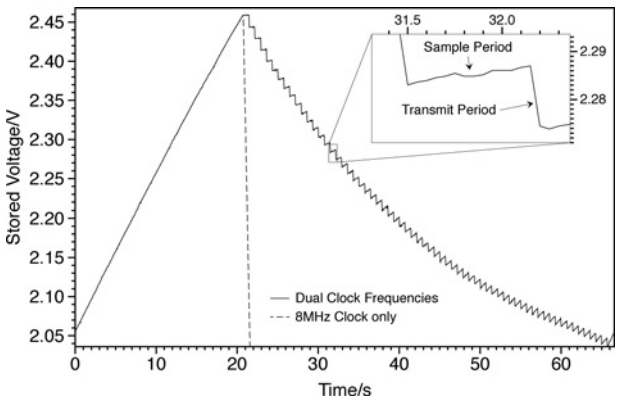

Fig. 6 *Charge/discharge waveform for the stored voltage with dual-clock operation at 100 mg acceleration*

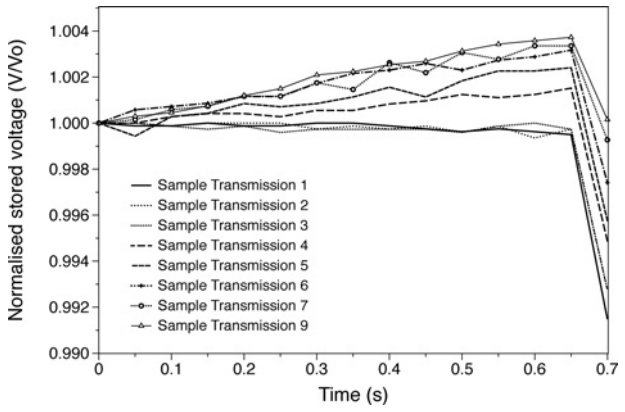

Fig. 7 *Normalised stored voltage for individual sample/transmit cycles across on-state*

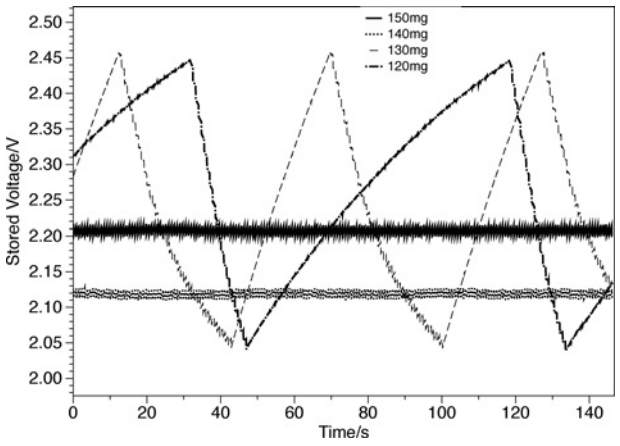

Fig. 8 *Stored voltage change against for multiple acceleration levels*

charge time (duty cycle greater than 1) and at 150 mg the system requires only one charge to activate the system and is then able to operate continuously (duty cycle is ∞). These data shows that as the acceleration increases, the sleep time decreases and the awake time increases to the point where it no longer requires a sleep period. At this point, the 31 kHz clock mode allows the system to fully replenish the energy used during the transmit mode. This causes the system to settle to an average operating voltage which is proportional to the driving acceleration.

This is shown more clearly by the data in Figs. 9 and 10, which show how the input acceleration affects the stored voltage charge and discharge rate. It is clear, and well reported in the literature, that an increase in input vibration acceleration increases the rate of charge. However, unique to this system, the input acceleration also has a marked effect on the discharge characteristic, as shown in Fig. 10. The data fit shows that at around 120 mg the system will stabilise and there will be no net discharge from the storage capacitor, this is supported by the measured discharge rate at accelerations between 120 and 160 mg. At these higher accelerations the system does not require a prolonged sleep period and so the voltage stabilises at a balanced operating point, this is also proportional to the input acceleration as shown in Fig. 11.

In this mode, the system is no longer controlled by the operating points, V_{upper} and V_{lower}, set in the software on the PIC, but instead by the required current consumption of

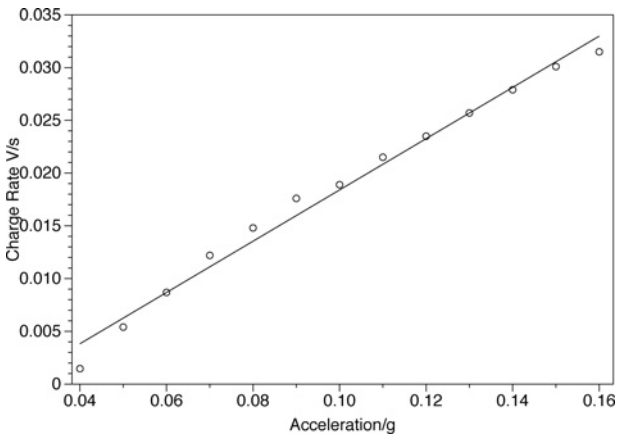

Fig. 9 *Change in stored voltage charge rate with acceleration*

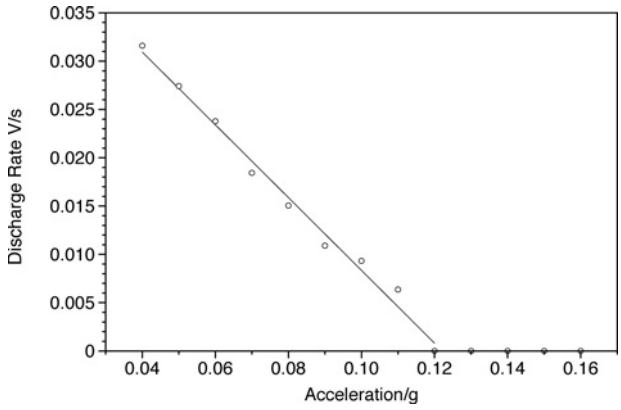

Fig. 10 *Change in stored voltage discharge rate with acceleration*

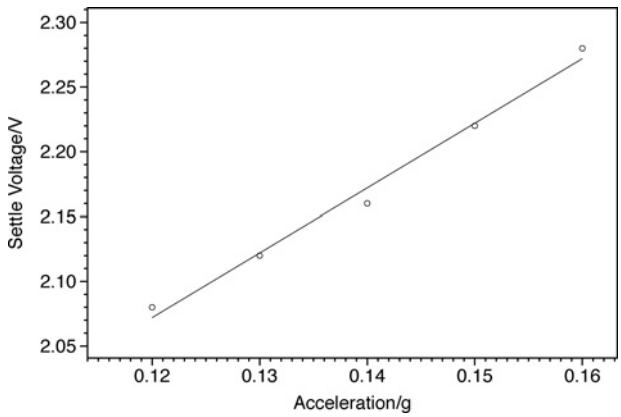

Fig. 11 *Change in continuous operation settle point with acceleration*

the system in the sample and transmit modes. For example, if the ambient vibration level decreases then the output power of the energy harvester also decreases, and so the transmit mode will deplete the stored energy more than the sample mode can replenish it. This leads to a decrease in the average operating point until the current consumption of the two modes balances. Many factors govern this behaviour, not least the current consumption of any subsystems active in either mode, in this instance the system is tested with an light dependant resistor (LDR) in series with a 22 kΩ resistor.

Using the dual-clock method there is a measurable gap between packet transmissions, caused by the time the system takes to carry out its operations in the 31 kHz clock mode. In this mode the gap between readings is 0.65 s, and has no dependence on V_{dd}. This limits the use of this particular system to applications where the measured environmental variable changes slower than 1.4 s, if the minimum Nyquist criterion is used as a limiter. However, in situations where the environment is more volatile, the sample mode clock frequency can be increased to reduce the time taken for readings. This will reduce the awake time because of a higher operating current, but the system will be able to feedback measurements more rapidly.

4.3 Stability test results

Fig. 12 shows the results for a 1.1 h test. In this test four accelerations were used to drive the energy harvester to determine the system stability in response to multiple

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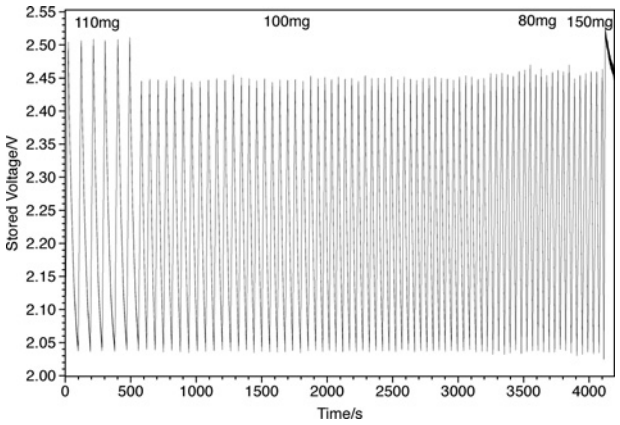

Fig. 12 *V_{Store} variation with time for multiple accelerations across more than 1 hours*

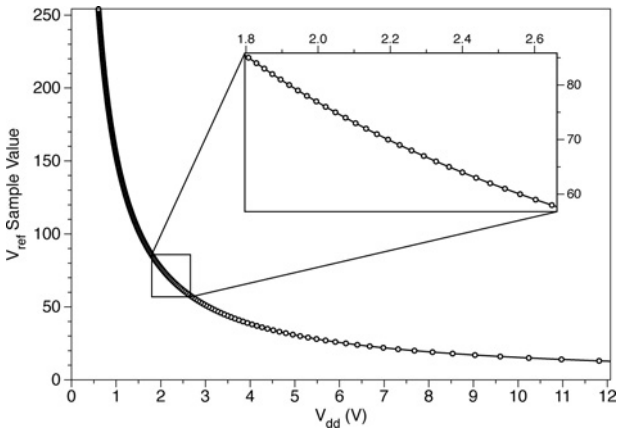

Fig. 14 *V_{ref} sample value as a function of V_{dd}*

accelerations. It is clear that the charge and discharge times are dependent on the input acceleration and from this extended test it can be seen that the system operates in a stable manner between V_{upper} and V_{lower}. The appears to be some instability in the upper-voltage threshold, this is caused by the 4 s sample delay when in sleep mode. If the PIC were to sample V_{ref} just before it crosses V_{upper} then there would be a 4 s delay before the PIC would begin an awake period. During these 4 s the stored voltage increases beyond the threshold, and this continues until the pic samples the stored voltage again. There appears to be little difference between 100 and 80 mg, and this is because the variation in charge and discharge times for these two accelerations leads to the system a change of only 3 s in the system time period. The final acceleration tested is 150 mg, it is clear that the system begins to operate continuously at this acceleration.

4.4 Received data analysis

As previously stated, the receiver software is a command line application that displays the most current reading to a terminal output. If a complete set of data matching the predetermined pattern is found then the value is displayed and saved, otherwise it is discarded. Fig. 13 shows the received data for two discrete test states, in the first period the LDR is covered and in the second it is illuminated by a halogen desk lamp. The received data show that the direct voltage reading decreases during the awake period. However, by compensating for this decrease in V_{dd}, the light level reading, as an intensity, remains constant. The received data are shown as a function of its received number, rather than time, to clearly show that the data are converted and stabilised.

Unlike the directly measured results, shown previously, the received V_{dd} data imply that the stored voltage decays in steps. As discussed in the design phase, the 10-bit digital sample is converted into an 8-bit byte for faster processing, and this means that the maximum resolution is now limited and some accuracy is lost. Equation (2) can be used to determine the system accuracy for a range of operating points and if the sampled V_{ref} value plotted as a function of of V_{dd} Fig. 14 can be produced. This graph shows that as V_{dd} increases the resolution of the system reduces, this is because the relationship between V_{dd} and V_{ref} is non-linear. This does not affect the accuracy of the sensor reading; however, as this has a linear relationship to V_{dd}. This does limit the range of operating points that the system can be set to, however, as the resolution is inversely dependent on V_{dd} and at higher voltages (above 10 V) large changes in V_{dd} equate to only a one bit change in the sampled V_{ref}. Most circuits now require less than 5 V to operate and so this is unlikely to be an issue for the design of wireless sensor nodes based on this approach, especially in this case where V_{dd} is never substantially larger than 2.5 V.

In Fig. 13 the 'light-on' section has fewer data points in than the 'light-off' section. It was first assumed that this was because of the increased current through the LDR circuit having a non-negligible effect on the system current. However, Fig. 15 shows

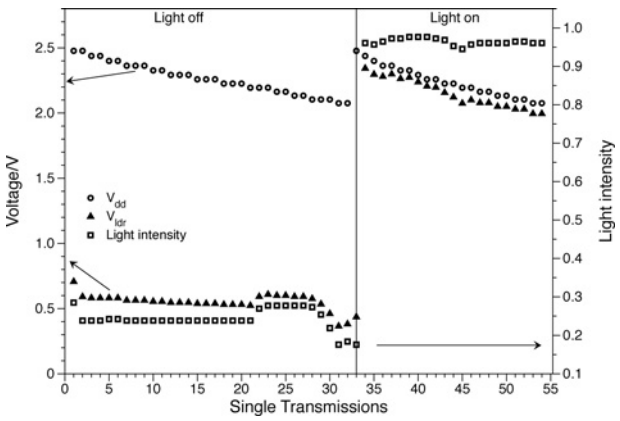

Fig. 13 *Received data displayed as a function of reading number to aid clarity*

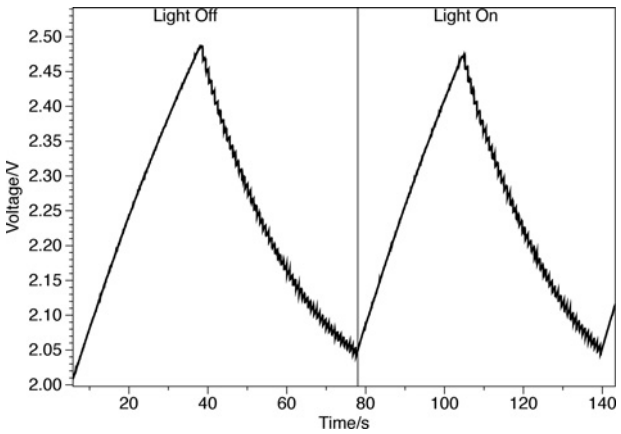

Fig. 15 *V_{Store} variation with time for multiple for two distinct sensor readings*

this not to be the case and that there are many more transmissions taking place than are being read in by the receiver software. This is because of the receiving software detecting and rejecting corrupted packets. There are potentially a large number of rejected packets depending on how electrically noisy the target environment is; however, for slowly varying environments a system such as this, which can send many packets of data over many seconds, the system reliability will increase.

5 Conclusion

This work has shown that an energy harvester-powered system can now be realised with commercial off-the-shelf components and that techniques can be used to maximise the operation time without the need for expensive non-standard components or custom electronics. By changing the operating parameters of the onboard electronics and selectively activating components on an as-required basis the system performance can be improved by several orders of magnitude if the duty ratio is used as the comparison metric. The system was able to operate at a range of accelerations with some of the lowest for a continually on piezoelectric-powered system reported to date. It was also shown that with a careful design approach the system can be designed to operate continuously above a certain threshold acceleration, this threshold is dependent on the current requirements of the chosen components and will vary from system to system. The system can easily be modified to run between smaller operating limits, and this will further decrease the minimum operating acceleration and increase the deployability of the system.

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