1. Description

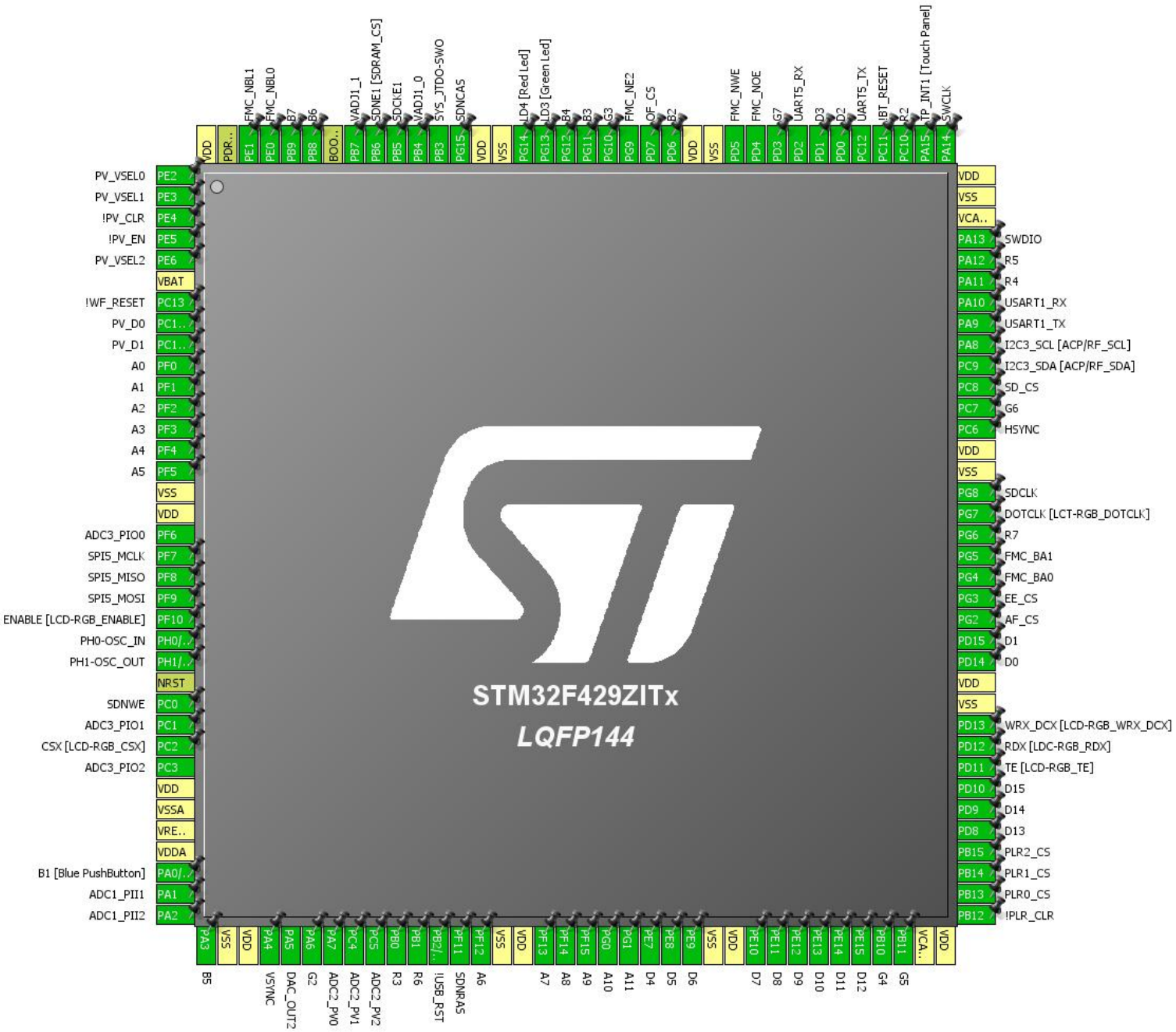
1.1. Project

Project Name	PRIME
Board Name	STM32F429I-DISCO
Generated with:	STM32CubeMX 4.12.0
Date	04/23/2016

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F429/439
MCU name	STM32F429ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	PV_VSEL0
2	PE3 *	I/O	GPIO_Output	PV_VSEL1
3	PE4 *	I/O	GPIO_Output	!PV_CLR
4	PE5 *	I/O	GPIO_Output	!PV_EN
5	PE6 *	I/O	GPIO_Output	PV_VSEL2
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Output	!WF_RESET
8	PC14/OSC32_IN *	I/O	GPIO_Output	PV_D0
9	PC15/OSC32_OUT *	I/O	GPIO_Output	PV_D1
10	PF0	I/O	FMC_A0	A0
11	PF1	I/O	FMC_A1	A1
12	PF2	I/O	FMC_A2	A2
13	PF3	I/O	FMC_A3	A3
14	PF4	I/O	FMC_A4	A4
15	PF5	I/O	FMC_A5	A5
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	ADC3_IN4	ADC3_PIO0
19	PF7	I/O	SPI5_SCK	SPI5_MCLK
20	PF8	I/O	SPI5_MISO	SPI5_MISO
21	PF9	I/O	SPI5_MOSI	SPI5_MOSI
22	PF10	I/O	LTDC_DE	ENABLE [LCD-RGB_ENABLE]
23	PH0/OSC_IN	I/O	RCC_OSC_IN	PH0-OSC_IN
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	PH1-OSC_OUT
25	NRST	Reset		
26	PC0	I/O	FMC_SDNWE	SDNWE
27	PC1	I/O	ADC3_IN11	ADC3_PIO1
28	PC2 *	I/O	GPIO_Output	CSX [LCD-RGB_CSX]
29	PC3	I/O	ADC3_IN13	ADC3_PIO2
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	GPIO_EXTI0	B1 [Blue PushButton]
35	PA1	I/O	ADC1_IN1	ADC1_PII1

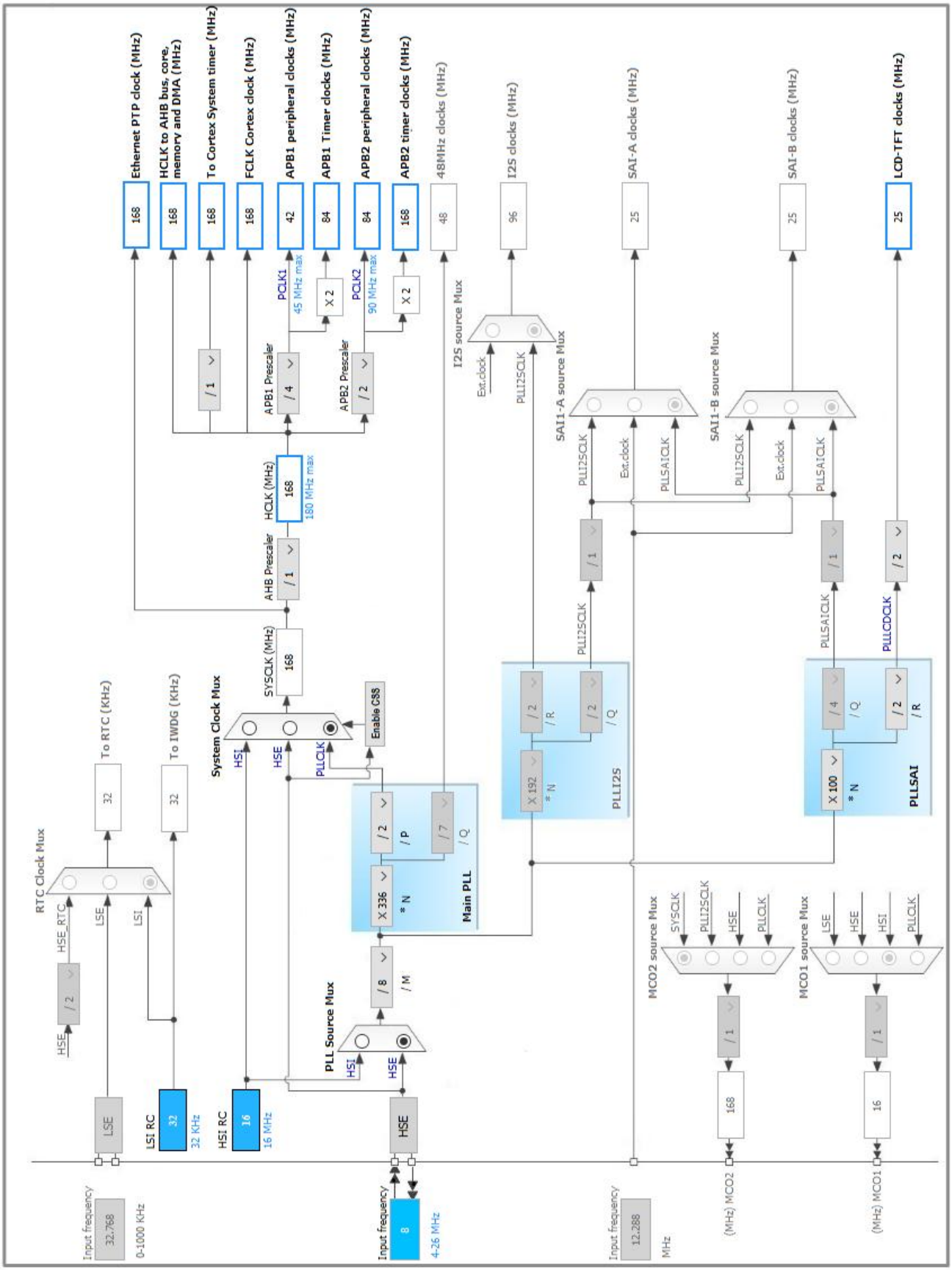
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
36	PA2	I/O	ADC1_IN2	ADC1_PII2
37	PA3	I/O	LTDC_B5	B5
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	LTDC_VSYNC	VSYNC
41	PA5	I/O	DAC_OUT2	
42	PA6	I/O	LTDC_G2	G2
43	PA7	I/O	ADC2_IN7	ADC2_PV0
44	PC4	I/O	ADC2_IN14	ADC2_PV1
45	PC5	I/O	ADC2_IN15	ADC2_PV2
46	PB0	I/O	LTDC_R3	R3
47	PB1	I/O	LTDC_R6	R6
48	PB2/BOOT1 *	I/O	GPIO_Output	!USB_RST
49	PF11	I/O	FMC_SDNRAS	SDNRAS
50	PF12	I/O	FMC_A6	A6
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	FMC_A7	A7
54	PF14	I/O	FMC_A8	A8
55	PF15	I/O	FMC_A9	A9
56	PG0	I/O	FMC_A10	A10
57	PG1	I/O	FMC_A11	A11
58	PE7	I/O	FMC_D4	D4
59	PE8	I/O	FMC_D5	D5
60	PE9	I/O	FMC_D6	D6
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	FMC_D7	D7
64	PE11	I/O	FMC_D8	D8
65	PE12	I/O	FMC_D9	D9
66	PE13	I/O	FMC_D10	D10
67	PE14	I/O	FMC_D11	D11
68	PE15	I/O	FMC_D12	D12
69	PB10	I/O	LTDC_G4	G4
70	PB11	I/O	LTDC_G5	G5
71	VCAP_1	Power		
72	VDD	Power		
73	PB12 *	I/O	GPIO_Output	!PLR_CLR
74	PB13 *	I/O	GPIO_Output	PLR0_CS

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
75	PB14 *	I/O	GPIO_Output	PLR1_CS
76	PB15 *	I/O	GPIO_Output	PLR2_CS
77	PD8	I/O	FMC_D13	D13
78	PD9	I/O	FMC_D14	D14
79	PD10	I/O	FMC_D15	D15
80	PD11 *	I/O	GPIO_Input	TE [LCD-RGB_TE]
81	PD12 *	I/O	GPIO_Output	RDX [LDC-RGB_RDX]
82	PD13 *	I/O	GPIO_Output	WRX_DCX [LCD-RGB_WRX_DCX]
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	FMC_D0	D0
86	PD15	I/O	FMC_D1	D1
87	PG2 *	I/O	GPIO_Output	AF_CS
88	PG3 *	I/O	GPIO_Output	EE_CS
89	PG4	I/O	FMC_BA0	
90	PG5	I/O	FMC_BA1	
91	PG6	I/O	LTDC_R7	R7
92	PG7	I/O	LTDC_CLK	DOTCLK [LCT-RGB_DOTCLK]
93	PG8	I/O	FMC_SDCLK	SDCLK
94	VSS	Power		
95	VDD	Power		
96	PC6	I/O	LTDC_HSYNC	HSYNC
97	PC7	I/O	LTDC_G6	G6
98	PC8 *	I/O	GPIO_Output	SD_CS
99	PC9	I/O	I2C3_SDA	I2C3_SDA [ACP/RF_SDA]
100	PA8	I/O	I2C3_SCL	I2C3_SCL [ACP/RF_SCL]
101	PA9	I/O	USART1_TX	
102	PA10	I/O	USART1_RX	
103	PA11	I/O	LTDC_R4	R4
104	PA12	I/O	LTDC_R5	R5
105	PA13	I/O	SYS_JTMS-SWDIO	SWDIO
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	SWCLK
110	PA15	I/O	GPIO_EXTI15	TP_INT1 [Touch Panel]
111	PC10	I/O	LTDC_R2	R2
112	PC11 *	I/O	GPIO_Output	!BT_RESET

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
113	PC12	I/O	UART5_TX	
114	PD0	I/O	FMC_D2	D2
115	PD1	I/O	FMC_D3	D3
116	PD2	I/O	UART5_RX	
117	PD3	I/O	LTDC_G7	G7
118	PD4	I/O	FMC_NOE	
119	PD5	I/O	FMC_NWE	
120	VSS	Power		
121	VDD	Power		
122	PD6	I/O	LTDC_B2	B2
123	PD7 *	I/O	GPIO_Output	OF_CS
124	PG9	I/O	FMC_NE2	
125	PG10	I/O	LTDC_G3	G3
126	PG11	I/O	LTDC_B3	B3
127	PG12	I/O	LTDC_B4	B4
128	PG13 *	I/O	GPIO_Output	LD3 [Green Led]
129	PG14 *	I/O	GPIO_Output	LD4 [Red Led]
130	VSS	Power		
131	VDD	Power		
132	PG15	I/O	FMC_SDNCAS	SDNCAS
133	PB3	I/O	SYS_JTDO-SWO	
134	PB4 *	I/O	GPIO_Output	VADJ1_0
135	PB5	I/O	FMC_SDCKE1	SDCKE1
136	PB6	I/O	FMC_SDNE1	SDNE1 [SDRAM_CS]
137	PB7 *	I/O	GPIO_Output	VADJ1_1
138	BOOT0	Boot		
139	PB8	I/O	LTDC_B6	B6
140	PB9	I/O	LTDC_B7	B7
141	PE0	I/O	FMC_NBL0	
142	PE1	I/O	FMC_NBL1	
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN1

mode: IN2

mode: Vrefint Channel

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel Vrefint ***
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. ADC2

mode: IN7

mode: IN14

mode: IN15

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 15 ***
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.3. ADC3

mode: IN4

mode: IN11

mode: IN13

5.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled

Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 11 ***
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.4. CRC

mode: Activated

5.5. DAC

mode: OUT2 Configuration

5.5.1. Parameter Settings:

DAC Out2 Settings:

Output Buffer	Enable
Trigger	None

5.6. DMA2D

mode: Activated

5.6.1. Parameter Settings:

Basic Parameters:

Transfer Mode	Memory to Memory
Color Mode	ARGB8888
Output Offset	0

Foreground layer Configuration:

DMA2D Input Color Mode	ARGB8888
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0

5.7. FMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: NE2

Memory type: SRAM

Address: 1 bit

Data: 8 bits

SDRAM 1

Clock and chip enable: SDCKE1+SDNE1

Internal bank number: 4 banks

Address: 12 bits

Data: 16 bits

Byte enable: set

5.7.1. NOR/PSRAM 1:

NOR/PSRAM control:

Memory type	SRAM
Bank	Bank 1 NOR/PSRAM 2
Write operation	Disabled
Extended mode	Disabled

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	15
Data setup time in HCLK clock cycles	255
Bus turn around time in HCLK clock cycles	15

5.7.2. SDRAM 1:

SDRAM control:

Bank	SDRAM bank 2
Column bit number	8 bits
Row bit number	11 bits

CAS latency	**3 memory clock cycles ***
Write protection	Disabled
SDRAM common clock	**2 HCLK clock cycles ***
SDRAM common burst read	Disabled
SDRAM common read pipe delay	**1 HCLK clock cycle ***

SDRAM timing in memory clock cycles:

Load mode register to active delay	**2 ***
Exit self-refresh delay	**7 ***
Self refresh time	**4 ***
SDRAM common row cycle delay	**7 ***
Write recovery time	**3 ***
SDRAM common row precharge delay	**2 ***
Row to column delay	**2 ***

5.8. I2C3

I2C: I2C

5.8.1. Parameter Settings:

Master Features:

I2C Speed Mode	**Fast Mode ***
I2C Clock Speed (Hz)	400000
Fast Mode Duty Cycle	Duty cycle Tlow/Thigh = 2

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

5.9. LTDC

Display Type: RGB666 (18 bits)

5.9.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	8
Horizontal Back Porch	7
Active Width	640
Horizontal Front Porch	6
HSync Width	7
Accumulated Horizontal Back Porch Width	14
Accumulated Active Width	654
Total Width	660

Synchronization for Height:

Vertical Synchronization Height	4
Vertical Back Porch	2
Active Height	480
Vertical Front Porch	2
VSync Height	3
Accumulated Vertical Back Porch Height	5
Accumulated Active Height	485
Total Height	487

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

BackGround Color:

Red	0
Green	0
Blue	0

5.9.2. Layer Settings:

BackGround Color:

Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0
Layer 1 - Blue	0
Layer 1 - Green	0
Layer 1 - Red	0

Number of Layers:

Number of Layers	2 layers

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	0
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	0
Layer 1 - Window Horizontal Start	0
Layer 1 - Window Horizontal Stop	0
Layer 1 - Window Vertical Start	0
Layer 1 - Window Vertical Stop	0

Pixel Parameters:

Layer 0 - Pixel Format	ARGB8888
Layer 1 - Pixel Format	ARGB8888

Blending:

Layer 0 - Alpha constant for blending	0
Layer 0 - Default Alpha value	0
Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant
Layer 1 - Alpha constant for blending	0
Layer 1 - Default Alpha value	0
Layer 1 - Blending Factor1	Alpha constant
Layer 1 - Blending Factor2	Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	0
Layer 0 - Color Frame Buffer Line Length (Image Width)	0
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	0
Layer 1 - Color Frame Buffer Start Adress	0
Layer 1 - Color Frame Buffer Line Length (Image Width)	0
Layer 1 - Color Frame Buffer Number of Lines (Image Height)	0

5.10. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.10.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled

Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Disabled

5.11. SPI5

Mode: Full-Duplex Master

5.11.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**42.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.12. SYS

Debug: SWD and Asynchronous Trace

5.13. TIM6

mode: Activated

5.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.14. TIM7

mode: Activated

5.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.15. UART5

Mode: Asynchronous

5.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.16. USART1

Mode: Asynchronous

5.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	ADC1_PII1
	PA2	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	ADC1_PII2
ADC2	PA7	ADC2_IN7	Analog mode	No pull-up and no pull-down	n/a	ADC2_PV0
	PC4	ADC2_IN14	Analog mode	No pull-up and no pull-down	n/a	ADC2_PV1
	PC5	ADC2_IN15	Analog mode	No pull-up and no pull-down	n/a	ADC2_PV2
ADC3	PF6	ADC3_IN4	Analog mode	No pull-up and no pull-down	n/a	ADC3_PIO0
	PC1	ADC3_IN11	Analog mode	No pull-up and no pull-down	n/a	ADC3_PIO1
	PC3	ADC3_IN13	Analog mode	No pull-up and no pull-down	n/a	ADC3_PIO2
DAC	PA5	DAC_OUT2	Analog mode	No pull-up and no pull-down	n/a	
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	High	A0
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	High	A1
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	High	A2
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	High	A3
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	High	A4
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	High	A5
	PC0	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	High	SDNWE
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	High	SDNRAS
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	High	A6
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	High	A7
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	High	A8
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	High	A9
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	High	A10
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	High	A11
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	High	D4
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	High	D5
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	High	D6
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	High	D7
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	High	D8
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	High	D9
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	High	D10
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	High	D11
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	High	D12
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	High	D13
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	High	D14

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	High	D15
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	High	D0
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	High	D1
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	High	SDCLK
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	High	D2
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	High	D3
	PD4	FMC_NOE	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD5	FMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG9	FMC_NE2	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	High	SDNCAS
	PB5	FMC_SDCKE1	Alternate Function Push Pull	No pull-up and no pull-down	High	SDCKE1
	PB6	FMC_SDNE1	Alternate Function Push Pull	No pull-up and no pull-down	High	SDNE1 [SDRAM_CS]
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	High	
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	Pull-up	Low	I2C3_SDA [ACP/RF_SDA]
	PA8	I2C3_SCL	Alternate Function Open Drain	Pull-up	Low	I2C3_SCL [ACP/RF_SCL]
LTDC	PF10	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	ENABLE [LCD-RGB_ENABLE]
	PA3	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low	B5
	PA4	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	VSYNC
	PA6	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low	G2
	PB0	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low	R3
	PB1	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low	R6
	PB10	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Low	G4
	PB11	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low	G5
	PG6	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low	R7
	PG7	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	DOTCLK [LCT-RGB_DOTCLK]
	PC6	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	HSYNC
	PC7	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low	G6
	PA11	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low	R4
	PA12	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low	R5
	PC10	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	Low	R2
	PD3	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low	G7
	PD6	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	Low	B2
	PG10	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low	G3
	PG11	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low	B3

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PG12	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low	B4
	PB8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low	B6
	PB9	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low	B7
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	PH0-OSC_IN
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	PH1-OSC_OUT
SPI5	PF7	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPI5_MCLK
	PF8	SPI5_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPI5_MISO
	PF9	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPI5_MOSI
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	
UART5	PC12	UART5_TX	Alternate Function Push Pull	Pull-up	**High ***	
	PD2	UART5_RX	Alternate Function Push Pull	Pull-up	**High ***	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**High ***	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**High ***	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PV_VSEL0
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PV_VSEL1
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	!PV_CLR
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	!PV_EN
	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PV_VSEL2
	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	!WF_RESET
	PC14/OSC32_IN	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PV_D0
	PC15/OSC32_OUT	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PV_D1
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CSX [LCD-RGB_CSX]
	PA0/WKUP	GPIO_EXTI0	**External Event Mode with Rising edge trigger detection ***	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PB2/BOOT1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	!USB_RST
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	!PLR_CLR
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PLR0_CS
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PLR1_CS
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PLR2_CS
	PD11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	TE [LCD-RGB_TE]
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RDX [LDC-RGB_RDX]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WRX_DCX [LCD-RGB_WRX_DCX]
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AF_CS
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EE_CS
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SD_CS
	PA15	GPIO_EXTI15	**External Event Mode with Rising edge trigger detection ***	No pull-up and no pull-down	n/a	TP_INT1 [Touch Panel]
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	!BT_RESET
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OF_CS
	PG13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Green Led]
	PG14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD4 [Red Led]
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	VADJ1_0
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	VADJ1_1

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	**Medium ***

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	**One Quarter Full ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word
Peripheral Burst Size:	Single
Memory Burst Size:	Single

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
System tick timer	true	0	0
DMA2 stream0 global interrupt	true	0	0
Non maskable interrupt	unused		
Hard fault interrupt	unused		
Memory management fault	unused		
Pre-fetch fault, memory access fault	unused		
Undefined instruction or illegal state	unused		
Debug monitor	unused		
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
USART1 global interrupt	unused		
FMC global interrupt	unused		
UART5 global interrupt	unused		
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	unused		
TIM7 global interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
SPI5 global interrupt	unused		
LTDC global interrupt	unused		
LTDC global error interrupt	unused		
DMA2D global interrupt	unused		

*** User modified value**

7. Power Plugin report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F429/439
MCU	STM32F429ZITx
Datasheet	024030_Rev5

7.2. Parameter Selection

Temperature	25
Vdd	null

8. Software Project

8.1. Project Settings

Name	Value
Project Name	PRIME
Project Folder	C:\Users\drmoore\Documents\PEGMA\Firmware\PRIME\environment\STM32Cub
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.10.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No