

Intra-Operation Dynamic Voltage Scaling

ABSTRACT

Embedded peripherals are often specified with a range of performance characteristics that are affected by their supply voltage. Typically the supply voltage is static and therefore both power consumption and performance traits are known at design-time. With Intra-Operation Dynamic Power Management (IODVS), we focus on reducing the power consumption of peripheral devices by dynamically modulating supply voltage as they perform specified operations. IODVS is designed to have minimal impact on CPU utilization through the use of peripheral power profiles (PPP) which designate an ideal voltage on a per-state basis. Any peripheral operation seamlessly flows through the pre-determined states and the supply voltage is modulated automatically upon each transition. Peripheral power profiles are unique in that during high-performance states such as data-transmission, peripherals can have the high supply voltage they demand. Likewise, during low-performance states such as mandatory delays, the system can decrease domain voltage and thus reduce power consumption intra-operation. We demonstrate this method on various common peripherals and have found energy savings of up to 40%.

Introduction

Consider an embedded system where the supply voltage to an application MCU is decoupled from the supply voltage of the peripherals that it is controlling. This is becoming more common as modern MCU applications take advantage of Dynamic Voltage and Frequency Scaling (DVFS) and, in effect, IODVS is a natural extension of DVFS to the peripheral domain. The same modulation techniques (DAC, PWM, etc.) that a MCU may use to control its own voltage can be used to control peripheral voltages. We have found that energy can be saved by lowering the domain voltage during timeframes where low-performance is allowed such as mandatory wait periods.

The Microchip SPI EEPROM [1] is a typical peripheral device. A typical write operation of the device has the following state transitions and timings:

Chip Select, Write Enabled	Write Cmd/Data	Delay	Verify Cmd/Data, Chip Deselect
1us	128us	5ms	128us

Table 1: EEPROM Write Cycle

Both the read and write operations are voltage/frequency dependent in that the 25AA512 can communicate at 20MHz while above 4.5v, 10MHz while above 3.3v and 2MHz while above 1.8v. It follows that one should communicate between the two domains at matched voltages thereby maximizing data transfer while minimizing energy delay product (EDP). The maximum benefit of IODVS can be realized during the longest portion of the transaction: the delay. By decreasing the supply voltage to 1.8v during the delay state, the energy cost of the delay is decreased by 58%.

The IODVS technique is applicable to many peripherals and this investigation considered the peripherals listed in Figure 1 as a representative sample:

approaches to date can be categorized as a combination of either online [4] or offline [5] and deterministic [6] or probabilistic [7].

Offline analysis can aid in the implementation of DPM by analyzing the CFG of a task to determine when a peripheral is likely to be accessed [5]. Similar data can be realized online by profiling a task and determining which paths lead to a peripheral access [8]. Both methods enhance the accuracy of predictions regarding the optimal peripheral wakeup time. In fact, all methods must evaluate the cost/benefit of peripheral deactivation with respect to the energy savings gleaned versus the time spent reactivating the device when next needed. This equality is commonly known as the breakeven time [9].

Some peripherals provide multiple performance/power states. As such, Mode Dependence Graphs were developed in order to accurately quantify the breakeven time between states [10]. Approaches have been explored with respect to optimally scheduling devices with multiple power saving states and in systems where multiple tasks share a common resource (inter-task DPM). Naturally, the decrease in voltage margin along with the decrease in available task slack time also decreases the ability to detect and correct errors as they occur [11].

The CADVS technique [12] is similar to IODVS in that an adjustable regulator is used to operate an embedded system at its minimum voltage requirements. IODVS extends the technique into multiple voltage domains and operates at a much finer granularity. The technique is different in that we seek to decrease the energy cost of performing peripheral operations as they are performed.

Assumptions

Create a completely controllable buck power supply via analog input through a DAC. The power source will be supplying voltage for multiple peripherals on a domain separate from the MCU. All digital transactions between the MCU and the peripheral domain will be made at the same voltage. The cost of level translation or isolation is too great to warrant implementation. Also, various sources have cited that the lowest EDP of communication occurs at matched voltage/frequencies. Thus we are left with intra-operation voltage modulation as our means of decreasing energy consumption.

Methods and Materials

The peripheral power supply (PPS) is outfitted with current sense resistors and amplifiers on both the input to the PPS and the output to the peripheral domain. These signals, along with the input voltage to the PPS and the output voltage from the PPS are fed into the ADC of the STM32F205 microcontroller and sampled at 1MSPS. The MCU has 3 simultaneously sampling ADCs which allows for simultaneous measurement of the output voltage, input current and output current.

Peripheral operations are broken up into states as per an intrinsic state transition diagram. For example, in order to write to EEPROM, the MCU must issue the write command and write the data, wait for a specified delay period and then read the data back in order to verify a correct write. Therefore, the states are delineated as Idle, Writing, Waiting and Verifying.

Each peripheral operation is associated with a specific voltage. For instance, as per our assumptions, data transfers must occur at equal voltages between the domain and MCU. Therefore the Writing and Verifying states voltage must equal that of the MCU (3.3v). This leaves the Idle and Waiting states free for energy optimization. Special care was taken to guarantee that the pins connecting the MCU to peripheral devices were changed to input mode upon transitions into the Idle/Wait states. This ensured that the peripherals were not inadvertently being powered from port pins on the MCU.

The set of states and associated voltages creates a power profile per peripheral. Each test designates a power profile to use. Peripheral memory was tested with random data and across random memory addresses. Tests were run 1000x and the results were averaged. If any test failed to complete the operation successfully then the test-set was considered to have failed.

Results

All test results were measured entirely in-system using the 3 simultaneously sampling ADC converters. The converters are triggered from a timer overflow using a reload value that allows for a complete buffer fill roughly corresponding to the expected length of the test. For example, the duration of the SDCard test was approximately 15ms with a buffer size of 10240 samples yielded 1.465us per sample (or a sample rate of 683KHz). Upon an ADC trigger, the state of the peripheral is stored synchronously with the sample. Each test data set was retrieve by MATLAB upon completion and is composed of:

- Time Scale
- 10240 12-bit ADC Samples per channel
 - Output Voltage
 - Input Current
 - Output Current
- 10240 State Samples (state of the device: reading/writing/etc)
- Bit Resolution (ADC sample → Current or Voltage value)

One immediately notices the effects of domain capacitance. The domain voltage changes at a rate corresponding to Equation 1. This is most noticeable as the voltage transitions from high to low because the power supply has a high current drive capability, but no current sink circuitry. This is a benefit to IODVS in that peripheral performance is unaffected by higher-than-necessary voltage in the states of concern.

$$V = V_0 e^{\frac{-t}{RC}}$$

Equation 1

$$I = C \frac{dV}{dt}$$

Equation 2

Likewise, on low to high transitions, the output current of the power supply spikes in order to charge the domain as quickly as possible via Equation 2. This is also beneficial to IODVS in that it allows for very fast transitions from the wait states to the communication states.

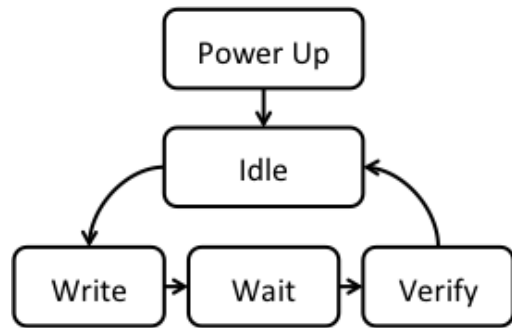


Figure 2: EEPROM Write Procedure

State	Static (uJ)	IODVS (uJ)	Delta
Idle	10.24	3.49	-65.91%
Write	13.79	17.85	29.47%
Wait	64.59	33.71	-47.80%
Verify	17.58	17.40	-1.02%
Idle	8.81	7.96	-9.57%
Total	115.02	80.43	-30.07%

Table 3: EEPROM Energy Consumption

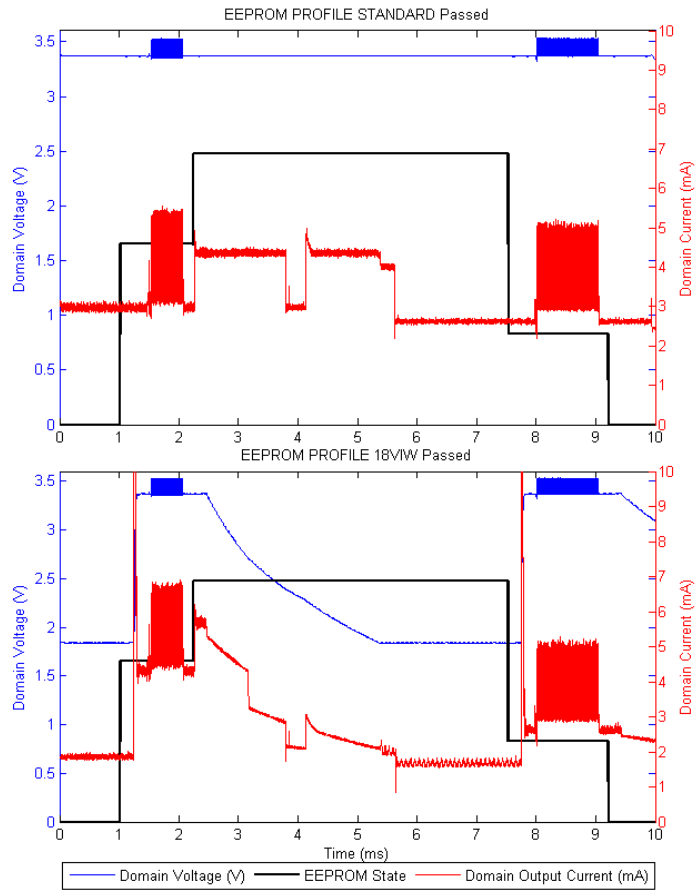


Figure 3: EEPROM Test Results

Microchip MCP25AA512 EEPROM

IODVS uses peripheral power profiles (PPP) correlate peripheral voltages with internal state. The standard PPP indicates that all states (writing/waiting/verifying/etc) should have 3.3V applied to the peripheral. The 1.8VIW (1.8V Idle/Wait) profile indicates that the EEPROM should have 1.8V applied during the idle and waiting states and 3.3V applied on all others. Figure 3 provides a comparison of both the standard PPP and the 1.8VIW profiles enabled by IODVS.

The state transition diagram of Figure 2 is known a-priori and is followed throughout the tests illustrated in Figure 3. The test begins with the powered up and having been idle for approximately 100ms. The delay ensures that any other devices on the domain have completed their power-on-reset routines and this effect is discussed further in the future work section.

The effects of IODVS are immediately noticeable during the Idle and Wait states. The energy consumption during these states decreased 66% and 48% respectively. Energy consumption during the Write state appears to have increased by 30%. This is primarily due to the energy required to charge the domain to 3.3V which is required to complete the transaction. Note that although the current measurement appears to clip the graph in Figure 3, that the current spike was indeed measured to be approximately 15mA and the data was analyzed accordingly.

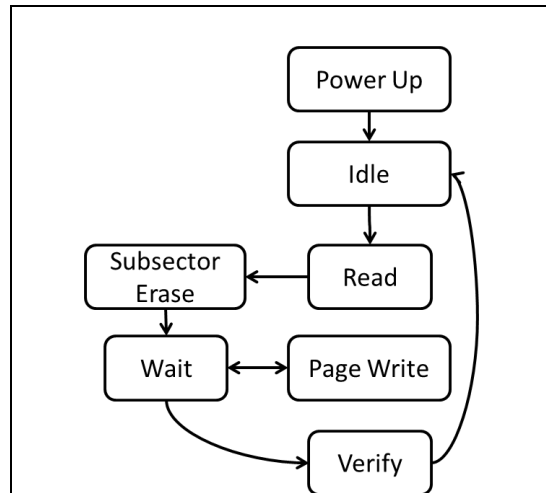


Figure 4: Serial Flash Read-Modify-Write Procedure

State	Static (uJ)	IODVS (uJ)	Delta
Idle	10.73	5.63	-47.58%
Read	71.51	72.36	1.19%
Erase	2.47	2.47	-0.13%
Write*	89.48	99.16	10.82%
Wait*	574.84	365.75	-36.37%
Verify	83.78	52.77	-37.02%
Idle	38.92	38.20	-1.85%
Total	2666.18	1614.57	-39.44%

Table 4: Serial Flash Energy Consumption

*Sequential writes and waits combined

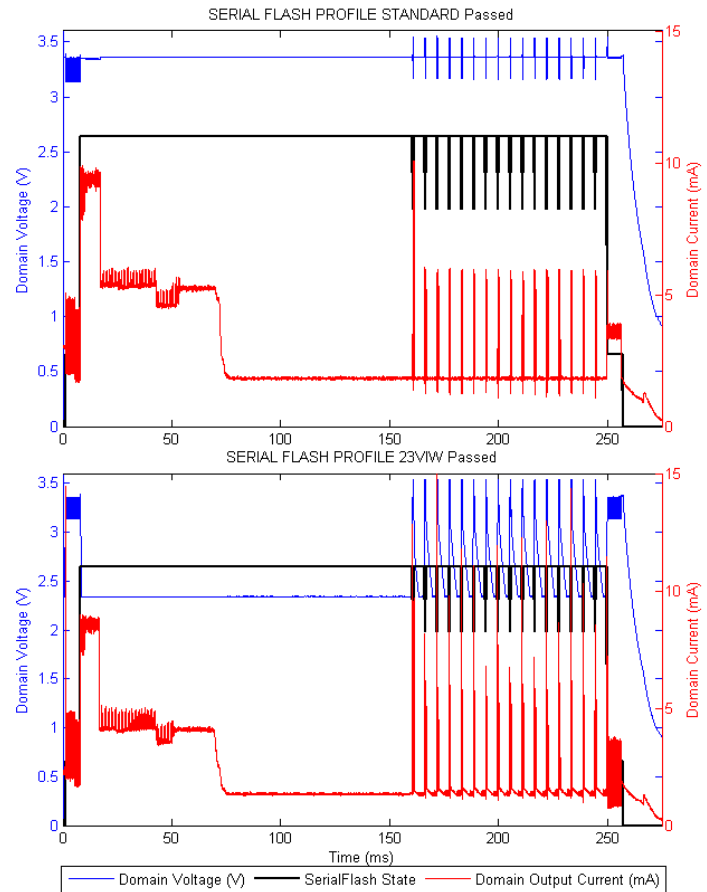


Figure 5: Serial Flash Test Results

Numonyx M25PX16 Serial Flash

Serial flash [12] modules have a somewhat more complicated state transition diagram than EEPROM. Serial flash chips can only write zeroes to their memory locations. At a simplistic level, this requirement necessitates a complete erase of a subsector before modifying any memory within it. The M25PX16 supports a minimum of 4KB (sub-sector) erase and a maximum of 256B (page) sequential writes. In order to perform a read-modify-write operation, the transition diagram shown in Figure 4 is followed wherein a 4KB sub-sector is erased and 16 page writes follow.

As the test begins, the chip is in the Idle state; it does not require an initialization routine to function. The specified sub-sector of memory is read into cache and modified with the data to be written while the sub-sector erase operation is ongoing. Note that cross-subsector writes were not evaluated because that would simply require two sequences to occur sequentially. Upon completion of the erase cycle, the modified data are written back to the flash module one page at a time. The writes cause a series of alternating “write-wait” states and the corresponding voltage/state changes are evident in Figure 5.

Table 4 summarizes the energy saved through the use of IODVS. As expected, the most significant savings are found in the Idle and Wait states and some small increase is seen in the active states.

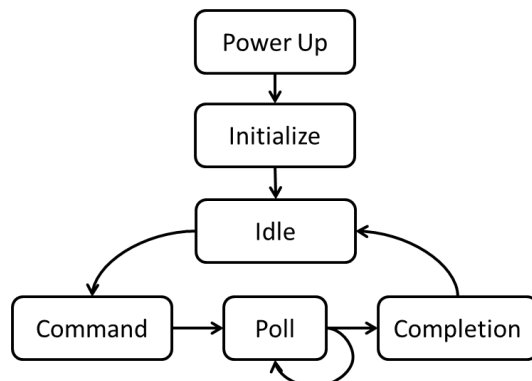


Figure 6: SD Card Measurement Procedure

State	Static	IODVS	Delta
Idle	3.10	1.16	-62.52%
Write	3.80	4.45	17.08%
Wait	18.09	8.90	-50.79%
Verify	4.97	6.05	21.73%
Idle	2.73	2.73	-0.11%
Total	32.6852	23.2879	-28.75%

Table 5: SD Card Write Energy Consumption

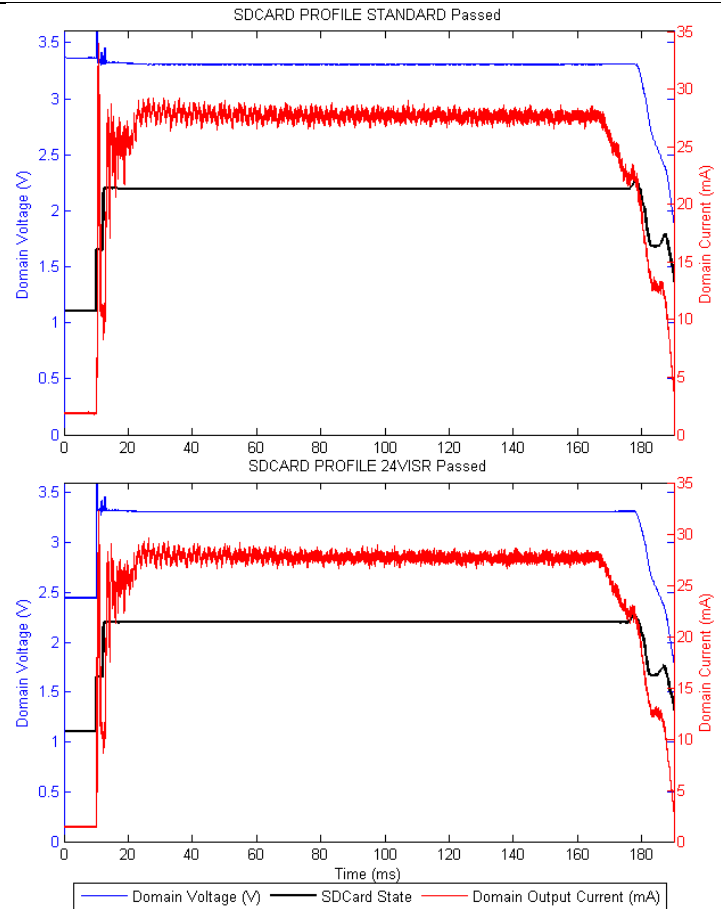


Figure 7: SD Card Test Results

Swissbit S-200U 512MB Micro-SD Memory Card

The SD Card protocol heavily relies on polling the peripheral device. As such, there is not much opportunity to apply IODVS like what was shown for the EEPROM and serial flash cases. However, it is very beneficial to apply IODVS to the SD Card after the device has completed its initialization routine.

An SD Card must be initialized before use, the test fixture communicates with the device via SPI and the initialization process takes approximately 200ms. Therefore, when the device is not in use, it can transition to the low-power 2.7V “Initialized” state, rather than undergoing a complete power-cycle as would be typical with DPM.

Thus, the benefits of IODVS with respect to the SD Card are highly dependent on duty cycle. It is shown that the initialized current consumption of the device is reduced by 30% while all other states have no change. Therefore, by using IODVS, the response time of the device is decreased when measured against DPM techniques and the power consumption of the devices is decreased when compared to the static-voltage case.

The SD Card has the highest current consumption of the devices tested and as such causes high droop in domain voltage when active. Decreasing this voltage sag while maintaining or decreasing domain capacitance would increase the efficacy of IODVS and this is further discussed in the future work section.

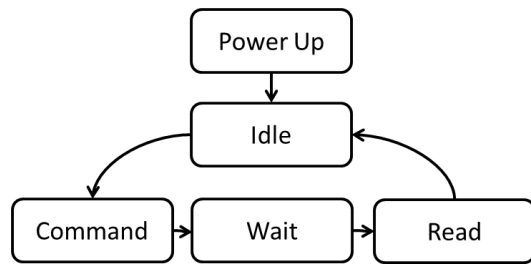


Figure 8: HIH-6130 Measurement Procedure

State	Static (uJ)	IODVS (uJ)	Delta
Idle	10.28	6.28	-38.87%
Write	1.68	1.05	-37.60%
Wait	399.07	245.89	-38.38%
Read	4.30	4.42	2.62%
Idle	17.08	19.50	14.18%
Total	432.41	277.14	-35.91%

Table 6: HIH-6130 Write Energy Consumption

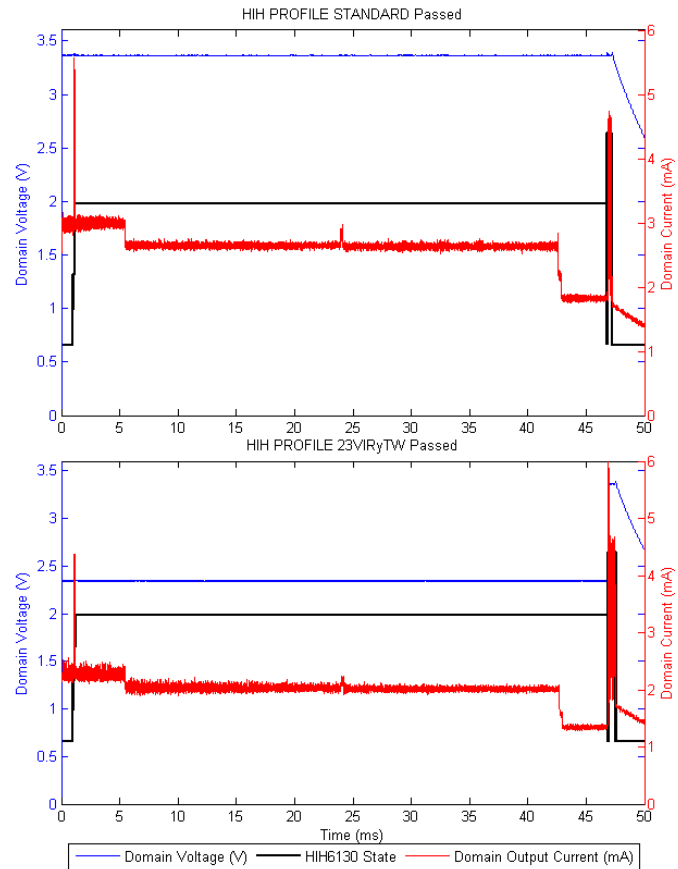


Figure 9: HIH6130 Test Results

Honeywell HIH6130 Temperature / Humidity Sensor

The MCU communicates with the temperature and humidity sensor [14] via I2C. The interface communicates in an open-drain fashion and therefore logic-high levels are accomplished simply by changing the MCU pin direction from output-low to input. The I2C bus was pulled to match the voltage level of the domain and therefore, when the MCU is sending data to the peripheral, it is not necessary to match the voltage of the MCU and peripheral domain. However, when the MCU is retrieving data from the peripheral, the voltages must be matched in order to ensure that input logic-level requirements are satisfied on the MCU.

As such, the test begins in the Idle state (Figure 8) and the MCU issues a “Measure” command to the sensor. The peripheral transitions to its Wait state where it is internally measuring temperature and humidity. There is a noticeable drop in current in Figure 9 upon the completion of the measurement and the MCU begins to read the data soon afterward.

The primary benefit of IODVS in the case of this peripheral is that the rate of I2C communication is highly dependent on the magnitude of the pull-up resistors enabling it and the voltage of communication. By allowing the voltage to increase to 3.3V during the read, larger pull-up resistors can be used, thus decreasing static power dissipation.

Conclusions and Future Work

IODVS has been shown to decrease energy consumption on a typical group of peripherals by 30-40% with no decreases in either performance or accuracy. The efficacy of the technique is increased with low-duty cycles. The overhead of performing IODVS is minimal through the use of pre-defined peripheral power profiles. The additional circuitry required to implement IODVS is minimal and in many cases, the performance increase may justify the expense or the power budget decrease may offset the additional cost.

IODVS would be more effective if it were used in a system with zero domain capacitance. This would allow for instantaneous changes in domain voltage and reduce the inrush current when charging a domain. Obviously zero-capacitance is impractical, but minimizing capacitance while maintaining steady voltage to peripheral devices with varying loads would certainly increase the efficiency of IODVS.

The efficacy of IODVS is highly dependent on the type of SMPS used to control domain voltage. It was seen that the input current to the controlling SMPS increased dramatically when changing domain voltage. As such, for a brief period of time, the efficiency of the SMPS is very low. This could be addressed by slowing the rate of change in feedback voltage (and augmented with a predictor), or by using a different type of adjustable SMPS.

Manipulating the voltage across a domain of devices is bound to impact some devices more than others. For instance, if the domain voltage drops below 2.7V, the SD Card reverts from an initialized state to the idle state. Therefore, before adjusting a particular device on the domain, IODVS should determine if that would cause an overall benefit or detriment to devices on the domain. This could be determined by majority vote of devices on the domain. If indeed the voltage is manipulated out of bounds for a particular device, the driver for each device on the domain needs to be notified of the voltage change so that re-initialization can take place if necessary.

References

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