PACER

Peripheral Activity Completion Estimation and Recognition

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*Abstract*—Embedded peripheral devices such as memories, sensors and communications interfaces are used to perform a function external to a host microcontroller. The device manufacturer typically specifies worst-case current consumption and latency estimates for each of these peripheral actions. Peripheral Activity Completion, Estimation and Recognition (PACER) is introduced as a variety of algorithms that can be applied to detect completed peripheral operations in real-time. By detecting activity completion, PACER enables the host to exploit slack between the worst-case estimate and the actual response time. These methods were tested independently and in conjunction with IODVS on multiple common peripheral devices. For the peripheral devices under test, the test fixture confirmed decreases in energy expenditures of up to 62% and latency reductions of up to 67%.

Keywords-Embedded Systems; Dynamic Voltage Scaling (DVS); Dynamic Power Management (DPM); low-power; low-energy; wireless sensor node (WSN); timing and performance analysis; energy-aware design; power aware embedded computing; adaptive embedded systems.

# Introduction

Embedded systems are often constrained by timing and energy budgets because both factors affect the resultant cost and size of the system. Peripheral devices external to the microcontroller (MCU) such as those shown in Figure 1 can play a significant role in system-wide energy consumption. There are many methods available for decreasing the static power usage of peripherals [1] [2] [3]. PACER decreases dynamic power consumption and latency by exploiting the slack between actual versus worst-case operation time.

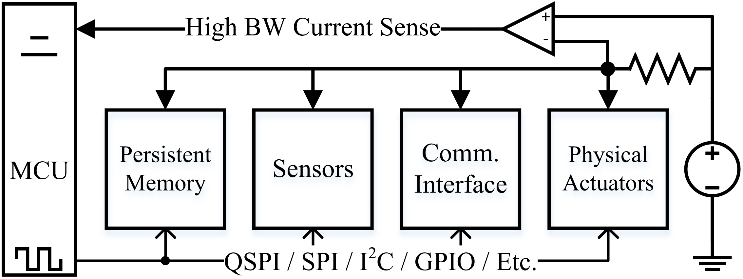
Device manufacturers derive and specify the worst-case operation duration by summing exacerbating factors including age, temperature and voltage. Using the worst-case operation time as a naïve guideline, the energy consumption of a given operation is characterized by (1).

Figure : System Diagram

|  |  |
| --- | --- |
|  | (1) |

Where and are the time and power comprising the actual operation while and are the time and power comprising the period between operation completion and the worst-case execution time.

Most peripheral devices provide a mechanism for signaling that operations completed earlier than the maximum. However, using these mechanisms results in sub-optimal power performance. For example, a common method of detecting write completion on external non-volatile memory relies on polling a status register. Performing this method has the following power and energy consequences:

|  |  |
| --- | --- |
|  | () |
|  | (3) |

* : MCU must be active while polling
* : MCU communications driver must be active
* : Communications incurs penalty
* : MCU and device voltages must be matched.
  + Neither can use dynamic voltage scaling
* : Device communications driver must be active

Of course, the optimal energy expenditure on an operation is simply As the energy cost of computation continues to decrease in modern microcontrollers, it becomes more rewarding to use onboard intelligence to minimize system-level energy consumption. PACER develops adaptive timing, current usage and charge consumption heuristics for estimating early completion of peripheral operations, thus reducing total latency and energy consumption.

The estimate is verified in real-time and the heuristic is updated with the results. In this fashion, the algorithms are resistant to variations in behavior that may occur across the lifecycle of the device. PACER is evaluated against a variety of embedded peripherals and is shown to significantly decrease both energy consumption and latency of peripherals with minimal computational overhead.

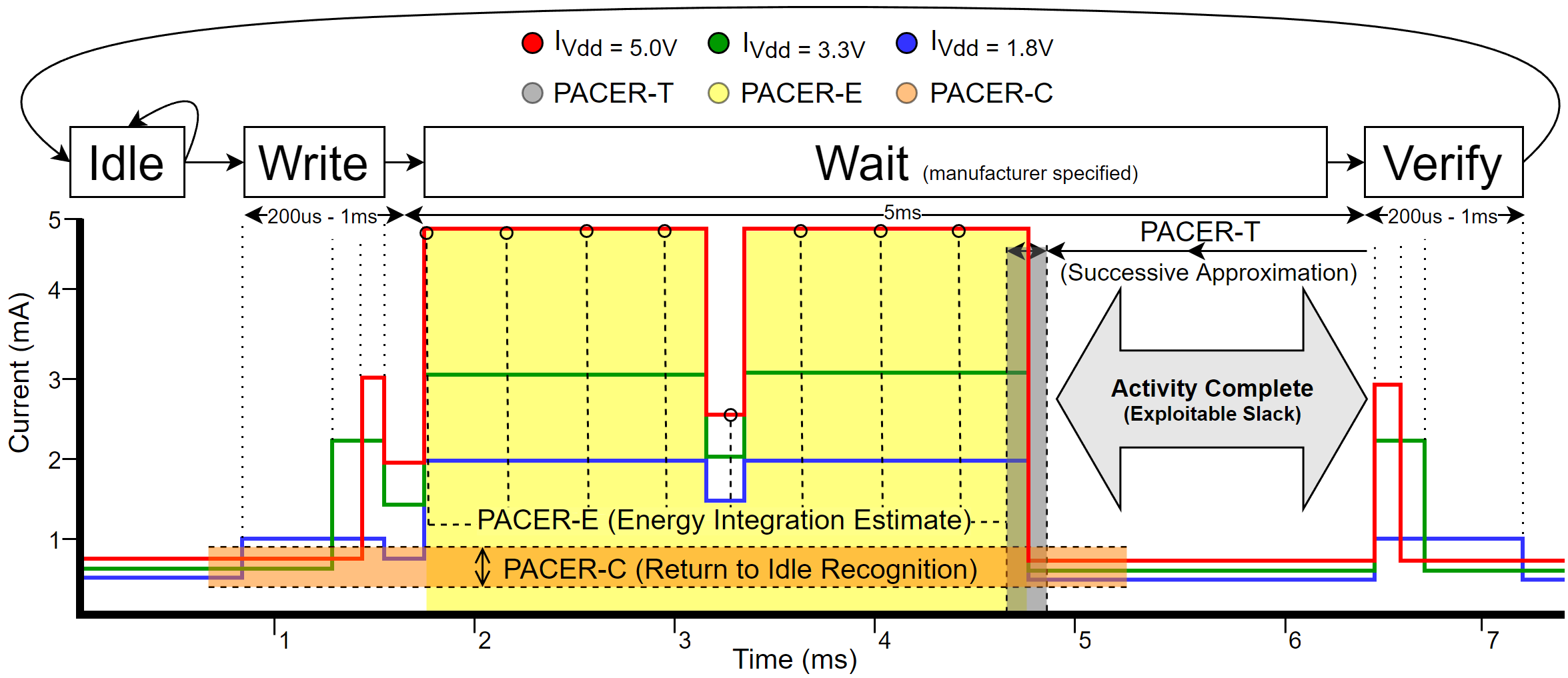
For example, when writing a page of EEPROM a voltage-independent wait state is encountered that is specified to a maximum duration of 5ms. However, that specification is for the worst case and is more suitable for a timeout value. The current consumption profile of an EEPROM write operation at varying voltages is shown in **Error! Reference source not found.**. As the device transitions through the Idle 🡪 Write 🡪 Wait 🡪 Verify states, it can be inferred from the current profile that the operation completed by the 5ms mark and that it was not necessary to delay until approximately 6.5ms per the specification.

Figure : A Typical External Memory Transaction with IODVS and PACER

In the case of EEPROM and most peripheral devices, a register is provided which indicates when the write has completed. Polling this register requires the MCU to communicate with the peripheral and thus results in transitioning to a voltage-dependent state. Thus, accurate estimations can decrease latency and energy consumption, but inaccurate estimates can result in an early transition to a voltage-dependent state and thus increase energy consumption.

There are a wide variety of peripheral devices with a correspondingly wide variety of completion determinism and current profiles. Devices with highly deterministic timing respond best to the timing heuristic while those with variable timing respond best to current or charge heuristics.

PACER seeks to estimate and detect early completion of operations in peripheral devices by applying timing and current usage heuristics. Through early completion detection, ACR is able to decrease both latency and system-wide energy consumption. PACER is particularly advantageous to systems implementing IODVS by decreasing the effective duration of voltage-independent states.

Related Work

Intra-Operation Dynamic Voltage Scaling [1] (IODVS) has been shown to significantly reduce the energy consumption of embedded peripherals (Flash, EEPROM, sensors, etc.) during their voltage-independent states. These states typically occur during mandatory delay periods as the device completes a specified operation. Peripheral Activity Completion Estimation and Recognition (PACER) seeks to further reduce system-wide energy consumption and decrease peripheral latency by recognizing the completion of the voltage-independent state and thus completing the overall operation early.

We propose three considerably different methods to decrease peripheral latency by detecting activity-complete.

## Timing Heuristic

Peripheral operations can vary in their latency or completion times due to a number of factors. Temperature can significantly affect the completion time for peripherals with deterministic timing requirements such as DRAM [2]. Device aging can also affect timing due to a number of issues resulting from fundamental semiconductor physics [3]. Furthermore, some devices simply have non-deterministic completion times due to features such as MMUs and caches that are implemented in various data storage devices like Micro-SD cards, or age and wear as they effect FLASH storage timing.

Because the latency can vary significantly between operations, it is necessary to develop a timing heuristic that can adapt to slowly changing effects like age and temperature as well as rapidly changing factors like cache hits and misses. Adaptive delay estimation is not a new problem [4] and research continues to compensate for non-deterministic delay with different approaches for wireless communications, control systems and mass storage latency [5].

## Energy Heuristic

For devices with highly variable timing and dynamic current consumption characteristics, integrating the current consumption of the device throughout an operation can allow for better detection of completion. Some operations can be characterized by the amount of charge necessary to complete them. This technique is referred to as “coulomb counting” and is a common technique used to determine the state of charge in rechargeable batteries [6].

## Current Heuristic

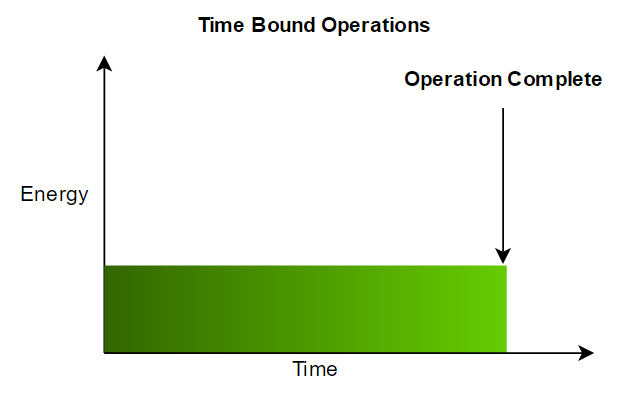
The completion of some peripheral operations are easily detectable by their current consumption profile. These devices have a distinct and deterministic current profile that can be characterized and used to estimate the moment when an operation completes.

Simple and differential power analysis (SPA and DPA) attacks are performed by monitoring device current consumption with very fine grained detail. These attacks seek to undermine encryption techniques by monitoring the current consumption of the processor and detecting the moment at which the processor executes a branch operation [7]. The attacks have been performed on an ARM Cortex MCU using AES and required an extensive measurement setup to accomplish [8]. PACER is inspired by this previous work using fine-grained in-circuit current measurement and fortunately benefits from much more lenient sampling requirements.

# Methods

## Timing Heuristic PACER-T

The PACER-T algorithm uses a successive binary approximation algorithm to determine the optimal delay latency for an operation. The algorithm begins by executing an operation with the amount of delay specified in the device datasheet. After each iteration, if the operation was successful, then the amount of delay is halved. Otherwise, the operation resulted in an error and the next delay is increased by half the distance to the last previously successful operation.

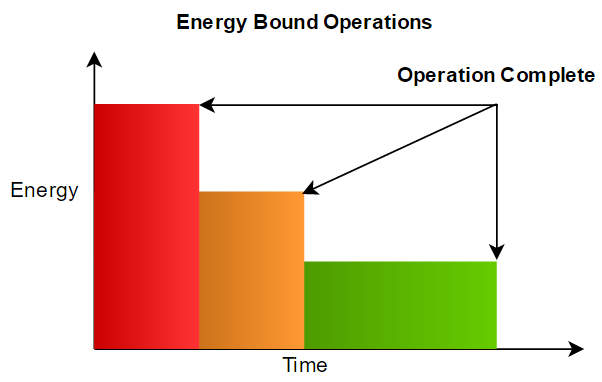


Figure

The algorithm is executed online and provides the tightest possible timing. In fact, the timing is so precise that it should be considered marginally stable. To account for extremely small variations in timing, for instance due to clock jitter or internal peripheral asynchronous operation, the minimum delay found by PACERT-T is increased by 5% in the following tests. This value was not optimized and may even be much smaller. It would likely be beneficial for a system using this algorithm to re-characterize the peripheral device periodically in order to account for temperature variations.

## Energy Heuristic PACER-E

The energy based heuristic was performed in much the same way as the timing heuristic. The system aggregates all output current samples from the power supply consumed by the peripheral device. When the digital integration has reached the test value, the operation is ‘complete’ and checked for correctness.



This algorithm is intended for use in devices that consume a constant amount of energy per operation. It compensates for devices that are energy bounded rather than time-bounded.

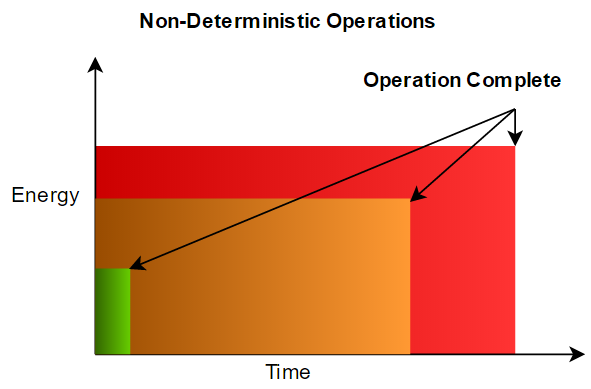
The algorithm uses a successive binary approximation in the same fashion as PACER-T in order to determine the exact amount of energy required to perform an operation. PACER-E is somewhat less precise than the timing based algorithm due to the time required to both sample and perform the digital integration necessary for threshold checking.

The energy consumed throughout a test is calculated using the fundamental relationship shown in (4). The results were calculated offline via (5) and (6), where S is the state of the device, and Ts is the sampling period.

|  |  |
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## Current Heuristic PACER-C

The charge algorithm is also performed online and makes use of the current profile in order to determine if an operation has completed. The algorithm begins by taking a sample of the power supply output current. Next, the operation is executed and is not considered complete until the output current returns to some percentage of its previous state.



For instance, if the output current were measured to be 1mA before the operation began, and assuming that the operation will result in some increase in current, it is logical to wait until the current is once again at 1mA before polling the peripheral device for operation completion.

PACER-C is the most basic method to determine in real time if an operation has completed and may also be prone to false positives in some cases. There are many more advanced algorithms that can suit the purpose such as a multi-layer perceptron that is used in neural networks. It is notable however, that reducing the complexity of the detector is very important so that the algorithm can ensure that it is maintaining pace with incoming samples. Naturally, more complex algorithms could be accommodated by a more powerful host microcontroller.

# Materials

PACER and IODVS are hosted on a STM32F429 MCU implemented on the STMicroelectronics DISCO board and hosted by the PRIME assembly. The board provides 64MB of SDRAM which allows for simultaneous sampling throughout the test suite at very high speed. All experiments were sampled at 1MSPS and the SDRAM allowed any individual experiment to last up to 1 full second. All of the analog conversions as well as the device state sampling were performed via DMA. Therefore, the test fixture is expected to have had no impact on the operation under test.

The PRIME (Precise Real-Time In-Circuit Micro-EMS) hosts a variety of peripherals commonly implemented in embedded designs. The board provides access to Bluetooth, Wi-Fi and a Si1143 proximity detector. PACER was evaluated on NAND and NOR FLASH memories, as well as a commercial EEPROM, temperature / humidity sensor and four independent Micro-SD cards.

At 1 MSPS and 4 channel measurements and 2 bytes per sample, each test can result in up to 8 megabytes of data. Because repeatability is so important, each test was run 50 times. Therefore, bandwidth became a limiting factor and a Hi-Speed (480mbps) USB module was added to the board to allow for rapid development. Operating as a virtual communications port, actual bandwidth was realized at approximately 120mbps.

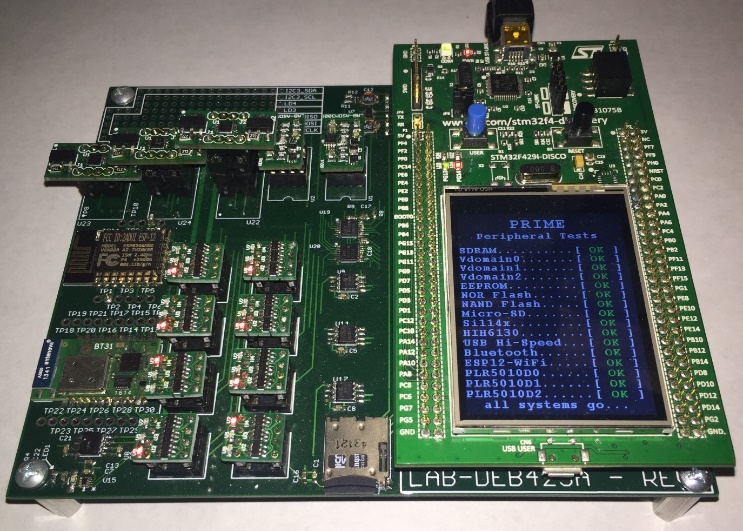


Figure : PRIME (Precise Real-Time In-Circuit Micro-EMS)

Each of the peripheral devices under test has some method of determining if an operation completed successfully. For the memory devices, a simple read-back verification is sufficient to determine correctness and is a common practice among embedded designs. The temperature and humidity sensor provides a status bit indicating if an operation is in progress, thus indicating that a requested operation has not yet completed.

Recall that when implementing IODVS, that the host MCU and peripheral devices are placed on different voltage domains throughout the course of the voltage-independent state. Because of this, it is not possible for the MCU to poll the peripheral device for operation completion. Polling is also shown to be a rather costly operation in and of itself. Without the ability to communicate to the peripheral device, PACER uses other methods to best judge operation completeness.

Power can be provided and modulated to each individual device on the domain using independently configurable power supplies. The ASDM-300F module provides a high-efficiency buck power supply, followed by a linear regulator with a high ripple-rejection ratio. A high-precision clean power supply is extremely important because PACER uses the current profile to make real-time decisions. If the power supply outputs a significant amount of noise, then it becomes more and more difficult to determine activity completion.

The ASDM-300F is also outfitted with a dual current measurement circuit using the Maxim MAXZZZ. This circuit allows the host to measure both the input and output current of the power supply with high analog bandwidth. Ultimately, these outputs are used to determine activity completion with the PACER-E and PACER-C algorithms. It is important to note the gain-bandwidth product of the MAX. High frequency content will be attenuated to some degree and the actionable data output would be of higher quality if a higher frequency device were available.

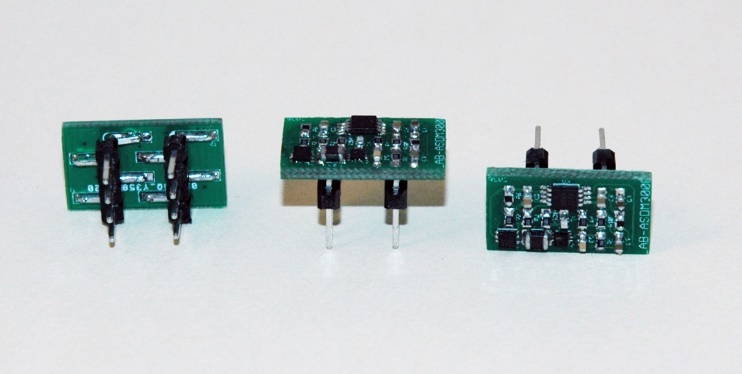


Figure : ASDM300F (Adjustable Step-Down Module with Feedback)

While measuring and classifying activity completion, it is important that each device be analyzed independently. The PPS-330D allows the host to switch the voltage domain of an individual peripheral to any one of three domains, or disconnect the device entirely (including the ground connection).

The PPS-330D devices are connected to each peripheral, and when a peripheral is under test, the other devices are switched to an alternate voltage domain. Thus, each device is can be independently classified in-system without removing other devices that may contribute to the current measurements.

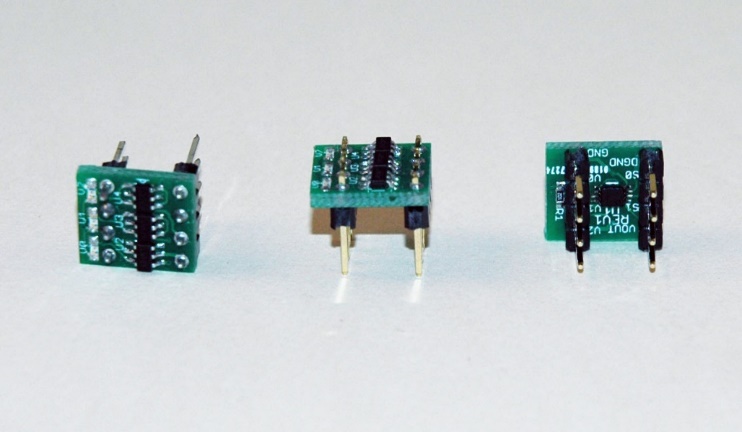


Figure : PPS-330D Peripheral Power Switch with Disconnect

# Results

Initial IODVS results were repeated so as to establish a baseline with which to compare the results of PACER. Previous experiments required the results to be averaged many times over. The PRIME assembly provides high enough signal to noise ratio that averaging multiple test results is unnecessary and a simple 50-sample moving average provides enough noise cancellation while maintaining a quick response time.

## MCP25AA512 EEPROM

The Microchip EEPROM is specified by the manufacturer for a 5ms mandatory wait period following the write command and data. This operation is highly deterministic with respect to time, energy and current profile. All PACER algorithms identified activity completion with a high degree of accuracy.





Figure : EEPROM Write Cycle Using IODVS and PACER-T

As can be inferred from the current profile, the EEPROM write operation appears to complete at approximately the 5ms mark of Figure 7 instead of the 6.5ms mark as is specified by the manufacturer. After applying the PACER-T algorithm, it is indeed true that the operation was complete at the 5ms mark, thus reducing the wait latency by 30%.

The PACER-E and PACER-C algorithms were also successful in identifying activity completion. The two algorithms do require additional computation to integrate or otherwise observe the current profile and therefore PACER-T is the best choice in this application, given identical performance.

## Numonyx M25PX16 NOR Serial Flash

NOR flash modules sacrifice byte-wise modification for overall capacity. In this fashion, the M25PX16 presents 16MBits of capacity in a small package, but the host must erase sub-sectors of flash (4K) to enable writes to pages of flash (128B). To perform a read-modify-write operation, one must read the contents of a sub-sector, modify the contents locally, erase the sub-sector in flash and finally write the modified contents back to the flash on a page-by-page basis.

Both the sub-sector erase and page write have a worst-case mandatory wait period specified by the manufacturer.





Figure : NOR Serial Flash Write Cycle Using IODVS and PACER-T

Although specified for 150ms, the initial sub-sector erase appears to complete at approximately 65ms after it begins. Page writes are specified for a worst-case completion time of 10ms but through the application of PACER-T, it is shown that they complete much faster.

## Microchip SST26VB Serial NAND Flash

NAND flash modules sacrifice byte-wise reads for the sake of overall capacity. The serial flash module must therefore read an entire page of flash into a local buffer before providing read data to the host. This can result in non-deterministic read and write access times.

As shown in Figure 9, the manufacturer specified erase time

|  |  |  |  |
| --- | --- | --- | --- |
| Stage | Mfg. Spec. | PACER-T | Diff. |
| Erase (4KB) | 25ms |  |  |
| 16x Write (256B) | 2ms |  |  |
| Total | 49ms |  |  |





Figure : NAND Serial Flash Write Cycle Using IODVS and PACER-T





Figure : A Micro-SD Card Cache Miss and a Cache Hit

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# Conclusions

Note that the “Active Total” items in the following tables encompass the test results ignoring the idle state contributions to both time and energy. The idle state is a byproduct of the test and in actual usage could be any arbitrary value. The value would be incorporated into the duty cycle discussion that was investigated in the results of IODVS.

# References

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| --- | --- |
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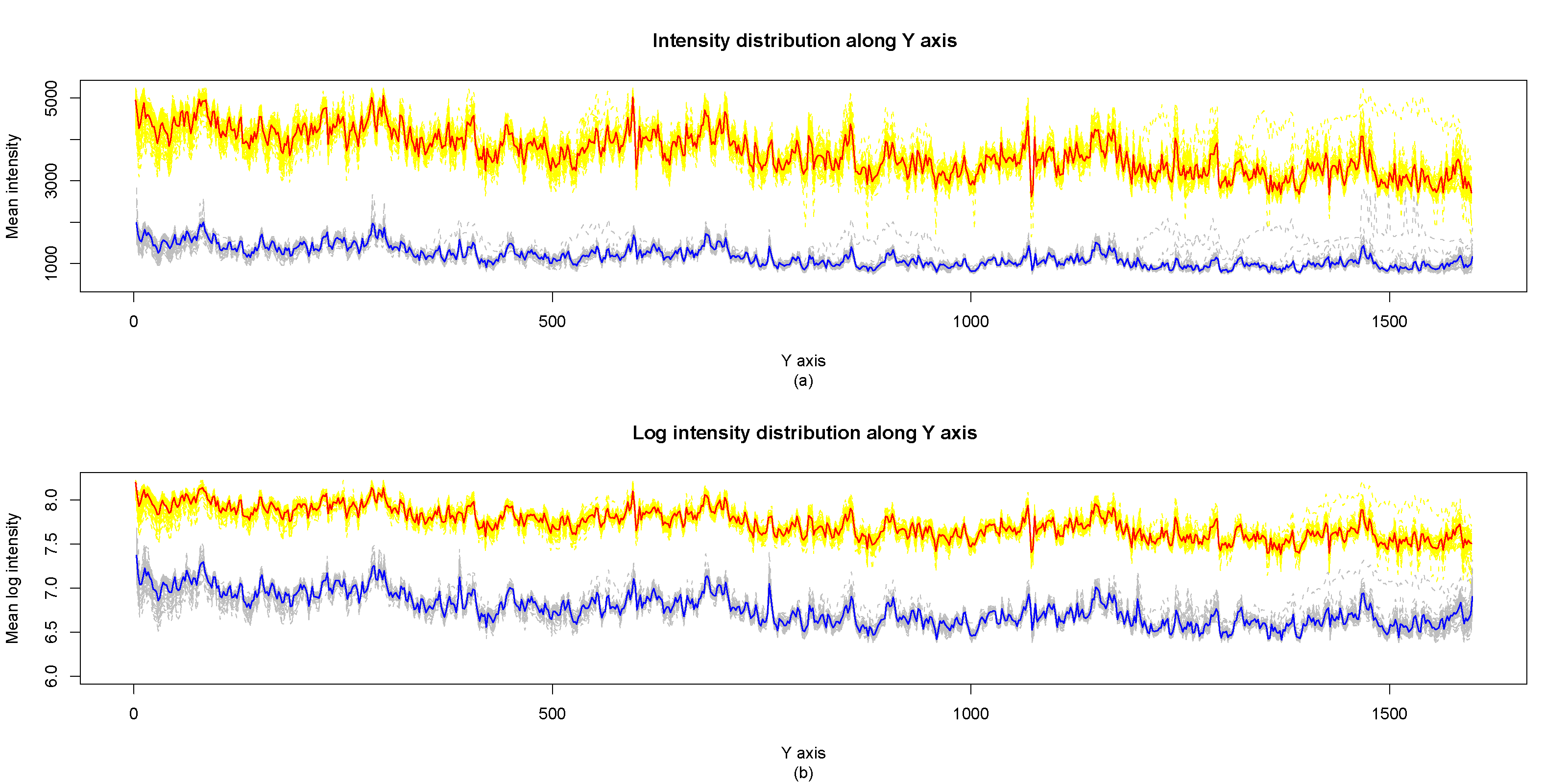
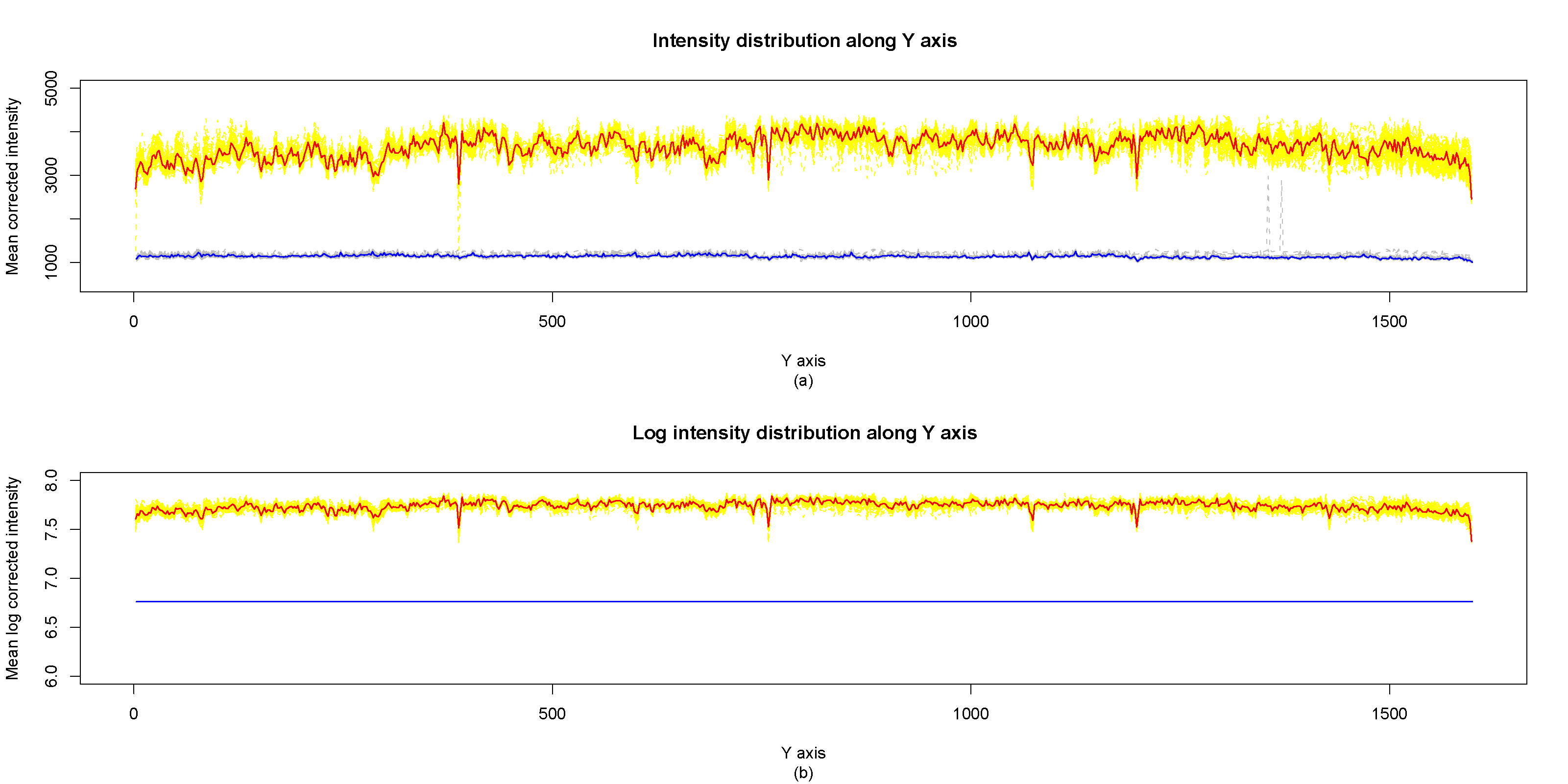
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1. A. Kito, Y. Mizumachi, K. Sato, Y. Matsuoka, “Emergent Design System Using Computer-Human Interactions and Serendipity” The Sixth International Conference on Advances in Computer-Human Interactions (ACHI 2013) IARIA, Feb. 2013, pp. 7-12, ISSN: 2308-4138, ISBN: 978-1-61208-250-9
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1. Example of a TWO-COLUMN figure caption: (a) this is the format for referencing parts of a figure.