PACER

Peripheral Activity Completion Estimation and Recognition

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*Abstract*—Embedded peripheral devices such as memories, sensors and communications interfaces are used to perform a function external to a host microcontroller. The device manufacturer typically specifies worst-case current consumption and latency estimates for each of these peripheral actions. Peripheral Activity Completion, Estimation and Recognition (PACER) is introduced as a variety of algorithms that can be applied to detect completed peripheral operations in real-time. By detecting activity completion, PACER enables the host to exploit slack between the worst-case estimate and the actual response time. These methods were tested independently and in conjunction with IODVS on multiple common peripheral devices. For the peripheral devices under test, the test fixture confirmed decreases in energy expenditures of up to 62% and latency reductions of up to 67%.

Keywords-Embedded Systems; Dynamic Voltage Scaling (DVS); Dynamic Power Management (DPM); low-power; low-energy; wireless sensor node (WSN); timing and performance analysis; energy-aware design; power aware embedded computing; adaptive embedded systems.

# Introduction

Embedded systems are often constrained by timing and energy budgets because both factors affect the resultant cost and size of the system. Peripheral devices external to the microcontroller (MCU) such as those shown in Figure 1 can play a significant role in system-wide energy consumption. There are many methods available for decreasing the static power usage of peripherals [1] [2] [3]. PACER decreases dynamic power consumption and latency by exploiting the slack between actual versus worst-case operation time.

Device manufacturers derive and specify the worst-case operation duration by summing exacerbating factors including age, temperature and voltage. Using the worst-case operation time as a naïve guideline, the worst-case energy consumption of a given operation is characterized by (1).

|  |  |
| --- | --- |
|  | (1) |

Where and are the time and power comprising the actual operation while and are the time and power comprising the period between operation completion and the worst-case execution time.

Most peripheral devices provide a mechanism for signaling that operations completed earlier than the maximum. However, using these mechanisms results in sub-optimal power performance. For example, a common method of detecting write completion on external non-volatile memory relies on polling a status register. Performing this signaled method has power and energy consequences:

|  |  |
| --- | --- |
|  | (2) |

* : MCU must be active while polling
* : MCU communications driver must be active
* : Communications incurs penalty
* : MCU and device voltages must be matched.
  + Neither can use dynamic voltage scaling
* : Device communications driver must be active

|  |  |
| --- | --- |
|  | (3) |

The components of are highly variable between systems and devices. The complexity of the signal may involve protocol-level communication or may be as simple as an interrupt pin and that signal may traverse PCB traces with considerable capacitance.

Both interface methods incur a power penalty and the naïve worst-case method also incurs a latency penalty. As the energy cost of computation continues to decrease in modern microcontrollers, it becomes more rewarding to use onboard intelligence to minimize the impact of power and latency penalties. PACER develops adaptive timing, current usage and charge consumption heuristics for estimating or recognizing early completion of peripheral operations, thus reducing total latency and energy consumption.

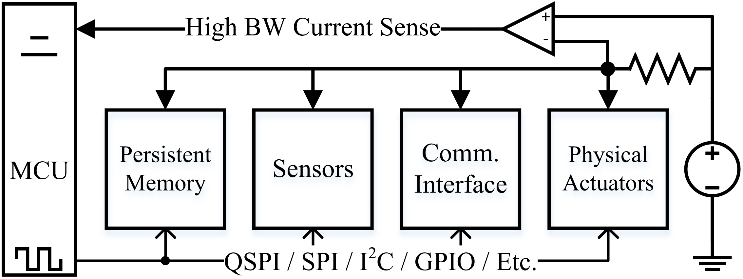
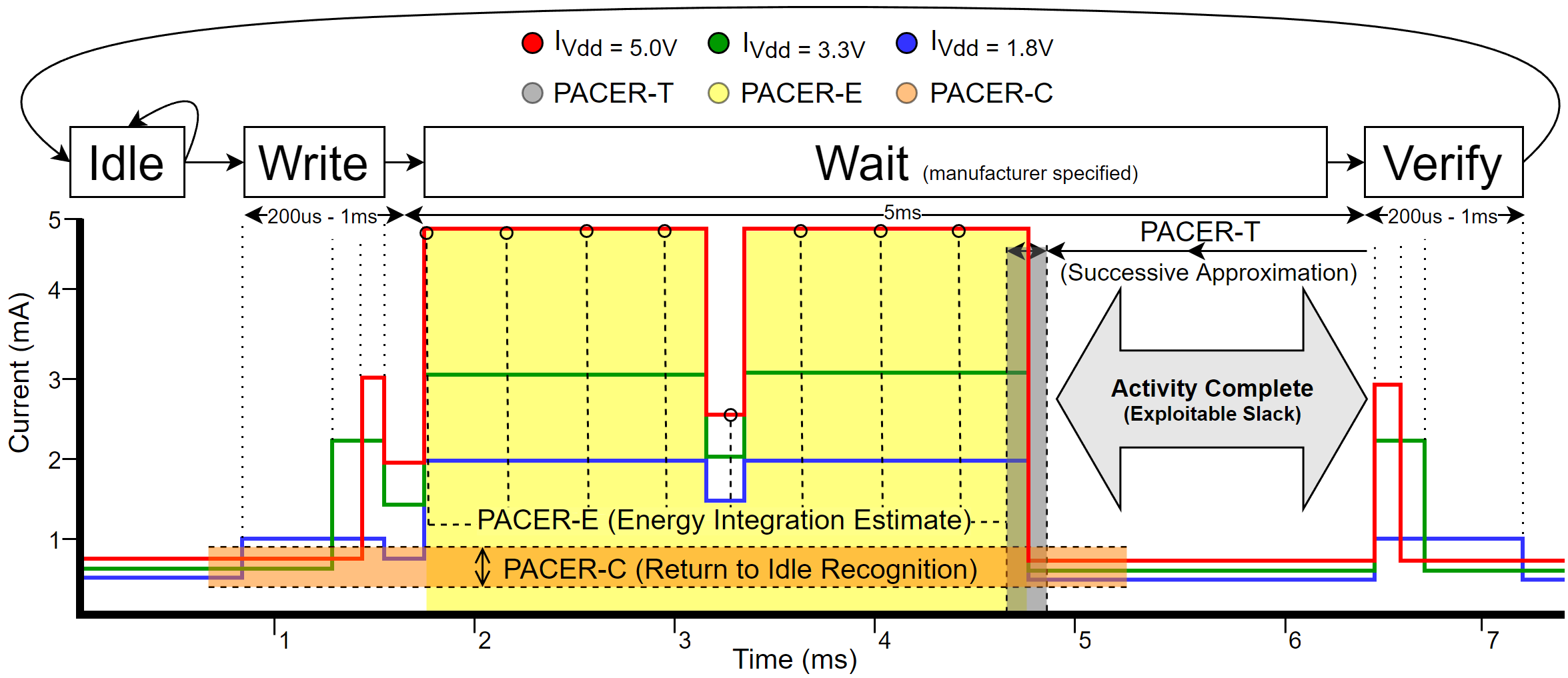
The prediction is verified in real-time against the actual state and the heuristic is updated with the results. In this fashion, the algorithms are resistant to variations in behaviorthat may occur across the lifecycle of the device. PACER is evaluated against a variety of embedded peripherals and is shown to significantly decrease both energy consumption and latency of peripherals with minimal computational overhead.

Figure 1: System Diagram

Figure 2: A Typical External Memory Transaction with IODVS and PACER

Consider that the peripheral operation of writing a page of EEPROM is specified with a worst-case duration of 5ms. The current consumption profile of an EEPROM write operation at varying voltages is shown in Figure 2. As the device transitions through the Idle 🡪 Write 🡪 Wait 🡪 Verify states, it can be inferred from the current profile that the operation completed by the 5ms mark and that it was not necessary to delay until approximately 6.5ms per the specification.

There are a wide variety of peripheral devices with a correspondingly wide variety of completion determinism and current profiles. PACER introduces three methods by which the host MCU can estimate or detect early completion of peripheral operations while also minimizing computational overhead. Devices with highly deterministic timing respond best to the timing heuristic while those with variable timing respond best to current or charge heuristics. Through low-overhead early completion detection, PACER is able to decrease both latency and system-wide energy consumption.

# Related Work

Intra-Operation Dynamic Voltage Scaling [1] (IODVS) has been shown to significantly reduce the energy consumption of embedded peripherals (Flash, EEPROM, sensors, etc.) during their voltage-independent states. These states typically occur during mandatory delay periods while the peripheral completes a specified operation. When implementing IODVS, the host MCU and peripheral devices are placed on different voltage domains throughout the course of the voltage-independent state. Because of this, it is not possible for the MCU to poll the peripheral device for operation completion. Polling is also shown to be a rather costly operation due to (2) and (3). Without the ability to communicate to the peripheral device, PACER is necessary to achieve minimal operation latencies.

## Timing Heuristic

Peripheral operations can vary in their latency or completion times due to a number of factors. Temperature can significantly affect the completion time for peripherals with deterministic timing requirements such as DRAM [2]. Device aging can also affect timing due to a number of issues resulting from fundamental semiconductor physics [3]. Furthermore, some devices simply have non-deterministic completion times due to features such as MMUs and caches that are implemented in various data storage devices like Micro-SD cards, or age and wear as they effect FLASH storage timing.

Because the latency can vary significantly between operations, it is necessary to develop a timing heuristic that can adapt to slowly changing effects like age and temperature as well as rapidly changing factors like cache hits and misses. Adaptive delay estimation is not a new problem [4] and research continues to compensate for non-deterministic delay with different approaches for wireless communications, control systems and mass storage latency [5].

## Energy Heuristic

For devices with highly variable timing and dynamic current consumption characteristics, integrating the current consumption of the device throughout an operation can allow for better detection of completion. Some operations can be characterized by the amount of charge necessary to complete them. This technique is referred to as “coulomb counting” and is a common technique used to determine the state of charge in rechargeable batteries [6].

## Current Heuristic

The completion of some peripheral operations are easily detectable by their current consumption profile. These devices have a distinct and deterministic current profile that can be characterized and used to estimate the moment when an operation completes.

Simple and differential power analysis (SPA and DPA) attacks are performed by monitoring device current consumption with very fine grained detail. These attacks seek to undermine encryption techniques by monitoring the current consumption of the processor and detecting the moment at which the processor executes a branch operation [7]. The attacks have been performed on an ARM Cortex MCU using AES and required an extensive measurement setup to accomplish [8]. PACER is inspired by this previous work using fine-grained in-circuit current measurement and fortunately benefits from much more lenient sampling requirements.

# Methods

## Timing Heuristic PACER-T

Some peripheral operations exhibit highly deterministic timing qualities. Such a device is likely to be internally clocked and the operation is waiting for some number of clock cycles to expire before signaling that the operation completed. Such operations are typified Figure 3 in that neither the total energy consumed, nor the profile of that consumption are necessary in order to predict completion. Regardless of the power profile, the operation always completes within a narrow window of time. Erases and write operations to EEPROM and flash are typical examples of this behavior.

PACER-T uses the successive approximation algorithm shown in (4) to determine the optimal delay for an operation. The algorithm begins by executing an operation with the amount of delay specified in the device datasheet. After each iteration, if the operation was successful, then the amount of delay is halved. Otherwise, the operation resulted in an error and the next delay is increased by half the distance to the last previously successful operation.

|  |  |
| --- | --- |
|  | (4) |

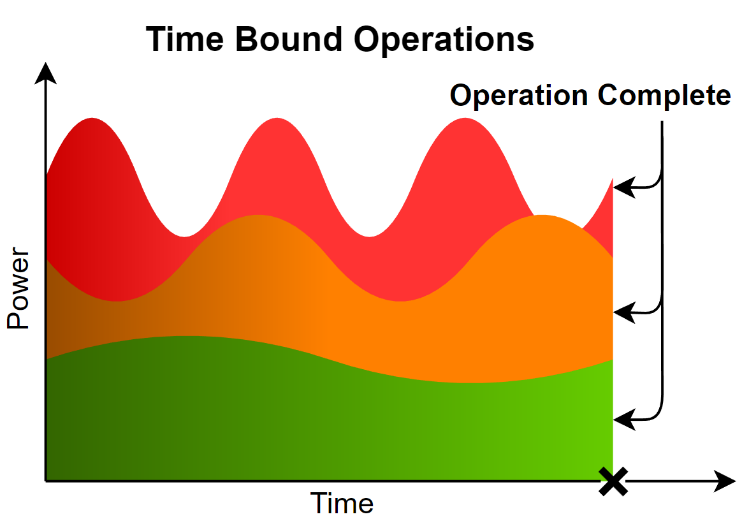


Figure 3: Profile of a Time-Deterministic Operation

The algorithm is executed online and provides the tightest possible timing. In fact, the timing is so precise that it should be considered marginally stable. To account for extremely small variations in timing, for instance due to clock jitter or internal peripheral asynchronous operation, the minimum delay found by PACERT-T is increased by 5% in the following tests. This value was not optimized and may even be much smaller. It would likely be beneficial for a system using this algorithm to re-characterize the peripheral device periodically in order to account for temperature variations.

## Energy Heuristic PACER-E

Operations that consume a deterministic amount of energy are better characterized by PACER-E. For example, the operation might involve the charging of a storage element such as an inductor or capacitor. In any case, a certain amount of energy is required to complete the operation and once that energy requirement has been satisfied, the peripheral device considers the operation to be complete. Figure 4 is an example of an energy bound operation.

The energy based heuristic was performed similarly to PACER-T in that successive approximation is used. The system multiply-accumulates voltage and current samples fed to the peripheral device. When the digital integration has reached the test value, the operation is ‘complete’ and checked for correctness. The mechanics of (4) are applied to PACER-E, except that all T limits are replaced with E energy limits. PACER-E is slightly less precise than the timing based algorithm due to the time required to both sample and perform the digital integration necessary for threshold checking.

The energy consumed throughout a test is calculated using the fundamental relationship shown in (5). The results were calculated offline via (6) and (7), where S is the state of the device, and Ts is the sampling period.

|  |  |
| --- | --- |
|  | (5) |
|  | (6) |
|  | (7) |

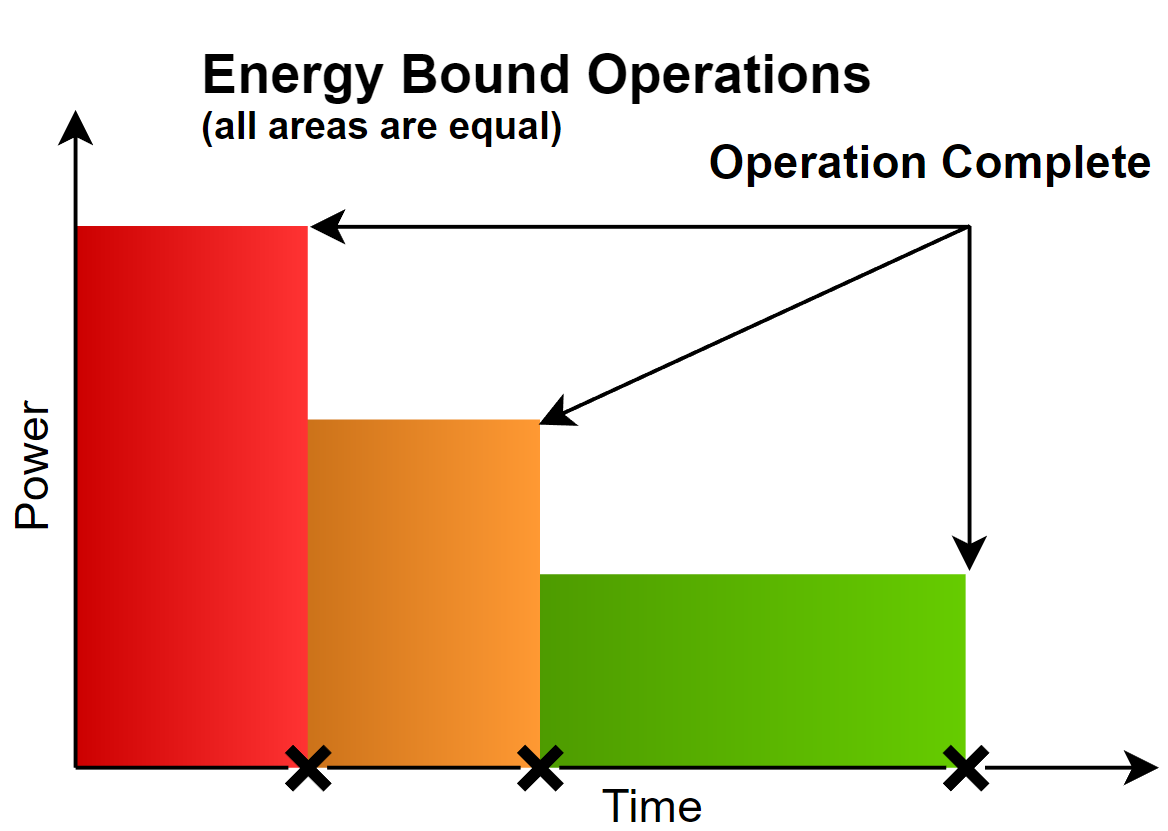


Figure 4: Profile of an Energy-Deterministic Operation

## Current Heuristic PACER-C

Figure 5: Profile of a Non-Deterministic Operation

Some operations cannot reliably be defined in terms of time nor energy. One example of a non-deterministic operation would be communications tasks performed by Ethernet or wireless devices that have non-deterministic transmissions latencies. Another example would be memory devices that incorporate an onboard memory hierarchy. In such devices, operations are affected by cache latencies.

PACER-C provides recognition that the operation is complete by measuring the idle current usage of the device before the operation begins and marking the operation as complete after the current returns to idle. In order to accommodate operations where the current returns to idle and yet the operation has not yet completed, the algorithm incorporates both a minimum latency and an idle current percent threshold to mark the operation as complete.

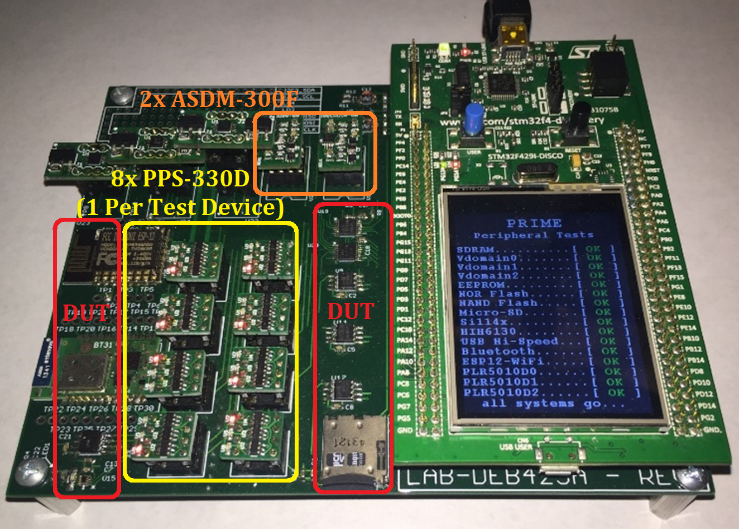
*Algorithm* 1: *PACER-C*

1: ICT = (Idle Current Measurement) \* threshold

2: Execute Operation

2: **While (**t < Minimum Latency) and (I > ICT) **then**

3: I = Current Measurement

4: **End While**

PACER-C is described by Algorithm 1 and begins by taking a sample of the device input current while idle. Next, the operation is executed and the algorithm waits for a minimum latency period to expire. The operation is considered complete after the output current returns to the threshold percentage of its previous state. The threshold for all following experiments was set empirically at 110%.

PACER-C is the most basic method to determine in real time if an operation has completed and may also be prone to false positives in some cases. There are many more advanced algorithms that can suit the purpose such as a multi-layer perceptron that is used in neural networks that could be used to identify features in real-time. It is notable however, that reducing the complexity of the detector is important so that the algorithm can ensure that it is keeping pace with incoming samples. Naturally, more complex algorithms could be accommodated by a more powerful host microcontroller.

Figure 6: PRIME (Precise Real-Time In-Circuit Micro-EMS)

# Materials

PACER and IODVS are implemented on an STM32F429 MCU supported by the STMicroelectronics DISCO board and hosted by the PRIME assembly. The board provides 64MB of SDRAM which allows for simultaneous sampling throughout the test suite at very high speed. All experiments were sampled at 1MSPS and the SDRAM allowed any individual experiment to last up to 1 full second. All of the analog conversions as well as the device state sampling were performed via DMA. Therefore, the test fixture is expected to have had no impact on the operation under test.

The PRIME (Precise Real-Time In-Circuit Micro-EMS) board, shown in Figure 6, hosts a variety of peripherals (labelled in red as DUT: Devices Under Test) that are commonly implemented in embedded designs. The board provides access to Bluetooth, Wi-Fi and a Si1143 proximity detector. PACER was evaluated on NAND and NOR FLASH memories, as well as a commercial EEPROM, temperature / humidity sensor and four independent Micro-SD cards.

At 1 MSPS and 4 channel measurements and 2 bytes per sample, each test can result in up to 8 megabytes of data. Because repeatability is so important, each test was run 50 times. Therefore, bandwidth became a limiting factor and a Hi-Speed (480mbps) USB module was added to the board to allow for rapid development. Operating as a virtual communications port and using MCU parallel bus, actual bandwidth was realized at approximately 120mbps.

Each of the peripheral devices under test has some method of determining if an operation completed successfully. For the memory devices, a simple read-back verification is sufficient to determine correctness and is a common practice among embedded designs. The temperature and humidity sensor provides a status bit indicating if an operation is in progress, thus indicating that a requested operation has not yet completed.

Power is provided and voltage is modulated to each individual device on the domain using independently configurable power supplies. The ASDM-300F module shown in orange on Figure 6 provides a high-efficiency buck power supply, followed by a linear regulator with a high ripple-rejection ratio. A high-precision and clean power supply is extremely important because PACER uses the current profile to make real-time decisions. If the power supply outputs a significant amount of noise, then it becomes difficult to acquire signal and determine activity completion in real-time.

The ASDM-300F is also outfitted with a dual current measurement circuit using the Maxim MAX4377HAUA+. This circuit allows the host to measure both the input and output current of the power supply with high analog bandwidth. Ultimately, these outputs are used to determine activity completion with the PACER-E and PACER-C algorithms. It is important to note the gain-bandwidth product of the amplifier. High frequency content will be attenuated to some degree and the actionable data output would be of higher quality if a higher frequency device were available.

While measuring and classifying activity completion, it is important that each device be analyzed independently. The PPS-330D shown in yellow on Figure 6 allows the host to switch the voltage domain of an individual peripheral to any one of three domains, or disconnect the device entirely (including the ground connection). Once the devices are characterized independently, then their individual contributions to the overall power supply current output can be deduced through superposition.

The PPS-330D devices are connected to each peripheral, and when a peripheral is under test, the other devices are switched to an alternate voltage domain. Thus, each device is can be independently classified in-system without removing other devices that may contribute to the current measurements.

# Results

Initial IODVS results were repeated so as to establish a baseline with which to compare the results of PACER. Previous experiments required the results to be averaged many times over. The PRIME assembly provides high enough signal to noise ratio that averaging multiple test results is unnecessary and a simple 50-sample moving average provides enough noise cancellation while maintaining a quick response time.

## MCP25AA512 EEPROM

The Microchip EEPROM is specified by the manufacturer for a 5ms mandatory wait period following the write command and data. This operation is highly deterministic with respect to time, energy and current profile. All PACER algorithms identified activity completion with high accuracy.

1. MCP25AA512 EEPROM PACER Results

| Stage | Latency Results (ms) | | | | |
| --- | --- | --- | --- | --- | --- |
| Control | PACER-T | Diff. | PACER+IODVS | Diff. |
| Write | 5.05 | 3.51 | 30.5% | 3.51 | 30.5% |
| All | 5.98 | 4.44 | 25.7% | 4.44 | 25.7% |
|  | Energy Results (uJ) | | | | |
| Write | 46.84 | 37.89 | 19.1% | 27.85 | 40.5% |
| All | 53.05 | 43.91 | 17.2% | 32.40 | 38.9% |





Figure 7: EEPROM Write Cycle Using IODVS and PACER-T

It can be inferred from the current waveform that the EEPROM write operation completed at approximately the 5ms mark of Figure 9 instead of the 6.5ms mark as is specified by the manufacturer. After applying the PACER-T algorithm, it is indeed true that the operation was complete at the 5ms mark, thus reducing the wait latency by 30.5%.

The PACER-E and PACER-C algorithms were also successful in identifying activity completion. The two algorithms do require additional computation to integrate or otherwise observe the current waveform. Given identical performance, PACER-T is the best choice in this application.

## Numonyx M25PX16 NOR Serial Flash

NOR flash modules sacrifice byte-wise modification for overall capacity. The M25PX16 presents 16MBits of capacity in a small package, but the host must erase sub-sectors of flash (4K) to write pages of flash (128B). To perform a read-modify-write operation, the host must read the contents of a sub-sector, modify the contents locally, erase the sub-sector in flash and finally write the modified contents back to the flash on a page-by-page basis.

Both the sub-sector erase and page write have a worst-case delay specified by the manufacturer. PACER algorithms were run against both operations to find the comprehensive result.

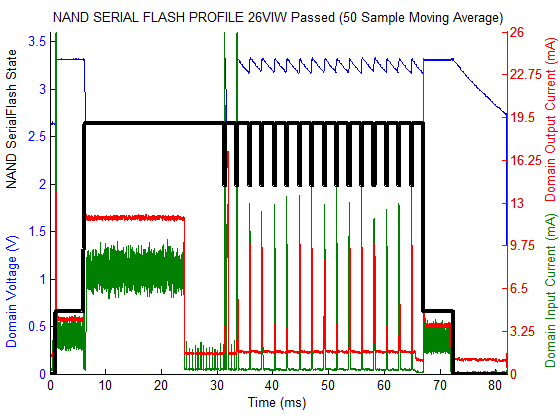
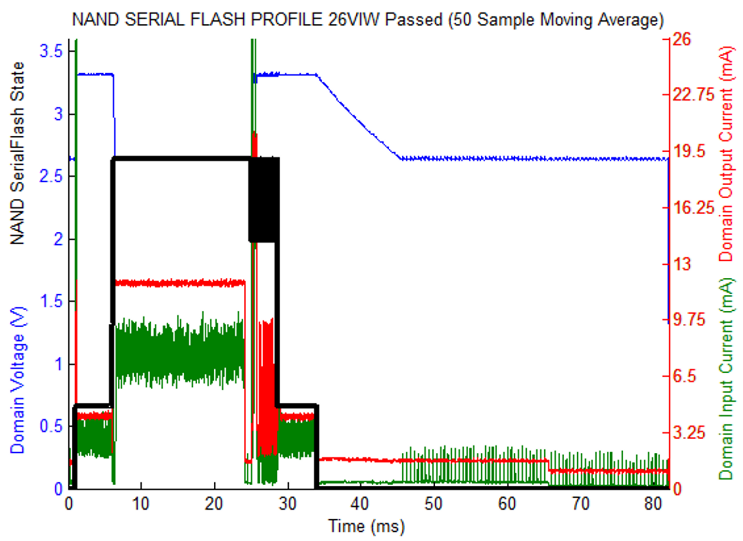




Figure 8: NAND Serial Flash Write Cycle Using IODVS and PACER-T

Figure 9: NOR Serial Flash Write Cycle Using IODVS and PACER-T

Although specified for 150ms, the current waveform indicates that the sub-sector erase completed approximately 65ms after it begins. Page writes are specified for a worst-case completion time of 10ms but through the application of PACER-T, it is shown that they complete much faster. The results are shown in Table II and the wait figure is the total amount of time spent waiting for the erase and the aggregated amount of time for each page write.

1. M25PX16 NOR Serial Flash PACER Results

| Stage | Latency Results (ms) | | | | |
| --- | --- | --- | --- | --- | --- |
| Control | PACER-T | Diff. | PACER+IODVS | Diff. |
| Wait | 231.57 | 69.47 | 70.0% | 66.92 | 71.1% |
| All | 243.87 | 82.45 | 66.2% | 80.26 | 67.1% |
|  | Energy Results (uJ) | | | | |
| Wait | 2138.3 | 1212.0 | 43.3% | 1029.52 | 51.9% |
| All | 2277.0 | 1392.0 | 38.9% | 1158.26 | 49.1% |

## Microchip SST26VB Serial NAND Flash

NAND flash modules sacrifice byte-wise reads for the sake of overall capacity. The serial flash module must therefore read an entire page of flash into a local buffer before providing read data to the host. This can result in non-deterministic read and write access times.

Sfsdfsd

1. SST26VB NAND Serial Flash PACER Results

| Stage | Latency Results (ms) | | | | |
| --- | --- | --- | --- | --- | --- |
| Control | PACER-T | Diff. | PACER+IODVS | Diff. |
| Wait | 57.61 | 19.26 | 66.6% | 19.27 | 66.6% |
| All | 71.28 | 32.94 | 53.8% | 32.95 | 53.8% |
|  | Energy Results (uJ) | | | | |
| Wait | 1053.0 | 806.2 | 23.8% | 584.87 | 44.5% |
| All | 1247.9 | 997.26 | 17.8% | 801.95 | 35.7% |

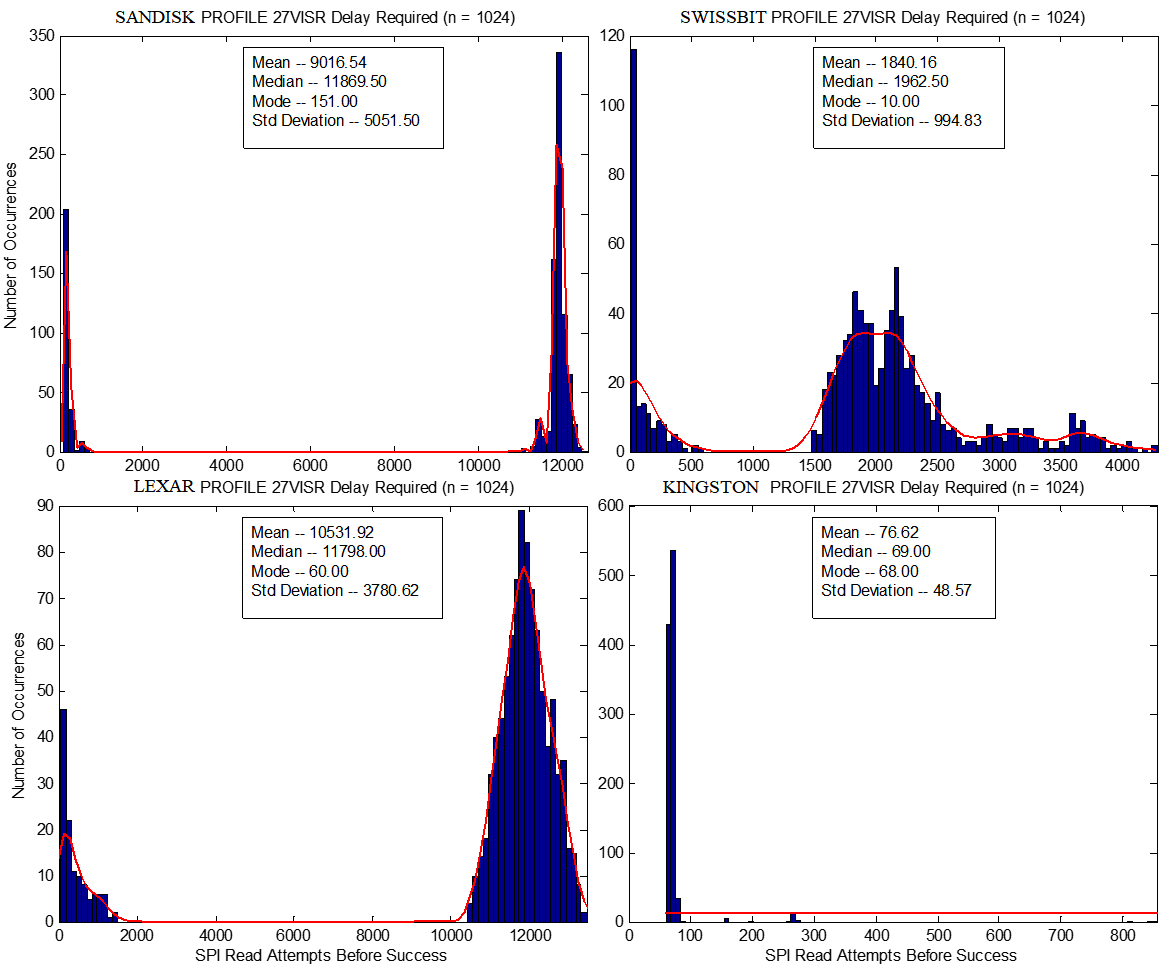


Figure 11: Timing Performance among Tested SD-Cards

Figure 10: A Micro-SD Card Cache Miss and a Cache Hit

## Various Micro-SD Memory Cards

Onboard caches and memory management units cause the write operation of Micro-SD cards to have non-deterministic timing. In this case, PACER-C is the only algorithm that can reliably detect when the operation is finished. As with all memory tests, writes were performed with random data to random addresses throughout the memory space and so the cache performance is thoroughly exercised. Figure 10 shows the power and latency difference between a cache miss and a cache hit.

Figure 11 helps to describe the performance differences shown in TABLE VI. The control delay is set to the median delay for each characterization, PACER-C allows the host to react to those operations deviating considerably from the median. Therefore, the Sandisk and Lexar cards benefitted considerably because they exhibit a bimodal timing distribution. The Swissbit card benefits decisively because of the mostly normal timing distribution and the Kingston card does not benefit much because of extremely quick and precise timing profile.

1. Micro-SD Card PACER Results

| Stage | Energy Results (uJ) | | | | |
| --- | --- | --- | --- | --- | --- |
| Control | PACER-C | Diff. | PACER+IODVS | Diff. |
| Sandisk | 17066 | 15198 | 10.9% | 11848 | 30.6% |
| Lexar | 22707 | 21428 | 5.6% | 16977 | 25.24 |
| Swissbit | 2763 | 914 | 66.9% | 554 | 80.0% |
| Kingston | 942 | 933 | 0.9% | 897 | 4.8% |

## Honeywell HIH-6130 Temperature / Humidity Sensor

The Honeywell HIH-6130 communicates via the I2C bus. The host requests the sensor to take a measurement and then waits for a specified amount of time (45ms) for the measurement to complete and is available to be retrieved. PACER-E demonstrated the best performance among the algorithms, perhaps because of the capacitive nature of the onboard ADC. The effects are shown in Figure 12 and the numeric results are presented in TABLE V.

The PACER-T algorithm also produced impressive results with a wait latency of 31.66ms and wait energy of 254.14uJ. Compared with PACER-E, the result corresponds with a *slightly* increased latency and energy consumption of 0.5% and 4.3% respectively. For some applications, the simplicity of the PACER-T implementation may be preferable when compared to the best performing PACER-E algorithm.

1. Honeywell HIH-6130 PACER Results

| Stage | Latency Results (ms) | | | | |
| --- | --- | --- | --- | --- | --- |
| Control | PACER-E | Diff. | PACER+IODVS | Diff. |
| Wait | 45.27 | 31.45 | 66.6% | 19.27 | 66.6% |
| All | 45.99 | 32.17 | 53.8% | 32.95 | 53.8% |
|  | Energy Results (uJ) | | | | |
| Wait | 325.95 | 240.29 | 26.3% | 169.62 | 48.0% |
| All | 330.50 | 245.39 | 25.8% | 173.89 | 47.4% |



Figure 12

# Conclusions

Applying the PACER suite of algorithms to a variety of common embedded peripherals resulted in significant reductions to both latency and energy consumption. The simple PACER-T algorithm performed best against time-bound operations and was very competitive in energy-bound operations. For non-deterministic operations, the PACER-C algorithm performed well. When measured against a median baseline, the algorithm performed even better as the operational latency increased in randomness.

The PACER-T and PACER-E algorithms use successive approximation and the PACER-C algorithm uses a return-to-idle measurement to determine activity completion. It is likely that the performance of both methods could be enhanced further through the application of more complex algorithms. For instance, the PACER-T could be applied to non-deterministic operations by first testing for a cache hit and then delaying for a determined cache-miss time. Likewise, the PACER-C algorithm could be modified online so as to identify the current features corresponding varying latencies.

As the cost of computation in embedded systems continues to decrease, it is natural to devote computational resources to minimizing system-wide energy consumption and latency. The PACER algorithms are presented as a suite of tools that can be deployed for such an endeavor. The algorithms are designed to require minimal computational overhead while also reacting in real-time.

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|  |  |
| --- | --- |
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* The word “data” is plural, not singular.
* The subscript for the permeability of vacuum **0, and other common scientific constants, is zero with subscript formatting, not a lowercase letter “o”.
* In American English, commas, semi-/colons, periods, question and exclamation marks are located within quotation marks only when a complete thought or name is cited, such as a title or full quotation. When quotation marks are used, instead of a bold or italic typeface, to highlight a word or phrase, punctuation should appear outside of the quotation marks. A parenthetical phrase or statement at the end of a sentence is punctuated outside of the closing parenthesis (like this). (A parenthetical sentence is punctuated within the parentheses.)
* A graph within a graph is an “inset”, not an “insert”. The word alternatively is preferred to the word “alternately” (unless you really mean something that alternates).
* Do not use the word “essentially” to mean “approximately” or “effectively”.
* In your paper title, if the words “that uses” can accurately replace the word “using”, capitalize the “u”; if not, keep using lower-cased.
* Be aware of the different meanings of the homophones “affect” and “effect”, “complement” and “compliment”, “discreet” and “discrete”, “principal” and “principle”.
* Do not confuse “imply” and “infer”.
* The prefix “non” is not a word; it should be joined to the word it modifies, usually without a hyphen.
* There is no period after the “et” in the Latin abbreviation “et al.”.
* The abbreviation “i.e.” means “that is”, and the abbreviation “e.g.” means “for example”.

An excellent style manual for science writers is [7].

# Using the Template

After the text edit has been completed, the paper is ready for the template. Duplicate the template file by using the Save As command, and use the naming convention prescribed by your conference for the name of your paper. In this newly created file, highlight all of the contents and import your prepared text file. You are now ready to style your paper.

## Authors and Affiliations

The template is designed so that author affiliations are not repeated each time for multiple authors of the same affiliation. Please keep your affiliations as succinct as possible (for example, do not differentiate among departments of the same organization). This template was designed for two affiliations.

### For author/s of only one affiliation (Heading 3): To change the default, adjust the template as follows.

#### Selection (Heading 4): Highlight all author and affiliation lines.

#### Change number of columns: Select Format > Columns >Presets > One Column.

#### Deletion: Delete the author and affiliation lines for the second affiliation.

#### For author/s of more than two affiliations: To change the default, adjust the template as follows.

#### Selection: Highlight all author and affiliation lines.

#### Change number of columns: Select Format > Columns > Presets > One Column.

#### Highlight author and affiliation lines of affiliation 1 and copy this selection.

#### Formatting: Insert one hard return immediately after the last character of the last affiliation line. Then paste the copy of affiliation 1. Repeat as necessary for each additional affiliation.

#### Reassign number of columns: Place your cursor to the right of the last character of the last affiliation line of an even numbered affiliation (e.g., if there are five affiliations, place your cursor at end of fourth affiliation). Drag the cursor up to highlight all of the above author and affiliation lines. Go to Format > Columns and select “2 Columns”. If you have an odd number of affiliations, the final affiliation will be centered on the page; all previous will be in two columns.

## Identify the Headings

Headings, or heads, are organizational devices that guide the reader through your paper. There are two types: component heads and text heads.

Component heads identify the different components of your paper and are not topically subordinate to each other. Examples include Acknowledgments and References and, for these, the correct style to use is “Heading 5”. Use “figure caption” for your Figure captions, and “table head” for your table title. Run-in heads, such as “Abstract”, will require you to apply a style (in this case, italic) in addition to the style provided by the drop down menu to differentiate the head from the text.

Text heads organize the topics on a relational, hierarchical basis. For example, the paper title is the primary text head because all subsequent material relates and elaborates on this one topic. If there are two or more sub-topics, the next level head (uppercase Roman numerals) should be used and, conversely, if there are not at least two sub-topics, then no subheads should be introduced. Styles named “Heading 1”, “Heading 2”, “Heading 3”, and “Heading 4” are prescribed.

## Figures and Tables

### Positioning Figures and Tables: Place figures and tables at the top and bottom of columns. Avoid placing them in the middle of columns. Large figures and tables may span across both columns. Figure captions should be below the figures; table heads should appear above the tables. Insert figures and tables after they are cited in the text. Use the abbreviation “Fig. 1”, even at the beginning of a sentence.

1. Table Type Styles

| Table Head | Table Column Head | | |
| --- | --- | --- | --- |
| Table column subhead | Subhead | Subhead |
| copy | More table copya |  |  |

a. Sample of a Table footnote. (Table footnote)

We suggest that you use a text box to insert a graphic (ideally 300 dpi), with all fonts embedded) because, in an MSW document, this method is somewhat more stable than directly inserting a picture.

To have non-visible rules on your frame, use the MSWord pull-down menu, select Format > Borders and Shading > Select “None”.

1. Example of a ONE-COLUMN figure caption.

Please see last page of this document for AN EXAMPLE of a 2-COLUMN Figure.

Figure Labels: Use 8 point Times New Roman for Figure labels. Use words rather than symbols or abbreviations when writing Figure axis labels to avoid confusing the reader. As an example, write the quantity “Magnetization”, or “Magnetization, M”, not just “M”. If including units in the label, present them within parentheses. Do not label axes only with units. In the example, write “Magnetization (A/m)” or “Magnetization {A[m(1)]}”, not just “A/m”. Do not label axes with a ratio of quantities and units. For example, write “Temperature (K)”, not “Temperature/K”.

## Footnotes

Use footnotes sparingly (or not at all) and place them at the bottom of the column on the page on which they are referenced. Use Times 8-point type, single-spaced. To help your readers, avoid using footnotes altogether and include necessary peripheral observations in the text (within parentheses, if you prefer, as in this sentence).

##### Acknowledgment

The preferred spelling of the word “acknowledgment” in America is without an “e” after the “g”. Avoid the stilted expression, “One of us (R.B.G.) thanks . . .” Instead, try   
“R.B.G. thanks”. Put applicable sponsor acknowledgments here; DO NOT place them on the first page of your paper or as a footnote.

##### References

List and number all bibliographical references in 9-point Times, single-spaced, at the end of your paper. When referenced in the text, enclose the citation number in square brackets, for example [1]. Where appropriate, include the name(s) of editors of referenced books. The template will number citations consecutively within brackets [1]. The sentence punctuation follows the bracket [2]. Refer simply to the reference number, as in [3]—do not use “Ref. [3]” or “reference [3]” except at the beginning of a sentence: “Reference [3] was the first . . .”

Number footnotes separately in superscripts. Place the actual footnote at the bottom of the column in which it was cited. Do not put footnotes in the reference list. Use letters for table footnotes.

Unless there are six authors or more give all authors’ names; do not use “et al.”. Papers that have not been published, even if they have been submitted for publication, should be cited as “unpublished” [4]. Papers that have been accepted for publication should be cited as “in press” [5]. Capitalize only the first word in a paper title, except for proper nouns and element symbols.

For papers published in translation journals, please give the English citation first, followed by the original foreign-language citation [6].

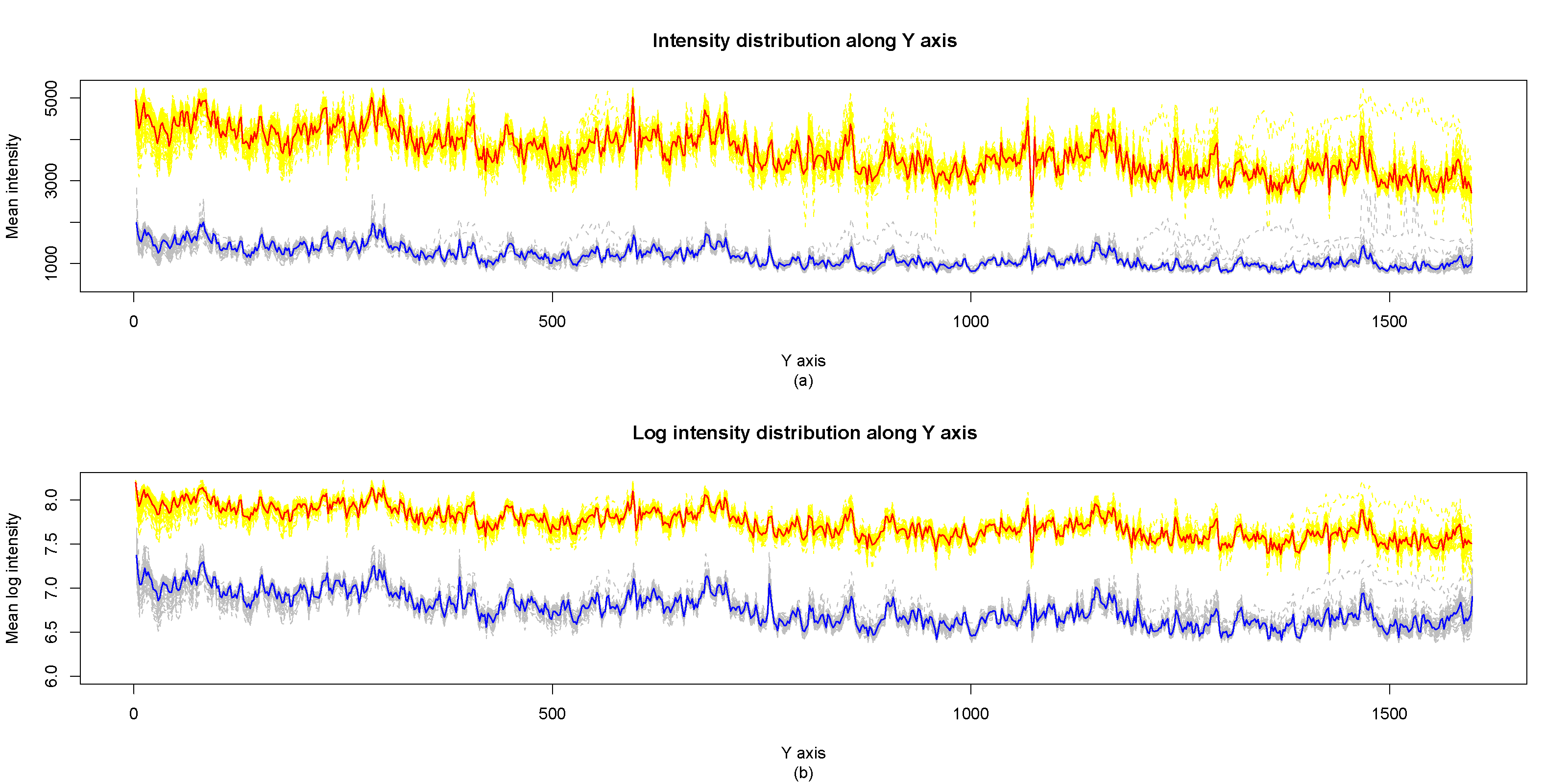
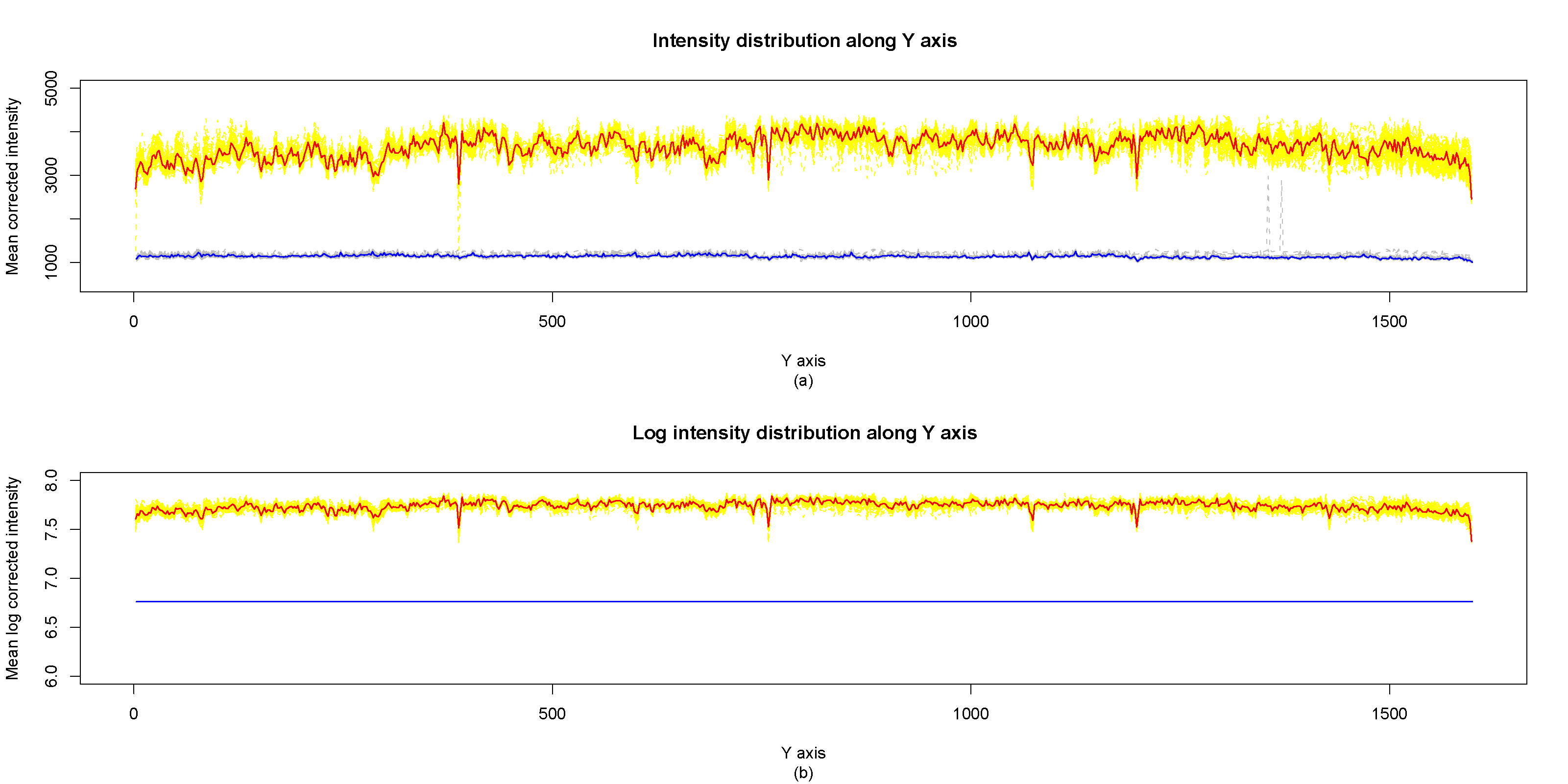
1. G. Eason, B. Noble, and I. N. Sneddon, “On certain integrals of Lipschitz-Hankel type involving products of Bessel functions,” Phil. Trans. Roy. Soc. London, vol. A247, pp. 529–551, April 1955. *(references)*
2. J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, pp.68–73, 1892,
3. I. S. Jacobs and C. P. Bean, “Fine particles, thin films and exchange anisotropy,” in Magnetism, vol. III, G. T. Rado and H. Suhl, Eds. New York: Academic, pp. 271–350, 1963.
4. K. Elissa, “Title of paper if known,” unpublished.
5. R. Nicole, “Title of paper with only first word capitalized,” J. Name Stand. Abbrev., in press.
6. Y. Yorozu, M. Hirano, K. Oka, and Y. Tagawa, “Electron spectroscopy studies on magneto-optical media and plastic substrate interface,” IEEE Transl. J. Magn. Japan, vol. 2, pp. 740–741, August 1987 [Digests 9th Annual Conf. Magnetics Japan, p. 301, 1982].
7. M. Young, The Technical Writer’s Handbook. Mill Valley, CA: University Science, 1989.
8. Electronic Publication: Digital Object Identifiers (DOIs):

Article in a journal:

1. D. Kornack and P. Rakic, “Cell Proliferation without Neurogenesis in Adult Primate Neocortex,” Science, vol. 294, pp. 2127-2130, Dec. 2001, doi:10.1126/science.1065467.
2. European Space Agency. *ESA: Missions, Earth Observation: ENVISAT*. [Online]. Available from: http://envisat.esa.int/ 2008.06.25

Article in a conference proceedings:

1. A. Kito, Y. Mizumachi, K. Sato, Y. Matsuoka, “Emergent Design System Using Computer-Human Interactions and Serendipity” The Sixth International Conference on Advances in Computer-Human Interactions (ACHI 2013) IARIA, Feb. 2013, pp. 7-12, ISSN: 2308-4138, ISBN: 978-1-61208-250-9
2. H. Goto, Y. Hasegawa, and M. Tanaka, “Efficient Scheduling Focusing on the Duality of MPL Representatives,” Proc. IEEE Symp. Computational Intelligence in Scheduling (SCIS 07), IEEE Press, Dec. 2007, pp. 57-64, doi:10.1109/SCIS.2007.357670.

1. Example of a TWO-COLUMN figure caption: (a) this is the format for referencing parts of a figure.