Toronto Metropolitan University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

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Instructor:	Fei Yuan

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*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: https://www.torontomu.ca/senate/policies/pol60.pdf

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Introduction

The *Design Project* was completed on April 7th, 2024. This report contains the steps taken towards the design and implementation of a multistage amplifier circuit. This includes the calculations and MultiSIM simulations.

Objectives

The purpose of this project is to design, simulate, and implement a single-supply, multistage, and inverting amplifier circuit with the use of transistors. The amplifier will abide by a list of specifications. In order for a successful design, the design must meet all the requirements listed.

Specifications

- Power supply: +**10*V*** relative to the ground;
- Quiescent current drawn from the power supply: **no larger than 10 *mA*;**
- No-load voltage gain (at 1 *kHz*): |***Avo***| = **50** (± **10**%);
- Maximum no-load output voltage swing (at 1 *kHz*): no smaller than 8 V peak to peak;
- Loaded voltage gain (at 1 *kHz* and with *RL* = 1 *k*Ω): **no smaller than 90% of the no-load voltage gain;**
- Maximum loaded output voltage swing (at 1 *kHz* and *RL* = 1 *k*Ω): **no smaller than 4 V peak to peak;**
- Input resistance (at 1 *kHz*): **no smaller than 20 *kΩ*;**
- Amplifier type: **inverting or non-inverting;**
- Frequency response: **20 Hz to 50 kHz (−3*dB* response);**
- Type of transistors: **BJT;**
- Number of transistors (stages): **no more than 3;**
- Resistances permitted: **values smaller than 220 *kΩ* from the E24 series;**
- Capacitors permitted: **0.1 *μF***, **1.0 *μF***, **2.2 *μF***, **4.7 *μF***, **10 *μF***, **47 *μF***, **100 *μF***, **220 *μF***;
- Other components (BJTs, diodes, Zener diodes, etc.): **only from your ELE404 lab kit.**

Circuit Under Test

Below is the circuit that was chosen as a base for the amplifier. It is a two-stage amplifier that contains a CE amplifier followed by a CC amplifier. The CC amplifier acts as a buffer between the CE amplifier and load. Using the specifications as a guideline, the values of each comment will be determined.

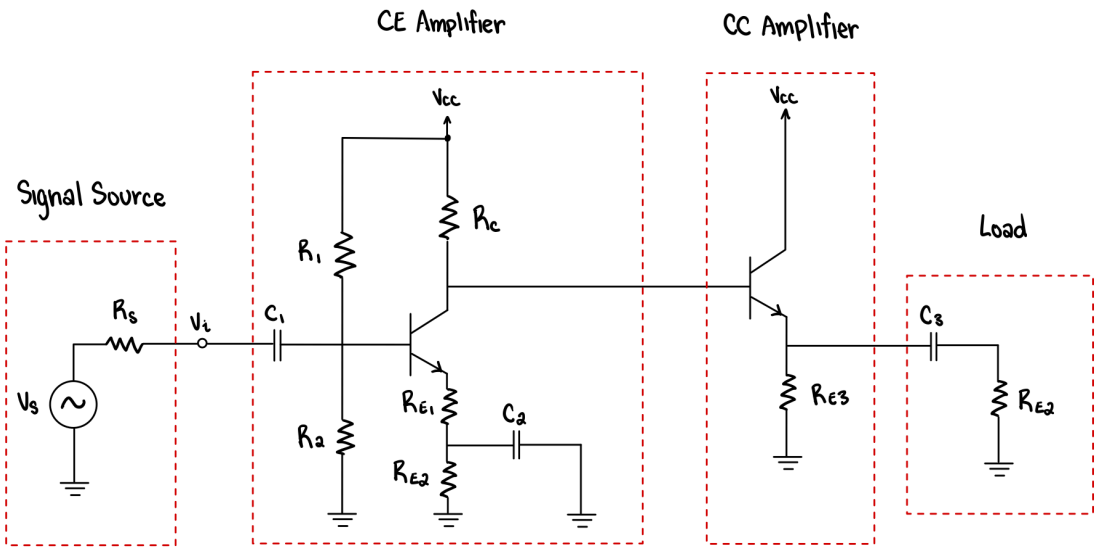


Figure 1. A Common-Emitter(CE) amplifier driving a buffered load.

Summary of Calculations

This section contains a summary of the calculations. Specifically, the values of the components.

C_1 (μF)	C_2 (μF)	C_3 (μF)
10	100	100

Table 1. Capacitor Values

The capacitor values of lab 7 were used for this design project. These were used initially based on assumptions, however they were later verified during simulations. C_1 was chosen to be $10\mu F$ as it acts as a coupling capacitor between amplifier stages. C_2 and C_3 were chosen to be $100\mu F$ as they are connected to the emitter degeneration resistors. This ensures consistency in resistance changes as small changes to resistors related to emitter degeneration result can have a big impact on the gain.

$R_s\ (k\Omega)$	$R_1\ (k\Omega)$	$R_2\ (k\Omega)$	$R_C\ (k\Omega)$	$R_{E1}\ (k\Omega)$	$R_{E2}\ (k\Omega)$	$R_{E3}\ (k\Omega)$	$R_L\ (k\Omega)$
0.6	100	43	20	0.24	5.6	1	1

Table 2. Resistor Values

These resistor values were determined via manual calculations based on the specifications.

It should be noted that there were a few assumptions made in order to obtain these calculations:

- $\beta = 150$: This value was given and used in lab 7
- $V_E = 3V_{BE} = 3(0.7) = 2.1V$: The value was decided upon for biasing current stability as the voltage of emitter degeneration should be at least $3V_{BE}$.
- $R_o = 20k\Omega$

MultiSIM Simulations

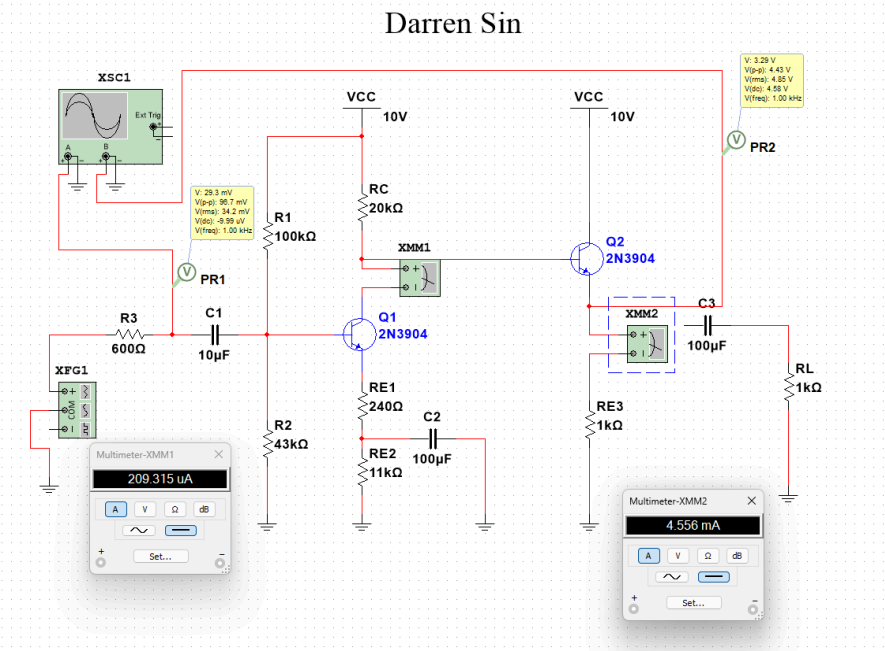


Figure 2. Schematic of the amplifier circuit and the calculated values of **Figure 1** without the load connected

For the voltage gain without load: $|A_{vo}| = \frac{4.43V}{96.7mV} = 45.8\frac{V}{V}$. This falls within the range of the specifications $(50 \pm 5V)$.

For the quiescent current: $I_c = 4.556mA + 0.209315mA = 4.765mA$. This falls within the specified range of $I_c \leq 10mA$.

Both specifications were met for the amplifier circuit without a load.

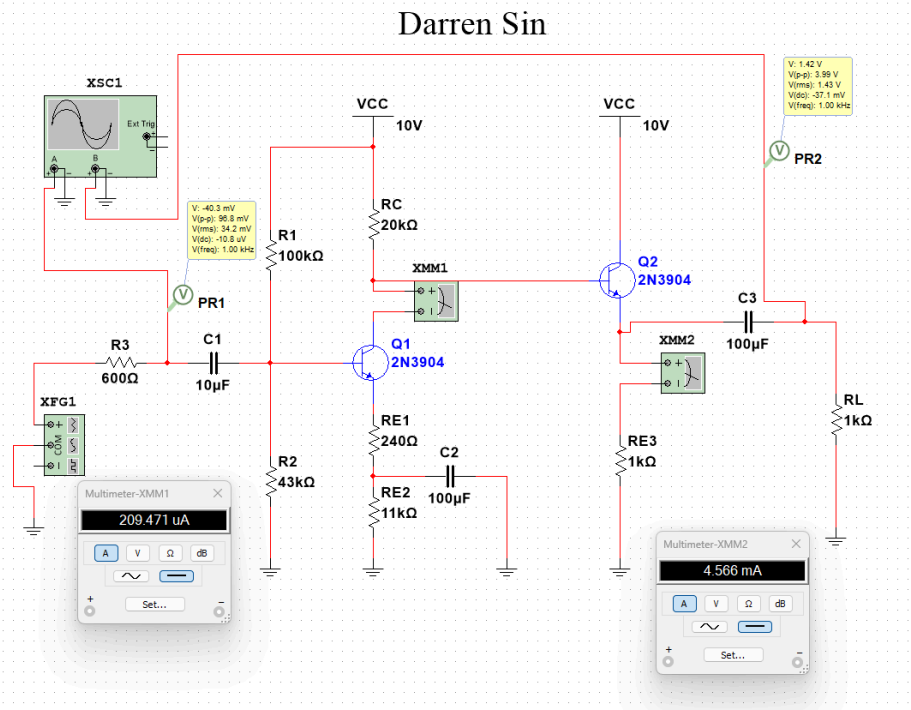


Figure 3. Schematic of the amplifier circuit and the calculated values of **Figure 1** with the load connected

For the voltage gain with a load of 1kHz: $|A_v| = \frac{3.98V}{96.8mV} = 41.22\frac{V}{V}$. This falls within the range of 90% of $|A_{vo}|$ as $0.9(A_{vo}) = 41.22\frac{V}{V}$.

For the quiescent current: $I_c = 4.566mA + 0.209471mA = 4.775mA$. This falls within the specified range of $I_c \leq 10mA$.

Both specifications were met for the amplifier circuit with a load.

Waveforms

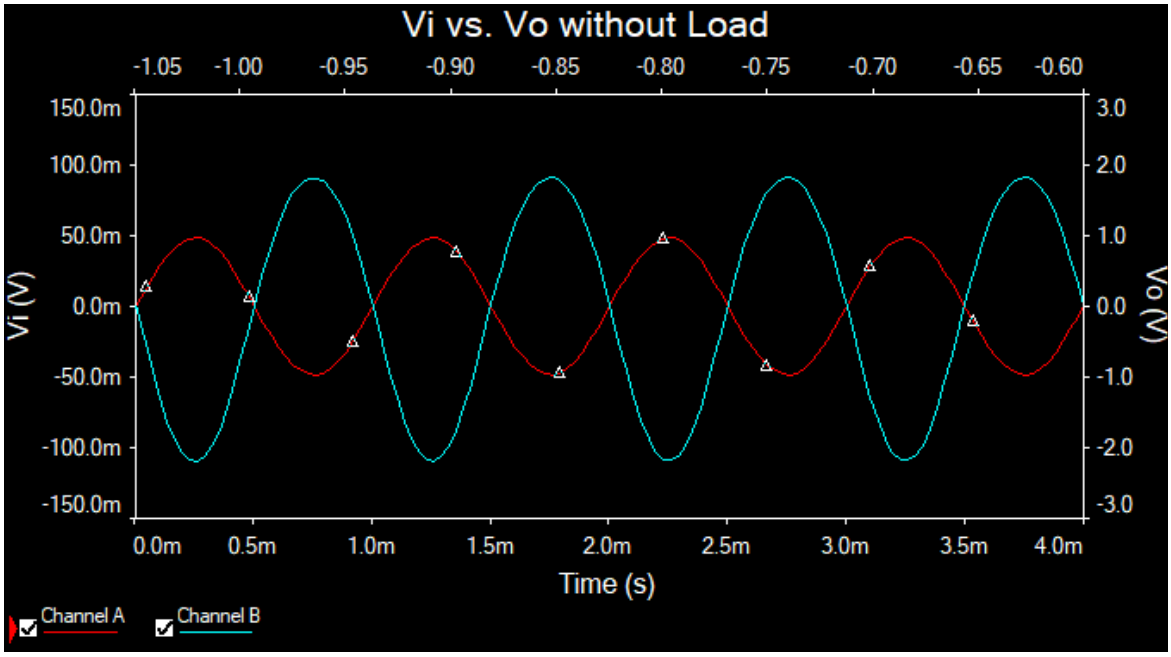


Figure 4. Simulated waveform for the circuit of **Figure 2**

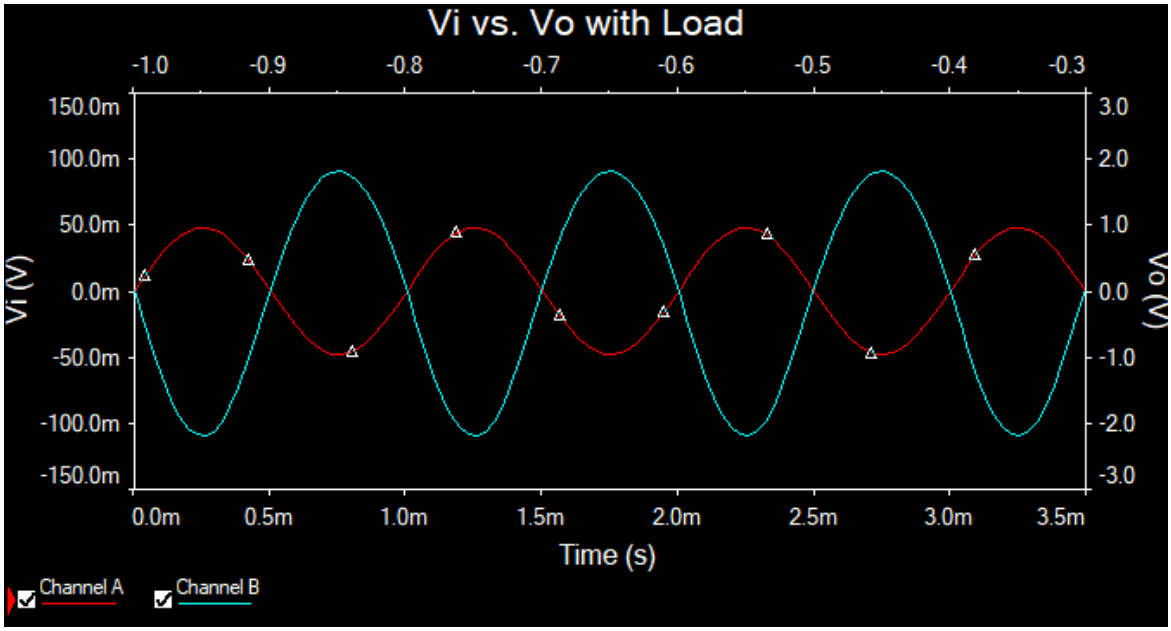


Figure 5. Simulated waveform for the circuit of **Figure 3**

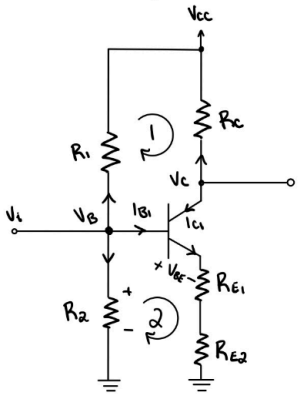
Conclusions and Remarks

This design project can be seen as a success. I was able to meet the requirements as shown from the manual calculations and MultiSIM simulations. It is important to note that there were discrepancies that had an impact on the results, leading to some inconsistencies. Notably, the resistors from the manual calculations were limited to the resistors listed in the E24 Series. This led to some resistors having different values in the circuit compared to the manual calculations. Ultimately, I was still able to achieve the specifications and I would deduce this project to be done with success.

Appendix

Calculations

Examine the CE stage in DC



Since the amplifier examined is a CE amplifier, $R_o \approx R_c$. Thus, $R_c = 20k\Omega$

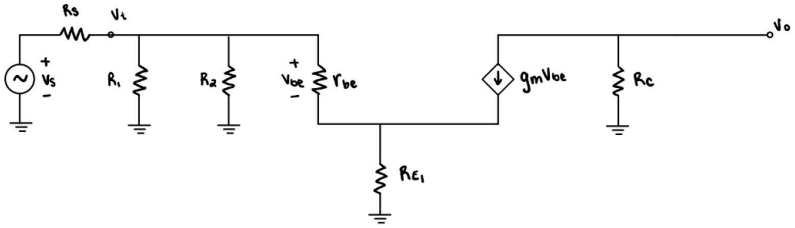
$$V_c = \frac{1}{2}(V_{cc} + V_E + 0.3)$$
$$= \frac{1}{2}(10 + 2.1 + 0.3)$$
$$= 6.2$$

$$I_{C1} = \frac{V_{cc} - V_c}{R_c}$$
$$= \frac{10 - 6.2}{20000}$$
$$= 0.19mA$$

$$I_{E1} = \frac{\beta}{1+\beta} I_{C1}$$
$$= \frac{150}{151}(0.19mA)$$
$$= 0.189\,mA$$

$$R_{E1} + R_{E2} = \frac{V_E}{I_{E1}}$$
$$= \frac{2.1}{0.188}$$
$$= 11.17k\Omega$$
$$\approx 11k\Omega \text{ (E24 series)}$$

Examine the CE stage using small signal analysis



$$g_{m1} = \frac{I_{C1}}{V_t}$$
$$= \frac{0.19}{0.026}$$
$$= 7.31\,mS$$

$$|A_{vo}| = 50$$
$$50 = \left|\frac{-g_{m1}R_c}{1+g_{m1}R_{E1}}\right|$$
$$1 + g_m R_{E1} = \frac{g_{m1}R_c}{50}$$
$$R_{E1} = \frac{1}{g_m}\left(\frac{g_m R_c}{50} - 1\right)$$
$$R_{E1} = \frac{R_c}{50} - \frac{1}{g_m}$$
$$R_{E1} = \frac{20000}{50} - \frac{1}{7.31\times10^{-3}}$$
$$R_{E1} = 263.14$$
$$\approx 240\,\Omega \text{ (E24 series)}$$

$$R_{E1} + R_{E2} = 11.17k\Omega$$
$$R_{E2} \approx 11k\Omega \text{ (E24 series)}$$

$$r_\pi = \frac{\beta}{g_m}$$
$$= \frac{150}{7.31\times10^{-3}}$$
$$= 20519.84\,\Omega$$

Since $R_i \geq 20k\Omega$, let $R_1 \| R_2 \| R_i' \geq 20k\Omega$

$$R_i' = r_\pi + (\beta+1)R_{E1}$$
$$= 20519.84 + 151(263)$$
$$= 60232.84$$

Let $R_1 \| R_2 = 30k$

$$\frac{R_1 R_2}{R_1 + R_2} = 30k \quad (1)$$

$$V_B = V_{cc}\left(\frac{R_2}{R_1+R_2}\right)$$
$$V_E + V_{BE} = V_{cc}\left(\frac{R_2}{R_1+R_2}\right)$$
$$\frac{R_2}{R_1+R_2} = \frac{V_E + V_{BE}}{V_{cc}}$$
$$\frac{R_2}{R_1+R_2} = 0.28 \quad (2)$$

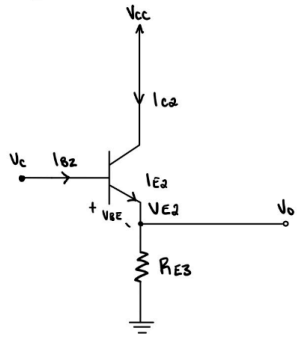
$$\frac{1}{\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_i'}} \geq 20k\Omega$$
$$\frac{1}{R_1}+\frac{1}{R_2} \geq \frac{1}{20k\Omega} - \frac{1}{R_i'}$$
$$R_1 \| R_2 \geq \left(\frac{1}{20k\Omega} - \frac{1}{R_i'}\right)^{-1}$$
$$R_1 \| R_2 \geq \left(\frac{1}{20k} - \frac{1}{60232.84}\right)^{-1}$$
$$R_1 \| R_2 \gtrsim 30k$$

Solving (1) and (2) yields

$$R_1 = 107142.857\,\Omega$$
$$= 100k\,\Omega \text{ (E24 series)}$$

$$R_2 = 41666.67\,\Omega$$
$$= 43k\,\Omega \text{ (E24 series)}$$

CC stage used as a buffer between the CE amplifier and the load



As a design choice, since $I_{B2} \ll I_{C1}$

Let $I_{B2} = \frac{1}{50} I_{C1}$

$= \frac{1}{50}(0.19\,mA)$

$= 0.0038\,mA$

$I_{C2} = (\beta+1) I_{B2}$

$= 0.574\,mA$

$I_{E2} = \beta I_{B2}$

$= 0.57\,mA$

$V_{E2} = V_C - V_{BE}$

$= 5.5\,V$

$g_{m2} = \frac{I_{C2}}{V_t}$

$= \frac{0.574}{0.026}$

$= 22.08\,mS$

$R_{E3} = \frac{V_{E2}}{I_{E2}}$

$= \frac{5.5}{0.57}$

$= 0.965\,k\Omega$

$\approx 1\,k\Omega$ (E24 series)

$r_{e2} = \frac{1}{g_{m2}}$

$= \frac{1}{22.08}$

$= 45.29\,\Omega$

$R_o = R_{E3} \parallel (r_{e2} + \frac{R_c}{\beta+1})$

$= 0.965k \parallel (45.29 + \frac{20000}{151})$

$= 150.1\,\Omega$

Gain for CC stage: $\frac{V_o}{V_c} = \frac{g_{m2} R_{E3}}{1 + g_{m2} R_{E3}}$

$= \frac{22.08(0.965)}{1+22.08(0.965)}$

$= 0.984$

$r_{\pi 2} = \frac{\beta}{g_{m2}}$

$= \frac{150}{22.08 \times 10^{-3}}$

$= 6793.48$

$R_{i2} = r_{\pi 2} + (\beta+1) R_{E3}$

$= 6793.48 + 151(0.965k)$

$= 152508.48\,\Omega$

$R_c \parallel R_{i2} = \frac{1}{\frac{1}{R_c} + \frac{1}{R_{i2}}}$

$= \frac{1}{\frac{1}{20000} + \frac{1}{152508.48}}$

$= 17681.27\,\Omega$

$\frac{V_c}{V_i} = -\frac{g_{m1}(R_c \parallel R_{i2})}{1 + g_{m1} R_{E1}}$

$\frac{V_c}{V_i} = -\frac{(7.31 \times 10^{-3})(17681.27)}{1 + (7.31 \times 10^{-3})(263.14)}$

$\frac{V_c}{V_i} = -46.21\ \frac{V}{V}$

The overall gain of the circuit without load is: $|A_{vo}| = 46.21\,(0.984) = 45.47\ \frac{V}{V}$

Figure 6. Manual calculation of the two-stage amplifier circuit of **Figure 1**.