BlueMax Pin Mapping

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October 20, 2021

Abstract

This document details the pin mapping of the BlueMax FPGA to the expansion connectors and buil-in peripherals.

1 Pin mapping of expansion connectors

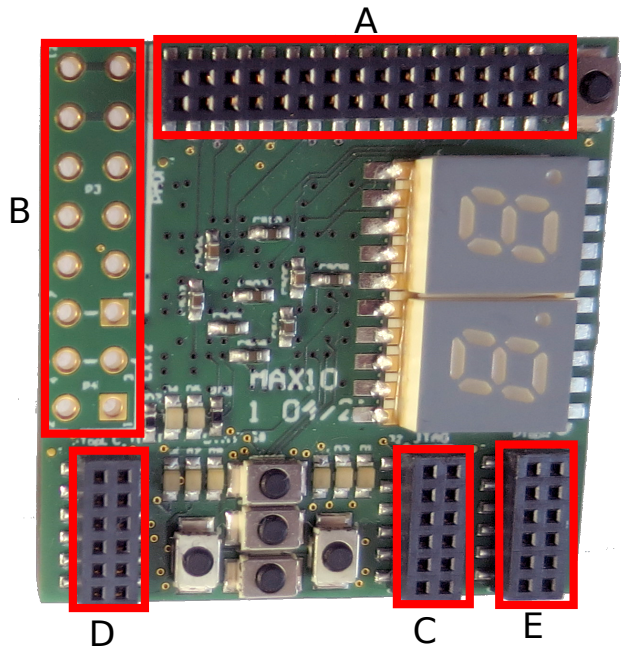

Figure 1: BlueMax has 5 expansion connectors. Connectors A, B, C are dedicated extensions of BlueMax. The connectors D and E allow BlueMax to be plugged onto BlueSense in which case the semantics of these pins is given by BlueSense.

Table 1: Expansion connector A (XF)

VCC	XF_PLL_CLK L3 CLKO	XF_2 N4 I/O	XF_4 J5 I/O	XF_6 L4 I/O	XF_8 N5 I/O	XF_10 N6 I/O	XF_12 N7 I/O	XF_14 J6 I/O	XF_16 M8 I/O	XF_18 J7 I/O	XF_20 N9 I/O	XF_22 K8 I/O	XF_24 M10 I/O	XF_26 M11 I/O	XF_28 M13 I/O
GND	CLK_MAIN H6 CLKI	XF_1 M4 I/O	XF_3 K5 I/O	XF_5 L5 I/O	XF_7 M5 I/O	XF_9 M7 I/O	XF_11 N8 I/O	XF_13 K6 I/O	XF_15 M9 I/O	XF_17 K7 I/O	XF_19 N10 I/O	XF_21 J8 I/O	XF_23 L10 I/O	XF_25 L11 I/O	XF_27 M12 I/O

Table 2: Expansion connector B (PMOD+XF)

VCC PWR	VCC PWR
GND PWR	GND PWR
XP_8 M1 I/O	XP_4 M2 I/O
XP_7 K1 I/O	XP_3 L2 I/O
XP_6 K2 I/O	XP_2 J1 I/O
XP_5 J2 I/O	XP_1 H2 I/O
XF_ADC1IN8 E1 AIN, I/O	XF_ANAIN1 D2 AIN
CLK_MAIN H6 CLKI	XF_PLL_CLK L3 CLKO

Table 3: Expansion connector D (general purpose or BlueSense extension). The naming convention follows that of BlueSense, on which BlueMax can be plugged onto, but this connector can also be used for general purpose I/O.

X_AUD_CLK N3 CLKI, I/O	X_AUD_DAT B2 I/O
GND PWR	UNC.
UNC.	UNC.
UNC.	VCCIN PWR
UNC.	X_SAI2A_SD_MOSI A3 I/O
X_SAI2A_MCLK_MISO A2 I/O	X_SAI2A_SCLK N2 CLKI, I/O

Table 4: Expansion connector C (Programming+XF)

GND PWR	P_JTAGEN E5 P
P_TDI P	P_TDO P
P_TMS P	P_TCK P
XF_ADC1IN6 B1 F1 AIN, I/O	XF_ADC1IN7 AIN, I/O
XF_ADC1IN8 E1 AIN, I/O	XF_ANAIN1 D2 AIN
VCC PWR	VCC PWR

Table 5: Expansion connector E (general purpose or BlueSense extension). The naming convention follows that of BlueSense, on which BlueMax can be plugged onto, but this connector can also be used for general purpose I/O.

X_5	X_4_ADC_DAC
GND PWR	UNC
AVCCIN PWR	S_SCL
S_SDA	X_SAIA2_FS_NSS
X_3_ADC3	X_2_ADC2
X_1_ADC1	X_0_ADC0

Table 6: BlueMax has two 7-segment displays. All the corresponding pins must be set as output.

LAn(1) J10 O	LAn(0) G13 O
seg(0) K11 O	seg(1) K12 O
seg(2) L12 O	seg(3) K10 O
seg(4) H13 O	seg(5) J13 O
seg(6) J12 O	segp L13 O

2 Pin mapping of internal peripherals

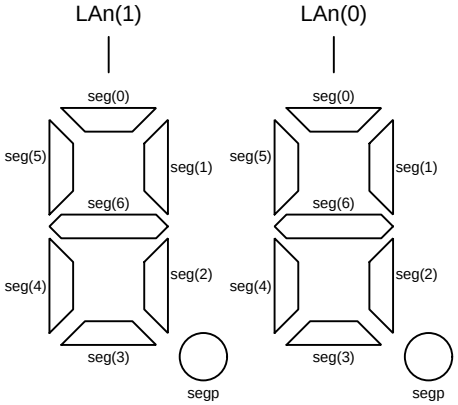

Figure 2: BlueMax has two 7-segment displays, including decimal point. The 7-segment displays are wired for a time-multiplexed use. The segments and decimal point of both digits are wired together to the FPGA. The anode common (LAn) to all the segments of a digit is distinct for each digit and controls whether the digit 1 or 0 is turned on.

Table 7: The 5 push buttons btn(4)... btn(0) must be configured as input with a pull-up. The reset push button clrn has a hardware pull-up and acts as a device-wide reset signal when this FPGA option is activated; alternatively it can be used as user input.

btn(0) B11 I	btn(1) C11 I
btn(2) D12 I	btn(3) C12 I
btn(4) A12 I	clrn B9 I

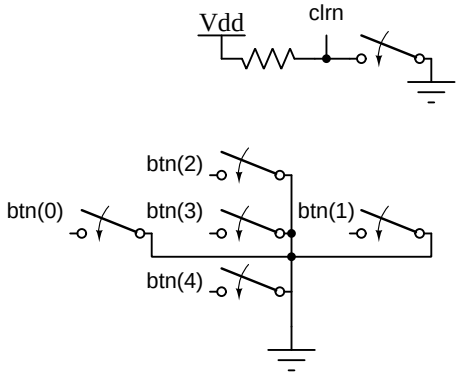

Figure 3: BlueMax has 5 push buttons and a reset button, without hardware debouncing circuitry.

Table 8: Unused pins.

A6	Unconnected
A8	Unconnected
A11	Unconnected
B4	Unconnected
B5	Unconnected
B6	Unconnected
C9	Unconnected
D6	Unconnected
D8	Unconnected
D9	Unconnected
D11	Unconnected
E6	Unconnected
E8	Unconnected
E9	Unconnected
E10	Unconnected
F4	Unconnected
F8	Unconnected
G4	Unconnected
H3	Unconnected
H8	Unconnected
H9	Unconnected
H10	Unconnected
J9	Unconnected
N12	Unconnected
H4	GND
H5	GND
D1	GND
C2	GND
E3	GND
E4	GND
G5	GND
M3	GND
G9	GND
G10	GND
E13	GND
F13	GND
F9	GND
F10	GND

3 Unused pins

A number of FPGA pins are unused and either left as unconnected, or wired to ground (Table 8). Unconnected pins should be configured as input with a pull-up. Pins wired to ground must be configured as input.