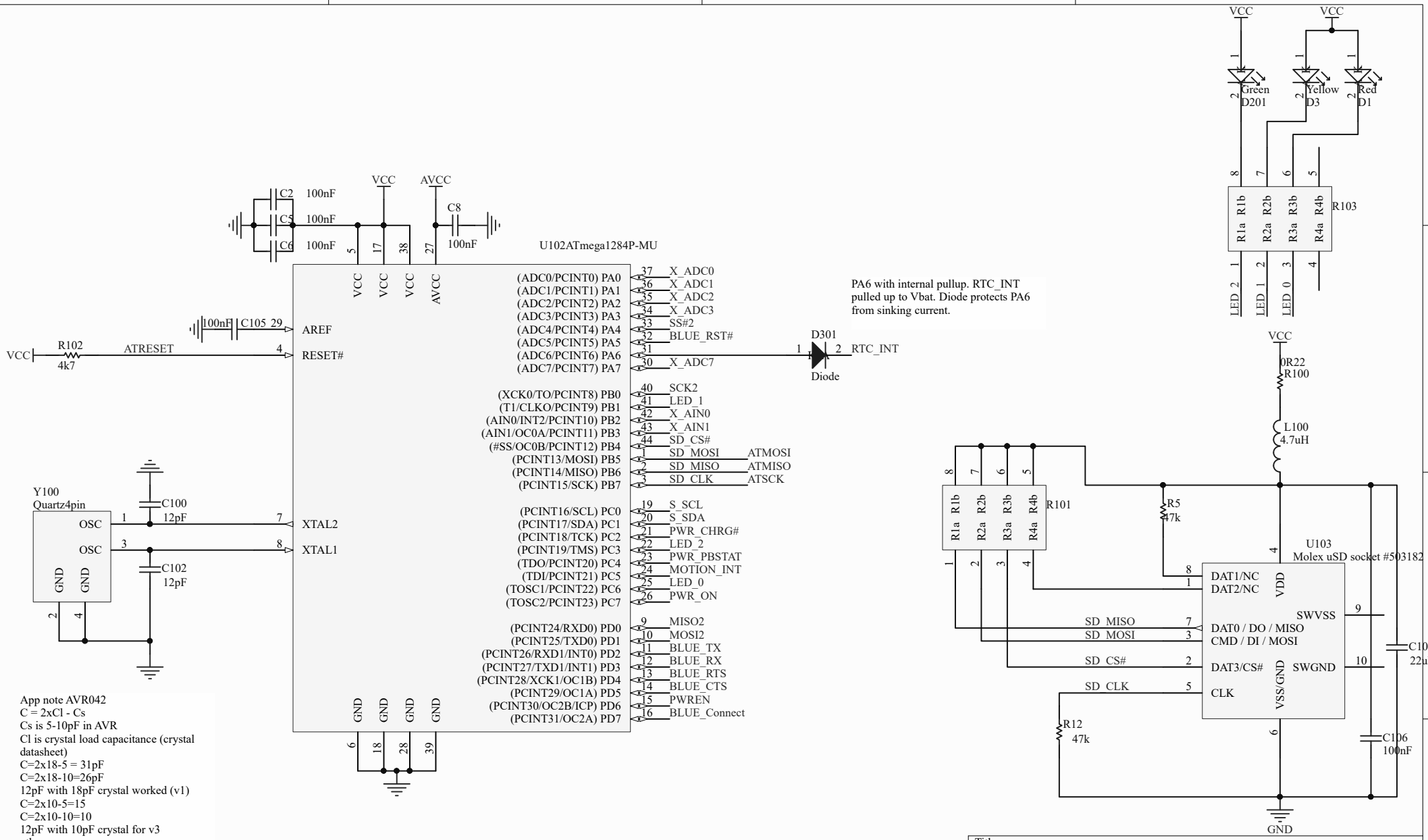

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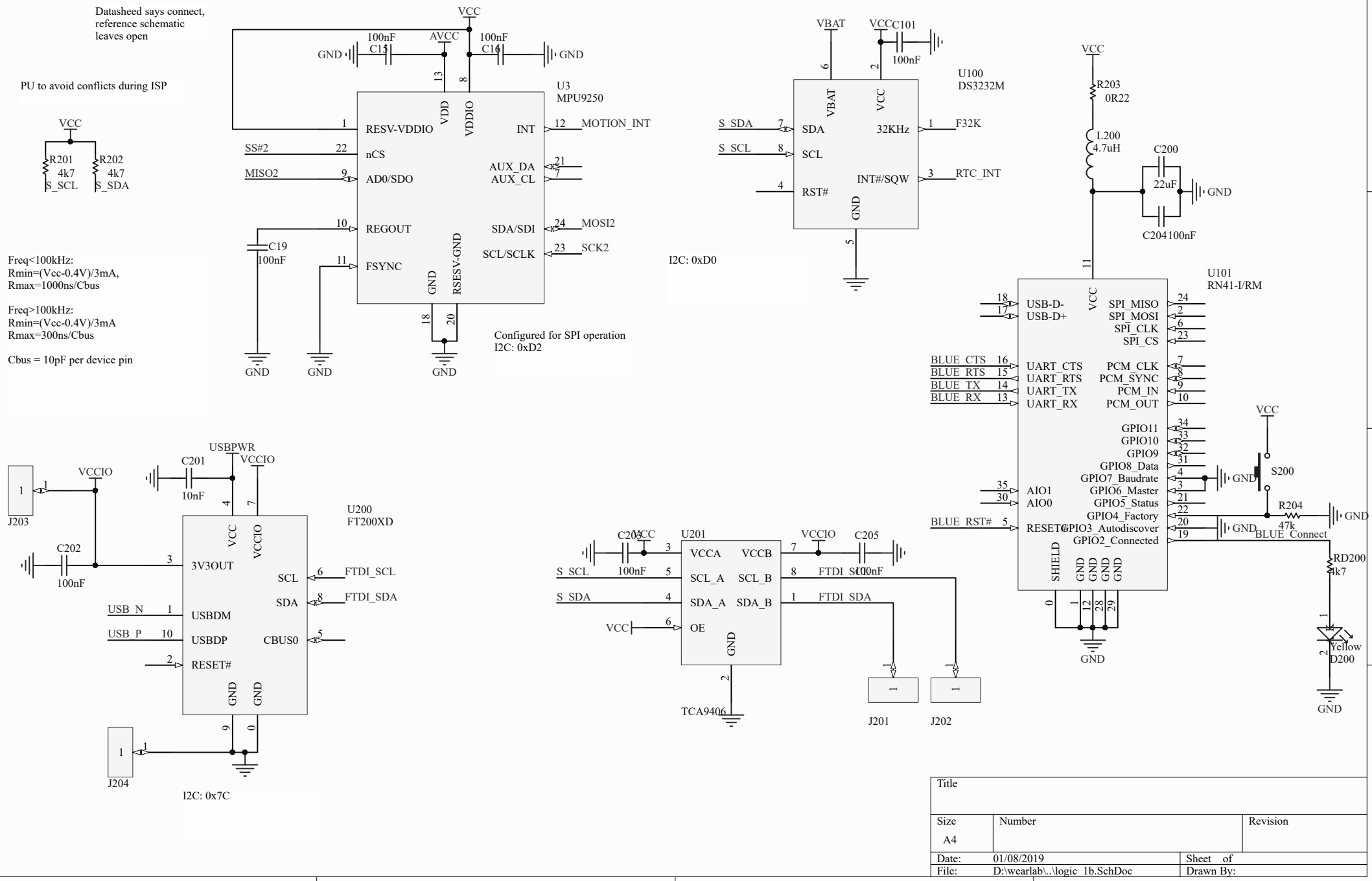
File: D:\wearlab\..\logic 1a.SchDoc		Drawn By:



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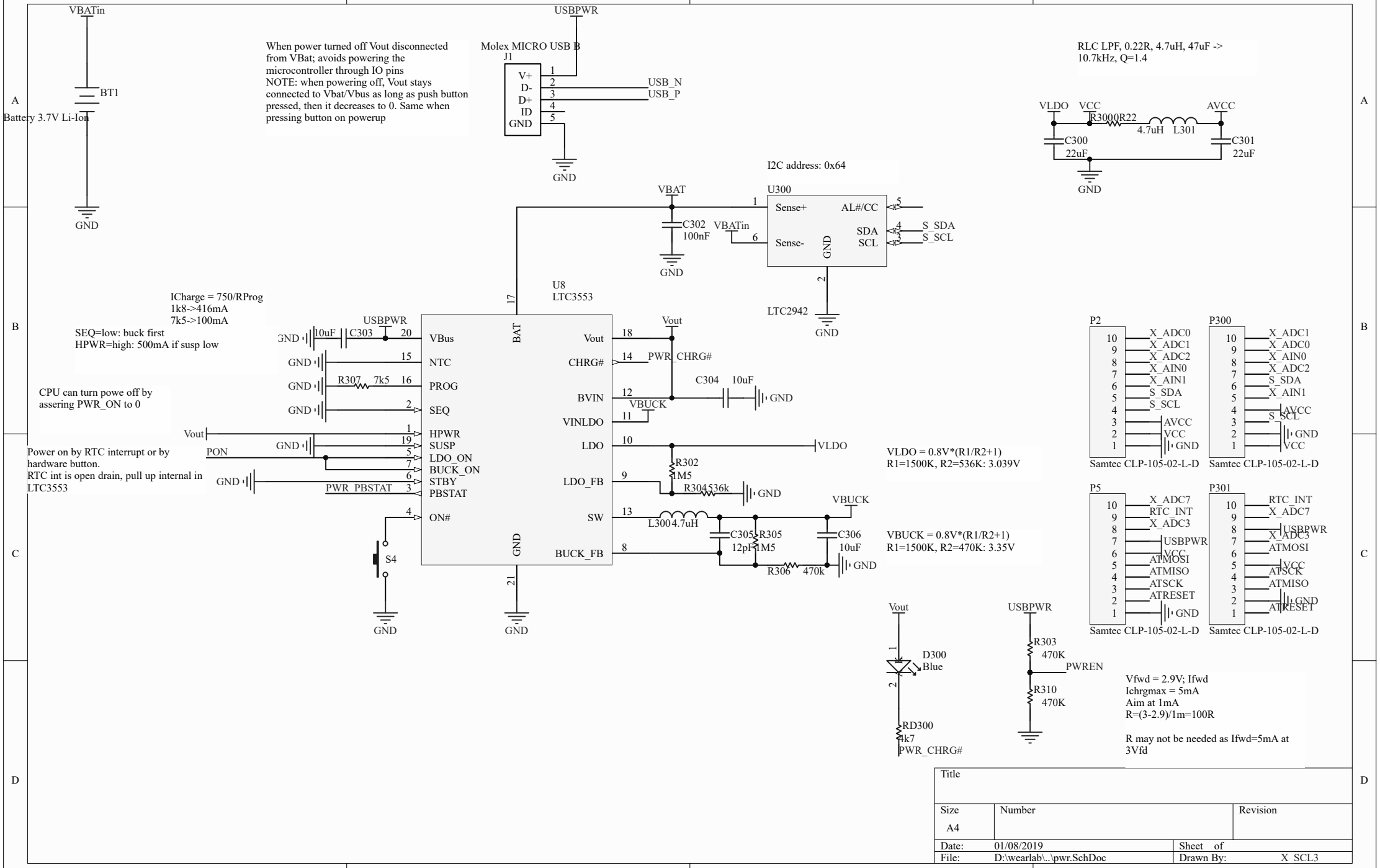
VBATin
BT1
Battery 3.7V Li-Ion
GND
When power turned off Vout disconnected from VBat; avoids powering the microcontroller through IO pins
NOTE: when powering off, Vout stays connected to Vbat/Vbus as long as push button pressed, then it decreases to 0. Same when pressing button on powerup
USBPWR
Molex MICRO USB B
J1
V+
D-
D+
ID
GND
USB_N
USB_P
RLC LPF, 0.22R, 4.7uH, 47uF -> 10.7kHz, Q=1.4
VLDO
VCC
AVCC
R3000R22
4.7uH
L301
C300
22uF
C301
22uF
I2C address: 0x64
U300
Sense+
Sense-
AL#/CC
SDA
SCL
S_SDA
S_SCL
VBAT
C302
100nF
VBATin
LTC2942
U8
LTC3553
ICharge = 750/RProg
1k8->416mA
7k5->100mA
SEQ=low: buck first
HPWR=high: 500mA if susp low
CPU can turn powe off by assering PWR_ON to 0
Power on by RTC interrupt or by hardware button.
RTC int is open drain, pull up internal in LTC3553
VBus
NTC
PROG
SEQ
HPWR
SUSP
LDO_ON
BUCK_ON
STBY
PBSTAT
ON#
BAT
Vout
CHRG#
BVIN
VINLDO
LDO
LDO_FB
SW
BUCK_FB
PWR_CHRG#
C303
10uF
R307
7k5
C304
10uF
VBUCK
R302
1M5
R304
536k
L300
4.7uH
C305
12pF
R305
1M5
C306
10uF
R306
470k
S4
VLDO = 0.8V*(R1/R2+1)
R1=1500K, R2=536K: 3.039V
VBUCK = 0.8V*(R1/R2+1)
R1=1500K, R2=470K: 3.35V
P2
Samtec CLP-105-02-L-D
X_ADC0
X_ADC1
X_ADC2
X_AIN0
X_AIN1
S_SDA
S_SCL
AVCC
VCC
GND
P300
Samtec CLP-105-02-L-D
X_ADC1
X_ADC0
X_AIN0
X_ADC2
S_SDA
X_AIN1
AVCC
S_SCL
GND
VCC
P5
Samtec CLP-105-02-L-D
X_ADC7
RTC_INT
X_ADC3
USBPWR
VCC
ATMOSI
ATMISO
ATSCK
ATRESET
GND
P301
Samtec CLP-105-02-L-D
RTC_INT
X_ADC7
USBPWR
X_ADC3
ATMOSI
VCC
ATSCK
ATMISO
GND
ATRESET
D300
Blue
RD300
4k7
PWR_CHRG#
R303
470K
PWREN
R310
470K
Vfwd = 2.9V; Ifwd
Ichrgmax = 5mA
Aim at 1mA
R=(3-2.9)/1m=100R
R may not be needed as Ifwd=5mA at 3Vfd
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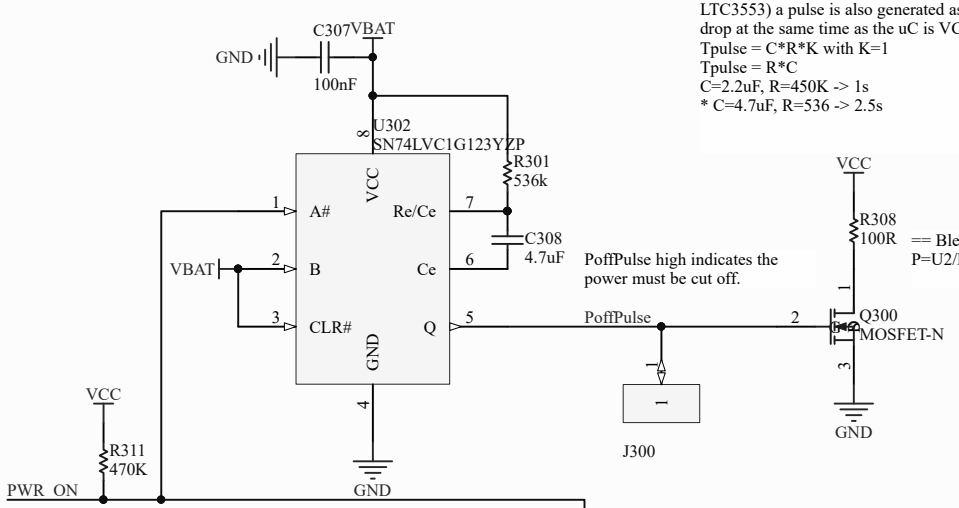
X_SCL3

Has to operate with Vbat: 3.4V-4.3V

== Falling edge detector on PWR_ON==
This generates a positive puse on the falling edge of PWR_ON (CPU controlled) or when VCC drops (e.g. through HRST). PWR_ON is a uC digital out and is pulled up to keep the supply active when the CPU is unprogrammed, in reset, or undergoing programming. Consequently, if VCC falls due to other reasons (e.g. due to a long-press/HRST on the LTC3553) a pulse is also generated as either VCC drops or PWR_ON drops (generally both drop at the same time as the uC is VCC powered).
Tpulse = C*R*K with K=1
Tpulse = R*C
C=2.2uF, R=450K -> 1s
* C=4.7uF, R=536 -> 2.5s

ON semi NSR05F40NXT5G has
Vf=0.1V 75C
Vf=0.2V 25C
Vf=0.3V -25C

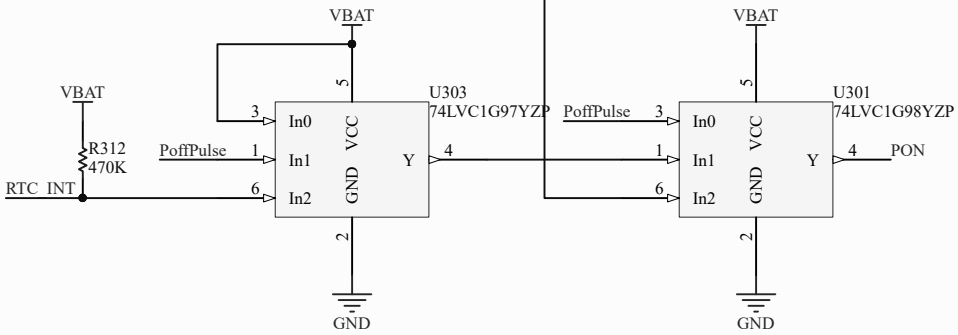
Input voltage range: 3.4-4.3
Output voltage range: 2.5-4.0V



== Bleeder circuit ==
P=U2/R=90mW

Put NMOS transistor to discharge
NXP PMZ200UNE

== Power circuit ==
There are 4 cases:
A. Power is off, pwron through extpwr or PB
B. Power is off, pwron through RTC interrupt
C. Power is on, pwroff through CPU (pull up/down pwron)
D. Power is on, pwroff through hrst (long-press pb)



Y=OR(In1,In2)
Y=OR(1,6)

Y=Mux#(In2,In1,In0)
Y=Mux#(6,1,3)

== Power circuit ==
PWR_ON: 1 to remain on, 0 to power off
RTC_INT: 0 to power on (1 no effect)
PoffPulse: 1 to power off.
The rationale for PoffPulse is to ensure PON remains low until the power circuit is bled. Otherwise, the CPU goes in reset and power may not be turned off (bug identified in V7).

PWR_ON	RTC_INT	PoffPulse	PON	Expl
0	0	0	1	RTC poweron
0	0	1	0	RTC poweron conflict with PoffPulse; turn off
0	1	0	0	CPU requests to turn off
0	1	1	0	CPU and PoffPulse request to turn off
1	0	0	1	CPU maintains on
1	0	1	0	Power off due to PoffPulse
1	1	0	1	CPU maintains on
1	1	1	0	Power off due to PoffPulse

PON = PWR_ON*PoffPulse# + RTC_INT#*PoffPulse#

Can be solved with a mux with inverted output (sn74lvc1g98) and a OR gate (sn74lvc1g97).
PON=MUX#(PWR_ON,OR(RTC_INT,PoffPulse),PoffPulse)
with MUX#(s,A,B)=A# when s=0.

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