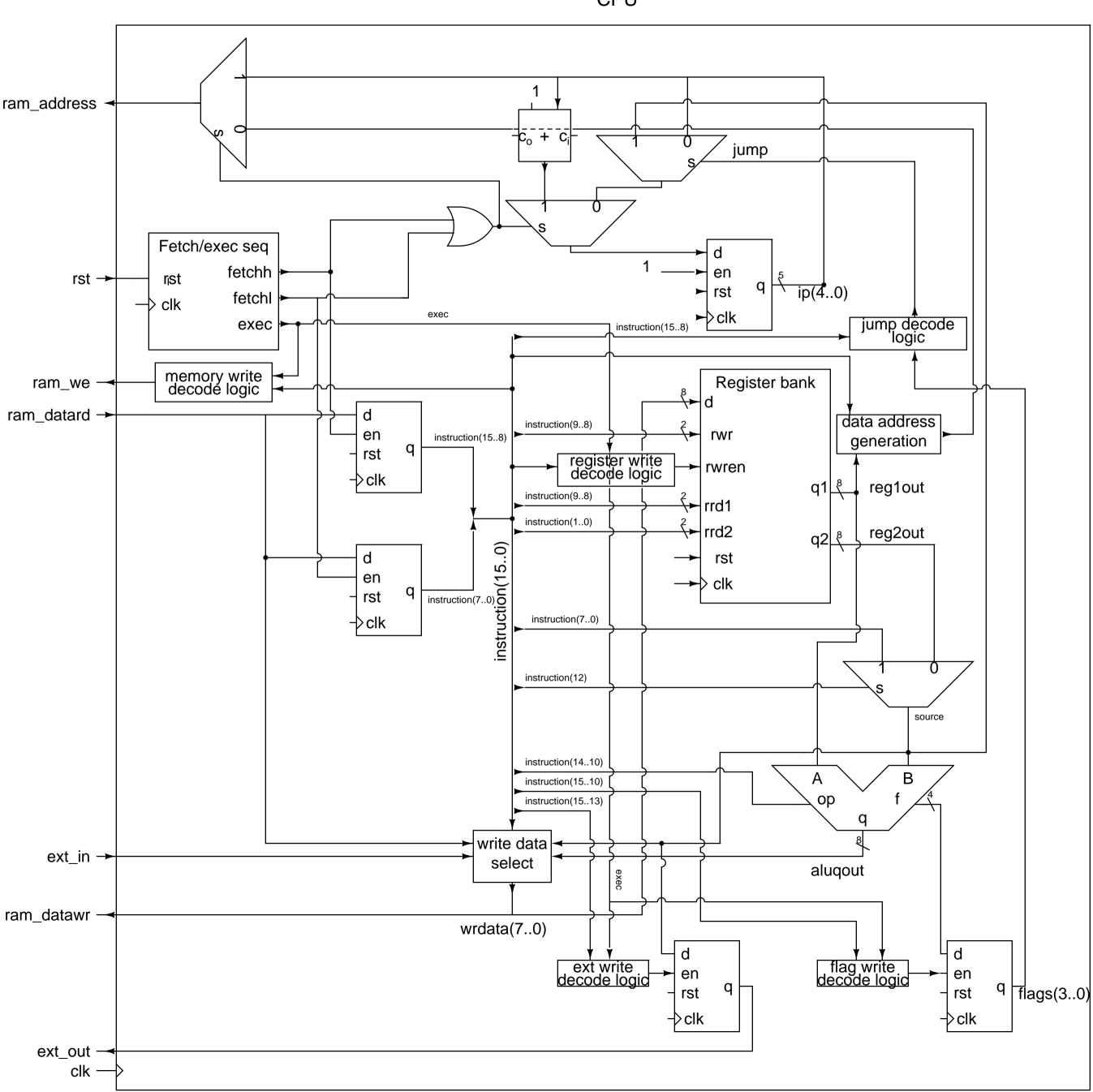
CPU



Jump decode logic

```
instr(15..13)=101 an(d
instr(11..8)=0000 or
(instr(11..8)=0001 and zf=1) or
(instr(11..8)=1001 and zf=0)
)
```

Register write decode logic

```
execute=1 and (
    (instr(15..13)=000 and instr(11)=0) or
    instr(15..13)=001 or
    (instr(15..13)=010 and instr(11..10) /= 01)
    instr(15..13)=011
)
```

Memory write decode logic

execute=1 and instr(15..10)=000X10

External write decode logic

execute=1 and instr(15..13)=110

Flag write decode logic

execute=1 and instr(15..10)=010X01

Write data select

wrdata = source when instr(15..10)=000X00 ram_datard when instr(15..10)=000X01 aluqout when instr(15..13)=001 aluqout when instr(15..13)=010 aluqout when instr(15..13)=011 ext_in when instr(15..10)=110X01

Data address generation

```
address =
reg1out when instr(15..10)=000001
instr(7..0) when instr(15..10)=000101
reg1out when instr(15..10)=000110
reg1out when instr(15..10)=000110
```