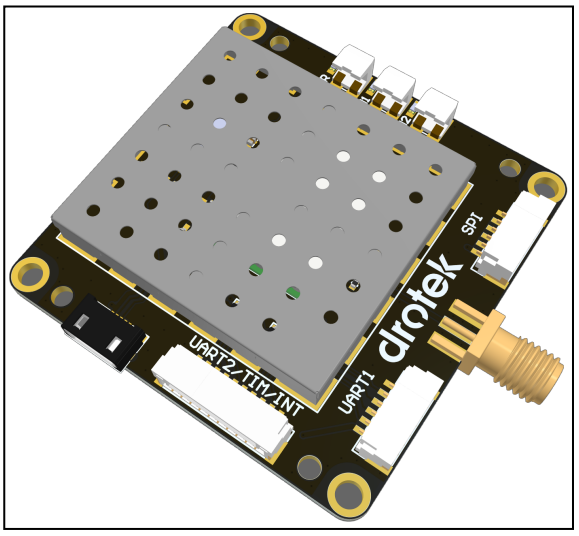
DP0701 (ZED-F9T)

Multi-band GNSS receiver with nanosecond-level accuracy

Datasheet - In Production



Features

- 5V - 100mA power supply
- LEDs status :Power/Timepulse 1&2
- Timepulse & External Interrupt
- USB/SPI/UART digital interfaces
- Gold plated SMA connector
- ESD protection diodes

Applications

- Nanosecond-level timing equipment
- 5G mobile devices
- Oscillators

Description

DP0701 is an affordable compact timing module that provides nanosecond-level timing accuracy to the most demanding infrastructure applications.

DP0701 is designed to meet the most stringent timing synchronization requirements in 5G mobile networks on a global scale. The timing module's multi-band capability reduces the tim-ing error under clear skies to less than 5 ns without the need for an external GNSS correction service

DP0701 includes advanced security features such as secure boot, secure interfaces, and T-RAIM to provide the highest level timing integrity.

The JST-GH connectors make them perfect to be connected to a Pixhawk3Pro or any other autopilot.

The DP0701 GNSS RTK is guaranteed to operate over a temperature range of -20°C to +70°C.

Table 1. Device summary

Order ref code	Temperature range [°C]	Product size [mm]
0916	-20 to +70	50.0 x 50.0 x 8.0

Contents

1. Block diagram and pin description **3**
1.1 Block diagram 3
1.2 LED description 3
1.3 Pin description 4

2. Specifications **5**

3. Absolute maximum ratings **7**

4. Applications **8**

5. Communication interfaces **9**
5.1 UART Interface 9
5.2 SPI interface 10
5.3 Slave I2C interface 11
5.4 USB interface 11

6. Mechanical drawings **12**

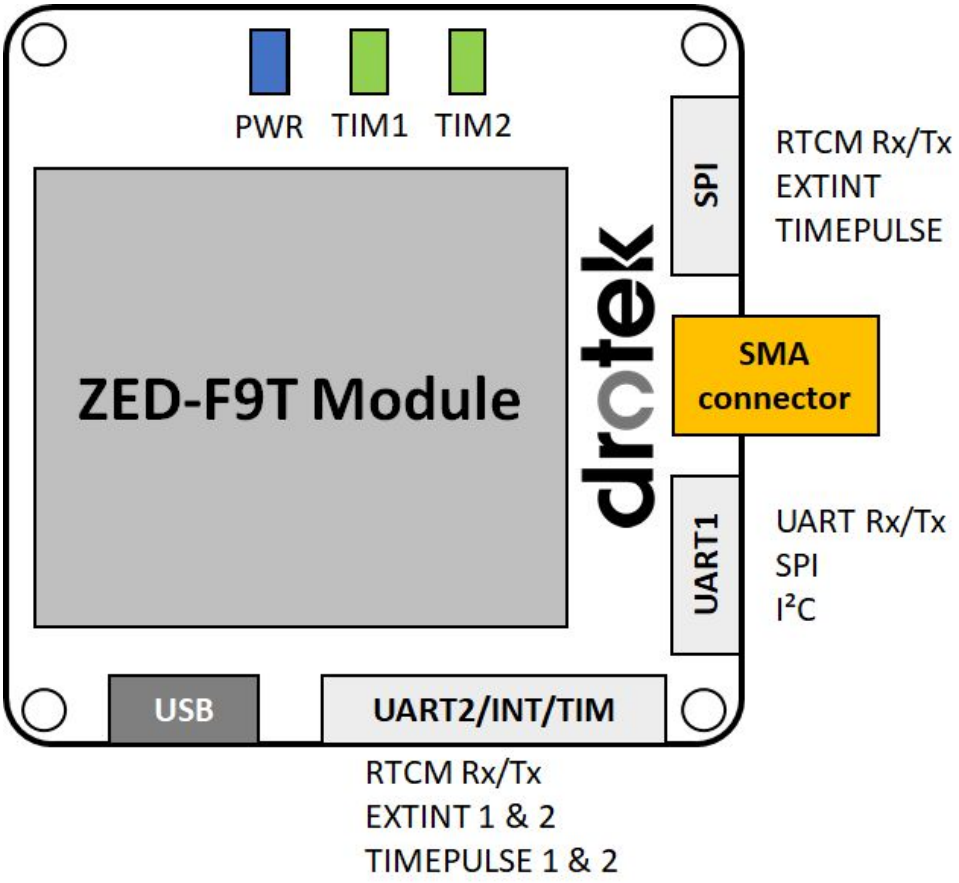
7. Revision history **13**

8. Appendix **13**

1. Block diagram and pin description

1.1 Block diagram

Figure 1. DP0701 block diagram & connectivity (top view)



1.2 LED description

Table 2. DP0701 LED sequence status

LED name	Color	Light sequence	Comment
Power	Blue	● ● ● ●	Solid blue LED when powered ON
Timepulse 1	Green	● ○ ● ○	linking LED when TIMEPULSE is available
Timepulse 2	Green	● ○ ● ○	linking LED when TIMEPULSE is available

1.3 Pin description

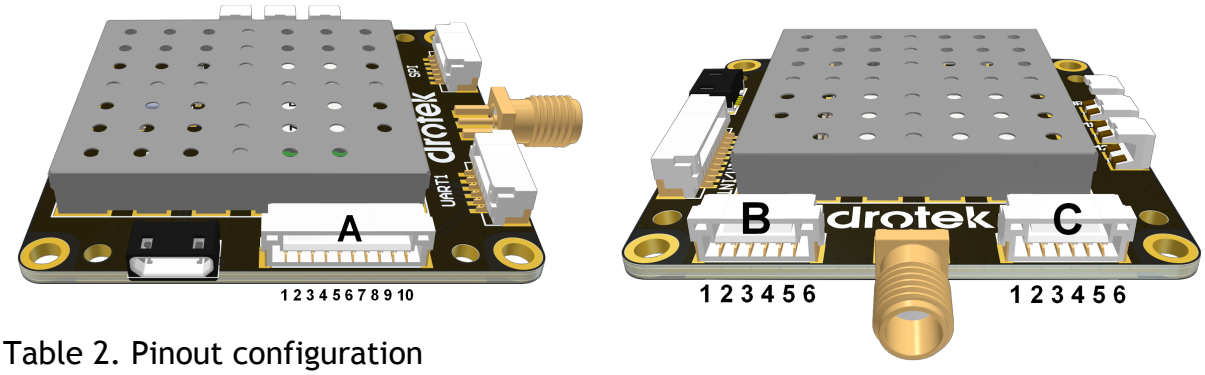


Table 2. Pinout configuration

	Pin	Name	Type	Function
UART2/TIM/INT	A1	5V IN	P	5V input
	A2	UART2 RX	I/O	UART2 receive NMEA/RTCM data
	A3	UART2 TX	I/O	UART2 transmit NMEA/RTCM data
	A4	RESET	I	F9T RESET input
	A5	SAFEBOOT	I	F9T SAFEBOOT input
	A6	EXTINT 1	O	External interrupt 1
	A7	EXTINT 2	O	External interrupt 2
	A8	TIMEPULSE 1	O	External interrupt on Timepulse 1
	A9	TIMEPULSE 2	O	External interrupt on Timepulse 2
	A10	GND	P	Ground reference
UART 1	B1	5V IN	P	5V input
	B2	UART1 RX / SPI MOSI	I/O	UART1 receive **OR** SPI MOSI
	B3	UART1 TX / SPI MISO	I/O	UART1 transmit **OR** SPI MISO
	B4	I2C SCL / SPI SCLK	I	I2C clock **OR** SPI clock
	B5	I2C SDA / SPI CS	I/O	I2C data **OR** SPI chip select
	B6	GND	P	Ground reference
SPI	C1	5V SPI	P	5V input to select SPI
	C2	SPI CLK	I	SPI clock input
	C3	SPI MOSI	I/O	SPI Master Output Slave Input

SPI	C4	SPI MISO	I/O	SPI Master Input Slave Output
	C5	SPI CS	I	SPI chip select input
	C6	GND	P	Ground reference

P : Power / I : Input / O : Output

2. Specifications

@Vdd = 5V, T = 25°C unless otherwise noted

Table 3. DP0701 mechanical and electrical specifications

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Vusb	USB supply voltage		4.5	5.0	5.5	V
Vdd	Internal supply voltage			3.3		V
Vdd_IO	Supply voltage for I/O			3.3		V
Idd	Current consumption	w/o active antenna		50		mA
		w/ TW7972 antenna		130		mA
Vil	IO pin low level input voltage		0		0.8	V
Vih	IO pin high level input voltage		2		Vdd+ 0.3	V
Vol	IO pin low level output voltage	Iol = 2mA			0.4	V
Voh	IO pin high level output voltage	Ioh = 2mA	Vdd- 0.4			V
W	Weight	w/o active antenna		18		g
Top	Operating temperature		-20		+70	°C

Table 4. DP0701 general performance

Parameter	Specifications	Value
Receiver type	Multi-band GNSS receiver for timing applications	
Accuracy of Timepulse	Absolute timing mode Differential timing mode	5ns 2.5ns
Frequency of Timepulse	Configurable	0.25 Hz to 25MHz
Timepulse Jitter		±4ns
Timemark Resolution		8ns
Operational limits	Dynamics Altitude Velocity	< 4g 50,000 m 500 m/s
Velocity accuracy		0.05 m/s
Dynamic heading accuracy		0.3deg

Table 5. DP0701 performance in different GNSS mode

GNSS	Parameter	GPS+GLO+GAL +BDS	GPS+GLO	GPS+BDS	GPS
Acquisition	Cold start Hot start Aided start	24 s 2 s 2 s	26 s 2 s 2 s	28 s 2 s 2 s	29 s 2 s 2 s
Navigation update rate	PVT	8Hz	15Hz	15Hz	20Hz
Horizontal pos. accuracy	Standalone	2.0m CEP	2.0m CEP	2.0m CEP	2.0m CEP
Sensitivity	Tracking & Nav. Reacquisition Cold start Hot start	-167 dBm -160 dBm -148 dBm -157 dBm			

3. Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

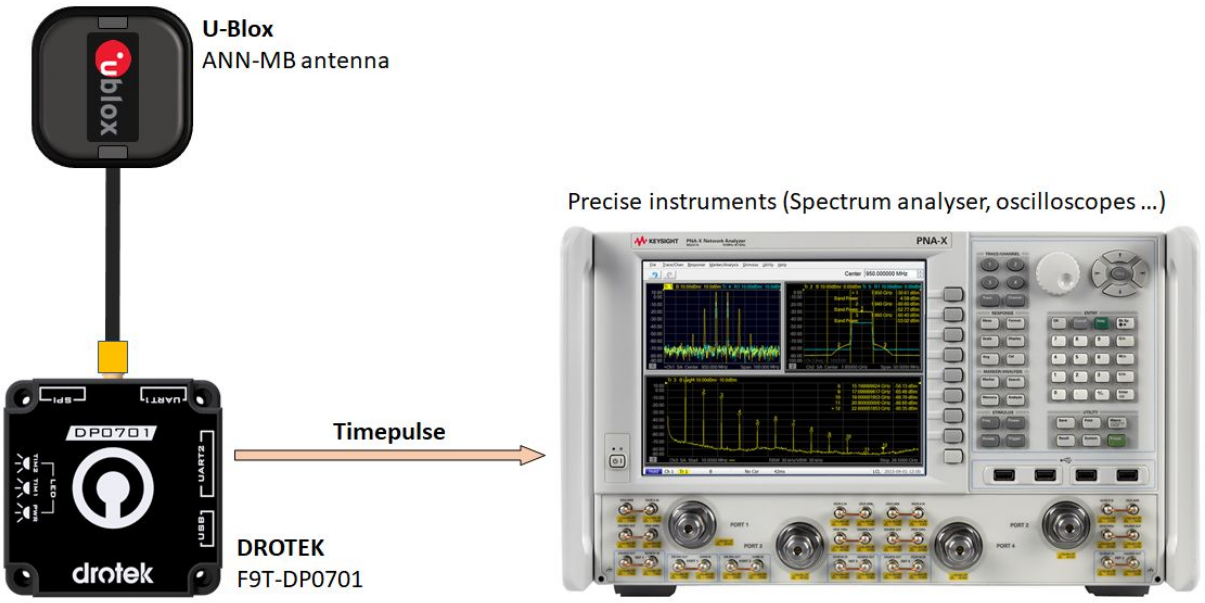
Table 6. DP0701 absolute maximum ratings

Symbol	Parameter	Maximum value	Unit
Vusb	USB supply voltage	-0.3 to +6	V
Vdd	Internal supply voltage	-0.5 to +3.6	V
Vdd_IO	I/O pins supply voltage	-0.5 to Vdd+0.5	V
Icc_RF	RF output current	100	mA
Prfin	Input power at RF_IN	10	dBm
TOP	Operating temperature	-20 to +70	°C
TSTG	Storage temperature	-40 to +80	°C

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

4. Applications

Figure 2. The DP0701 used as a precise timebase with low jitter for high precision radio-frequency equipments



U-blox ANN-MB antenna : https://store.drotek.com/u-blox-ann-mb-multi-band-antenna

5. Communication interfaces

There are several communications interfaces including UART, SPI, I2C and USB. All the inputs have internal pull-up resistors in normal operation and can be left open if not used. All the PIOs are supplied by VCC, therefore all the voltage levels of the PIO pins are related to Vdd supply voltage.

5.1 UART Interface

There are two UART interfaces: UART1 and UART2. UART1 and UART2 operate up to and including a speed of 921600 baud. No hardware flow control on UART1 and UART2 is supported. UART1 is enabled by default if there is no 5V input voltage on pin A1 (5V SPI).

Figure 3. UART chronogram specifications

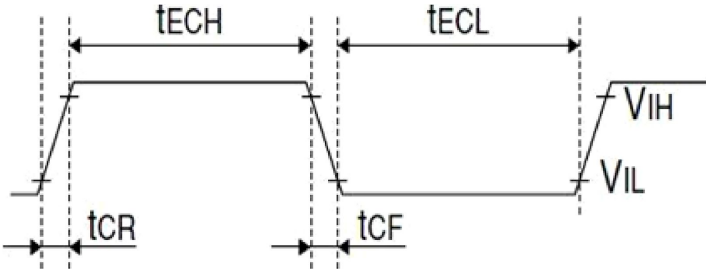


Table 7. DP0701 serial UART timing specifications

Symbol	Parameter	Min.	Max.	Unit
Vil	LOW-LEVEL input voltage	0	0.2xVdd	V
Vih	HIGH-LEVEL input voltage	0.7xVdd	Vdd+0.3	V
tECH	HIGH period of external data input	0	0.4	µs
tECL	LOW period of external data input	TBA	TBA	µs
Ru	Baudrate	9600	921600	bps
tCR	Rise time of data		5	ns
tCF	Fall time of data		5	ns

5.2 SPI interface

The DP0601 has an SPI slave interface that can be selected by supplying a 5V voltage on pin A1 (5V SPI). The SPI slave interface is shared with UART1. The SPI pins available are: SPI_MISO (TXD), SPI_MOSI (RXD), SPI_CS_N, SPI_CLK. The SPI interface is designed to allow communication to a host CPU. The interface can be operated in slave mode only. Note that SPI is not available in the default configuration because its pins are shared with the UART and I2C interfaces. The maximum transfer rate using SPI is 125 kB/s and the maximum SPI clock frequency is 5.5 MHz.
This section provides SPI timing values for the ZED-F9P slave operation. The following tables present timing values under different capacitive loading conditions. Default SPI configuration is CPOL = 0 and CPHA = 0.

Figure 4. SPI chronogram specifications

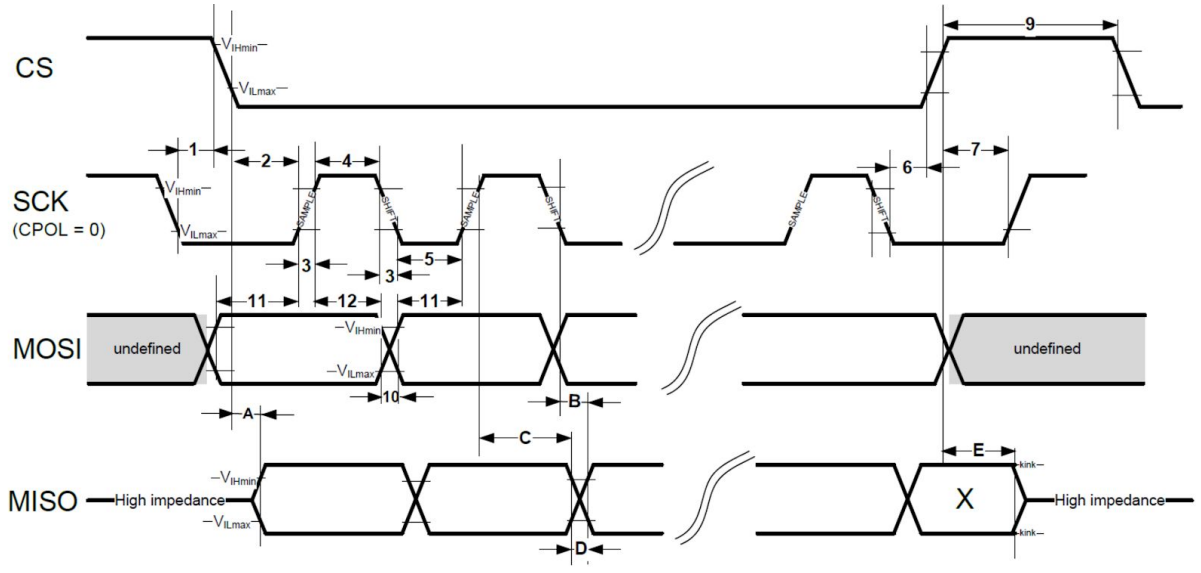


Table 8. DP0701 SPI timing specifications

Timing value @ 20pF load	Min [ns]	Max [ns]
"A" - MISO data valid time (CS)	19	52
"B" - MISO data valid time (SCK) weak driver mode	25	51
"C" - MISO data hold time	117	137
"D" - MISO rise/fall time, weak driver mode	6	16
"E" - MISO data disable lag time	20	32

5.3 Slave I2C interface

An I2C compliant interface is available for communication with an external host CPU. The interface can be operated in slave mode only. It is fully compatible with Fast-Mode of the I2C industry standard. Since the maximum SCL clock frequency is 400 kHz, the maximum bit rate is 400 kbit/s. The interface stretches the clock when slowed down while serving interrupts, therefore the real bit rates may be slightly lower.

Note : The I2C interface is only available with the UART default mode. If the SPI interface is selected by supplying a 5V onto the A1 pin (5V SPI), the I2C is not available.

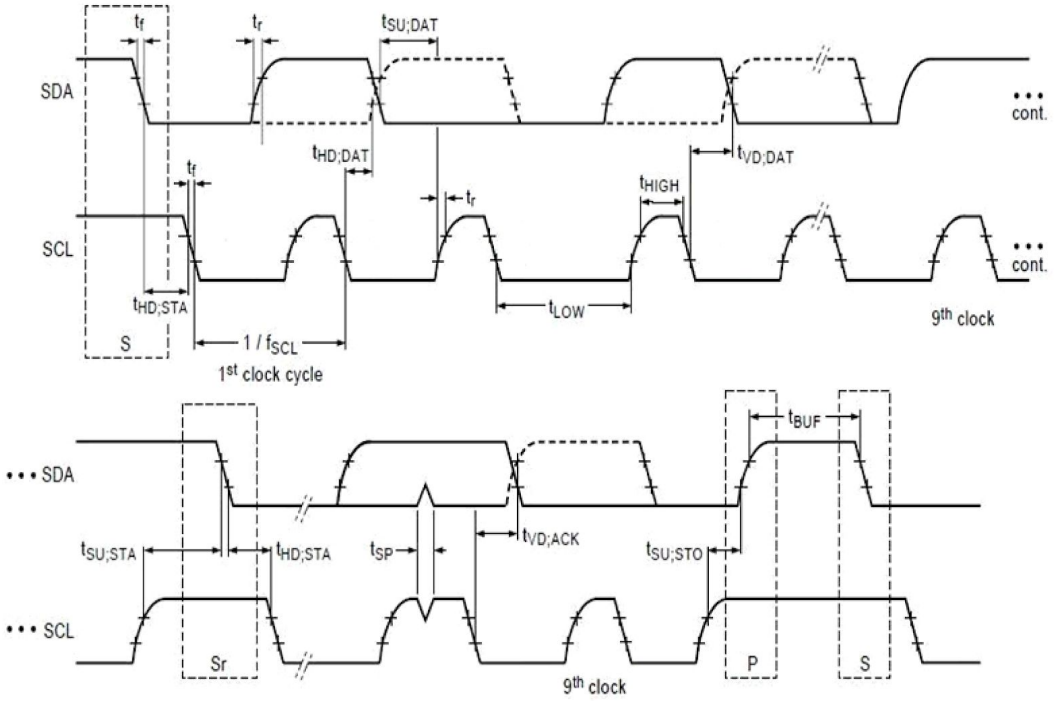


Table 9. DP0701 I2C timing specifications

Symbol	Parameter	Min	Max	Unit
Vil	LOW-LEVEL input voltage	Vss-0.3	0.3xVdd	V
Vih	HIGH-LEVEL input voltage	0.7xVdd	Vdd+0.3	V
Vol	LOW-LEVEL output voltage		0.4	V
Voh	HIGH-LEVEL output voltage	Vdd-0.4		V
Fscl	SCL clock frequency	0	400	KHz

5.4 USB interface

A USB interface, which is compatible to USB version 2.0 FS (Full Speed, 12 Mbit/s), can be used for communication as an alternative to the UART.

6. Mechanical drawings

Figure 6. DP0701 v1.0 mechanical drawing

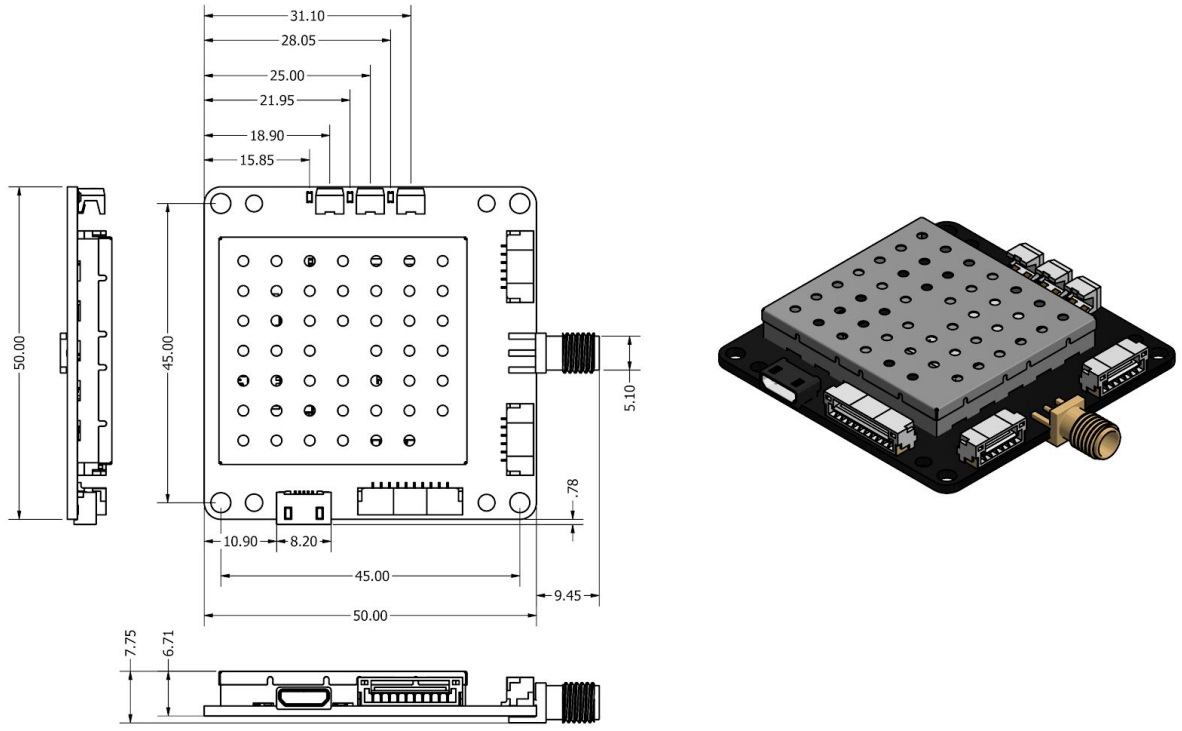
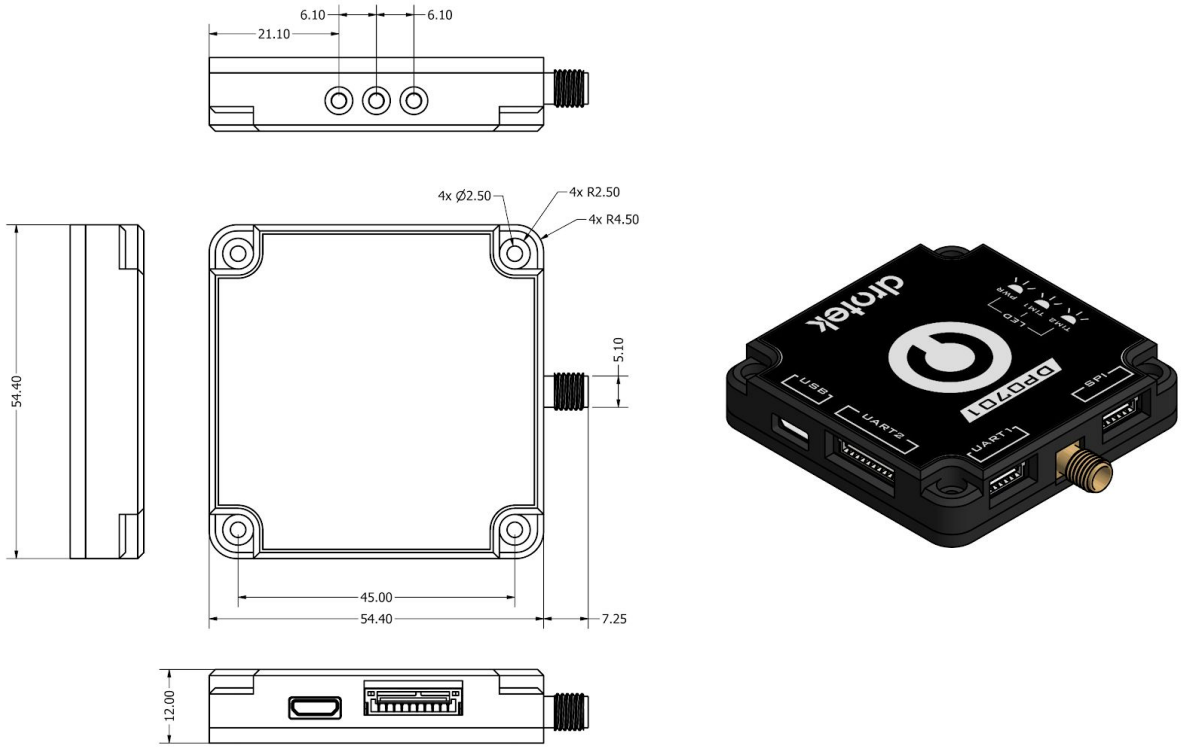


Figure 7. DP0701 v1.0 mechanical drawing enclosure version



7. Revision history

Table 10. Document revision history

Date	Revision	Changes
01-Apr-2020	1.0	DrotekDoc_0916 / Initial release

8. Appendix

U-blox ZED-F9T datasheet : https://www.u-blox.com/en/docs/UBX-18053713

U-blox ZED-F9T integration manual : https://www.u-blox.com/en/docs/UBX-19005590

U-blox ZED-F9T interface description : https://www.u-blox.com/en/docs/UBX-18053584

IMPORTANT NOTICE – PLEASE READ CAREFULLY

Drotek reserves the right to make changes, corrections, enhancements, modifications, and improvements to Drotek products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on Drotek products before placing orders. Drotek products are sold pursuant to Drotek's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of Drotek products and Drotek assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by Drotek herein.

Resale of Drotek products with provisions different from the information set forth herein shall void any warranty granted by Drotek for such product.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.