

Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page		
(\$FF)	Reserved	-	-	-	_	-	-	-	_			
	Reserved	-	-	-	-	-	-	-	-			
(\$9E)	Reserved	-	-	-	-	-	-	-	-			
(\$9D)	UCSR1C	-	UMSEL1	UPM11	UPM10	USBS1	UCSZ11	UCSZ10	UCPOL1	191		
(\$9C)	UDR1				USART1 I/C	Data Register				189		
(\$9B)	UCSR1A	RXC1	TXC1	UDRE1	FE1	DOR1	UPE1	U2X1	MPCM1	189		
(\$9A)	UCSR1B	RXCIE1	TXCIE1	UDRIE1	RXEN1	TXEN1	UCSZ12	RXB81	TXB81	190		
(\$99)	UBRR1L		1	1	USART1 Baud	Rate Register Lov	N			193 193		
(\$98)	UBRR1H	-	USART1 Baud Rate Register High									
(\$97)	Reserved	_	-	-	_	-	_	_	-			
(\$96)	Reserved	_	-	_	_	_	-	_	-			
(\$95)	UCSR0C	_	UMSEL0	UPM01	UPM00	USBS0	UCSZ01	UCSZ00	UCPOL0	191		
(\$94)	Reserved	_	_	-	-	-	_	_	-			
(\$93)	Reserved	-	-	_	-	-	_	_	-			
(\$92)	Reserved	-	_	_	-	_	-	-	-			
(\$91)	Reserved	-	-	_	-	-		_	_			
(\$90)	UBRR0H	-	_	-	-		USART0 Baud F	Rate Register High	h T	193		
(\$8F)	Reserved	-	-	_	_	-	-	_	-			
(\$8E)	Reserved	-	_	_	-	_	-	-	-			
(\$8D)	Reserved	-	_	_	-	_	_	_	-			
(\$8C)	TCCR3C	FOC3A	FOC3B	FOC3C	_	-	-	-	-	135		
(\$8B)	TCCR3A	COM3A1	COM3A0	COM3B1	COM3B0	COM3C1	COM3C0	WGM31	WGM30	131		
(\$8A)	TCCR3B	ICNC3	ICES3	-	WGM33	WGM32	CS32	CS31	CS30	134		
(\$89)	TCNT3H				er/Counter3 – Co					136		
(\$88)	TCNT3L				er/Counter3 – Co					136		
(\$87)	OCR3AH				unter3 – Output C					136		
(\$86)	OCR3AL				unter3 – Output C					136		
(\$85)	OCR3BH				unter3 – Output C					137		
(\$84)	OCR3BL				unter3 – Output C		•			137		
(\$83)	OCR3CH				unter3 – Output C					137		
(\$82)	OCR3CL				unter3 – Output C		•			137		
(\$81)	ICR3H				Counter3 – Input (137		
(\$80)	ICR3L				Counter3 – Input		1 .			137		
(\$7F)	Reserved	_	_	_	-	_	-	_	_			
(\$7E)	Reserved	_	_	- TICIFO	-	- OCIE0D	- TOIE0	-	-	100		
(\$7D)	ETIMSK	_	-	TICIE3	OCIE3A	OCIE3B OCF3B	TOIE3 TOV3	OCIE3C OCF3C	OCIE1C	138 139		
(\$7C) (\$7B)	ETIFR Reserved	_	_	ICF3	OCF3A	– UCF3B	-	– –	OCF1C -	139		
(\$7A)	TCCR1C	FOC1A	FOC1B	FOC1C	_	_		_	_	135		
(\$79)	OCR1CH	FOCIA	FOCIB		unter1 – Output C			_	_	136		
(\$78)	OCR1CL									136		
(\$77)	Reserved	_	Timer/Counter1 – Output Compare Register C Low Byte									
(\$76)	Reserved	_	_	_	_	_	_	_	_			
(\$75)	Reserved	_	_	_	_	_	_	_	_			
(\$74)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	_	TWIE	206		
(\$73)	TWDR	Two-wire Serial Interface Data Register										
(\$72)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	208 208		
(\$71)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	_	TWPS1	TWPS0	207		
(\$70)	TWBR	Two-wire Serial Interface Bit Rate Register										
(\$6F)	OSCCAL					ibration Register	-			206 39		
(\$6E)	Reserved	_	_	_	_	-	-	-	-			
(\$6D)	XMCRA	_	SRL2	SRL1	SRL0	SRW01	SRW00	SRW11		29		
(\$6C)	XMCRB	XMBK	-	_	-	_	XMM2	XMM1	XMM0	31		
(\$6B)	Reserved	_	_	_	-	-	-	_	-			
(\$6A)	EICRA	ISC31	ISC30	ISC21	ISC20	ISC11	ISC10	ISC01	ISC00	87		
(\$69)	Reserved	_	_	_	_	_	-	-	-			
(\$68)	SPMCSR	SPMIE	RWWSB	_	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	279		
(\$67)	Reserved	_	_	_	-	-	-	-	-			
(\$66)	Reserved	_	_	_	_	_	-	-	-			
(\$65)	PORTG	_	_	_	PORTG4	PORTG3	PORTG2	PORTG1	PORTG0	86		
	_			_	DDG4	DDG3	DDG2	DDG1	DDG0	86		
(\$64)	DDRG	_	_		DDG4	DDG3	DDGZ	DDG1	DDG0	- 00		
(\$64) (\$63)	DDRG PING	-	_	_	PING4	PING3	PING2	PING1	PING0	86		

Register Summary (Continued)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page	
(\$61)	DDRF	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0	86	
(\$60)	Reserved	-	-	-	-	-	-	-	-		
\$3F (\$5F)	SREG	I	Т	Н	S	V	N	Z	С	9	
\$3E (\$5E)	SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	12 12	
\$3D (\$5D)	SPL	SP7									
\$3C (\$5C)	XDIV	XDIVEN	41								
\$3B (\$5B)	RAMPZ	-	12								
\$3A (\$5A)	EICRB	ISC71	ISC70	ISC61	ISC60	ISC51	ISC50	ISC41	ISC40	88	
\$39 (\$59)	EIMSK	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INTO	89	
\$38 (\$58) \$37 (\$57)	EIFR TIMSK	OCIE2	INTF6 TOIE2	INTF5 TICIE1	INTF4 OCIE1A	INTF3 OCIE1B	INTF TOIE1	OCIE0	INTF0 TOIE0	89 106, 138, 158	
\$36 (\$56)	TIFR	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	OCF0	TOV0	106, 139, 158	
\$35 (\$55)	MCUCR	SRE	SRW10	SE	SM1	SM0	SM2	IVSEL	IVCE	29, 42, 61	
\$34 (\$54)	MCUCSR	JTD	-	-	JTRF	WDRF	BORF	EXTRF	PORF	51, 256	
\$33 (\$53)	TCCR0	FOC0	WGM00	COM01	COM00	WGM01	CS02	CS01	CS00	101	
\$32 (\$52)	TCNT0					unter0 (8 Bit)				103	
\$31 (\$51)	OCR0			Tii	mer/Counter0 Ou	tput Compare Re	gister			103	
\$30 (\$50)	ASSR	-	-	-	_	AS0	TCN0UB	OCR0UB	TCR0UB	104	
\$2F (\$4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	COM1C1	COM1C0	WGM11	WGM10	131	
\$2E (\$4E)	TCCR1B	ICNC1	ICES1	-	WGM13	WGM12	CS12	CS11	CS10	134	
\$2D (\$4D)	TCNT1H			Time	er/Counter1 – Co	unter Register Hig	gh Byte			136	
\$2C (\$4C)	TCNT1L					unter Register Lo	•			136	
\$2B (\$4B)	OCR1AH					Compare Register				136	
\$2A (\$4A)	OCR1AL				•	Compare Register				136	
\$29 (\$49)	OCR1BH				· · · · · · · · · · · · · · · · · · ·	Compare Register				136	
\$28 (\$48)	OCR1BL				•	Compare Register	•			136	
\$27 (\$47) \$26 (\$46)	ICR1H					Capture Register Capture Register				137 137	
\$25 (\$45)	ICR1L TCCR2	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	156	
\$25 (\$45) \$24 (\$44)	TCON2	F002	WGIVIZU	COIVIZT		unter2 (8 Bit)	0322	U321	U320	158	
\$23 (\$43)	OCR2			Tir		tput Compare Re	nister			158	
\$22 (\$42)	OCDR	IDRD/OCDR7	OCDR6	OCDR5	OCDR4	OCDR3	OCDR2	OCDR1	OCDR0	253	
\$21 (\$41)	WDTCR	_	_	_	WDCE	WDE	WDP2	WDP1	WDP0	53	
\$20 (\$40)	SFIOR	TSM	-	-	-	ACME	PUD	PSR0	PSR321	70, 107, 143, 228	
\$1F (\$3F)	EEARH	-	-	-	_		EEPROM Addr	ess Register High		19	
\$1E (\$3E)	EEARL				EEPROM Addres	s Register Low B	yte			19	
\$1D (\$3D)	EEDR				EEPROM	Data Register				20	
\$1C (\$3C)	EECR	-	-	-	-	EERIE	EEMWE	EEWE	EERE	20	
\$1B (\$3B)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	84	
\$1A (\$3A)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	84	
\$19 (\$39)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	84	
\$18 (\$38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	84	
\$17 (\$37) \$16 (\$36)	DDRB PINB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	84 84	
\$16 (\$36) \$15 (\$35)	PORTC	PINB7 PORTC7	PINB6 PORTC6	PINB5 PORTC5	PINB4 PORTC4	PINB3 PORTC3	PINB2 PORTC2	PINB1 PORTC1	PINB0 PORTC0	84 84	
\$13 (\$33)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	84	
\$13 (\$33)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	85	
\$12 (\$32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	85	
\$11 (\$31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	85	
\$10 (\$30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	85	
\$0F (\$2F)	SPDR				SPI Da	ta Register				168	
\$0E (\$2E)	SPSR	SPIF	WCOL	-	-	-	-	-	SPI2X	168	
\$0D (\$2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	166	
\$0C (\$2C)	UDR0		1	1		Data Register	1	1	1	189	
\$0B (\$2B)	UCSR0A	RXC0	TXC0	UDRE0	FE0	DOR0	UPE0	U2X0	MPCM0	189	
\$0A (\$2A)	UCSR0B	RXCIE0	TXCIE0	UDRIE0	RXEN0	TXEN0	UCSZ02	RXB80	TXB80	190	
\$09 (\$29)	UBRR0L	465	4050	460		Rate Register Lo		40'0'	40:00	193	
\$08 (\$28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	228	
\$07 (\$27) \$06 (\$26)	ADMUX	REFS1	REFS0	ADLAR	MUX4 ADIF	MUX3 ADIE	MUX2 ADPS2	MUX1	MUX0	244	
\$06 (\$26) \$05 (\$25)	ADCSRA ADCH	ADEN	ADSC	ADFR			ADP52	ADPS1	ADPS0	245 246	
\$03 (\$23)	ADCL	ADC Data Register High Byte ADC Data Register Low byte							246		
\$03 (\$23)	PORTE	PORTE7	PORTE6	PORTE5	PORTE4	PORTE3	PORTE2	PORTE1	PORTE0	85	
\$02 (\$22)	DDRE	DDE7	DDE6	DDE5	DDE4	DDE3	DDE2	DDE1	DDE0	85	
. (+/											





Register Summary (Continued)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
\$01 (\$21)	PINE	PINE7	PINE6	PINE5	PINE4	PINE3	PINE2	PINE1	PINE0	85
\$00 (\$20)	PINF	PINF7	PINF6	PINF5	PINF4	PINF3	PINF2	PINF1	PINF0	86

Notes: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

2. Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers \$00 to \$1F only.