

## Interrupts

This section describes the specifics of the interrupt handling as performed in ATmega128. For a general explanation of the AVR interrupt handling, refer to “Reset and Interrupt Handling” on page 13.

### Interrupt Vectors in ATmega128

**Table 23.** Reset and Interrupt Vectors

Vector No.	Program Address <sup>(2)</sup>	Source	Interrupt Definition
1	\$0000 <sup>(1)</sup>	RESET	External Pin, Power-on Reset, Brown-out Reset, Watchdog Reset, and JTAG AVR Reset
2	\$0002	INT0	External Interrupt Request 0
3	\$0004	INT1	External Interrupt Request 1
4	\$0006	INT2	External Interrupt Request 2
5	\$0008	INT3	External Interrupt Request 3
6	\$000A	INT4	External Interrupt Request 4
7	\$000C	INT5	External Interrupt Request 5
8	\$000E	INT6	External Interrupt Request 6
9	\$0010	INT7	External Interrupt Request 7
10	\$0012	TIMER2 COMP	Timer/Counter2 Compare Match
11	\$0014	TIMER2 OVF	Timer/Counter2 Overflow
12	\$0016	TIMER1 CAPT	Timer/Counter1 Capture Event
13	\$0018	TIMER1 COMPA	Timer/Counter1 Compare Match A
14	\$001A	TIMER1 COMPB	Timer/Counter1 Compare Match B
15	\$001C	TIMER1 OVF	Timer/Counter1 Overflow
16	\$001E	TIMER0 COMP	Timer/Counter0 Compare Match
17	\$0020	TIMER0 OVF	Timer/Counter0 Overflow
18	\$0022	SPI, STC	SPI Serial Transfer Complete
19	\$0024	USART0, RX	USART0, Rx Complete
20	\$0026	USART0, UDRE	USART0 Data Register Empty
21	\$0028	USART0, TX	USART0, Tx Complete
22	\$002A	ADC	ADC Conversion Complete
23	\$002C	EE READY	EEPROM Ready
24	\$002E	ANALOG COMP	Analog Comparator
25	\$0030 <sup>(3)</sup>	TIMER1 COMPC	Timer/Counter1 Compare Match C
26	\$0032 <sup>(3)</sup>	TIMER3 CAPT	Timer/Counter3 Capture Event
27	\$0034 <sup>(3)</sup>	TIMER3 COMPA	Timer/Counter3 Compare Match A
28	\$0036 <sup>(3)</sup>	TIMER3 COMPB	Timer/Counter3 Compare Match B
29	\$0038 <sup>(3)</sup>	TIMER3 COMPC	Timer/Counter3 Compare Match C
30	\$003A <sup>(3)</sup>	TIMER3 OVF	Timer/Counter3 Overflow

**Table 23.** Reset and Interrupt Vectors (Continued)

Vector No.	Program Address <sup>(2)</sup>	Source	Interrupt Definition
31	\$003C <sup>(3)</sup>	USART1, RX	USART1, Rx Complete
32	\$003E <sup>(3)</sup>	USART1, UDRE	USART1 Data Register Empty
33	\$0040 <sup>(3)</sup>	USART1, TX	USART1, Tx Complete
34	\$0042 <sup>(3)</sup>	TWI	Two-wire Serial Interface
35	\$0044 <sup>(3)</sup>	SPM READY	Store Program Memory Ready

- Notes:
1. When the BOOTRST fuse is programmed, the device will jump to the Boot Loader address at reset, see “Boot Loader Support – Read-While-Write Self-Programming” on page 275.
  2. When the IVSEL bit in MCUCR is set, interrupt vectors will be moved to the start of the Boot Flash section. The address of each interrupt vector will then be address in this table added to the start address of the boot Flash section.
  3. The Interrupts on address \$0030 - \$0044 do not exist in ATmega103 compatibility mode.

Table 24 shows Reset and interrupt vectors placement for the various combinations of BOOTRST and IVSEL settings. If the program never enables an interrupt source, the interrupt vectors are not used, and regular program code can be placed at these locations. This is also the case if the Reset Vector is in the Application section while the interrupt vectors are in the Boot section or vice versa.

**Table 24.** Reset and Interrupt Vectors Placement

BOOTRST	IVSEL	Reset Address	Interrupt Vectors Start Address
1	0	\$0000	\$0002
1	1	\$0000	Boot Reset Address + \$0002
0	0	Boot Reset Address	\$0002
0	1	Boot Reset Address	Boot Reset Address + \$0002

- Note: The Boot Reset Address is shown in Table 112 on page 286. For the BOOTRST fuse “1” means unprogrammed while “0” means programmed.