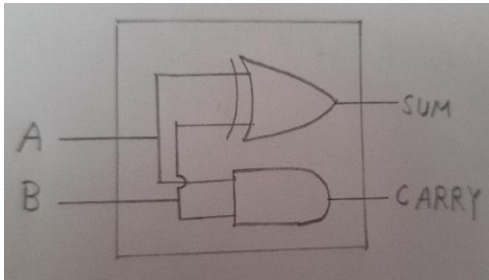


DIGITAL DESIGN

LAB-1 REPORT

1. Half-Adder



Logic Code:

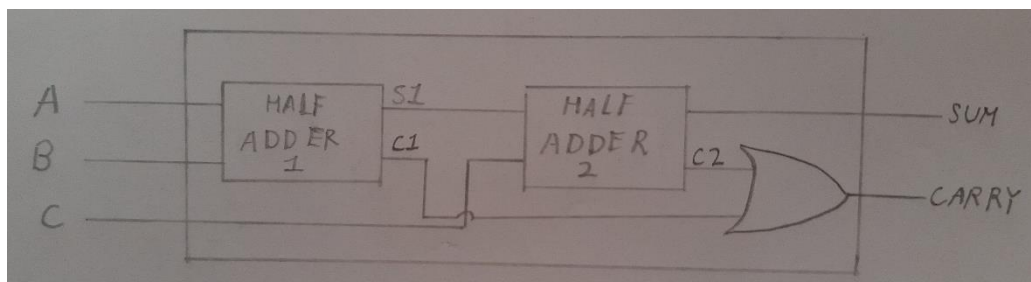
```
module half_addder (A,B,sum,carry);  
input A,B;  
output sum,carry;  
  
assign sum=A^B;  
assign carry=A&B;  
endmodule
```

Test Bench:

```
module test_half_addder;  
reg A,B;  
wire sum,carry;  
half_addder H1(A,B,sum,carry);  
initial  
begin  
    A=1'b0;  
    B=1'b0;  
    #10 A=1'b1;  
    #10 A=1'b0; B=1'b1;  
    #10 A=1'b1;  
    #10 A=1'b0; B=1'b0;  
end  
initial #40 $finish;  
endmodule
```



2. FULL ADDER (USING HALF ADDER)



Logic Code:

```

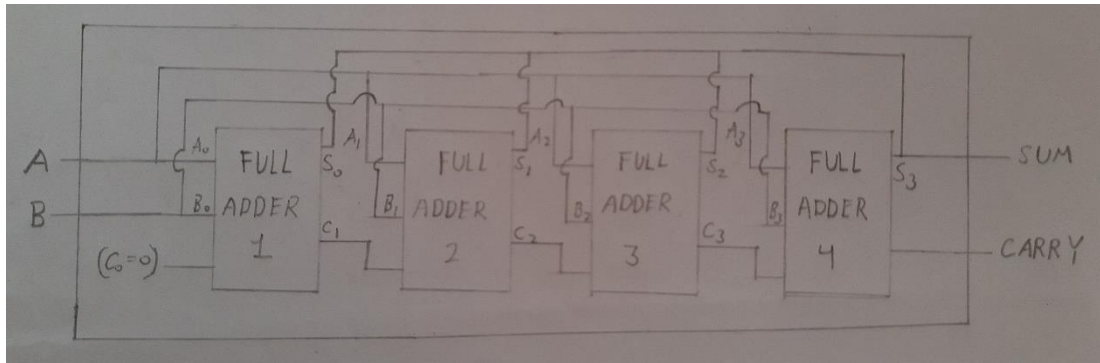
module full_adder(A,B,C,sum,carry);
input A,B,C;
output sum,carry;
wire S1,C1,C2;

half_adder H1(A,B,S1,C1);
half_adder H2(S1,C,sum,C2);
assign carry=C1|C2;
endmodule

```



3. FOUR BIT ADDER



Logic Code:

```
module four_bit_adder(A,B,S,carry);
input [3:0]A,B;
output [3:0]S;
output carry;
reg C0=1'b0;
wire C1,C2,C3;

full_adder FA1(A[0],B[0],C0,S[0],C1);
full_adder FA2(A[1],B[1],C1,S[1],C2);
full_adder FA3(A[2],B[2],C2,S[2],C3);
full_adder FA4(A[3],B[3],C3,S[3],carry);
endmodule
```

Test Bench:

```
module test_four_bit_adder;
reg [3:0]A,B;
wire [3:0]S;
wire carry;
four_bit_adder FBA1(A,B,S,carry);
initial
begin
    A=4'b0001; B=4'b0010;
    #10 A=4'b1100; B=4'b0100;
    #10 A=4'b0011; B=4'b1000;
    #10 A=4'b1111; B=4'b1111;
    #10 A=4'b0111; B=4'b0100;
    #10 A=4'b1010; B=4'b0110;
    #10 A=4'b1110; B=4'b0101;
    #10 A=4'b0000; B=4'b1011;
    #10 A=4'b1011; B=4'b0100;
    #10 A=4'b1100; B=4'b0111;
end
initial #100 $finish;
endmodule
```

Name	Value	Name	Value
A[3:0]	0001	A[3:0]	1100
B[3:0]	0010	B[3:0]	0100
S[3:0]	0011	S[3:0]	0000
carry	0	carry	1

Name	Value	Name	Value
A[3:0]	0011	A[3:0]	1111
B[3:0]	1000	B[3:0]	1111
S[3:0]	1011	S[3:0]	1110
carry	0	carry	1

Name	Value	Name	Value
A[3:0]	0111	A[3:0]	1010
B[3:0]	0100	B[3:0]	0110
S[3:0]	1011	S[3:0]	0000
carry	0	carry	1

Name	Value	Name	Value
A[3:0]	1110	A[3:0]	0000
B[3:0]	0101	B[3:0]	1011
S[3:0]	0011	S[3:0]	1011
carry	1	carry	0

Name	Value	Name	Value
A[3:0]	1011	A[3:0]	1100
B[3:0]	0100	B[3:0]	0111
S[3:0]	1111	S[3:0]	0011
carry	0	carry	1

