

521 Digital ASIC Design

Title: HW- 2

For

By: Saroj Shah

Date: Feb 18, 2026

HW-2, Professor Seetal Potluri

Introduction and Summary:

In this HW- 2 assignment, we are designing, and simulating fundamental combinational logic circuits using Verilog HDL and Cadence Xcelium. The following digital building blocks were implemented:

- 2-Input XOR Gate
- 1-Bit Full Adder
- 4-Bit Subtractor (using Full Adders)

All designs were written in Verilog at gate-level and structural modeling style.

Testbenches were developed for each module to verify correctness through simulation and waveform analysis in SimVision..

Materials:

- Computer system
- Cadence Xcelium (xrun)
- SimVision waveform viewer
- MobaXterm (remote terminal access)

Data:

Please refer to the screenshot provided below:

1. Two in-put XOR Gate:

The XOR gate was implemented using the Boolean equation:

$$Y = A'B + AB'$$

The design uses: 2 NOT gates; 2 AND gates; 1 OR gate

```

[ss819183@ceashpc-12 ~]$ cd cadence
[ss819183@ceashpc-12 cadence]$ module load cadence/IC618-v2
[ss819183@ceashpc-12 cadence]$ xrun -compile HW2/XOR2.v
TOOL: xrun(64) 19.09-s001: Started on Feb 15, 2026 at 19:53:19 EST
xrun(64): 19.09-s001: (c) Copyright 1995-2019 Cadence Design Systems, Inc.
file: HW2/XOR2.v
module worklib.XOR2.v
errors: 0, warnings: 0
TOOL: xrun(64) 19.09-s001: Exiting on Feb 15, 2026 at 19:53:19 EST (total: 00:00:00)
[ss819183@ceashpc-12 cadence]$ xrun -compile HW2/XOR2_tb.v
TOOL: xrun(64) 19.09-s001: Started on Feb 15, 2026 at 19:53:34 EST
xrun(64): 19.09-s001: (c) Copyright 1995-2019 Cadence Design Systems, Inc.
file: HW2/XOR2_tb.v
module worklib.XOR2_tb.v
errors: 0, warnings: 0
TOOL: xrun(64) 19.09-s001: Exiting on Feb 15, 2026 at 19:53:34 EST (total: 00:00:00)
[ss819183@ceashpc-12 cadence]$ xrun -gui -access rwc HW2/XOR2.v HW2/XOR2_tb.v
TOOL: xrun(64) 19.09-s001: Started on Feb 15, 2026 at 19:53:48 EST
xrun(64): 19.09-s001: (c) Copyright 1995-2019 Cadence Design Systems, Inc.
Caching library 'worklib' ..... Done
Elaborating the design hierarchy:
Top level design units:
XOR2_tb
Building instance overlay tables: ..... Done
Generating native compiled code:
worklib.XOR2_tb.v <8x7becb0e2>
streams: 5, words: 5614
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
Instances Unique
Modules: 2 2
Primitives: 5 3
Registers: 2 2
Scalar wires: 2 -
Initial blocks: 2 2
Pseudo assignments: 2 2
Simulation timescale: 1ps
Writing initial simulation snapshot: worklib.XOR2_tb.v
waiting for SimVision/Indago to connect...

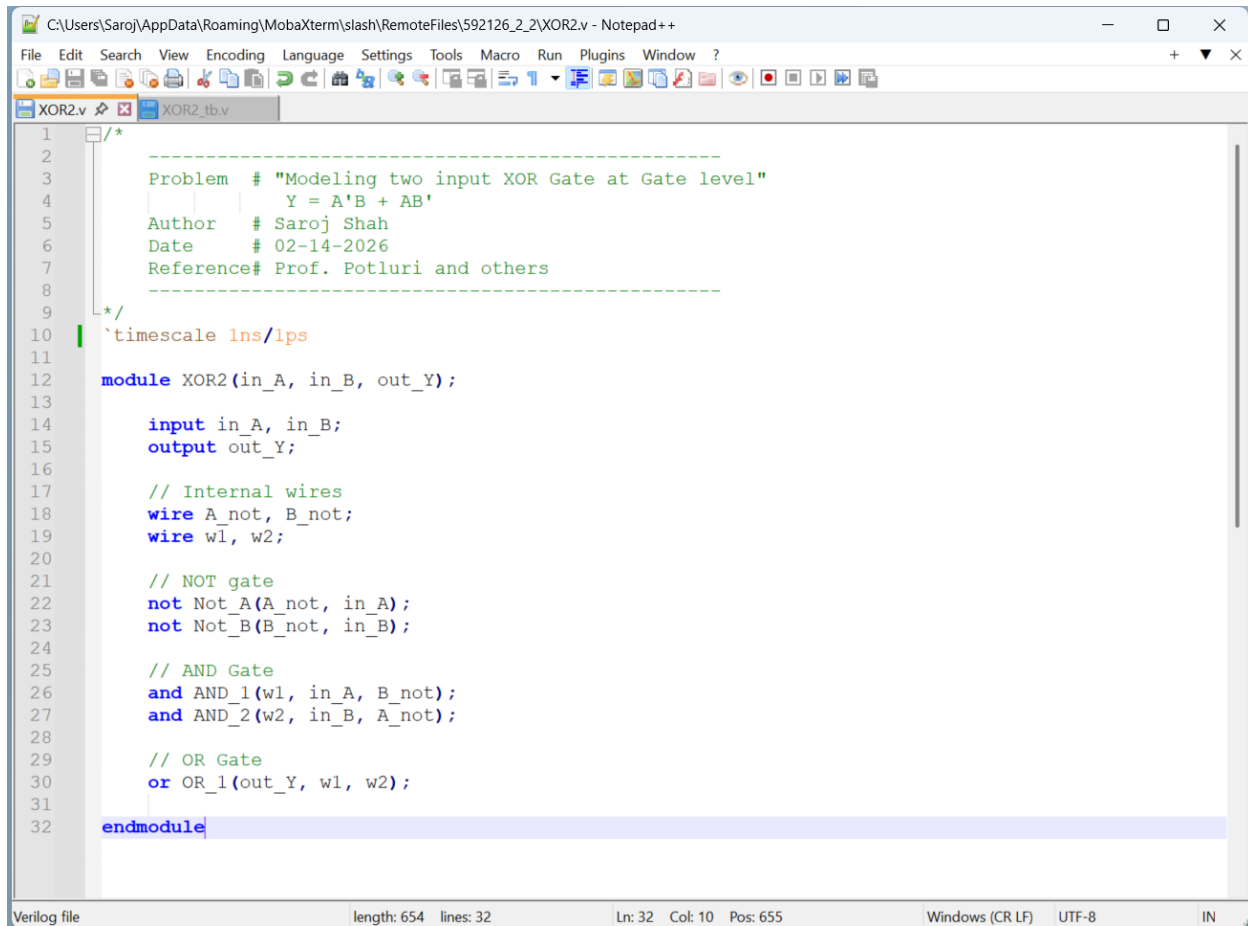
-----
Relinquished control to SimVision...
xcelium> source /network/rit/lab/ceashpc/software/cadence/XCELIUM1909/tools/inca/files/xmsimrc
xcelium> error starting plugin /network/rit/lab/ceashpc/software/cadence/XCELIUM1909/tools/simvision/plugins/64bit/in
voke_ida.so
child process exited abnormally

```

UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: <https://mobaxterm.mobatek.net>

Fig: 1 (MobaXterm window)

The above figure shows the code compiling and Cadence Xcelium running without any error.



```
1  /*
2
3  Problem # "Modeling two input XOR Gate at Gate level"
4          Y = A'B + AB'
5  Author  # Saroj Shah
6  Date    # 02-14-2026
7  Reference# Prof. Potluri and others
8  -----
9  */
10 `timescale 1ns/1ps
11
12 module XOR2(in_A, in_B, out_Y);
13
14     input in_A, in_B;
15     output out_Y;
16
17     // Internal wires
18     wire A_not, B_not;
19     wire w1, w2;
20
21     // NOT gate
22     not Not_A(A_not, in_A);
23     not Not_B(B_not, in_B);
24
25     // AND Gate
26     and AND_1(w1, in_A, B_not);
27     and AND_2(w2, in_B, A_not);
28
29     // OR Gate
30     or OR_1(out_Y, w1, w2);
31
32 endmodule
```

Verilog file length: 654 lines: 32 Ln: 32 Col: 10 Pos: 655 Windows (CR LF) UTF-8 IN

Fig: 2A (Code for XOR2 Gate)

```

1  /*
2
3  Problem # "Testbench for two input XOR Gate"
4  Author  # Saroj Shah
5  Date    # 02-14-2026
6  Reference# Prof. Potluri and others
7  */
8
9
10 `timescale 1ns/1ps
11
12 module XOR2_tb;
13
14     reg in_A;
15     reg in_B;
16     wire out_Y;
17
18
19     // Instantiate
20     XOR2 XOR_gate(in_A, in_B, out_Y);
21
22     initial
23     begin
24         // Initializing inputs
25         in_A = 0;
26         in_B = 0;
27
28         #5 in_A = 1; in_B = 0;
29
30         #5 in_A = 0; in_B = 1;
31
32         #5 in_A = 1; in_B = 1;
33
34         #5 $finish; // End simulation
35     end
36
37     initial
38     $monitor("Time=%0t | in_A = %b, in_B = %b, out_Y = %b\n", $time, in_A, in_B, out_Y);
39
40 endmodule

```

Fig: 2B (Code for XOR2 Testbench Gate)

Figure 2A and 2B shows the code for XOR gate and XOR gate testbench. The testbench code is used to run the simulation.

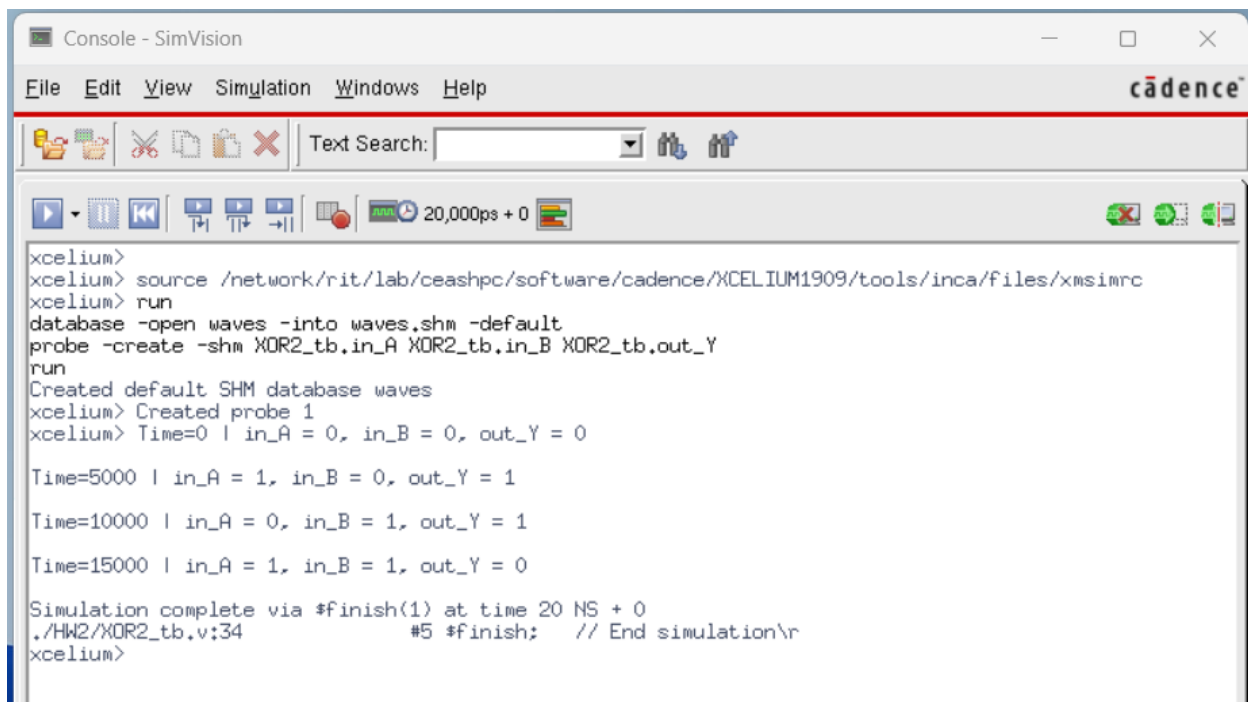
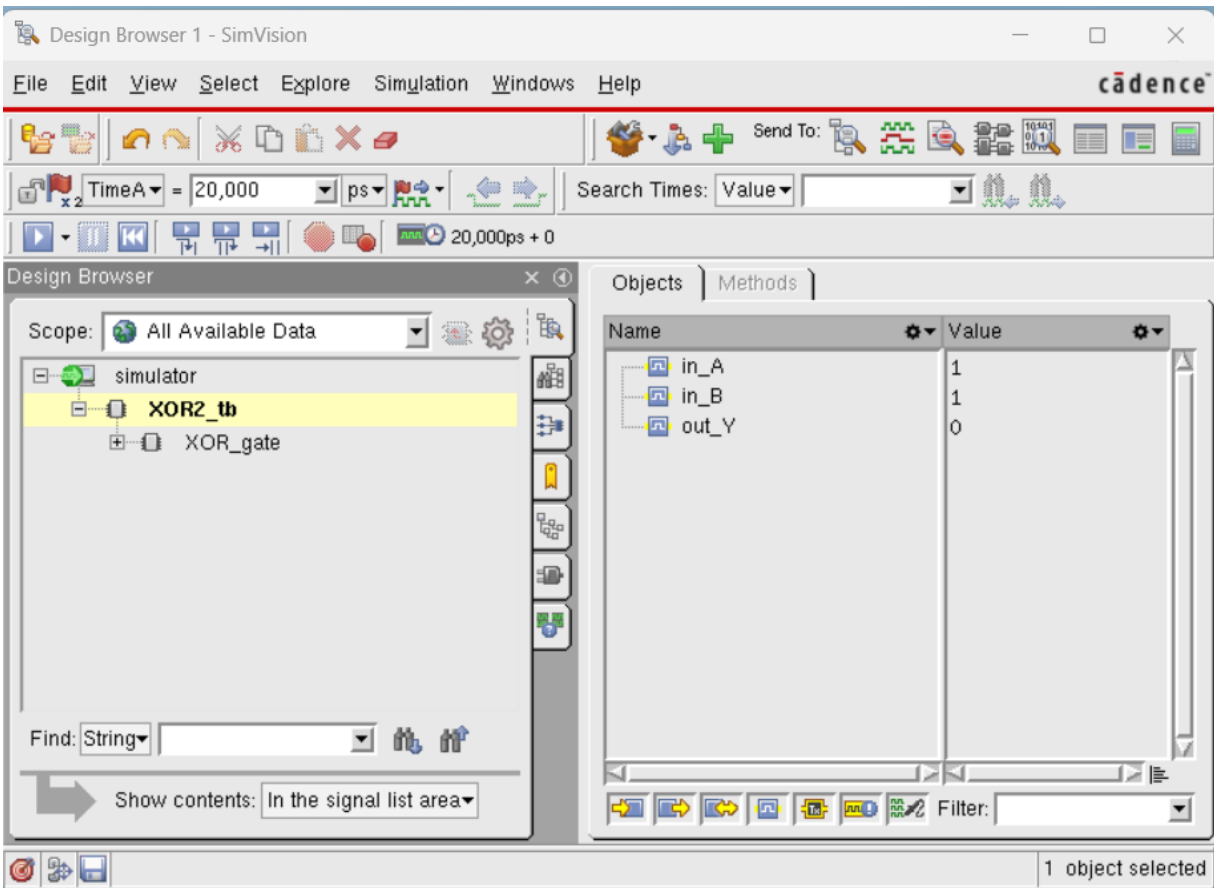


Fig: 3A (Simulation of XOR Gate)

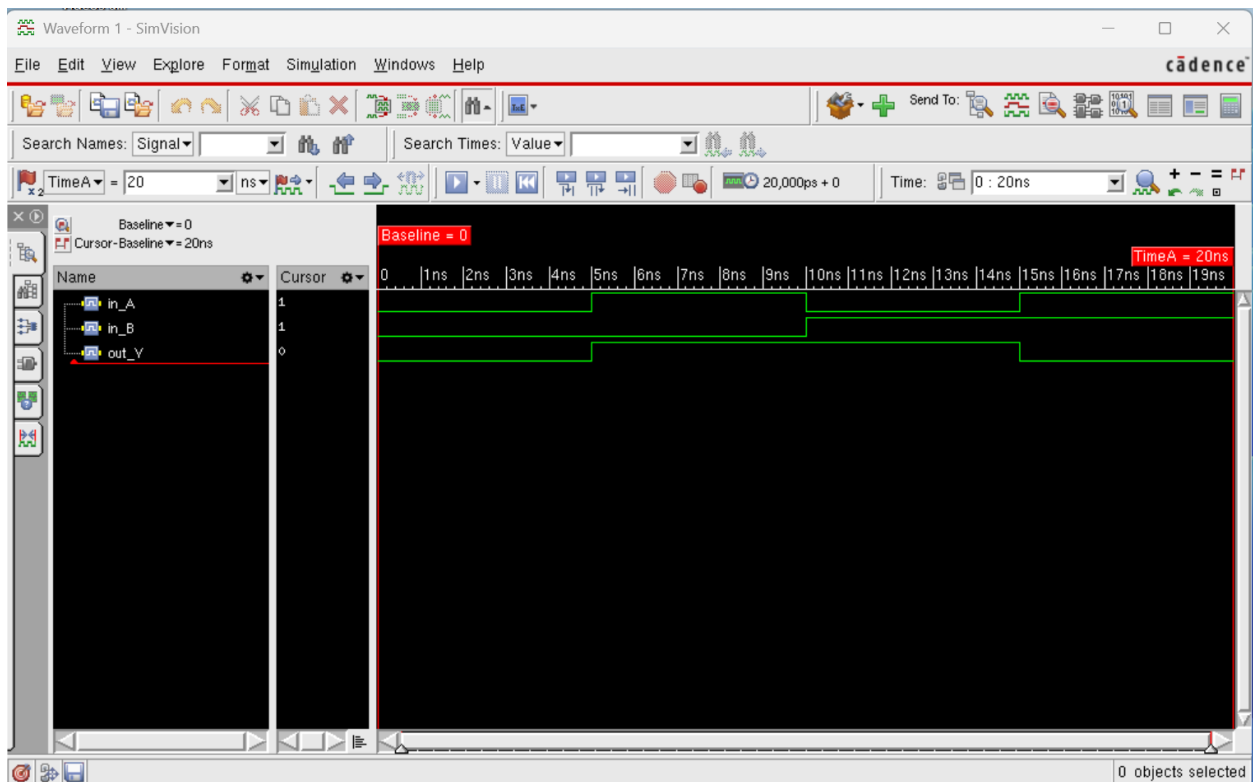


Fig: 3B (Waveform of XOR Gate)

The simulation ran successfully without compilation errors.

Waveform analysis confirms:

- When both inputs are equal (00 or 11), output = 0
- When inputs differ (01 or 10), output = 1

This verifies correct XOR behavior.

2. One-Bit Full adder:

The Full Adder was implemented using:

- $Sum = (A \oplus B) \oplus Cin$
- $Cout = A.B + (A \oplus B).Cin$

The design reuses the XOR2 module and basic AND/OR gates.

```

ss819183@ceashpc-12.rlt.albany.edu
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...
[network/rit/home/ss819183/cad]
Name
..
.cadence
.simvision
.tmp_ss819183
HW2
logs_ss819183
sandbox
TechLibs
Test_DE4_1
Test_DE5_1
Test_DE5_2
Test_DE5_3
Test_DE6_2
Test_DE6_6
waves.shm
Wed_class_prof
xcellium.d
.cdserv
.cdsinit
basic_or.v
basic_or_tb.v
Cadence_bkup.tar.gz
cadence_bkup.tar.gz
cds.lib_disabled
libManager.log
pegasus_ui.log
pegasus_ui_rv.log
Result_Test_DE5_4.grf
TechLibs_bkup.tar.gz
Test_DE4_1_bkup.tar.gz
Test_DE5_1_bkup.tar.gz
Test_DE5_2_bkup.tar.gz
Test_DE5_3_bkup.tar.gz
Test_DE6_2_bkup.tar.gz
Test_DE6_6_bkup.tar.gz
Wed_class_prof_bkup.tar.gz

[ss819183@ceashpc-12 cadence]$ xrun -compile HW2/XOR2.v HW2/FA.v
T00L: xrun(64) 19.09-s001: Started on Feb 15, 2026 at 20:19:37 EST
xrun(64): 19.09-s001: (c) Copyright 1995-2019 Cadence Design Systems, Inc.
file: HW2/FA.v
module worklib.FA:v
errors: 0, warnings: 0
T00L: xrun(64) 19.09-s001: Exiting on Feb 15, 2026 at 20:19:37 EST (total: 00:00:00)
[ss819183@ceashpc-12 cadence]$ xrun -compile HW2/XOR2.v HW2/FA tb.v
T00L: xrun(64) 19.09-s001: Started on Feb 15, 2026 at 20:20:47 EST
xrun(64): 19.09-s001: (c) Copyright 1995-2019 Cadence Design Systems, Inc.
file: HW2/FA_tb.v
module worklib.FA_tb:v
errors: 0, warnings: 0
T00L: xrun(64) 19.09-s001: Exiting on Feb 15, 2026 at 20:20:47 EST (total: 00:00:00)
[ss819183@ceashpc-12 cadence]$ xrun -gui -access rwc HW2/XOR2.v HW2/FA.v HW2/FA_tb.v
T00L: xrun(64) 19.09-s001: Started on Feb 15, 2026 at 20:22:02 EST
xrun(64): 19.09-s001: (c) Copyright 1995-2019 Cadence Design Systems, Inc.
file: HW2/FA_tb.v
module worklib.FA_tb:v
errors: 0, warnings: 0
Caching library 'worklib' ..... Done
Elaborating the design hierarchy:
Top level design units:
FA_tb
Building instance overlay tables: ..... Done
Generating native compiled code:
worklib.FA_tb:v <0x60bbe245>
streams: 6, words: 9146
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
Instances Unique
Modules: 4 3
Primitives: 13 3
Registers: 3 3
Scalar wires: 3 -
Initial blocks: 2 2
Pseudo assignments: 3 3
Simulation timescale: 1ps
Writing initial simulation snapshot: worklib.FA_tb:v
  
```

Fig: 4 (MobaXterm window for running FA)

The above Figure 4 shows the MobaXterm window for running one-bit Full Adder.

```

1  /*
2
3  Problem # "Modeling 1-Bit Full Adder"
4          Sum = (A XOR B) XOR Cin
5          Cout= A.B + (A XOR B).Cin
6  Author  # Saroj Shah
7  Date    # 02-14-2026
8  Reference# Prof. Potluri and others
9
10 */
11 `timescale 1ns/1ps
12
13 module FA(in_A, in_B, in_Cin, out_Sum, out_Cout);
14
15     input in_A, in_B, in_Cin;
16     output out_Sum, out_Cout;
17
18     // Internal wires
19     wire w3;
20     wire w4, w5;
21
22     // XOR - Sum
23     XOR2 xor_a(in_A, in_B, w3);
24     XOR2 xor_b(w3, in_Cin, out_Sum);
25
26     // AND gate
27     and AND_3(w4, in_A, in_B);
28     and AND_4(w5, w3, in_Cin);
29
30     //OR gate => Carry out
31     or OR_2(out_Cout, w4, w5);
32
33 endmodule
34

```

Fig: 5A (Code for 1-Bit Full Adder)

```

1  /*
2  -----
3  Problem # Testbench for 1-Bit Full Adder
4  Author  # Saroj Shah
5  Date   # 02-14-2026
6  Reference# Prof. Potluri and others
7  -----
8  */
9
10 `timescale 1ns/1ps
11
12 module FA_tb;
13
14     reg in_A, in_B, in_Cin;
15     wire out_Sum, out_Cout;
16
17     // Instantiate
18     FA FA_1(in_A, in_B, in_Cin, out_Sum, out_Cout);
19
20     initial
21     begin
22         // All combinations
23         in_A=0; in_B=0; in_Cin=0;
24         #5 in_A=0; in_B=0; in_Cin=1;
25
26         #5 in_A=0; in_B=1; in_Cin=0;
27         #5 in_A=0; in_B=1; in_Cin=1;
28
29         #5 in_A=1; in_B=0; in_Cin=0;
30         #5 in_A=1; in_B=0; in_Cin=1;
31
32         #5 in_A=1; in_B=1; in_Cin=0;
33         #5 in_A=1; in_B=1; in_Cin=1;
34
35         #5 $finish;
36     end
37
38     initial
39     $monitor("\nTime=%0t | A=%b B=%b Cin=%b | Sum=%b Cout=%b",
40             $time, in_A, in_B, in_Cin, out_Sum, out_Cout);
41
42 endmodule
43

```

Fig: 5B (Testbench for 1-Bit Full Adder)

Figure 5A and 5B shows the code for one-bit Full Adder and one-bit Full Adder's testbench. The testbench code is used to running the simulation.

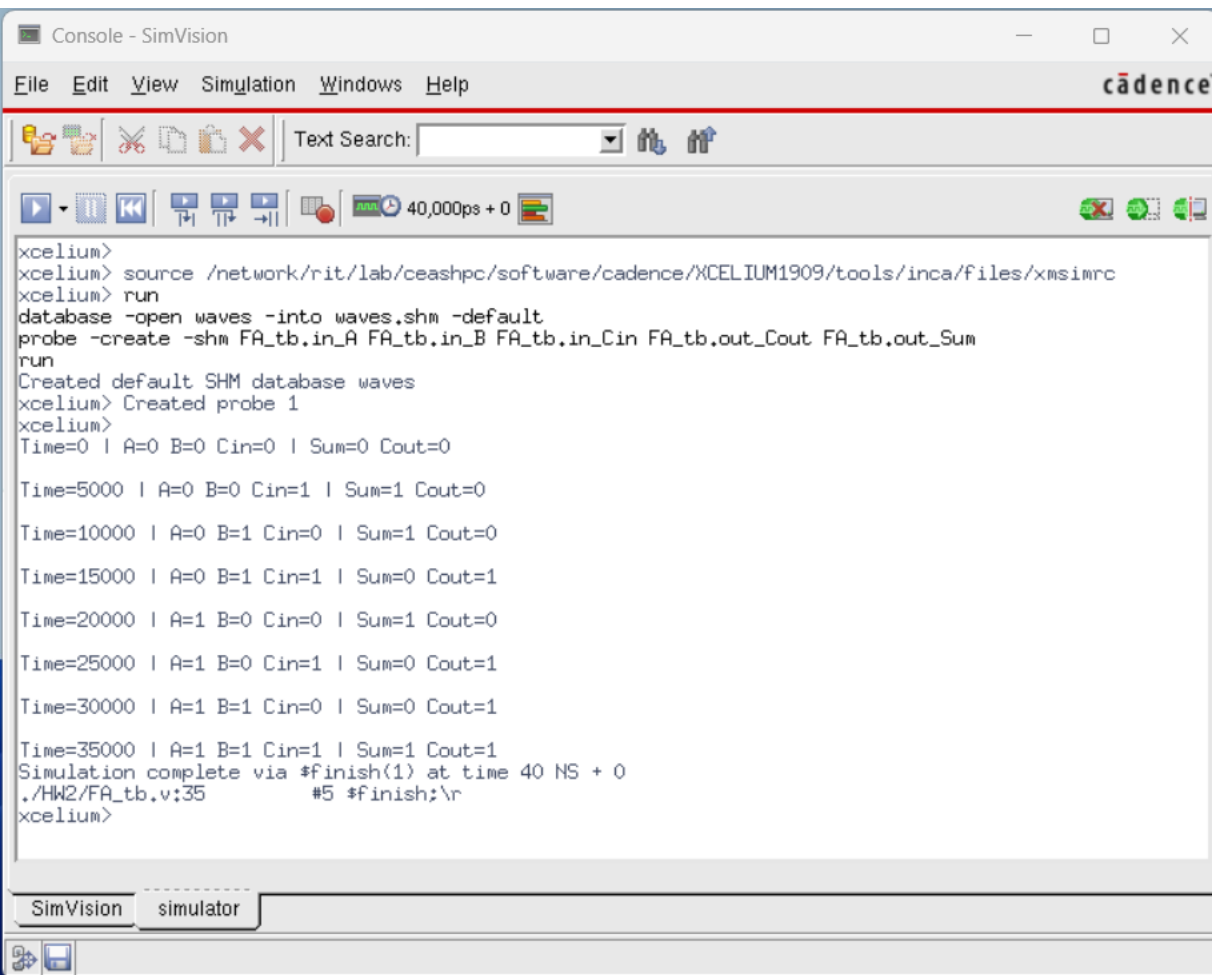
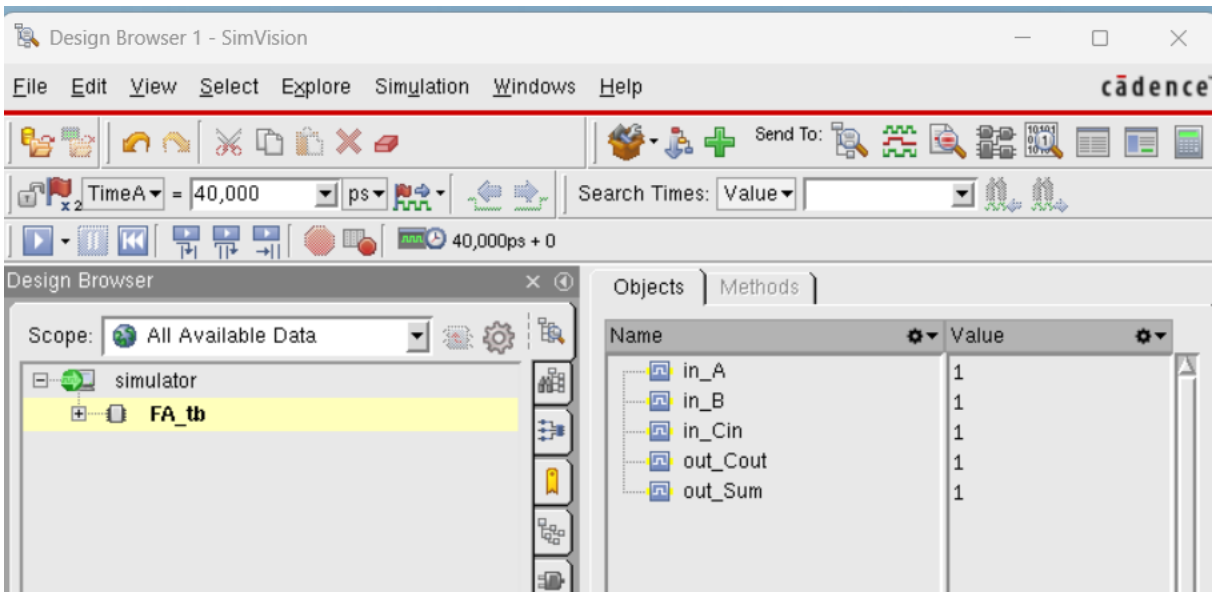


Fig: 6A (Simulation of 1-Bit Full Adder)

```

Time=0 | A=0 B=0 Cin=0 | Sum=0 Cout=0
Time=5000 | A=0 B=0 Cin=1 | Sum=1 Cout=0
Time=10000 | A=0 B=1 Cin=0 | Sum=1 Cout=0
Time=15000 | A=0 B=1 Cin=1 | Sum=0 Cout=1
Time=20000 | A=1 B=0 Cin=0 | Sum=1 Cout=0
Time=25000 | A=1 B=0 Cin=1 | Sum=0 Cout=1
Time=30000 | A=1 B=1 Cin=0 | Sum=0 Cout=1
Time=35000 | A=1 B=1 Cin=1 | Sum=1 Cout=1

```

Fig: 6B (Showing correct calculation)

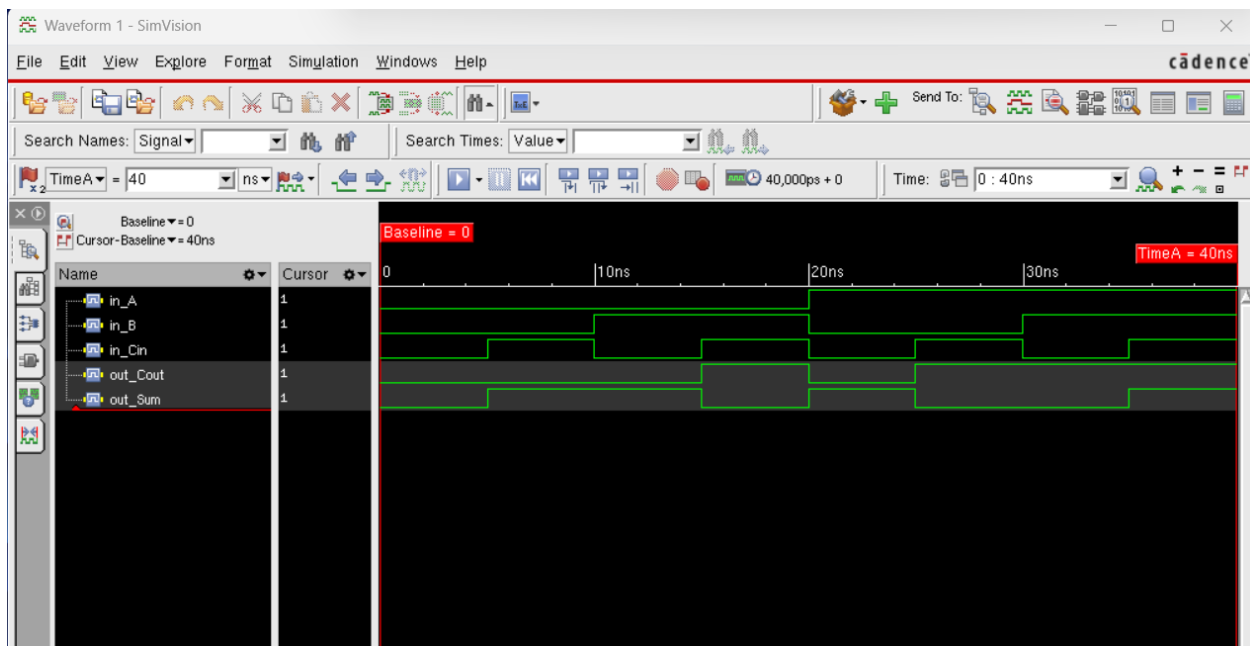


Fig: 6C (Waveform of 1-Bit Full Adder)

The simulation figures shown in figure 6A and 6B verifies correct Full Adder operation. The Sum output follows the XOR relationship of inputs, while the Carry output is asserted whenever at least two inputs are high. Same way the figure 6C, the waveforms clearly show correct propagation of carry and sum bits for all input combinations.

3. Four-Bit Full Subtractor (Using Full Adder):

Subtraction was implemented using 2's complement logic:

$$A - B = A + (B' + 1)$$

Implementation steps:

- Each bit of B is XORed with Bin (control signal).
- Bin is also connected as the initial carry-in.
- Four Full Adders are connected in ripple-carry fashion.
- Final borrow is obtained from the inverted final carry

```

[ss819183@ceashpc-12.nit.albany.edu]
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
/network/nit/home/ss819183/cad...
Name
..
.cadence
.simvision
.tmp_ss819183
HW2
logs_ss819183
sandbox
TechLibs
Test_DE4_1
Test_DE5_1
Test_DE5_2
Test_DE5_3
Test_DE5_2
Test_DE6_6
waves.shm
Wed_class_prof
xcclium.d
.cdseiv
.cdseiv
basic_or.v
basic_or_tb.v
Cadence_bkup.tar.gz
cde.lib.disabled
libManager.log
pegasus_ui.log
pegasus_ui.log
Result_Test_DE5_4.grf
TechLibs_bkup.tar.gz

[ss819183@ceashpc-12 cadence]$ xrun -gui -access rwc HW2/XOR2.v HW2/FA.v HW2/Sub_4bit.v HW2/Sub_4bit_tb.v
TOOL: xrun(64) 19.09-s001: Started on Feb 15, 2026 at 22:19:11 EST
xrun(64): 19.09-s001: (c) Copyright 1995-2019 Cadence Design Systems, Inc.
Recompiling... reason: file './HW2/Sub_4bit_tb.v' is newer than expected.
expected: Sun Feb 15 21:58:42 2026
actual: Sun Feb 15 22:19:00 2026
file: HW2/Sub_4bit_tb.v
module worklib.Sub_4bit_tb.v
errors: 0, warnings: 0
Caching library 'worklib' ..... Done
Elaborating the design hierarchy:
Top level design units:
Sub_4bit_tb
Building instance overlay tables: ..... Done
Generating native compiled code:
worklib.Sub_4bit_tb.v: <0x50258ffc>
streams: 6, words: 8346
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
Instances Unique
Modules: 18 4
Primitives: 73 3
Registers: 3 3
Scalar wires: 1 -
Expanded wires: 8 2
Initial blocks: 2 2
Pseudo assignments: 3 3
Simulation timescale: 1ps
Writing initial simulation snapshot: worklib.Sub_4bit_tb.v
waiting for SimVision/Indago to connect...

```

Fig: 7 (MobaXterm window)

The above Figure 4 shows the MobaXterm window for running Four-bit Subtractor.

```

1  /*
2  3  -----
3  4  Problem # "Modeling 4-Bit subtractor using FA"
4  5  Sum= (A XOR B) XOR Bin
5  6  Bout= A'.B + (A XOR B)'.Bin
6  7  Author # Saroj Shah
7  8  Date # 02-15-2026
8  9  Reference# Prof. Potluri and others
9  10 -----
10 11 */
11 12 `timescale 1ns/1ps
12 13 module Sub_4bit(in_A, in_B, in_Bin, out_D, out_Bout);
13 14     input [3:0] in_A;
14 15     input [3:0] in_B;
15 16     input      in_Bin;
16 17
17 18     output [3:0] out_D;
18 19     output      out_Bout;
19 20
20 21     // Internal wires
21 22     wire [3:0] B_xor;
22 23     wire c1, c2, c3, c4;
23 24
24 25     // XOR stage
25 26     XOR2 x0(in_B[0], in_Bin, B_xor[0]);
26 27     XOR2 x1(in_B[1], in_Bin, B_xor[1]);
27 28     XOR2 x2(in_B[2], in_Bin, B_xor[2]);
28 29     XOR2 x3(in_B[3], in_Bin, B_xor[3]);
29 30
30 31     // Ripple-carry Full Adders
31 32     FA FA0(in_A[0], B_xor[0], in_Bin, out_D[0], c1);
32 33     FA FA1(in_A[1], B_xor[1], c1, out_D[1], c2);
33 34     FA FA2(in_A[2], B_xor[2], c2, out_D[2], c3);
34 35     FA FA3(in_A[3], B_xor[3], c3, out_D[3], c4);
35 36
36 37     // Borrow output
37 38     not n1(out_Bout, c4);
38 39
39 40 endmodule

```

Fig: 8A (Code for 4-Bit Subtractor)

```

1  /*
2
3  -----
4  Problem   # "Testbench for 4-Bit subtractor"
5  Author    # Saroj Shah
6  Date      # 02-15-2026
7  Reference # Prof. Potluri and others
8  -----
9  */
10
11 `timescale 1ns/1ps
12
13 module Sub_4bit_tb;
14
15     reg [3:0] in_A;
16     reg [3:0] in_B;
17     reg      in_Bin;
18
19     wire [3:0] out_D;
20     wire      out_Bout;
21
22     // Instantiating
23     Sub_4bit sub1(in_A, in_B, in_Bin, out_D, out_Bout);
24
25     initial begin
26
27         /*
28         // When in_Bin = 0, it will do ADDITION
29         in_Bin = 0;
30
31         #10 in_A = 4'b0101; in_B = 4'b0011; // 5 + 3 = 8
32         #10 in_A = 4'b1001; in_B = 4'b0110; // 9 + 6 = 15
33         #10 in_A = 4'b0111; in_B = 4'b1000; // 7 + 8 = 15
34         */
35
36         // When in_Bin = 1, it will do SUBTRACTION
37         in_Bin = 1;
38
39         #10 in_A = 4'b1001; in_B = 4'b0011; // 9 - 3 = 6
40         #10 in_A = 4'b0101; in_B = 4'b0111; // 5 - 7 = -2 (Borrow=1)
41         #10 in_A = 4'b1000; in_B = 4'b1000; // 8 - 8 = 0
42         #10 in_A = 4'b0000; in_B = 4'b0001; // 0 - 1 = -1 (Borrow=1)
43         #10 $finish;
44     end
45
46     initial begin
47         $monitor("\nTime=%0t | Mode=%b | A=%0d(%b) B=%0d(%b) | Result=%0d(%b) Borrow=%b",
48             $time, in_Bin, in_A, in_A, in_B, in_B, out_D, out_D, out_Bout);
49     end
50 endmodule

```

Fig: 8B (Testbench code for 4-Bit Subtractor)

Figure 8A and 8B shows the code for 4-bit subtractor and 4-bit subtractor's testbench.

The testbench code is used to running the simulation. The figures are shown below.

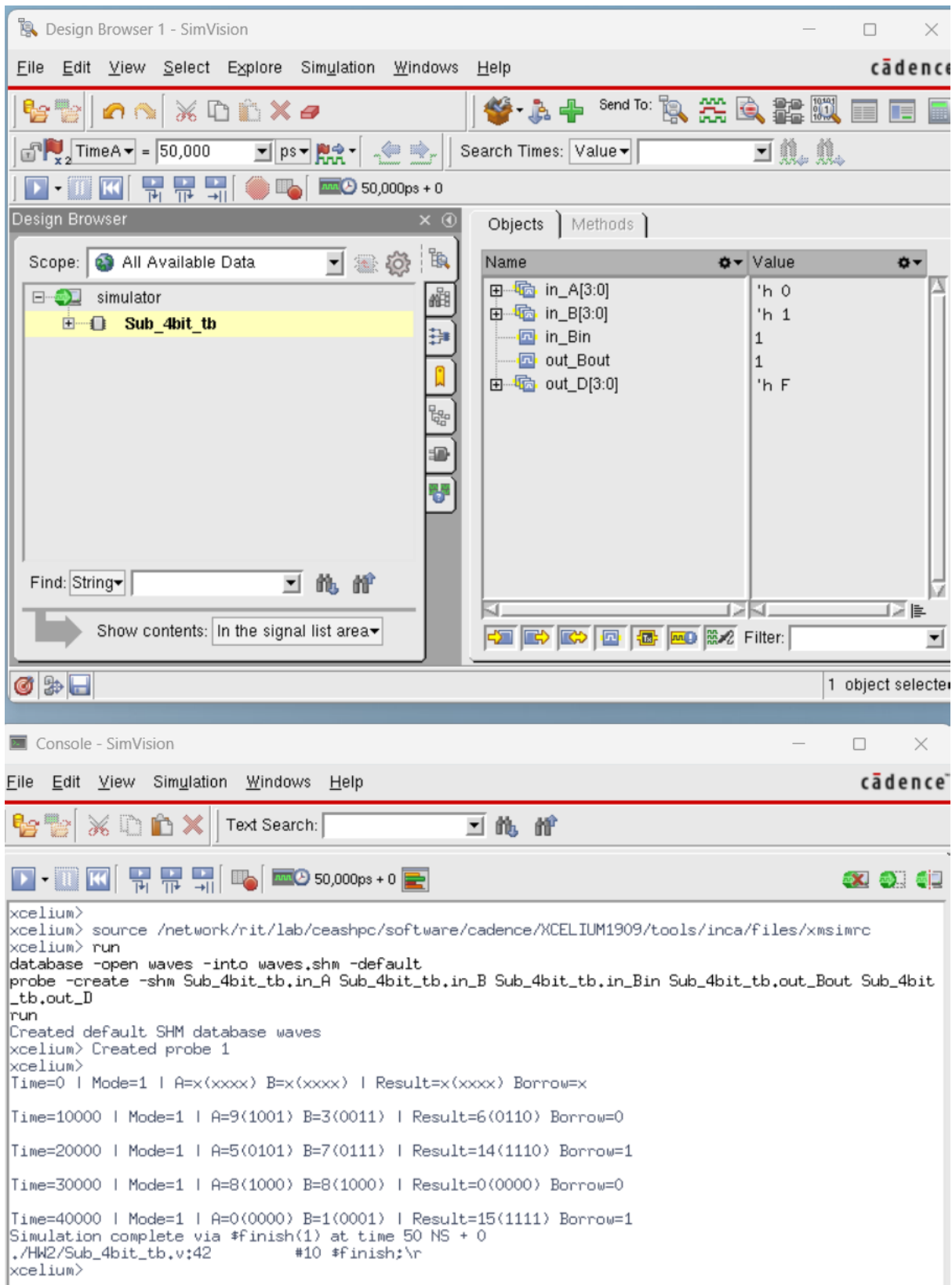


Fig: 9A (Simulation of 4-Bit Subtractor)

```

Time=0 | Mode=1 | A=x(xxxx) B=x(xxxx) | Result=x(xxxx) Borrow=x
Time=10000 | Mode=1 | A=9(1001) B=3(0011) | Result=6(0110) Borrow=0
Time=20000 | Mode=1 | A=5(0101) B=7(0111) | Result=14(1110) Borrow=1
Time=30000 | Mode=1 | A=8(1000) B=8(1000) | Result=0(0000) Borrow=0
Time=40000 | Mode=1 | A=0(0000) B=1(0001) | Result=15(1111) Borrow=1

```

Fig: 9B (Result of 4-Bit Subtractor)

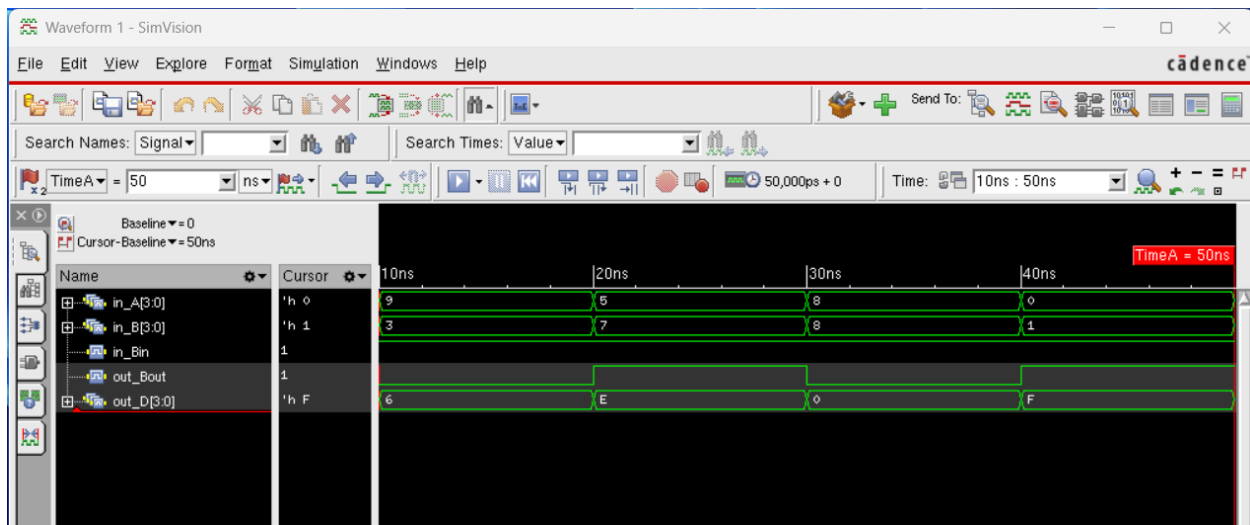


Fig: 9C (Waveform of 4-Bit Subtractor)

Test cases verified:

- $9 - 3 = 6$
- $5 - 7 = -2$ (Borrow = 1)
- $8 - 8 = 0$
- $0 - 1 = -1$ (Borrow = 1)

The simulation figures and waveform shown in figure 9A, 9B and 9C verifies correct operation and result of the Subtractor. The waveforms show correct difference bits and proper borrow generation. The subtractor correctly performs subtraction when Bin = 1.

Conclusion:

In this assignment, several fundamental combinational logic circuits were successfully designed and simulated using structural Verilog modeling in Cadence Xcelium. The simulation waveforms verified the correct functional behavior for all modules.

Works Cited

Potluri, Seetal. Class Notes, PDF and videos, Spring 2026.