

521 Digital ASIC Design

Title: HW- 2

For

By: Saroj Shah

Date: Feb 18, 2026

HW-2, Professor Seetal Potluri

Introduction and Summary:

In this HW- 2 assignment, we are designing, and simulating fundamental combinational logic circuits using Verilog HDL and Cadence Xcelium. The following digital building blocks were implemented:

- 2-Input XOR Gate
- 1-Bit Full Adder
- 4-Bit Subtractor (using Full Adders)

All designs were written in Verilog at gate-level and structural modeling style.

Testbenches were developed for each module to verify correctness through simulation and waveform analysis in SimVision..

Materials:

- Computer system
- Cadence Xcelium (xrun)
- SimVision waveform viewer
- MobaXterm (remote terminal access)

Data:

Please refer to the screenshot provided below:

1. Two in-put XOR Gate:

The XOR gate was implemented using the Boolean equation:

$$Y = A'B + AB'$$

The design uses: 2 NOT gates; 2 AND gates; 1 OR gate

The screenshot shows a MobaXterm window with a terminal session running on a remote host. The terminal window title is "ss819183@ceashpc-12.rit.albany.edu". The terminal output shows the user navigating to the "/network/rit/home/ss819183/cadence" directory and executing commands related to Cadence design tools like "xrun" and "xcelium". The terminal also displays statistics for memory usage, network traffic, and disk space.

```

[ss819183@ceashpc-12 ~]$ cd cadence
[ss819183@ceashpc-12 cadence]$ module load cadence/IC618-v2
[ss819183@ceashpc-12 cadence]$ xrun -compile HW2/XOR2.v
TOOL: xrun(64) 19.09-s001: Started on Feb 15, 2026 at 19:53:19 EST
xrun(64): 19.09-s001: (c) Copyright 1995-2019 Cadence Design Systems, Inc.
file: HW2/XOR2.v
    module worklib.XOR2:v
        errors: 0, warnings: 0
TOOL: xrun(64) 19.09-s001: Exiting on Feb 15, 2026 at 19:53:19 EST (total: 00:00:00)
[ss819183@ceashpc-12 cadence]$ xrun -compile HW2/XOR2_tb.v
TOOL: xrun(64) 19.09-s001: Started on Feb 15, 2026 at 19:53:34 EST
xrun(64): 19.09-s001: (c) Copyright 1995-2019 Cadence Design Systems, Inc.
file: HW2/XOR2_tb.v
    module worklib.XOR2_tb:v
        errors: 0, warnings: 0
TOOL: xrun(64) 19.09-s001: Exiting on Feb 15, 2026 at 19:53:34 EST (total: 00:00:00)
[ss819183@ceashpc-12 cadence]$ xrun -gut -access rwc HW2/XOR2.v HW2/XOR2_tb.v
TOOL: xrun(64) 19.09-s001: Started on Feb 15, 2026 at 19:53:48 EST
xrun(64): 19.09-s001: (c) Copyright 1995-2019 Cadence Design Systems, Inc.
    Caching library 'worklib' ..... Done
    Elaborating the design hierarchy:
    Top level design units:
        XOR2_tb
    Building instance overlay tables: ..... Done
    Generating native compiled code:
        worklib.XOR2_tb:v <0x7becb0e2>
            streams: 5, words: 5614
    Building instance specific data structures.
    Loading native compiled code: ..... Done
    Design hierarchy summary:
        Instances Unique
        Modules: 2 2
        Primitives: 5 3
        Registers: 2 2
        Scalar wires: 2 -
        Initial blocks: 2 2
        Pseudo assignments: 2 2
        Simulation timescale: 1ps
    Writing initial simulation snapshot: worklib.XOR2_tb:v
    waiting for SimVision/Indago to connect...

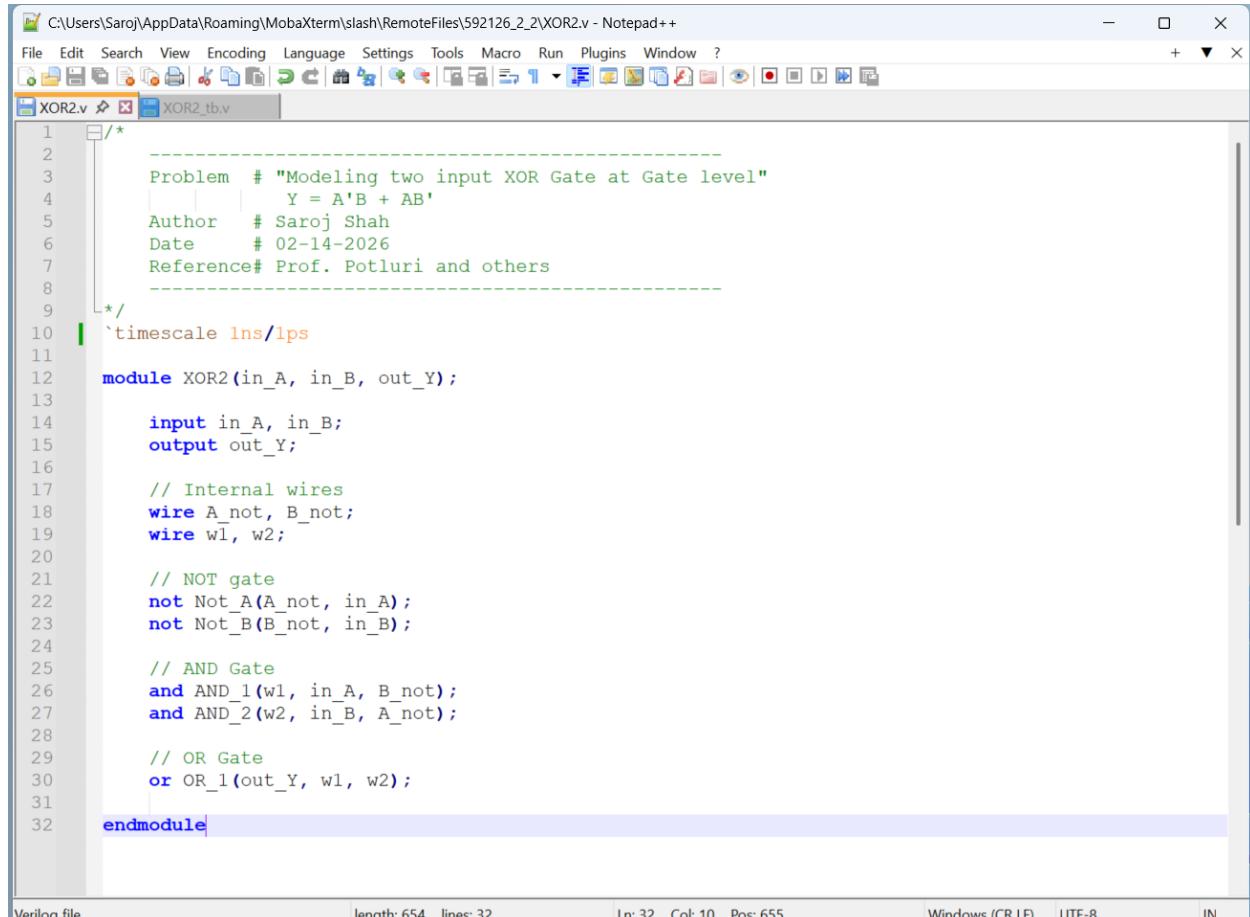
-----
Relinquished control to SimVision...
xcelium>
xcelium> source /network/rit/lab/ceashpc/software/cadence/XCELIUM1909/tools/inca/files/xmsimrc
xcelium> error starting plugin /network/rit/lab/ceashpc/software/cadence/XCELIUM1909/tools/simvision/plugins/64bit/invoke_ida.so
child process exited abnormally

```

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Fig: 1 (MobaXterm window)

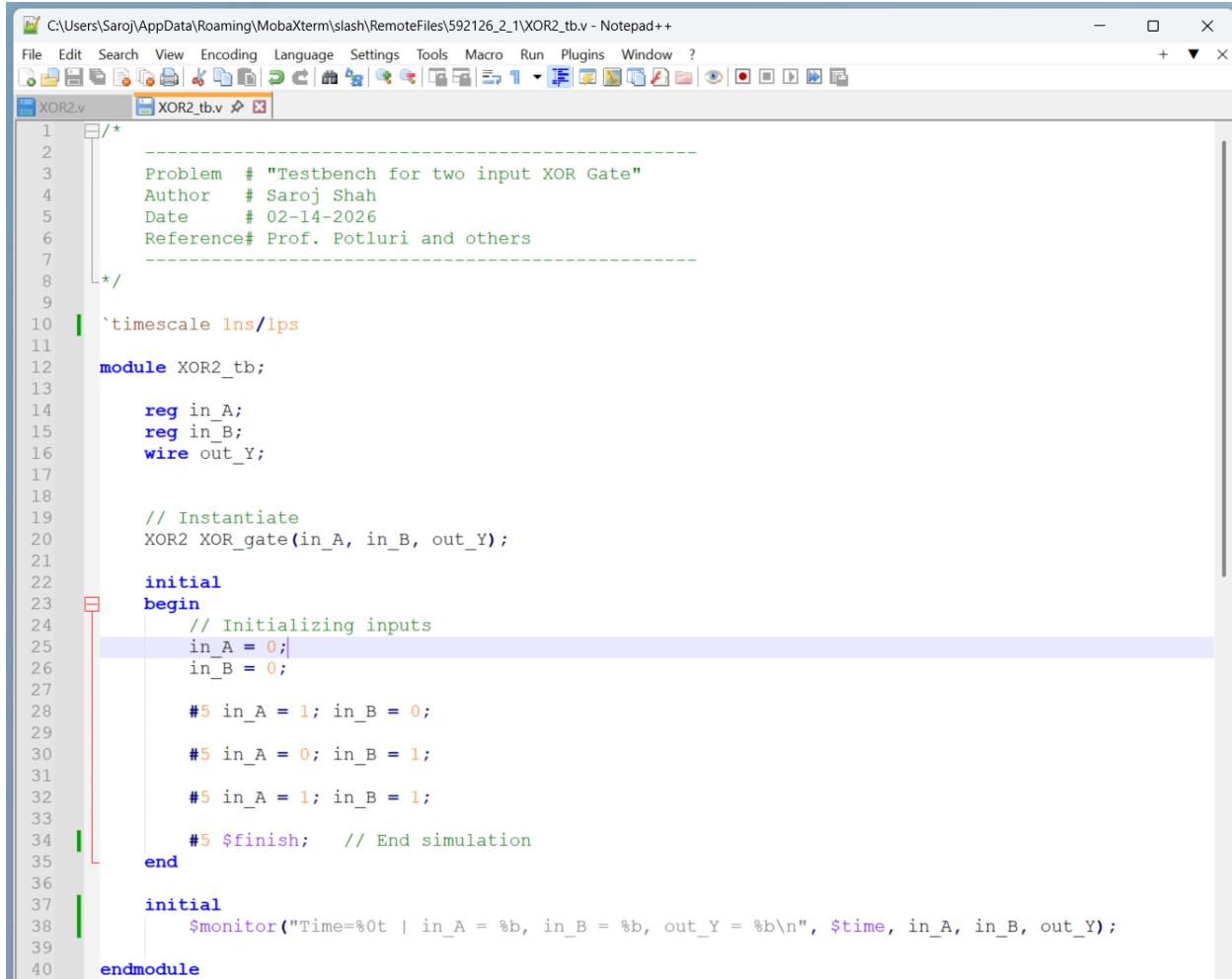
The above figure shows the code compiling and Cadence Xcelium running without any error.



The screenshot shows a Notepad++ window displaying Verilog code for a XOR2 gate. The code is contained in a file named XOR2.v. The code defines a module XOR2 with two inputs (in_A, in_B) and one output (out_Y). It uses internal wires (A_not, B_not, w1, w2) and NOT, AND, and OR gates to implement the logic $Y = A'B + AB'$. The code includes comments and a header section with problem, author, date, and reference information.

```
1  /*-----*
2   Problem # "Modeling two input XOR Gate at Gate level"
3   | Y = A'B + AB'
4   Author # Saroj Shah
5   Date # 02-14-2026
6   Reference# Prof. Potluri and others
7   -----*/
8
9 */
10 `timescale 1ns/1ps
11
12 module XOR2(in_A, in_B, out_Y);
13
14     input in_A, in_B;
15     output out_Y;
16
17     // Internal wires
18     wire A_not, B_not;
19     wire w1, w2;
20
21     // NOT gate
22     not Not_A(A_not, in_A);
23     not Not_B(B_not, in_B);
24
25     // AND Gate
26     and AND_1(w1, in_A, B_not);
27     and AND_2(w2, in_B, A_not);
28
29     // OR Gate
30     or OR_1(out_Y, w1, w2);
31
32 endmodule
```

Fig: 2A (Code for XOR2 Gate)



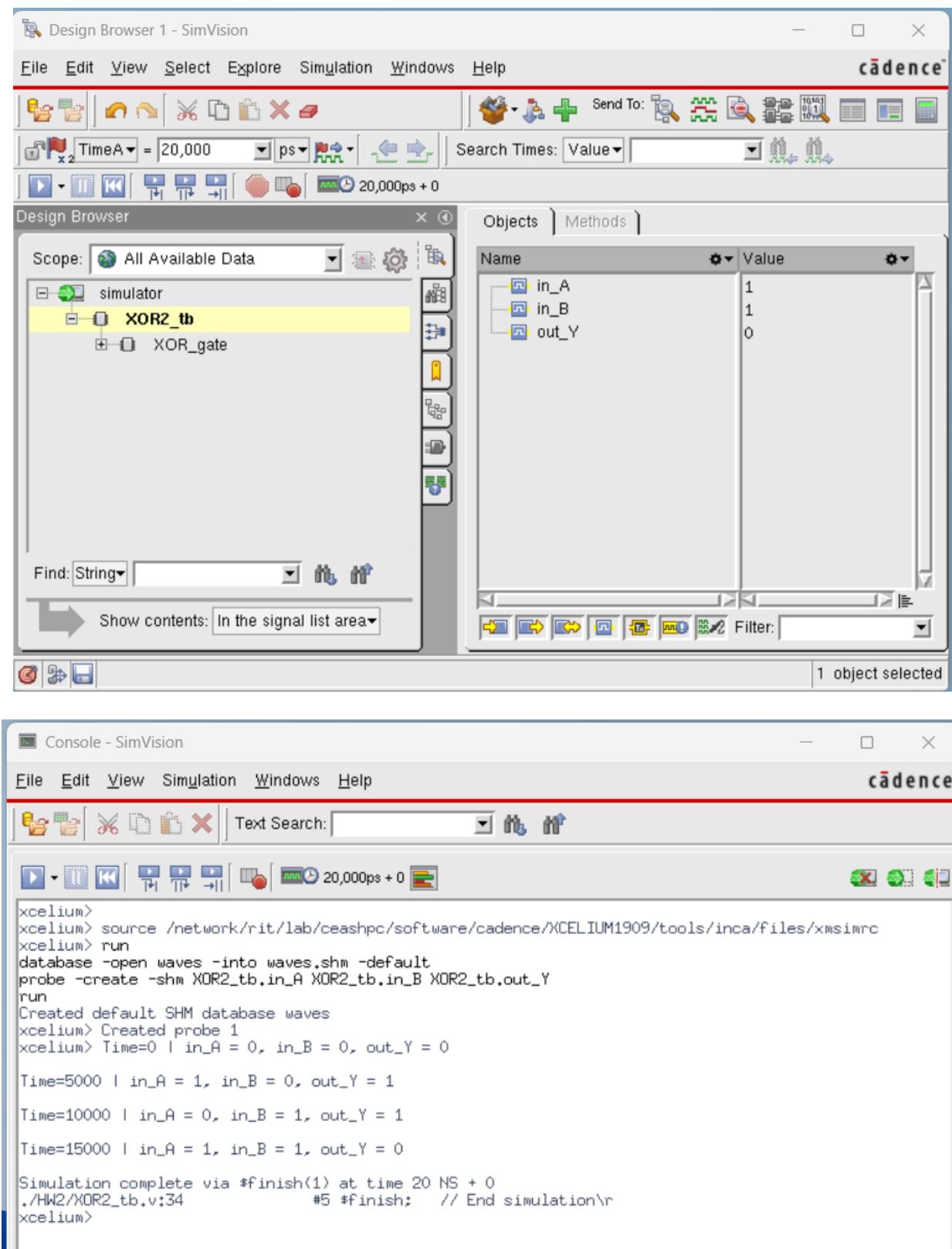
```

1  /* 
2   -----
3   Problem # "Testbench for two input XOR Gate"
4   Author  # Saroj Shah
5   Date    # 02-14-2026
6   Reference# Prof. Potluri and others
7   -----
8 */
9
10 `timescale 1ns/1ps
11
12 module XOR2_tb;
13
14     reg in_A;
15     reg in_B;
16     wire out_Y;
17
18
19 // Instantiate
20 XOR2 XOR_gate(in_A, in_B, out_Y);
21
22 initial
23 begin
24     // Initializing inputs
25     in_A = 0;
26     in_B = 0;
27
28     #5 in_A = 1; in_B = 0;
29
30     #5 in_A = 0; in_B = 1;
31
32     #5 in_A = 1; in_B = 1;
33
34     #5 $finish; // End simulation
35 end
36
37 initial
38     $monitor("Time=%0t | in_A = %b, in_B = %b, out_Y = %b\n", $time, in_A, in_B, out_Y);
39
40 endmodule

```

Fig: 2B (Code for XOR2 Testbench Gate)

Figure 2A and 2B shows the code for XOR gate and XOR gate testbench. The testbench code is used to run the simulation.

**Fig: 3A (Simulation of XOR Gate)**

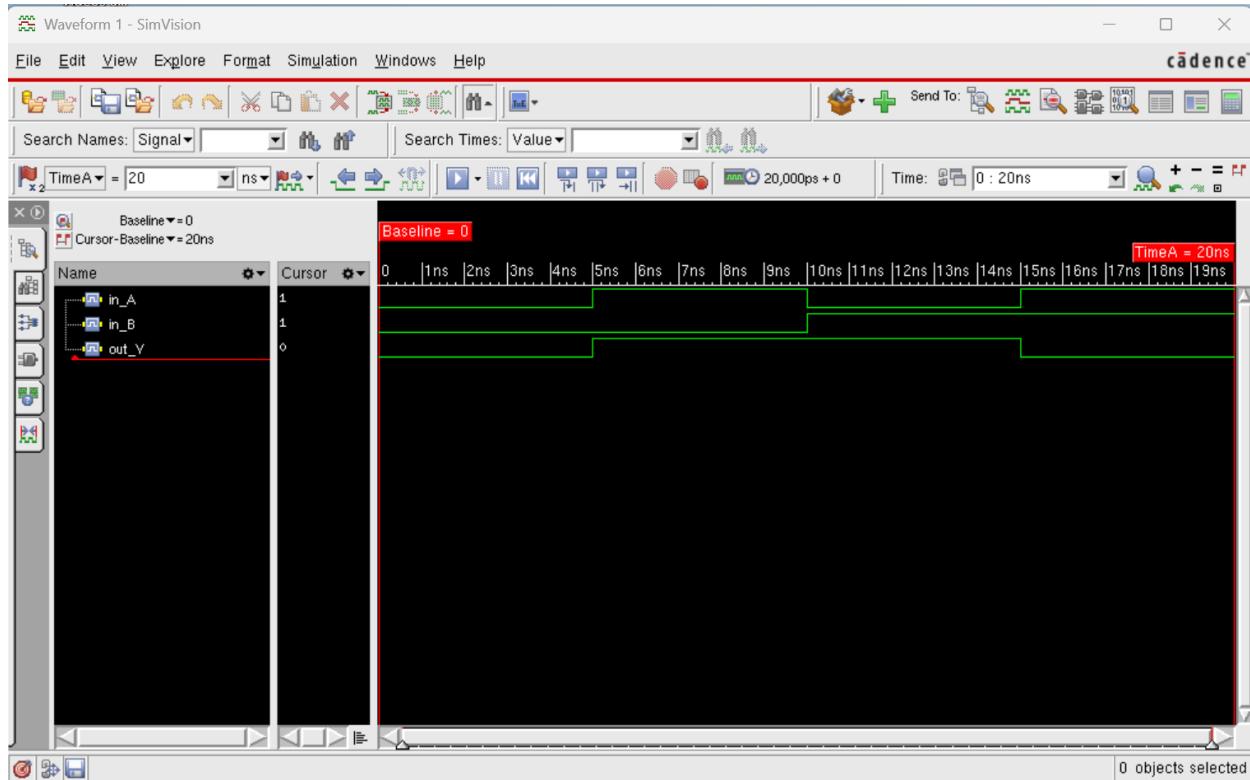


Fig: 3B (Waveform of XOR Gate)

The simulation ran successfully without compilation errors.

Waveform analysis confirms:

- When both inputs are equal (00 or 11), output = 0
- When inputs differ (01 or 10), output = 1

This verifies correct XOR behavior.

2. One-Bit Full adder:

The Full Adder was implemented using:

- $Sum = (A \oplus B) \oplus Cin$
- $Cout = A.B + (A \oplus B).Cin$

The design reuses the XOR2 module and basic AND/OR gates.

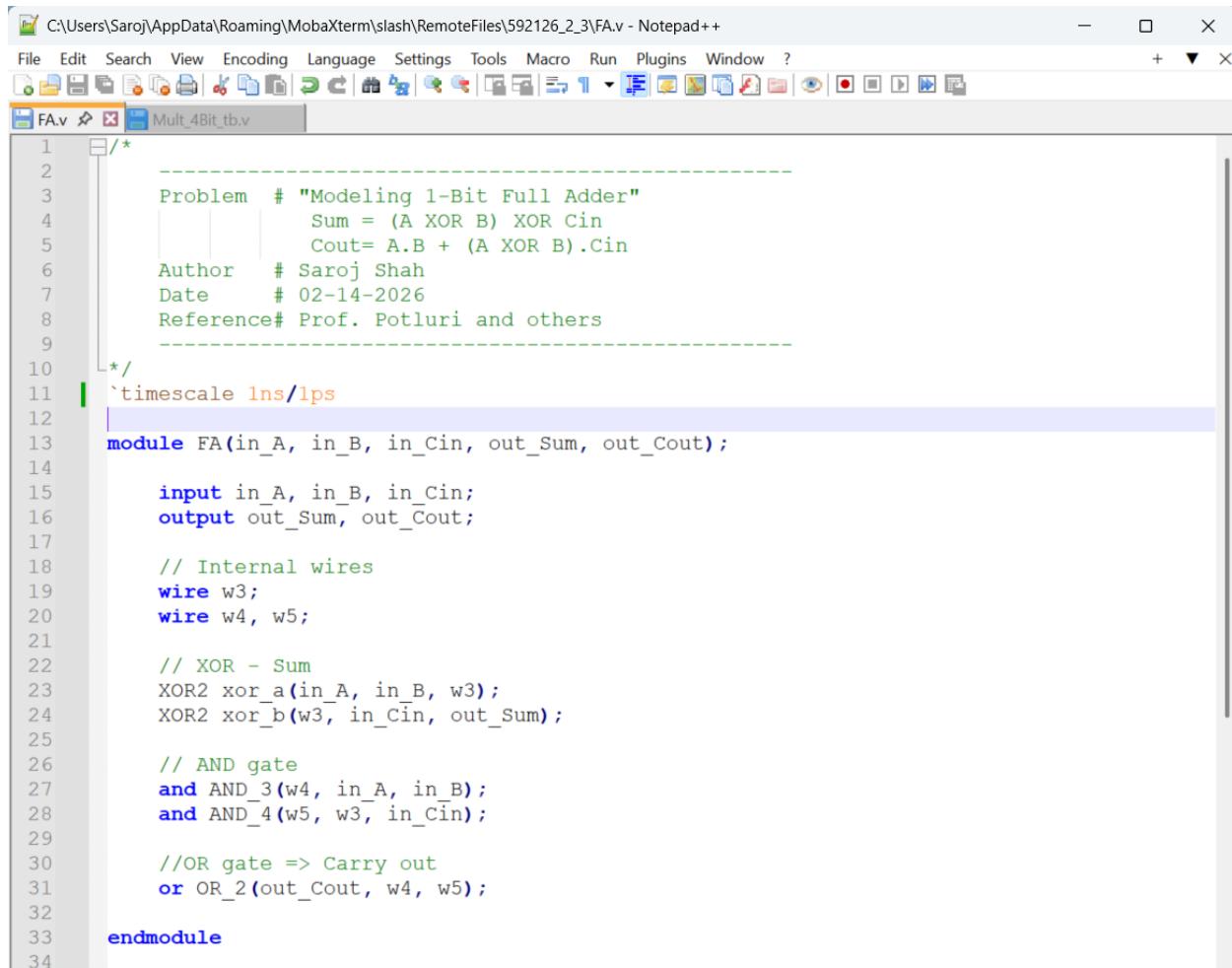
```

ss819183@ceashpc-12.rit.albany.edu ~
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
X server Exit
Quick connect...
[ss819183@ceashpc-12.rit.albany.edu ~] $ xrun -compile HW2/XOR2.v HW2/FA.v
TOOL: xrun(64) 19.09-s001: Started on Feb 15, 2026 at 20:19:37 EST
xrun(64): 19.09-s001: (c) Copyright 1995-2019 Cadence Design Systems, Inc.
file: HW2/FA.v
    module worklib.FA;
        errors: 0, warnings: 0
TOOL: xrun(64) 19.09-s001: Exiting on Feb 15, 2026 at 20:19:37 EST (total: 00:00:00)
[ss819183@ceashpc-12 cadence]$ xrun -compile HW2/XOR2.v HW2/FA_tb.v
TOOL: xrun(64) 19.09-s001: Started on Feb 15, 2026 at 20:20:47 EST
xrun(64): 19.09-s001: (c) Copyright 1995-2019 Cadence Design Systems, Inc.
file: HW2/FA_tb.v
    module worklib.FA_tb;
        errors: 0, warnings: 0
TOOL: xrun(64) 19.09-s001: Exiting on Feb 15, 2026 at 20:20:47 EST (total: 00:00:00)
[ss819183@ceashpc-12 cadence]$ xrun -gui -access rvc HW2/XOR2.v HW2/FA.v HW2/FA_tb.v
TOOL: xrun(64) 19.09-s001: Started on Feb 15, 2026 at 20:22:02 EST
xrun(64): 19.09-s001: (c) Copyright 1995-2019 Cadence Design Systems, Inc.
file: HW2/FA_tb.v
    module worklib.FA_tb;
        errors: 0, warnings: 0
        Caching library 'worklib' ..... Done
Elaborating the design hierarchy:
Top level design units:
    FA_tb
Building instance overlay tables: ..... Done
Generating native compiled code:
    worklib.FA_tb:v <0x60bbe245>
        streams: 6, words: 9146
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
    Instances Unique
    Modules: 4 3
    Primitives: 13 3
    Registers: 3 3
    Scalar wires: 3 -
    Initial blocks: 2 2
    Pseudo assignments: 3 3
    Simulation timescale: 1ps
Writing initial simulation snapshot: worklib.FA_tb:v

```

Fig: 4 (MobaXterm window for running FA)

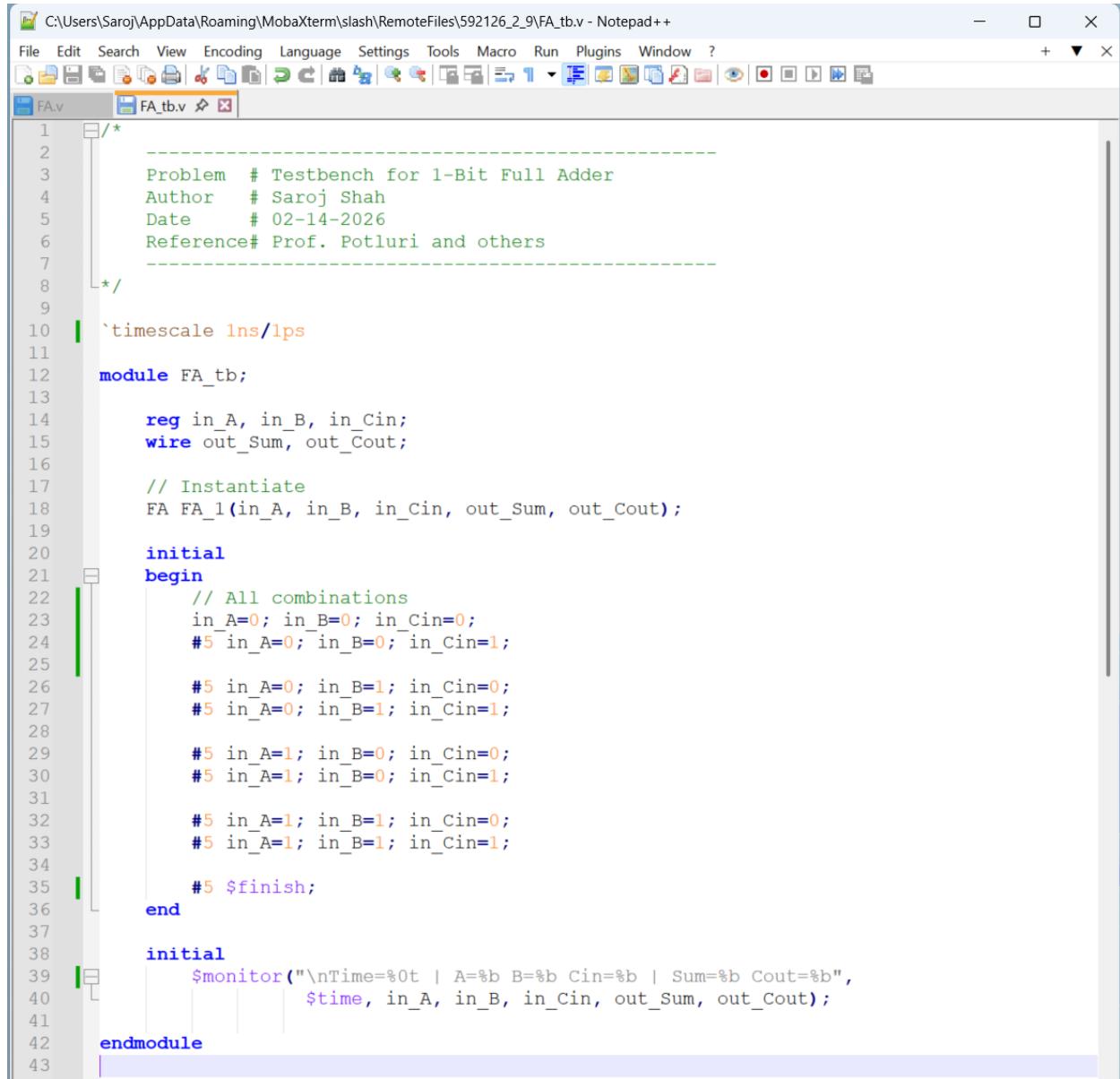
The above Figure 4 shows the MobaXterm window for running one-bit Full Adder.



The screenshot shows a Notepad++ window with the file 'FA.v' open. The code is a Verilog module for a 1-bit Full Adder. It includes comments explaining the logic: 'Problem # "Modeling 1-Bit Full Adder"', 'Sum = (A XOR B) XOR Cin', 'Cout= A.B + (A XOR B).Cin', and author information. The code defines inputs (in_A, in_B, in_Cin), outputs (out_Sum, out_Cout), and internal wires (w3, w4, w5). It uses XOR and AND gates to calculate the sum and carry out.

```
1  /* Problem  # "Modeling 1-Bit Full Adder"
2   | Sum = (A XOR B) XOR Cin
3   | Cout= A.B + (A XOR B).Cin
4   | Author  # Saroj Shah
5   | Date    # 02-14-2026
6   | Reference# Prof. Potluri and others
7   -----
8 */
9
10 `timescale 1ns/1ps
11
12 module FA(in_A, in_B, in_Cin, out_Sum, out_Cout);
13
14     input in_A, in_B, in_Cin;
15     output out_Sum, out_Cout;
16
17     // Internal wires
18     wire w3;
19     wire w4, w5;
20
21     // XOR - Sum
22     XOR2 xor_a(in_A, in_B, w3);
23     XOR2 xor_b(w3, in_Cin, out_Sum);
24
25     // AND gate
26     and AND_3(w4, in_A, in_B);
27     and AND_4(w5, w3, in_Cin);
28
29     //OR gate => Carry out
30     or OR_2(out_Cout, w4, w5);
31
32 endmodule
33
34
```

Fig: 5A (Code for 1-Bit Full Adder)



The screenshot shows a Notepad++ window with the file FA_tb.v open. The code is a Verilog testbench for a 1-bit Full Adder. It includes comments at the top providing authorship and date information. The code defines a module FA_tb with an initial block that generates all possible input combinations (00, 01, 10, 11) for A, B, and Cin, and monitors the output Sum and Cout. The code uses \$monitor to print the time and the state of each signal.

```

1  /*
2   -----
3   Problem # Testbench for 1-Bit Full Adder
4   Author # Saroj Shah
5   Date   # 02-14-2026
6   Reference# Prof. Potluri and others
7   -----
8 */
9
10 `timescale 1ns/1ps
11
12 module FA_tb;
13
14     reg in_A, in_B, in_Cin;
15     wire out_Sum, out_Cout;
16
17     // Instantiate
18     FA FA_1(in_A, in_B, in_Cin, out_Sum, out_Cout);
19
20     initial
21     begin
22         // All combinations
23         in_A=0; in_B=0; in_Cin=0;
24         #5 in_A=0; in_B=0; in_Cin=1;
25
26         #5 in_A=0; in_B=1; in_Cin=0;
27         #5 in_A=0; in_B=1; in_Cin=1;
28
29         #5 in_A=1; in_B=0; in_Cin=0;
30         #5 in_A=1; in_B=0; in_Cin=1;
31
32         #5 in_A=1; in_B=1; in_Cin=0;
33         #5 in_A=1; in_B=1; in_Cin=1;
34
35         #5 $finish;
36     end
37
38     initial
39         $monitor("\nTime=%0t | A=%b B=%b Cin=%b | Sum=%b Cout=%b",
40                 $time, in_A, in_B, in_Cin, out_Sum, out_Cout);
41
42 endmodule
43

```

Fig: 5B (Testbench for 1-Bit Full Adder)

Figure 5A and 5B shows the code for one-bit Full Adder and one-bit Full Adder's testbench. The testbench code is used to running the simulation.

The screenshot displays two windows from the Cadence Design System:

- Design Browser 1 - SimVision**: This window shows the simulation environment. The top menu bar includes File, Edit, View, Select, Explore, Simulation, Windows, and Help. The toolbar contains various simulation and design tools. A status bar at the bottom shows "TimeA = 40,000 ps" and "40,000ps + 0". The main area is divided into two panes: "Design Browser" and "Objects". The "Design Browser" pane shows a tree structure with "simulator" expanded to show "FA_tb". The "Objects" pane displays a table of simulation results for the "FA_tb" instance, listing inputs (in_A, in_B, in_Cin) and outputs (out_Cout, out_Sum) all having a value of 1.
- Console - SimVision**: This window shows the command-line interface for the simulation. It includes a menu bar (File, Edit, View, Simulation, Windows, Help), a toolbar, and a text search field. The main text area displays the Xcelium simulation logs, which include source commands for the XCELIUM1909 tools, database opening, probe creation, and simulation results. The results show the progression of the full adder's state over time, starting from Time=0 and ending at Time=35000.

Fig: 6A (Simulation of 1-Bit Full Adder)

```

Time=0 | A=0 B=0 Cin=0 | Sum=0 Cout=0

Time=5000 | A=0 B=0 Cin=1 | Sum=1 Cout=0

Time=10000 | A=0 B=1 Cin=0 | Sum=1 Cout=0

Time=15000 | A=0 B=1 Cin=1 | Sum=0 Cout=1

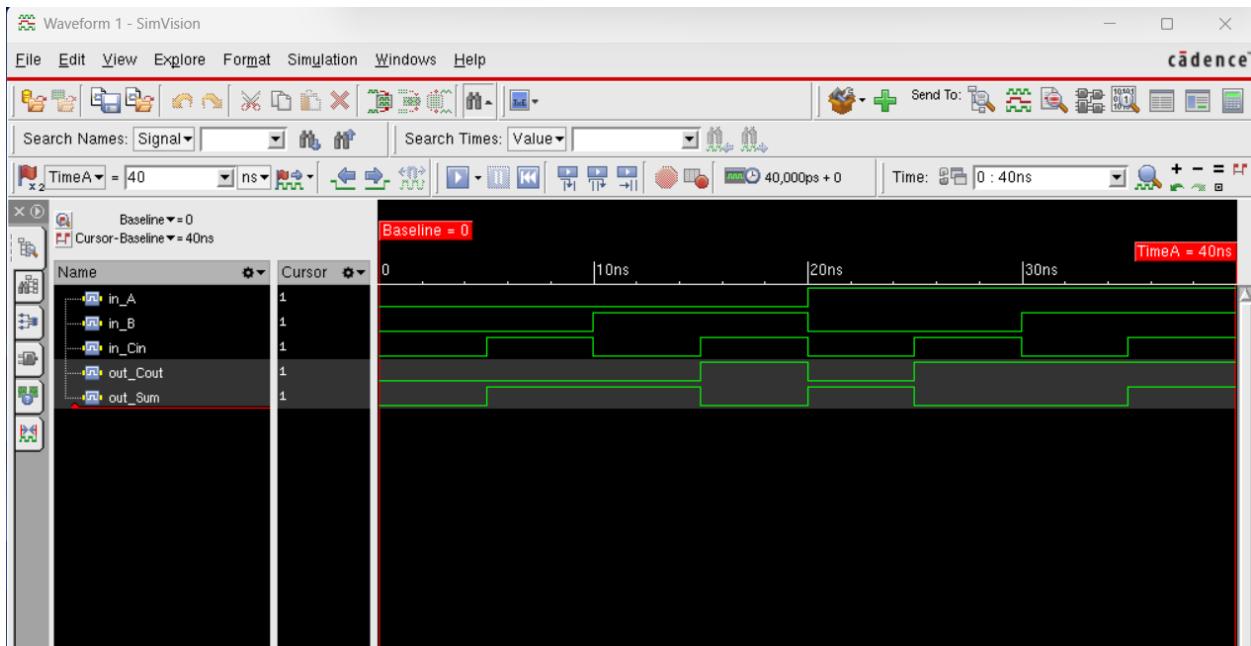
Time=20000 | A=1 B=0 Cin=0 | Sum=1 Cout=0

Time=25000 | A=1 B=0 Cin=1 | Sum=0 Cout=1

Time=30000 | A=1 B=1 Cin=0 | Sum=0 Cout=1

Time=35000 | A=1 B=1 Cin=1 | Sum=1 Cout=1

```

Fig: 6B (Showing correct calculation)**Fig: 6C (Waveform of 1-Bit Full Adder)**

The simulation figures shown in figure 6A and 6B verifies correct Full Adder operation.

The Sum output follows the XOR relationship of inputs, while the Carry output is asserted whenever at least two inputs are high. Same way the figure 6C, the waveforms clearly show correct propagation of carry and sum bits for all input combinations.

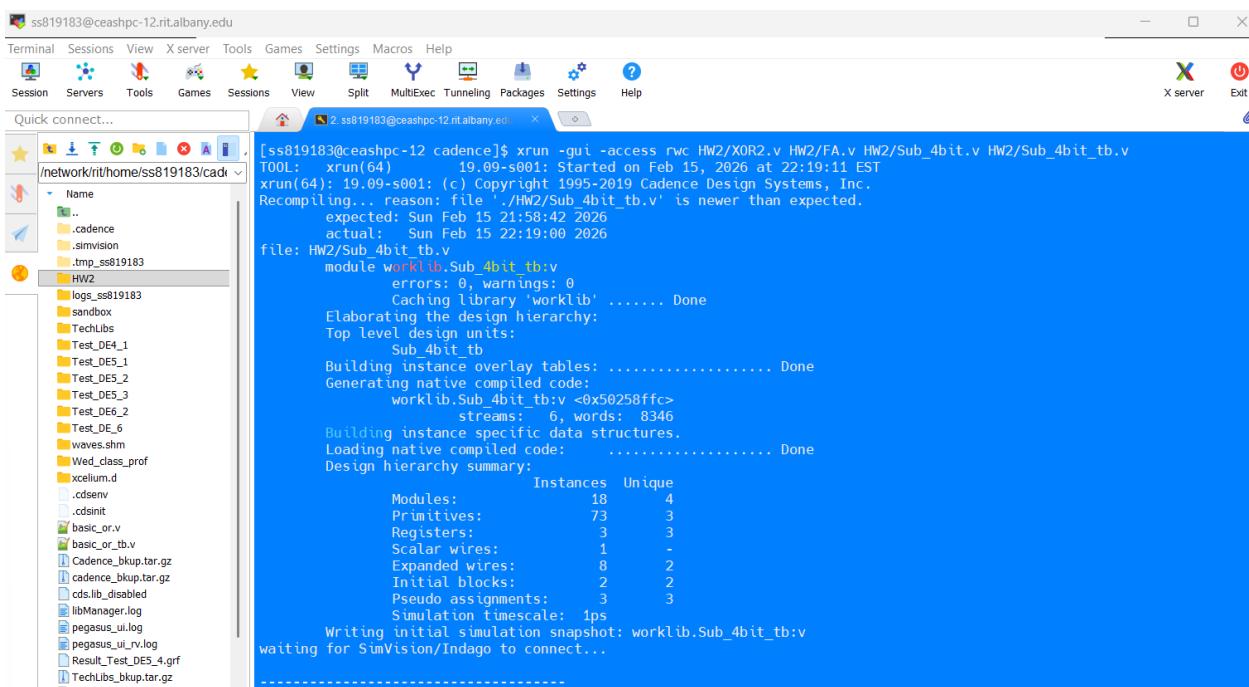
3. Four-Bit Full Subtractor (Using Full Adder):

Subtraction was implemented using 2's complement logic:

$$A - B = A + (B' + 1)$$

Implementation steps:

- a) Each bit of B is XORed with Bin (control signal).
- b) Bin is also connected as the initial carry-in.
- c) Four Full Adders are connected in ripple-carry fashion.
- d) Final borrow is obtained from the inverted final carry

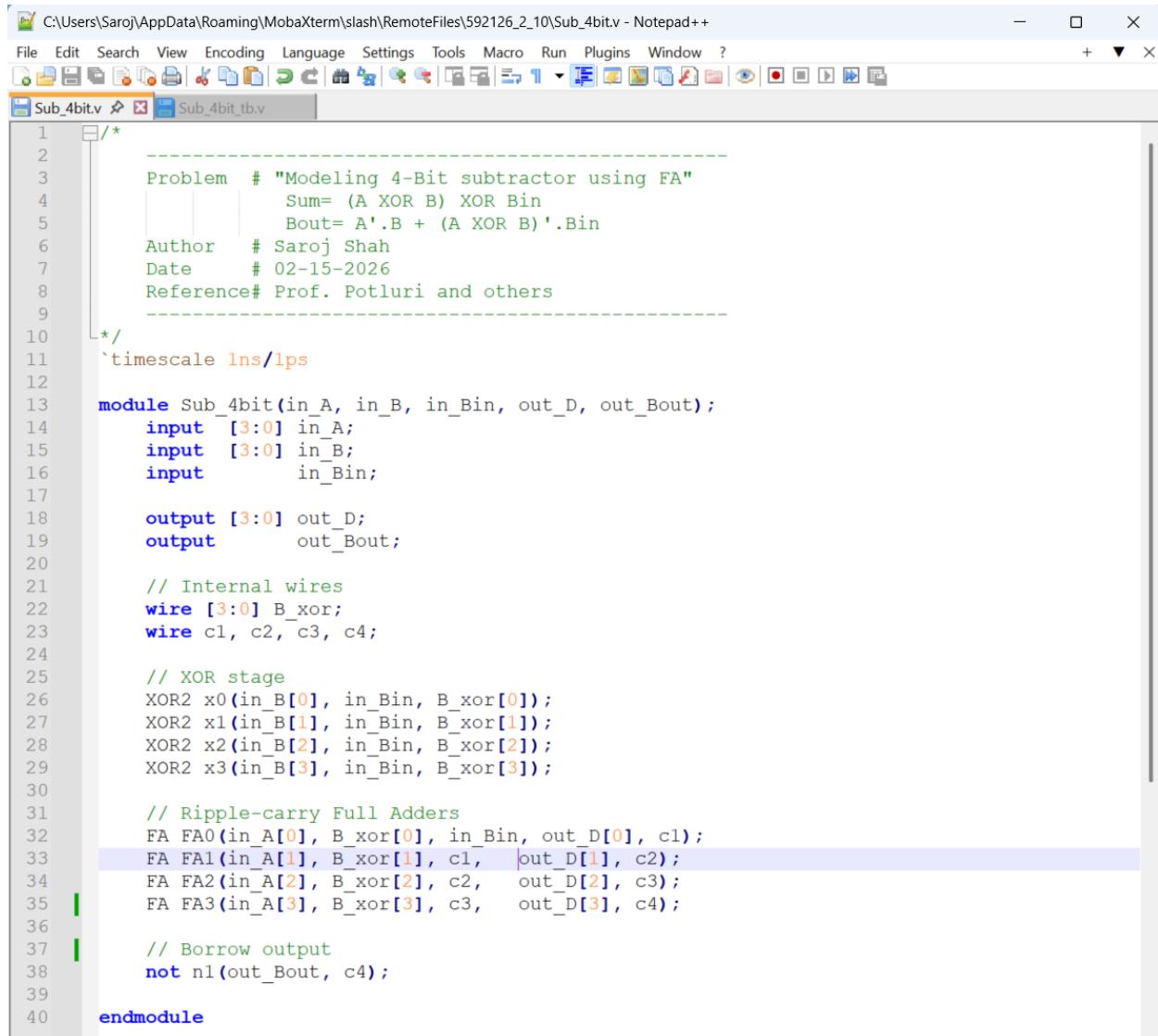


The screenshot shows a MobaXterm window with a terminal session titled 'ss819183@ceashpc-12.rit.albany.edu'. The terminal window displays the command 'xrun -gui -access rwc Hw2/XOR2.v Hw2/FA.v Hw2/Sub_4bit.v Hw2/Sub_4bit_tb.v' being run. The output of the command shows the simulation process starting on Feb 15, 2026, at 22:19:11 EST. It includes copyright information for Cadence Design Systems, Inc., recompiling details, and a summary of the design hierarchy and simulation parameters. The terminal window has a standard Xfce interface with icons for Session, Servers, Tools, Games, Sessions, View, Split, MultiExec, Tunneling, Packages, Settings, Help, X server, and Exit.

```
[ss819183@ceashpc-12 cadence]$ xrun -gui -access rwc Hw2/XOR2.v Hw2/FA.v Hw2/Sub_4bit.v Hw2/Sub_4bit_tb.v
TOOL: xrun(64)      19.09-s001: Started on Feb 15, 2026 at 22:19:11 EST
xrun(64): 19.09-s001: (c) Copyright 1995-2019 Cadence Design Systems, Inc.
Recompiling... reason: file './Hw2/Sub_4bit_tb.v' is newer than expected.
    expected: Sun Feb 15 21:58:42 2026
    actual:  Sun Feb 15 22:19:00 2026
file: Hw2/Sub_4bit_tb.v
module worklib.Sub_4bit_tb:v
    errors: 0, warnings: 0
    Caching library 'worklib' ..... Done
Elaborating the design hierarchy:
Top level design units:
    Sub_4bit_tb
Building instance overlay tables: ..... Done
Generating native compiled code:
    worklib.Sub_4bit_tb:v <0x50258ffc>
        streams: 6, words: 8346
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
      Instances  Unique
Modules:          18      4
Primitives:       73      3
Registers:        3      3
Scalar wires:     1      -
Expanded wires:   8      2
Initial blocks:   2      2
Pseudo assignments: 3      3
Simulation timescale: 1ps
Writing initial simulation snapshot: worklib.Sub_4bit_tb:v
waiting for SimVision/Indago to connect...
```

Fig: 7 (MobaXterm window)

The above Figure 4 shows the MobaXterm window for running Four-bit Subtractor.



The screenshot shows a Notepad++ window with the file path `C:\Users\Saroj\AppData\Roaming\MobaXterm\slash\RemoteFiles\592126_2_10\Sub_4bit.v`. The code is written in Verilog and defines a module for a 4-bit subtractor. The code includes comments explaining the problem, author information, and the logic implementation using XOR gates and full adders.

```

1  /*
2   -----
3   Problem # "Modeling 4-Bit subtractor using FA"
4   | Sum= (A XOR B) XOR Bin
5   | Bout= A'.B + (A XOR B)'.Bin
6   Author # Saroj Shah
7   Date # 02-15-2026
8   Reference# Prof. Potluri and others
9   -----
10 */
11 `timescale 1ns/1ps
12
13 module Sub_4bit(in_A, in_B, in_Bin, out_D, out_Bout);
14     input [3:0] in_A;
15     input [3:0] in_B;
16     input      in_Bin;
17
18     output [3:0] out_D;
19     output      out_Bout;
20
21     // Internal wires
22     wire [3:0] B_xor;
23     wire c1, c2, c3, c4;
24
25     // XOR stage
26     XOR2 x0(in_B[0], in_Bin, B_xor[0]);
27     XOR2 x1(in_B[1], in_Bin, B_xor[1]);
28     XOR2 x2(in_B[2], in_Bin, B_xor[2]);
29     XOR2 x3(in_B[3], in_Bin, B_xor[3]);
30
31     // Ripple-carry Full Adders
32     FA FA0(in_A[0], B_xor[0], in_Bin, out_D[0], c1);
33     FA FA1(in_A[1], B_xor[1], c1,    out_D[1], c2);
34     FA FA2(in_A[2], B_xor[2], c2,    out_D[2], c3);
35     FA FA3(in_A[3], B_xor[3], c3,    out_D[3], c4);
36
37     // Borrow output
38     not nl(out_Bout, c4);
39
40 endmodule

```

Fig: 8A (Code for 4-Bit Subtractor)

```

C:\Users\Saroj\AppData\Roaming\MobaXterm\slash\RemoteFiles\592126_2_11\Sub_4bit_tb.v - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
Sub_4bit.v Sub_4bit_tb.v

1  /*
2   -----
3   Problem    # "Testbench for 4-Bit subtractor"
4   Author     # Saroj Shah
5   Date       # 02-15-2026
6   Reference  # Prof. Potluri and others
7   -----
8 */
9
10 `timescale 1ns/1ps
11
12 module Sub_4bit_tb;
13
14     reg [3:0] in_A;
15     reg [3:0] in_B;
16     reg         in_Bin;
17
18     wire [3:0] out_D;
19     wire         out_Bout;
20
21     // Instantiating
22     Sub_4bit sub1(in_A, in_B, in_Bin, out_D, out_Bout);
23
24     initial begin
25
26         /*
27         // When in_Bin = 0, it will do ADDITION
28         in_Bin = 0;
29
30         #10 in_A = 4'b0101;  in_B = 4'b0011;    // 5 + 3 = 8
31         #10 in_A = 4'b1001;  in_B = 4'b0110;    // 9 + 6 = 15
32         #10 in_A = 4'b0111;  in_B = 4'b1000;    // 7 + 8 = 15
33         */
34
35         // When in_Bin = 1, it will do SUBTRACTION
36         in_Bin = 1;
37
38         #10 in_A = 4'b1001;  in_B = 4'b0011;    // 9 - 3 = 6
39         #10 in_A = 4'b0101;  in_B = 4'b0111;    // 5 - 7 = -2 (Borrow=1)
40         #10 in_A = 4'b1000;  in_B = 4'b1000;    // 8 - 8 = 0
41         #10 in_A = 4'b0000;  in_B = 4'b0001;    // 0 - 1 = -1 (Borrow=1)
42         #10 $finish;
43     end
44
45     initial begin
46         $monitor("\nTime=%0t | Mode=%b | A=%0d(%b) B=%0d(%b) | Result=%0d(%b) Borrow=%b",
47         | $time, in_Bin, in_A, in_A, in_B, in_B, out_D, out_D, out_Bout);
48     end
49
50 endmodule

```

Fig: 8B (Testbench code for 4-Bit Subtractor)

Figure 8A and 8B shows the code for 4-bit subtractor and 4-bit subtractor's testbench.

The testbench code is used to running the simulation. The figures are shown below.

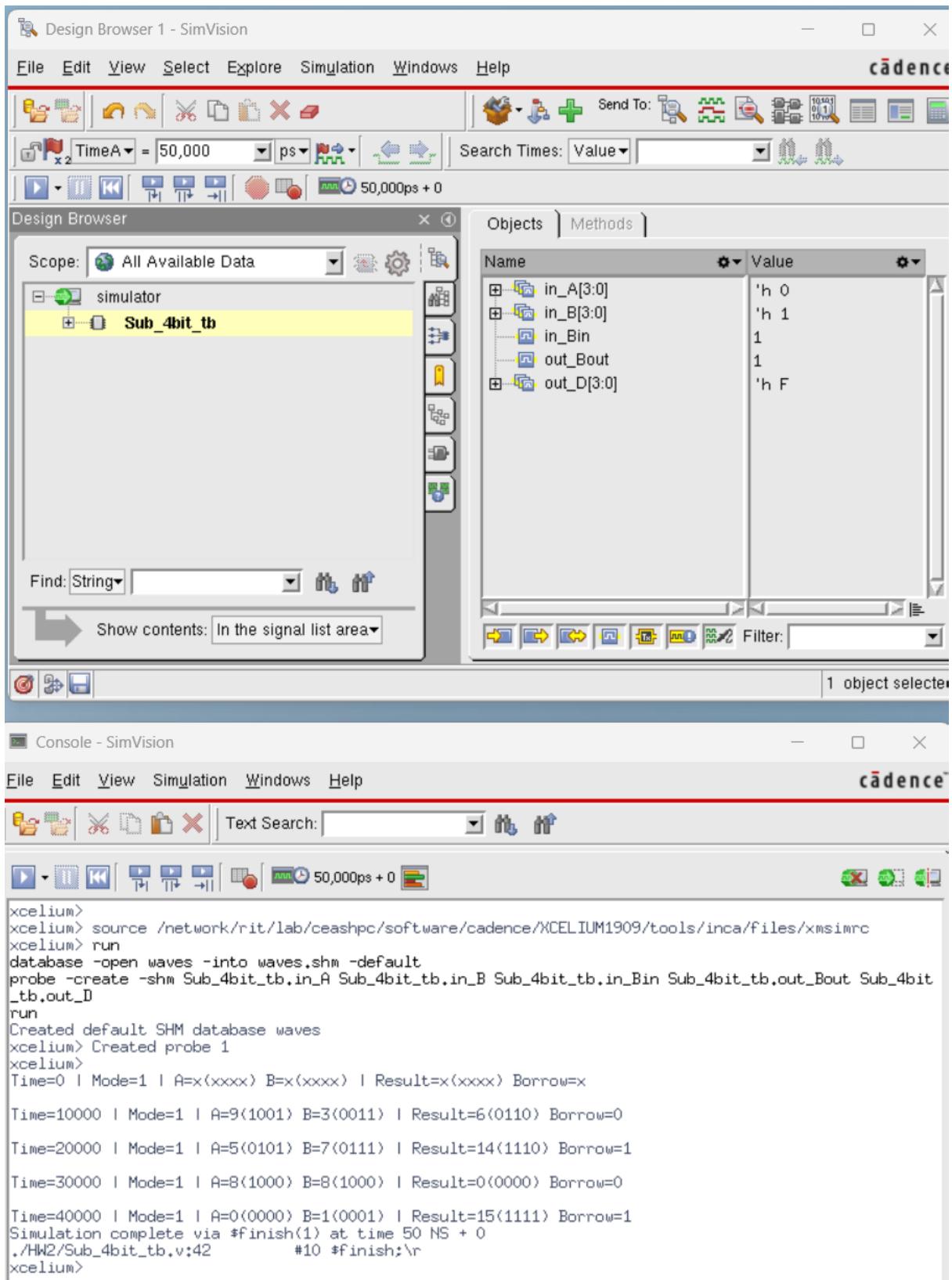
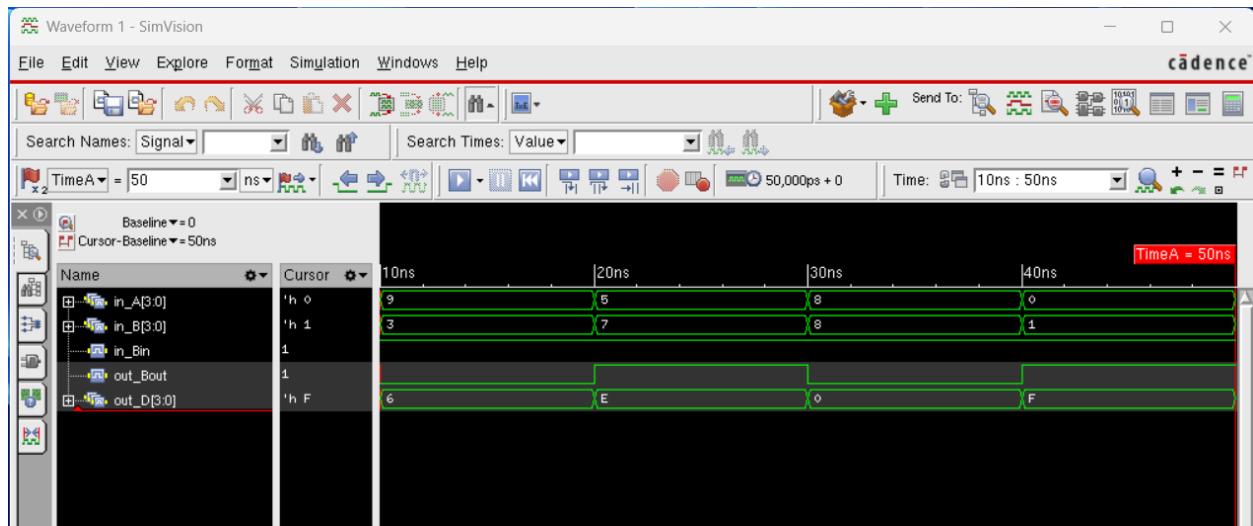


Fig: 9A (Simulation of 4-Bit Subtractor)

```

Time=0 | Mode=1 | A=x(xxxx) B=x(xxxx) | Result=x(xxxx) Borrow=x
Time=10000 | Mode=1 | A=9(1001) B=3(0011) | Result=6(0110) Borrow=0
Time=20000 | Mode=1 | A=5(0101) B=7(0111) | Result=14(1110) Borrow=1
Time=30000 | Mode=1 | A=8(1000) B=8(1000) | Result=0(0000) Borrow=0
Time=40000 | Mode=1 | A=0(0000) B=1(0001) | Result=15(1111) Borrow=1

```

Fig: 9B (Result of 4-Bit Subtractor)**Fig: 9C (Waveform of 4-Bit Subtractor)**

Test cases verified:

- $9 - 3 = 6$
- $5 - 7 = -2$ (Borrow = 1)
- $8 - 8 = 0$
- $0 - 1 = -1$ (Borrow = 1)

The simulation figures and waveform shown in figure 9A, 9B and 9C verifies correct operation and result of the Subtractor. The waveforms show correct difference bits and proper borrow generation. The subtractor correctly performs subtraction when Bin = 1.

Conclusion:

In this assignment, several fundamental combinational logic circuits were successfully designed and simulated using structural Verilog modeling in Cadence Xcelium. The simulation waveforms verified the correct functional behavior for all modules.

Works Cited

Potluri, Seetal. Class Notes, PDF and videos, Spring 2026.