

Cover Sheet

520 VLSI Design Exercise 6

Title: Design, layout, and simulate

CMOS 3-input OR circuit

using Cadence

For

By: Saroj Shah

Date: Nov 20, 2025

Design Exercise-6, Professor James R. Moulic

Introduction and Summary:

In this design exercise, using Cadence software, we are designing, laying out, and simulating a standard-cell **10-track macro** of a **0.045 μm (45nm) CMOS 3-input OR circuit**.

Materials:

Computer and Cadence software.

Data:

Please refer to the screenshot provided below:

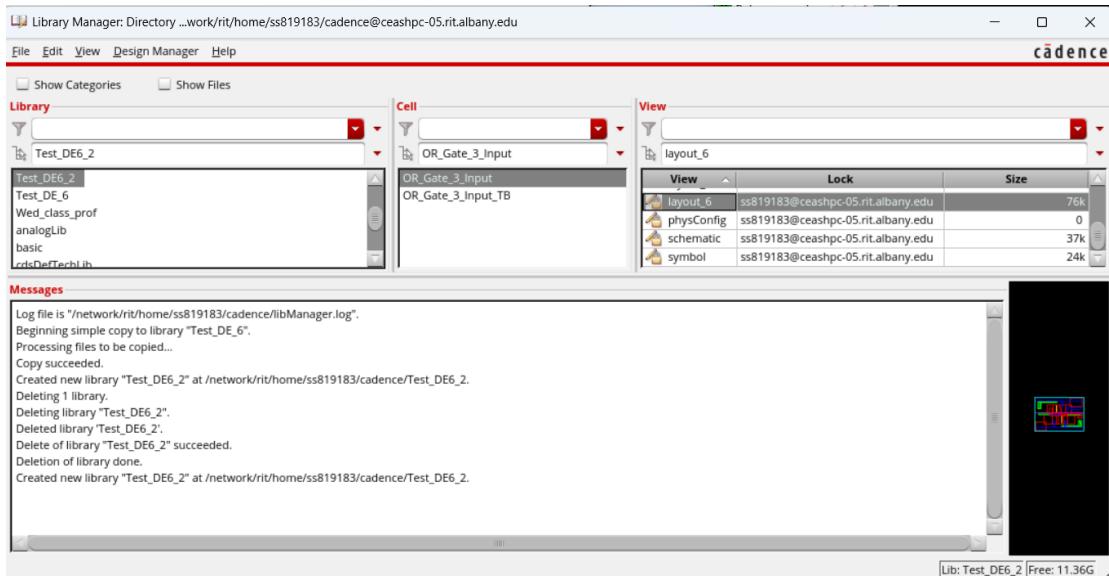


Fig: Library manager

Schematic Part:

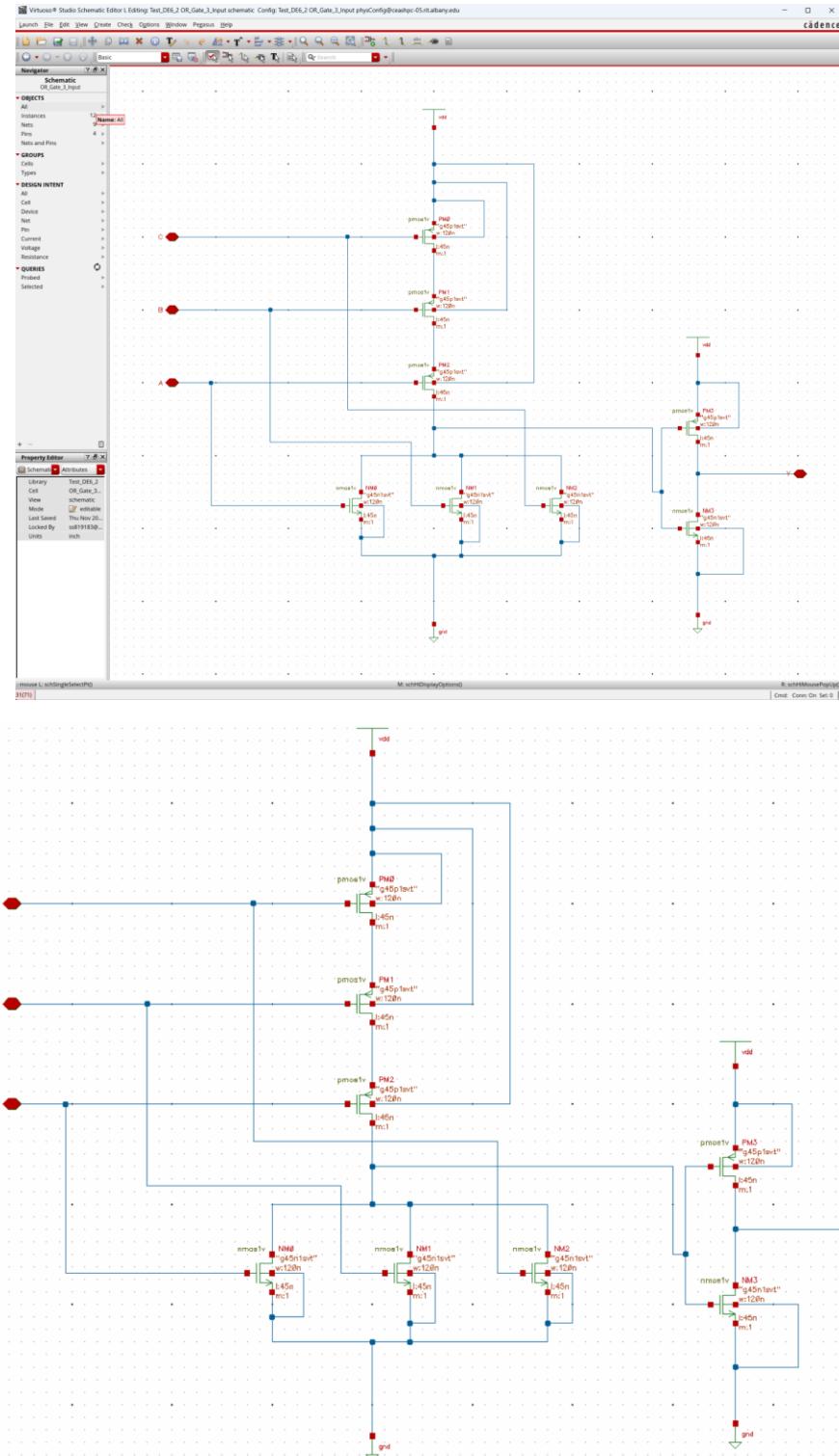


Fig: Schematic showing the OR-Gate

Symbol creation:

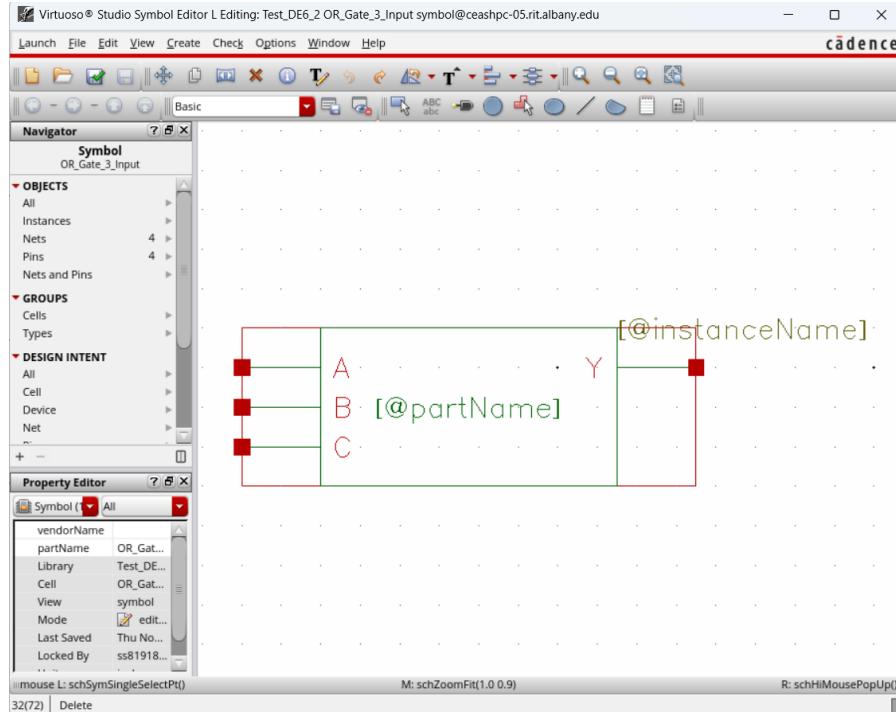


Fig: The ‘OR’ gate schematic is symbolically represented

Testbench:

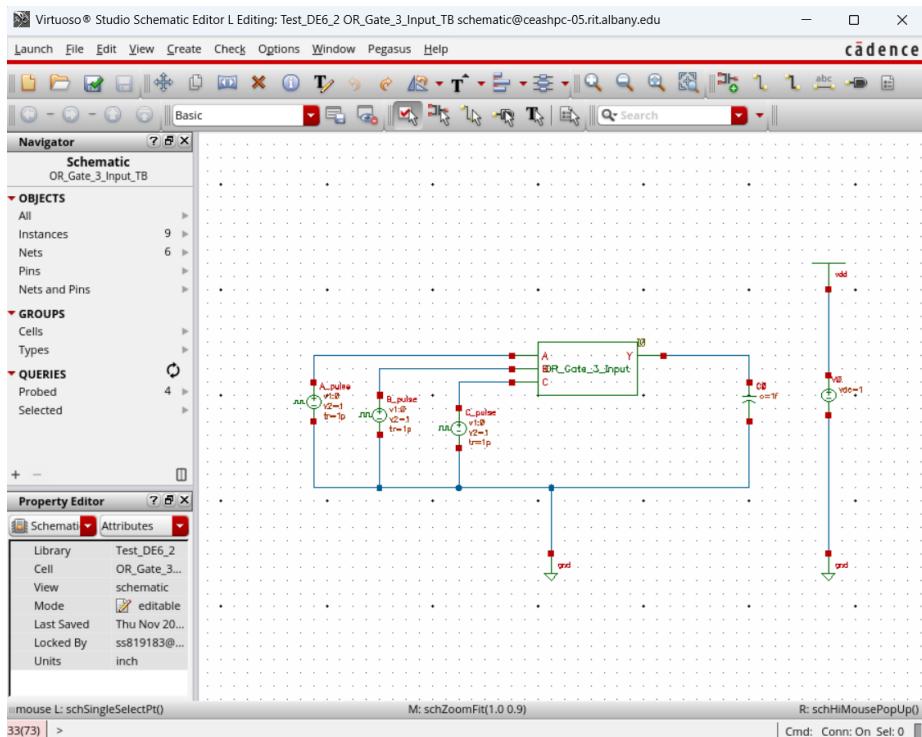


Fig: Testbench’s Schematic

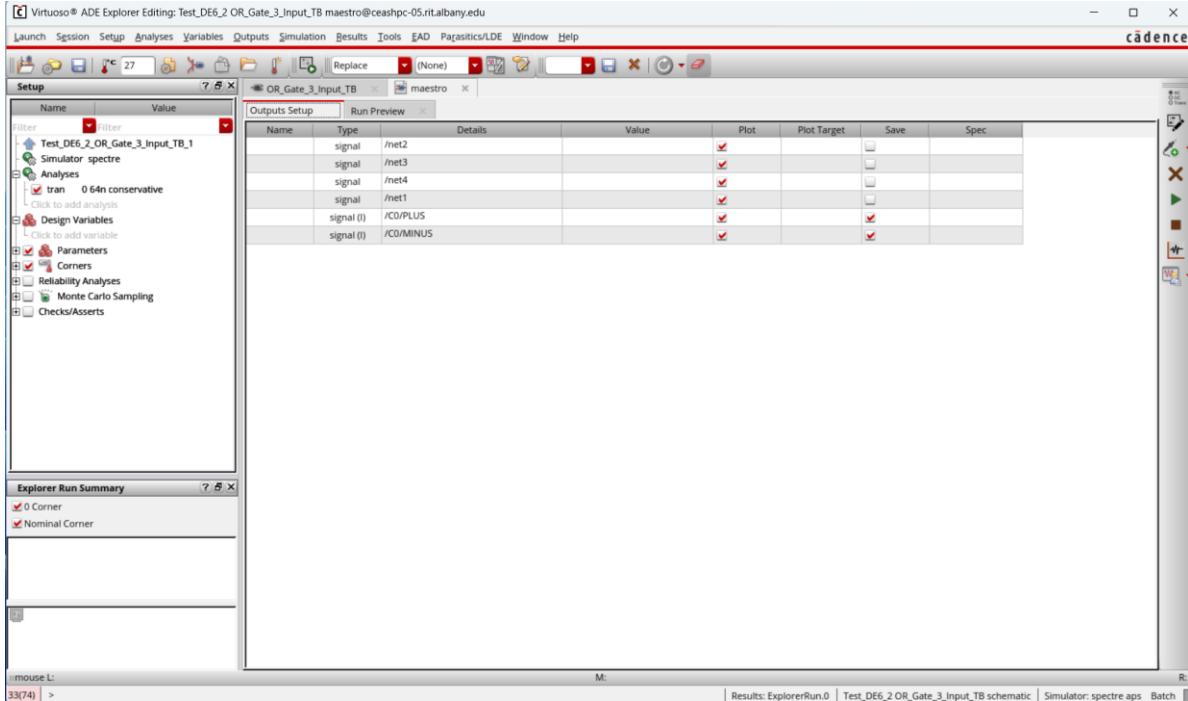


Fig: Output setup (in Maestro)

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C:/network/rit/home/ss819183/simulation/Test_DE6_2/OR_Gate_3_Input_TB/maestro/results/maestro/ExplorerRun.0/1/Test_DE6_2_OR_Gate_3_Input_TB.1/psf/spectre.out@ceash...
File Edit View Help
cadence

34 (2.2 %) 36 (4.5 %) 40 (1.1 %) 44 (1.1 %)
55 (1.1 %)
Total: 147.1%
Initial condition solution time: CPU = 4.481 ms, elapsed = 4.51994 ms.
Intrinsic tran analysis time: CPU = 192.709 ms, elapsed = 198.973 ms.
Total time required for tran analysis`tran`: CPU = 199.276 ms, elapsed = 207.572 ms, util. = 96%.
Time accumulated: CPU = 823.611 ms, elapsed = 942.066 ms.
Peak resident memory used = 193 Mbytes.

finalTimeOP: writing operating point information to rawfile.
Opening the PSF file ../psf/finalTimeOP.info ...
modelParameter: writing model parameter values to rawfile.
Opening the PSF file ../psf/modelParameter.info ...
element: writing instance parameter values to rawfile.
Opening the PSF file ../psf/element.info ...
outputParameter: writing output parameter values to rawfile.
Opening the PSF file ../psf/outputParameter.info ...
designParamVals: writing netlist parameters to rawfile.
Opening the PSFASCII file ../psf/designParamVals.info ...
primitives: writing primitives to rawfile.
Opening the PSFASCII file ../psf/primitives.info.primitives ...
subckts: writing subcircuits to rawfile.
Opening the PSFASCII file ../psf/subckts.info.subckts ...
Licensing Information:
Lic Summary:
[23:27:33.380587] CdsLmd servers:5280@cadence-lm-p102.its.albany.edu
[23:27:33.380618] Feature usage summary:
[23:27:33.380618] Virtuoso_Multi_mode_Simulation

Aggregate audit (11:27:33 PM, Thur Nov 20, 2025):
Time used: CPU = 847 ms, elapsed = 980 ms, util. = 86.4%.
Time spent in licensing: elapsed = 111 ms, percentage of total = 11.4%.
Peak memory used = 195 Mbytes.
Simulation started at: 11:27:32 PM, Thur Nov 20, 2025, ended at: 11:27:33 PM, Thur Nov 20, 2025, with elapsed time (wall clock): 980 ms.
spectre completes with 0 errors, 0 warnings, and 5 notices.

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Fig: Showing portion of Netlist

Simulation of testbench:

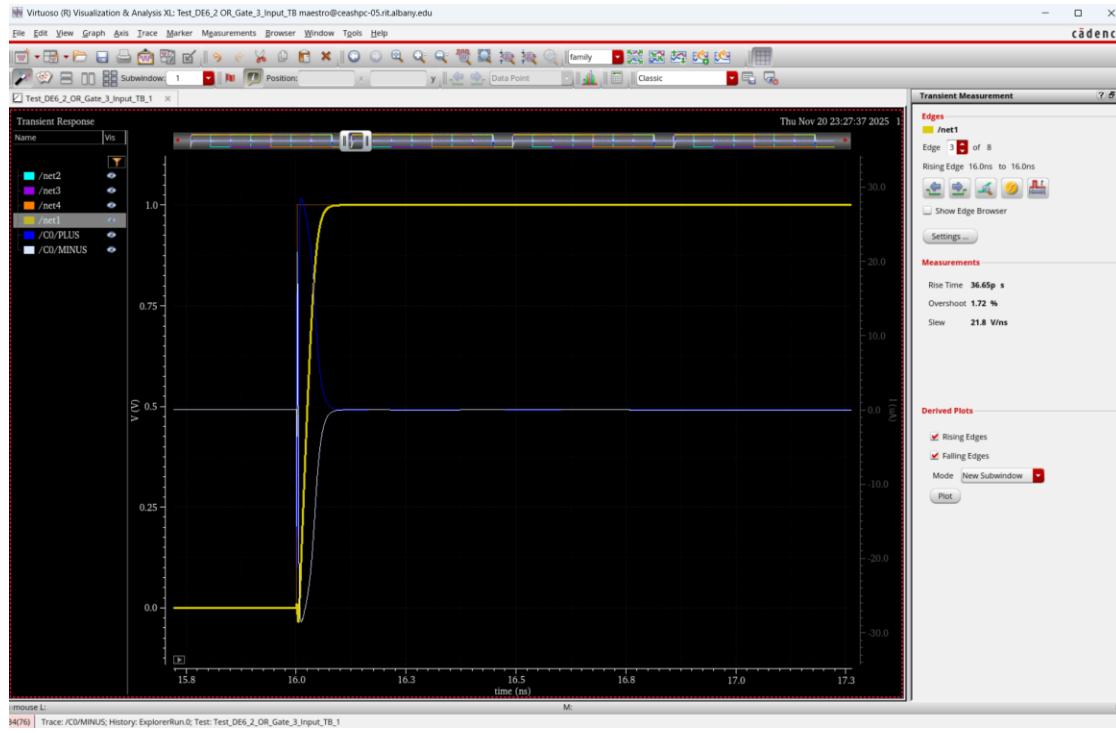


Fig: Simulation showing Rise time: 36.59p s and source current of 28.51uA

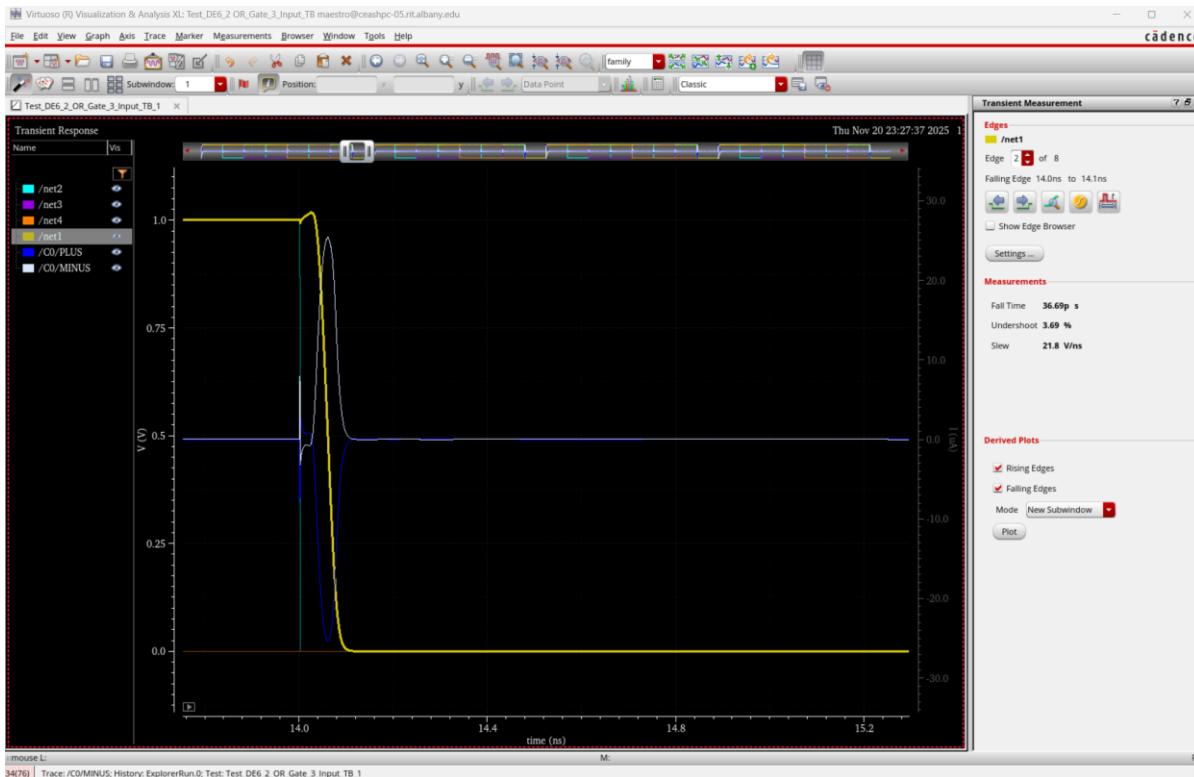


Fig: Simulation showing Fall Time of 36.69p s and sink current of 25.40uA

Layout:

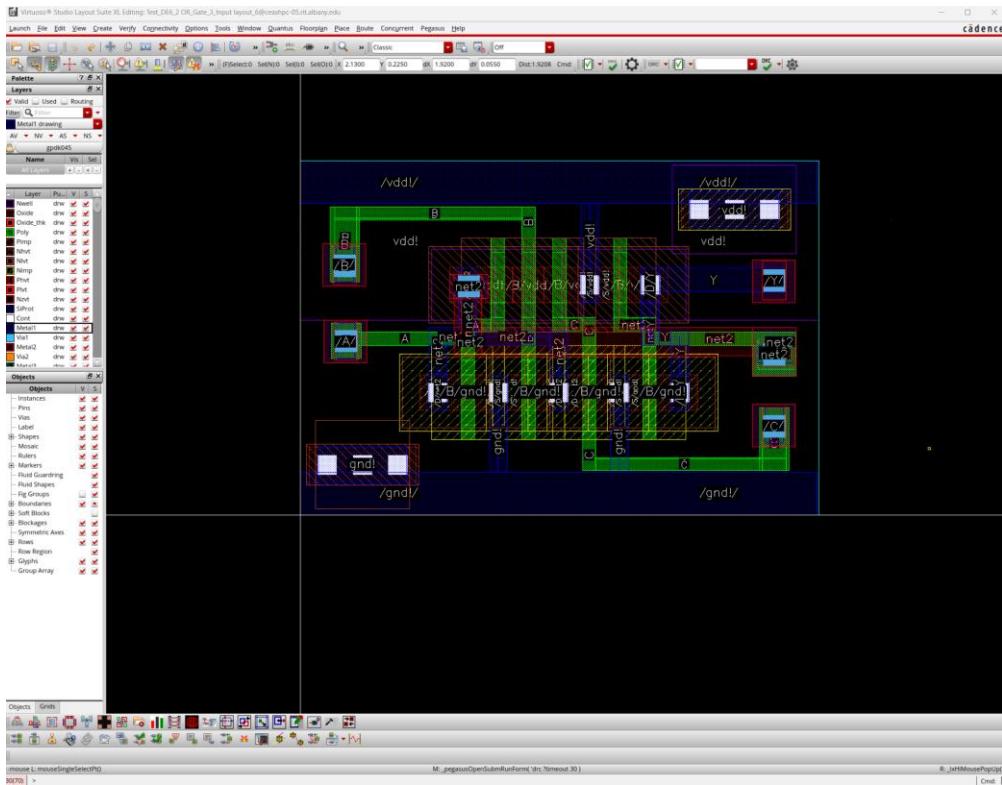


Fig: Layout

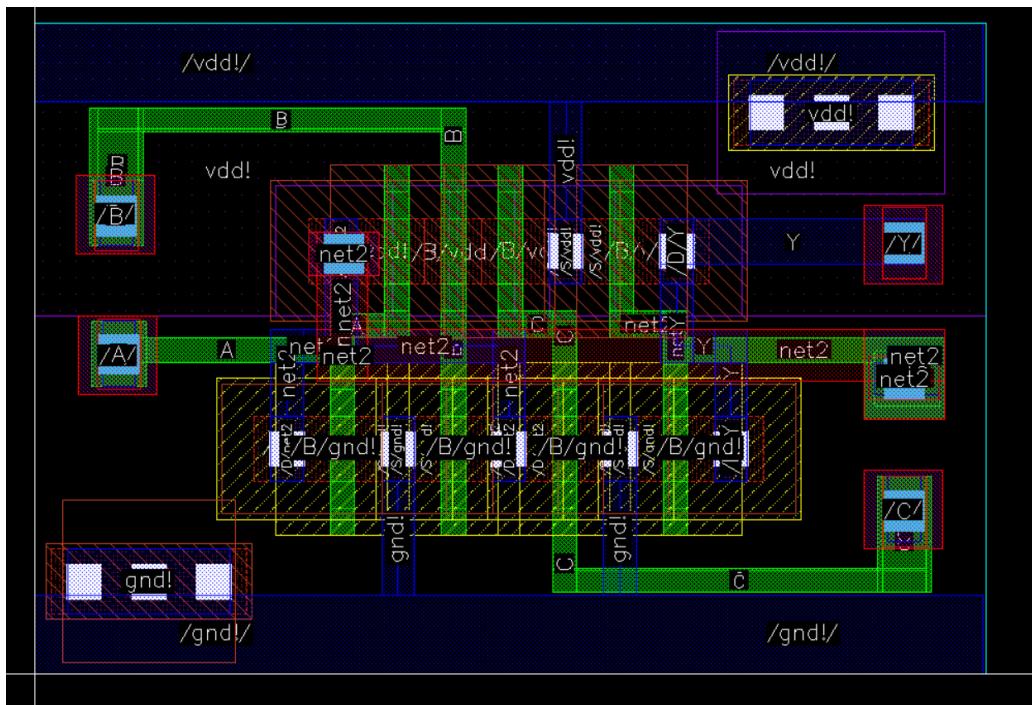


Fig: Layout in detail

DRC Results:

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Pegasus 23.26-64b Reports: Done [DRC] layout_...@ceashpc-05.rit.albany.edu
[DRC] layout_5 [DRC] layout_6

Total CPU Time : 1 (s)
Total Real Time : 2 (s)
Total Original Geometry : 166(190)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
ASCII report database is /network/rit/home/ss819183/cadence/Test_DE6_2/OR_Gate_3_Input.drc_errors.ascii
INFO: Checking in all SoftShare licenses.

Pegasus finished normally. 2025-11-20 22:52:15

Issues List
No errors found
Find [ ] Prev [ ] Next [ ] Match case [ ] Whole word [ ] Use RegExp [ ] Highlight [ ]
Warnings: 9 Info: 21
WARNING (XSTREAM-20): Output Stream file '/network/rit/home/ss819183/cadence/Test_DE6_2/OR_Gate_3_Input/layout_6/OR_Gate_3_Input.gds.gz' already exists. It will be overwritten.
WARNING (XSTREAM-333): The 'enableColoring' option will be ignored during XStream Out. This is because there is no color entry in the layer map and the object map file.
WARNING: In technology 'gpdk045_pvs', the rule set 'default' is not a Pegasus rule set.
WARNING: LAYOUT_PATH at line 30 in file /network/rit/home/ss819183/cadence/TechLibs/gpdk045_v_6_0/pvs/.pviDRC.rul is skipped. It is set in control file.
WARNING: Cmdline override: LAYOUT IT PRIMARY "OR_Gate_3_Innm1".

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Fig: DRC running

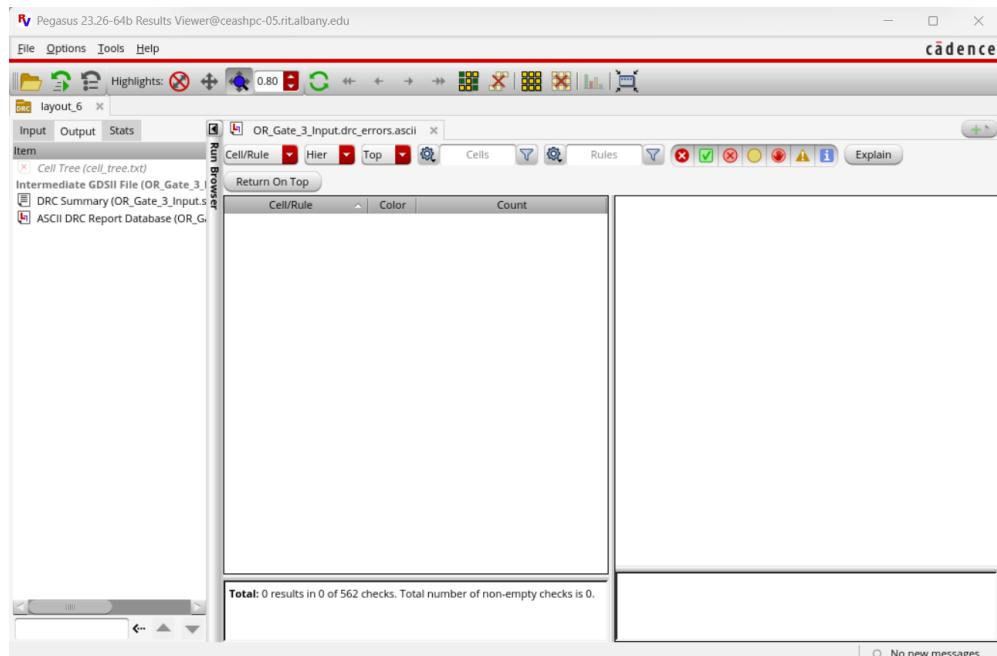


Fig: DRC Result showing absence of error

The above DRC check shows no errors, indicating that the Layout was created successfully.

Conclusion:

The testbench simulation shows a rise time of 36.59 ps with a source current of 28.51 μ A, and a fall time of 36.69 ps with a sink current of 25.40 μ A. These values fall within the acceptable range specified in the problem statement. Furthermore, the absence of DRC errors confirms that the layout of the three-input OR gate has been successfully completed.

Works Cited

Moulic, James R. Class Notes. PDF and videos.