Cover Sheet

520 VLSI Design Exercise 6

Title: Design, layout, and simulate

CMOS 3-input OR circuit

using Cadence

For

By: Saroj Shah

Date: Nov 20, 2025

Design Exercise-6, Professor James R. Moulic

Introduction and Summary:

In this design exercise, using Cadence software, we are designing, laying out, and simulating a standard-cell **10-track** macro of a **0.045 µm (45nm) CMOS 3-input OR circuit.**

Materials:

Computer and Cadence software.

Data:

Please refer to the screenshot provided below:

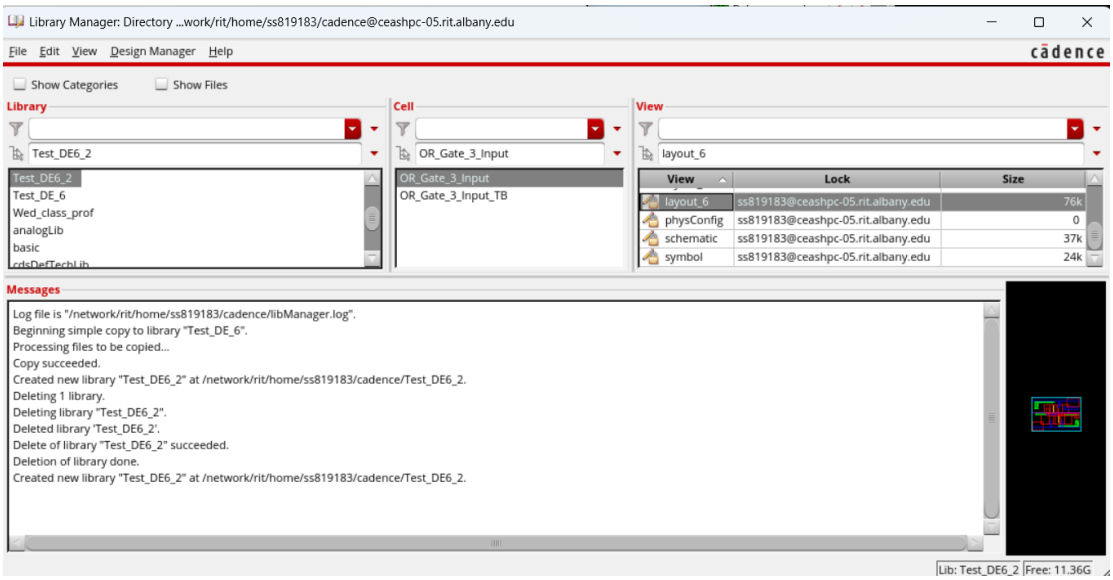

Fig: Library manager

Schematic Part:

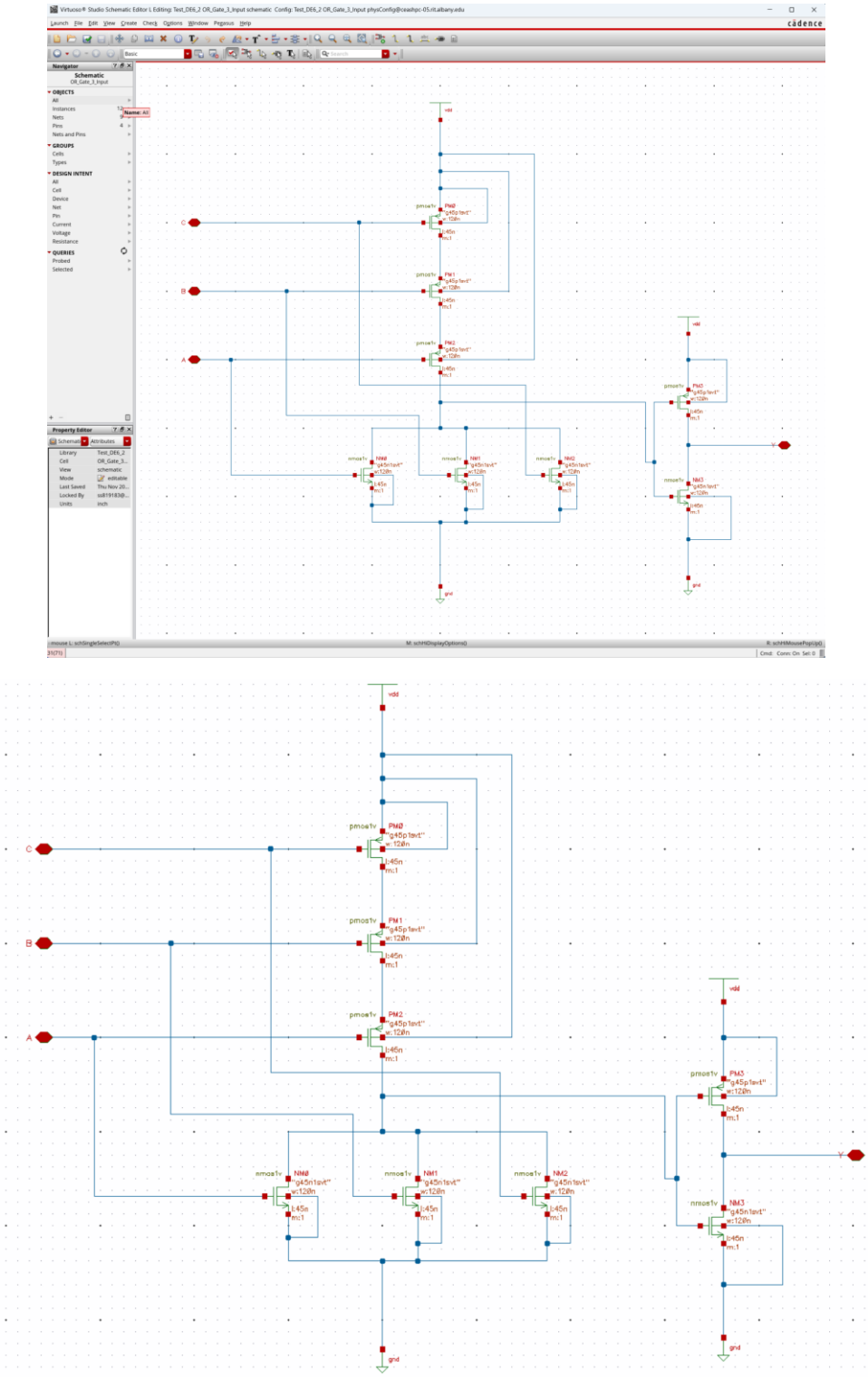

Fig: Schematic showing the OR-Gate

Symbol creation:

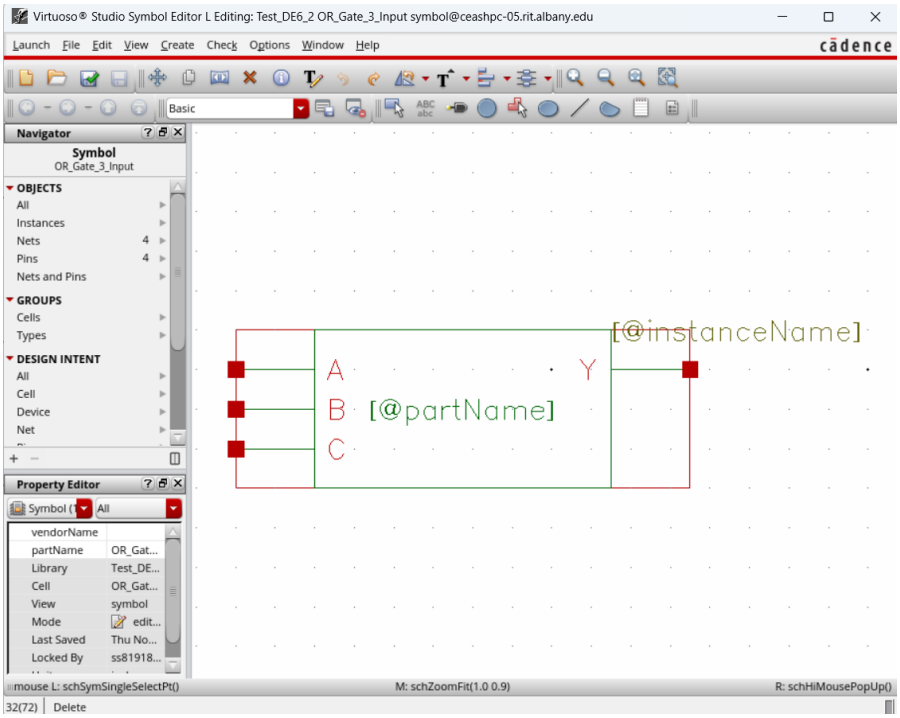

Fig: The 'OR' gate schematic is symbolically represented

Testbench:

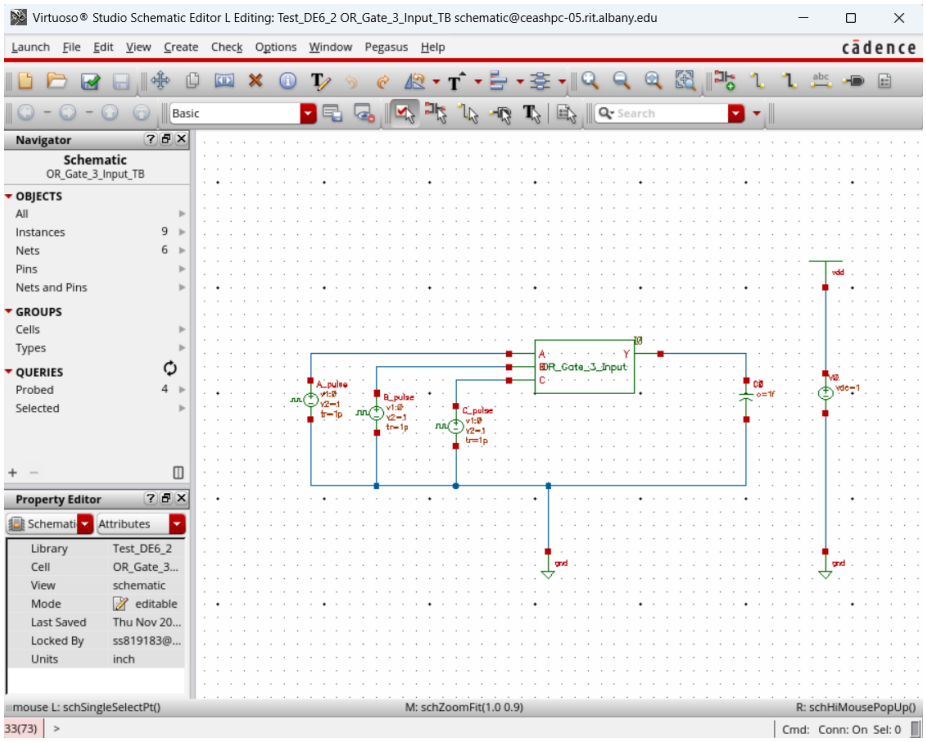

Fig: Testbench's Schematic

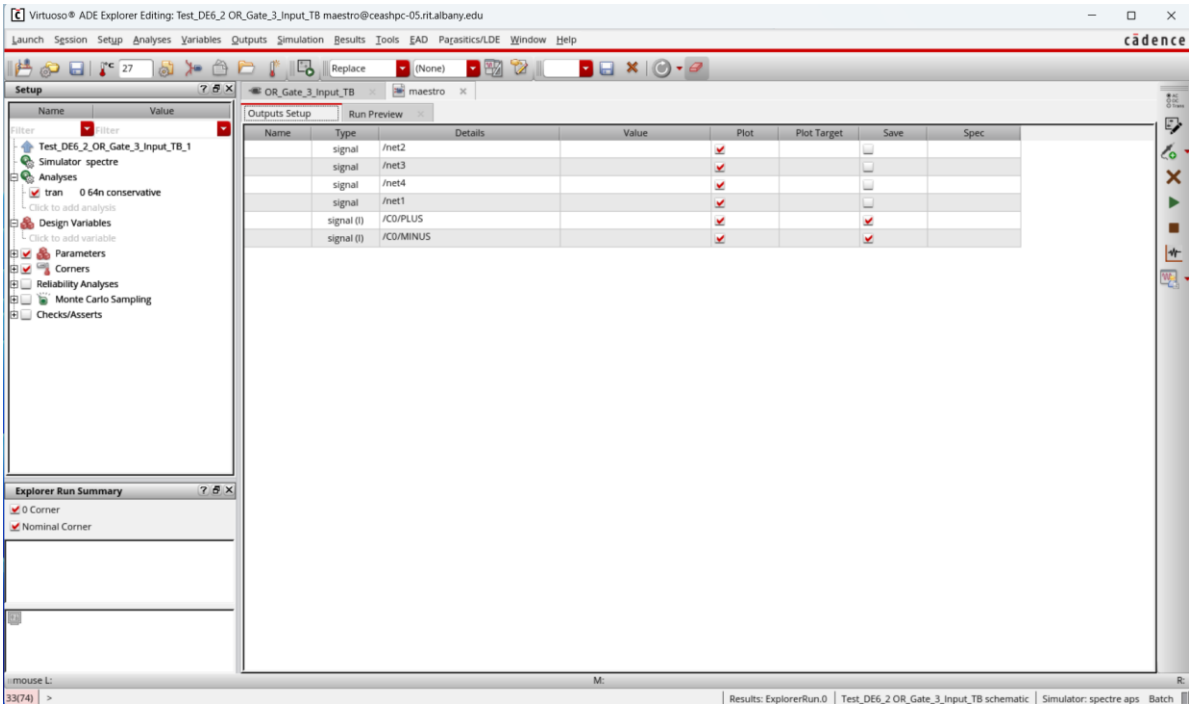

Fig: Output setup (in Maestro)

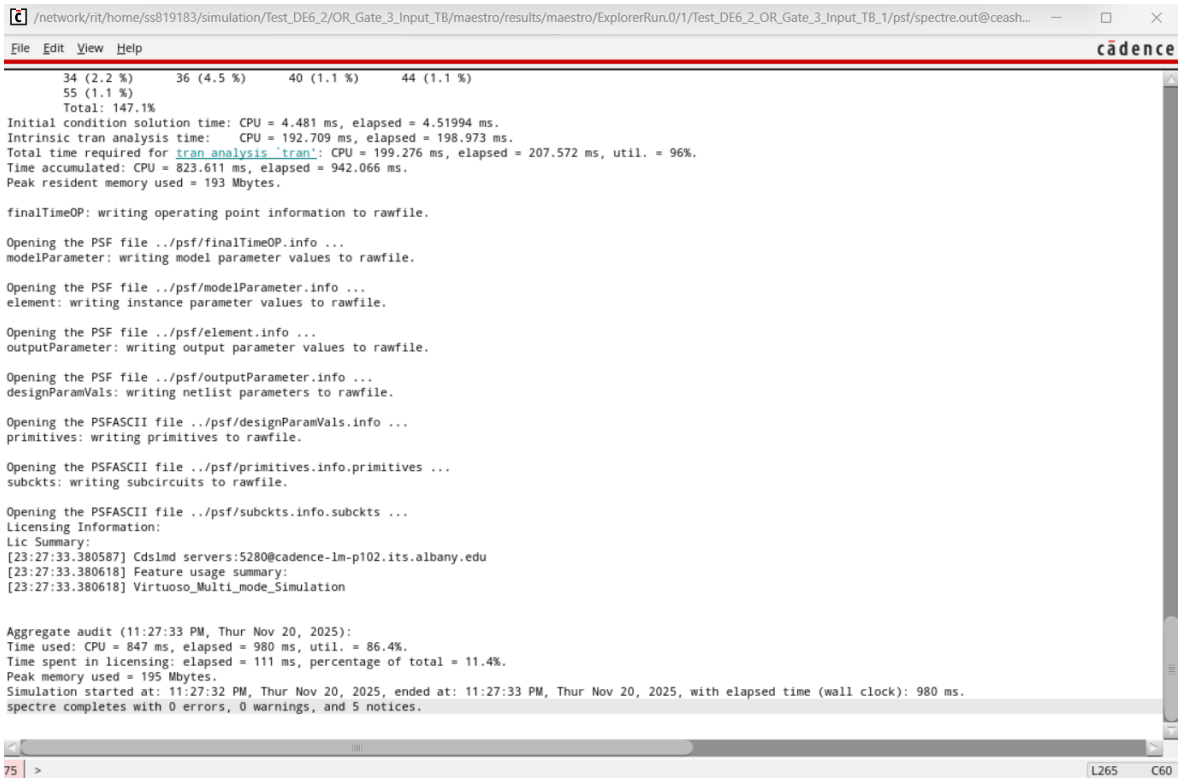

Fig: Showing portion of Netlist

Simulation of testbench:

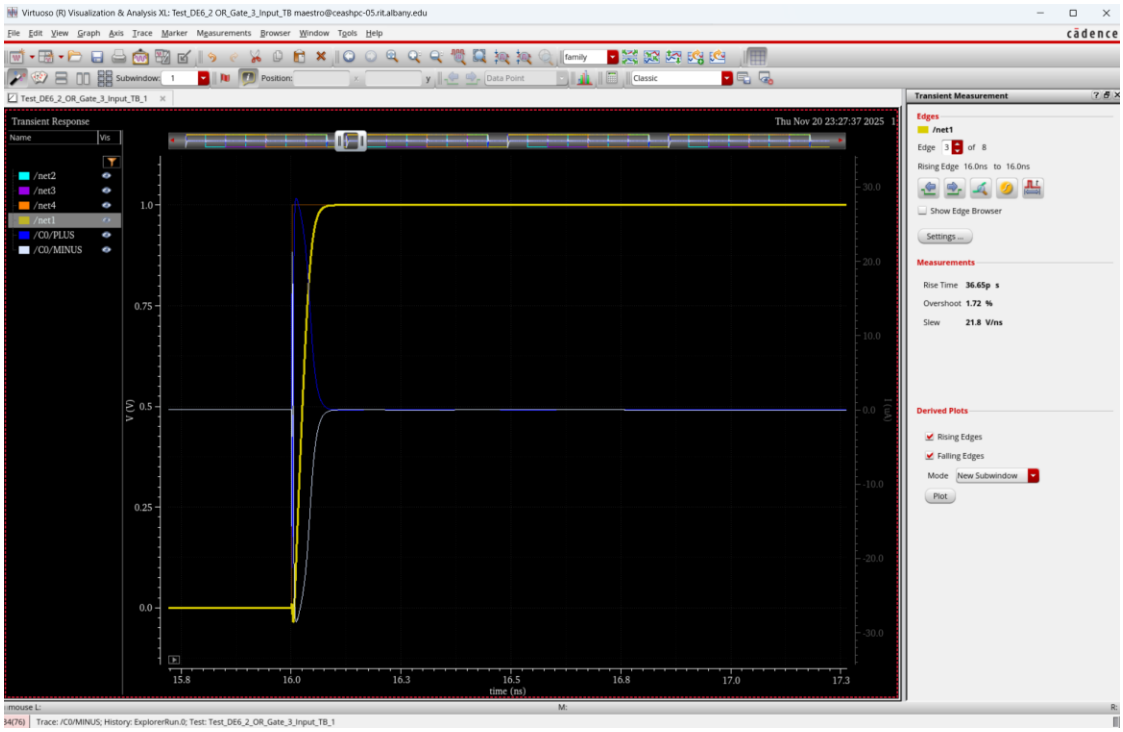

Fig: Simulation showing Rise time: 36.59p s and source current of 28.51uA

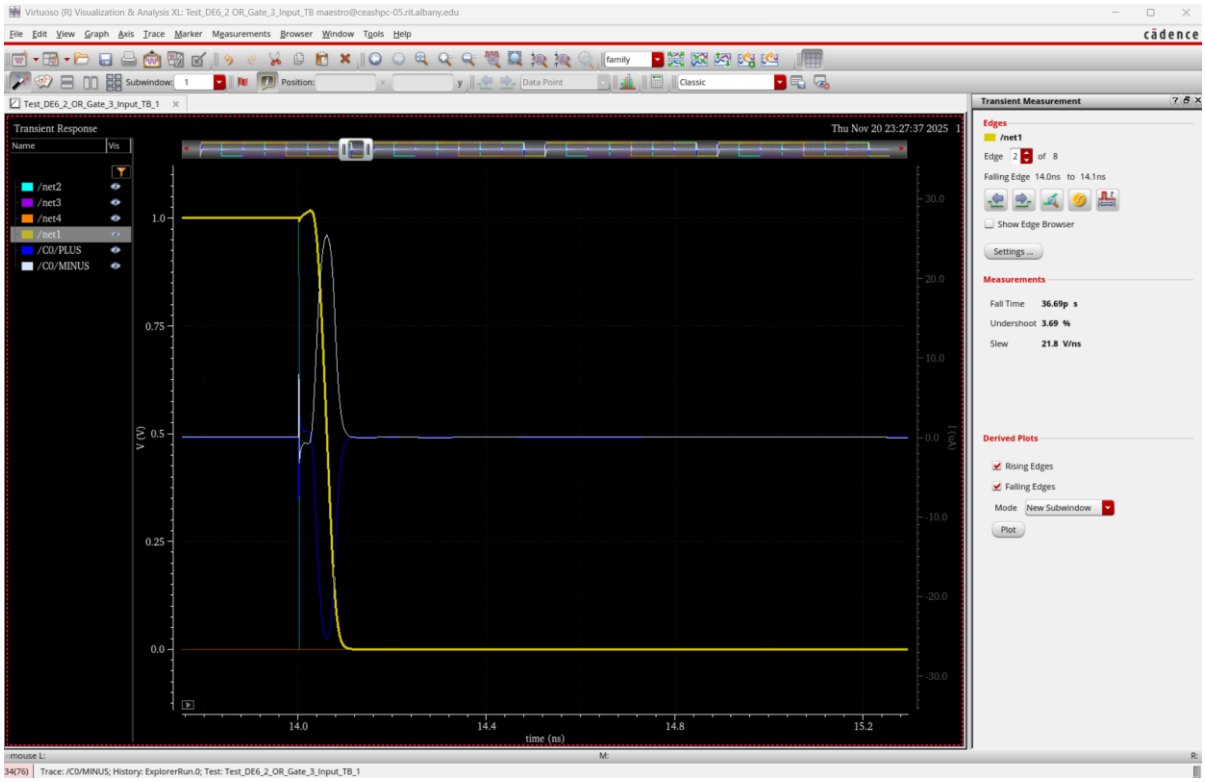

Fig: Simulation showing Fall Time of 36.69p s and sink current of 25.40uA

Layout:

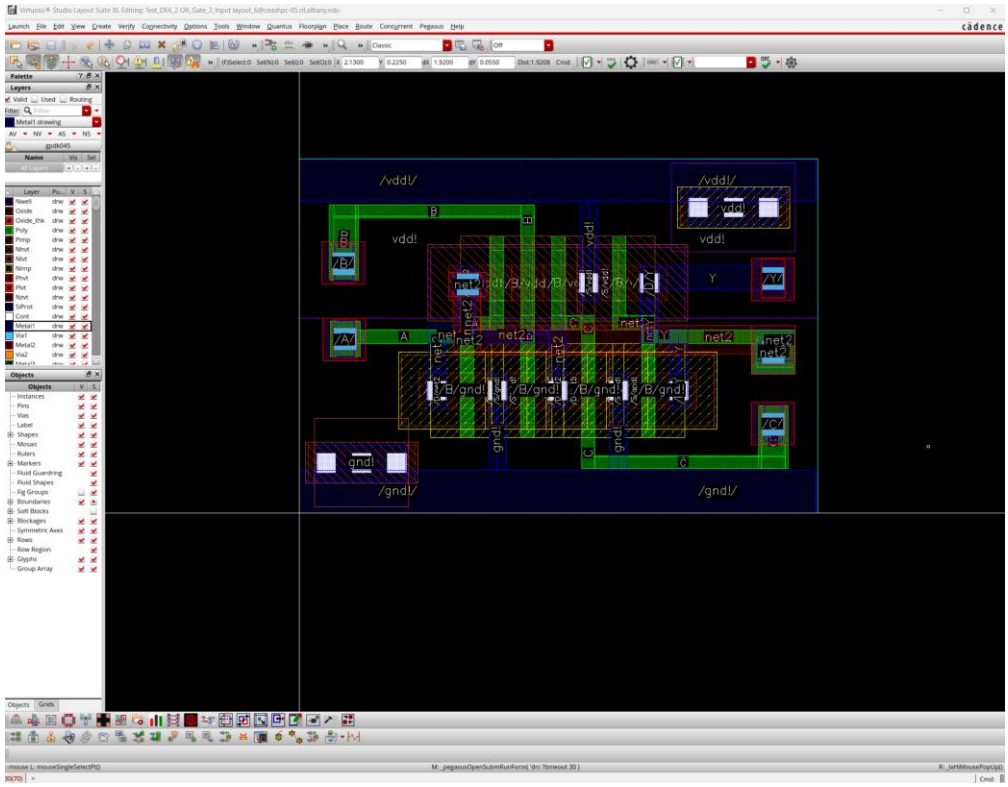

Fig: Layout

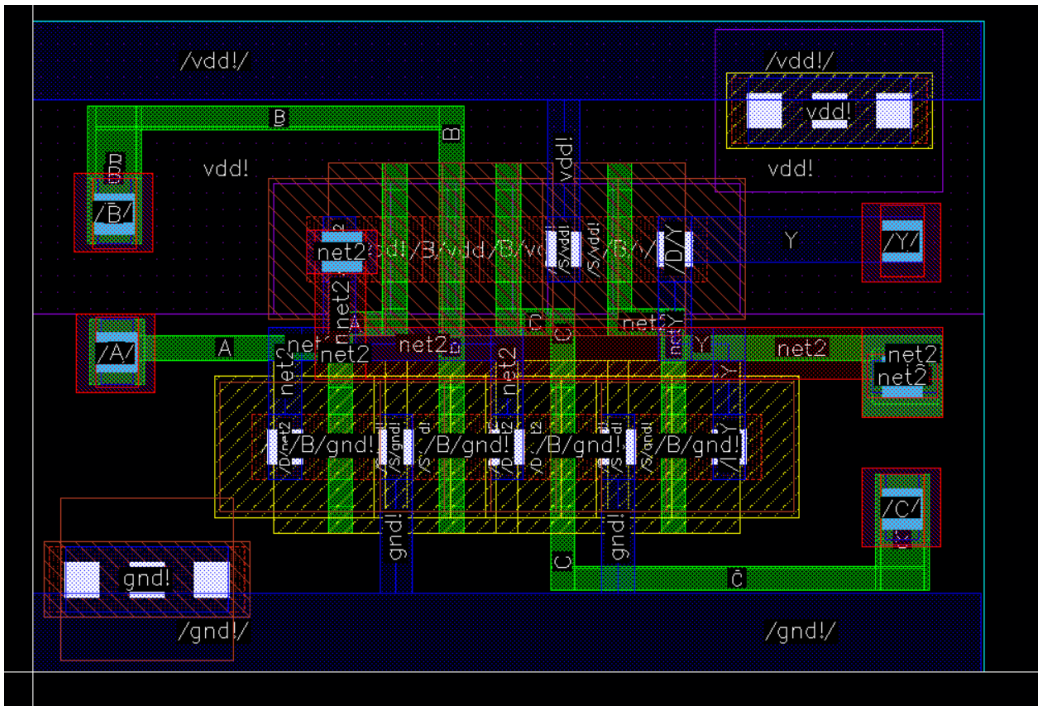

Fig: Layout in detail

DRC Results:

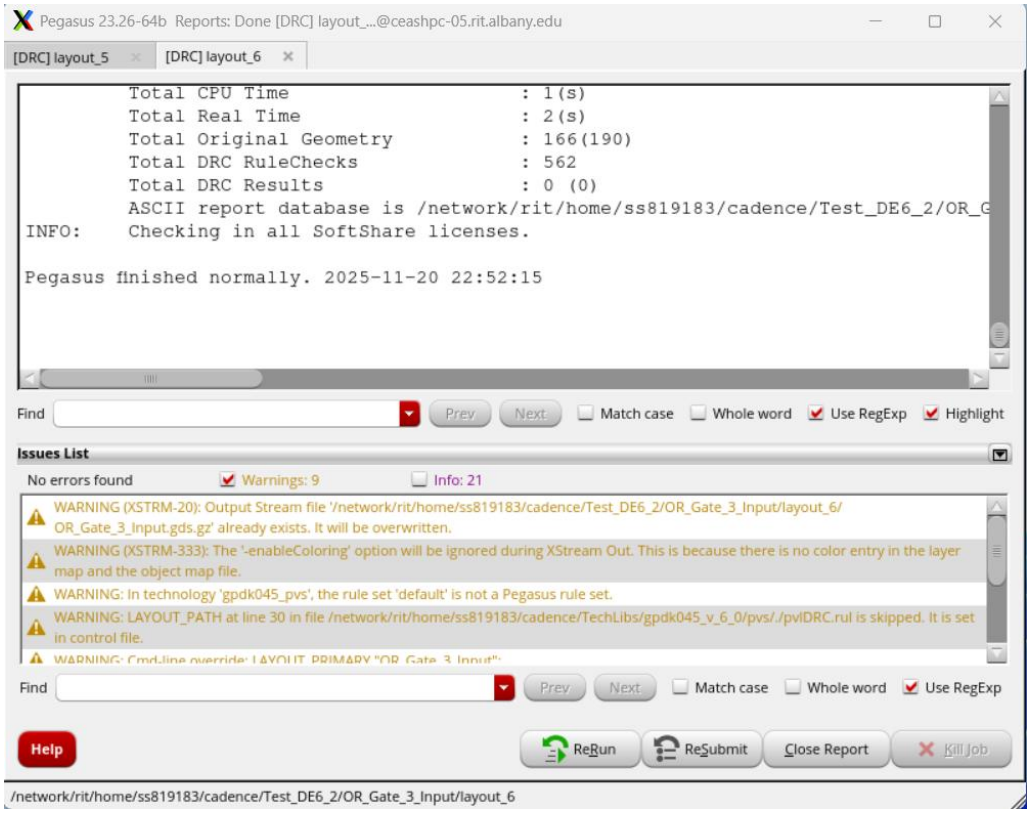

Fig: DRC running

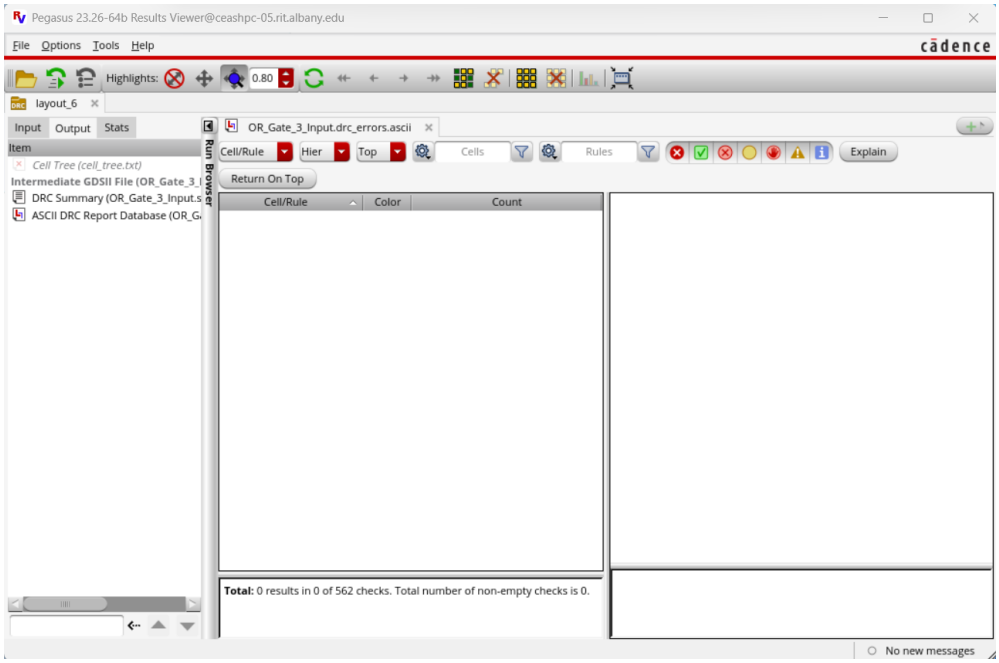

Fig: DRC Result showing absence of error

The above DRC check shows no errors, indicating that the Layout was created successfully.

Conclusion:

The testbench simulation shows a rise time of 36.59 ps with a source current of 28.51 μA, and a fall time of 36.69 ps with a sink current of 25.40 μA. These values fall within the acceptable range specified in the problem statement. Furthermore, the absence of DRC errors confirms that the layout of the three-input OR gate has been successfully completed.

Works Cited

Moulic, James R. Class Notes. PDF and videos.