Sigma Delta Analog to Digital Converter: Design and Implementation with reduction in Power Consumption

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***Abstract*— Data converters play an instrumental part in all communication systems. The numerous benefits of digital signal over analog signals have necessitated the use of analog to digital(A/D) converters in the transmitter side and of digital to analog(D/A) converters in the receiver side of the communication system. The steady developments in VLSI and signal processing domain have made Sigma-Delta(ΣΔ) A/D Converter an absolute choice for data conversion due to its architectural efficiency and easy implementation. The reduced requirement of chip area, reduced power consumption and improved frequency response without affecting the compatibility and design cost have made these converters the preferred choice. But like all other systems, Sigma Delta converters are not perfect. They have their own drawbacks which need to be reduced or removed to be at par for the efficient designing of the communication system. The decimation filter being a crucial block in a ΣΔ A/D Converter, the demands for efficient design are met by improving its design. The paper highlights the benefits of ΣΔ A/D Converter over other converter technologies and some Decimation filter design architectures. A ΣΔ A/D Converter for audio bandwidth application has been designed. The designing has been done using Matlab Simulink DSP Toolbox.**

Keywords—analog to digital converter; decimation filtering; modulator; oversampling; sigma delta;

I. INTRODUCTION

Data converters are the passage between two worlds- analog and digital. The ease of data processing in digital domain due to the varied benefits like reduced power requirements, lesser space for storage of signal data and so on necessitates the real world analog signal to be converted into its equivalent digital form. Thus A/D converters have a significant importance in the design of a sensor network. In a conventional analog to digital converter, the analog signal read from the sensor is sampled, quantized and encoded to give an equivalent digital signal. For proper reconstruction of the analog signal from the obtained digital signal, the analog signal must be sampled at a rate equal to or greater than twice the bandwidth of the input analog signal, failing which would give rise to the problem of aliasing. Depending on the varying coding schemes, large variety of A/D converters have evolved over the years. The ΣΔ analog to digital converters are the data converters that work on the principle of oversampling. Oversampling means sampling the signal at rates which are much higher than twice the sampling rate aka the Nyquist rate. The ΣΔ A/D converter is implemented using a ΣΔ modulator in conjunction with the digital decimation filter. The input analog signal is given to the modulator. In modulator, the difference between input signal and error signal is integrated and is compared to zero in the comparator. The difference that falls within the signal band are passed through the filter. The difference beyond this limit is suppressed by the filter. The digital bit stream coming out of the modulator is at much higher rate than that required by our application. Thus a decimation filter is applied to bring down the data rate to the required rate of the system for which the converter is used.

II. SIGMA DELTA ADC

A/D converters are broadly classified into two categories, namely- Nyquist converters and oversampling converters. This classification is based on the rate at which the incoming analog signal is sampled. The A/D converters that sample the analog input at the Nyquist frequency, which is twice the bandwidth of input signal are Nyquist rate A/D converters, depicted in equation (1).

$$f_s = f_n = 2 \times f_b \quad (1)$$

where f_s is the frequency at which the input signal is sampled, f_n is the Nyquist frequency and f_b is the bandwidth.
Oversampling A/D converters, as the name suggests, sample the analog input at a much higher rate than the Nyquist rate. This rate is higher, usually, by the factor between 8 and 512. ΣΔ A/D converters are included in this category. Thus, the name oversampled A/D converter has been justly given. In a sigma-delta A/D converter, the input signal is sampled at an oversampling frequency $f_s = K \times f_n$. Here, K is called the oversampling ratio(OSR) and its value is given as in equation (2)

$$K = f_s / 2f_b \quad (2)$$

The architecture of ΣΔ Analog-Digital Converter is shown in fig 1.

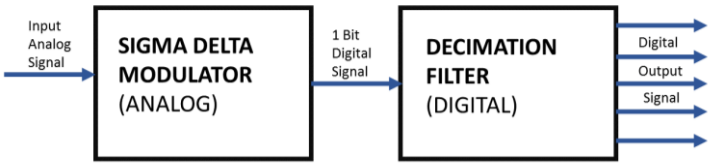

Fig 1. Sigma Delta ADC

A. Oversampling

A digital signal can only take on finite discrete values. The difference between the analog signal and its digital representation is known as quantization noise. Quantization noise causes distortion in the signal. The Nyquist theorem states that a signal, to be properly reconstructed without distortion, needs to be sampled at a rate at least twice the bandwidth of the input signal. Oversampling is beneficial in a way that it greatly reduces the quantization noise in the required band. When the incoming signal is oversampled by oversampling ratio K, the quantization noise power which was in the Nyquist bandwidth (fs/2) spreads over the wider bandwidth, Kfs/2. The total quantization noise is still the same but spreads over a larger bandwidth. Thus, the quantization noise in the bandwidth of interest gets reduced. Oversampling does not reduce the quantization noise. It only redistributes the noise over a larger band. Thus, the total quantization noise in our band of interest is significantly reduced. This is depicted in the fig 2(a) and fig. 2(b).

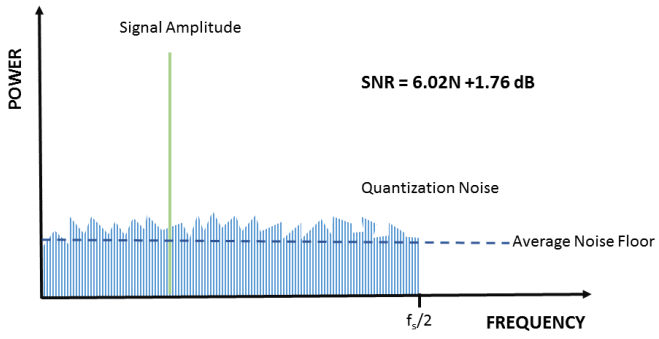

Fig. 2(a) Signal and Noise density for Nyquist ADC

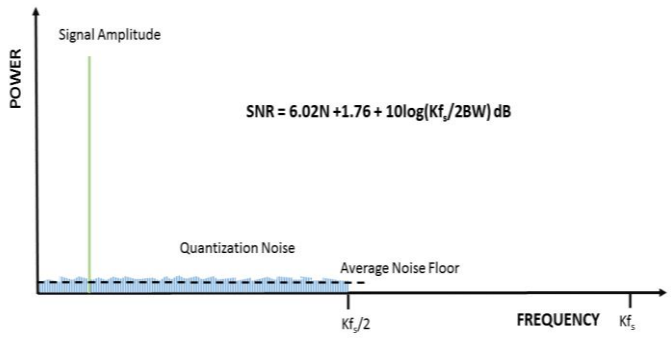

Fig. 2(b) Signal and Noise density for Oversampled ADC

To prevent aliasing, the input signal must be band limited. For this purpose, an anti- aliasing filter is used before the converter. The filtered signal should not contain frequency components above the frequency fs/2. To ensure this, the filter should have a very narrow transition band. Realizing a filter with stringent band requirements is complex and expensive task.

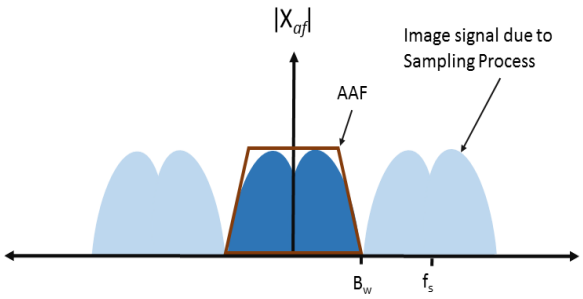

Fig.3(a). Anti aliasing Filter for Nyquist A/D converter

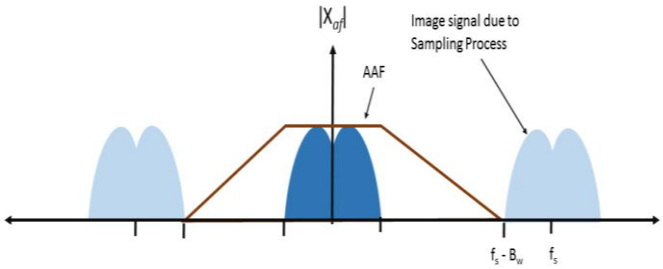

Fig.3(b). Anti aliasing Filter for Oversampled A/D converter

Another drawback of Nyquist rate converters is its low resolution which renders its uselessness for conversion of very low voltage signals. Oversampled A/D converters have the benefit of high signal to noise ratio and high resolution making them a preferred choice, over Nyquist A/D converters, for low voltage applications.

B. Noise Shaping

When analog signal is converted into digital representation, quantization noise is introduced in the signal. For all practical purpose, the maximum value of this noise is ±LSB/2. Higher resolution of A/D converter implies that the LSB is lower. Thus, we can say higher resolution means a lower quantization noise. To understand the effect of resolution on the Signal to Noise ratio (SNR) let us have a look at the equation (3)

$$SNR = 6.02N + 1.76 \text{ dB} \quad (3)$$

where, N is the effective number of bits. Thereupon we can imply that as the resolution increases, the signal to noise ratio also increases.

The ΣΔ modulator behaves as a low pass filter for the signal and as high pass filter for quantization noise thereby pushing the noise to higher frequency range. This phenomenon is called noise shaping. The decimation filter applied at the output of the modulator attenuates this high frequency noise.

The SNR due to oversampling is measured as mentioned in equation (4),

$$SNR = 6.02N + 1.76 + 10\log(Kf_s/2f_b)\ dB \quad (4)$$

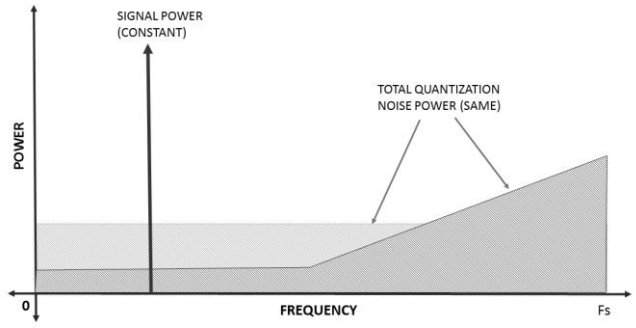

Fig. 4. Noise Shaping

III. DESIGN

A. Modulator

The ΣΔ modulator structure is depicted in the fig. 5. The modulator shown is a second order modulator.

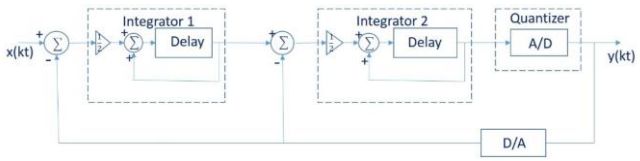

Fig. 5. Second Order Modulator

The input is an analog signal x(t). It is sampled at frequency f_s. The digital filter attenuates the quantization noise present in desired band from the modulator. The decimation filter brings down the sampling rate to the Nyquist rate. The noise power at the filter output, S, is the total of in-band quantization noise, thermal noise and the noise due to clock jitter. The expression for quantization noise is given as in equation (5)

$$S = \frac{\pi^4}{5}\frac{1}{K^5}\frac{\Delta^2}{12} \quad (5)$$

One important method of reducing the noise in the signal is by increasing the sampling rate. The greater the number of samples of input we take, closer is our digital representation to the original waveform. But the clock rate cannot be increased indefinitely. A better way to minimize noise is by using high order modulators. With the use of higher order modulator, effective number of bits also increases. For a second order modulator, a reduction of 15dB in quantization noise is obtained for every octave of oversampling. A second order modulator can achieve 19 bits as against the first order modulator which can obtain only 13 bits.

B. Digital Decimation Filter

The bit stream coming out of the Delta Sigma Modulator is given to the Digital Decimation filter. The digital decimation filter averages and down samples the incoming bit stream thus producing the n-bit sample as desired by our system. The averaging has a similar effect as low pass filtering in frequency domain. The quantization noise is attenuated and the aliases are removed from the band of interest. This decimation filter has a sharp roll-off near the cut off frequency and excellent rejection in the stopband. This makes it very effective in anti-aliasing. Decimation filter is implemented as an FIR Comb filter.

The Cascaded Integrator Comb (CIC) filter consists of 1-bit integrators and 1-bit differentiators. It can handle large frequency changes and is multiplier free filter. Due to its symmetric design, it can be efficiently implemented in a hardware. Its transfer function in Z-domain is given as

$$H(z) = \left(\frac{1-z^{-k}}{1-z^{-1}}\right)^N \quad (6)$$

where, K is the OSR and N is the filter order. The averaging is performed followed by decimation operation. The block diagram of a first order filter is as in fig.6(a)

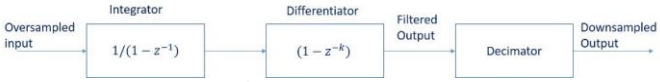

Fig. 6(a). Digital filter with decimator as last stage

The number or delay units in the differentiator circuit is equal to the oversampling ratio. These delay units are implemented using nothing but registers. This leads to dependency of the number of delay elements on the number of register bits used to store the data. As the order increases, the circuit complexity increases with higher sampling ratio. By inserting a decimator between the integrator and differentiator, this issue can be solved. This is depicted in the fig.6(b)

Fig. 6(b). Digital filter with decimator as middle stage

The integrator is made to operate at frequency fs, the sampling frequency. The differentiator operates on a much lower frequency. Its operational frequency is sampling frequency factored by the oversampling ratio i.e. fs/K. This enables us to achieve a reduced power consumption.

IV. RESULTS

The ΣΔ A/D converter has been designed and its performance parameters measured. Fig.7 shows the implementation results of a ΣΔ A/D converter using FIR low pass filter with a single stage filter as well as filters in cascade respectively. The benefit of using cascaded filters is reduction in hardware requirements and is depicted in table 1. Further improvement in effi-

ciency is obtained by using Look up Tables as depicted in fig.8(a) and fig 8(b).

TABLE I: Performance parameters of single stage and multi-stage filter

Decimation Factor	64	8	2	4
Passband edge	21.6KHz	0.014063	0.1125	0.225
Stopband Edge	26.4KHz	0.23281	0.8625	0.275
Number of Multipliers	2968	40	12	194
Number of adders	2967	39	11	193
Multiplication per Input Sample	46.375	5	6	48.5
Addition per input samples	46.3594	4.875	5.5	48.25

As depicted in the results, a single stage filter requires 5935 arithmetic units whereas, the multistage filter requires a total of 489 units. There is a lumpsum 92% reduction in the hardware requirement. The number of arithmetic operations to be performed is slightly increased, thereby reducing the speed of operation, though, there has been no significant reduction in speed observed. The target of reducing the power consumption of the circuit without affecting its overall performance has been achieved.

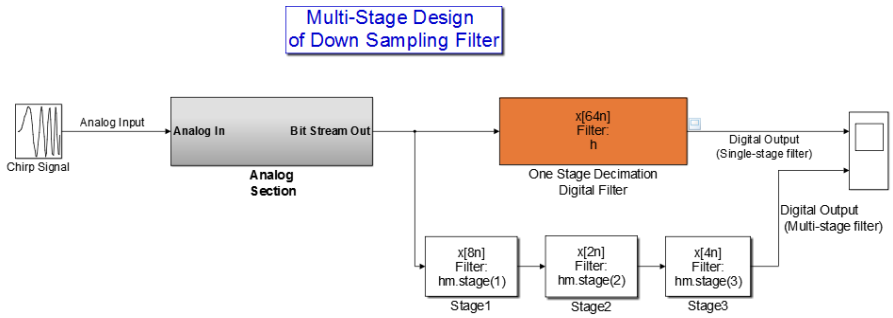

Fig.7(a) Sigma delta A/D CONVERTER using single stage and multistage filters

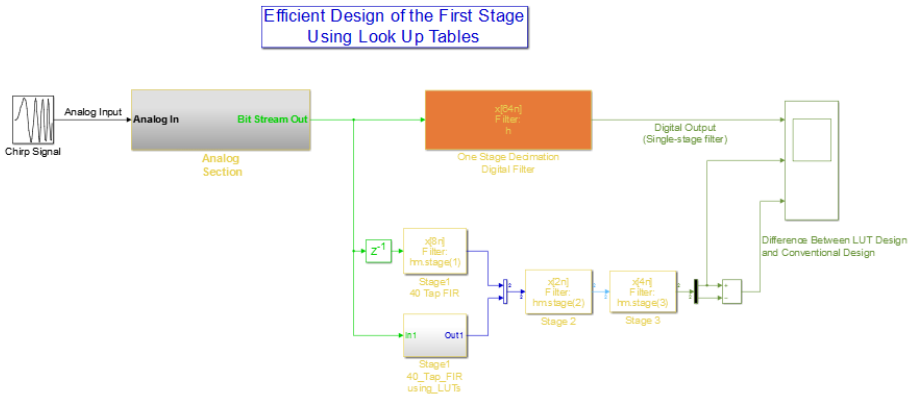

Fig.8(a) Sigma delta A/D CONVERTER using single stage and multistage filters with a LUT

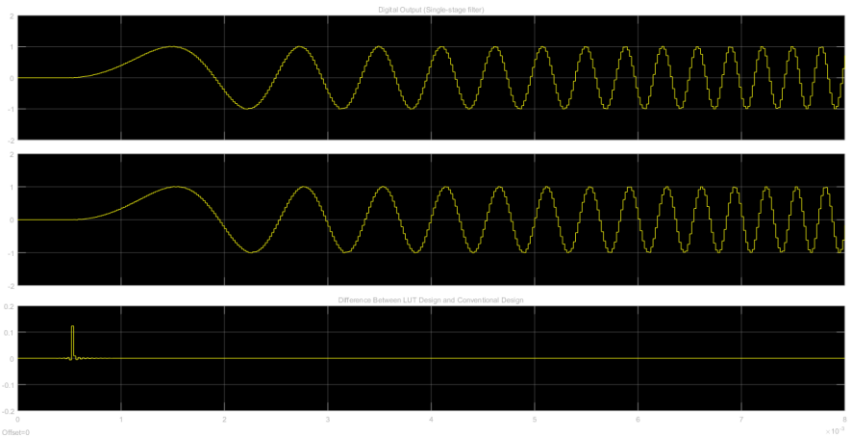

Fig.8(b) . Output of Sigma Delta A/D converter with and without LUT

V. CONCLUSION

A ΣΔ A/D converter using a second order modulator and a CIC filter has been designed. It has been observed that by increasing the modulator order, there is an effective increase in the SNR. But the order cannot be indefinitely increased because it causes instability in the system. Second order ΣΔ modulators have been observed to be an efficient architecture for high resolution converters. By using cascaded filters, the hardware requirements have been observed to have significantly reduced. The power consumption of the circuit has also decreased to 1.6mW. This is very low compared to current converters. One important observation to make is the reduction in the operations performed. Thus, the overall speed of the system is increased.

REFERENCES

[1] José M. de la Rosa, "Sigma-Delta Modulators: Tutorial Overview, Design Guide, and State-of-the-Art Survey", IEEE transactions on circuits and systems—I: regular papers, Vol. 58, No. 1, January 2011

[2] S. Brigati, SD Toolbox, 2016 [Online]. Available: http://www.mathworks.com/matlabcentral/fileexchange/2460

[3] Mohammed Arifuddin Sohel, Dr. K. Chennakeshava Reddy and Dr. Syed Abdul Sattar, "A 12 Bit Third Order Continuous Time Low Pass Sigma Delta Modulator for Audio Applications", International Journal of Electronics and Communication Technology (IJECT), vol. II, Issue 4, page(s): 211-216, October 2011.

[4] R. Schreier, in The Delta-Sigma Toolbox v. 7.3, 2009 [Online]. Available: http://www.mathworks.com/matlabcentral/fileexchange/19

[5] R. Winotoand B. Nikolic, "A highly reconfigurable 400–1700 MHz receiver using a down-converting sigma-delta A/D with 59-dB SNR and 57-dB SFDR over 4-MHz bandwidth," in Proc. IEEE Symp. VLSI Circuits, 2009, pp. 142–143.

[6] Libin Yao, Michiel S. J. Steyaertand Willy Sansen,"A 1-V 140-W 88-dB Audio Sigma-Delta Modulator in 90-nm CMOS", IEEE journal of solid-state circuits, Vol. 39, No. 11, November 2014

[7] M.Keskin, U. Moon, and G. C. Temes, "A1-V 10-MHz clock-rate 13-bit CMOS Delta sigma modulator using unity-gain-reset opamps," IEEE J. Solid-State Circuits, vol. 38, pp. 817–824, July 2012.

[8] M. Dessoukyand A. Kaiser, "Very low-voltage digital-audiomodulatorwith 88-dB dynamic range using local switch-bootstrapping," IEEE J. Solid-State Circuits, vol. 36, pp. 349–355, Mar. 2001.

[9] V. Peluso, P. Vancorenland, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 900-mV low-power A/D converter with 77-dB dynamic range," IEEE J. Solid-State Circuits, vol. 33, pp. 1887–1897, Dec. 1998.

[10] R. Schreierand G. C. Temes, Understanding Delta-Sigma Data Converters, New York: IEEE Press, 2005.

[11] Bernhard Boser, Bruce Wooley, "The design of Sigma Delta Modulation Analog-to-Digital Converters", IEEE Journal of Solid State Circuits,VOl. 23, No. 6, December 1988

[12] J. Sauerbrey, T. Tille, D. Schmitt-Landsiedel, and R. Thewes, "A 0.7-V MOSFET-only switched-opamp Delta sigma modulator in standard digital CMOS technology," IEEE J. Solid-State Circuits, vol. 37, pp. 1662–1669, Dec. 2012