ECE/CS 5780/6780

Spring 2017

FINITE STATE MACHINE DESIGN EXERCISE SESSION

MONITORING SYSTEM FOR WATER FLOW THROUGH PIPE: Water flow through pipe should maintain a steady velocity above or around a standard value for seamless usage at homes and other commercial places. With long complex structures of piping systems used in commercial usage, there are chances that defects start to arise resulting in an unusable water flow.

In these exercises, we are going to design a *monitoring system* for water flow through pipe. When this system detects a problem it will assert a warning signal to the maintenance team to check the pipe. Signal from a Water Flow Probe will be used by the system to monitor the water velocity in pipe against a minimum and maximum threshold value.

EXERCISE-1:

Assume the following:

1. There is an analog-to-digital converter (ADC) that converts the velocity value from water flow probe to an 8-bit number, **data**
2. The ADC is started by a high pulse on the **adcStart** signal.
3. The ADC indicates completion by a rising edge on the **adcDone** signal.
4. An issue in the pipe is assumed when **100 consecutive violations are detected**.
5. Once the issue is confirmed, a **warning** is indicated by setting an I/O port pin high.

Preamble question: What is the type of each signal?

State Machine Modeling: Draw an extended state machine diagram for the monitoring system. You may add any other variables that you need. For simplicity, you can assume that the ADC delay and software delays are negligible compared with the waiting time between readings.

Additional questions:

When does a reaction occur in your model?

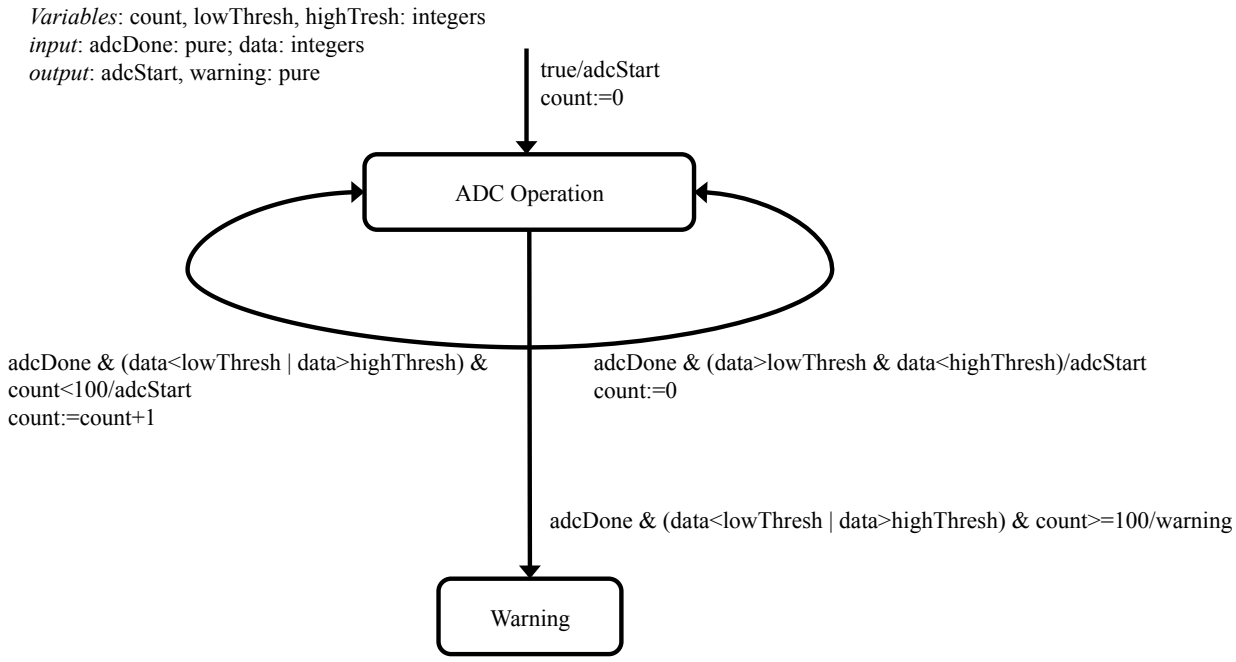
What is the associated model type?

How to reinitialize the system?

SOLUTION FOR EXERCISE-1 (Event-triggered model):

Preamble: data = integer variable; adcStart, adcDone and warning = pure signals

FSM:



Additional Questions:

Reaction: Every time one of the pure inputs becomes present.

Model type: Event-triggered FSM

Initialization: Needs a physical reboot of the system

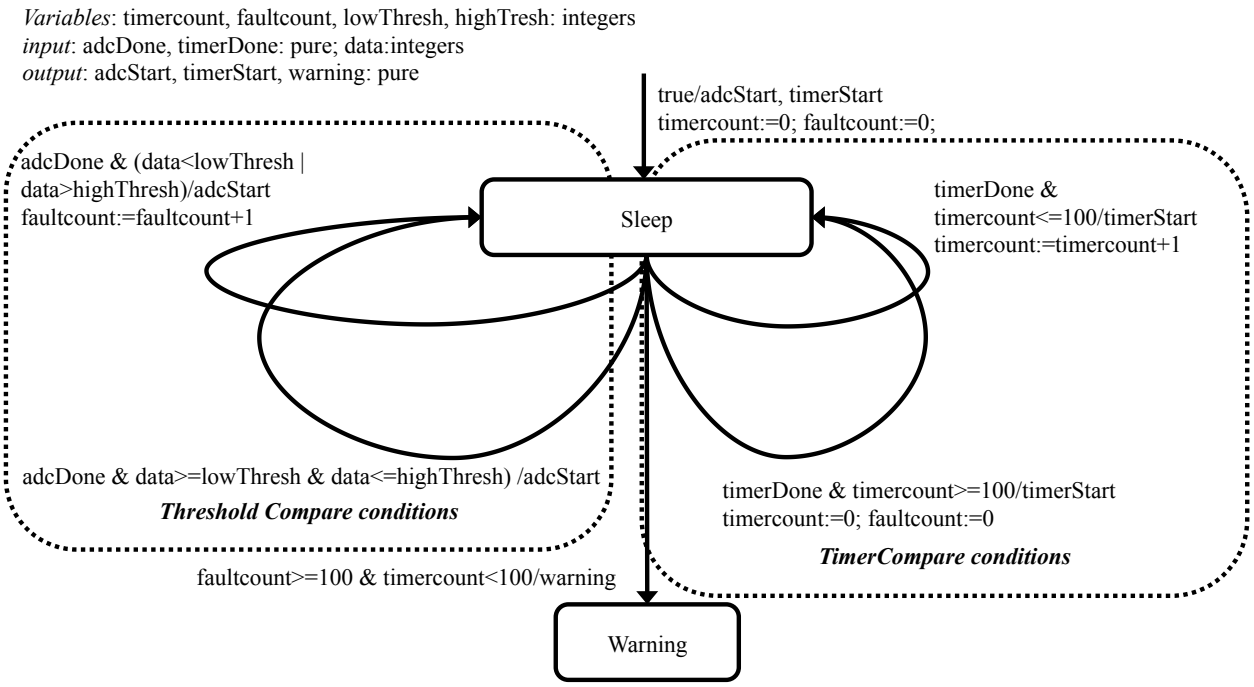
EXERCISE-2:

Assume the following:

1. There is an analog-to-digital converter (ADC) that converts the velocity value from water flow probe to an 8-bit number, **data.**
2. The ADC is started by a high pulse on the **adcStart** signal.
3. The ADC indicates completion by a rising edge on the **adcDone** signal.
4. An issue in the pipe is assumed when **100 violations are detected during a sensing period of 10 seconds of time**. We assume that a new sensing period starts every 10 seconds. At the beginning of a period start, the current violation count is reset.
5. Use a timer for monitoring the time. The timer is started by a high pulse on the **timerStart** signal.
6. The timer waits for **100ms** before asserting **timerDone** signal.
7. Once the issue is confirmed, a **warning** is indicated by setting an I/O port pin high.

State Machine Modeling: Draw an event-triggered extended state machine diagram for the monitoring system. For simplicity, you can assume that the ADC delay and software delays are negligible compared with the waiting time between readings.

SOLUTION FOR EXERCISE-2 (Event-triggered model):



How many samples of the ADC do you get? – As many as possible depending on the speed of the ADC

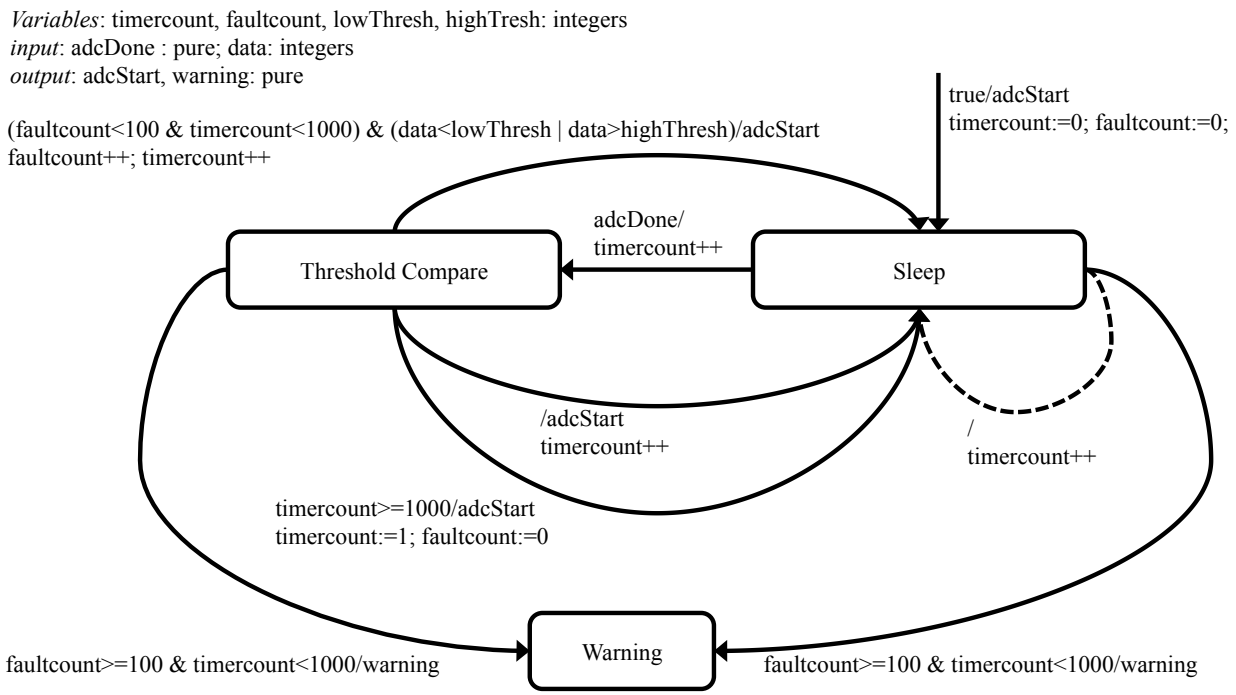
EXERCISE-3:

Assume the following:

1. There is an analog-to-digital converter (ADC) that converts the velocity value from water flow probe to an 8-bit number, **data.**
2. The ADC is started by a high pulse on the **adcStart** signal.
3. The ADC indicates completion by a rising edge on the **adcDone** signal.
4. An issue in the pipe is assumed when **100 violations are detected during a sensing period of 10 seconds of time**. We assume that a new sensing period starts every 10 seconds. At the beginning of a period start, the current violation count is reset.
5. Use a system/external clock to monitor the time. Assume clock period of 10ms.

State Machine Modeling: Draw an extended state machine diagram for the monitoring system. For simplicity, you can assume that the ADC delay and software delays are negligible compared with the waiting time between readings.

SOLUTION FOR EXERCISE-3 (Time triggered model):



How many samples? – 500.