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-Why can't both pins PA0 and PC0 be used for external interrupts at the same time?

PA0, PB0 ... PF0 are grouped on a single multiplexer with the output routed to the EXTI0 input. Because only a single pin from a group can be used, pins need to be chosen such that they do not conflict with each other when using multiple external interrupts.

-What software priority level gives the highest priority, what level gives the lowest?

0 gives the highest priority, and 3 gives the lowest for the NVIC. -14 to is the highest, while 31 is the lowest in the hardware priorities.

-How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt? (including non-implemented bits)

Four 8-bit regions.

-Which bits in the group are implemented?

The uppermost two bits from the regions mentioned in previous question.

-What was the latency between pushing the Discovery board button and the LED change (interrupt handler start) that you measured with the logic analyzer?

0.504ms

-Why do you need to clear status flag bits in peripherals when servicing their interrupts?

The interrupt will continuously repeat because the request is never acknowledged as completed.