UNIVERSITY OF UTAH
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
ECE 2280

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3/2014

Lab #4 {100 pts} MOSFET TRANSISTORS

OBJECTIVES

- To bias a NMOS transistor.
- To use a NMOS transistor in a common-source amplifier configuration and to measure its amplification.
- To study the effect of the source resistor and bypass capacitor on the amplification.
- To study the effect of a load resistor on the amplification.

Parts List:

☐ CD4007 MOS transistor array OR {any p-type and n-type enhancement single transistors}
☐ 1 - 33 nF capacitor
☐ 1 - 0.1 microFarad capacitor
☐ 1 microFarad capacitor
☐ 10 kOhm resistor
☐ 50 kOhm resistor
☐ 2 - resistors: TBD
☐ 1 - 100 kOhm potentiometer

Background

A MOSFET can be used as a basic common-source amplifier which is similar to the BJT common-emitter amplifier. The key to amplification is a good bias for the transistor.

Biasing:

Similar to the BJT biasing configurations, a resistor divider at the gate and a source resistance provide the best configuration to give stability and also have the bias current insensitive to temperature variations and transistor characteristics. Note that the same biasing configurations as there were for BJT transistors exist for the MOSFET transistor. A resistor divider biasing configuration is shown in Figure 1.

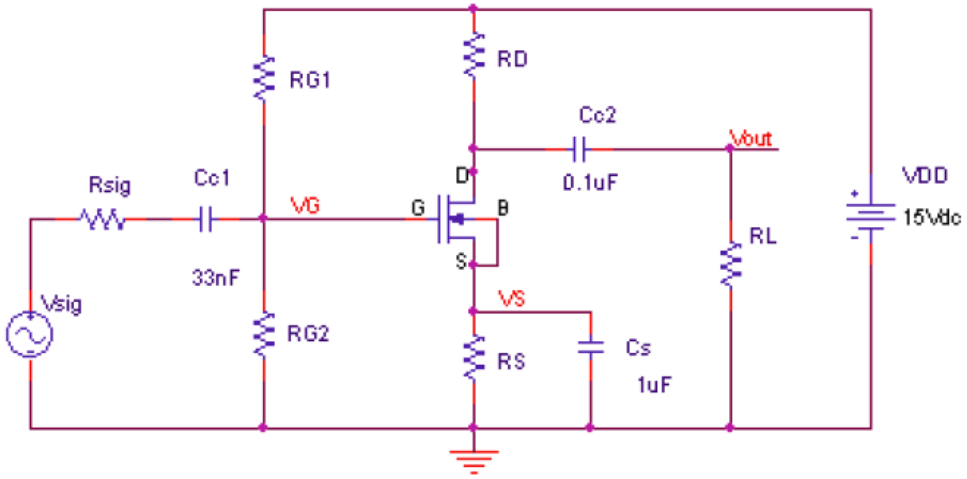

Figure 1. Common source amplifier with a voltage divider at the gate and source resistance. Note that the body of the transistor is tied to the source to eliminate the "body effect" which can raise the threshold voltage of the transistor. Also note that the input signal, Vsig, is coupled to at the gate through the coupling capacitor Cc1.

Biasing: Rule of Thumb

1. 1/3 to 1/5 of power supply VDD is placed between VS and ground. Choose RS to achieve this voltage.
2. RD is chosen such that VD=(VDD-VS)/2.
3. Find VG from

$I_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(V_{GS}-V_t)^2$ when $V_{DS} > (V_{GS}-V_t)$

knowing the current I_D and the other process parameters and VS. Once VG is determined, find R_{G1} and R_{G2}. Note that these resistors also determine the input resistance and so should be relatively large.

Amplification

Assuming that the capacitors act as a short, the small signal equivalent circuit can be drawn:

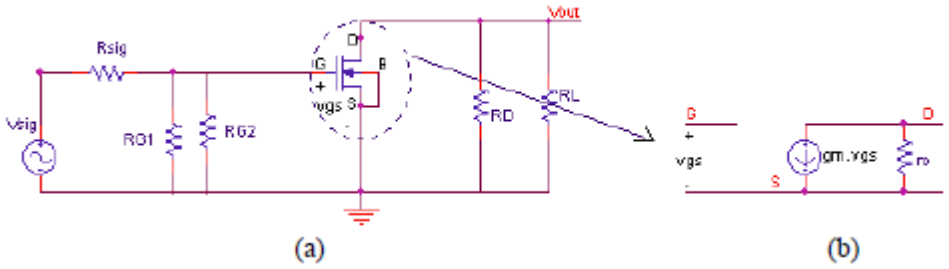

Figure 2. (a) AC circuit, (b) hybrid$-\pi$ equivalent model.

The *transconductance* parameter, g_m, is a key parameter in determining the AC gain. It is found by

$$g_m = \sqrt{2I_D k_n'\left(\frac{W}{L}\right)} = \frac{2I_D}{V_{GS}-V_t}$$

Similar to the BJT transistor, the AC parameter depends on the DC bias current I_D. The other AC parameter is due to the early effect and is defined as

$$r_o = \frac{V_A}{I_D} = \frac{1}{\lambda I_D}$$

Determining the overall gain V_o/V_{sig} can be done by writing an equation for Vo and then v_{gs} (note that this is NOT the same as the DC value for V_{GS}since we are looking now at the AC amplification).

$$V_O = -g_m v_{gs}(RD||RL||r_o)$$
$$v_{gs} = V_{sig}(RG1||RG2)/(R_{sig} + (RG1||RG2))$$
$$V_o/V_{sig} = -g_m(RD||RL)(RG1||RG2)/(R_{sig} + (RG1||RG2))$$

Experiment 1: Design and Simulation (50 point)

1. (10 pts) Design the circuit in Figure 1 for the following:
   - $I_D = 0.6mA$
   - VS=3V
   - VD should be in the middle of VS and V_{DD}.
   - Rin>15k
   - Choose resistor values available in the lab.

   Note: (CD4007 array chip) - $V_t = 1.2V, k_n'\left(\frac{W}{L}\right) = 0.7mA/V^2, \lambda = 0.004V^{-1}$
2. (5 pts) Draw your design in PSpice and simulate it. Verify(print out your results and place in your notebook) that the above requirements in 1 are met. If not, modify your values to achieve the above requirements.

3. (5 pts) Use the hybrid-π model to calculate by hand the values for the gain, Rin, and Rout. Use $R_L = 10k$ and $R_{sig} = 50$.
4. (10 pts) Do an AC sweep in PSpice along with the other simulations to find the gain, Rin and Rout. Print these results and place them in your lab notebook. Note the location of the low-frequency cut-off value. Compare the simulation results with your hand calculations.
5. (5 pts) Remove R_L and perform another simulation to find the gain magnitude Bode plot. Comment on the results.
6. (15 pts) Perform a transient simulation using the frequency within the midband region and an amplitude of 0.2V. Run the simulation with the load resistor and then without the load resistor. Compare these values to the Bode plots from 4 and 5.

Experiment 2: Prototype (50 point)

Use the CD4007 MOSFET array if possible. Otherwise, a discrete transistor can be used. The CD4007 array contains three NMOS and three PMOS transistors as shown in Figure 3. Again, the key point to remember is that the bulk (or substrates) of all NMOS transistors are connected to the VSS (pin 7) and all PMOS substrates are connected to VDD (pin 14). When using this array pin 7 should be connected to the most negative supply voltage or to the source of the transistor. Pin 14 is the substrate of the PMOS and must be connected to the most positive supply voltage in the circuit!

It should be mentioned that the transistor characteristics of the CD4007 can vary considerably from chip to chip. The transistors may come from a different batch, which can explain why the threshold voltage, the transconductance parameter and the output resistance is different from the one used in the hand calculations and Spice simulation.

WARNING: MOSFET transistors are very susceptible to breakdown due to electrostatic discharge. It is recommended that you always ground yourself before picking up the MOSFET chip. Do no touch any of the pins of the chip!!

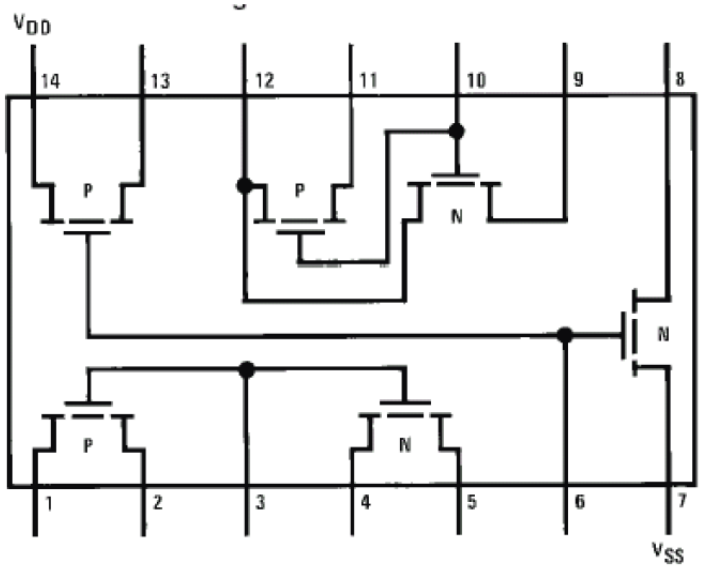

Figure 3. CD4007 pin diagram.

1. (10 pts) First build just the bias circuit(Fig. 4) for the amplifier you previously simulated. Use a potentiometer for RG2. Use the transistor between the pins 3, 4 and 5. Notice that the bulk (pin 7) is connected to the source (pin 4) of the NMOS transistor. Do this with a wire connecting pins 4 and 7 together. This can be done since we are only using a single NMOS transistor in the array. The reason for shorting

drain-to-bulk is to eliminate the body effect on the threshold voltage. For the biasing resistor RG2, use a100k potentiometer.

2. (5 pts) Measure the DC voltage at the drain. Adjust the potentiometer RG2 so that VD is around 9V. After adjusting the gate voltage, measure the gate and source voltages. What is the corresponding drain current ID?

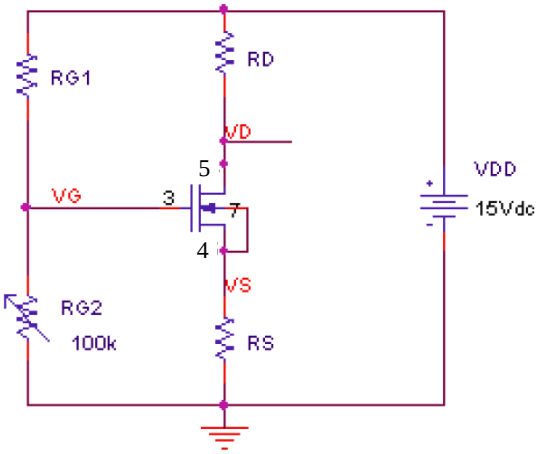

Figure 4. Biasing circuit for the common-source amplifier.

3. (10 pts) Modify the circuit of Figure 4 by adding the capacitors Cc1, and CS as shown in Figure 5. Connect a sinusoidal input signal of 0.2V amplitude (0.4Vpp) and 5kHz frequency. Measure the voltage swing at the drain using the oscilloscope. Display the VD on one channel and the input voltage Vsig on the other channel. Measure the peak to peak values of the input and output signal. What is the open-circuit amplification (voltage gain) Avo? Include this graph in your notebook. How does it compare to the calculated one? It should be mentioned that the transistor characteristics can vary considerably from chip to chip. It is not unusual the measured values differ by as much as 10-20% from the specified ones.

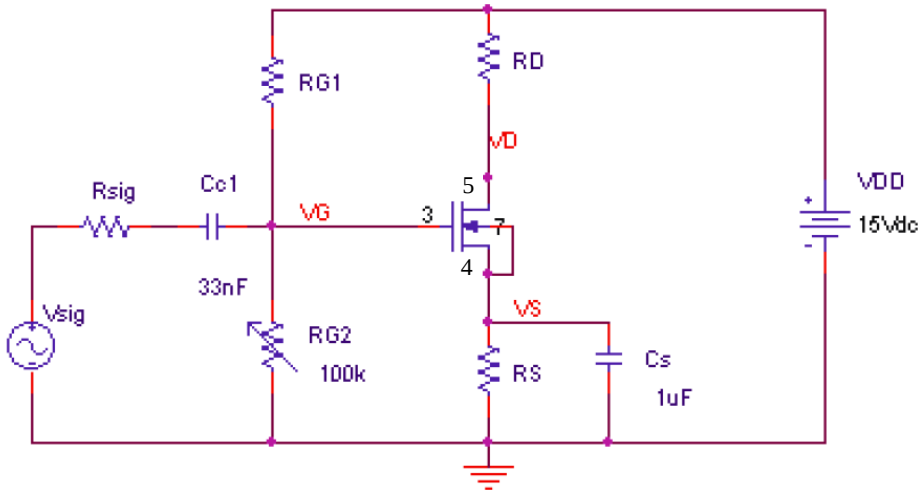

Figure 5. Common-source amplifier. Rsig is the internal resistance of the function generator and is negligible.

4. (5 pts) Increase the amplitude of the input signal from 0.2V and observe the output signal. When does the output signal start to distort? What is the maximum output voltage swing before considerable distortion occurs?

5. (10 pts) Reduce the input signal amplitude back to 0.2V. Add the coupling capacitor CC2 and the load resistor RL as shown in Figure 1. Use a Cc2 value of 0.1 uF and an RL value of 10k. Measure the output voltage Vo at VD and the corresponding amplification Av. Notice that the DC voltage has been removed from the output voltage. What happened to the amplification?

6. (10 pts) Measure the frequency response of the amplifier with the load resistor connected. Change the frequency of the input signal. Starting from 5 kHz, reduce the frequency till the amplitude of the output has decreased by a factor of 0.707 (or 3dB). Record this 3dB frequency. Next, increase the value of the input frequency till the amplification Av reduces to 0.707 of its value at 5kHz. Record the high-frequency 3dB point. What is the bandwidth of the amplifier? Compare these values to your simulation results.