Architecture Diagram

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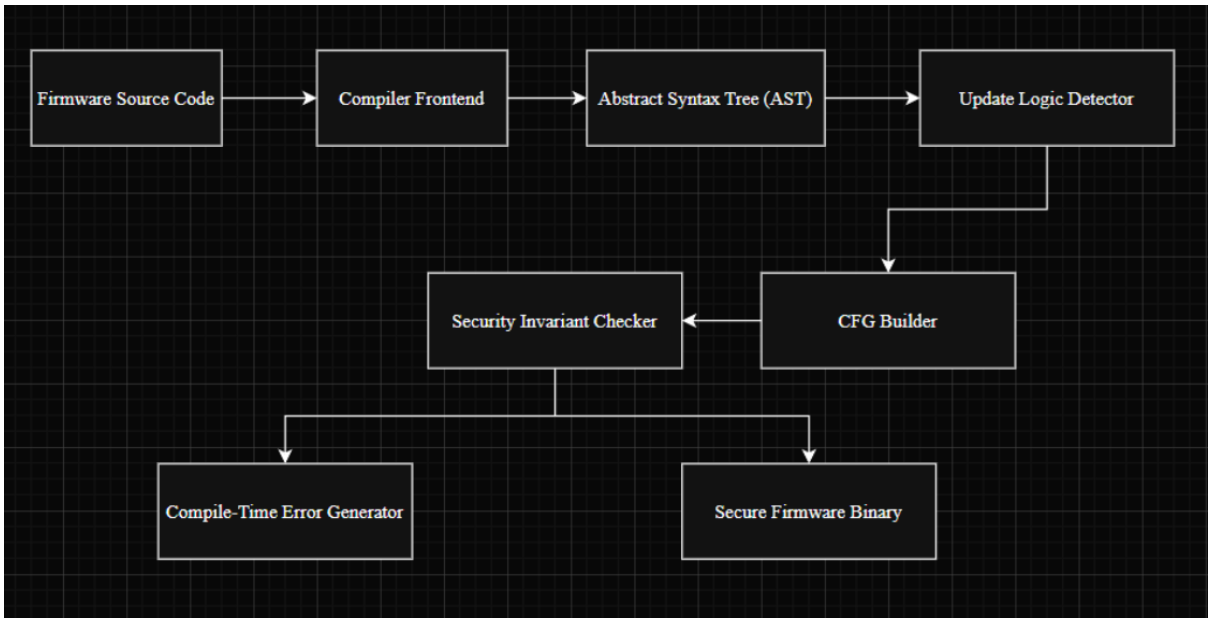
CSE - A
Q119 - Secure OTA Update Compiler

System Architecture

This diagram presents the high-level architecture of the Secure OTA Update Compiler and its integration into the firmware build pipeline.



Explanation

Firmware source code is processed by the compiler frontend to generate an AST. Update logic detection and CFG construction feed into the security invariant checker, which either produces compile-time errors or allows generation of a secure firmware binary.