

A

A

B

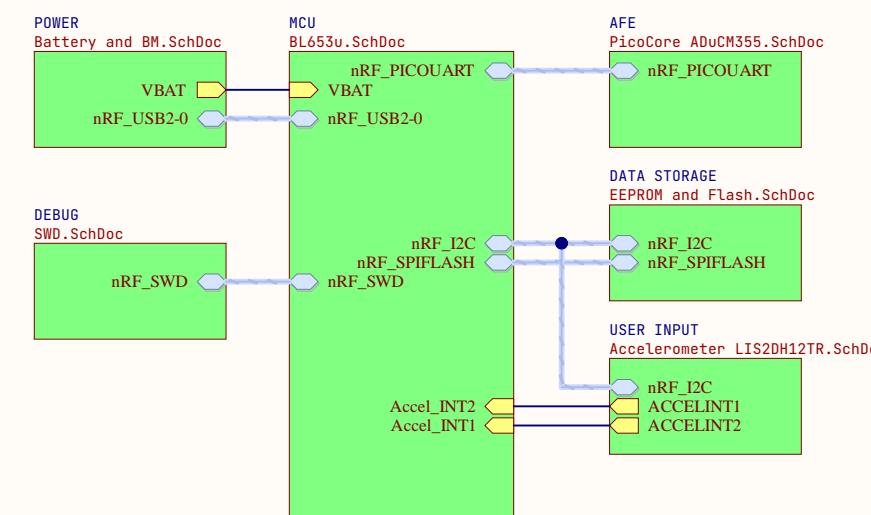
B

C

C

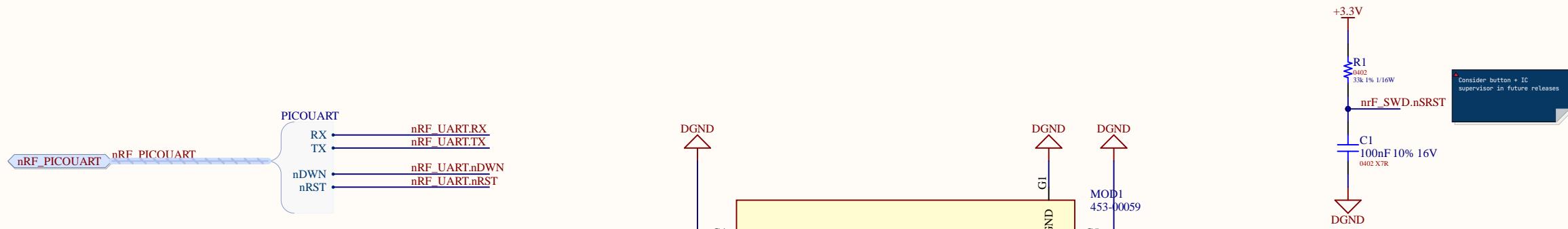
D

D

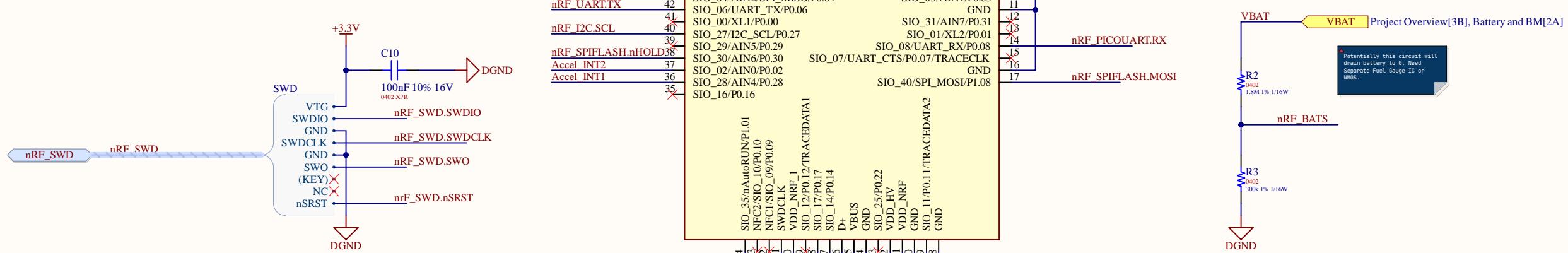


Title	Project Overview.SchDoc	Author	Dian Song	Cence Inc. 104 San Andreas Dr. Novato CA 94945 <b>CONFIDENTIAL</b>
Pj	<b>Alpha4.1.PpjPcb</b>	Modified	8/25/2022	
Date	9/9/2022 9:05:31 PM	Sheet	1 of 7	
Repository	<a href="https://git-dev.cence.cloud/limina-hardware/dsc_alpha4.1.git">https://git-dev.cence.cloud/limina-hardware/dsc_alpha4.1.git</a>	Variant	[No Variations]	

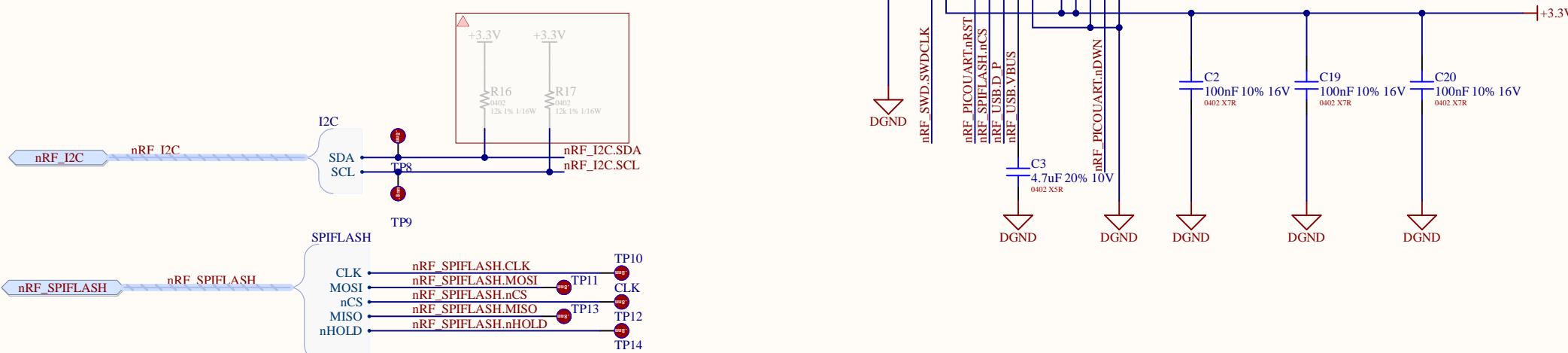
A



B



C



D

Title	BL653u.SchDoc	Author	Dian Song
Pj	Alpha4.1.PpjPcb	Modified	8/31/2022
Date	9/9/2022 9:05:32 PM	Variant	[No Variations]
Repository	<a href="https://git-dev.cence.cloud/lmina-hardware/dsc_alpha4.1.git">https://git-dev.cence.cloud/lmina-hardware/dsc_alpha4.1.git</a>		
Git Hash			

CENCE™

A

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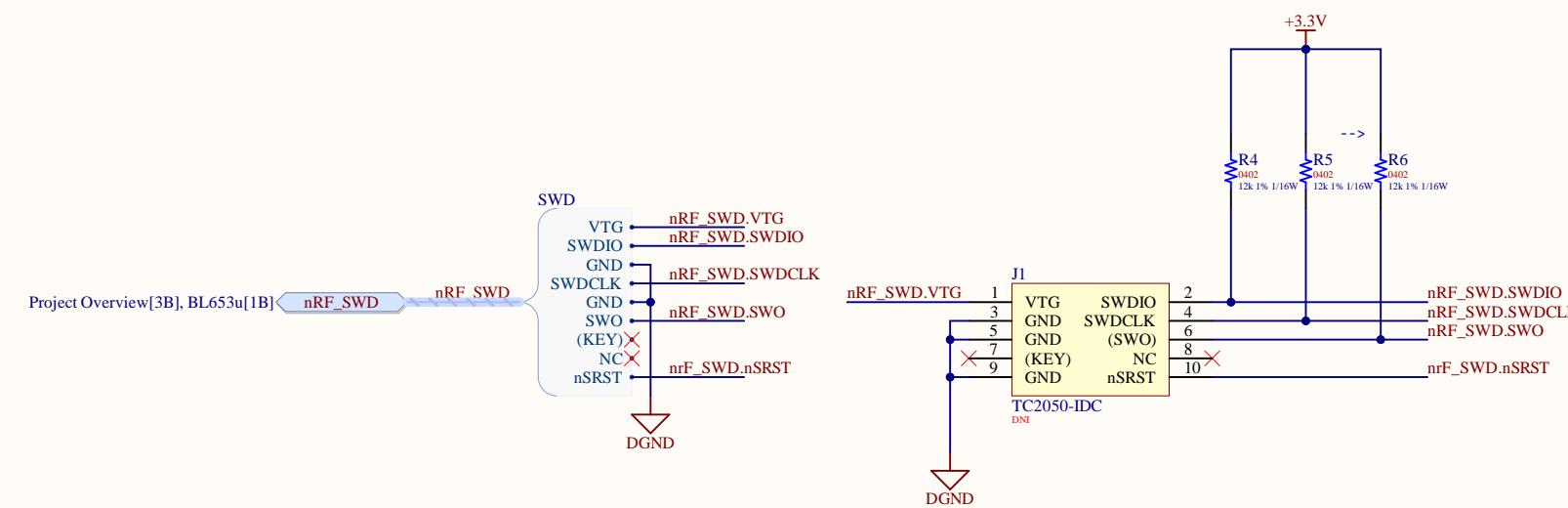
B

C

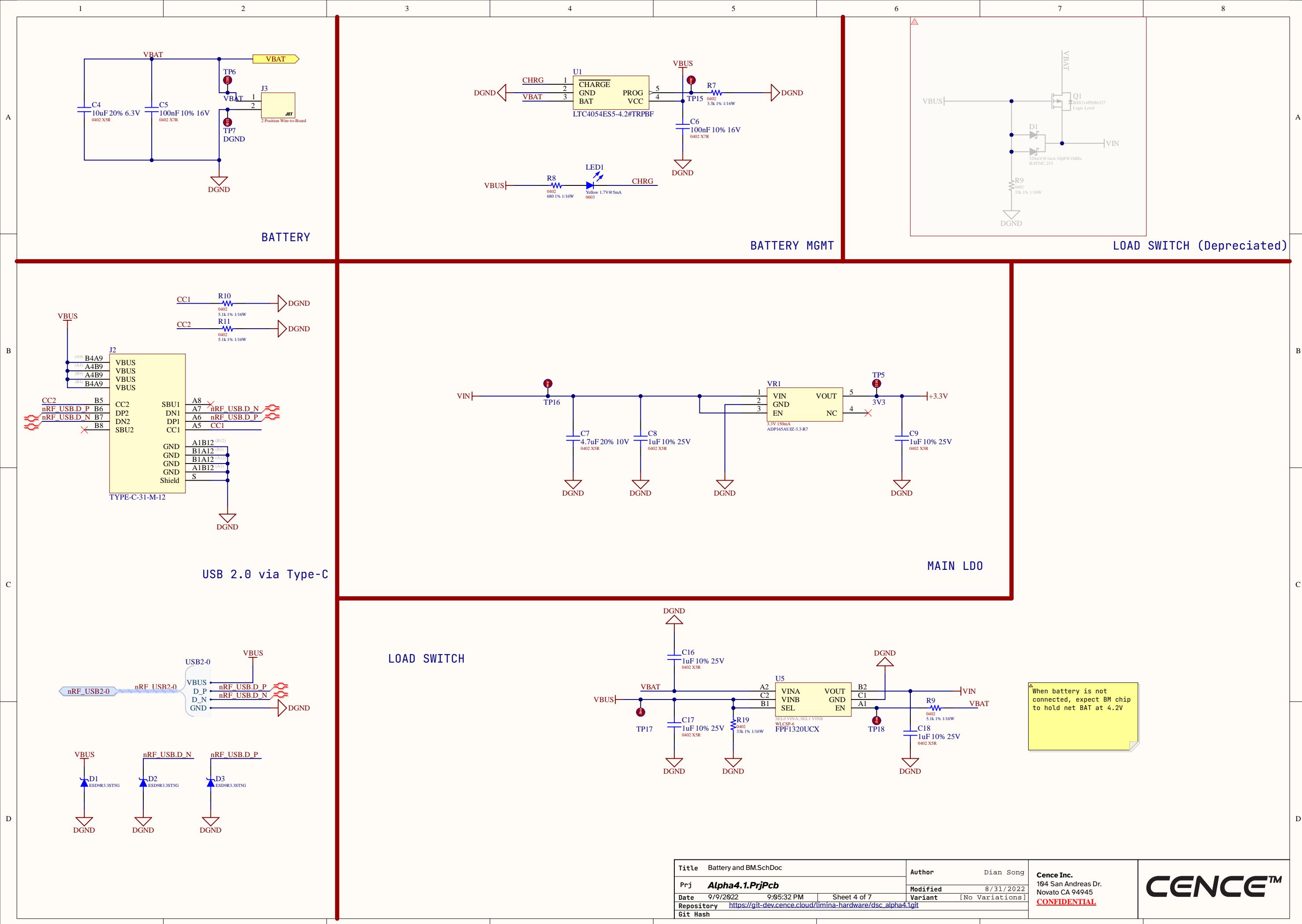
C

D

D

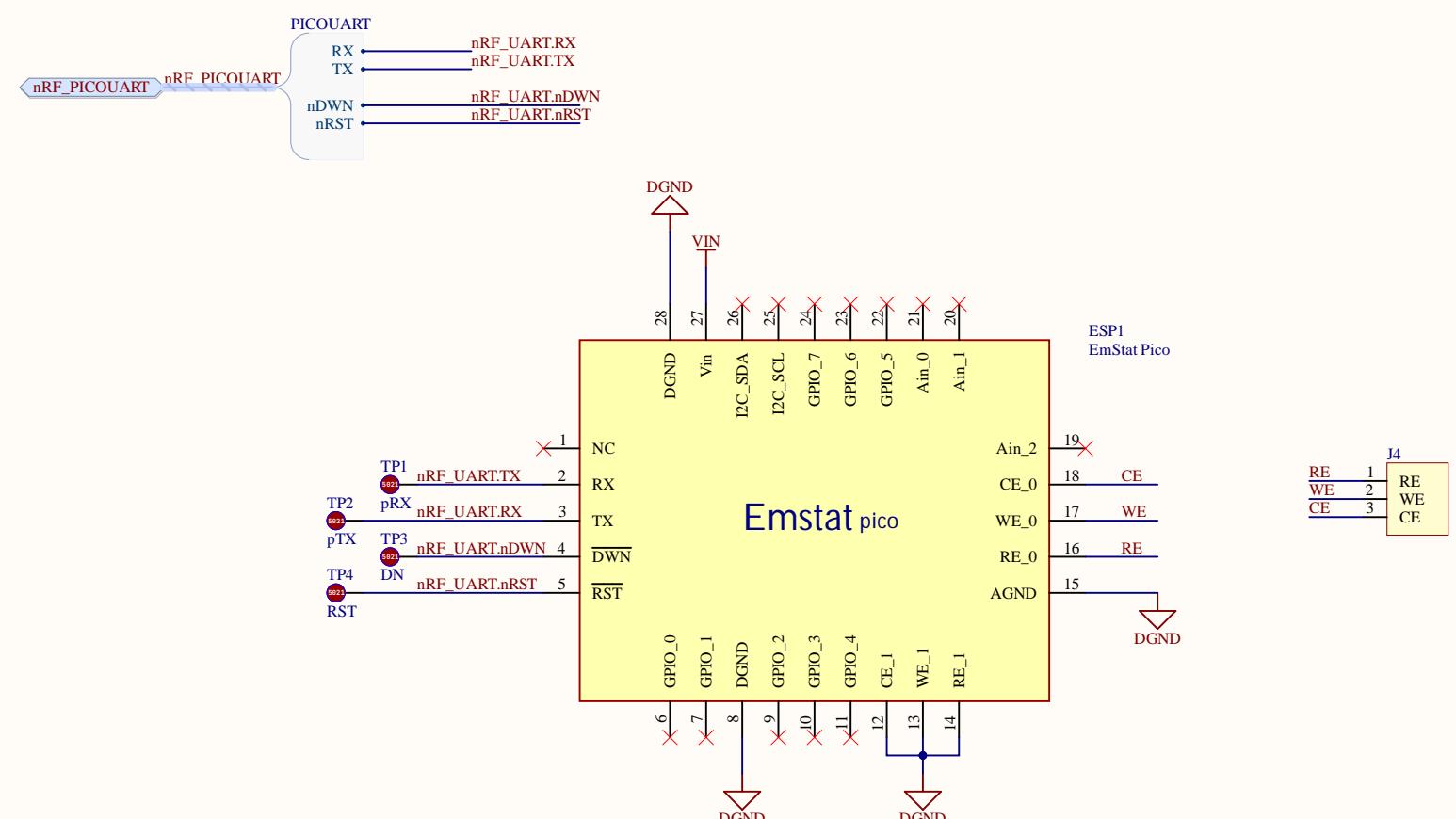


Title	SWD.SchDoc	Author	Dian Song	Cence Inc. 104 San Andreas Dr. Novato CA 94945 <b>CONFIDENTIAL</b>
Pj	<b>Alpha4.1.PpjPcb</b>	Modified	9/6/2022	
Date	9/9/2022 9:05:32 PM	Sheet	3 of 7	
Repository	<a href="https://git-dev.cence.cloud/limina-hardware/dsc_alpha4.1.git">https://git-dev.cence.cloud/limina-hardware/dsc_alpha4.1.git</a>	Variant	[No Variations]	



A

A



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D

<b>Title</b>	PicoCore ADuCM355.SchDoc	<b>Author</b>	Dian Song	<b>Cence Inc.</b> 104 San Andreas Dr. Novato CA 94945 <b>CONFIDENTIAL</b>
<b>Proj</b>	<b>Alpha4.1.PpjPcb</b>	<b>Modified</b>	8/31/2022	
<b>Date</b>	9/9/2022 9:05:32 PM	<b>Sheet</b>	5 of 7	
<b>Repository</b>	<a href="https://git-dev.cence.cloud/limina-hardware/dsc_alpha4.1.git">https://git-dev.cence.cloud/limina-hardware/dsc_alpha4.1.git</a>	<b>Variant</b>	[No Variations]	
<b>Git Hash</b>				

A

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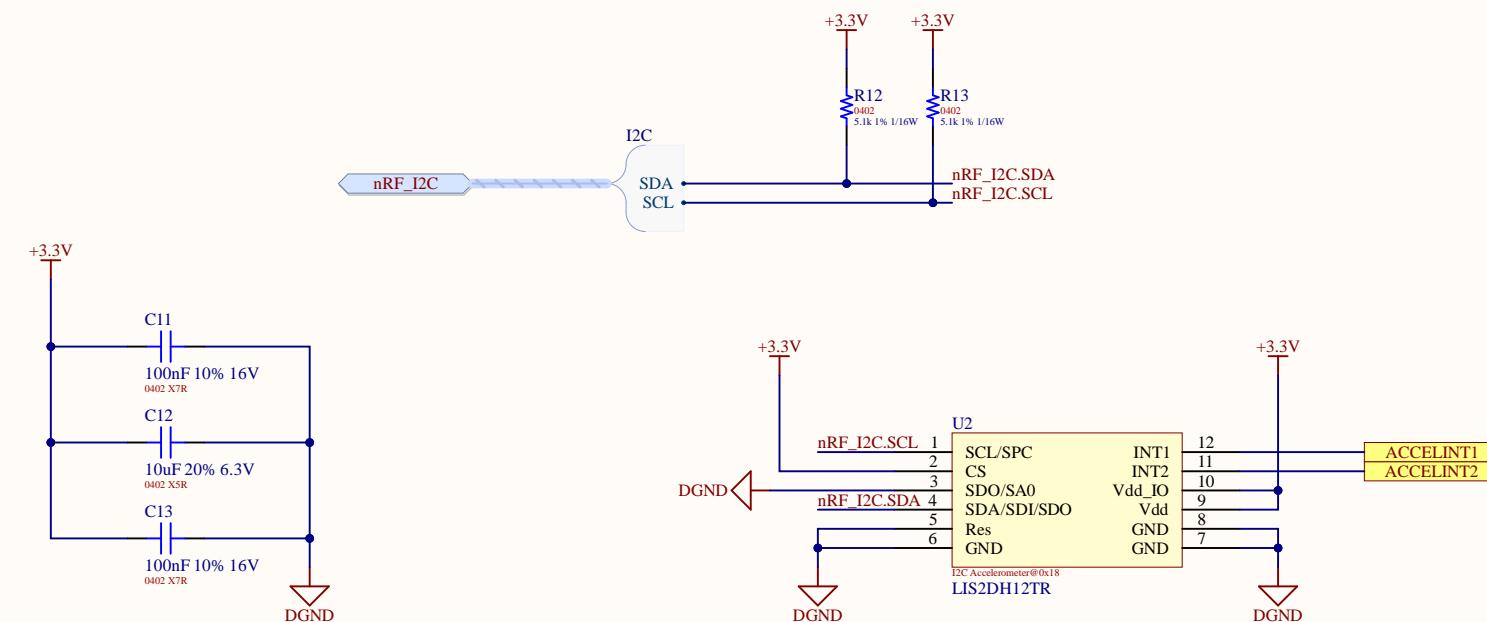
B

C

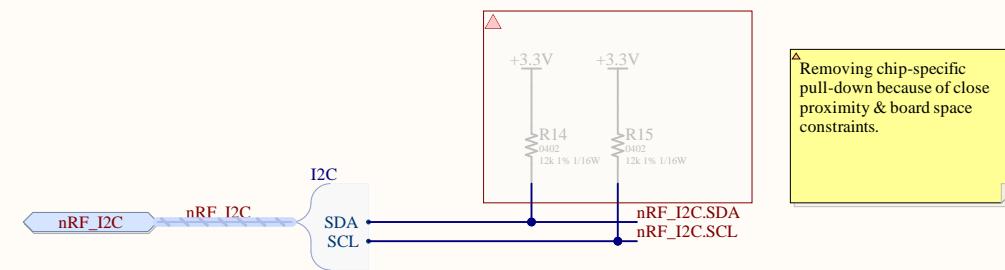
C

D

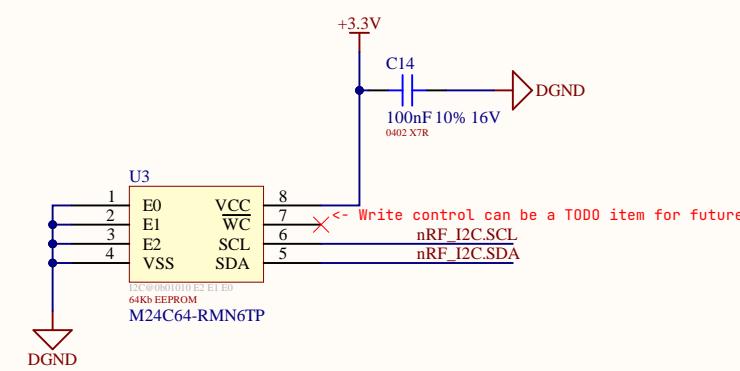
D



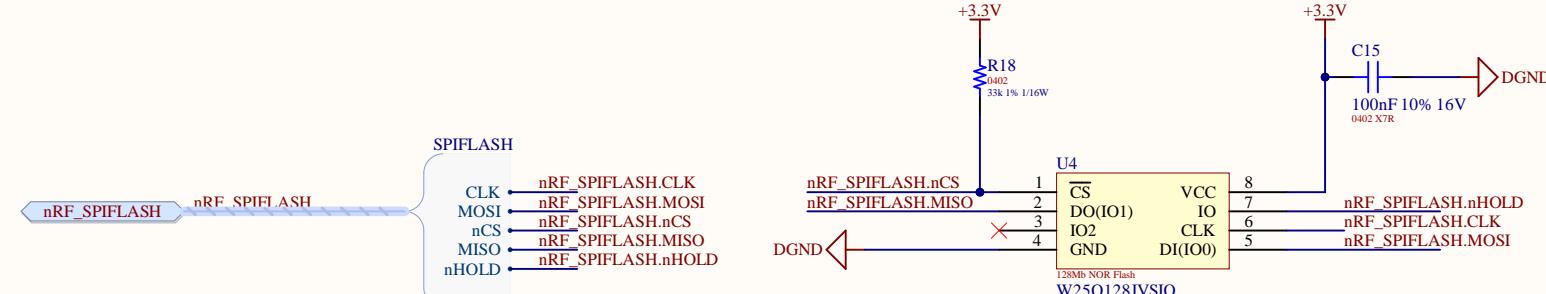
A



B



C



D

Title	EEPROM and Flash.SchDoc	Author	Dian Song
Proj	Alpha4.1.PjPcb	Modified	8/31/2022
Date	9/9/2022 9:05:32 PM	Sheet	7 of 7
Repository	<a href="https://git-dev.cence.cloud/lmina-hardware/dsc_alpha4.1.git">https://git-dev.cence.cloud/lmina-hardware/dsc_alpha4.1.git</a>	Variant	[No Variations]
Git Hash		Cence Inc.	104 San Andreas Dr. Novato CA 94945 <b>CONFIDENTIAL</b>
			<b>CENCE™</b>

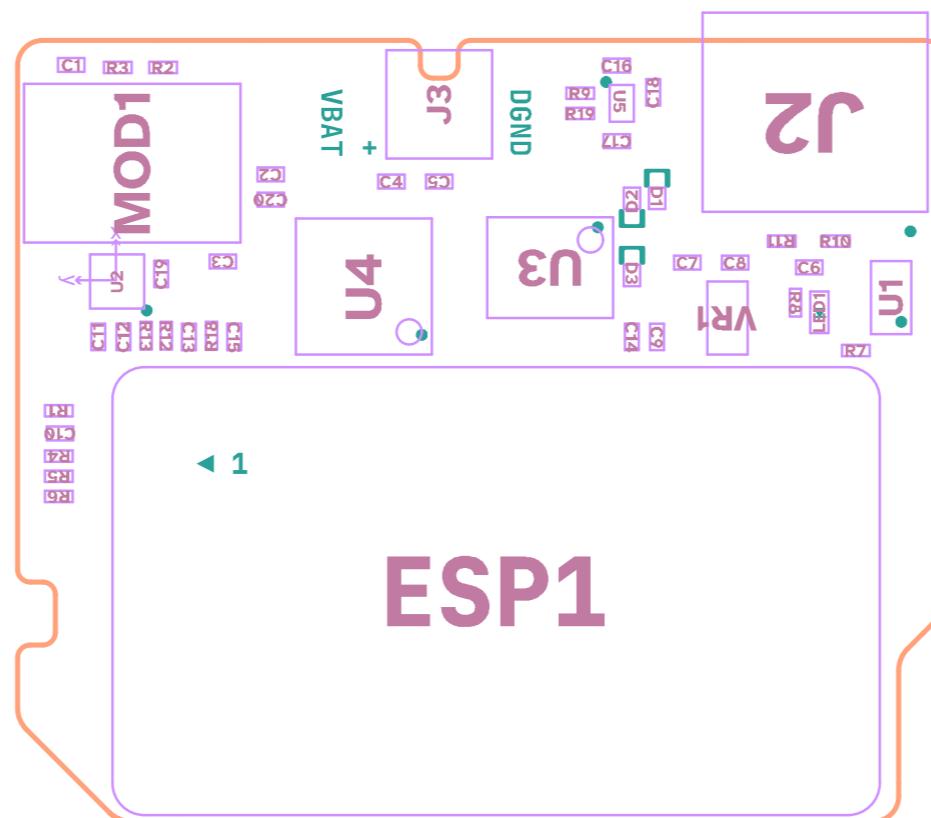
## Top Assembly Drawing

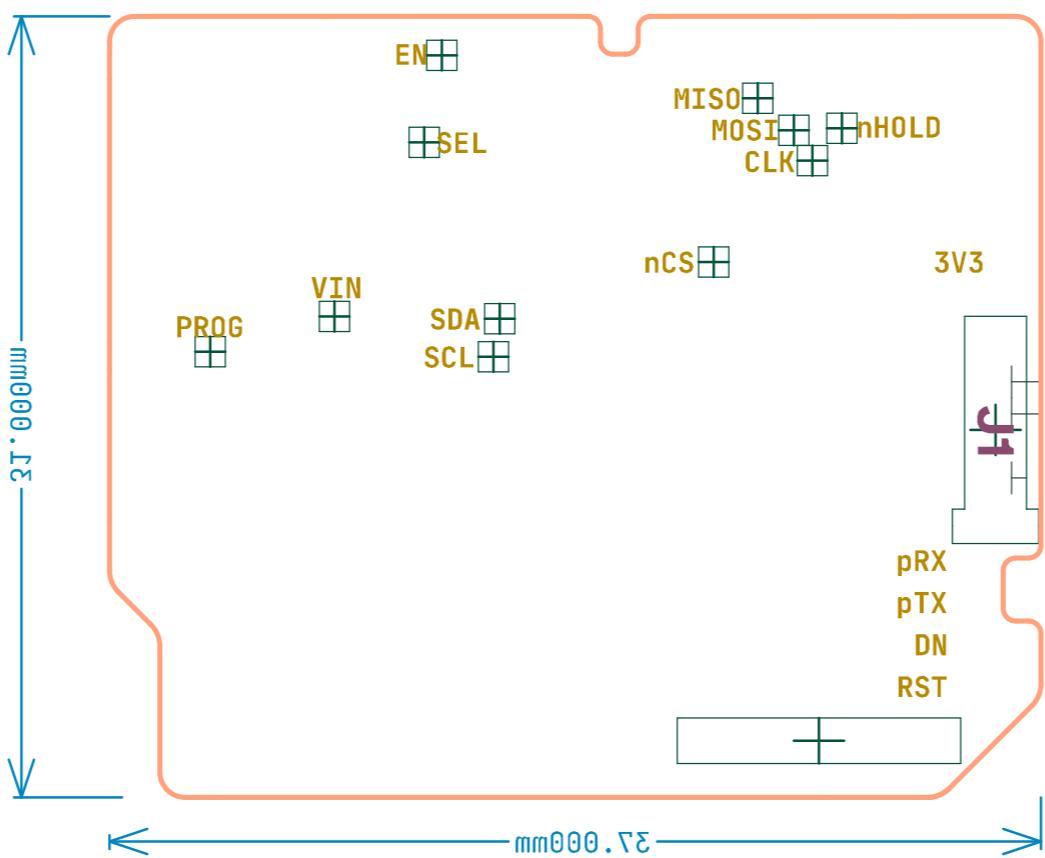
## Top Assembly Drawing

### Board Statistics

Nets 34  
Components 73  
Pads 805  
Tracks 1739  
Arcs 55  
Polygons 11  
Vias 142  
Holes 690

LAST MODIFICATION 9/9/2022 5:28:50 PM  
BY Dian Song  
Using Altium Designer 22.8.2.66



**Board Statistics**

Holes	690
Alcs	55
Polygons	7739
Tracks	802
Bads	34
Components	73
Netw	34

LAST MODIFICATION 2\2022 5:28:26 PM  
BY Dian Sun Soud  
Using Affinity Designer 22.8.2.89

Board Part/Sect	Layer	Name	Material	Thickness	Count/Pkt	Group
Top Deferal				0.0125mm	3,8	ET2
Top Mask				0.025mm	1	ET1
Top Copper				0.025mm	1	ET1
Differential I	1	2058	Solder Resist	0.0125mm	3,8	ET2
2	2058			0.0125mm	3,8	ET2
3	2058			0.0125mm	3,8	ET2
4	2058			0.0125mm	3,8	ET2
5	2058			0.0125mm	3,8	ET2
6	2058			0.0125mm	3,8	ET2
7	2058			0.0125mm	3,8	ET2
8	2058			0.0125mm	3,8	ET2
9	2058			0.0125mm	3,8	ET2
10	2058			0.0125mm	3,8	ET2
11	2058			0.0125mm	3,8	ET2
12	2058			0.0125mm	3,8	ET2
13	2058			0.0125mm	3,8	ET2
14	2058			0.0125mm	3,8	ET2
15	2058			0.0125mm	3,8	ET2
16	2058			0.0125mm	3,8	ET2
17	2058			0.0125mm	3,8	ET2
18	2058			0.0125mm	3,8	ET2
19	2058			0.0125mm	3,8	ET2
20	2058			0.0125mm	3,8	ET2
21	2058			0.0125mm	3,8	ET2
22	2058			0.0125mm	3,8	ET2
23	2058			0.0125mm	3,8	ET2
24	2058			0.0125mm	3,8	ET2
25	2058			0.0125mm	3,8	ET2
26	2058			0.0125mm	3,8	ET2
27	2058			0.0125mm	3,8	ET2
28	2058			0.0125mm	3,8	ET2
29	2058			0.0125mm	3,8	ET2
30	2058			0.0125mm	3,8	ET2
31	2058			0.0125mm	3,8	ET2
32	2058			0.0125mm	3,8	ET2
33	2058			0.0125mm	3,8	ET2
34	2058			0.0125mm	3,8	ET2
35	2058			0.0125mm	3,8	ET2
36	2058			0.0125mm	3,8	ET2
37	2058			0.0125mm	3,8	ET2
38	2058			0.0125mm	3,8	ET2
39	2058			0.0125mm	3,8	ET2
40	2058			0.0125mm	3,8	ET2
41	2058			0.0125mm	3,8	ET2
42	2058			0.0125mm	3,8	ET2
43	2058			0.0125mm	3,8	ET2
44	2058			0.0125mm	3,8	ET2
45	2058			0.0125mm	3,8	ET2
46	2058			0.0125mm	3,8	ET2
47	2058			0.0125mm	3,8	ET2
48	2058			0.0125mm	3,8	ET2
49	2058			0.0125mm	3,8	ET2
50	2058			0.0125mm	3,8	ET2
51	2058			0.0125mm	3,8	ET2
52	2058			0.0125mm	3,8	ET2
53	2058			0.0125mm	3,8	ET2
54	2058			0.0125mm	3,8	ET2
55	2058			0.0125mm	3,8	ET2
56	2058			0.0125mm	3,8	ET2
57	2058			0.0125mm	3,8	ET2
58	2058			0.0125mm	3,8	ET2
59	2058			0.0125mm	3,8	ET2
60	2058			0.0125mm	3,8	ET2
61	2058			0.0125mm	3,8	ET2
62	2058			0.0125mm	3,8	ET2
63	2058			0.0125mm	3,8	ET2
64	2058			0.0125mm	3,8	ET2
65	2058			0.0125mm	3,8	ET2
66	2058			0.0125mm	3,8	ET2
67	2058			0.0125mm	3,8	ET2
68	2058			0.0125mm	3,8	ET2
69	2058			0.0125mm	3,8	ET2
70	2058			0.0125mm	3,8	ET2
71	2058			0.0125mm	3,8	ET2
72	2058			0.0125mm	3,8	ET2
73	2058			0.0125mm	3,8	ET2
74	2058			0.0125mm	3,8	ET2
75	2058			0.0125mm	3,8	ET2
76	2058			0.0125mm	3,8	ET2
77	2058			0.0125mm	3,8	ET2
78	2058			0.0125mm	3,8	ET2
79	2058			0.0125mm	3,8	ET2
80	2058			0.0125mm	3,8	ET2
81	2058			0.0125mm	3,8	ET2
82	2058			0.0125mm	3,8	ET2
83	2058			0.0125mm	3,8	ET2
84	2058			0.0125mm	3,8	ET2
85	2058			0.0125mm	3,8	ET2
86	2058			0.0125mm	3,8	ET2
87	2058			0.0125mm	3,8	ET2
88	2058			0.0125mm	3,8	ET2
89	2058			0.0125mm	3,8	ET2
90	2058			0.0125mm	3,8	ET2
91	2058			0.0125mm	3,8	ET2
92	2058			0.0125mm	3,8	ET2
93	2058			0.0125mm	3,8	ET2
94	2058			0.0125mm	3,8	ET2
95	2058			0.0125mm	3,8	ET2
96	2058			0.0125mm	3,8	ET2
97	2058			0.0125mm	3,8	ET2
98	2058			0.0125mm	3,8	ET2
99	2058			0.0125mm	3,8	ET2
100	2058			0.0125mm	3,8	ET2
101	2058			0.0125mm	3,8	ET2
102	2058			0.0125mm	3,8	ET2
103	2058			0.0125mm	3,8	ET2
104	2058			0.0125mm	3,8	ET2
105	2058			0.0125mm	3,8	ET2
106	2058			0.0125mm	3,8	ET2
107	2058			0.0125mm	3,8	ET2
108	2058			0.0125mm	3,8	ET2
109	2058			0.0125mm	3,8	ET2
110	2058			0.0125mm	3,8	ET2
111	2058			0.0125mm	3,8	ET2
112	2058			0.0125mm	3,8	ET2
113	2058			0.0125mm	3,8	ET2
114	2058			0.0125mm	3,8	ET2
115	2058			0.0125mm	3,8	ET2
116	2058			0.0125mm	3,8	ET2
117	2058			0.0125mm	3,8	ET2
118	2058			0.0125mm	3,8	ET2

## Top Paste Mask Print

## Top Paste Mask Print

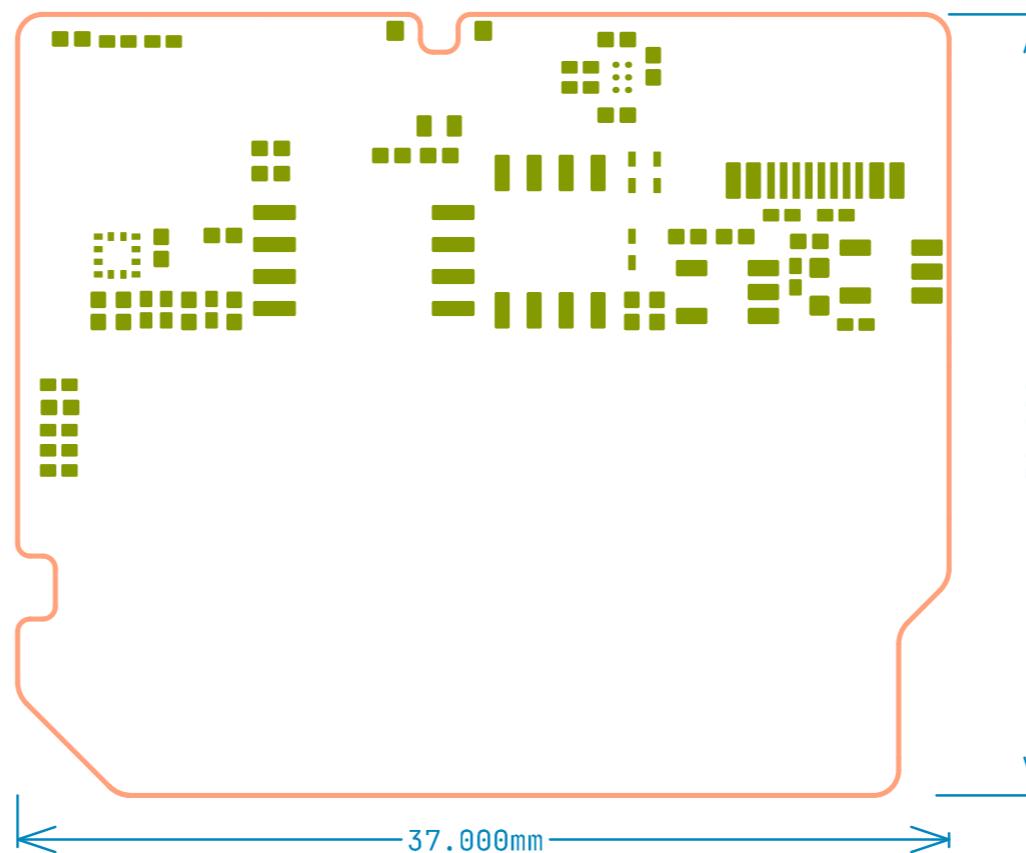
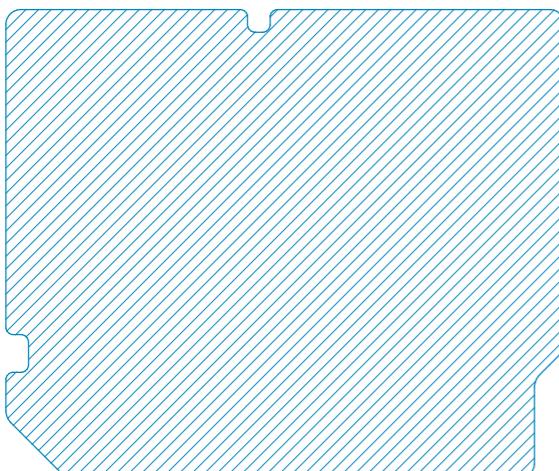
### Board Statistics

Nets 34  
Components 73  
Pads 805  
Tracks 1739  
Arcs 55  
Polygons 11  
Vias 142  
Holes 690

LAST MODIFICATION 9/9/2022 5:28:50 PM  
BY Dian Song  
Using Altium Designer 22.8.2.66

Board Layer Stack	Layer	Name	Material	Thickness	Constant	Gerber
		Top Overlay				GTO
		Top Mask	Solder Resist	0.015mm	3.8	GTS
1		Top Copper		0.035mm		GTL
		Dielectric 1	7628	0.280mm	4.6	
2		Signal Layer 1		0.018mm		G1
		Core	FR-4	0.465mm	4.5	
3		Signal Layer 2		0.018mm		G2
		Dielectric 2	7628	0.280mm	4.6	
4		Bottom Copper		0.035mm		GBL
		Bottom Mask	Solder Resist	0.015mm	3.8	GBS
		Bottom Overlay				GBO

Total board thickness: 1.000mm



## Bottom Paste Mask Print

## Bottom Paste Mask Print

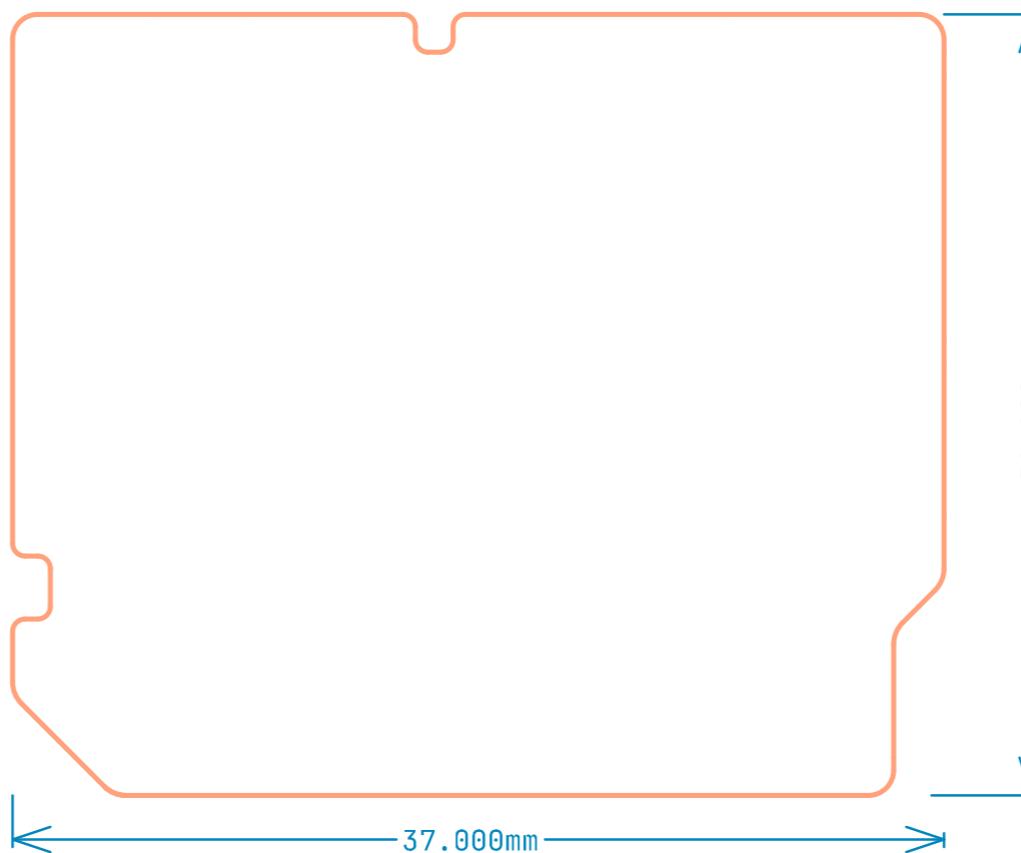
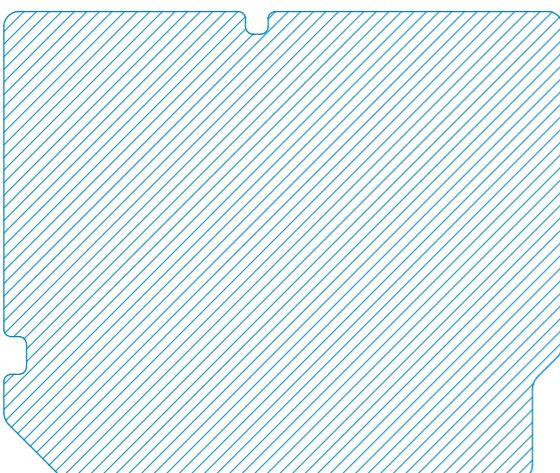
### Board Statistics

Nets 34  
Components 73  
Pads 805  
Tracks 1739  
Arcs 55  
Polygons 11  
Vias 142  
Holes 690

LAST MODIFICATION 9/9/2022 5:28:50 PM  
BY Dian Song  
Using Altium Designer 22.8.2.66

Board Layer Stack	Layer	Name	Material	Thickness	Constant	Gerber
		Top Overlay				GTO
		Top Mask	Solder Resist	0.015mm	3.8	GTS
	1	Top Copper		0.035mm		GTL
		Dielectric 1	7628	0.280mm	4.6	
	2	Signal Layer 1		0.018mm		G1
		Core	FR-4	0.465mm	4.5	
	3	Signal Layer 2		0.018mm		G2
		Dielectric 2	7628	0.280mm	4.6	
	4	Bottom Copper		0.035mm		GBL
		Bottom Mask	Solder Resist	0.015mm	3.8	GBS
		Bottom Overlay				GBO

Total board thickness: 1.000mm



## Top Solder Mask Print

## Top Solder Mask Print

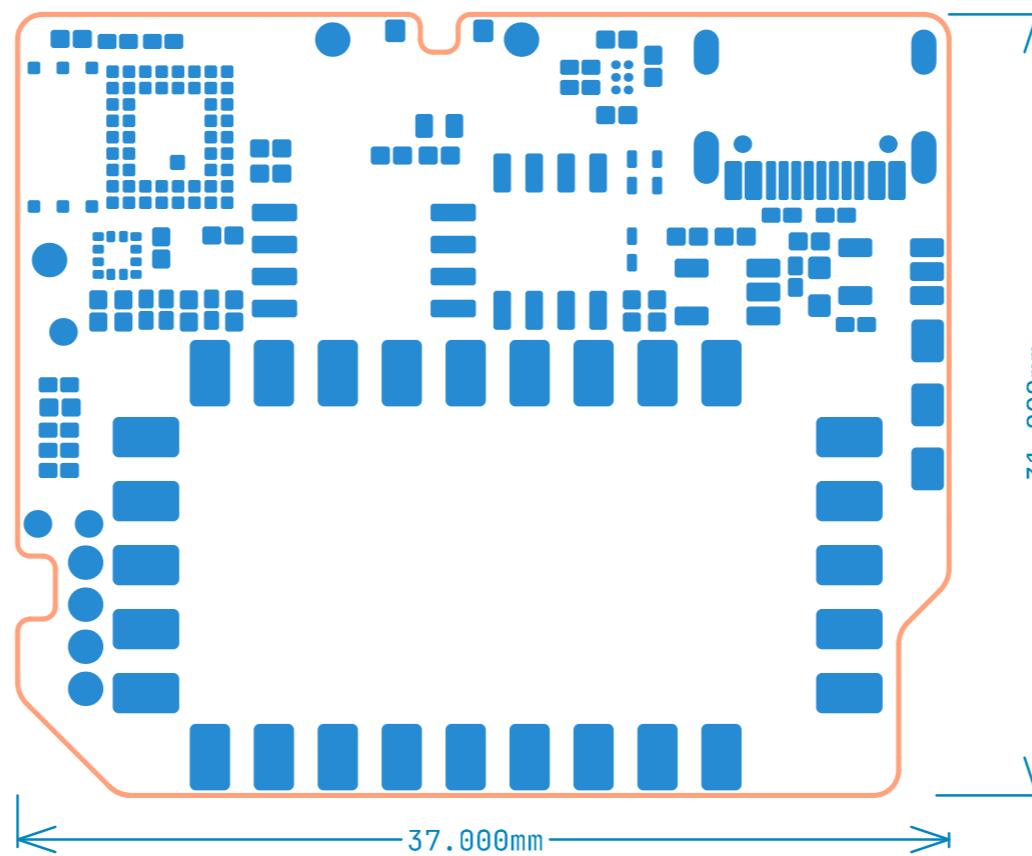
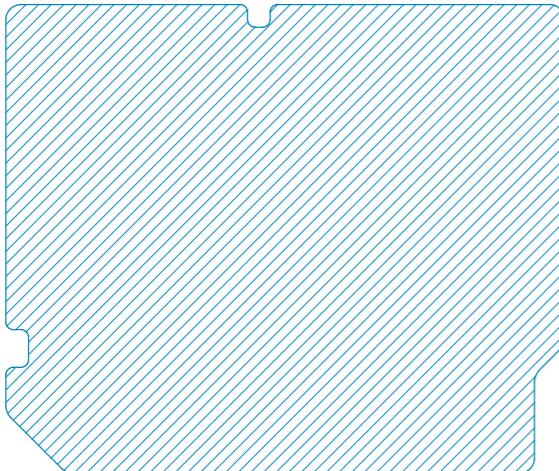
### Board Statistics

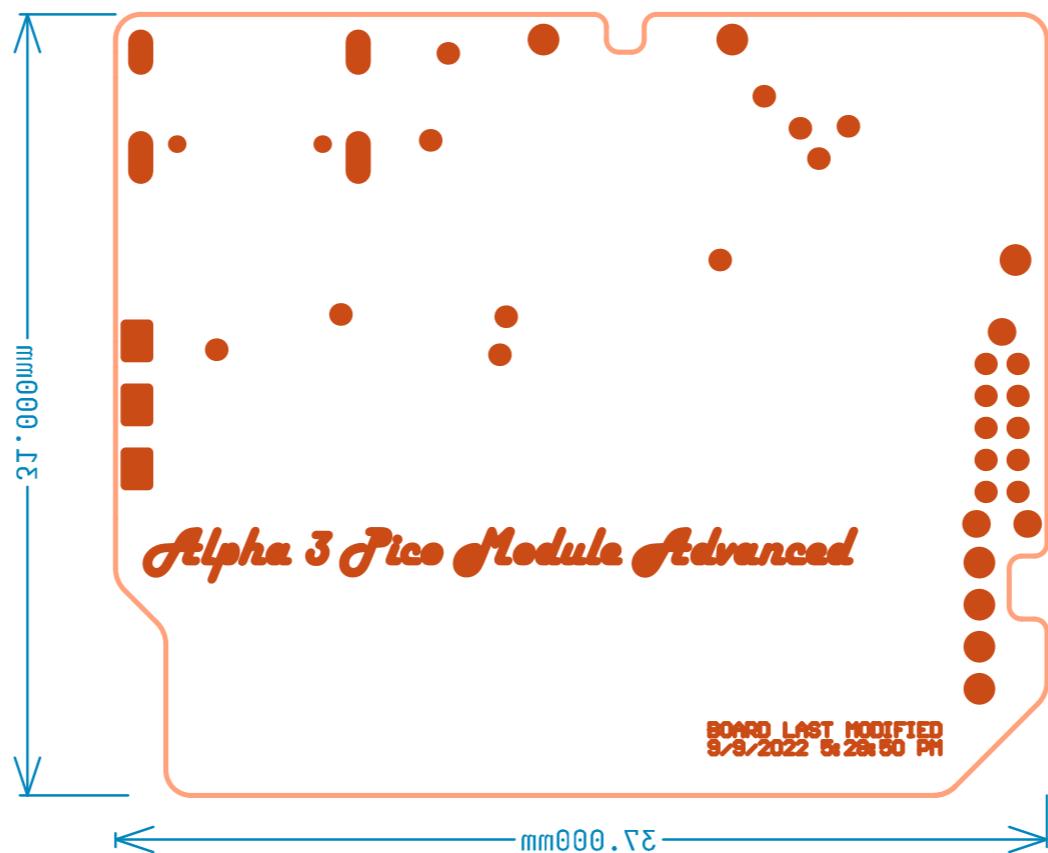
Nets 34  
Components 73  
Pads 805  
Tracks 1739  
Arcs 55  
Polygons 11  
Vias 142  
Holes 690

LAST MODIFICATION 9/9/2022 5:28:50 PM  
BY Dian Song  
Using Altium Designer 22.8.2.66

Board Layer Stack	Layer	Name	Material	Thickness	Constant	Gerber
		Top Overlay				GTO
		Top Mask	Solder Resist	0.015mm	3.8	GTS
1		Top Copper		0.035mm		GTL
		Dielectric 1	7628	0.280mm	4.6	
2		Signal Layer 1		0.018mm		G1
		Core	FR-4	0.465mm	4.5	
3		Signal Layer 2		0.018mm		G2
		Dielectric 2	7628	0.280mm	4.6	
4		Bottom Copper		0.035mm		GBL
		Bottom Mask	Solder Resist	0.015mm	3.8	GBS
		Bottom Overlay				GBO

Total board thickness: 1.000mm



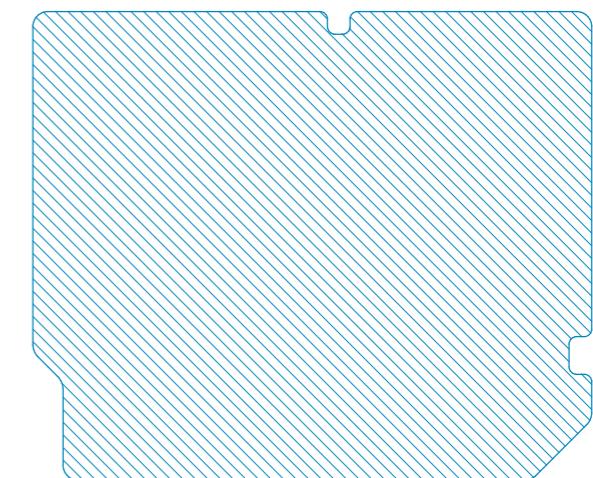


## Board Statistics

Category	Count
Masks	34
Components	73
Pad	802
Tracks	573
Arches	55
Polygons	77
Vias	745
Holes	690

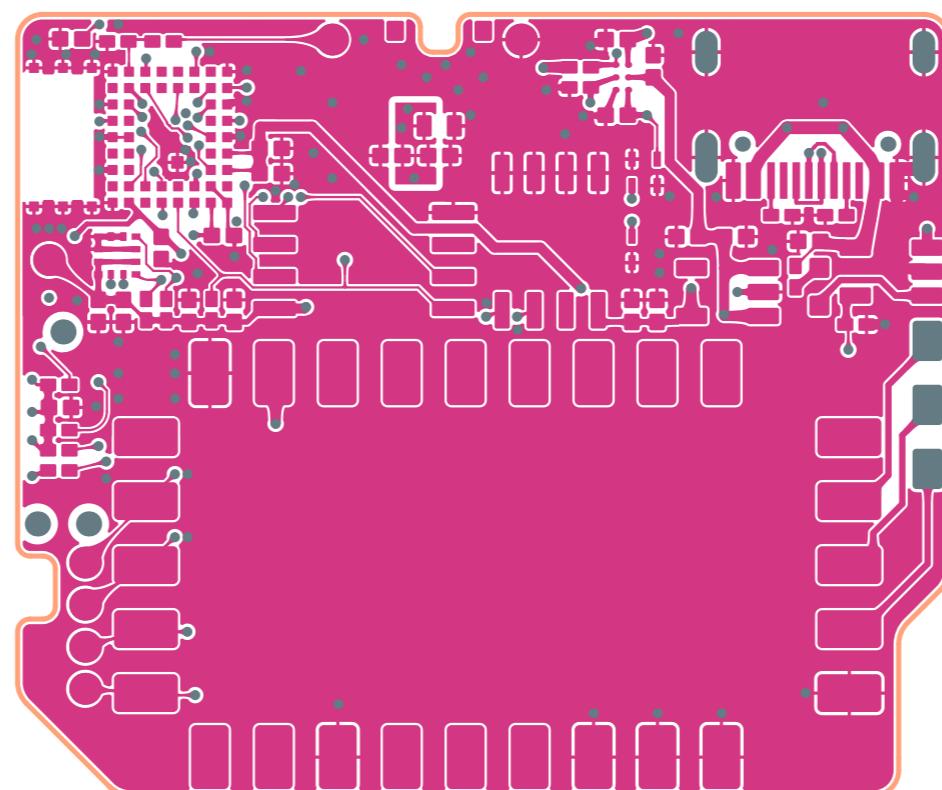
LAST MODIFICATION 9\9\2022 5:28:50 PM  
BY Dian Sun BY Dian Sun  
Using Affinity Designer 22.8.2.99

Board Layer Stack	Layer	Name	Material	Thickness	Conductive	Ground
1	Top Overlay	Top Overlay	0.0125in	3.8	ET2	
2	Top Padbar	Padbar	0.025in	4.0	ET1	
3	Differential 1	Differential 1	0.025in	4.0	ET1	
4	Simpler Layer 1	Simpler Layer 1	0.025in	4.0	ET1	
5	Cable	Cable	0.040in	4.0	ET1	
6	Simpler Layer 2	Simpler Layer 2	0.010in	4.0	ES	
7	Differential 2	Differential 2	0.025in	4.0	ES	
8	Bottom Padbar	Padbar	0.025in	4.0	EB2	
9	Bottom Mask	Padbar	0.0125in	3.8	EB2	
10	Bottom Overlay	Bottom Overlay	0.0125in	3.8	EB2	



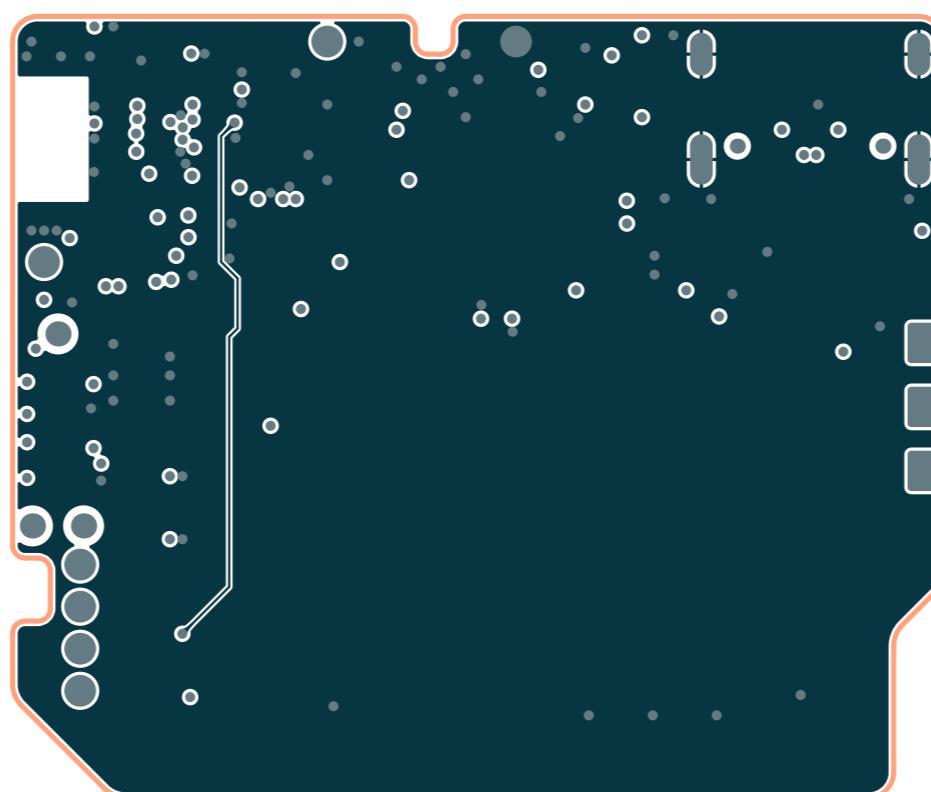
TOP COPPER

TOP COPPER



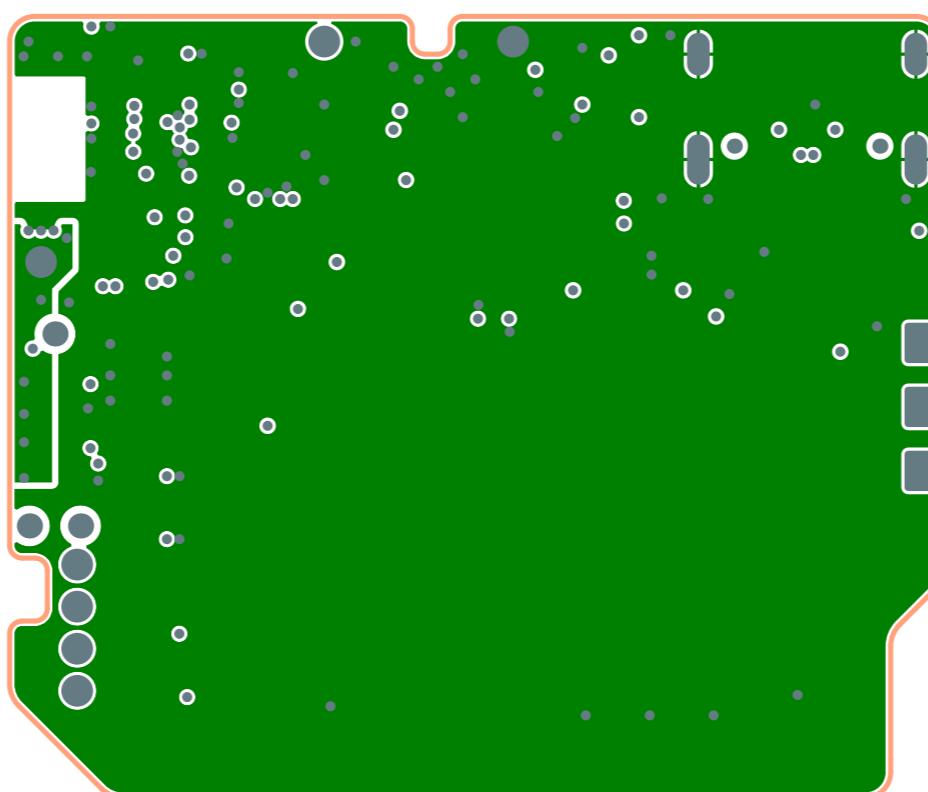
SIGNAL 1

SIGNAL 1



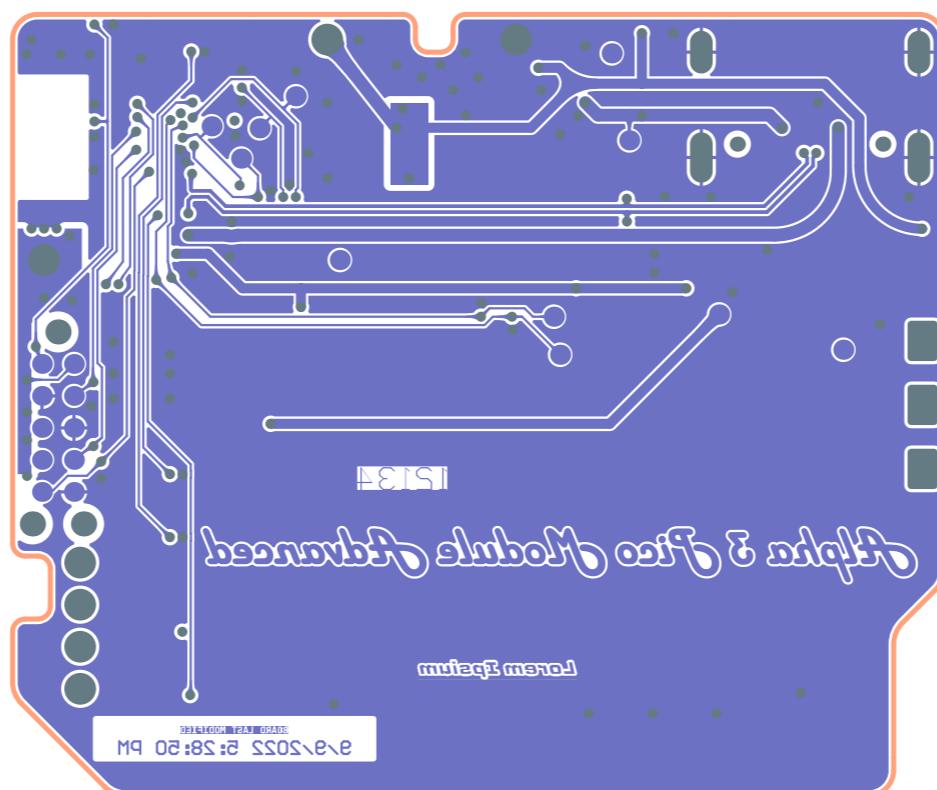
SIGNAL 2

SIGNAL 2



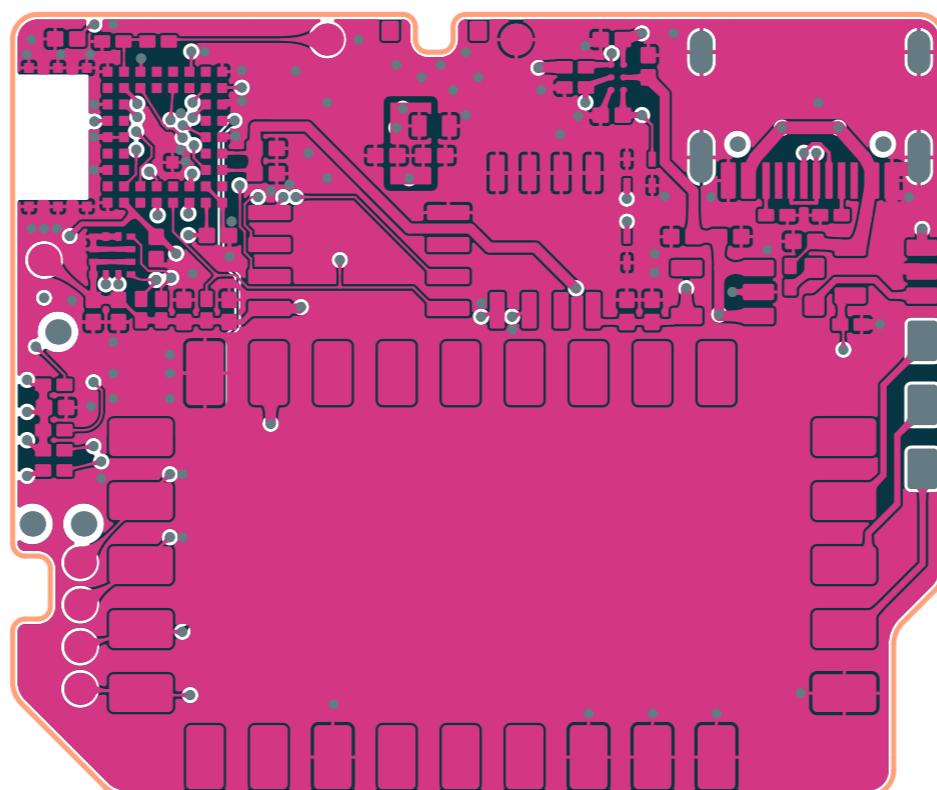
BOTTOM COPPER

BOTTOM COPPER



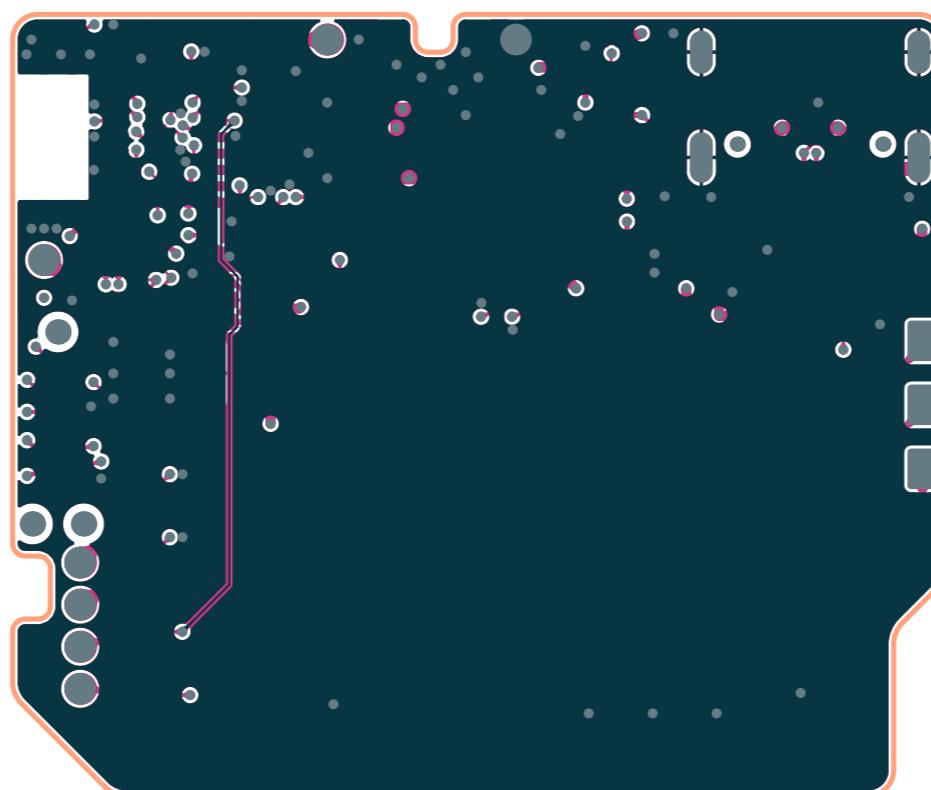
TOP ON SIGNAL 1

TOP ON SIGNAL 1



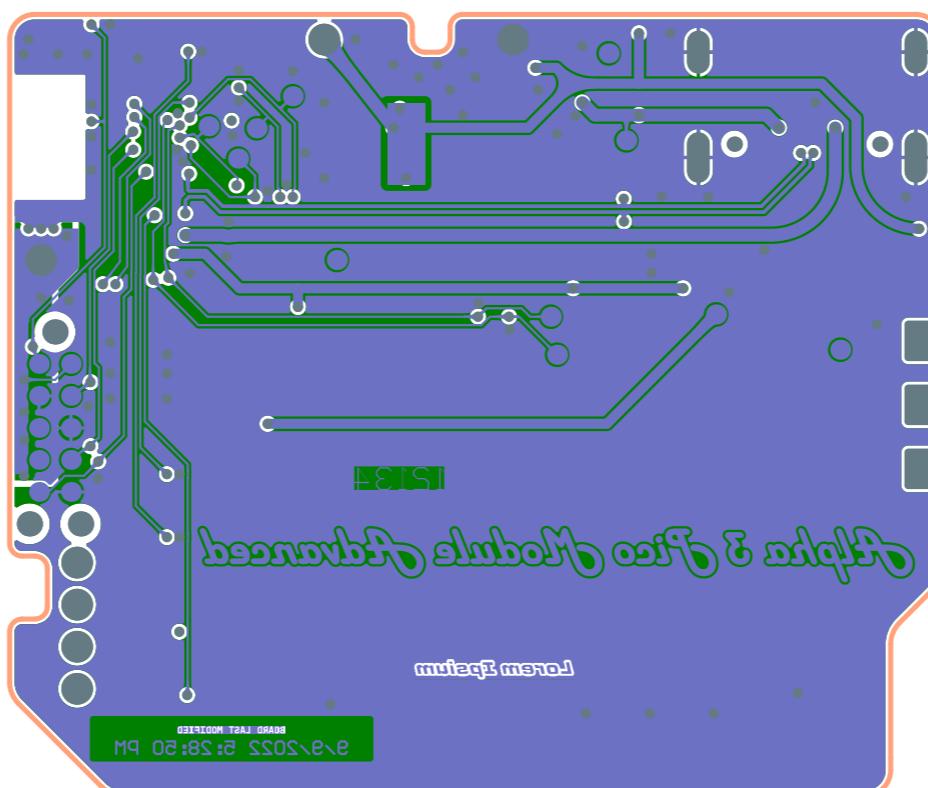
SIGNAL 1 ON TOP

SIGNAL 1 ON TOP



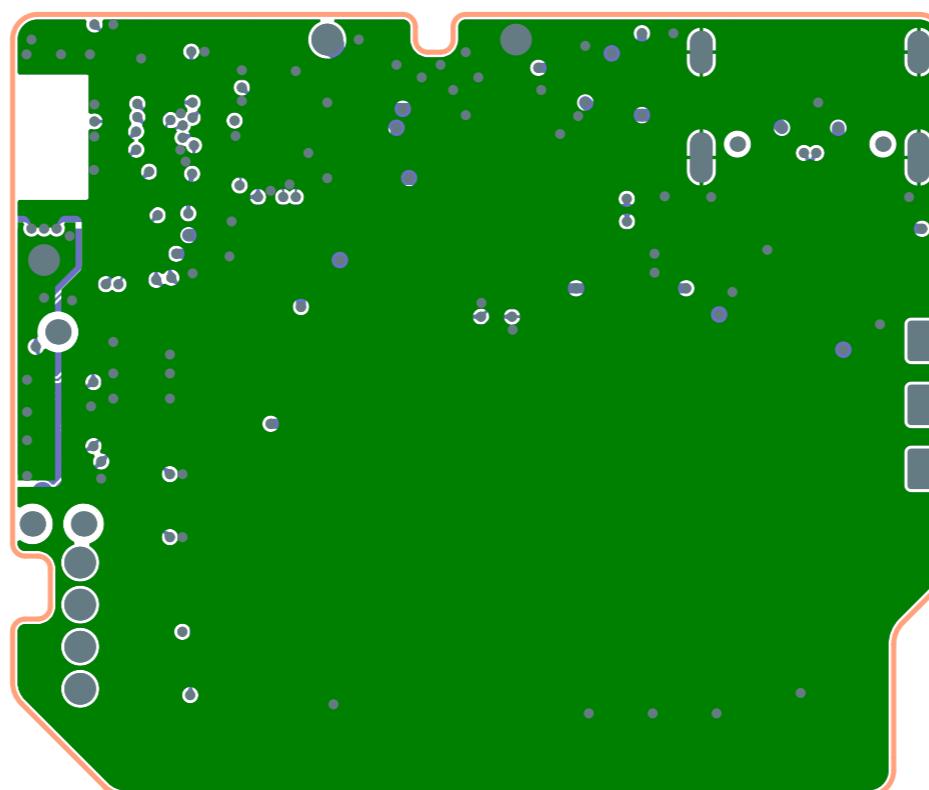
BOTTOM ON SIGNAL 2

BOTTOM ON SIGNAL 2



SIGNAL 2 ON BOTTOM

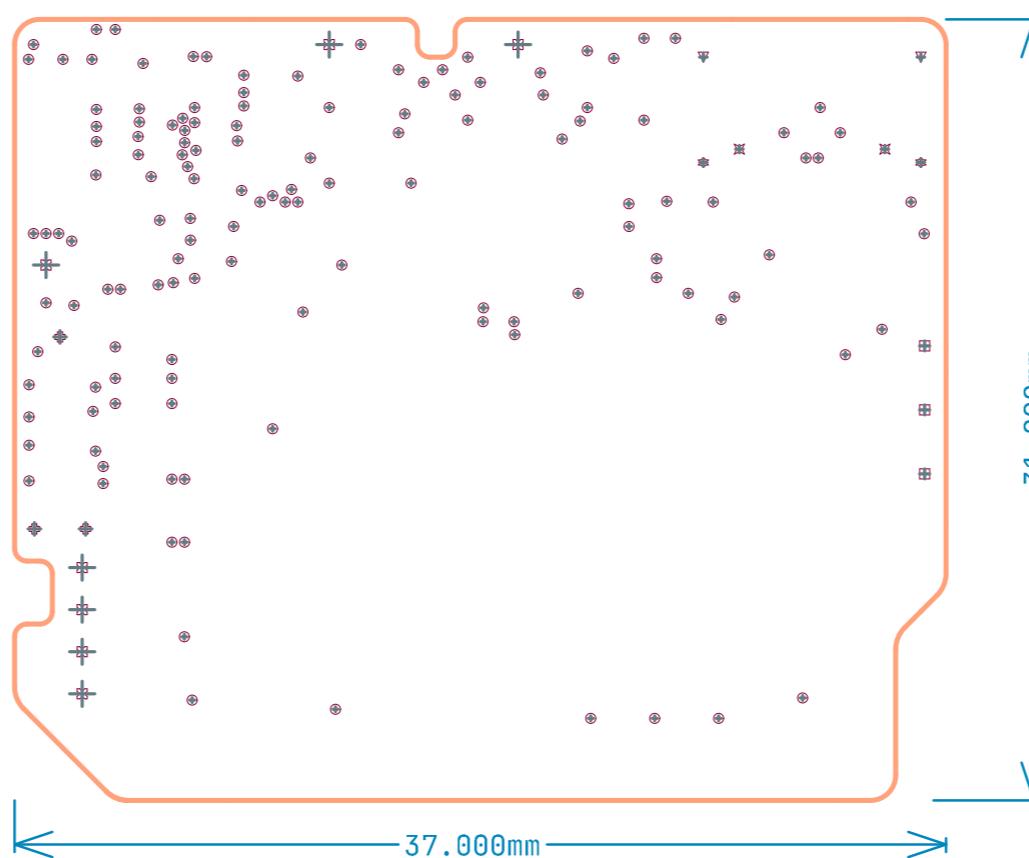
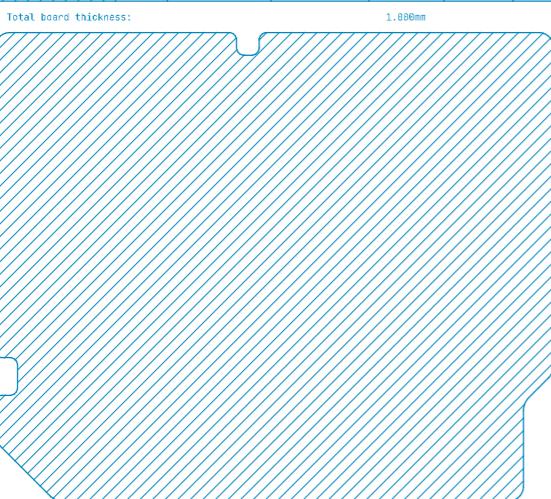
SIGNAL 2 ON BOTTOM



## FABRICATION NOTES

## FABRICATION NOTES

Board Layer Stack	Layer	Name	Material	Thickness	Constant	Gerber
		Top Overlay				GTO
		Top Mask	Solder Resist	0.015mm	3.8	GTS
1	Top Copper			0.035mm		GTL
		Dielectric 1	7628	0.280mm	4.6	
2	Signal Layer 1			0.018mm		G1
		Core	FR-4	0.465mm	4.5	
3	Signal Layer 2			0.018mm		G2
		Dielectric 2	7628	0.280mm	4.6	
4	Bottom Copper			0.035mm		GBL
		Bottom Mask	Solder Resist	0.015mm	3.8	GBS
		Bottom Overlay				GBO

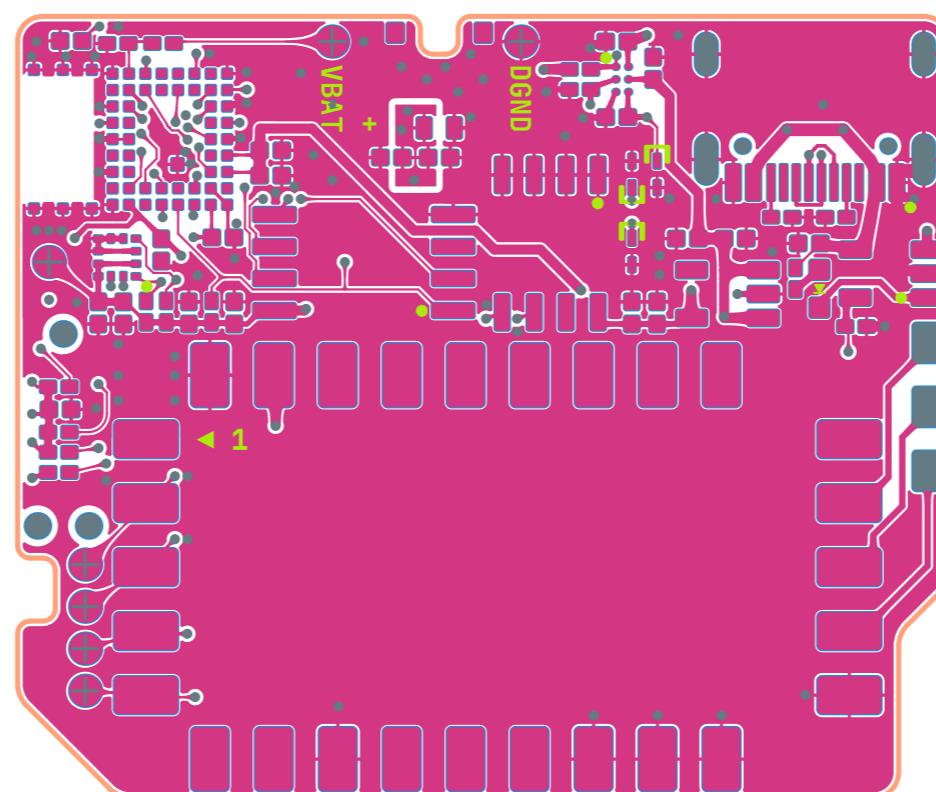


Symbol	Count	Finished Hole Diameter	Hole Tolerance	Plated	Via/Pad	Via Type	Via Feature	Hole Type	Hole Length	Routed Path Length
☒	2	0.60mm (23.622mil)		NPTH	Pad			Round	-	-
✚	3	1.00mm (39.370mil)		NPTH	Pad			Round	-	-
○	135	0.20mm (7.874mil)	+0.13mm/-0.08mm	PTH	Via	Type 2b	Tenting Both, Covering Both	Round	-	-
▽	2	0.60mm (23.622mil)		PTH	Pad			Slot	1.40mm (55.118mil)	0.80mm (31.496mil)
☆	2	0.60mm (23.622mil)		PTH	Pad			Slot	1.70mm (66.929mil)	1.10mm (43.307mil)
□	3	0.80mm (31.496mil)		PTH	Pad			Round	-	-
✗	7	1.00mm (39.370mil)		PTH	Via			Round	-	-

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.  
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

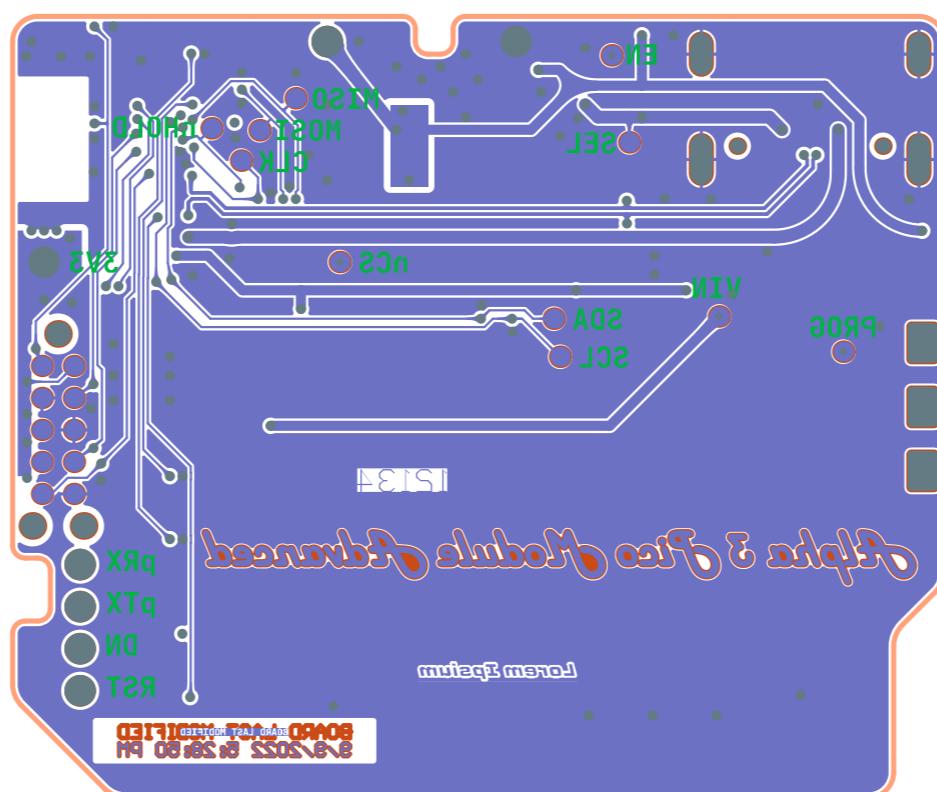
TOP VIEW

TOP VIEW



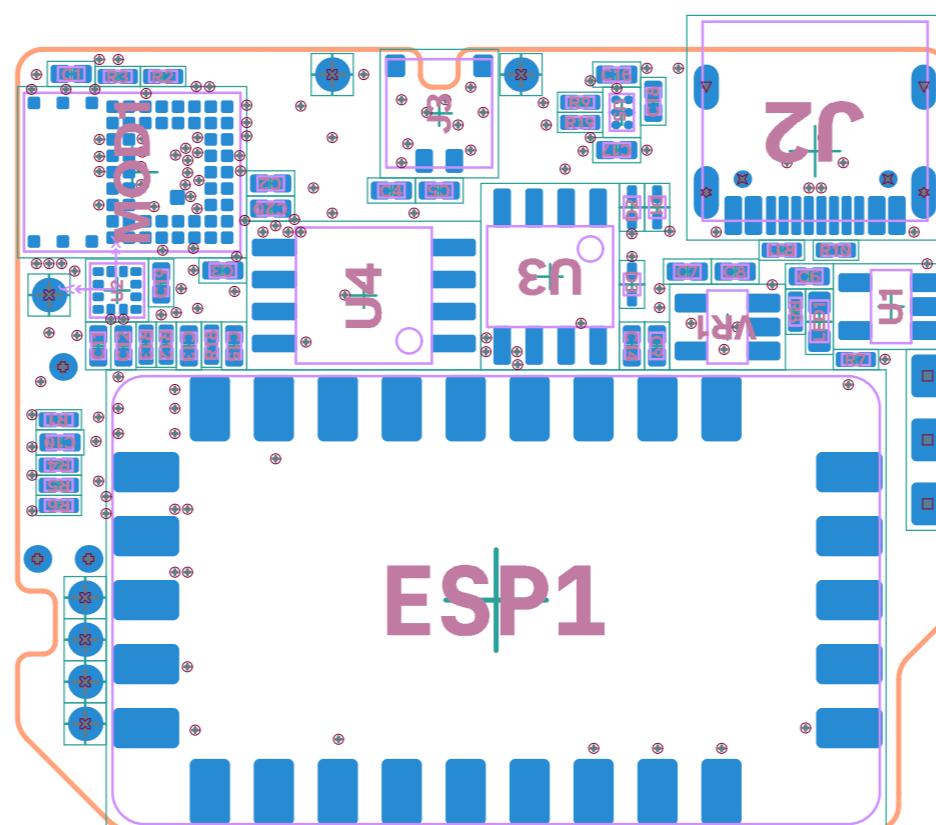
BOTTOM VIEW

BOTTOM VIEW



## TOP PLACEMENT

## TOP PLACEMENT

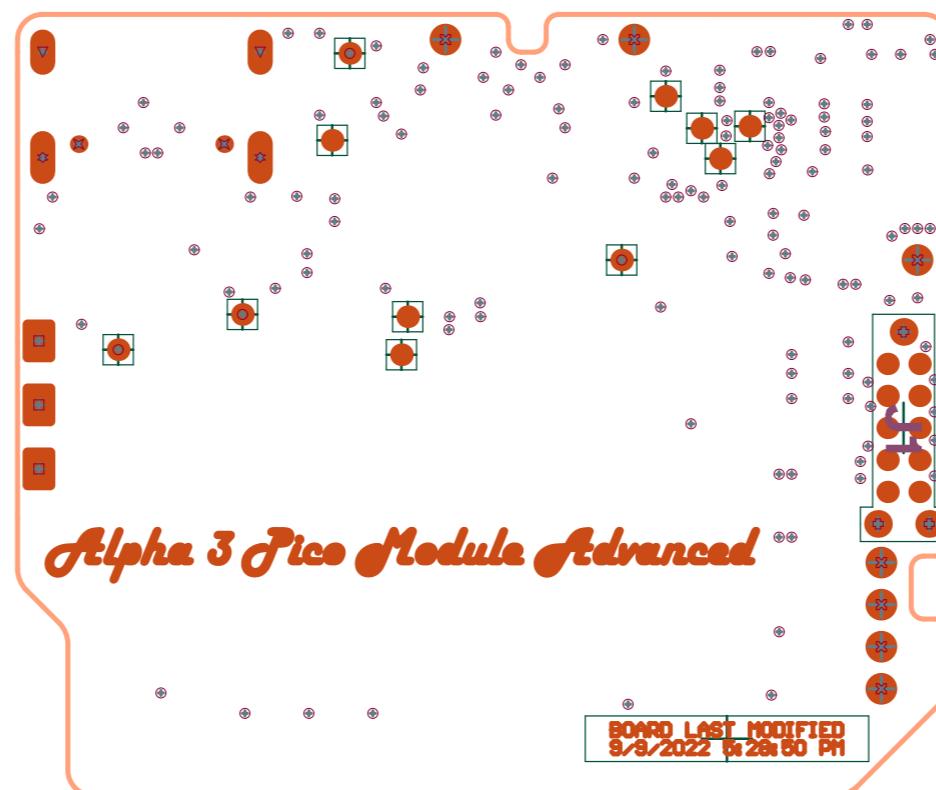


Symbol	Count	Finished Hole Diameter	Hole Tolerance	Plated	Via/Pad	Via Type	Via Feature	Hole Type	Hole Length	Routed Path Length
☒	2	0.60mm (23.622mil)		NPTH	Pad			Round	-	-
✚	3	1.00mm (39.370mil)		NPTH	Pad			Round	-	-
○	135	0.20mm (7.874mil)	+0.13mm/-0.08mm	PTH	Via	Type 2b	Tenting Both, Covering Both	Round	-	-
▽	2	0.60mm (23.622mil)		PTH	Pad			Slot	1.40mm (55.118mil)	0.80mm (31.496mil)
☆	2	0.60mm (23.622mil)		PTH	Pad			Slot	1.70mm (66.929mil)	1.10mm (43.307mil)
□	3	0.80mm (31.496mil)		PTH	Pad			Round	-	-
✗	7	1.00mm (39.370mil)		PTH	Via			Round	-	-

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.  
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

## TENMAGA MOTTO

## BOTTOM PLACEMENT



Symbol	Count	Furnished Hole Diameter	Hole Tolerance	Pfater	Via Pad	Via Type	Via Feature	Hole Length	Hole Type	Routed Path Length	Tool Length	Tool Type	Tenmag Moto
☒	2	0.06mm (3.0mil)	-	NPTH	Pad	NPTH	-	-	Round	-	-	-	-
☒	3	(3.0mil) mm00.1	-	Pad	Pad	NPTH	-	-	Round	-	-	-	-
○	736	(3.0mil) mm00.0	mm80.0-mm35.0+	HTP	Via	HTP	Type 2P	-	Texturing Both, Covering Both	-	-	Soft	(3.0mil) mm00.1
▽	2	(3.0mil) mm00.0	-	Pad	HTP	HTP	-	-	Round	-	-	Soft	(3.0mil) mm00.1
⊗	2	(3.0mil) mm00.0	-	Pad	HTP	HTP	-	-	Round	-	-	Soft	(3.0mil) mm00.1
□	3	(3.0mil) mm00.0	-	Pad	HTP	HTP	-	-	Round	-	-	Soft	(3.0mil) mm00.1
☒	7	0.06mm (3.0mil)	-	NPTH	Pad	NPTH	-	-	Round	-	-	-	-

Soft definitions : Routed Path Length = Calculated from tool start center position to tool end end center position.  
Hole Length = Routed Path Length + Tool Size = Soft length as defined in the PCB layout.

77.000mm

77.000mm

89.000mm

Hole Tolerance	Calculated Hole Diameter	Hole Length	Routed Path
+0.13mm / -0.0mm	1.40mm (55.118mil)	0.80mm (31.496mil)	-
+0.13mm / -0.0mm	1.70mm (66.929mil)	1.10mm (43.307mil)	-

Designator	Description	LibRef	Quantity	LCSC#	Installation Status	Manufacturer Part Number	Supplier Unit Price 1
			1				
			1				
[NoValue].1			2				
C1, C2, C5, C6, C10, C11, C13, C14, C15, C19, C20	16V 100nF X7R ±10% 0402 MULTILAYER CERAMIC CAPACITORS MLCC - SMD/SMT ROHS	dsCapPassive_Cap0402_100nF_-10%_16V_X7R_Samsung_CL	11	C1525	Install	CLO5B104K05NNNC	
C3, C7	10V 4.7uF X5R ±20% 0402 MULTILAYER CERAMIC CAPACITORS MLCC - SMD/SMT ROHS	dsCapPassive_Cap0402_4.7uF_-20%_10V_X5R_Samsung_CL	2	C23733	Install	CLO5A475MP5NRNC	
C4, C12	6.3V 10uF X5R ±20% 0402 MULTILAYER CERAMIC CAPACITORS MLCC - SMD/SMT ROHS	dsCapPassive_Cap0402_10uF_-20%_6.3V_X5R_Samsung_CL	2	C15525	Install	CLO5A106M05NUNC	
C8, C9, C16, C17, C18	25V 1uF X5R ±10% 0402 MULTILAYER CERAMIC CAPACITORS MLCC - SMD/SMT ROHS	dsCapPassive_Cap0402_1uF_-10%_25V_X5R_Samsung_CL	5	C52923	Install	CLO5A105KA5NQNC	
D1, D2, D3	7.8V Clamp 1A (8/20us) Ipp Tvs Diode Surface Mount SOD-923	dsDiode_TVS_ESD983.3ST5G_ONSem	3	C233388	Install	ESD983.3ST5G	
ESP1	EmStat Pico	EmStat Pico	1				
J2	USB - Type C Female 16.844" 3mm USB Connectors RoHS	dsEMech_Conn_USB-Type-C-31-M-12	1	C165948	Install	TYPE-C-31-M-12	
J3	Connector Header Surface Mount, Right Angle, 2 position 0.047" (1.20mm)	dsConn_W2B_2POS_JST_ACH	1		Install	BM02B-ACHSS-GAN-TF	
LED1	Yellow 589nm LED Indication - Discrete 2V 0603 (1608 Metric)	dsDiode_LED0603_Yellow_5mA_1.7V_Everlight	1	C72038	Install	19-213/Y2C-CQ2R2L/3T	
MOD1	BL653 Integrated Antenna module .453 0059	Laird BL653u	1			453-00059	
R1, R18, R19	33kO 1/16W Thick Film Resistors 50V ±1%±200ppm/°C -55°C~+15°C 0402 Chip Resistor - Surface Mount ROHS	dsPassive_Res0402_33k_1%_UNI-ROYAL	3	C25779	Install	0402WGF3302TCE	
R2	1.8MΩ 1/16W Thick Film Resistors 50V ±1%±200ppm/°C -55°C~+15°C 0402 Chip Resistor - Surface Mount ROHS	dsPassive_Res0402_1.8M_1%_UNI-ROYAL	1	C38587	Install	0402WGF1804TCE	
R3	300kΩ 1/16W Thick Film Resistors 50V ±1%±200ppm/°C -55°C~+15°C 0402 Chip Resistor - Surface Mount ROHS	dsPassive_Res0402_300k_1%_UNI-ROYAL	1	C25774	Install	0402WGF3003TCE	
R4, R5, R6	12kΩ 1/16W Thick Film Resistors 50V ±1%±200ppm/°C -55°C~+15°C 0402 Chip Resistor - Surface Mount ROHS	dsPassive_Res0402_12k_1%_UNI-ROYAL	3	C25752	Install	0402WGF1202TCE	
R7	3.3kΩ 1/16W Thick Film Resistors 50V ±1%±200ppm/°C -55°C~+15°C 0402 Chip Resistor - Surface Mount ROHS	dsPassive_Res0402_3.3k_1%_UNI-ROYAL	1	C25890	Install	0402WGF3301TCE	
R8	680Ω 1/16W Thick Film Resistors 50V ±1%±200ppm/°C -55°C~+15°C 0402 Chip Resistor - Surface Mount ROHS	dsPassive_Res0402_680_1%_UNI-ROYAL	1	C25130	Install	0402WGF6800TCE	
R9, R10, R11, R12, R13	5.1kΩ 1/16W Thick Film Resistors 50V ±1%±200ppm/°C -55°C~+15°C 0402 Chip Resistor - Surface Mount ROHS	dsPassive_Res0402_5.1k_1%_UNI-ROYAL	5	C25905	Install	0402WGF5101TCE	
U1	Charger Li Lithium Ion TSOT-23-5	dsIC_BM_LTC4054ESS-4.2_AD	1	C462648	Install	LTC4054ESS-4.2#TRPBF	
U2	Accelerometer X, Y, Z Axis ±2g, 4g, 8g, 16g 0.5Hz ~ 67Hz 12-LGA (2x2)	dsIC_Accel_Lis2DH12TR_STM	1	C110926	Install	LIS2DH12TR	
U3	EEPROM Memory IC 64kB (8x8) PC 1 Mhz 450 ns 8-SOIC	dsIC_EEPROM_M24C64-RMN6TP_STM	1	C79988	Install	M24C64-RMN6TP	
U4	FLASH - NOR Memory IC 128Mb (16Mx8) SPI - Quad I/O, QPI, DTR 133MHz 8-SOIC	dsIC_FLASH_W25Q128JVSIQ_Windbond	1	C97521	Install	W25Q128JVSIQ	
U5	Power Switch/Driver 2:1 P-Channel 1.5A 6-WL CSP (0.96x1.66)	dsIC_SWITCH_FPF1320UCK_OnSemi	1	C457734	Install	FPF1320UCK	
VR1	Linear Voltage Regulator IC Positive Fixed 1 Output 150mA TSOT-23-5	dsIC_LDO_3.3V_ADP165_AD	1			ADP165AUJZ-3.3-R7	

## Electrical Rules Check Report

Class	Document	Message
Warning	Project Overview.SchDoc	Nets Wire +3.3V has multiple names (Net Label nRF_SWD.VTG (4), Power Object +3.3V (13), Sheet Entry DEBUG-nRF_SWD.VTG(Passive), Sheet Entry MCU-nRF_SWD.VTG(Passive))
Warning	Project Overview.SchDoc	Nets Wire Accel_INT1 has multiple names (Net Label Accel_INT1 (2), Sheet Entry MCU-Accel_INT1(Input), Sheet Entry USER INPUT-ACCELINT2(Output))
Warning	Project Overview.SchDoc	Nets Wire Accel_INT2 has multiple names (Net Label Accel_INT2 (2), Sheet Entry MCU-Accel_INT2(Input), Sheet Entry USER INPUT-ACCELINT1(Output))
Warning	Project Overview.SchDoc	Nets Wire DGND has multiple names (Net Label nRF_SWD.GND (2), Net Label nRF_USB2-0.GND (2), Power Object DGND (48), Sheet Entry DEBUG-nRF_SWD.GND(Passive), Sheet Entry MCU-nRF_SWD.GND(Passive), Sheet Entry
Warning	Project Overview.SchDoc	Nets Wire nRF_PICOUART.nDWN has multiple names (Net Label nRF_PICOUART.nDWN (3), Net Label nRF_UART.hDWN (3), Sheet Entry AFE-nRF_PICOUART.nDWN(Passive), Sheet Entry MCU-nRF_PICOUART.nDWN(Passive))
Warning	Project Overview.SchDoc	Nets Wire nRF_PICOUART.nRST has multiple names (Net Label nRF_PICOUART.nRST (3), Net Label nRF_UART.nRST (3), Sheet Entry AFE-nRF_PICOUART.nRST(Passive), Sheet Entry MCU-nRF_PICOUART.nRST(Passive))
Warning	Project Overview.SchDoc	Nets Wire nRF_PICOUART.RX has multiple names (Net Label nRF_PICOUART.RX (3), Net Label nRF_UART.RX (3), Sheet Entry AFE-nRF_PICOUART.RX(Passive), Sheet Entry MCU-nRF_PICOUART.RX(Passive))
Warning	Project Overview.SchDoc	Nets Wire nRF_PICOUART.TX has multiple names (Net Label nRF_PICOUART.TX (2), Net Label nRF_UART.TX (4), Sheet Entry AFE-nRF_PICOUART.TX(Passive), Sheet Entry MCU-nRF_PICOUART.TX(Passive))
Warning	Project Overview.SchDoc	Nets Wire nRF_USB2-0.D_N has multiple names (Net Label nRF_USB2-0.D_N (2), Net Label nRF_USB.D_N (6), Sheet Entry MCU-nRF_USB2-0.D_N(Passive), Sheet Entry POWER-nRF_USB2-0.D_N(Passive))
Warning	Project Overview.SchDoc	Nets Wire nRF_USB2-0.D_P has multiple names (Net Label nRF_USB2-0.D_P (2), Net Label nRF_USB.D_P (6), Sheet Entry MCU-nRF_USB2-0.D_P(Passive), Sheet Entry POWER-nRF_USB2-0.D_P(Passive))
Warning	Project Overview.SchDoc	Nets Wire VBUS has multiple names (Net Label nRF_USB2-0.VBUS (2), Net Label nRF_USB.VBUS (2), Power Object VBUS (6), Sheet Entry MCU-nRF_USB2-0.VBUS(Passive), Sheet Entry POWER-nRF_USB2-0.VBUS(Passive))

# Design Rules Verification Report

Filename : C:\Users\SongDian\Desktop\dsc\_alpha4.1\Alpha4.1\rev0.PcbDoc

Warnings 0  
Rule Violations 4

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=3.5mil) (All), (All)	0
Clearance Constraint (Gap=3.5mil) (HasFootprint("TC 2050")), (All)	0
Clearance Constraint (Gap=3.5mil) (All), (All)	0
Clearance Constraint (Gap=5mil) (InNet("DGND")), (InNet("+3.3V") OR InNet("VBUS") OR InNet("VIN"))	0
Short-Circuit Constraint (Allowed=No) (All), (All)	2
Un-Routed Net Constraint ( All )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=3.5mil) (Max=100mil) (Preferred=15.748mil) (InNet("DGND") OR InNet("+3.3V"))	0
Width Constraint (Min=3.5mil) (Max=100mil) (Preferred=3.5mil) (All)	0
Power Plane Connect Rule(Direct Connect )(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Power Plane Connect Rule(Relief Connect )(Expansion=11.811mil) (Conductor Width=4mil) (Air Gap=4mil) (Entries=4)	0
Minimum Annular Ring (Minimum=3mil) (All)	0
Hole Size Constraint (Min=7.874mil) (Max=248.031mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All), (All)	0
Minimum Solder Mask Sliver (Gap=0mil) (All), (All)	0
Silk To Solder Mask (Clearance=4mil) (IsPad), (All)	2
Silk To Silk (Clearance=0mil) (All), (All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) (All)	0
Matched Lengths(Tolerance=1000mil) (InDifferentialPair ('nRF_USB2-0.D'))	0
Height Constraint (Min=0mil) (Max=71497.938mil) (Preferred=500mil) (All)	0
Total	4

## Short-Circuit Constraint (Allowed=No) (All), (All)

Short-Circuit Constraint: Between Polygon Region (32 hole(s)) Bottom Copper And Text "12134" (679.724mil, 477.778mil) on Bottom Copper Location : [X =

Short-Circuit Constraint: Between Polygon Region (32 hole(s)) Bottom Copper And Text "Lorem Ipsum" (883.137mil, 189.786mil) on Bottom Copper

## Silk To Solder Mask (Clearance=4mil) (IsPad), (All)

Silk To Solder Mask Clearance Constraint: (3.655mil < 4mil) Between Pad C16-1(919.685mil, 1181.102mil) on Top Copper And Text "?"

Silk To Solder Mask Clearance Constraint: (1mil < 4mil) Between Pad R13-1(200.985mil, 775.787mil) on Top Copper And Text "?" (188.352mil, 797.852mil)