LUMIR
Harmony in Differences

ETRI

Korea Lunar Exploration Program

DTN Payload Thermal Vacuum Test Procedure

Date: 12 March. 2019

Doc. No: KPLO-D0-550-460
Issue: **1.0**
Total page: 54

Superseding Revised

Prepared By:

Sun-Ku Kim Date
DTN Engineer, Lumir

Reviewed By:

Chang-Soo Lee Date
DTN Product Assurance, Lumir

Dae-Soo Oh Date
DTN Project Manager, Lumir

Kyung-Rak Lee Date
DTN System Engineer, ETRI

Reviewed By:

Chol-Oh Jeong Date
DTN Product Assurance, ETRI

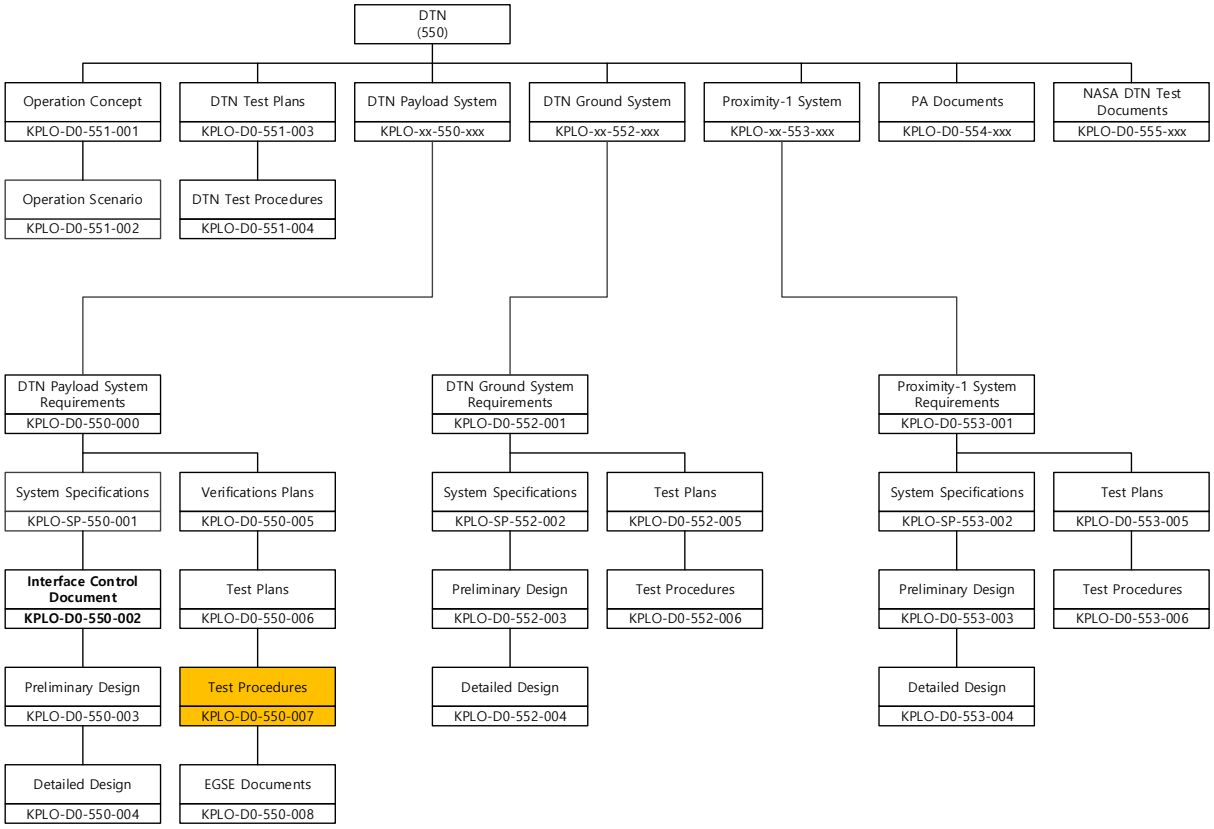
Jin-Ho Jo Date
DTN Project Leader, ETRI

Original CDMO Release_____

Revision History

Version	Author(s)	Date	Description
1.0	Sun-ku Kim	2019. 03. 12	Initial

Documents Tree



Contents

1. Introduction 8

1.1. Purpose and Scope 8

1.2. Applicable Documents 8

1.2.1. ETRI Documents 8

1.2.2. Reference Documents 8

1.3. Abbreviations 8

2. Test Article 10

2.1. DTNPL Configurations 10

2.1.1. CON_PWR 10

2.1.2. CON_COMM 10

2.1.3. CON_DEBUG 11

2.2. Verification Cross Reference 12

2.3. Notification for Qualification and Acceptance Test 12

3. Test Condition 13

3.1. Test Personal 13

3.2. Precaution and Warnings 14

4. Test Setup 15

4.1. Test Facility 15

4.2. Thermal Vacuum Chamber Setup 15

4.3. Test Preparation 15

4.3.1. Control and Measuring Equipment 15

5. Test Description 17

5.1. Thermal Vacuum Test Levels 17

5.2. Temperature Profile 17

5.3. Test Parameters 18

6. Test 19

6.1. Test Procedure 19

6.2. Test preparation 24

6.3. Ambient Test Before Thermal Vacuum Test 25

6.4. Highest Non-Operational Temperature 26

6.5. First Hot Plateau 27

6.6. Lowest Non-Operational Temperature 28

6.7. First Cold Plateau 29

6.8. Intermediate Cycle 30

6.8.1. 2nd Cycle 30
6.8.2. 3rd Cycle 32
6.8.3. 4th Cycle 34
6.8.4. 5th Cycle 36
6.8.5. 6th Cycle 38
6.8.6. 7th Cycle 40
6.8.7. 8th Cycle 42
6.8.8. 9th Cycle 44
6.9. Last Hot Plateau 46
6.10. Last Cold Plateau 47
6.11. Back to Ambient Temperature 48
6.12. Functional Test After Thermal Vacuum Test 49
6.13. Remove DTNPL From Chamber 50
7. Test Conclusion 50

Figures

Figure 2-1 DTNPL Configurations ---------- 10
Figure 2-2 Power Connector ---------- 10
Figure 2-3 Commend Connector ---------- 11
Figure 2-4 Debug Connector ---------- 12
Figure 4-1 Thermal Vacuum Chamber Layout ---------- 15
Figure 4-2 Location of Thermal Sensors ---------- 16
Figure 5-1 Temperature Design and Test Limits ---------- 17
Figure 5-2 Timeline for Thermal Cycle Profile ---------- 18

Tables

Table 4-1 Control Thermal Sensors ---------- 16
Table 4-2 Measurement Thermal Sensors ---------- 16
Table 5-1 DTNPL Test Temperature Limits ---------- 17

1. Introduction

1.1. Purpose and Scope

This document defines the Thermal Vacuum test procedure DTN payload of KPLO.

The purpose of this is to demonstrate that the DTN payload is working as expected under the required environmental conditions. During the Thermal Test a representative collection of functionality and performance test will be performed to check interfaces and hardware related functions.

1.2. Applicable Documents

1.2.1. ETRI Documents

	Document Number	Document Title
AD01	KPLO-D0-550-000	System Requirement of DTN Payload
AD02	KPLO-D0-550-001	System Specification of DTN Payload
AD03	KPLO-SP-320-002	KPLO Environmental Design and Test Specification

1.2.2. Reference Documents

	Document Number	Document Title
RD01	MIL-STD-1540C	Test Requirements for Launch, Upper-Stage, and Space Vehicles
RD02	PSS-01-801	Test Requirements Specification for Space Equipment
RD03	ECSS-E-10-03-A	ECSS Space Engineering-Testing

1.3. Abbreviations

AMS	Asynchronous Message Service
BP	Bundle Protocol
BSS	Bundle Streaming Service
CCSDS	Consultative Committee for Space Data Systems
CFDP	CCSDS File Delivery Protocol
DCC	DTN Control Center
CRC	Cyclical Redundancy Check
DMA	Direct Memory Access
DTN	Delay(Disruption) Tolerant Network
DTNPL	DTN Payload
EOD	End of Data
EOF	End of File
FW	Firm Ware
FSW	Flight Software
ION	Interplanetary Overlay Network

KDSA	Korea Deep Space Antenna
KPLO	Korea Pathfinder Lunar Orbiter
LCM	Lander Communication Model
LTP	Licklider Transmission Protocol
MOC	Mission Operation Center
OBC	On Board Computer
OBT	On Board Time
PDHU	Payload Data Handling Unit
RCM	Rover Communication Model
RFU	Reserved for Future Use
SBC	Single Board Computer
SOD	Start of Data
SOF	Start of File
SOH	Start of Head
TBC	To Be Confirmed
TBD	To Be Defined
TC	Tele-command
TCP	Transmission Control Protocol
TM	Telemetry
UART	Universal Asynchronous Receiver Transmitter
USRT	Universal Synchronous Receiver Transmitter

2. Test Article

The Objective of this Thermal Vacuum test is to demonstrate compliance of the DTNPL Requirements Specification [AD 03]

This test procedure shall be used for test of the DTNPL QM.

The test procedure is written such that results and other information shall be filled into it.

2.1. DTNPL Configurations

The unit under test is shown in the following figures :

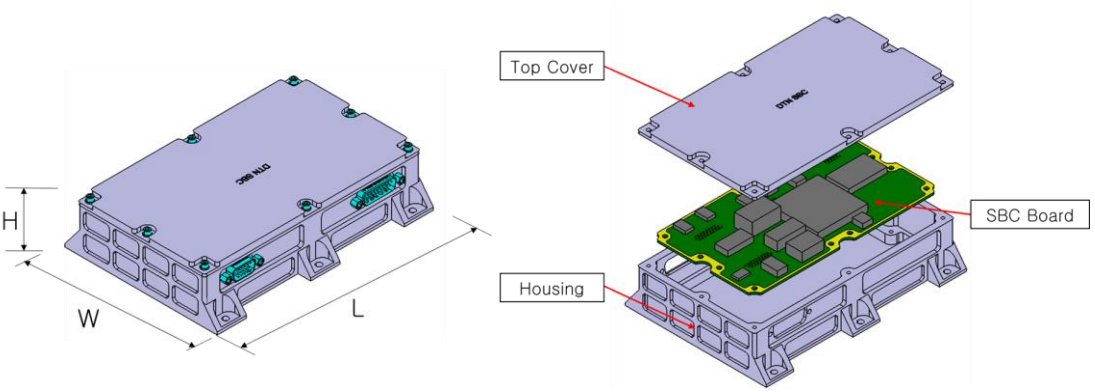


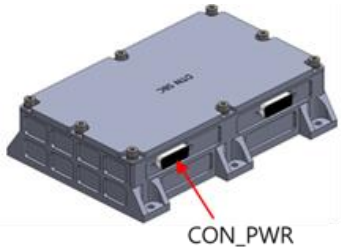
Figure 2-1 DTNPL Configurations

Dimension: 120 x 170 x 39 ㎜

Weight: 1.23 kg

2.1.1. CON_PWR

- Power Input (2 lines for +28V, 2 lines for RTN)



Pin	Description	Pin	Description	Pin	Description
1	DTNPL_+28V	6	(Reserved)	11	DTNPL_+28V_rtn
2	DTNPL_+28V	7	(Reserved)	12	DTNPL_+28V_rtn
3		8	(Reserved)	13	
4		9	(Reserved)	14	
5		10	(Reserved)	15	

Figure 2-2 Power Connector

2.1.2. CON_COMM

- 1 UART for OBC
- 2 USRT for PDHU(P/R)

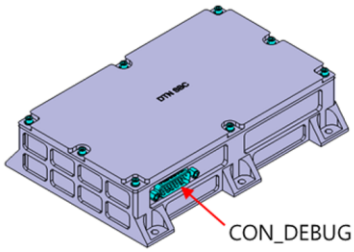
- 1 Bi-level Status for OBC
- 1 Bi-level Command for OBC

Pin	Description	Pin	Description	Pin	Description
1	DTNPL_UART_SBMU_Tx_DTNPL_Rx_P	10	DTNPL_PDHUp_Rx_DTNPL_TxEn_P	19	(Reserved)
2	DTNPL_UART_SBMU_Tx_DTNPL_Rx_N	11	DTNPL_PDHUp_Rx_DTNPL_TxEn_N	20	(Reserved)
3	DTNPL_UART_SBMU_Rx_DTNPL_Tx_P	12	(Reserved)	21	(Reserved)
4	DTNPL_UART_SBMU_Rx_DTNPL_Tx_N	13	DTNPL_PDHU_Rx_DTNPL_TxData_P	22	(Reserved)
5	(Reserved)	14	DTNPL_PDHU_Rx_DTNPL_TxData_N	23	DTNPL_STATUS
6	DTNPL_PDHUp_Rx_DTNPL_TxData_P	15	DTNPL_PDHUr_Rx_DTNPL_TxClk_P	24	DTNPL_STATUS_rtn
7	DTNPL_PDHUp_Rx_DTNPL_TxData_N	16	DTNPL_PDHUr_Rx_DTNPL_TxClk_N	25	DTNPL_RESET
8	DTNPL_PDHUp_Rx_DTNPL_TxClk_P	17	DTNPL_PDHUr_Rx_DTNPL_TxEn_P	26	DTNPL_RESET_rtn
9	DTNPL_PDHUp_Rx_DTNPL_TxClk_N	18	DTNPL_PDHUr_Rx_DTNPL_TxEn_N		

Figure 2-3 Commend Connector

2.1.3. CON_DEBUG

- 1 JTAG for Firmware Uploading
- 1 RS422 for Debugging UART
- 1 SpaceWire for Image Uploading, 40 Mbps (TBR)
- 1 GPIO for Debugging
- 1 SPI for DT10 (S/W Test Platform)



Pin	Description	Pin	Description	Pin	Description
1	DTNPL_JTAG_TDI	10	DTNPL_DBD_SpW_TxDp	19	DTNPL_UART422_TXp
2	DTNPL_JTAG_TDO	11	DTNPL_DBD_SpW_TxDn	20	DTNPL_UART422_TXn
3	DTNPL_JTAG_TCK	12	DTNPL_DBD_SpW_TxSp	21	DTNPL_UART422_RXp
4	DTNPL_JTAG_TMS	13	DTNPL_DBD_SpW_TxSn	22	DTNPL_UART422_RXn
5	DTNPL_JTAG_TRSTB	14	DTNPL_DBD_SpW_RxDp	23	DTNPL_DT10_SCK
6	DTNPL_JTAG_GND	15	DTNPL_DBD_SpW_RxDn	24	DTNPL_DT10_SDI
7	DTNPL_JTAG_GND	16	DTNPL_DBD_SpW_RxSp	25	DTNPL_DT10_nCS
8	DTNPL_JTAG_+3.3V	17	DTNPL_DBD_SpW_RxSn	26	DTNPL_DT10_CNG
9	DTNPL_JTAG_+3.3V	18	DTNPL_GPIO		

Figure 2-4 Debug Connector

2.2. Verification Cross Reference

The requirements which have to be verified by a successful performance in the test and its relevant test steps are given below:

Applicable Doc.	Requirement	Verified by Test Step	Compliance
KPLO-SP-320-002	Environmental Design and Test Specification	All	C

2.3. Notification for Qualification and Acceptance Test

This test procedure shall be approved by the ETRI prior to performance of the test, either by signature on cover page of by performance of a dedicated Test Readiness Review(TRR).

3. Test Condition

3.1. Test Personal

The personnel required for the performance of the test is listed below:

Test Engineers

The test engineers are responsible for :

- Operation of measuring instrumentation, data acquisition, data handling, data recording
- Identification and compilation of data sheet
- Safety precaution for test articles
- Test personnel to be present in the test area
- The accuracy of the measured values & Data report

Test Manager

The test manager is responsible for :

- Test articles and technical aspects of the test performance
- Record the correct software version for test article and EGSE
- Examination of disturbances
- Test article Integration and handling
- Test performance
- Evaluation of test results & Providing of test reports

Quality Assurance Engineer

The QA engineer is responsible for :

- Surveillance of test equipment according to regulations as well as the test procedure
- Statement that the test articles to be tested have passed all checks before testing
- Checking the identification markings on the test articles
- Supervision of the proceeding with respect to quality assurance performance

The customer has the fight to participate or observe the test

Responsibility	Company /Dep.	Name
Test Engineer	Lumir / R&D	Sun-ku Kim
Test Manager	Lumir / R&D	Dae-Soo Oh
Quality Assurance Engineer	Lumir / PA	Chang-Soo Lee
Facility Engineer / Operator	KASI / Engineer	

3.2. Precaution and Warnings

For all testing and handling, Environmental requirements concerning personnel, facilities and test equipment shall be regarded.

No special hazard exists during the test.

The following precautions apply:

- Only trained personnel are allowed to handle the test specimen.
- A test cable or breakout box shall never be connected of disconnected when the test specimen is powered.
- Correct set-up of the test equipment has to be checked carefully prior to the connection/switch-on of flight hardware, e.g. bonding, grounding, voltages, current limiters, etc.
- The test specimen shell be protected by a clean, antistatic bag all the time no activities are performed at the hardware.

4. Test Setup

4.1. Test Facility

The DTNPL test will be performed at the Thermal Vacuum facility. Thermal Vacuum chamber provides the anechoic chamber.

4.2. Thermal Vacuum Chamber Setup

For Thermal Vacuum Test the following setup will be used:

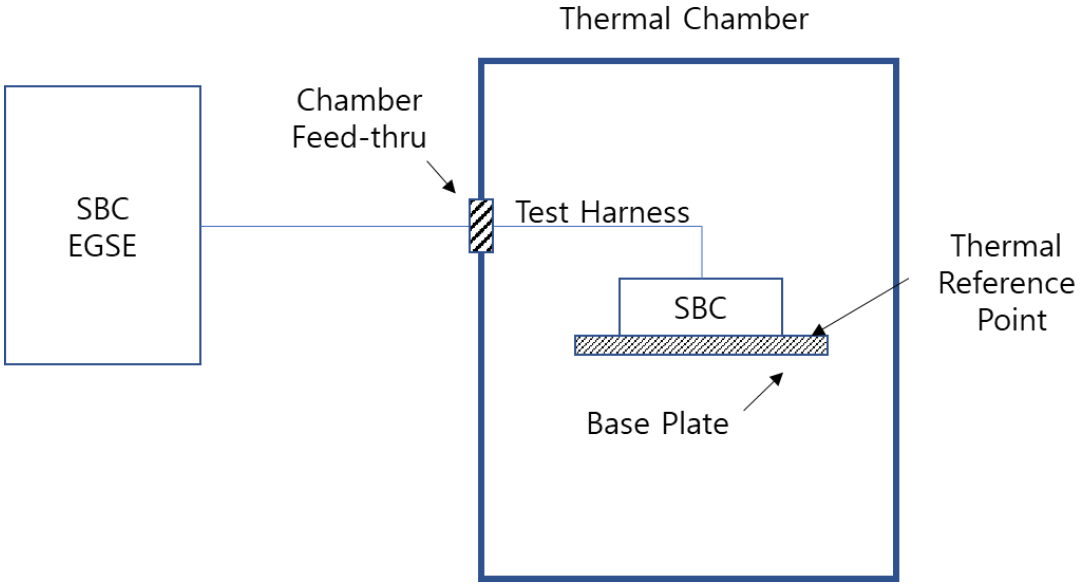


Figure 4-1 Thermal Vacuum Chamber Layout

Following Software will be used for Thermal Vacuum Test

- Software : KPLO_DTN_EGSE_SW.exe
- Version : v1.0:

4.3. Test Preparation

The test harness shall be connected from DTNPL EGSE to the DTNPL through the Thermal Vacuum Chamber feed-thru. During the test, the DTNPL shall be operated in representative manner
(i.e. data are transferred via all interfaces and stored).

4.3.1. Control and Measuring Equipment

The thermal plate and the DTNPL unit will be equipped with temperature sensors(Thermocouples) on the positions defined in the descriptions below. The actual sensor positions will be noted after fixing on the equipment as given in the sensor location plan at the following tables:

Table 4-1 Control Thermal Sensors

No.	Position	Remark
C1	Base Plate	Defined by Test Engineer
C2	Base Plate (optional)	Defined by Test Engineer

Table 4-2 Measurement Thermal Sensors

No	Position	Remark
T1	DTNPL Top Cover	
T2	DTNPL Case Side	

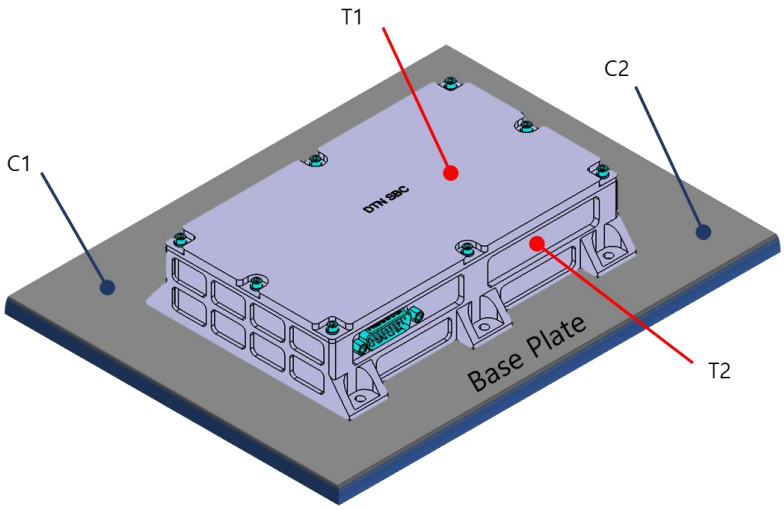


Figure 4-2 Location of Thermal Sensors

5. Test Description

5.1. Thermal Vacuum Test Levels

The nominal sequence of the thermal cycles is depicted in and temperature range for tests are summarized in

Table 5-1 DTNPL Test Temperature Limits

Equipment	Temperature Limits (degree C)						
	Proto-flight (Operating) Range		Cold Turn-On	Acceptance (Operating) Range		Survival (Non-Operating) Range	
	Min	Max		Min	Max	Min	Max
DTNE_DTNPL	-30	60	-30	-20	50	-35	70

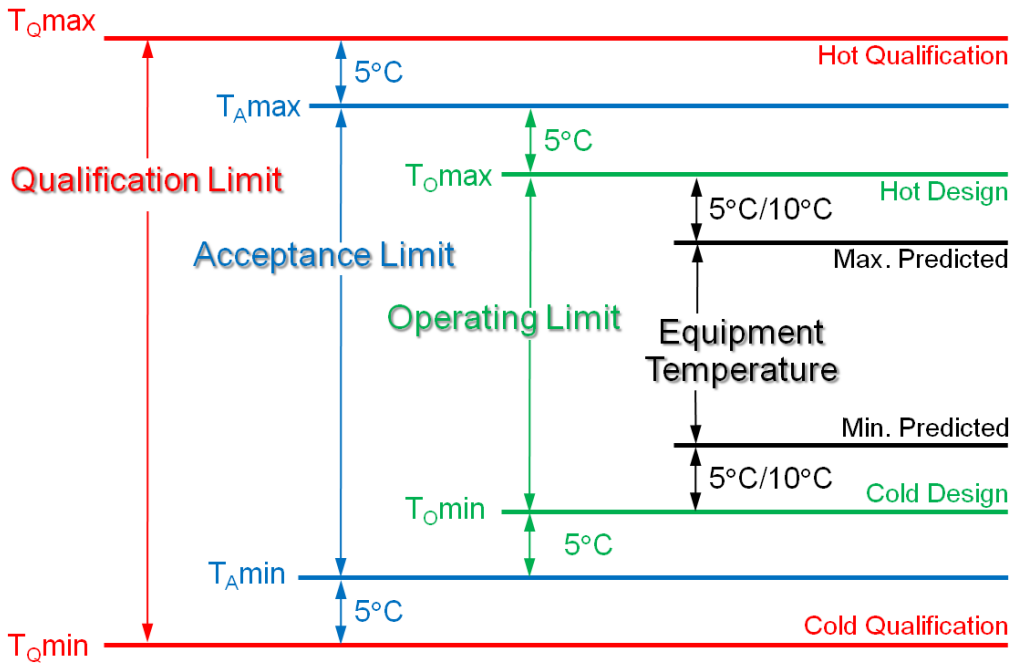


Figure 5-1 Temperature Design and Test Limits

5.2. Temperature Profile

The DTNPL shall be subjected to temperature cycles as described in the following figure. DTNPL operation over the range of temperatures shall be demonstrated at specific points during the thermal cycling test according to the following figure.

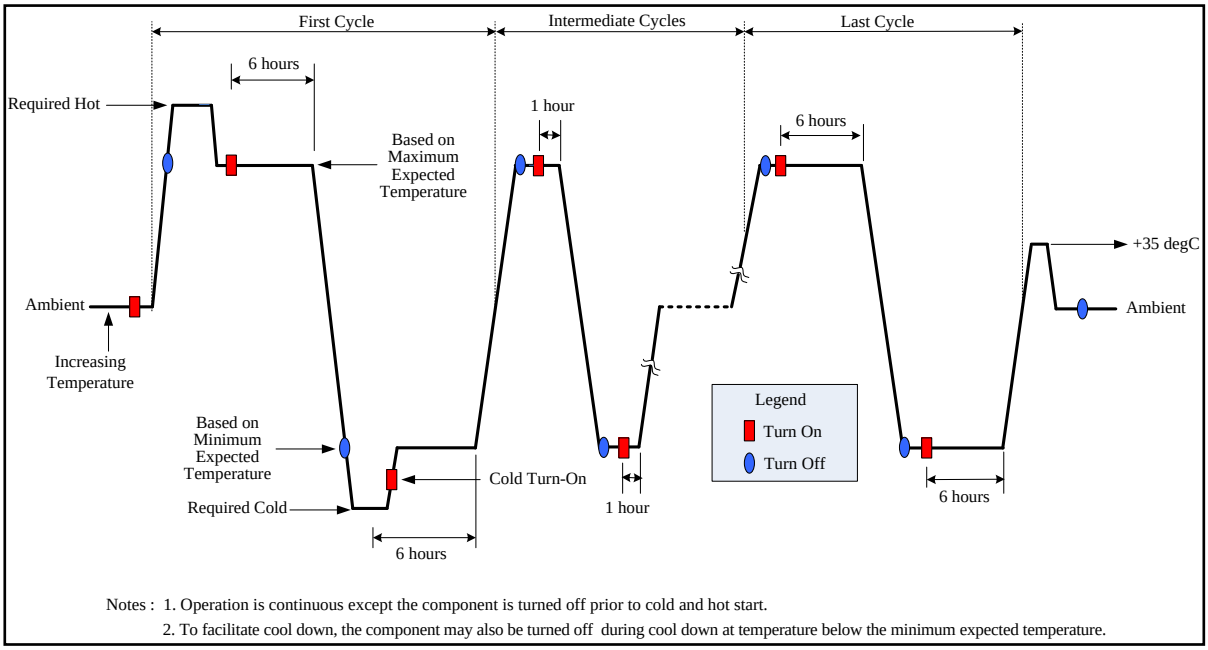


Figure 5-2 Timeline for Thermal Cycle Profile

5.3. Test Parameters

The following test parameters shall apply:

Temperature range : As defined in the applicable equipment specification and Table 5-1

Temperature exposure : As described in Table 5-1 and Figure 5-2

6. Test

The DTNPL shall have a full functional test performed at ambient temperature prior to beginning the thermal cycling test. Thermal soak duration shall be at least 6 hours at the hot temperatures and 6 hours at the cold temperatures during the first and last cycle (Figure 5-2). Intermediate cycles shall give at least 1 hour soak at the hot and cold temperatures. During the thermal soak, the unit shall be turned off until the temperature stabilizes and turn on. Remaining on until the next soak period off on sequence. Measurement of thermal soak duration shall begin at the time of unit turn on (Figure 5-2).

Functional tests shall be conducted after the DTNPL temperature have stabilized at hot and cold temperatures during the first and last thermal cycle, and after return to ambient. During the remainder of the test, electrical and electronic units, including all redundant circuits and paths, shall be cycled through various operation modes. DTNPL shall meet their performance requirements within specification over the maximum expected temperature range extended at both temperatures by 10°C. The final thermal cycle should employ a sufficiently slow temperature transition to permit a complete functional check to be repeated at essentially all temperatures.

Moisture condensation in side of DTNPL shall be prevented.

6.1. Test Procedure

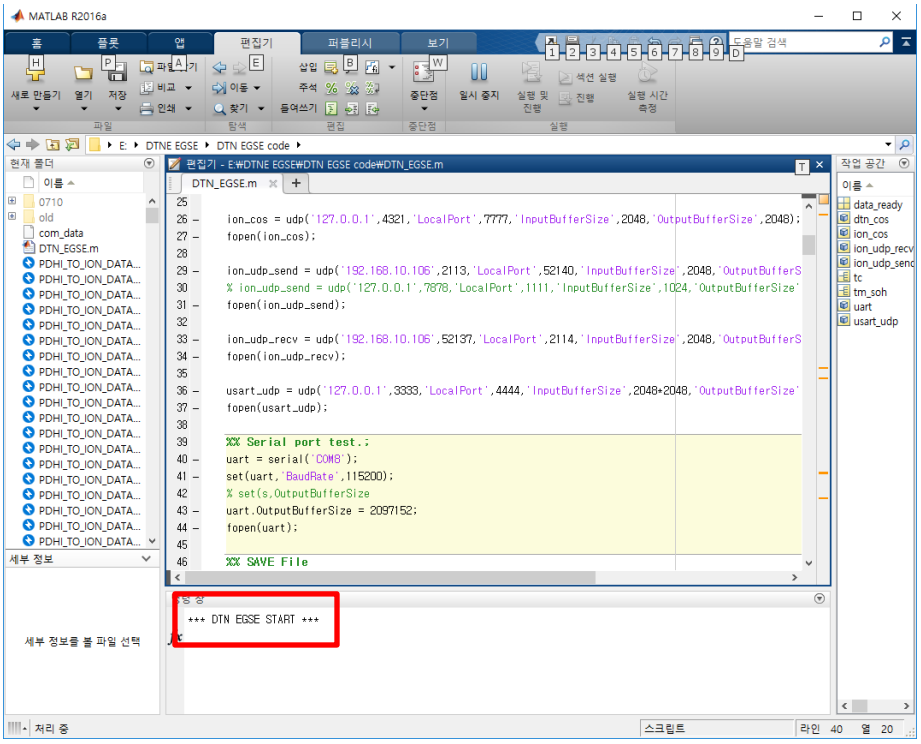
With feed assembly in the EMC Chamber, the functional test should be performed at the ambient condition in accordance with the following sequence and record the test results per the indicated method.

(1) Power Input

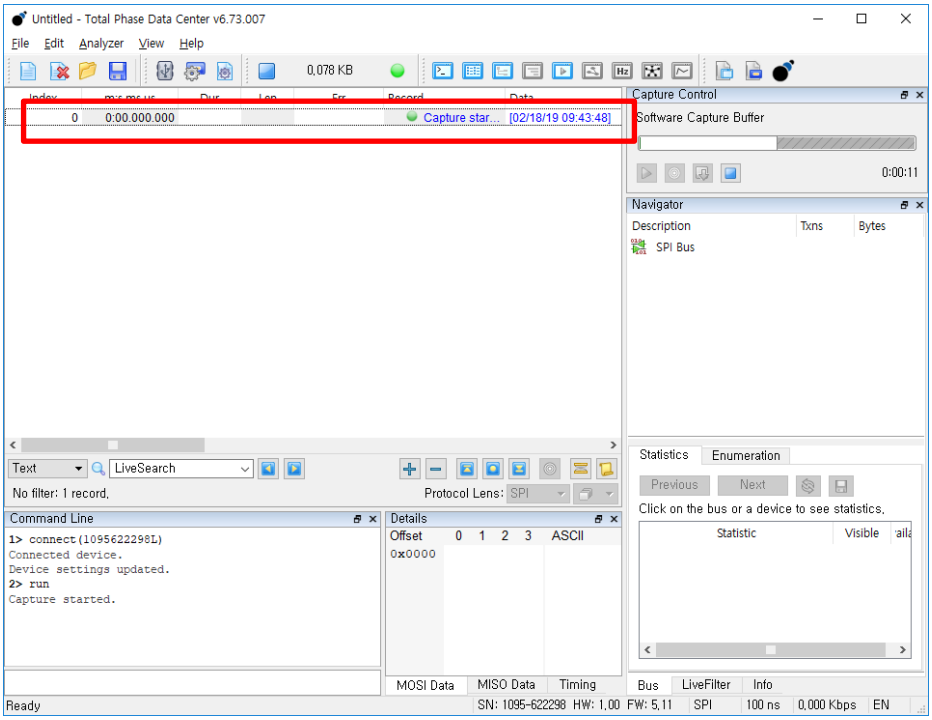
A. Nominal Voltage : 28V

B. Nominal Current < 0.50A

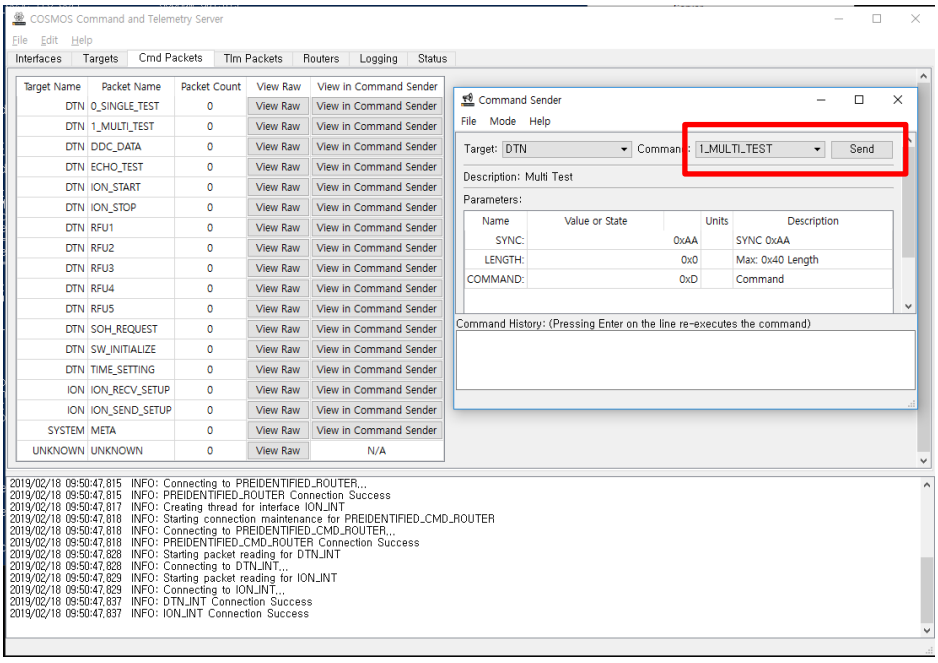
(2) MATLAB DTN_EGSE.m execution PASS



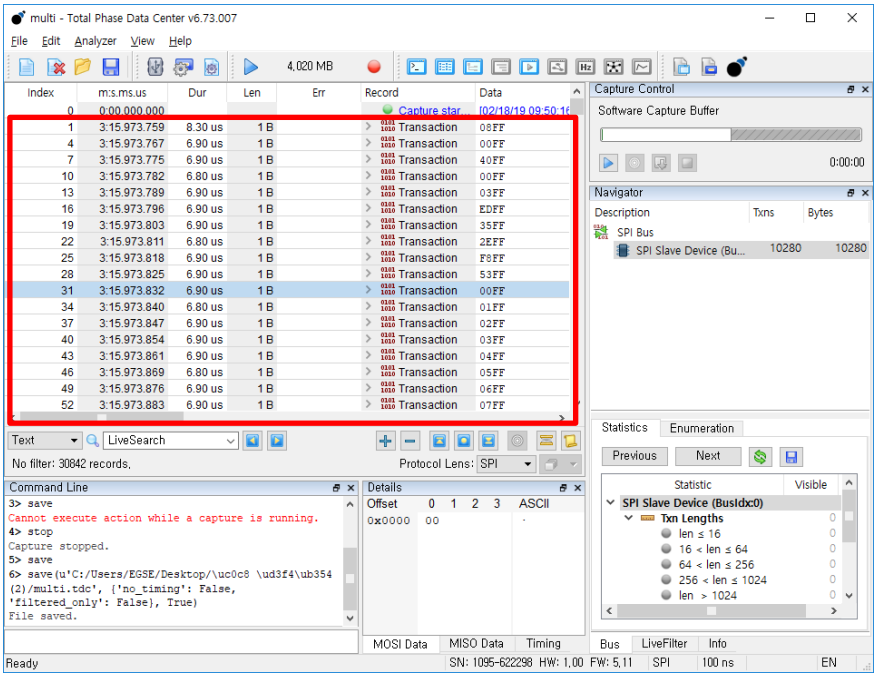
(3) Set up environment to receive data by running 'Data Center' Software.



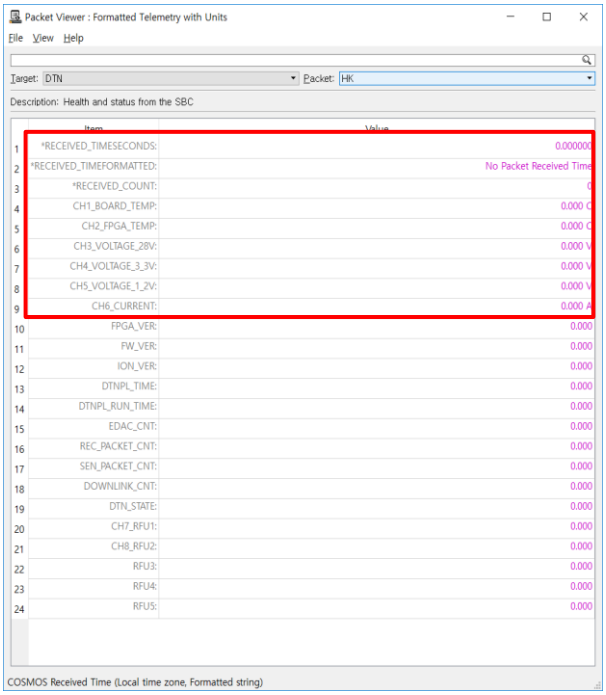
(4) After COSMOS Software execution, In the cmd packet window, select '1_MULTI_Test and click the send button.



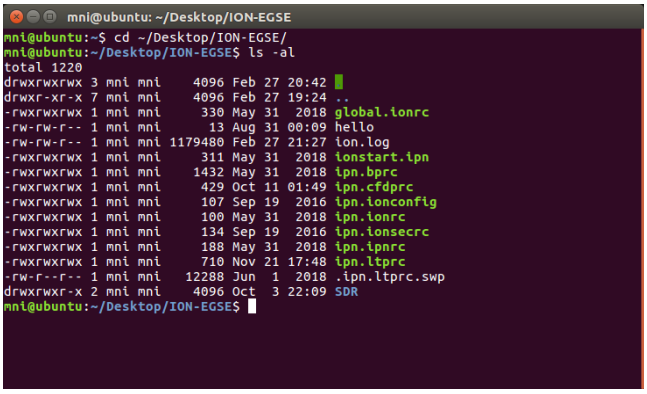
(5) Storing data when data comes in 'Data center' Software.



(6) Send SOH request by COSMOS and check the value of SOH.

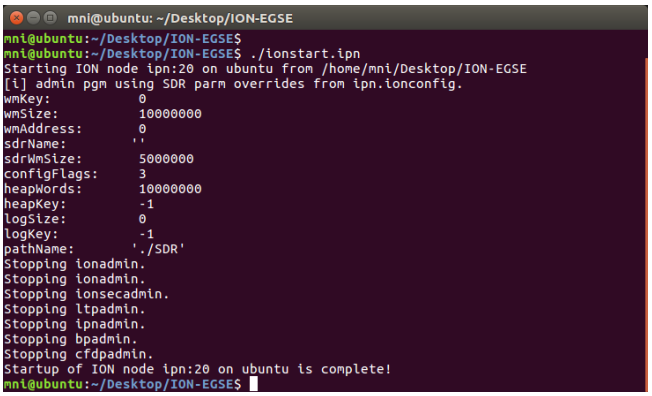


(7) Run ION software on ION-EGSE



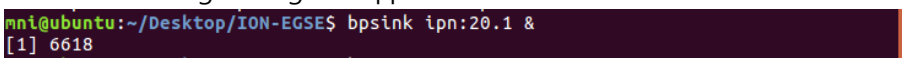
(8) Go to "~/Desktop/ION-EGSE" path (having ION resource file)

- cd ~/Desktop/ION-EGSE



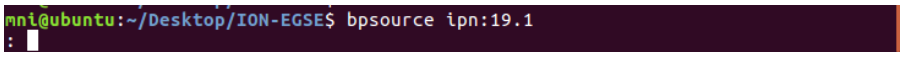
(9) Start ION software using "ionstart.ipn" script file

- ./ionstart.ipn
- Send & Receive messages using ION application



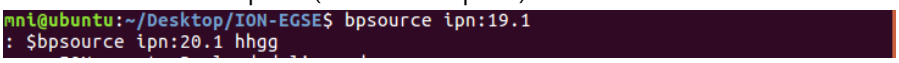
(10) Run bpsink program on background

- bpsink i-pn:20.1 &
- "bpsink" is ION message receive application
- "ipn:20.1" is own endpoint (ION-EGSE's end point)



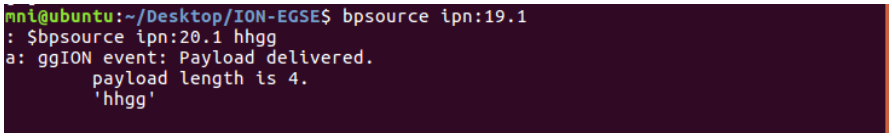
(11) Run bpsource program

- bpsource ipn:19.1
- "bpsource" is ION message send application
- "ipn:19.1" is destination endpoint (DTNPL's end point)



(12) Send command message

- $bpsource ipn:20.1 'text'
- Command message adds $ ($ + Commnad)



(13) Receive message from DTNPL

- DTNPL sends message using bpsource
- ION-EGESE receives message using bpsink

6.2. Test preparation

Start Date : _____ / Time : _____

(1)	Fill out test environment conditions	Pass / Fail	Sign
(2)	Fill out test personnel	Pass / Fail	Sign
(3)	Check test articles and fill out, check, and sign Test Article list above	Pass / Fail	Sign
(4)	Check test equipment and fill out, check, Test Equipment list above setup complete	Pass / Fail	Sign
(5)	Power off for each test article and test equipment switched off Install DTNPL in Thermal Vacuum Cycling chamber	Pass / Fail	Sign
(6)	Mount DTNPL onto the base plate by fixing of screws.	Pass / Fail	Sign
(7)	Attach temperature sensors according to chapter 4.4.1	Pass / Fail	Sign
(8)	Check that connector savers installed on all used interfaces	Pass / Fail	Sign
(9)	Connect harness to DTNPL and connect harness to chamber feed- through	Pass / Fail	Sign
(10)	Take pictures of the mounted DTNPL when ready for thermal cycling test	Pass / Fail	Sign
(11)	Start recording temperature measurement points and chamber temperature continuously	Pass / Fail	Sign
(12)	Correlate time, Temperature and test results exactly	Pass / Fail	Sign

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

6.3. Ambient Test Before Thermal Vacuum Test

Start Date: _____ / Time: _____

Temperature: _____℃ (19 ~ 25℃)

Humidity: _____% (35 ~ 55℃)

With feed assembly in the thermal chamber, the functional test should be performed at the ambient condition in accordance with the following sequence and record the test results per the indicated method.

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

6.4. Highest Non-Operational Temperature

Start Date: _____ / Time: _____

(1) Increase the temperature in the T/C chamber to the maximum test temperature(+70℃)

(2) Turn off DTNPL at + 60℃ during thermal transition
Turn off time: _____

(3) Wait until the temperature of Thermal Chamber reaches +70℃

	Temperature			
	C1	C2	T1	T2
Start				
End				

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

6.5. First Hot Plateau

Start Date: _____ / Time: _____

(1) Start thermal transition setting to Temperature(+60℃)

	Temperature			
	C1	C2	T1	T2
Start				
End				

(2) Wait until the temperature of the Thermal Chamber reaches +60℃ and switch DTNPL on.
Turn on time: _____

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(3) Hold temperature for at least 6 hours.

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

6.6. Lowest Non-Operational Temperature

Start Date: _____ / Time: _____

(1) Start thermal transition by decreasing temp setting down to -35℃.

(2) Turn off DTNPL at -30℃ during thermal transition
Turn off time: _____

(3) Wait until the temperature of Thermal Chamber reaches -35℃

	Temperature			
	C1	C2	T1	T2
Start				
End				

(4) Hold temperature for at least 1 hour

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

6.7. First Cold Plateau

Start Date: _____ / Time: _____

(1) Start thermal transition by increasing temp setting up to -30℃.

(2) Turn on DTNPL at -30℃ during thermal transition
Turn on time: _____

(3) Wait until the temperature of the Thermal Chamber reaches -30℃

	Temperature			
	C1	C2	T1	T2
Start				
End				

(4) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(5) Hold temperature for at least 5 hours.

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

6.8. Intermediate Cycle

6.8.1. 2nd Cycle

Start Date: _____ / Time: _____

(1) Start thermal transition by increasing temp setting up to +60℃.

	Temperature			
	C1	C2	T1	T2
Start				
End				

(2) When base plate temperature reaches +60℃ switch DTNPL off
Turn off time: _____

(3) Hold temperature for at least 10 minutes and Turn on DTNPL
Turn on time: _____

(4) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(5) Hold temperature for at least 1 hour.

(6) Start thermal transition by decreasing temp setting down to -30℃.

(7) When Thermal Chamber reaches -30℃ switch DTNPL off
Turn off time: _____

(8) Hold temperature for 10 minutes and switch DTNPL on
Turn on time: _____

(9) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(10) Hold temperature for at least 1 hour.

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

6.8.2. 3rd Cycle

Start Date: _____ / Time: _____

(1) Start thermal transition by increasing temp setting up to +60℃.

	Temperature			
	C1	C2	T1	T2
Start				
End				

(2) When base plate temperature reaches +60℃ switch DTNPL off
Turn off time: _____

(3) Hold temperature for at least 10 minutes and Turn on DTNPL
Turn on time: _____

(4) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(5) Hold temperature for at least 1 hour.

(6) Start thermal transition by decreasing temp setting down to -30℃.

(7) When Thermal Chamber reaches -30℃ switch DTNPL off

Turn off time: _____

(8) Hold temperature for 10 minutes and switch DTNPL on

Turn on time: _____

(9) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(10) Hold temperature for at least 1 hour.

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

6.8.3. 4th Cycle

Start Date: _____ / Time: _____

(1) Start thermal transition by increasing temp setting up to +60℃.

	Temperature			
	C1	C2	T1	T2
Start				
End				

(2) When base plate temperature reaches +60℃ switch DTNPL off
Turn off time: _____

(3) Hold temperature for at least 10 minutes and Turn on DTNPL
Turn on time: _____

(4) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(5) Hold temperature for at least 1 hour.

(6) Start thermal transition by decreasing temp setting down to -30℃.

(7) When Thermal Chamber reaches -30℃ switch DTNPL off

Turn off time: _____

(8) Hold temperature for 10 minutes and switch DTNPL on

Turn on time: _____

(9) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(10) Hold temperature for at least 1 hour.

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

6.8.4. 5th Cycle

Start Date: _____ / Time: _____

(1) Start thermal transition by increasing temp setting up to +60℃.

	Temperature			
	C1	C2	T1	T2
Start				
End				

(2) When base plate temperature reaches +60℃ switch DTNPL off
Turn off time: _____

(3) Hold temperature for at least 10 minutes and Turn on DTNPL
Turn on time: _____

(4) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(5) Hold temperature for at least 1 hour.

(6) Start thermal transition by decreasing temp setting down to -30℃.

(7) When Thermal Chamber reaches -30℃ switch DTNPL off

Turn off time: _____

(8) Hold temperature for 10 minutes and switch DTNPL on

Turn on time: _____

(9) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(10) Hold temperature for at least 1 hour.

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

6.8.5. 6th Cycle

Start Date: _____ / Time: _____

(1) Start thermal transition by increasing temp setting up to +60℃.

	Temperature			
	C1	C2	T1	T2
Start				
End				

(2) When base plate temperature reaches +60℃ switch DTNPL off
Turn off time: _____

(3) Hold temperature for at least 10 minutes and Turn on DTNPL
Turn on time: _____

(4) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(5) Hold temperature for at least 1 hour.

(6) Start thermal transition by decreasing temp setting down to -30℃.

(7) When Thermal Chamber reaches -30℃ switch DTNPL off

Turn off time: _____

(8) Hold temperature for 10 minutes and switch DTNPL on

Turn on time: _____

(9) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(10) Hold temperature for at least 1 hour.

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

6.8.6. 7th Cycle

Start Date: _____ / Time: _____

(1) Start thermal transition by increasing temp setting up to +60℃.

	Temperature			
	C1	C2	T1	T2
Start				
End				

(2) When base plate temperature reaches +60℃ switch DTNPL off
Turn off time: _____

(3) Hold temperature for at least 10 minutes and Turn on DTNPL
Turn on time: _____

(4) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(5) Hold temperature for at least 1 hour.

(6) Start thermal transition by decreasing temp setting down to -30℃.

(7) When Thermal Chamber reaches -30℃ switch DTNPL off

Turn off time: _____

(8) Hold temperature for 10 minutes and switch DTNPL on

Turn on time: _____

(9) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(10) Hold temperature for at least 1 hour.

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

6.8.7. 8th Cycle

Start Date: _____ / Time: _____

(1) Start thermal transition by increasing temp setting up to +60℃.

	Temperature			
	C1	C2	T1	T2
Start				
End				

(2) When base plate temperature reaches +60℃ switch DTNPL off
Turn off time: _____

(3) Hold temperature for at least 10 minutes and Turn on DTNPL
Turn on time: _____

(4) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(5) Hold temperature for at least 1 hour.

(6) Start thermal transition by decreasing temp setting down to -30℃.

(7) When Thermal Chamber reaches -30℃ switch DTNPL off

Turn off time: _____

(8) Hold temperature for 10 minutes and switch DTNPL on

Turn on time: _____

(9) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(10) Hold temperature for at least 1 hour.

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

6.8.8. 9th Cycle

Start Date: _____ / Time: _____

(1) Start thermal transition by increasing temp setting up to +60℃.

	Temperature			
	C1	C2	T1	T2
Start				
End				

(2) When base plate temperature reaches +60℃ switch DTNPL off
Turn off time: _____

(3) Hold temperature for at least 10 minutes and Turn on DTNPL
Turn on time: _____

(4) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(5) Hold temperature for at least 1 hour.

(6) Start thermal transition by decreasing temp setting down to -30℃.

(7) When Thermal Chamber reaches -30℃ switch DTNPL off

Turn off time: _____

(8) Hold temperature for 10 minutes and switch DTNPL on

Turn on time: _____

(9) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(10) Hold temperature for at least 1 hour.

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

6.9. Last Hot Plateau

Start Date: _____ / Time: _____

(1) Start thermal transition setting to Temperature(+60℃)

	Temperature			
	C1	C2	T1	T2
Start				
End				

(2) Wait until the temperature of the Thermal Chamber reaches +60℃ and switch DTNPL on.
Turn on time: _____

(3) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(4) Hold temperature for at least 6 hours.

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

6.10. Last Cold Plateau

Start Date: _____ / Time: _____

(1) Start thermal transition by increasing temp setting up to -30℃.

(2) Turn on DTNPL at -30℃ during thermal transition
Turn on time: _____

(3) Wait until the temperature of the Thermal Chamber reaches -30℃

	Temperature			
	C1	C2	T1	T2
Start				
End				

(4) Perform short Functional Test of DTNPL

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(5) Hold temperature for at least 5 hours.

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

6.11. Back to Ambient Temperature

Start Date: _____ / Time: _____

(1) Start thermal transition by increasing temp setting up to +35℃.

(2) Check the temperature as it reaches +35℃.

(3) Hold temperature for at least 30 minutes.

(4) Start thermal transition by decreasing temp setting down to +25℃.

(5) Check the temperature as it reaches +25℃.

	Temperature			
	C1	C2	T1	T2
Start				
End				

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

6.12. Functional Test After Thermal Vacuum Test

Start Date: _____ / Time: _____

(1) Perform Functional test in '6.1 Test Procedure'

	Test Description	Nominal Value	Actual Value
(1)	Measure input voltage	Under 0.5A	
(2)	Measure input voltage	28V	
(3)	Perform Funtional test in '6.1 Test Procedure'	PASS	
(4)	Board Temperature		
(5)	FPGA Junction Temperature		
(6)	28V	28V ± 10%	
(7)	3.3V	3.3V ± 10%	
(8)	1.2V	1.2V ± 10%	
(9)	USRT Downlink simulation Test	PASS	
(10)	DTN Protocols simulation Test	PASS	

(2) Switch DTNPL off.
Turn off time: _____

(3) Stop recording chamber data

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

6.13. Remove DTNPL From Chamber

Start Date: _____ / Time: _____

(1) Disconnect Test Harness from DTNPL EGSE and chamber feed-through.

(2) Disconnect TC Harness from DTNPL EGSE and chamber feed-through.

(3) Remove temperature sensors.

(4) Dismount DTNPL Base plate fixations.

(5) Remove DTNPL from Chamber.

End Date: _____ / Time: _____

Test Engineer: _____ (Signature)

7. Test Conclusion

The PA shall review the test data for acceptance of the thermal Vacuum test.

The following sign off is verification that the test article has satisfactorily passed thermal Cycling test.

PA: _____ Date: _____