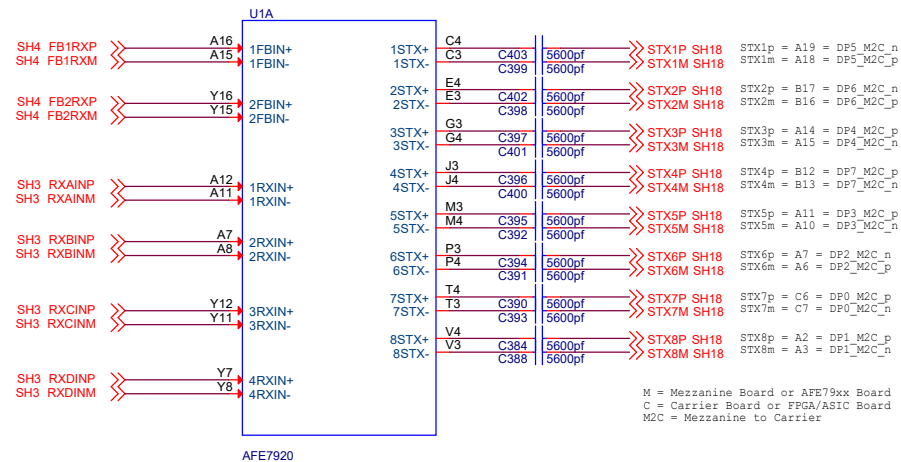
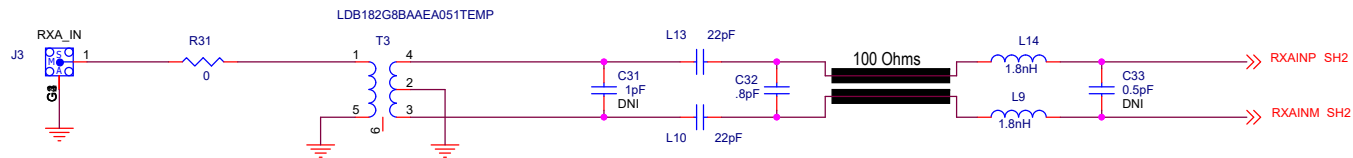
 TEXAS INSTRUMENTS		
Title		
BLOCK DIAGRAM		
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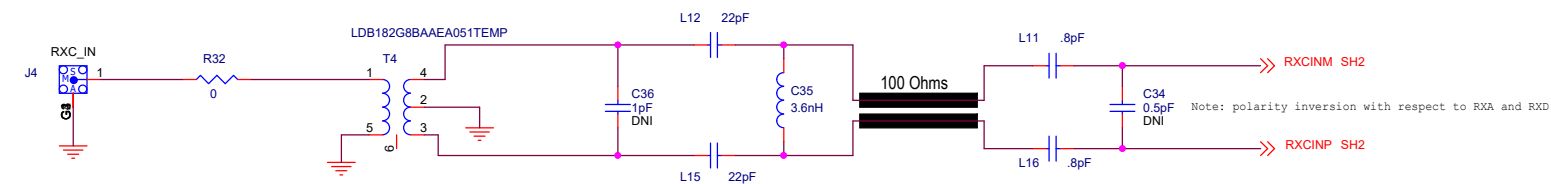
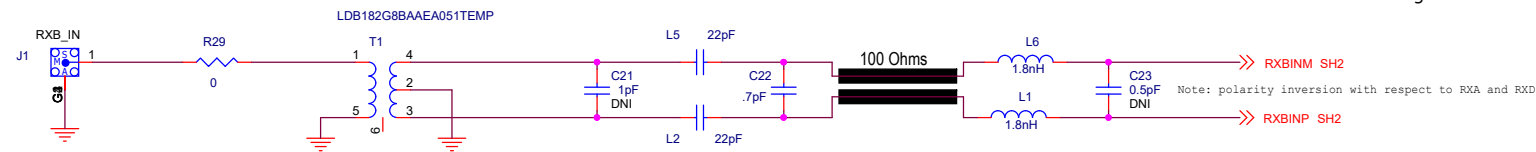
Drawn:	ASHWIN 08/2019
Approved:	SRINIVAS 08/2019



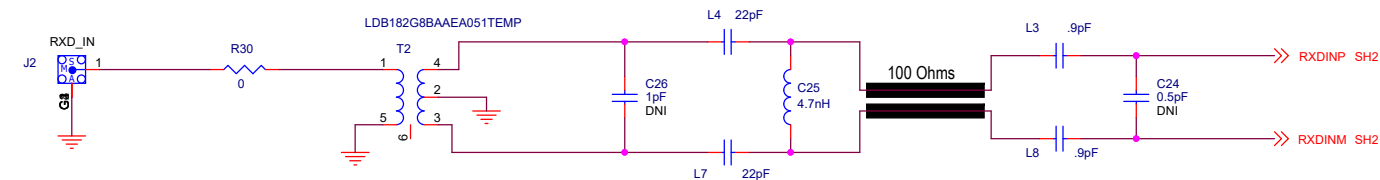
Title		
ADC		
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2.6GHz Matching

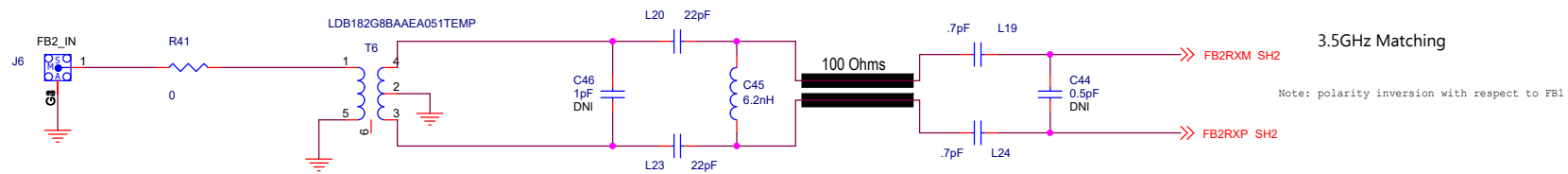
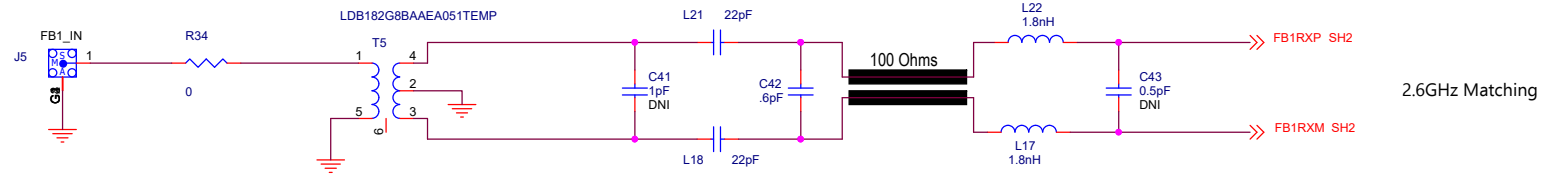


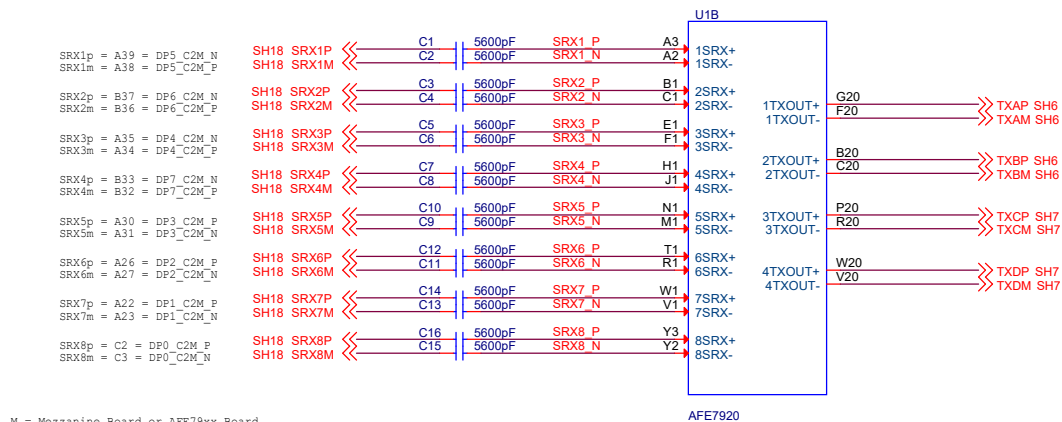
3.5GHz Matching



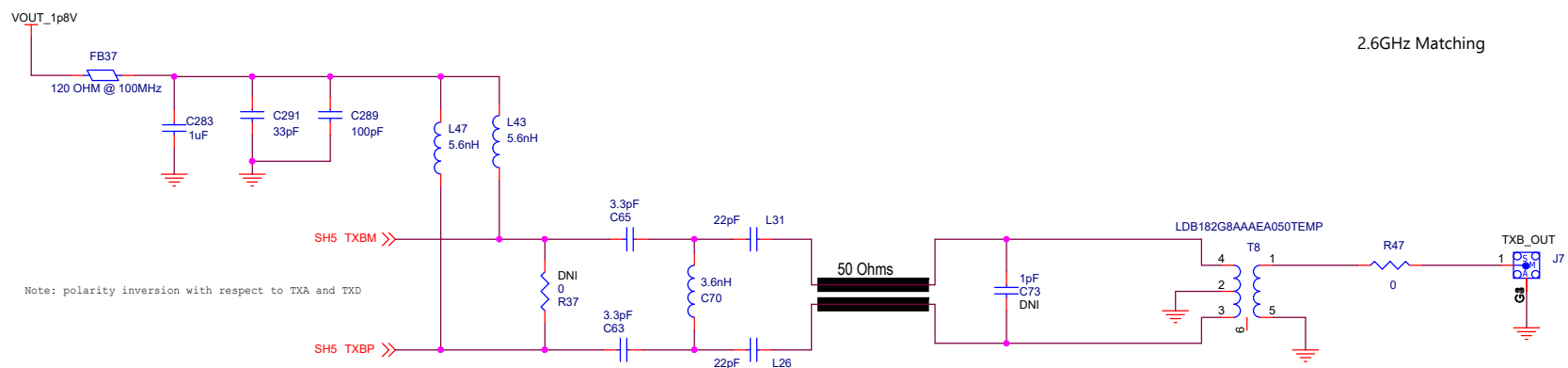
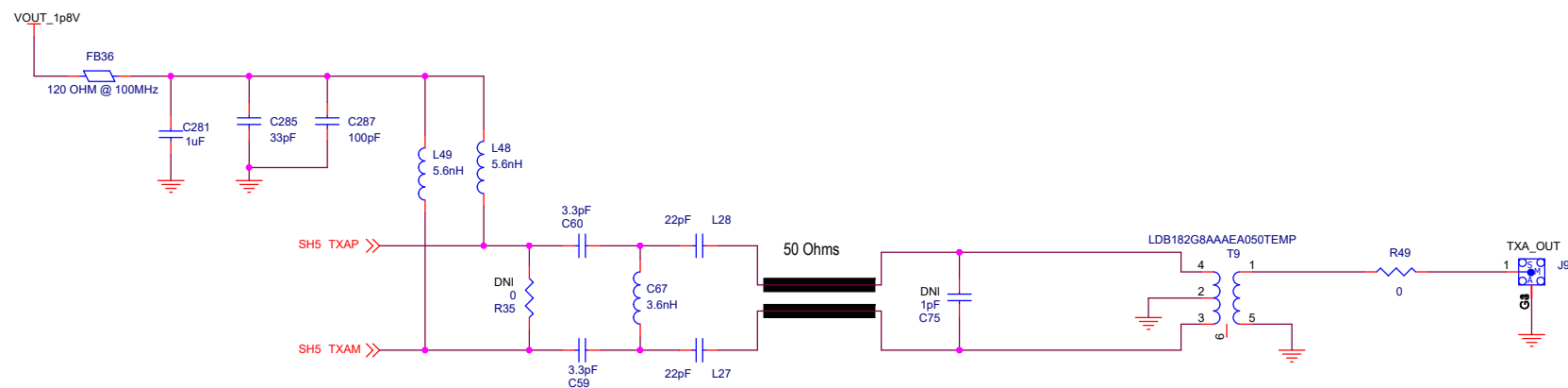
TEXAS INSTRUMENTS

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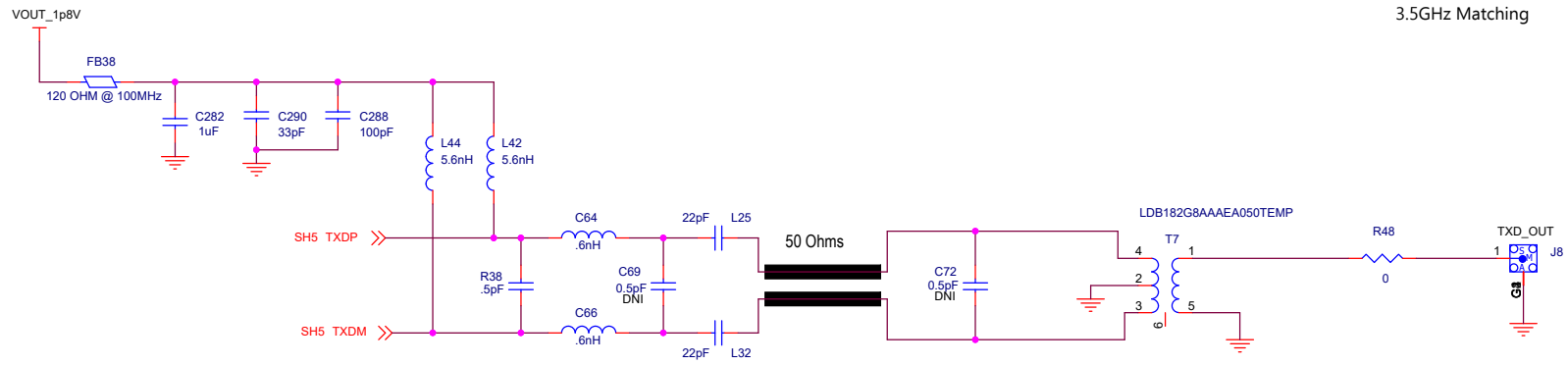
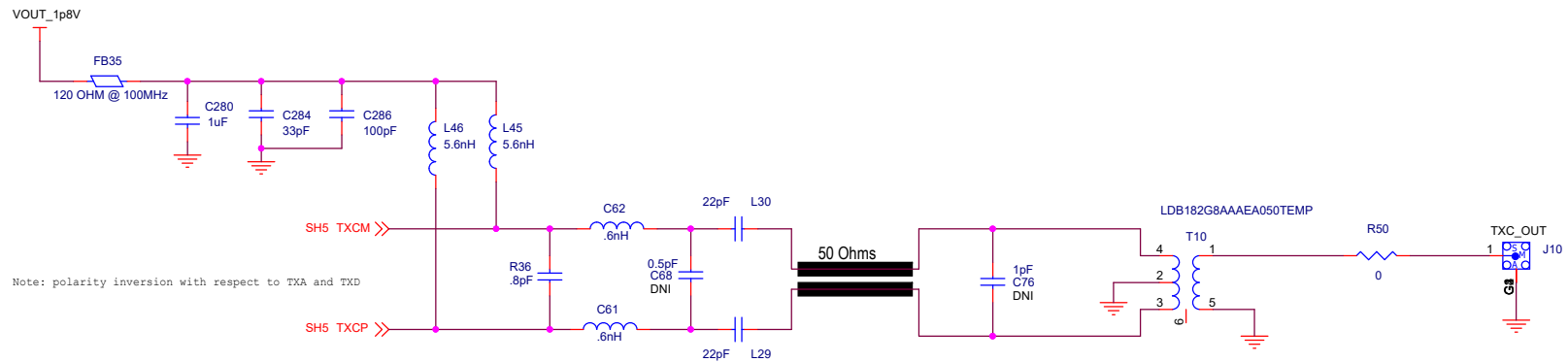


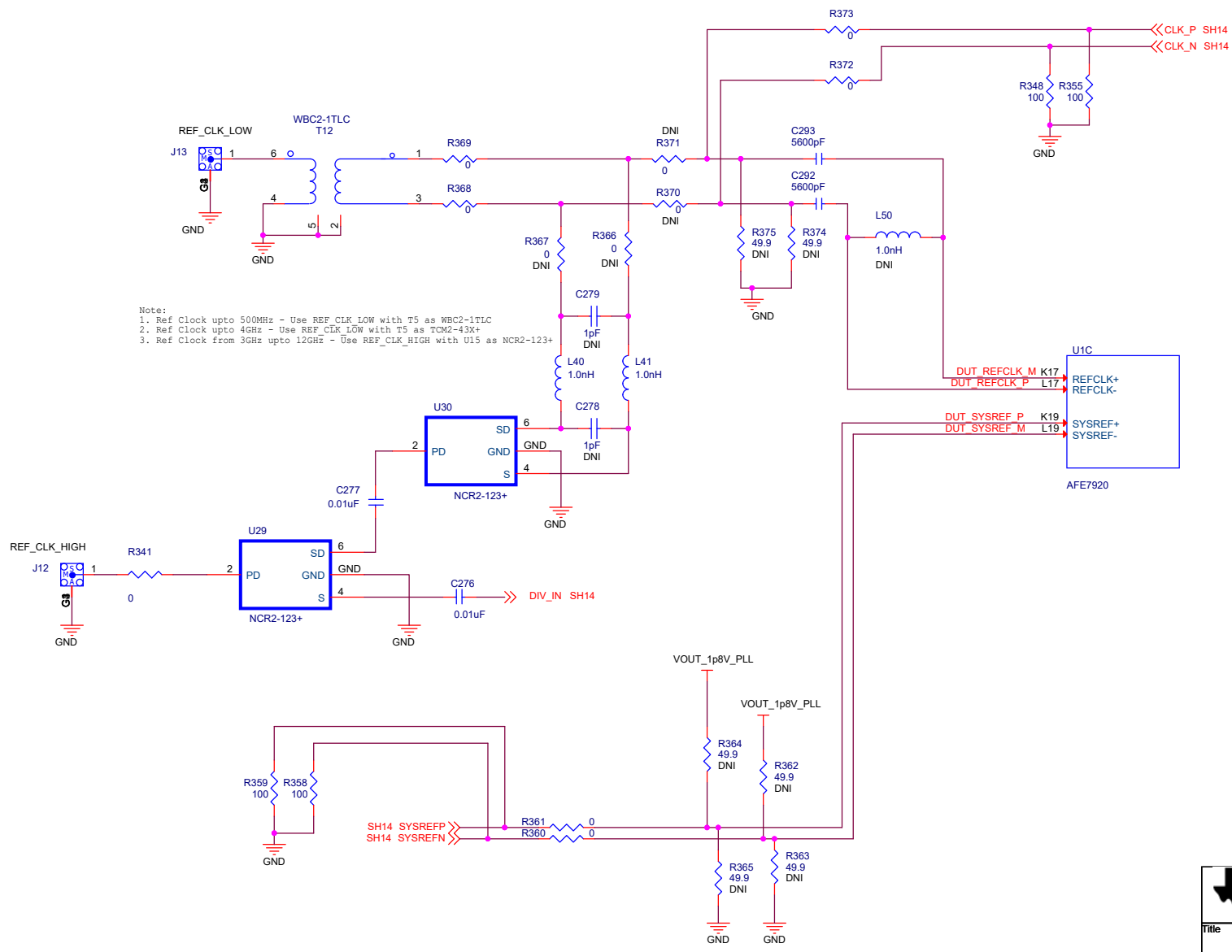


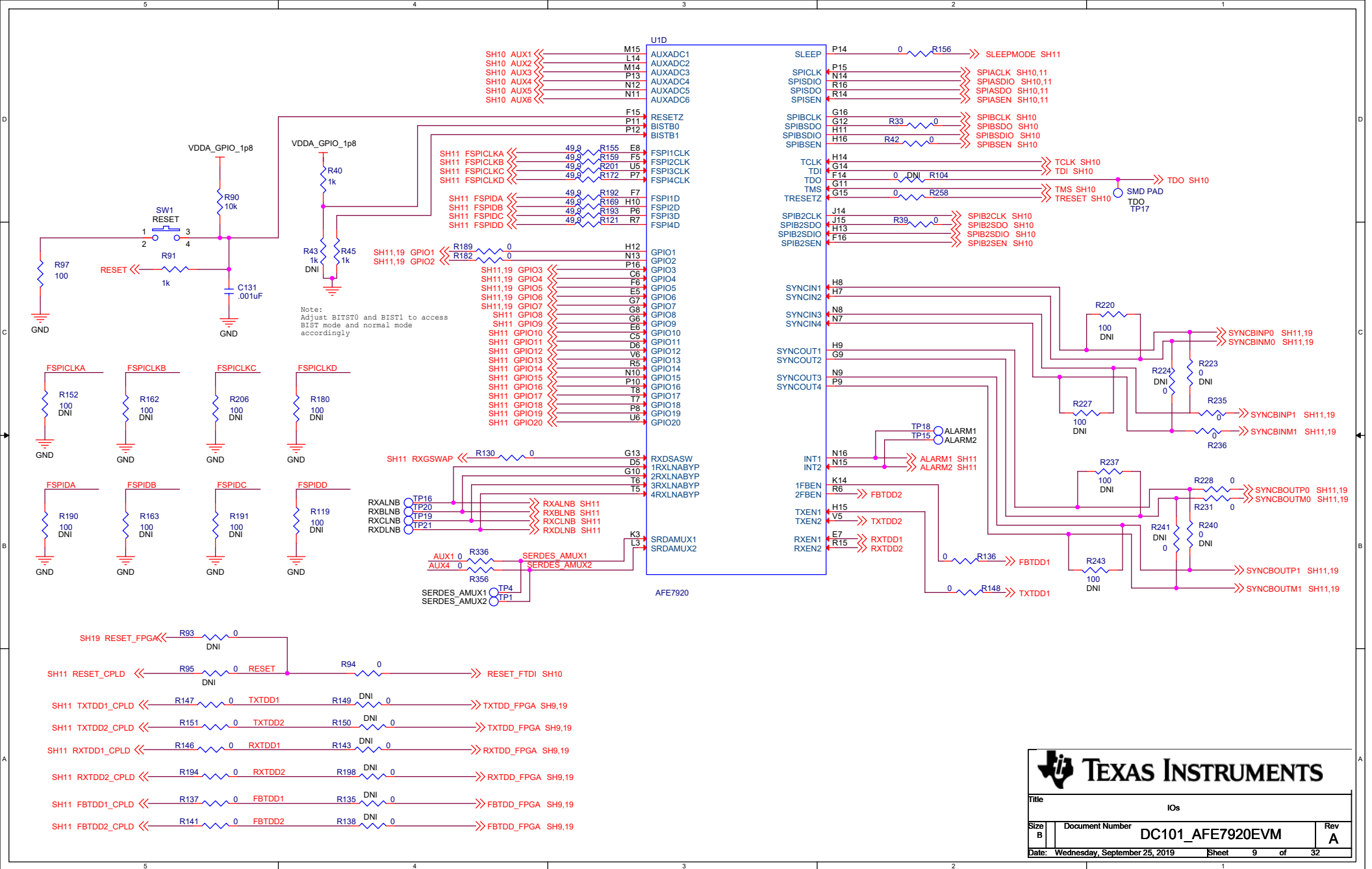
M = Mezzanine Board or AFE79xx Board
C = Carrier Board or FPGA/ASIC Board
M2C = Mezzanine to Carrier

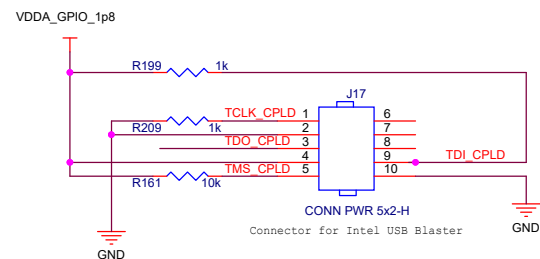
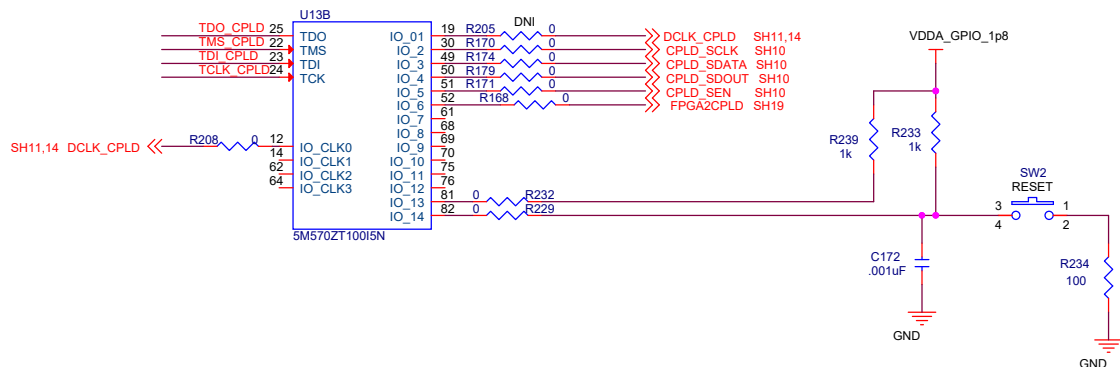
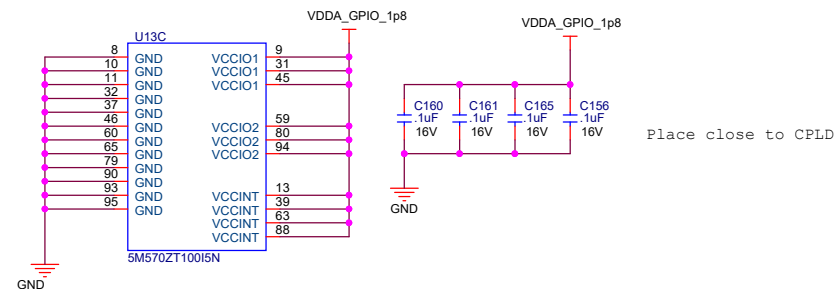
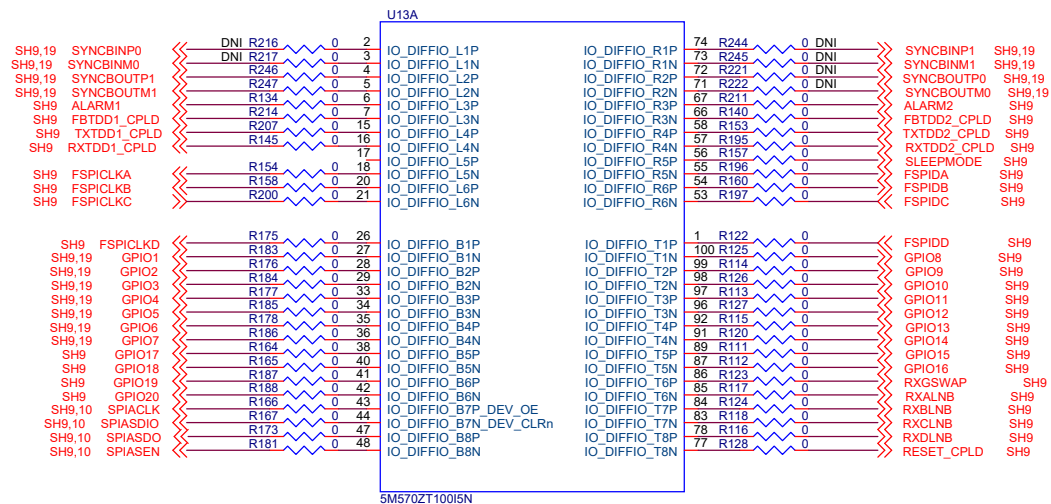


Title			
TXA & TXB			
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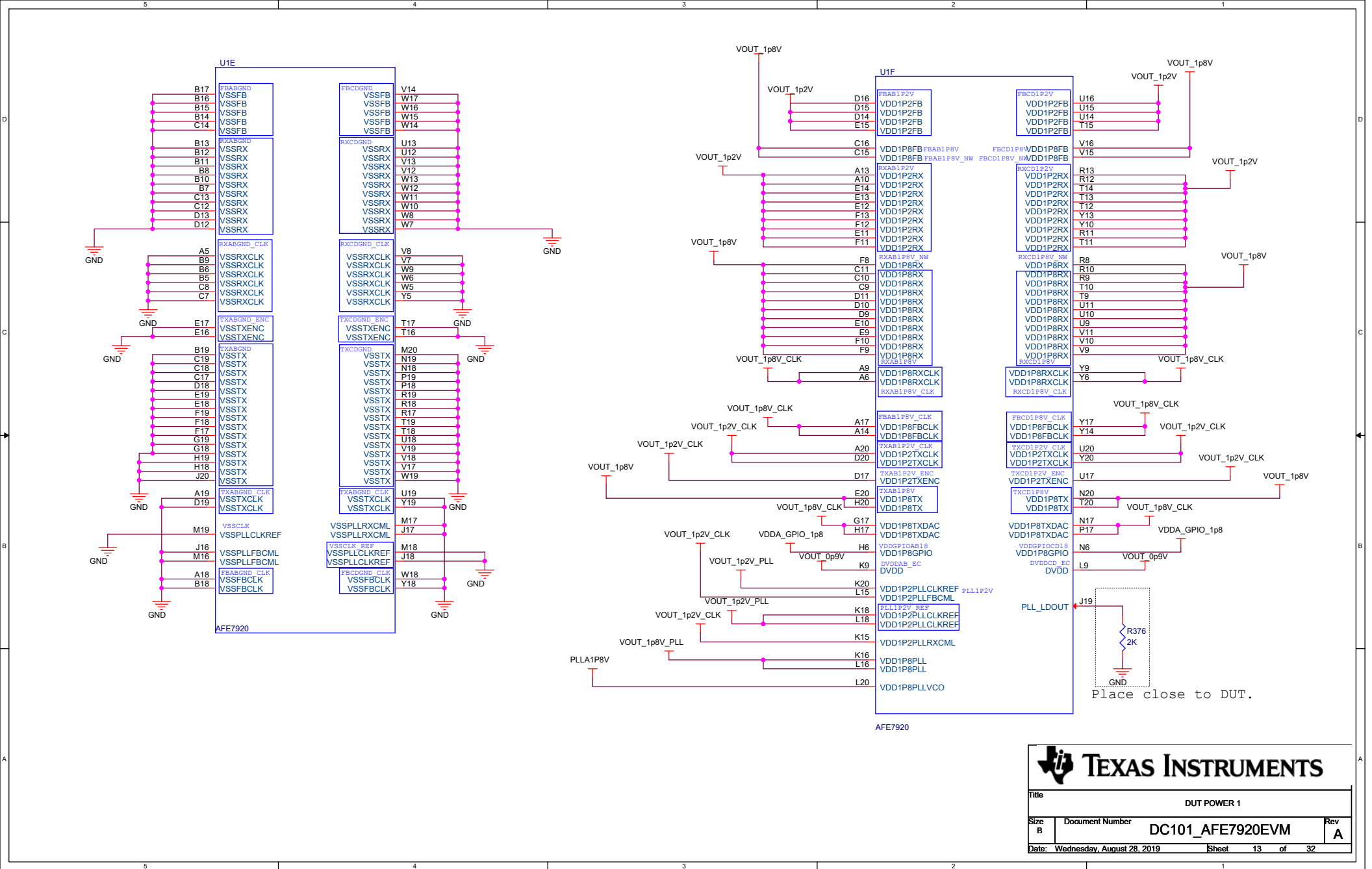


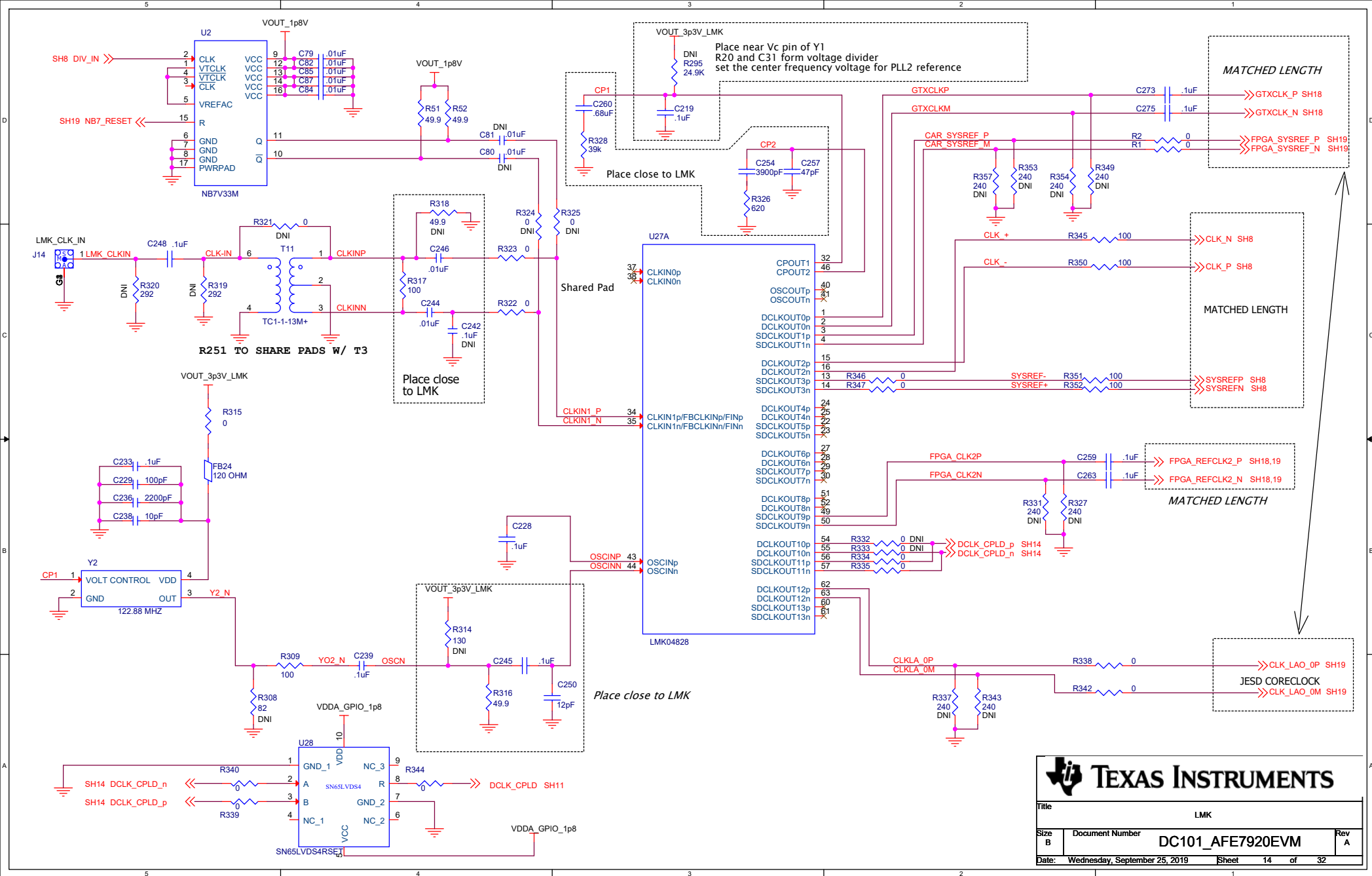
TEXAS INSTRUMENTS

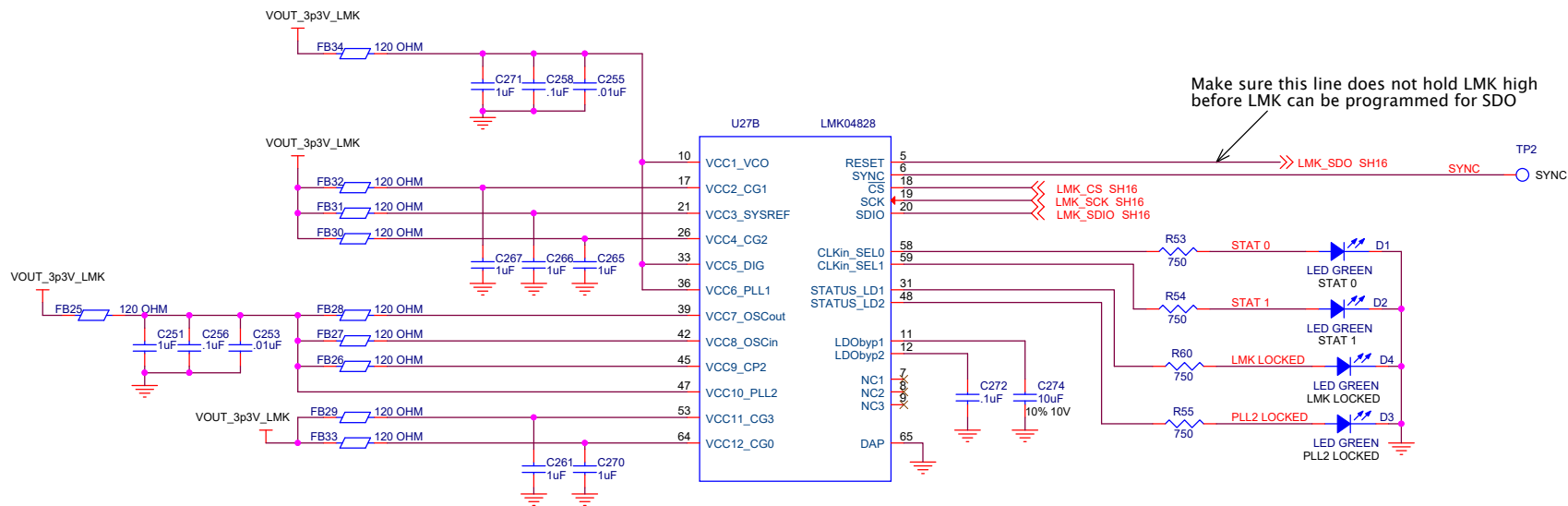
Title: CPLD

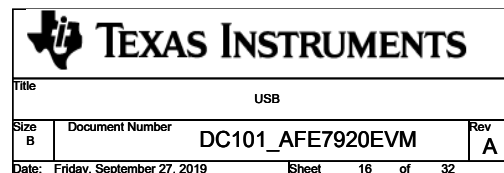
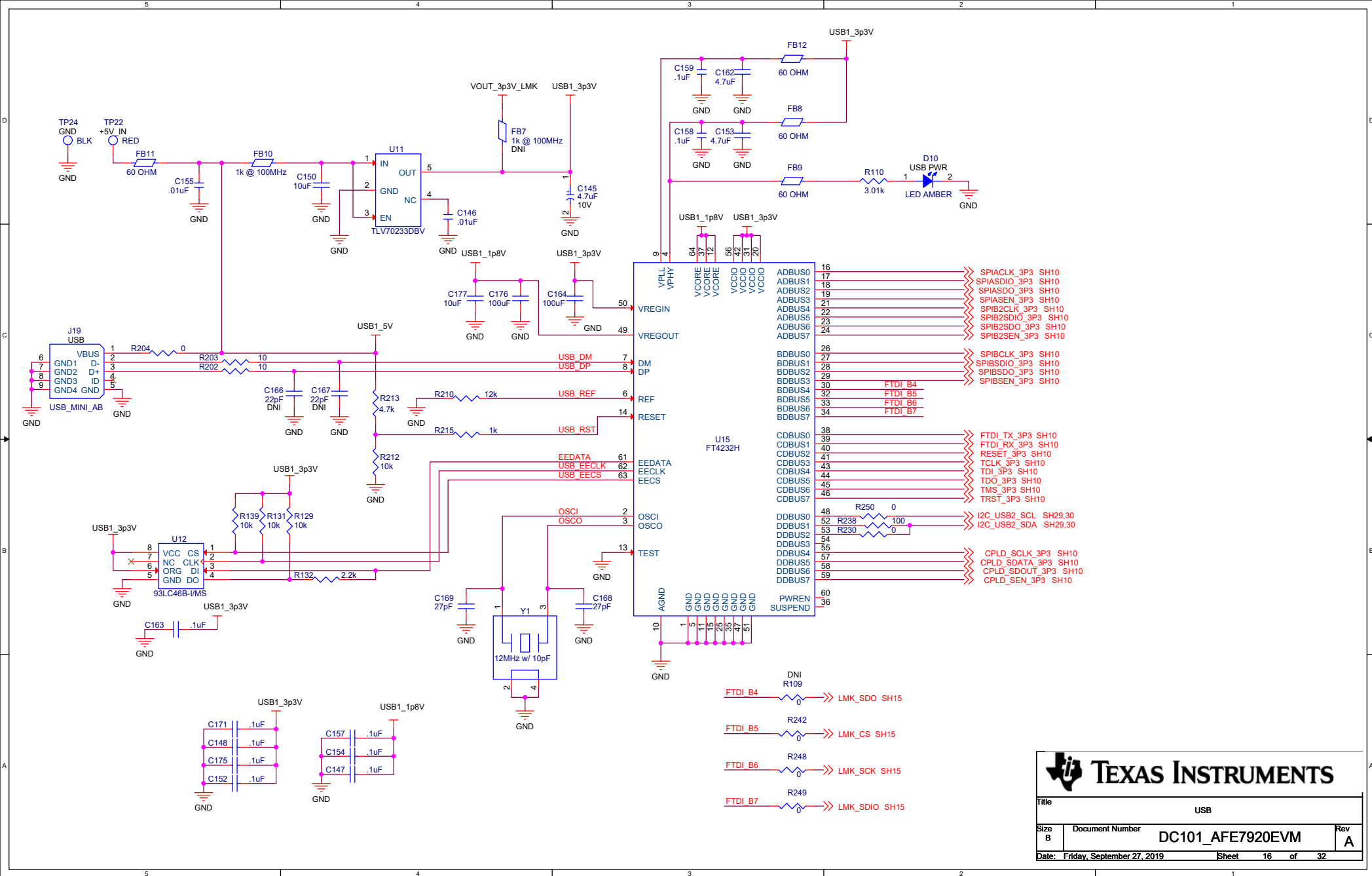
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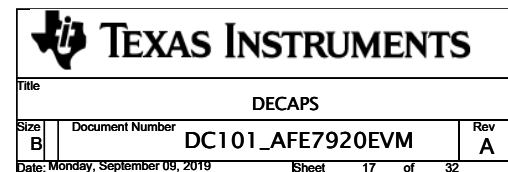
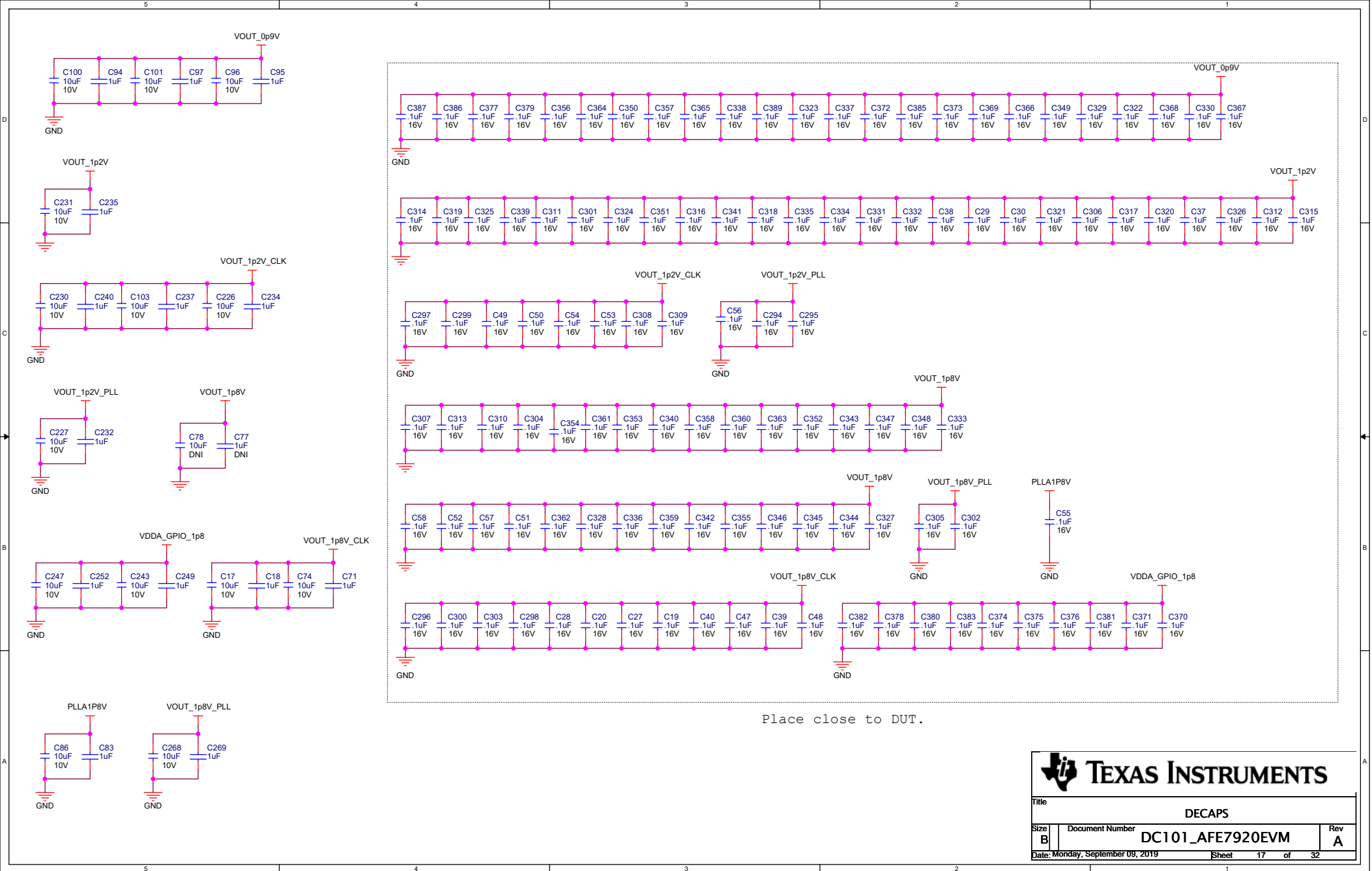
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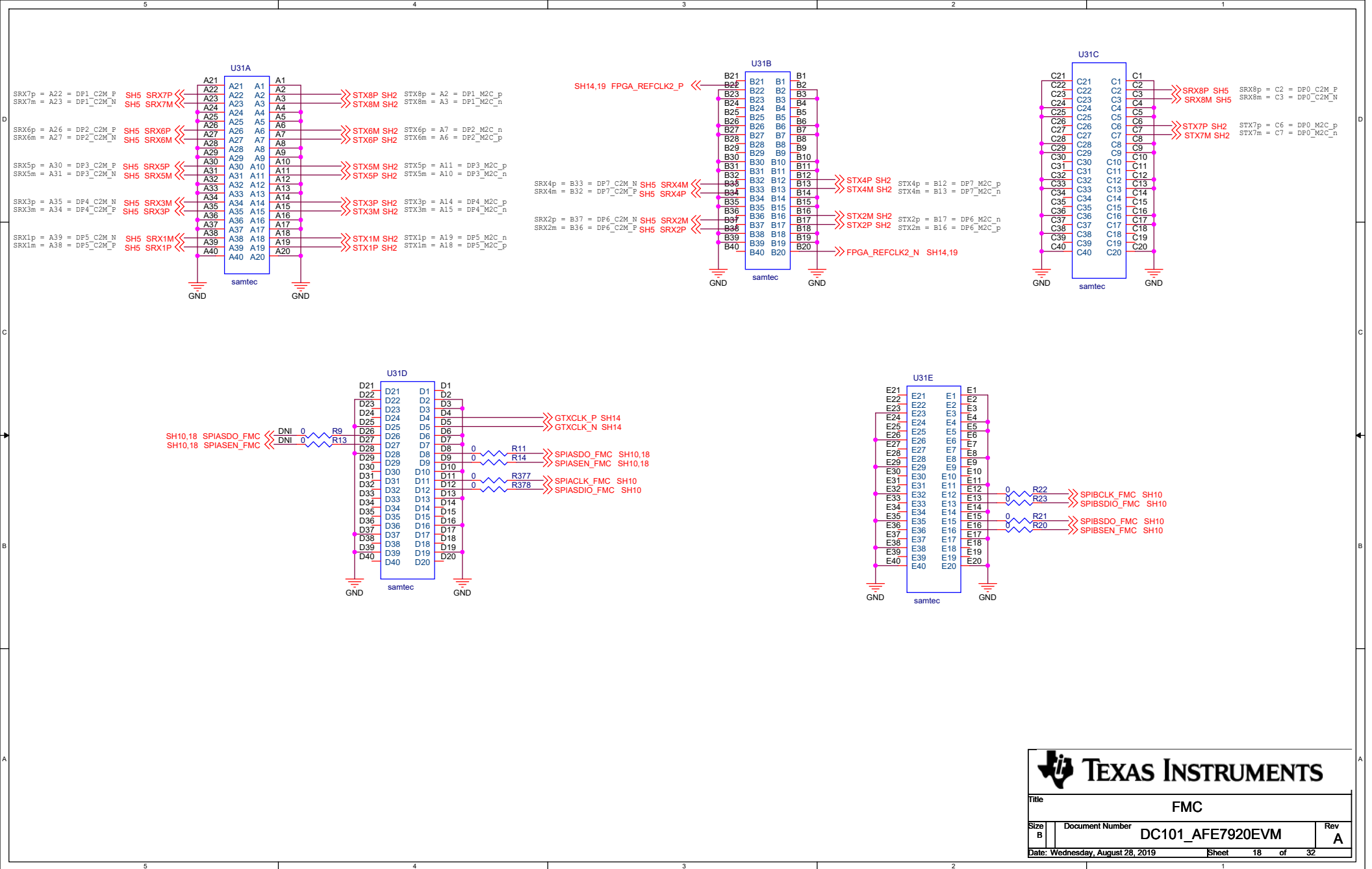


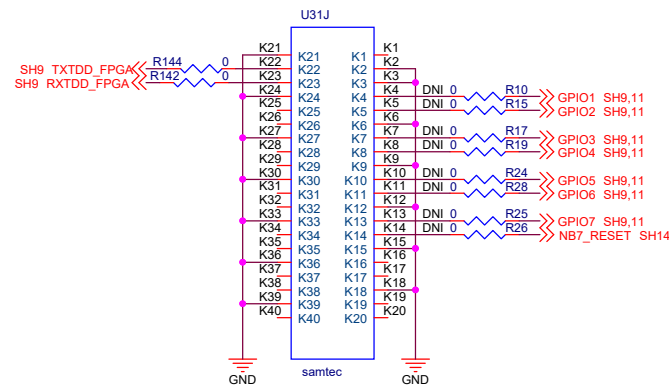
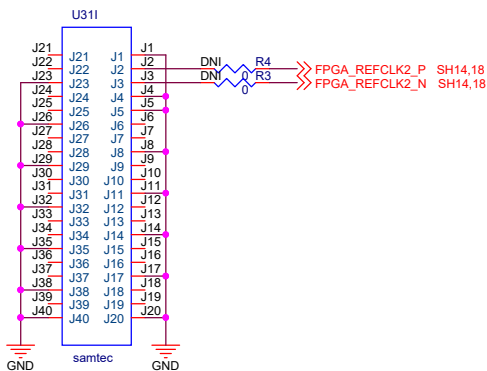
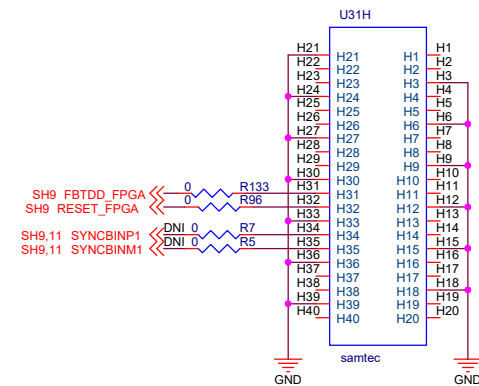
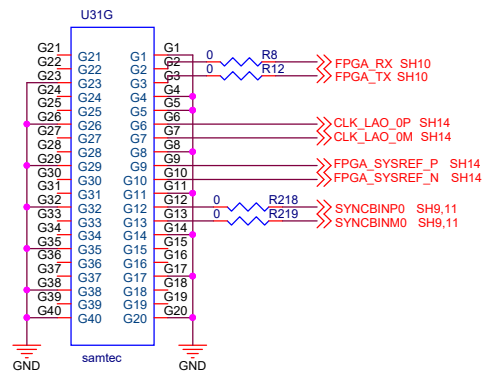
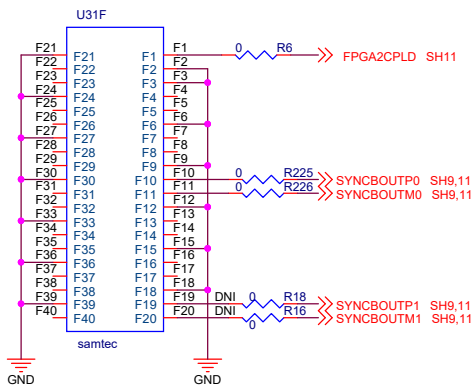




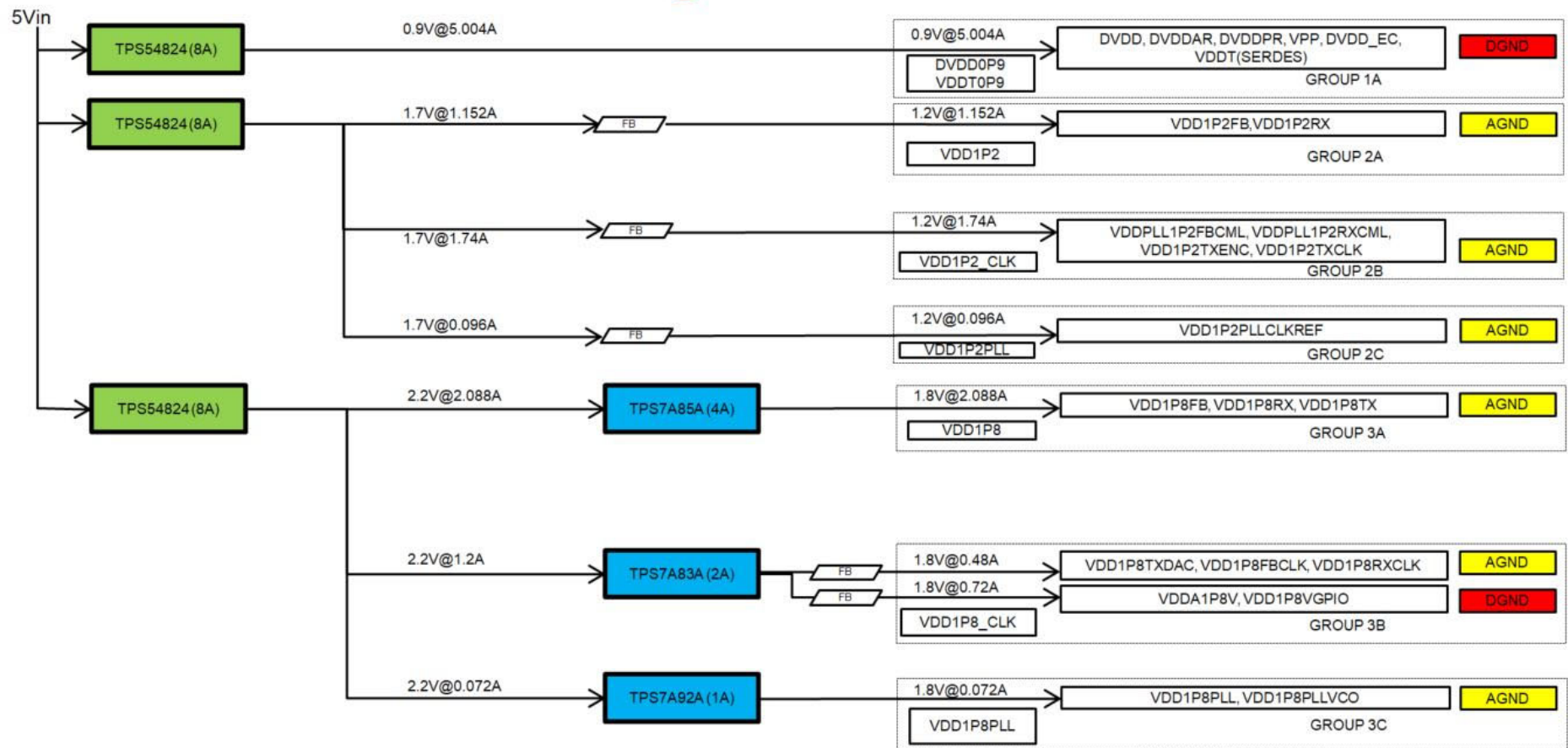




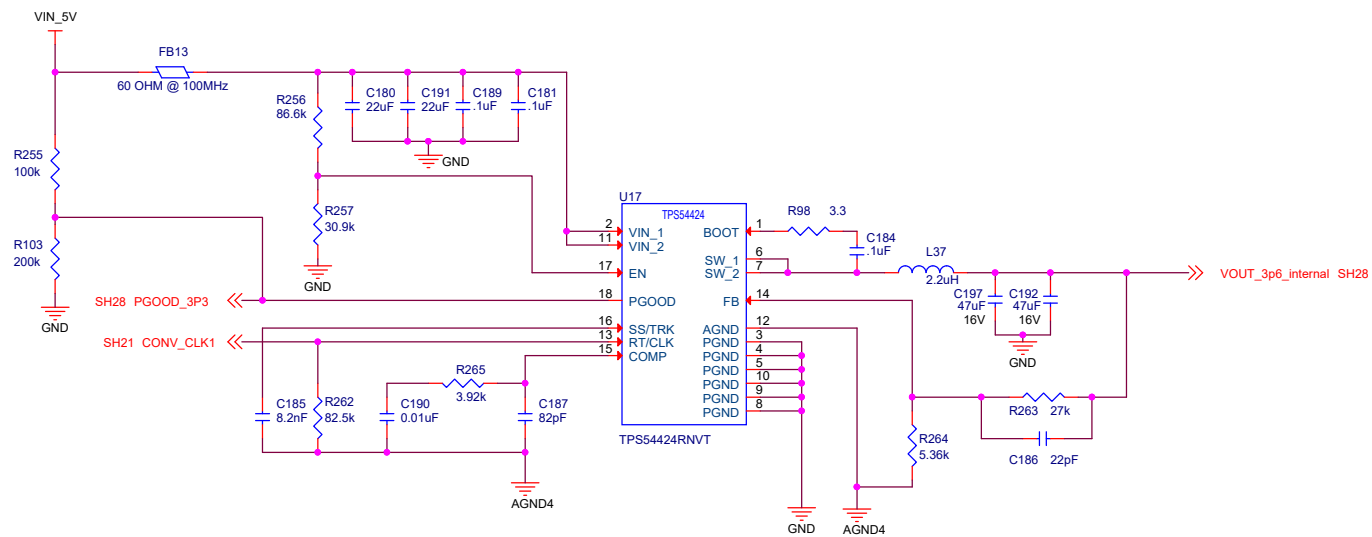


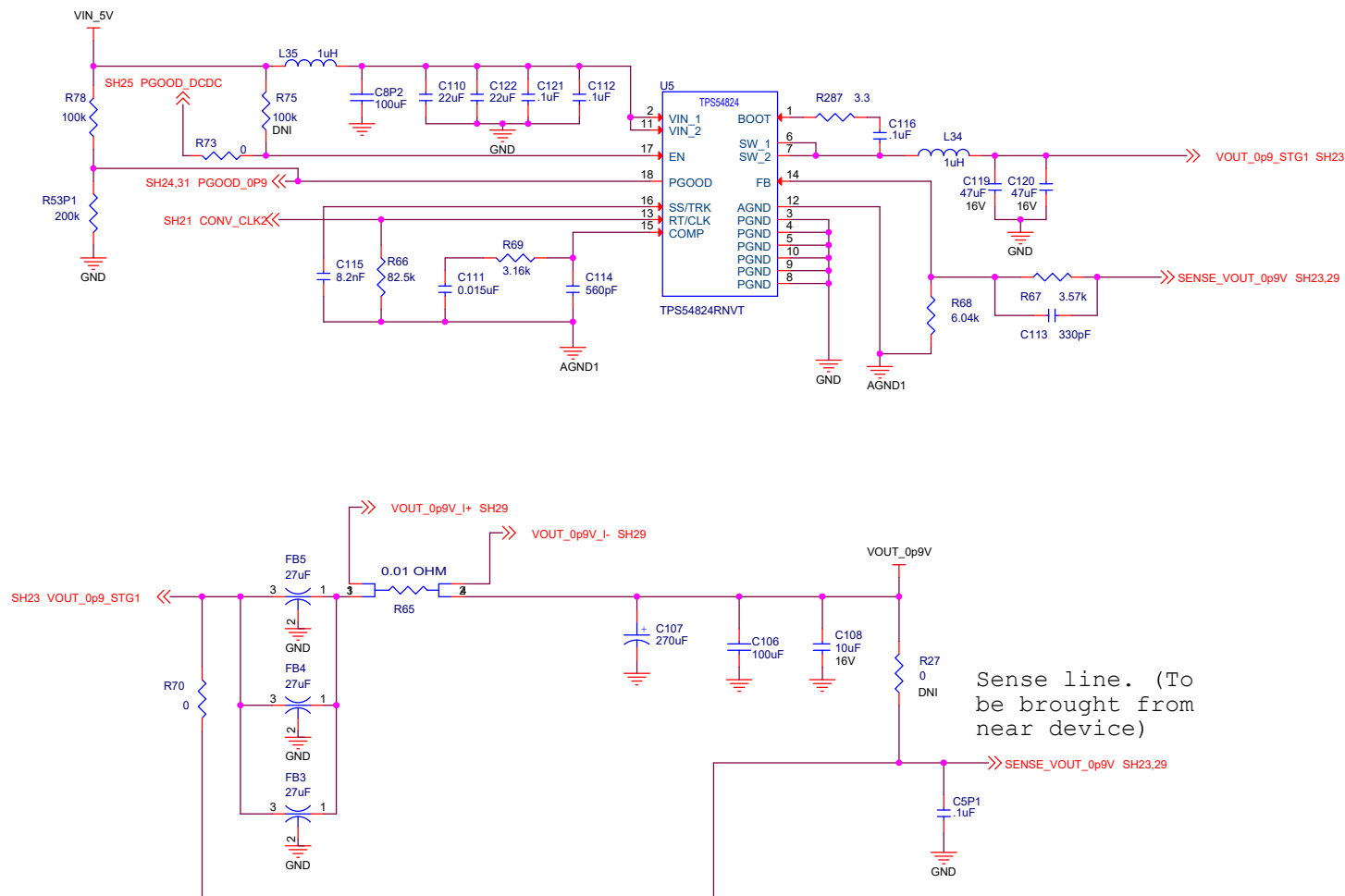


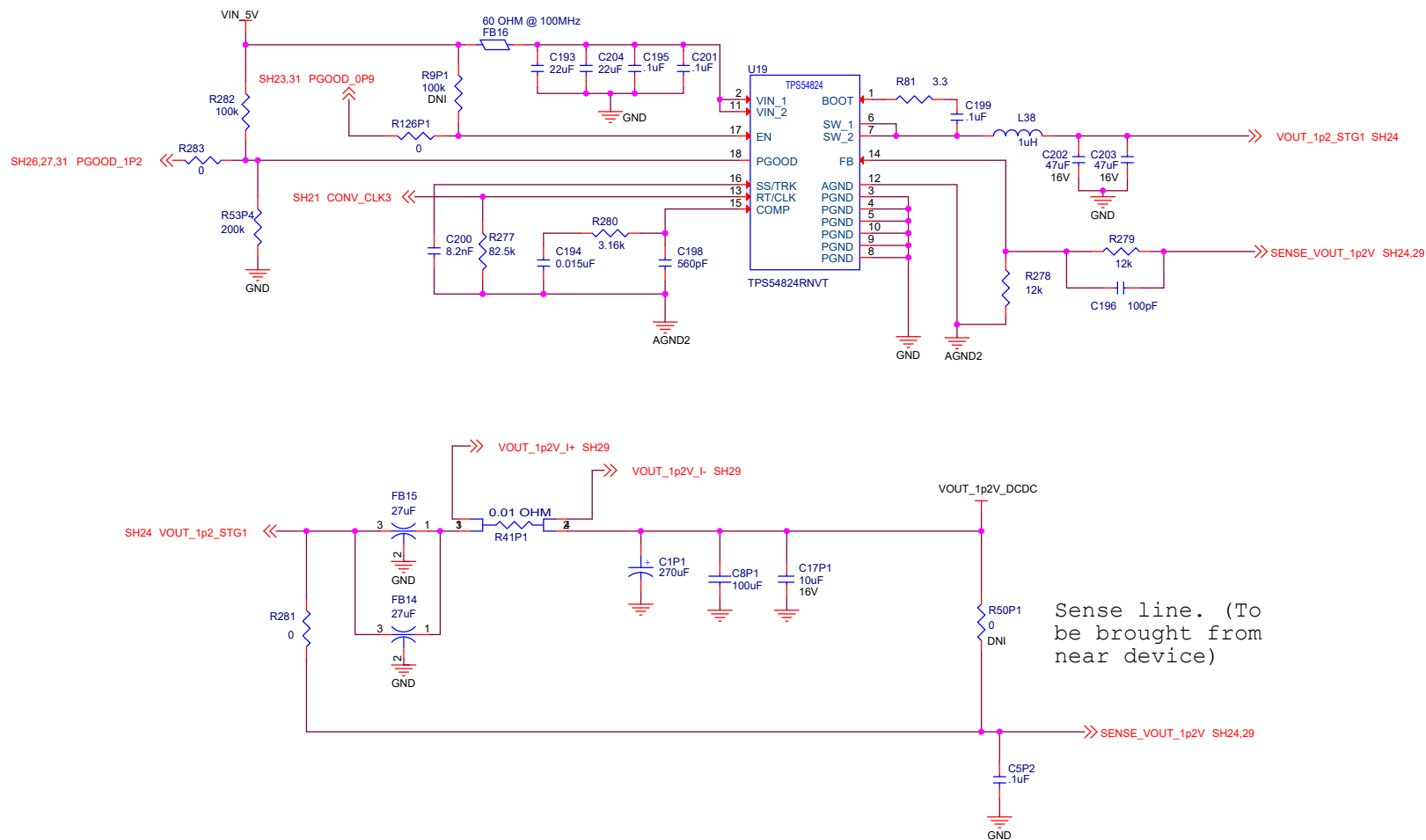
1x AFE78xx Block Diagram



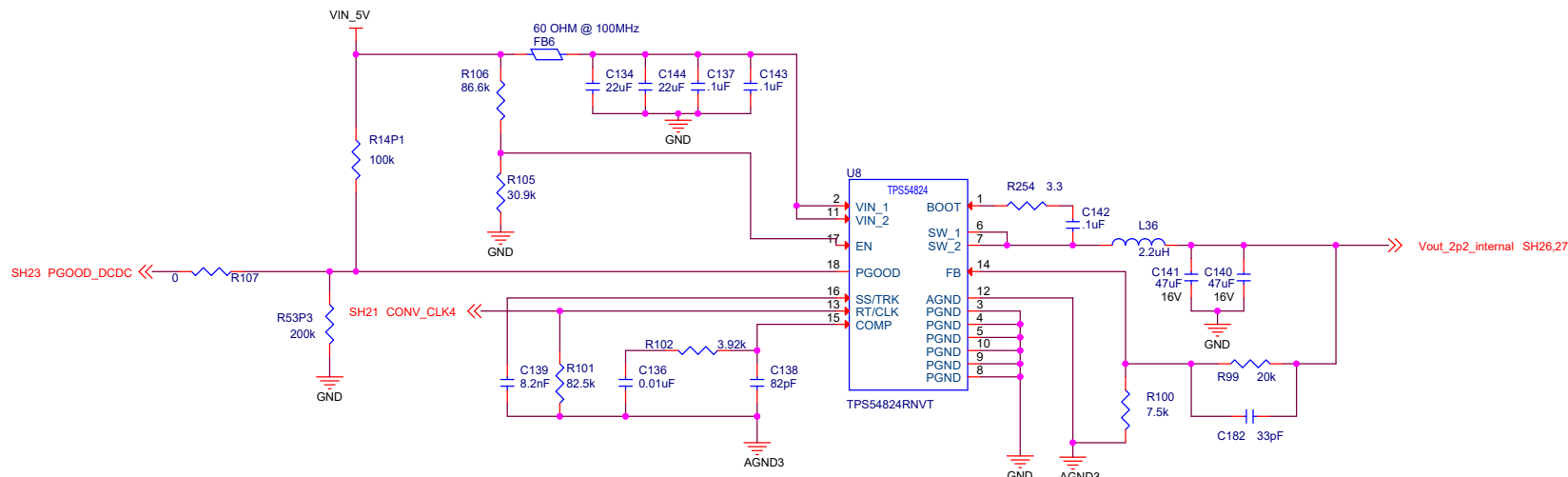
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POWER TREE			
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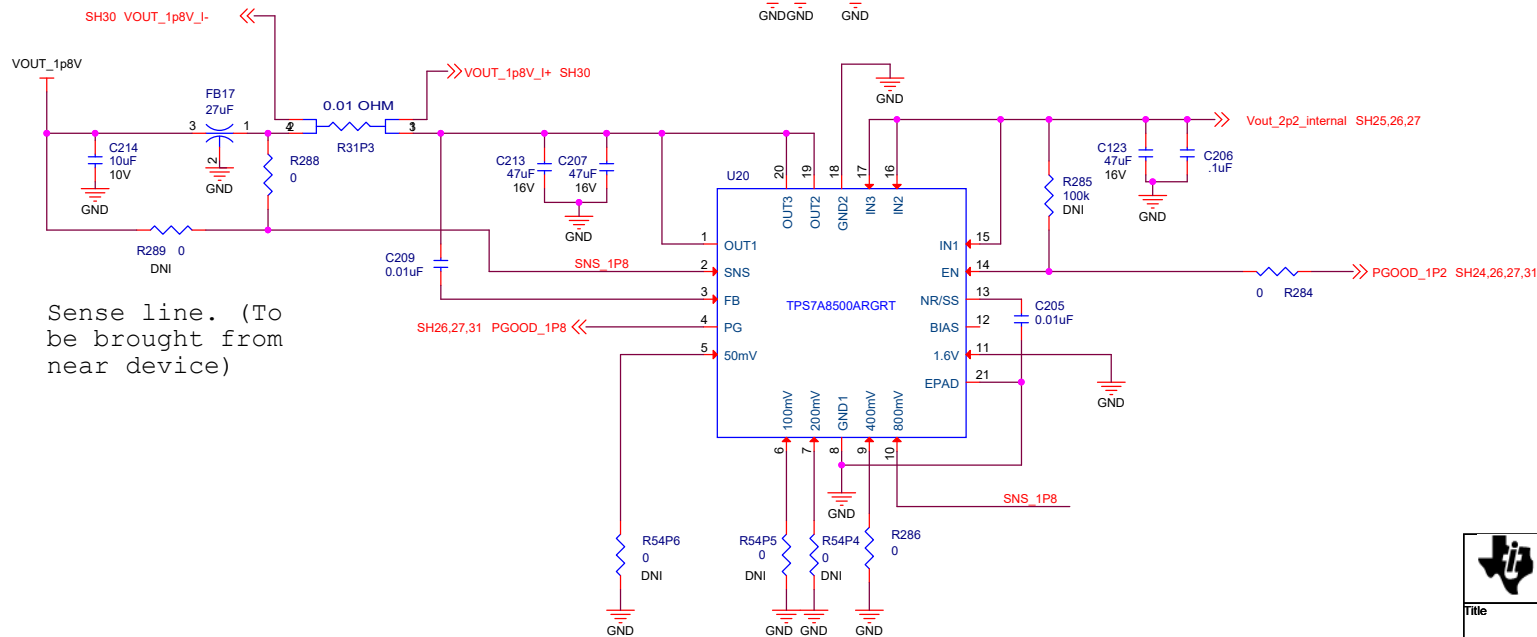
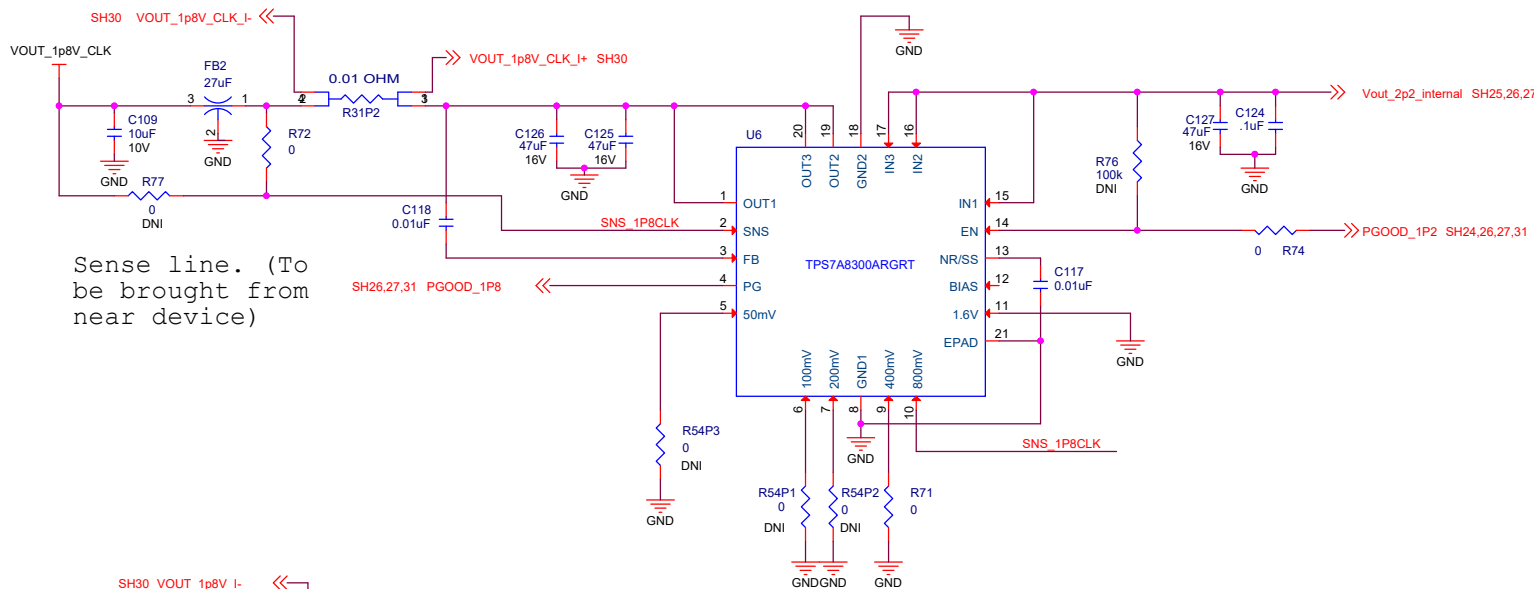


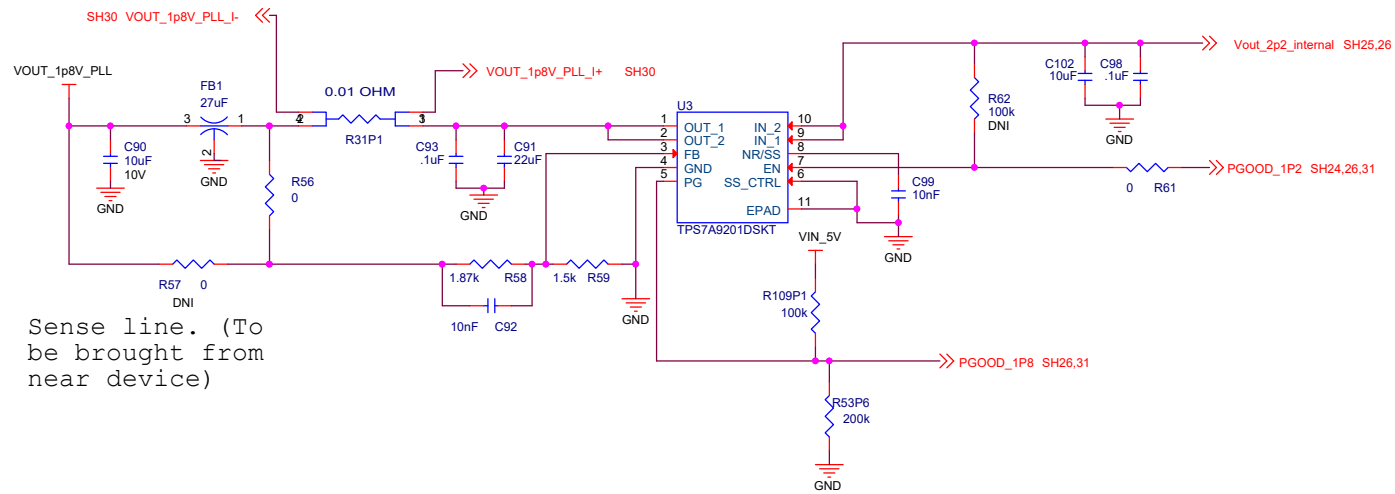


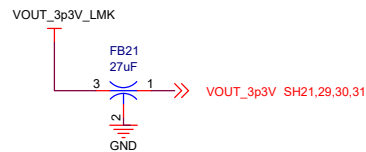
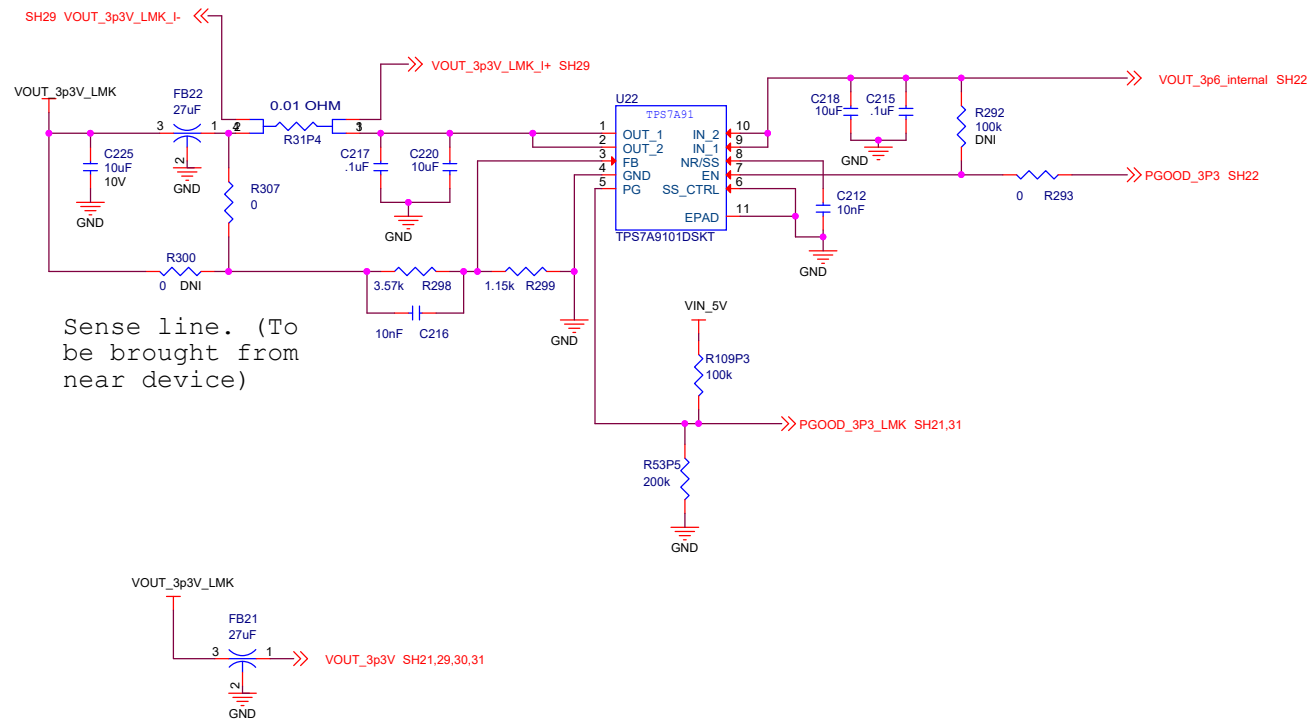


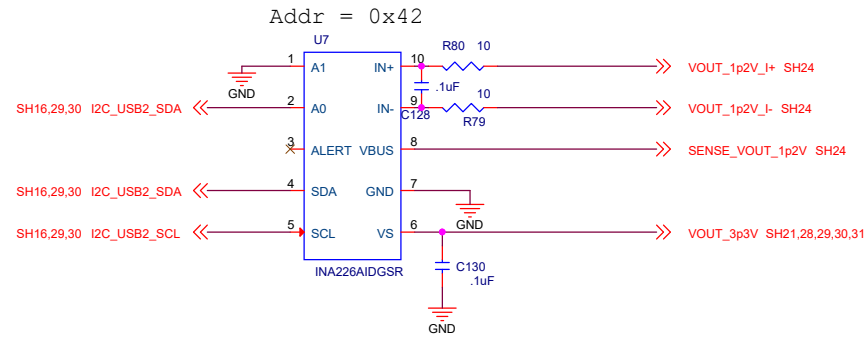
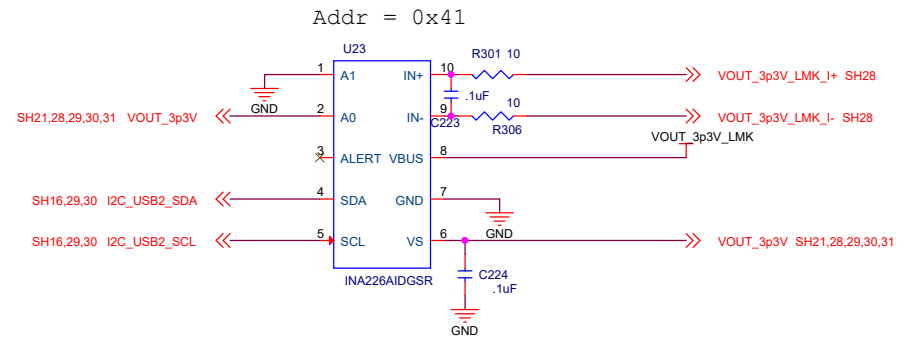
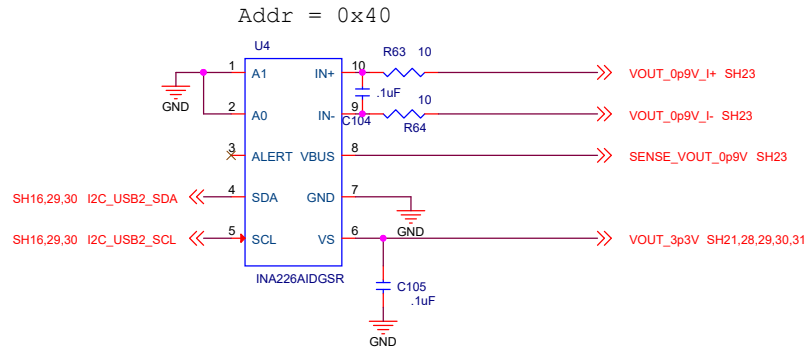
Sense line. (To be brought from near device)



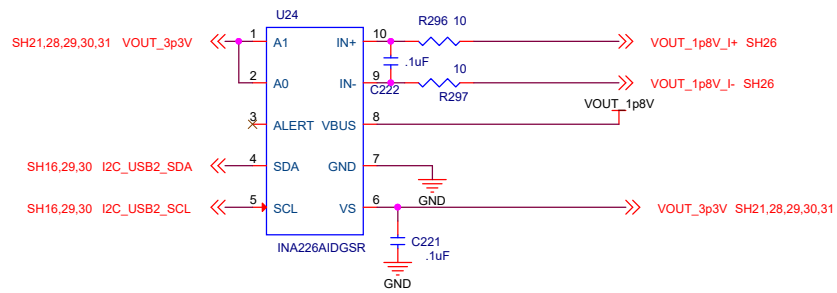




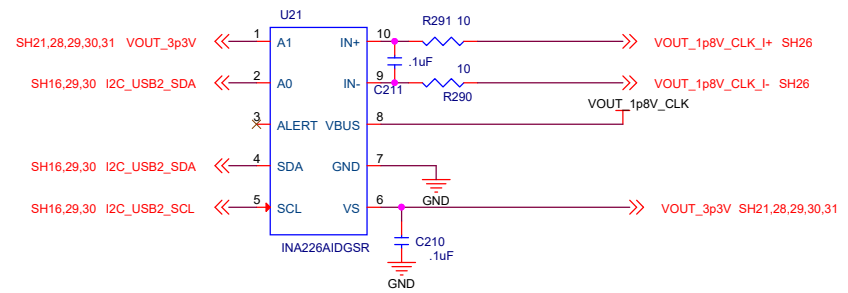




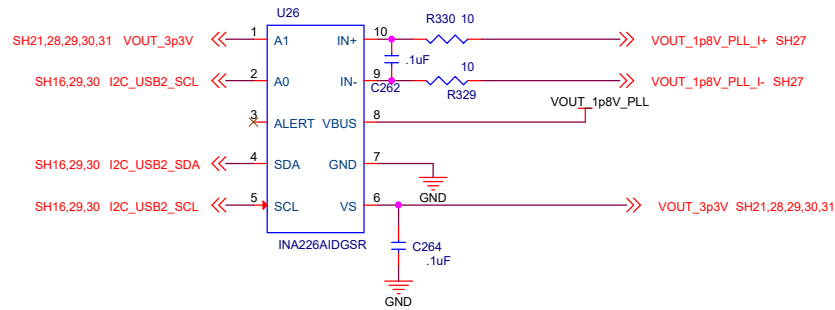
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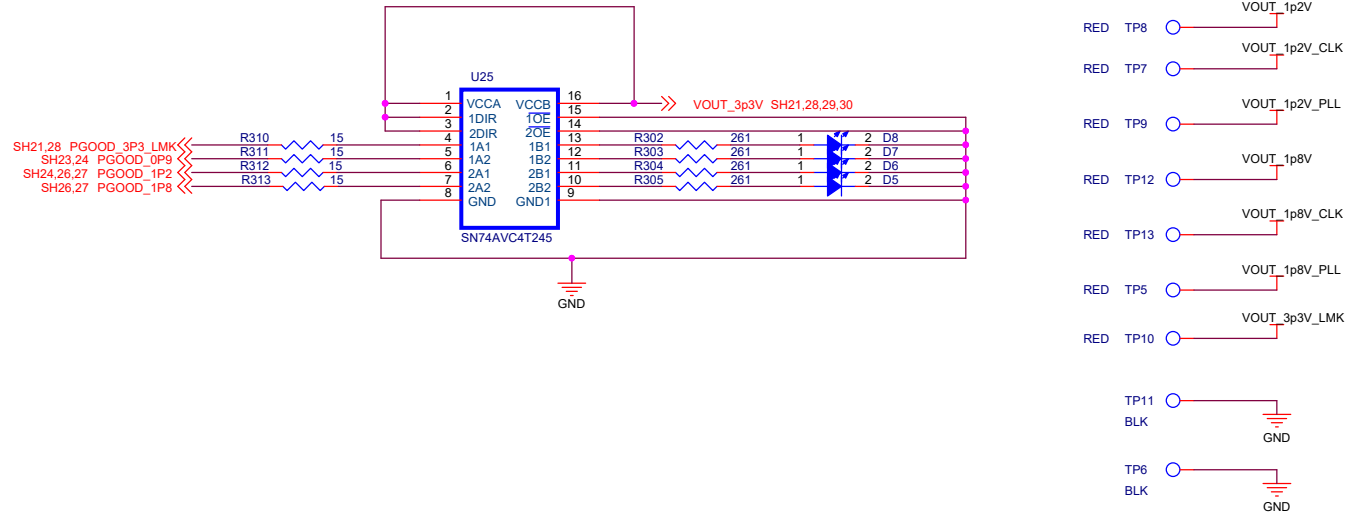
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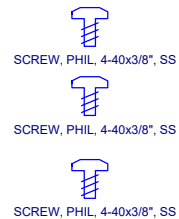
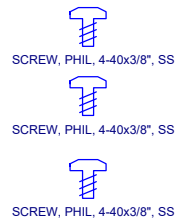
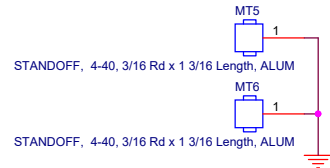
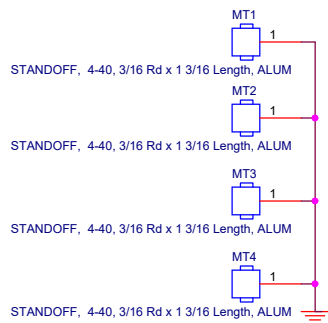
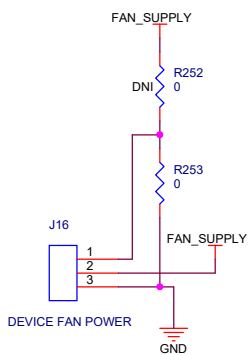
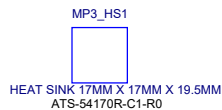


Addr = 0x47



All VBUS to be connected to sense lines of LDO





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