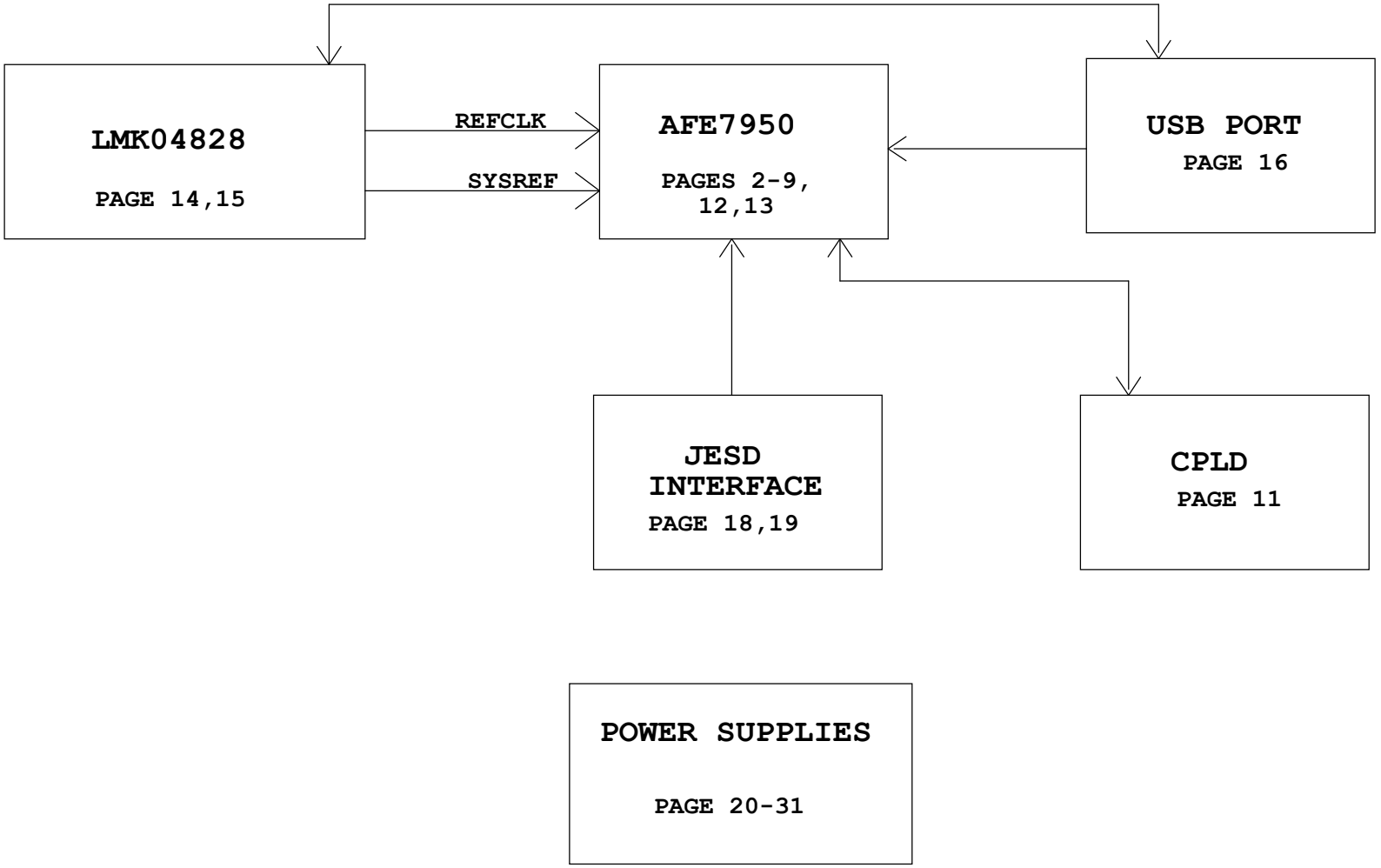
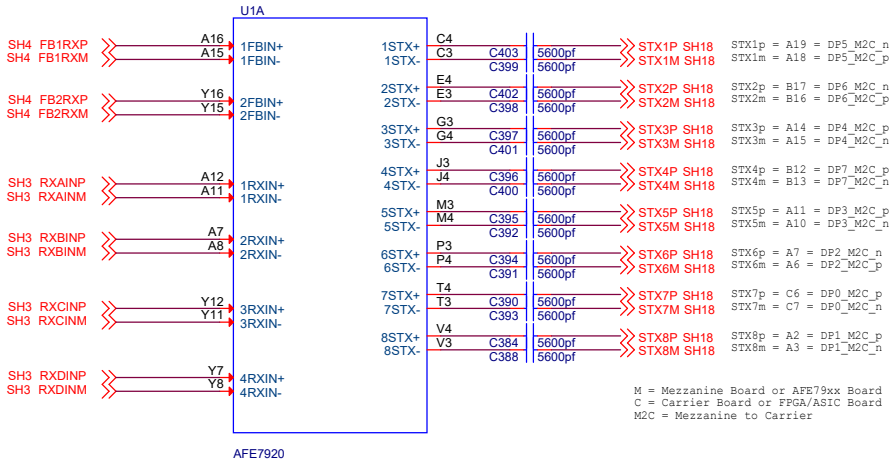


Drawn: L. NGUYEN 06/2020

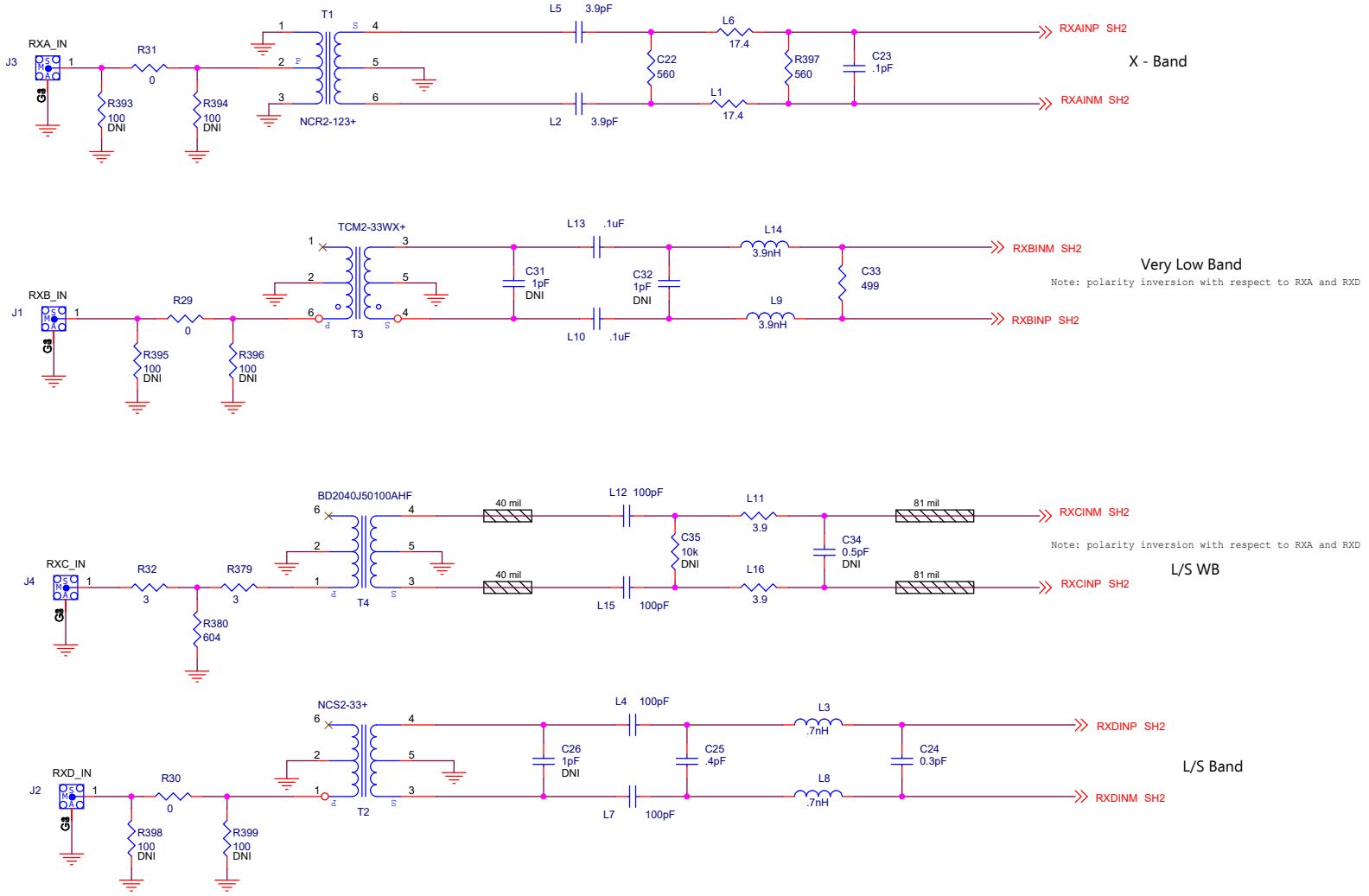
TEXAS INSTRUMENTS

Title: BLOCK DIAGRAM		
Size: B	Document Number: AFE7950EVM	Rev: A
Date: Monday, June 29, 2020	Sheet 1 of 32	



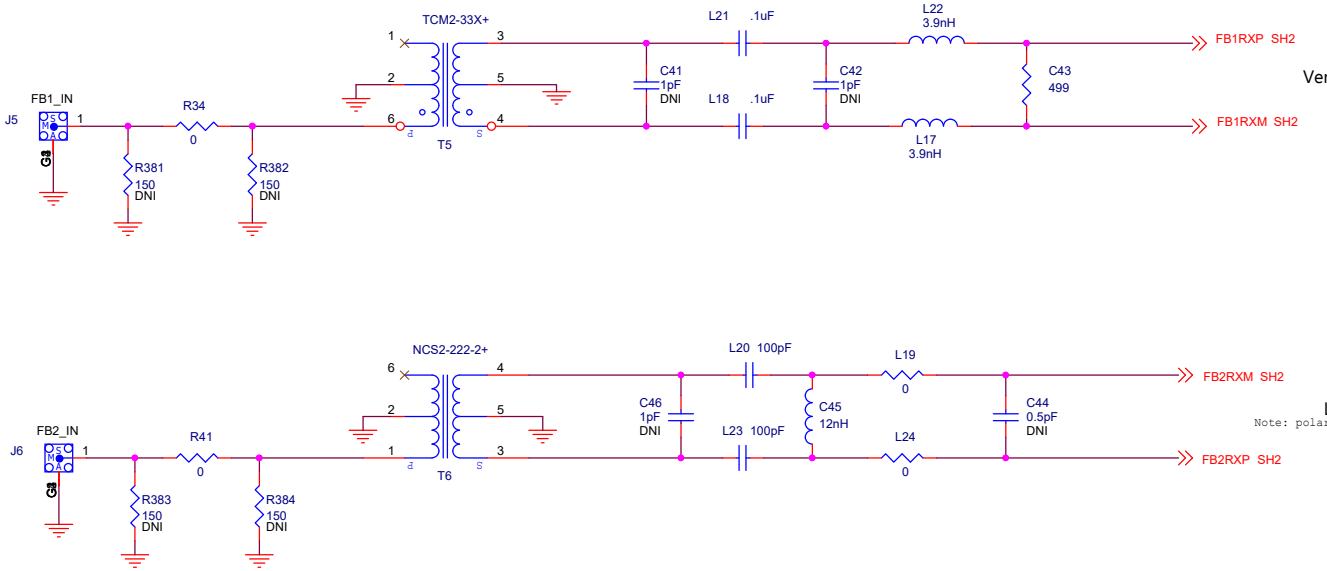
TEXAS INSTRUMENTS

Title: ADC		
Size: B	Document Number: AFE7950EVM	Rev: A
Date: Wednesday, May 20, 2020	Sheet 2 of 32	

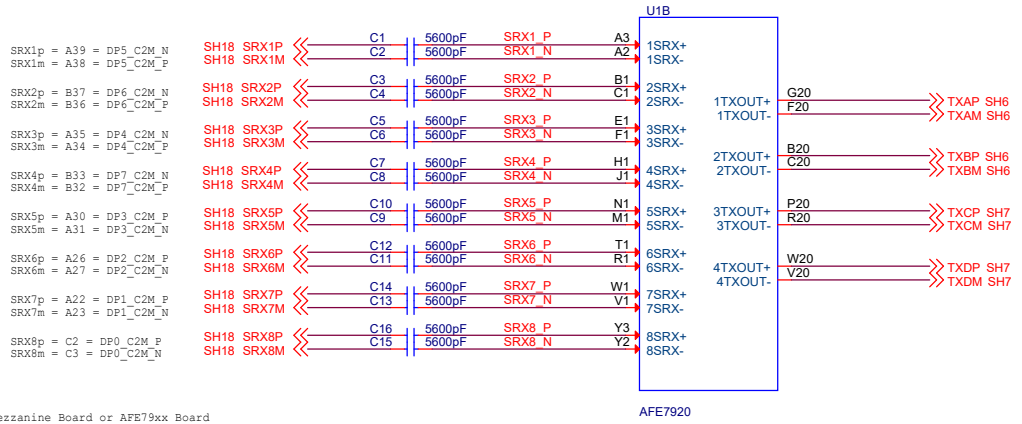


TEXAS INSTRUMENTS

Title	RX	
Size B	Document Number AFE7950EVM	Rev A
Date: Monday, June 29, 2020	Sheet 3 of 32	



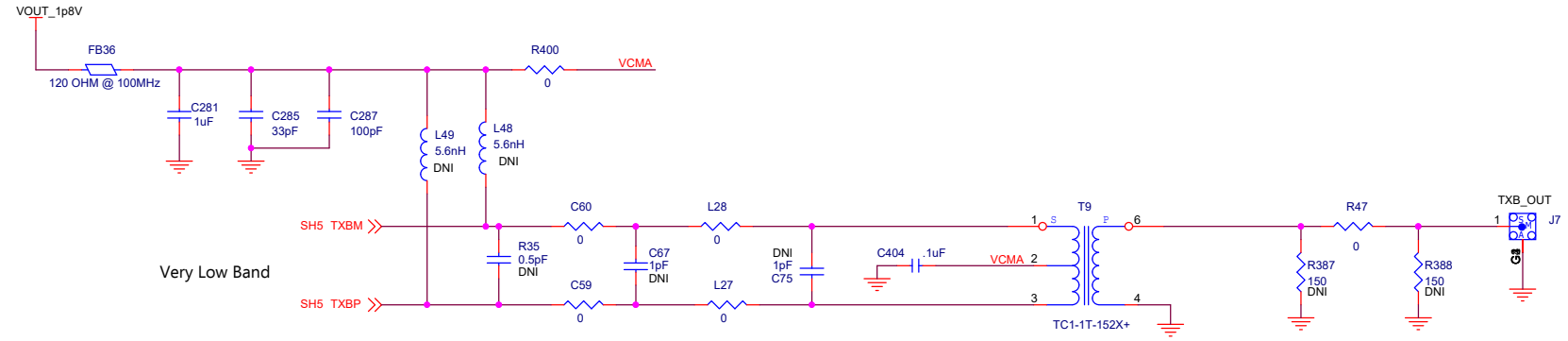
Title	FEEDBACK	
Size B	Document Number AFE7950EVM	Rev A
Date: Monday, June 29, 2020	Sheet 4 of 32	

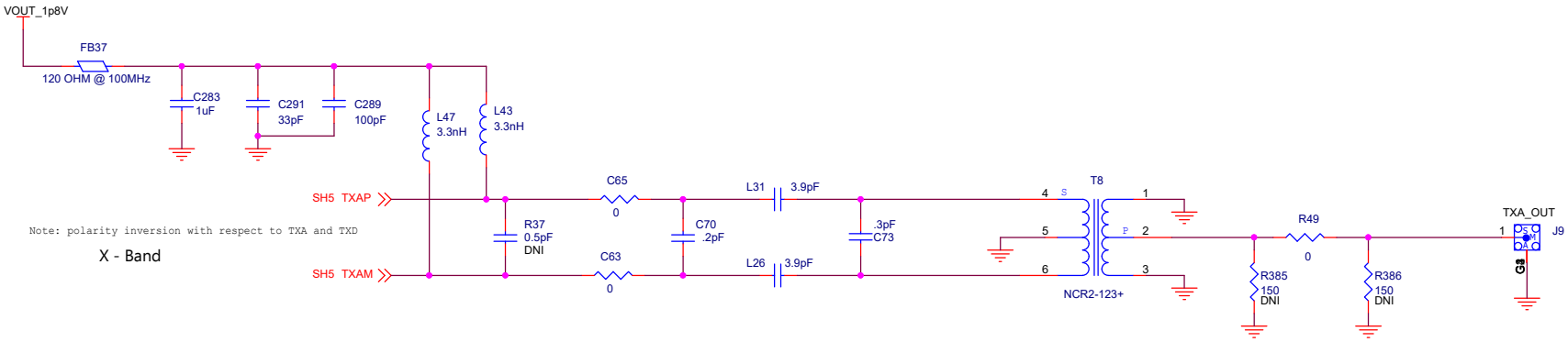


M = Mezzanine Board or AFE79xx Board
C = Carrier Board or FPGA/ASIC Board
M2C = Mezzanine to Carrier

TEXAS INSTRUMENTS

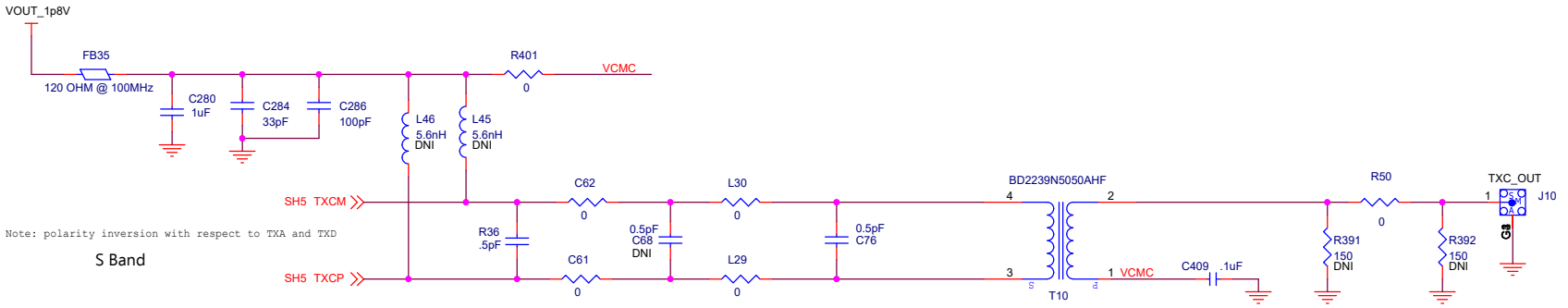
Title: DAC		
Size: B	Document Number: AFE7950EVM	Rev: A
Date: Wednesday, May 20, 2020	Sheet 5 of 32	

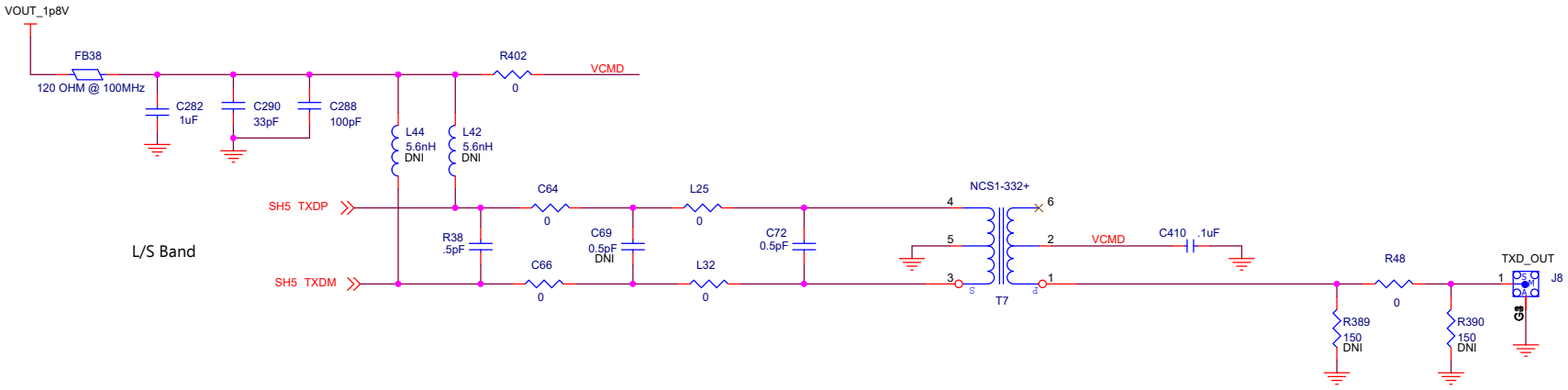




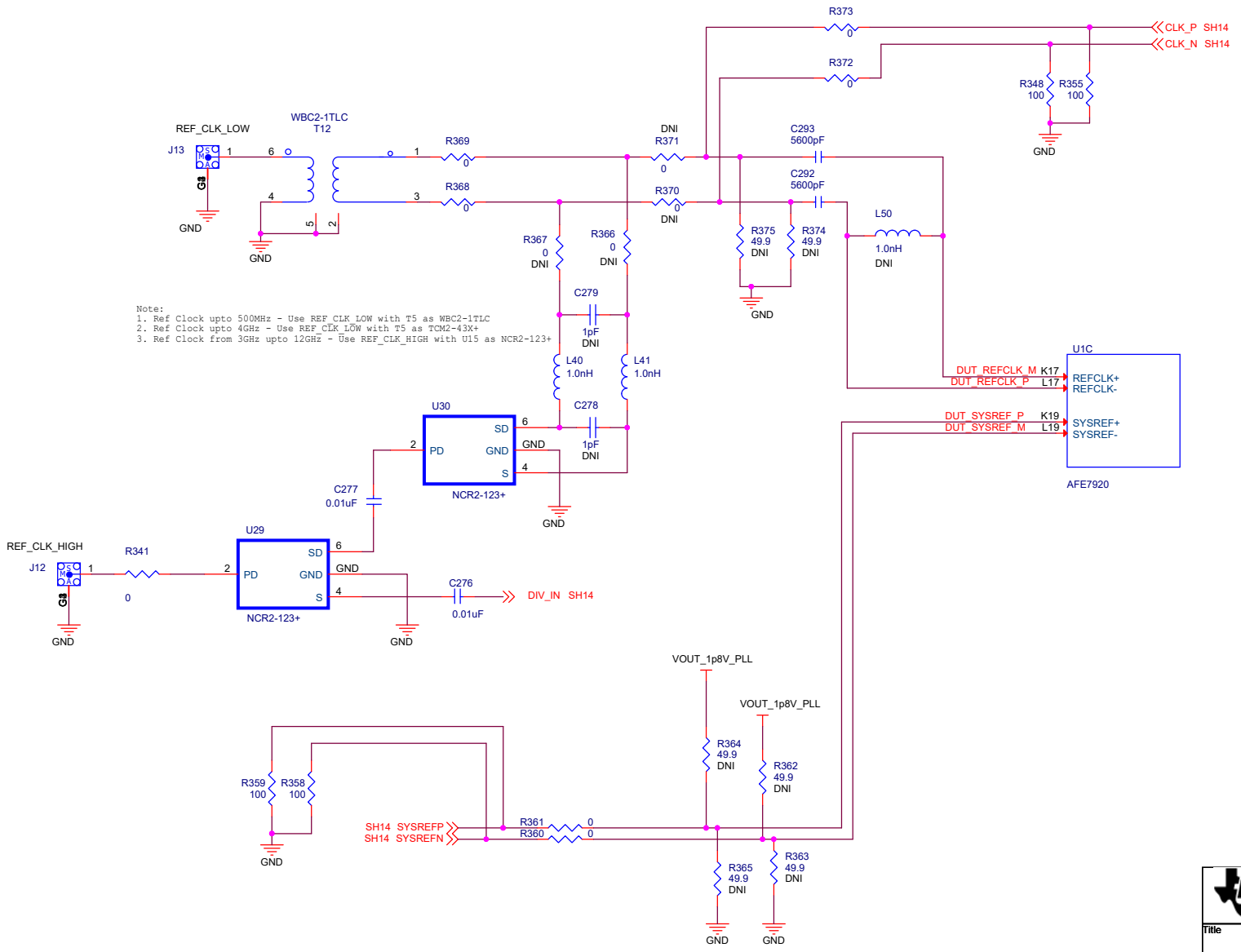
TEXAS INSTRUMENTS

Title: TXA & TXB		
Size: B	Document Number: AFE7950EVM	Rev: A
Date: Thursday, June 18, 2020	Sheet 6 of 32	



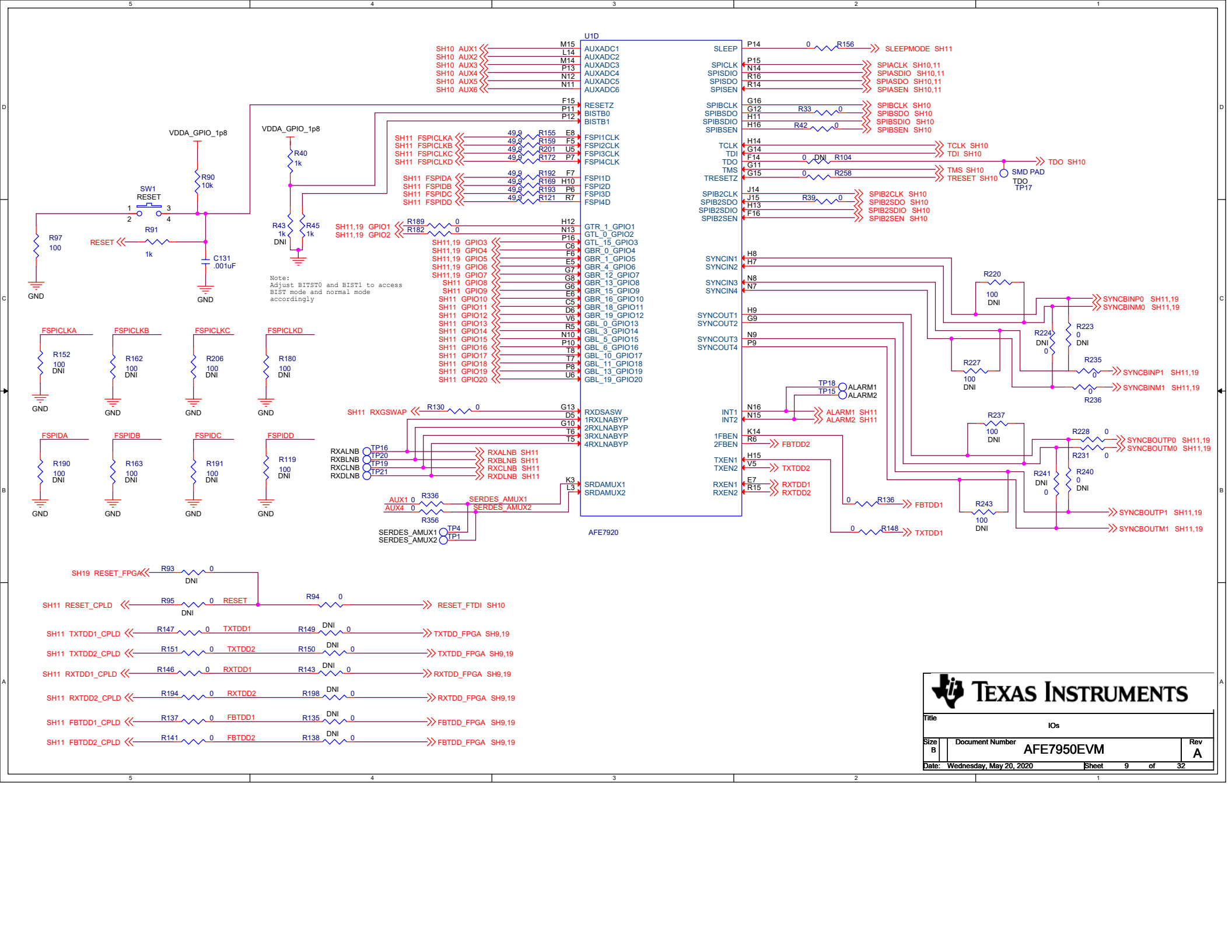


Title	TXC & TXD	
Size B	Document Number AFE7950EVM	Rev A
Date: Wednesday, May 20, 2020	Sheet 7 of 32	



TEXAS INSTRUMENTS

Title: DUT CLOCK		
Size: B	Document Number: AFE7950EVM	Rev: A
Date: Wednesday, May 20, 2020	Sheet 8 of 32	


U1D
AFE7920
VDDA_GPIO_1p8
SW1
RESET
Note:
Adjust BITST0 and BIST1 to access
BIST mode and normal mode
accordingly
SLEEPMODE SH11
SPIACLK SH10,11
SPIASDIO SH10,11
SPIASDO SH10,11
SPIASEN SH10,11
SPIBCLK SH10
SPIBSDO SH10
SPIBSDIO SH10
SPIBSEN SH10
TCLK SH10
TDI SH10
TDO SH10
TMS SH10
TRESET SH10
SMD PAD
TDO
TP17
SPIB2CLK SH10
SPIB2SDO SH10
SPIB2SDIO SH10
SPIB2SEN SH10
SYNCBINP0 SH11,19
SYNCBINM0 SH11,19
SYNCBINP1 SH11,19
SYNCBINM1 SH11,19
ALARM1 SH11
ALARM2 SH11
FBTDD2
TXTDD2
RXTDD1
RXTDD2
FBTDD1
TXTDD1
SYNCBOUTP0 SH11,19
SYNCBOUTM0 SH11,19
SYNCBOUTP1 SH11,19
SYNCBOUTM1 SH11,19
RXALNB SH11
RXBLNB SH11
RXCLNB SH11
RXDLNB SH11
SERDES_AMUX1
SERDES_AMUX2
RESET_FTDI SH10
TXTDD_FPGA SH9,19
RXTDD_FPGA SH9,19
FBTDD_FPGA SH9,19
Texas Instruments
Title
IOs
Size B
Document Number
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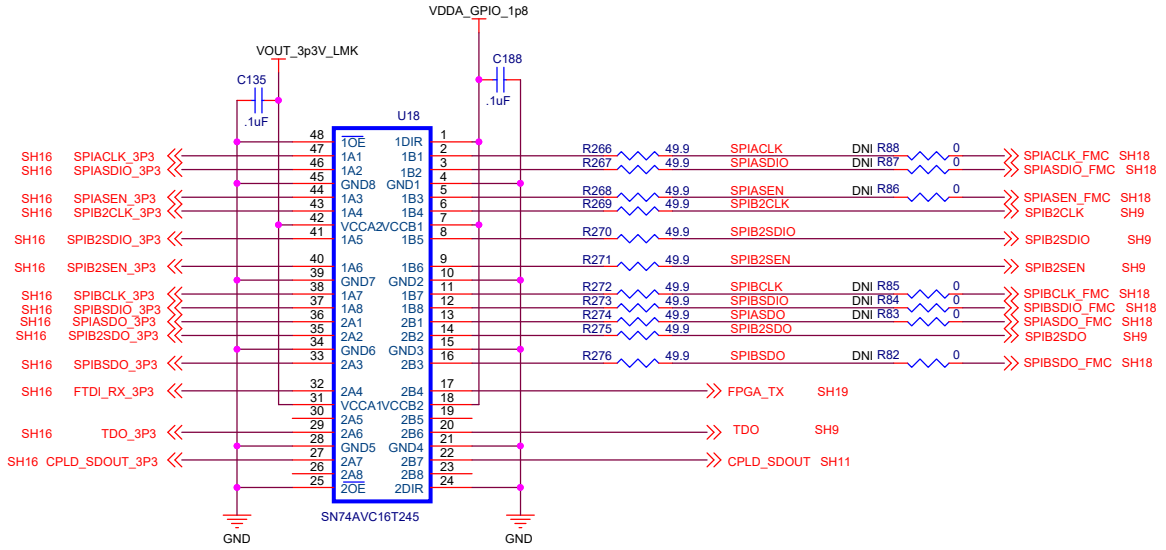
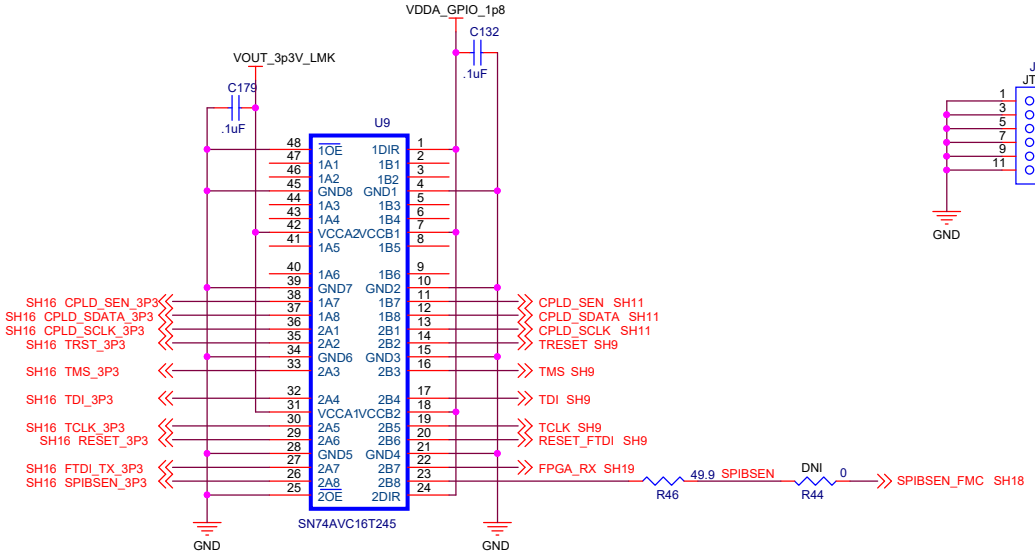
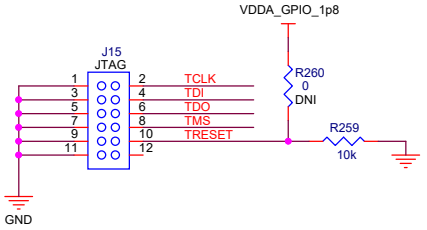
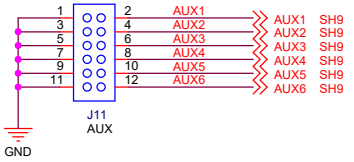
Date: Wednesday, May 20, 2020
Sheet 9 of 32









TEXAS INSTRUMENTS

Title	LEVEL SHIFTERS	
Size B	Document Number AFE7950EVM	Rev A
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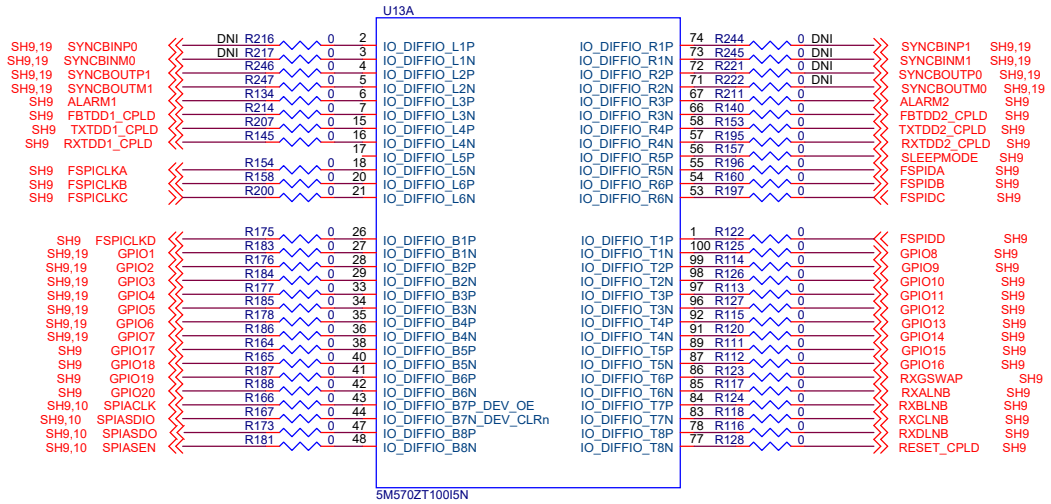
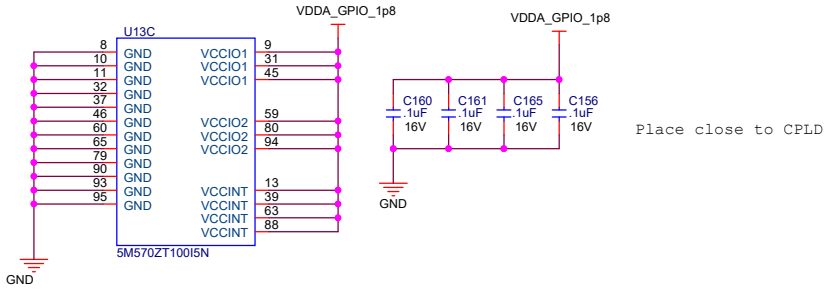
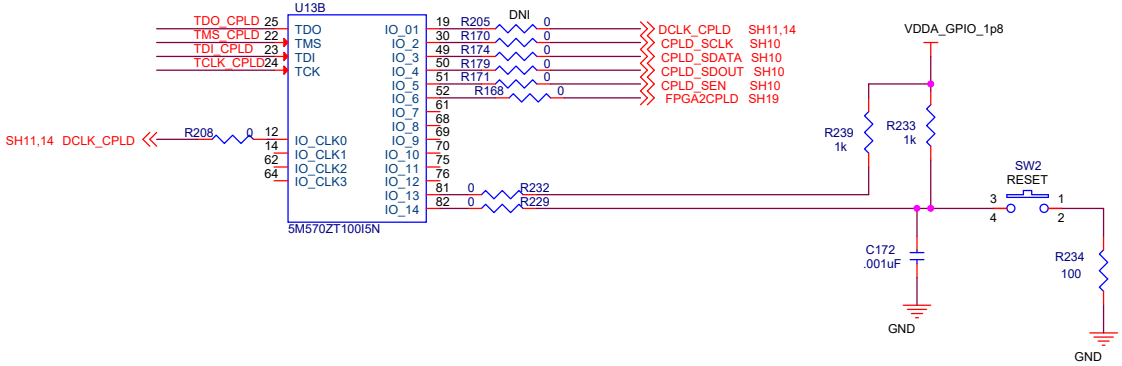
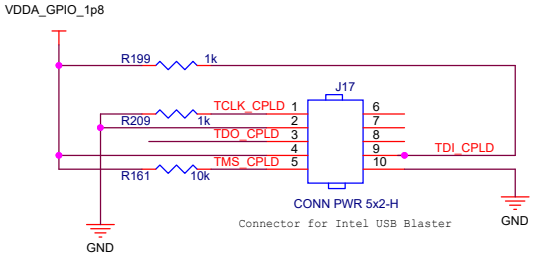


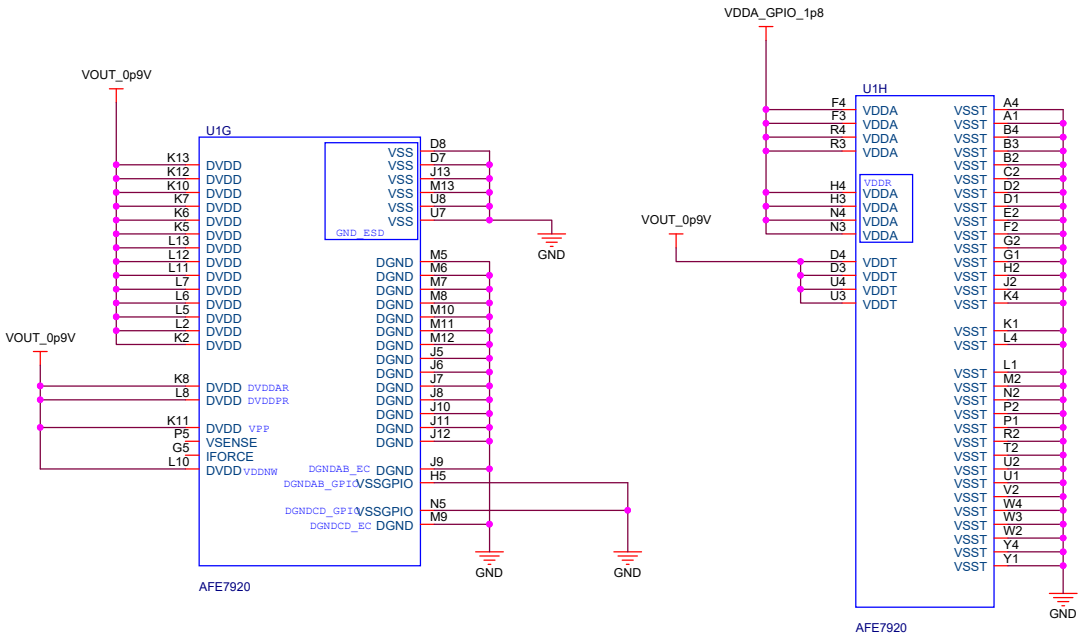






TEXAS INSTRUMENTS

Title	CPLD	
Size B	Document Number AFE7950EVM	Rev A
Date: Wednesday, May 20, 2020	Sheet 11 of 32	



TEXAS INSTRUMENTS

Title	DUT POWER 1	
Size B	Document Number AFE7950EVM	Rev A
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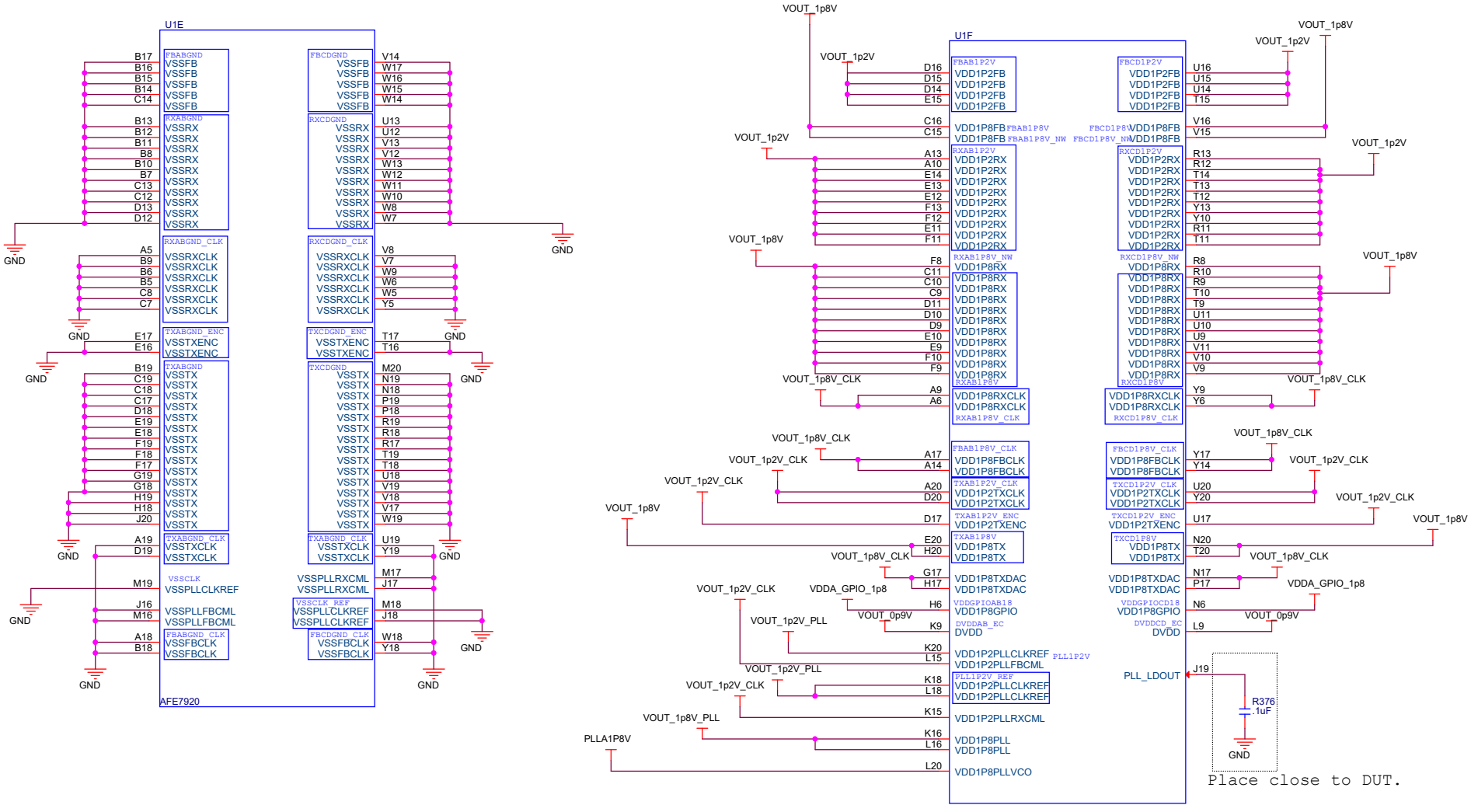
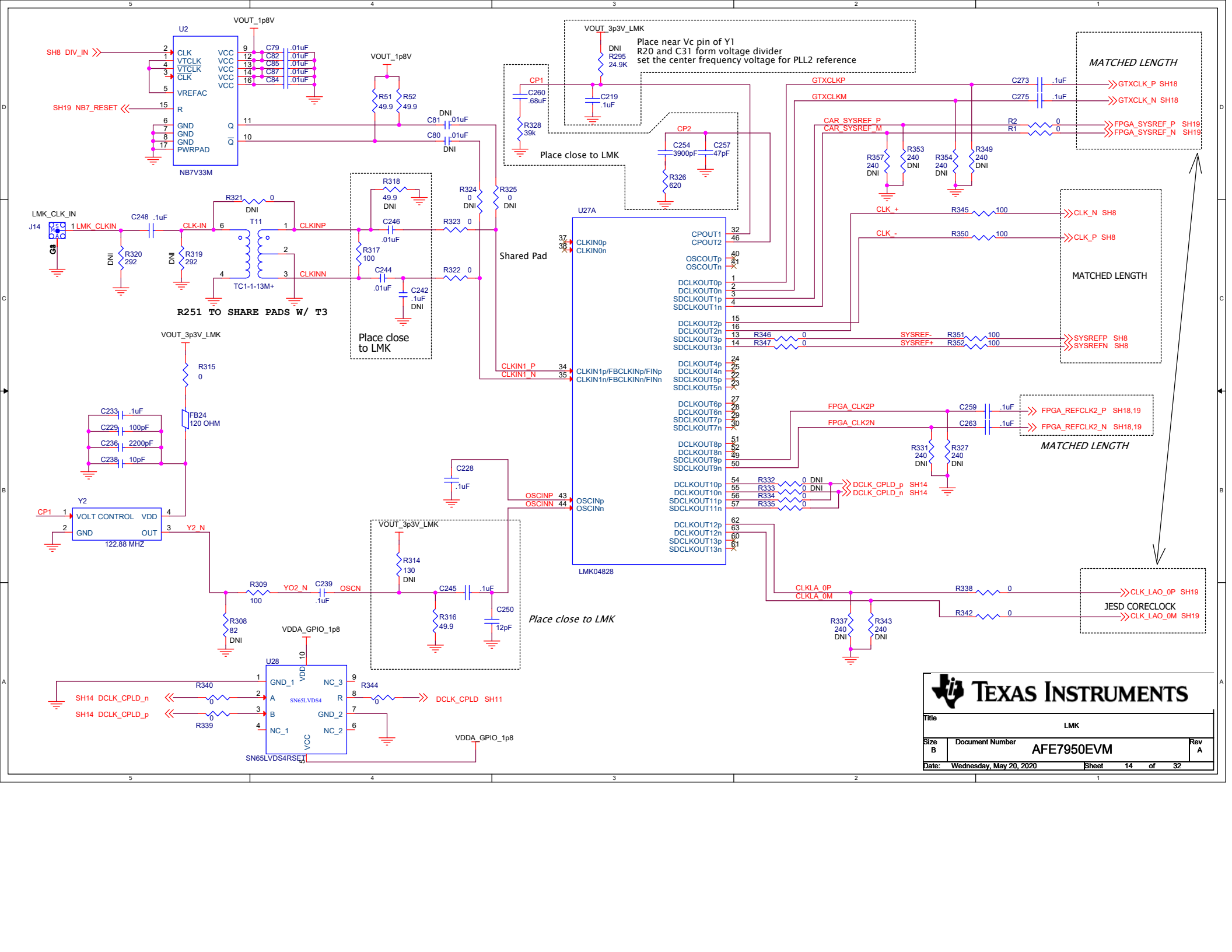


TEXAS INSTRUMENTS

Title	DUT POWER 1	
Size B	Document Number AFE7950EVM	Rev A
Date: Wednesday, May 20, 2020	Sheet 13 of 32	


U2
NB7V33M
VOUT_1p8V
SH8 DIV_IN
SH19 NB7_RESET
CLK
VTCLK
VTCLK
CLK
VREFAC
R
GND
GND
GND
PWRPAD
VCC
Q
Q
C79 .01uF
C82 .01uF
C85 .01uF
C87 .01uF
C84 .01uF
R51 49.9
R52 49.9
C81 .01uF DNI
C80 .01uF DNI
VOUT_3p3V_LMK
DNI
R295
24.9K
Place near Vc pin of Y1
R20 and C31 form voltage divider
set the center frequency voltage for PLL2 reference
CP1
C260 .68uF
R328 39k
Place close to LMK
CP2
C254 3900pF
C257 47pF
R326 620
MATCHED LENGTH
GTXCLKP
GTXCLKM
C273 .1uF
C275 .1uF
GTXCLK_P SH18
GTXCLK_N SH18
CAR_SYSREF_P
CAR_SYSREF_M
R2 0
R1 0
FPGA_SYSREF_P SH19
FPGA_SYSREF_N SH19
R357 240 DNI
R353 240 DNI
R354 240 DNI
R349 240 DNI
LMK_CLK_IN
J14
LMK_CLKIN
C248 .1uF
CLK-IN
R321 0 DNI
T11
TC1-1-13M+
CLKINP
CLKINN
R320 292 DNI
R319 292 DNI
R318 49.9 DNI
C246 .01uF
R317 100
C244 .01uF
C242 .1uF DNI
R324 0 DNI
R325 0 DNI
R323 0
R322 0
Shared Pad
R251 TO SHARE PADS W/ T3
Place close to LMK
U27A
CLKIN0p
CLKIN0n
CLKIN1_P
CLKIN1_N
CLKIN1p/FBCLKINp/FINp
CLKIN1n/FBCLKINn/FINn
OSCINP
OSCINN
OSCINp
OSCINn
CPOUT1
CPOUT2
OSCOUTp
OSCOUTn
DCLKOUT0p
DCLKOUT0n
SDCLKOUT1p
SDCLKOUT1n
DCLKOUT2p
DCLKOUT2n
SDCLKOUT3p
SDCLKOUT3n
DCLKOUT4p
DCLKOUT4n
SDCLKOUT5p
SDCLKOUT5n
DCLKOUT6p
DCLKOUT6n
SDCLKOUT7p
SDCLKOUT7n
DCLKOUT8p
DCLKOUT8n
SDCLKOUT9p
SDCLKOUT9n
DCLKOUT10p
DCLKOUT10n
SDCLKOUT11p
SDCLKOUT11n
DCLKOUT12p
DCLKOUT12n
SDCLKOUT13p
SDCLKOUT13n
LMK04828
CLK_+
CLK_-
R345 100
R350 100
CLK_N SH8
CLK_P SH8
MATCHED LENGTH
R346 0
R347 0
SYSREF-
SYSREF+
R351 100
R352 100
SYSREFP SH8
SYSREFN SH8
FPGA_CLK2P
FPGA_CLK2N
C259 .1uF
C263 .1uF
FPGA_REFCLK2_P SH18,19
FPGA_REFCLK2_N SH18,19
MATCHED LENGTH
R331 240 DNI
R327 240 DNI
R332 0 DNI
R333 0 DNI
R334 0
R335 0
DCLK_CPLD_p SH14
DCLK_CPLD_n SH14
CLKLA_0P
CLKLA_0M
R338 0
R342 0
CLK_LAO_0P SH19
CLK_LAO_0M SH19
JESD CORECLOCK
R337 240 DNI
R343 240 DNI
VOUT_3p3V_LMK
R315 0
FB24 120 OHM
C233 .1uF
C229 100pF
C236 2200pF
C238 10pF
Y2
VOLT CONTROL
VDD
GND
OUT
122.88 MHZ
Y2_N
C228 .1uF
R314 130 DNI
R309 100
YO2_N
C239 .1uF
OSCN
C245 .1uF
R316 49.9
C250 12pF
Place close to LMK
R308 82 DNI
VDDA_GPIO_1p8
U28
SN65LVDS4
SN65LVDS4RSET
GND_1
A
B
NC_1
NC_3
R
GND_2
NC_2
VDD
VCC
R340 0
R339 0
R344 0
SH14 DCLK_CPLD_n
SH14 DCLK_CPLD_p
DCLK_CPLD SH11
VDDA_GPIO_1p8
TEXAS INSTRUMENTS
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LMK
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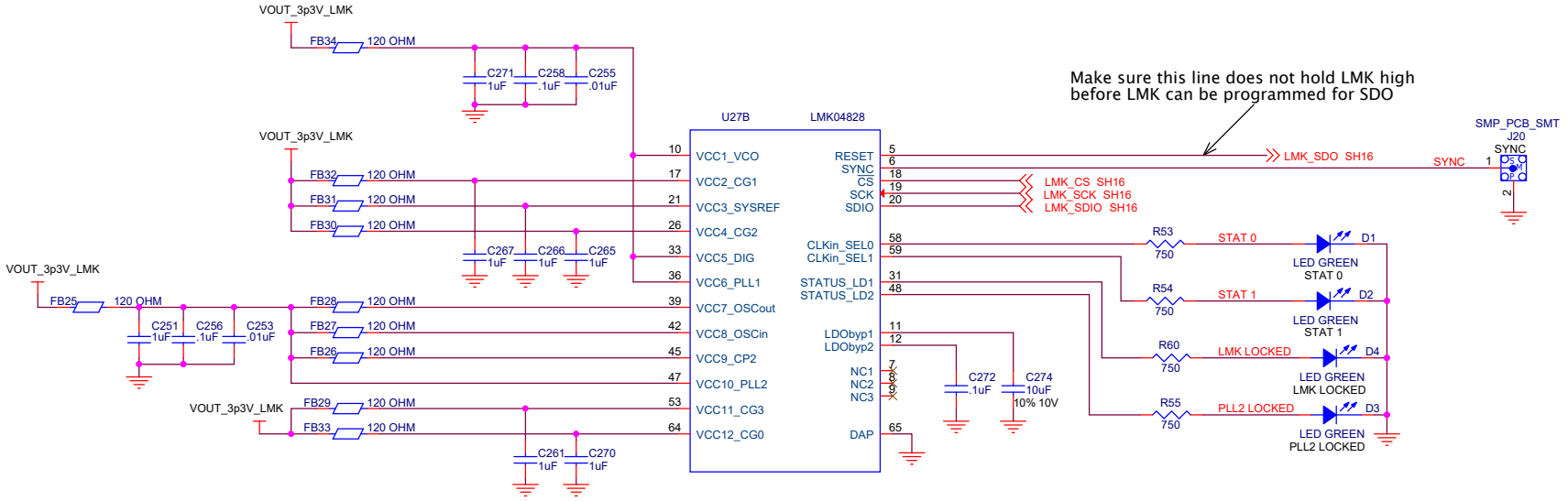

TEXAS INSTRUMENTS

Title	LMK	
Size B	Document Number AFE7950EVM	Rev A
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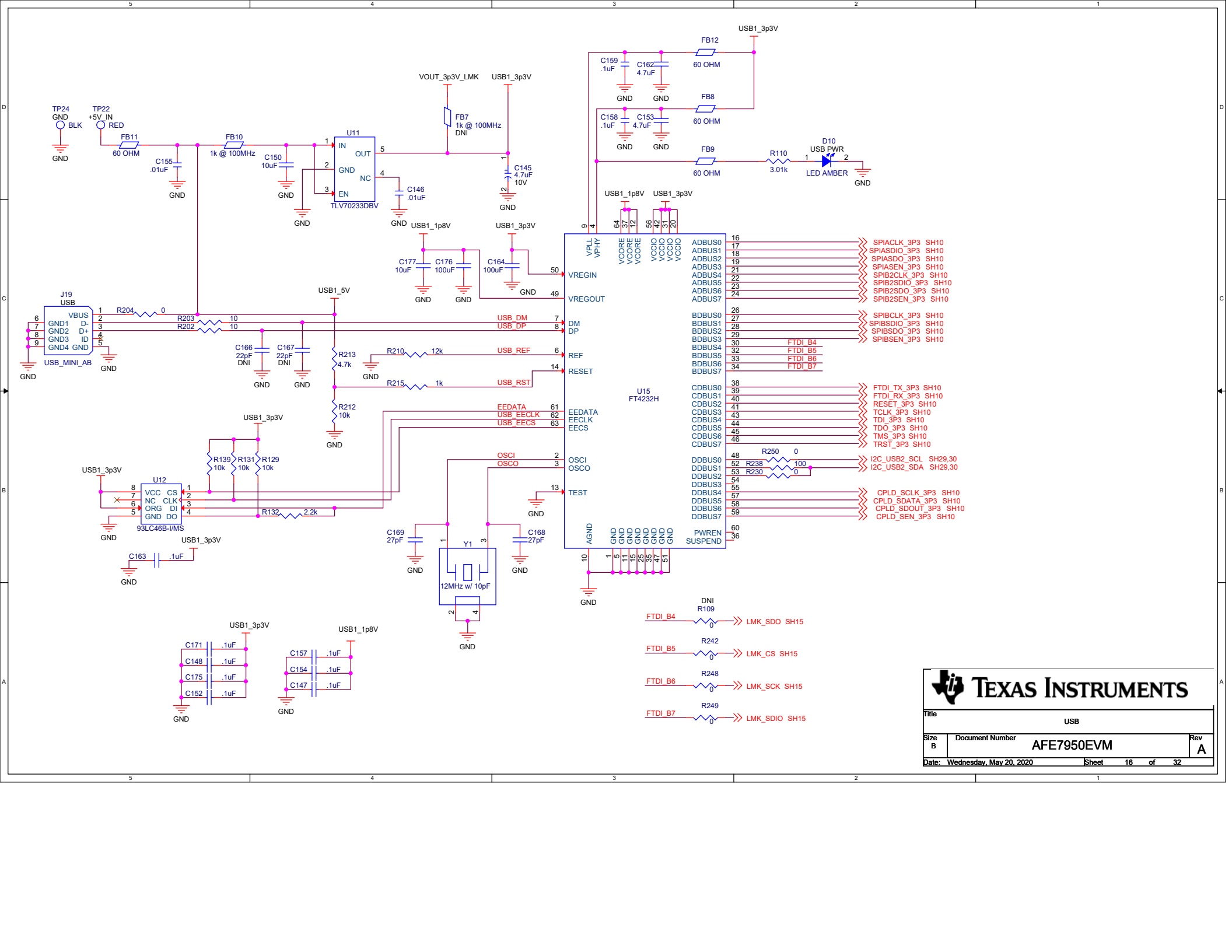

TEXAS INSTRUMENTS

Title	USB	
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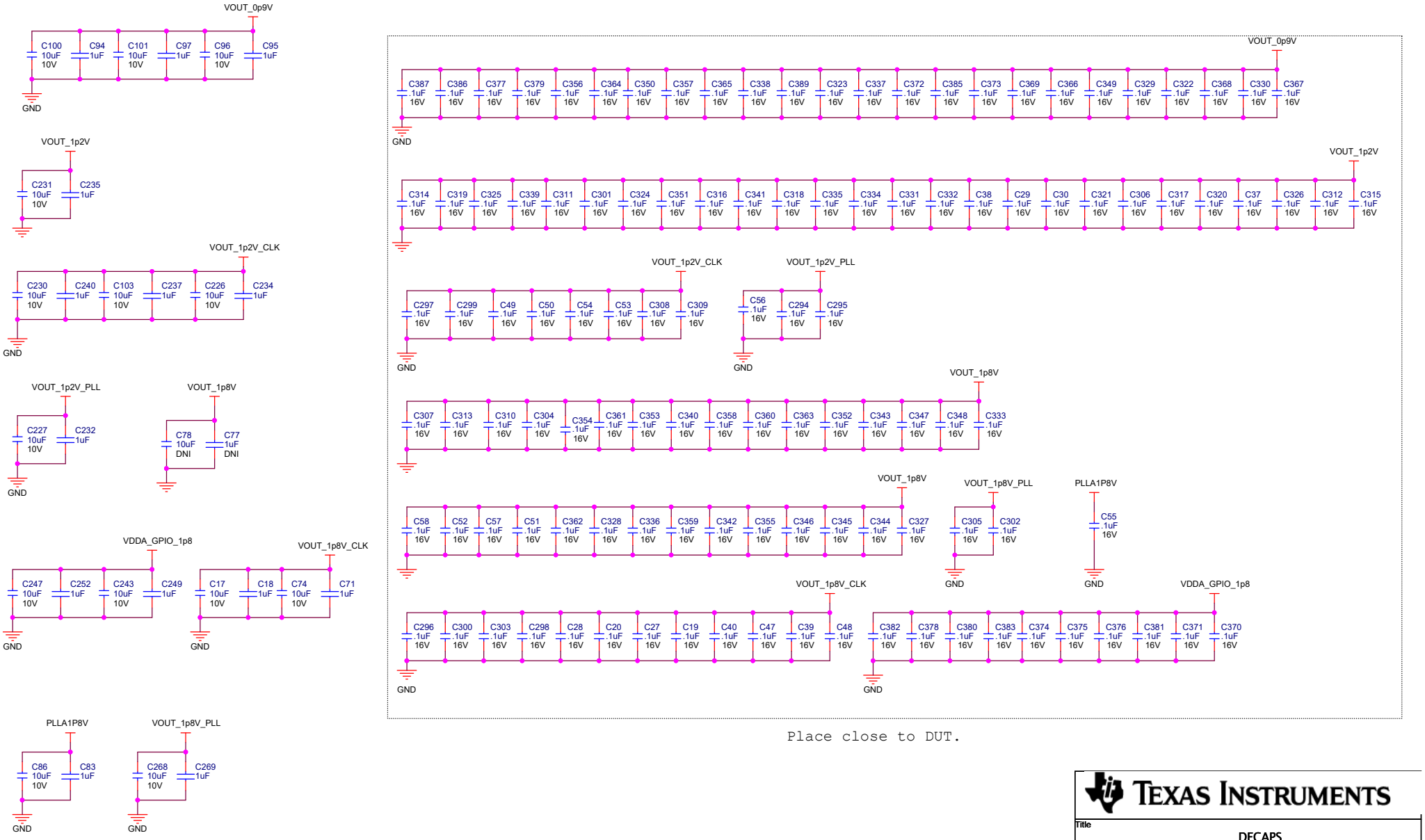
Date: Wednesday, May 20, 2020	Sheet 16 of 32	



Place close to DUT.

TEXAS INSTRUMENTS

Title: DECAPS		
Size: B	Document Number: AFE7950EVM	Rev: A
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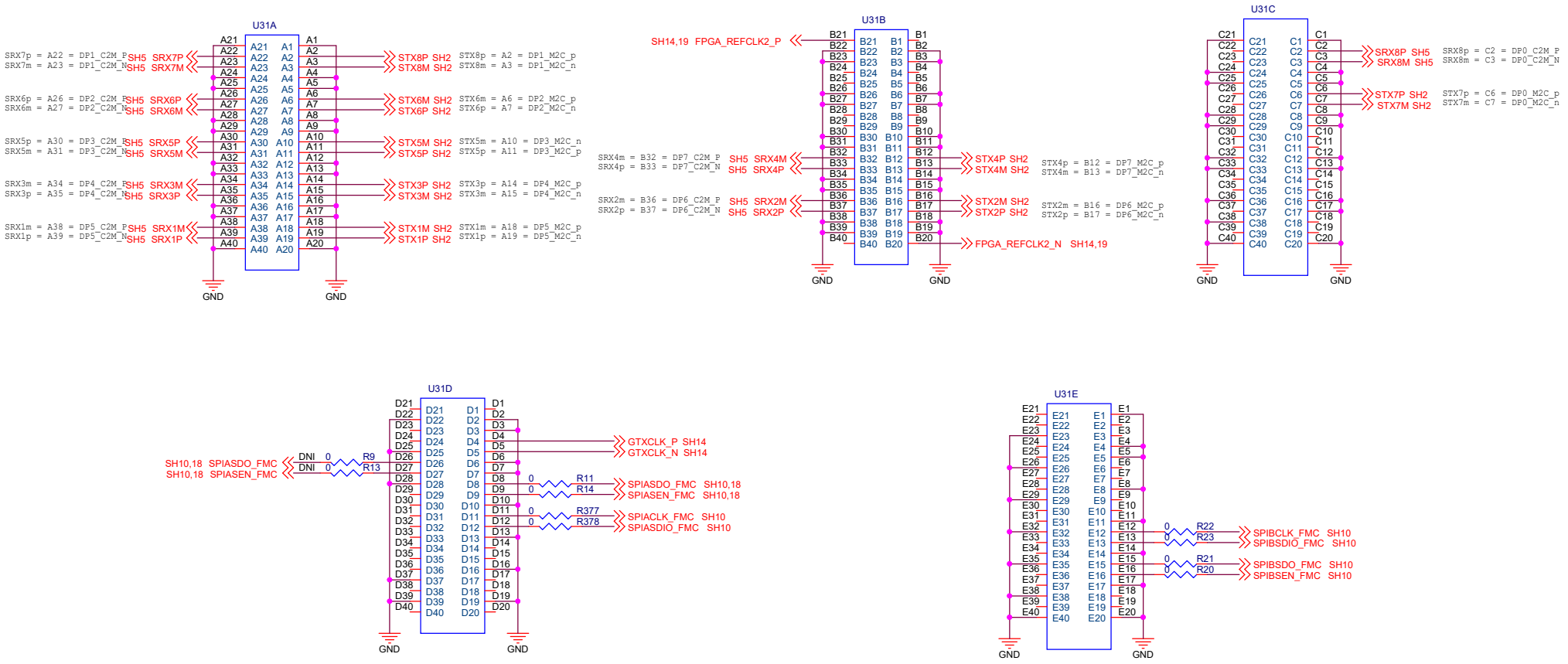

TEXAS INSTRUMENTS

Title	FMC	
Size B	Document Number AFE7950EVM	Rev A
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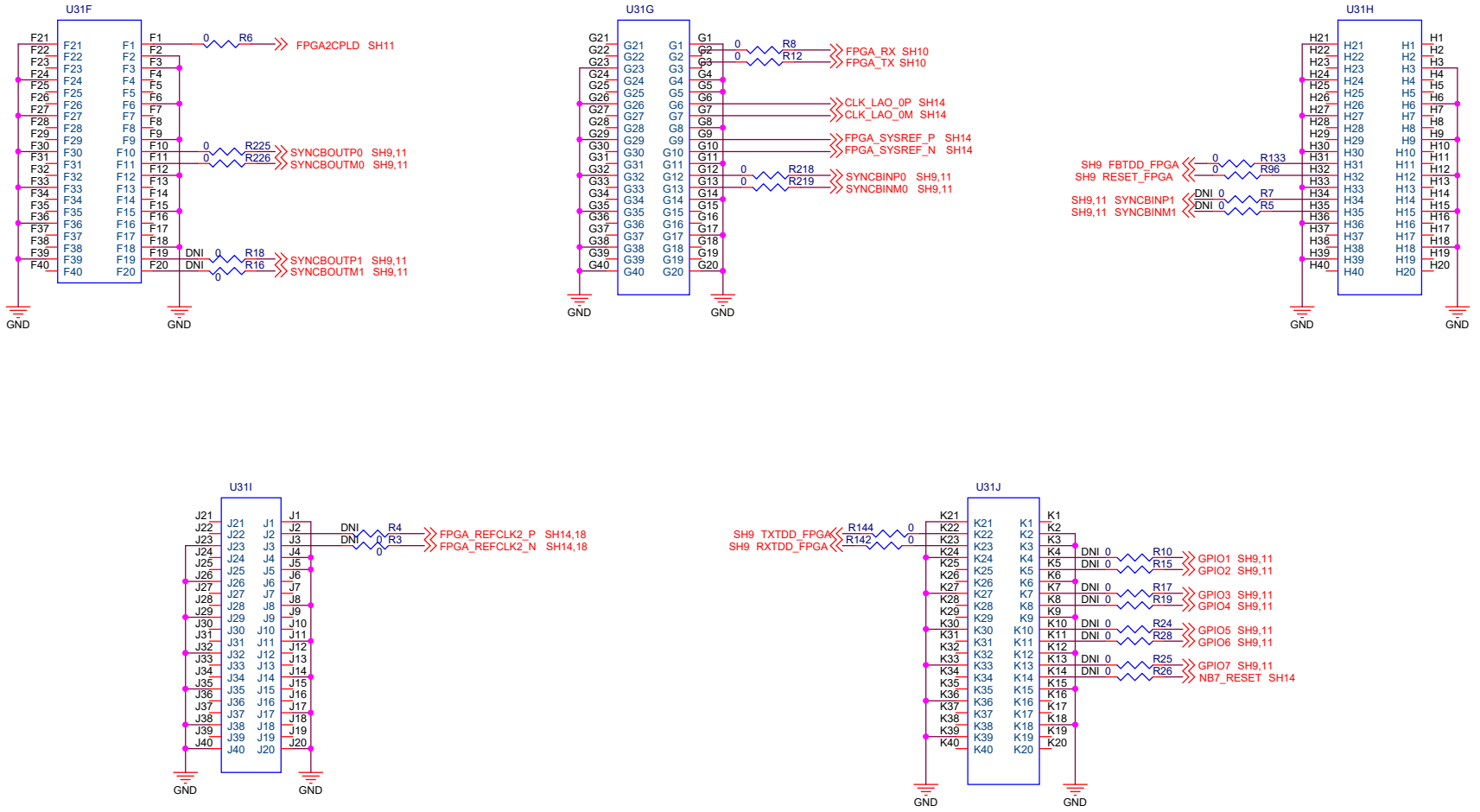

TEXAS INSTRUMENTS

Title	FMC	
Size B	Document Number AFE7950EVM	Rev A
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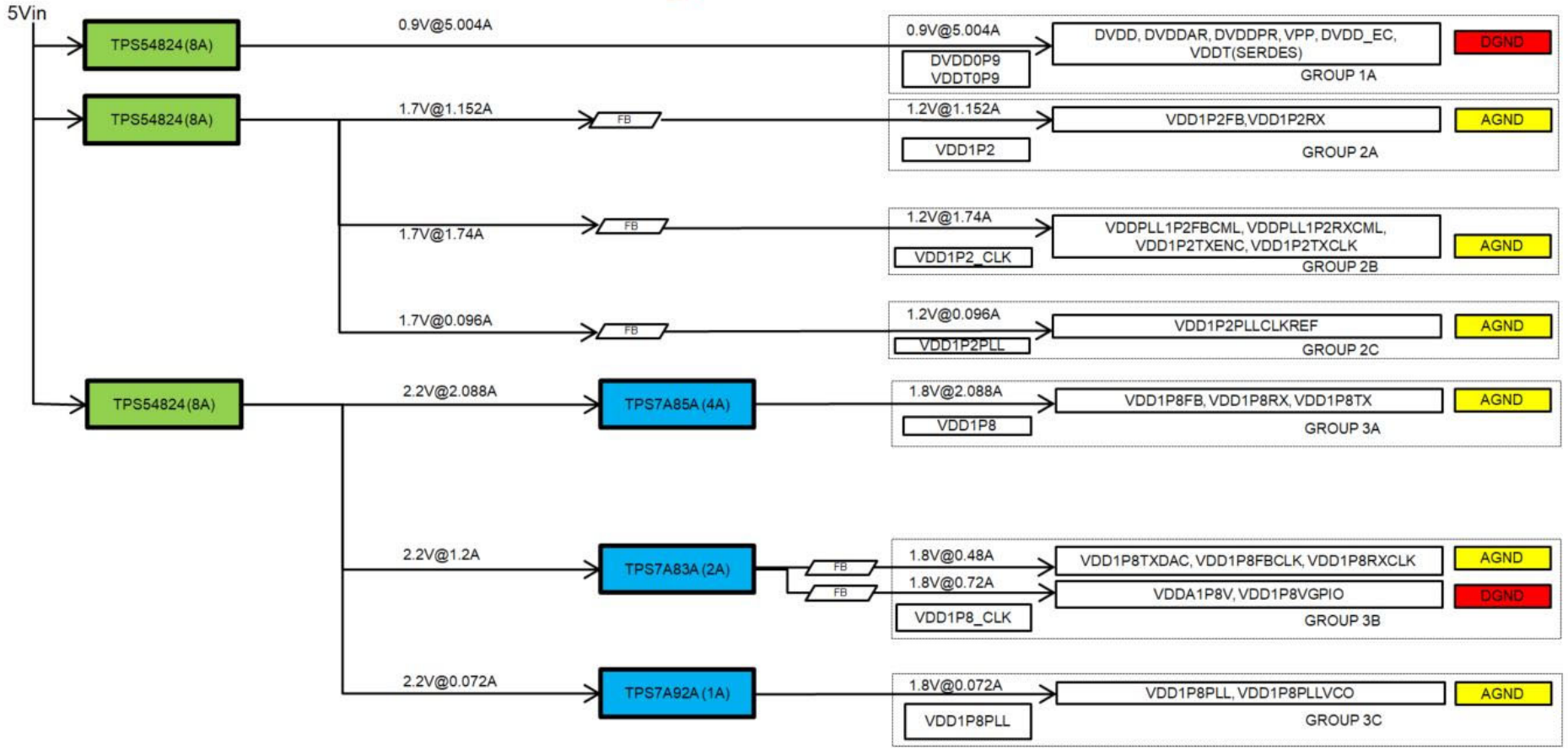
1x AFE78xx Block Diagram



TEXAS INSTRUMENTS

Title: POWER TREE		
Size: B	Document Number: AFE7950EVM	Rev: A
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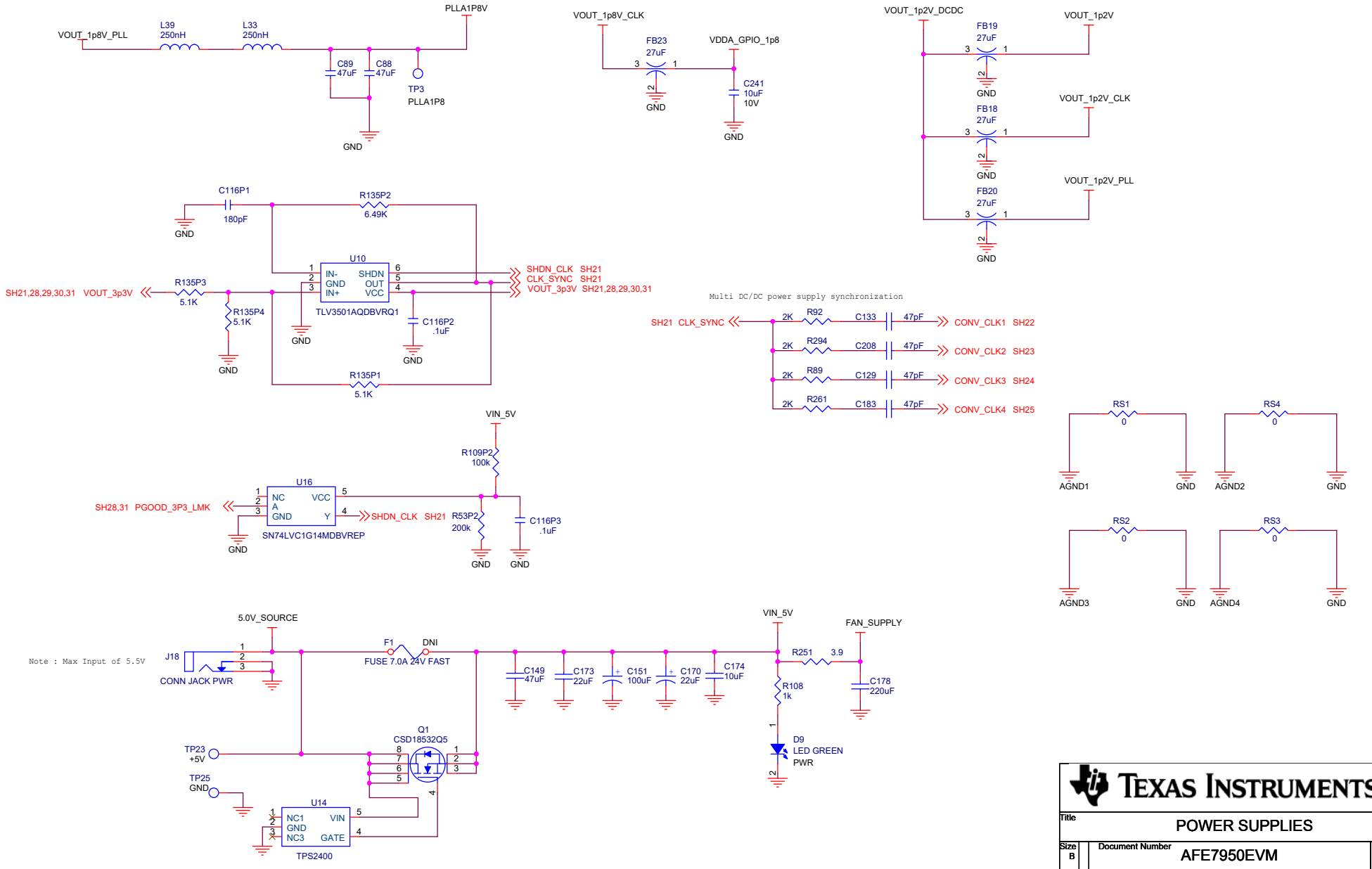

TEXAS INSTRUMENTS

Title	POWER SUPPLIES	
Size B	Document Number AFE7950EVM	Rev A
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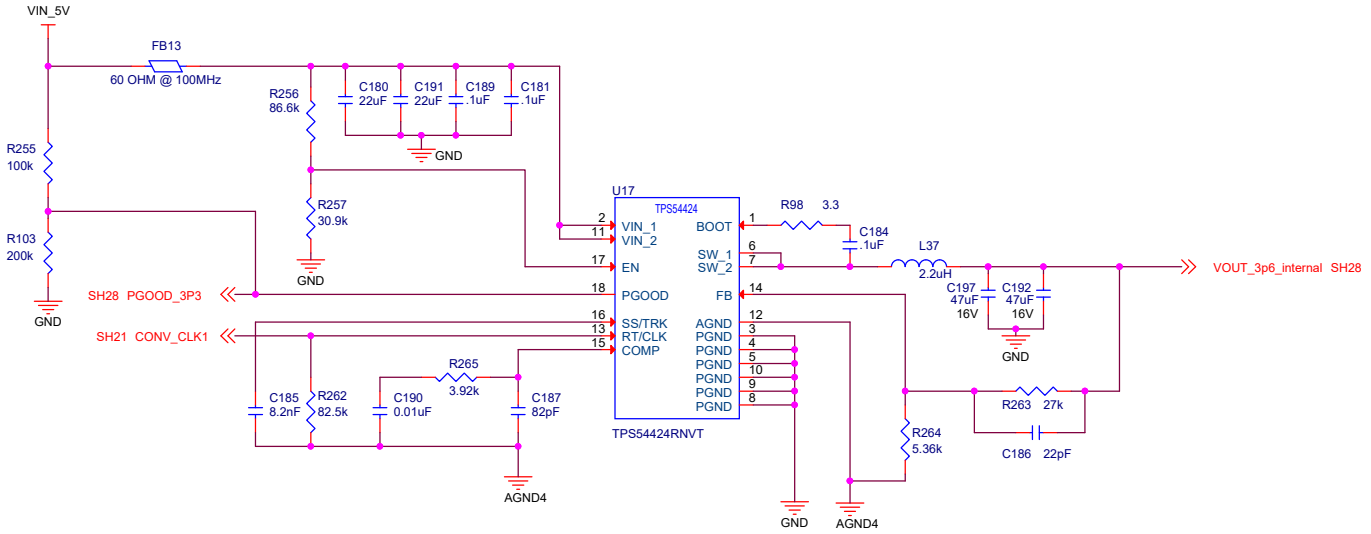

TEXAS INSTRUMENTS

Title	POWER SUPPLIES	
Size B	Document Number AFE7950EVM	Rev A
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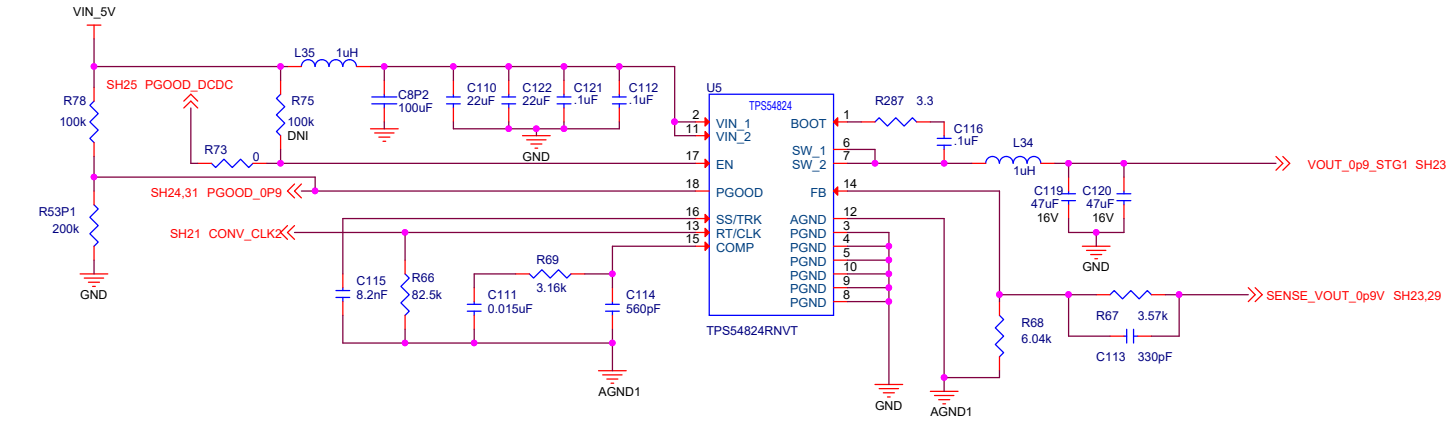
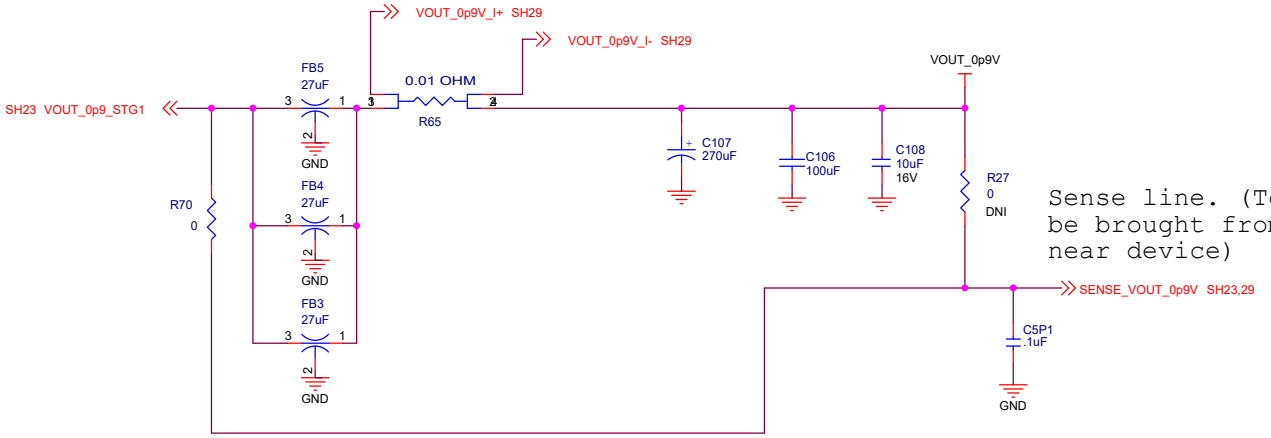
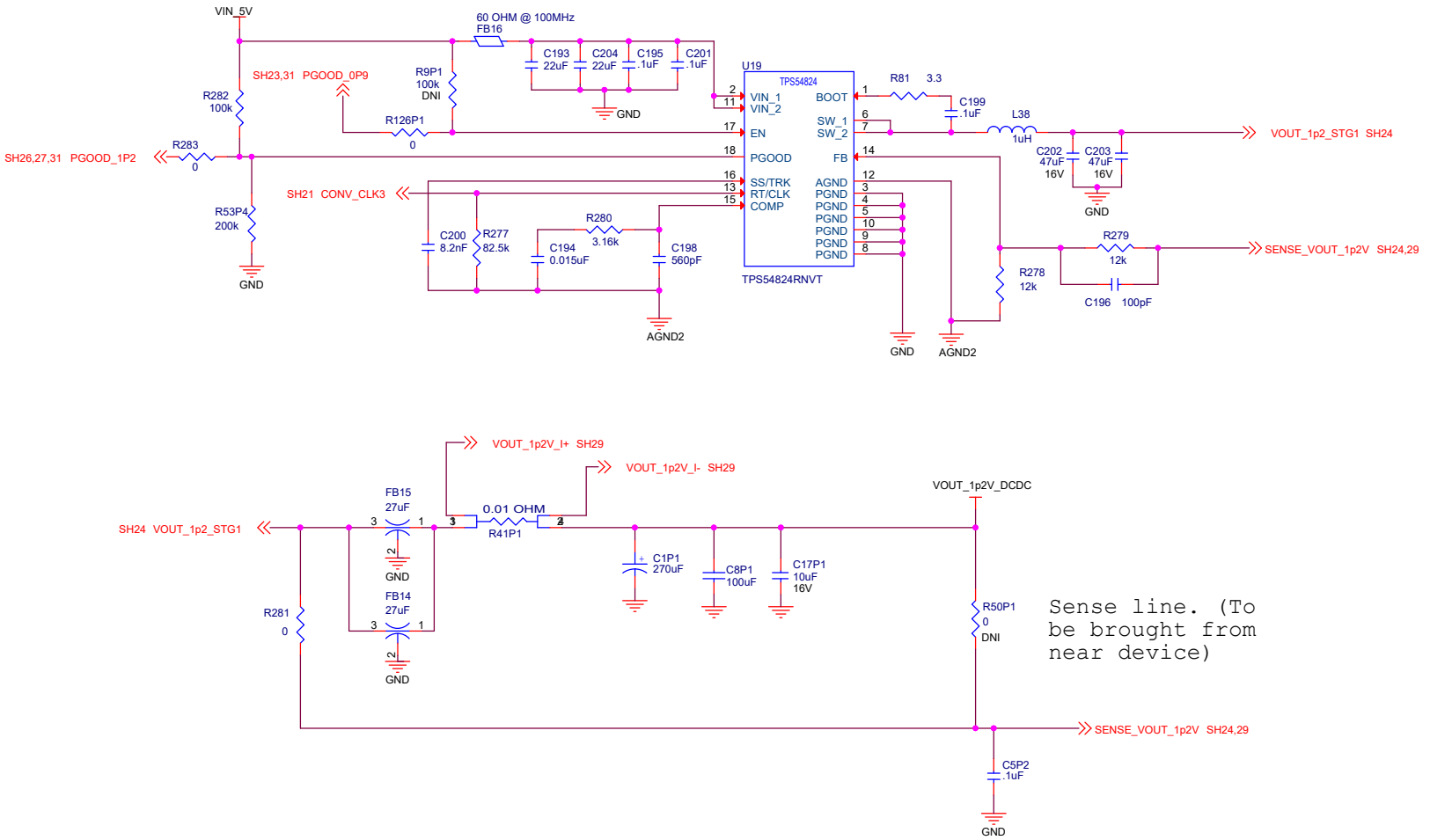




Sense line. (To be brought from near device)

TEXAS INSTRUMENTS

Title	POWER SUPPLIES	
Size B	Document Number AFE7950EVM	Rev A
Date: Wednesday, May 20, 2020	Sheet 23 of 32	



TEXAS INSTRUMENTS

Title	POWER SUPPLIES	
Size B	Document Number AFE7950EVM	Rev A
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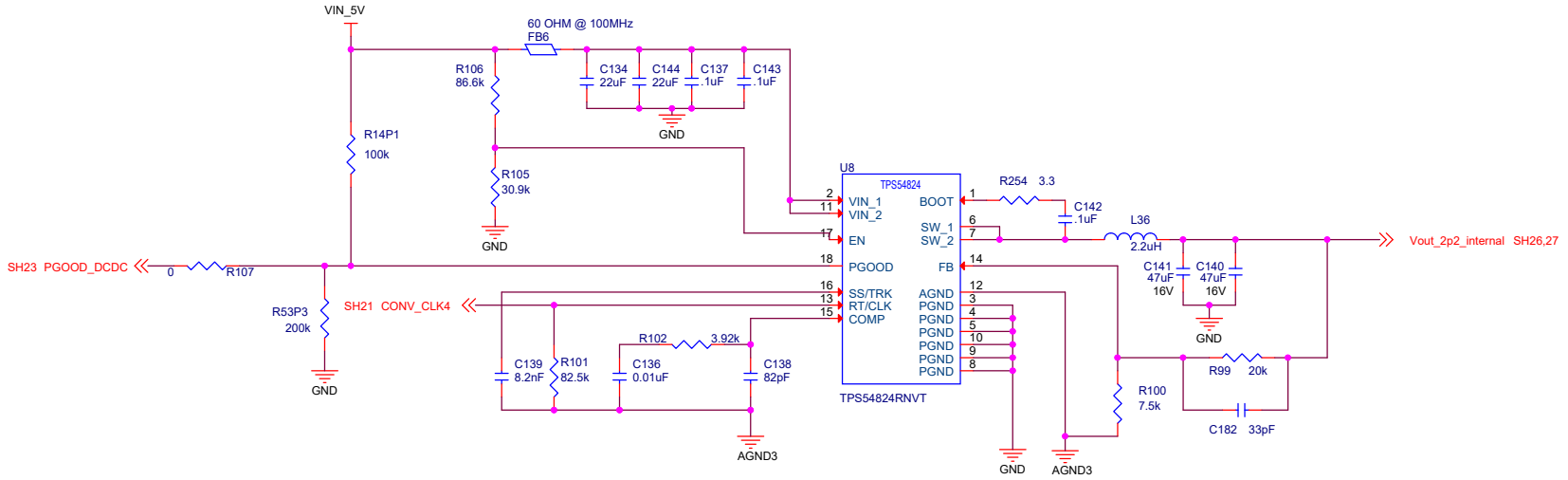

TEXAS INSTRUMENTS

Title	POWER SUPPLIES	
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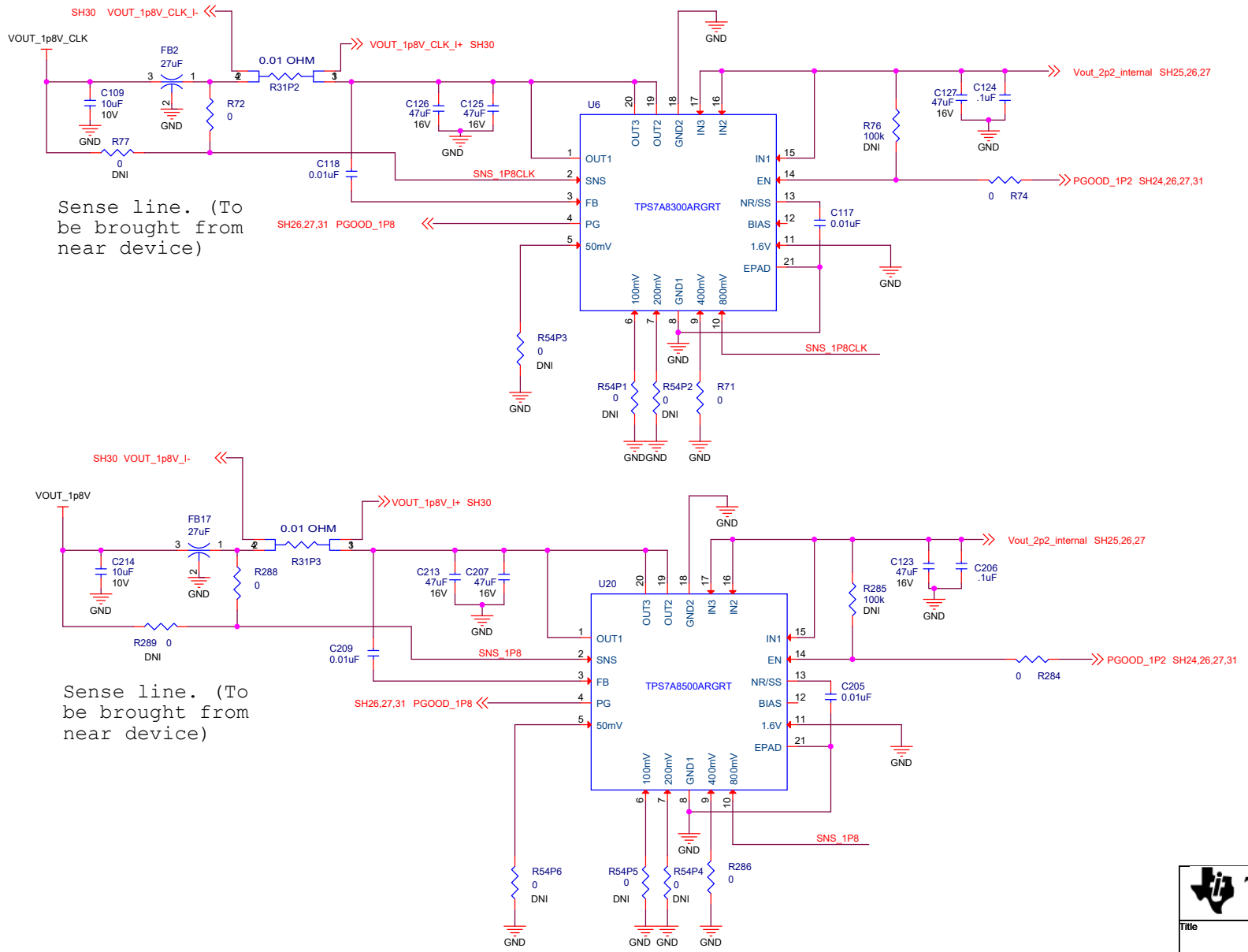
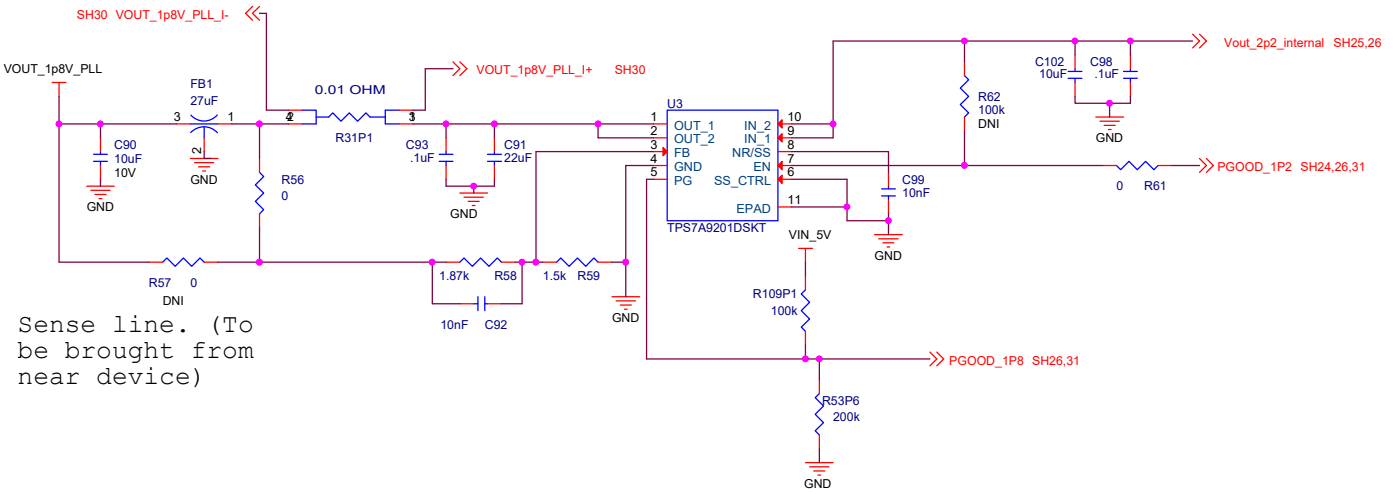


TEXAS INSTRUMENTS

Title	POWER SUPPLIES	
Size B	Document Number AFE7950EVM	Rev A
Date: Wednesday, May 20, 2020	Sheet 26 of 32	



Sense line. (To be brought from near device)

TEXAS INSTRUMENTS

Title	POWER SUPPLIES	
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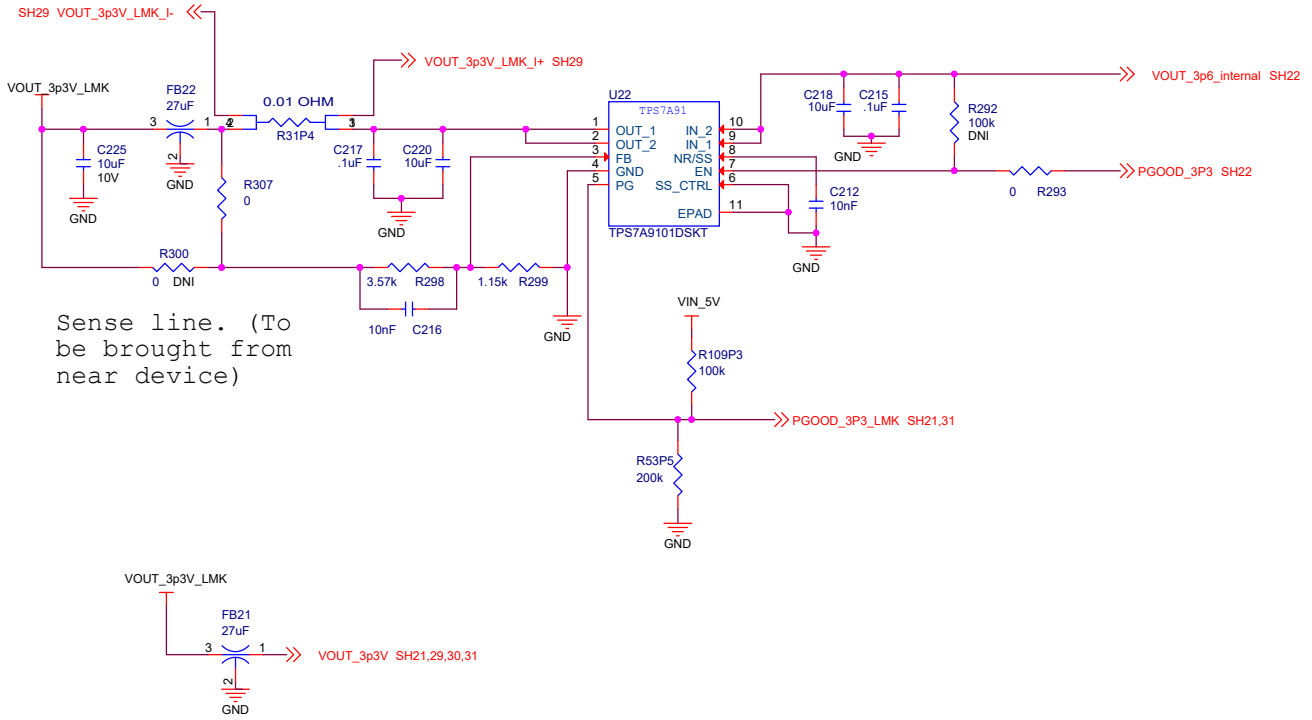

TEXAS INSTRUMENTS

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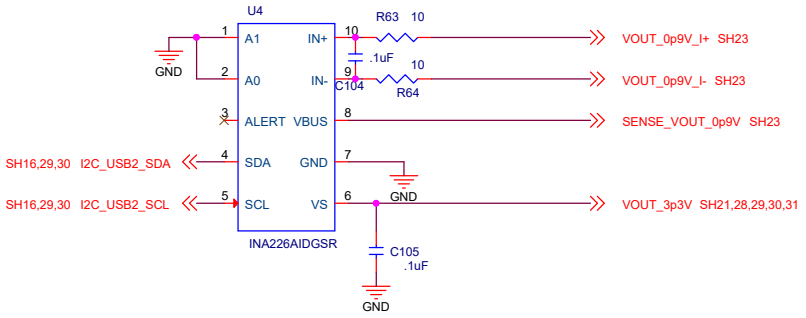
Addr = 0x40



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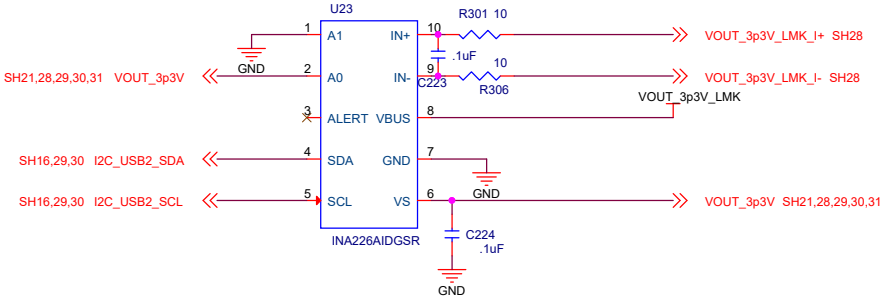

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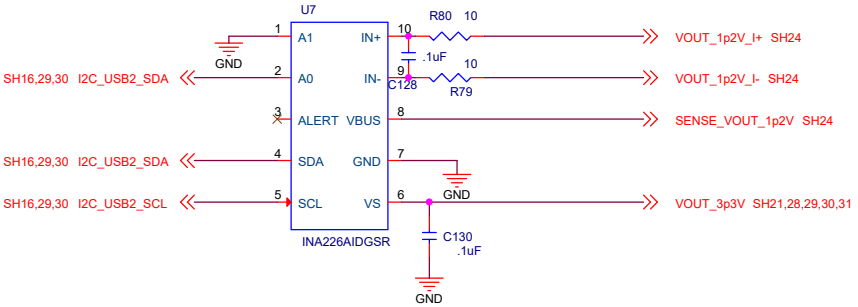

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Title	POWER SUPPLIES		
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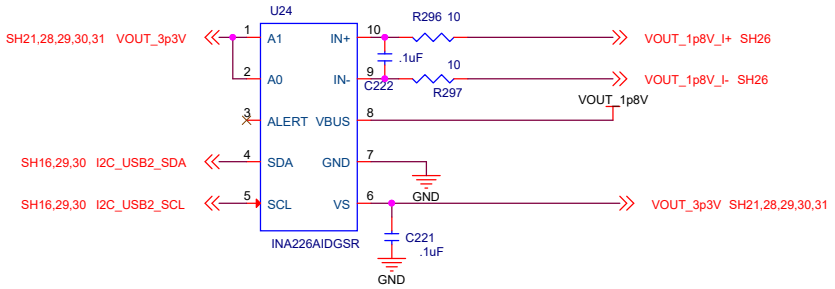

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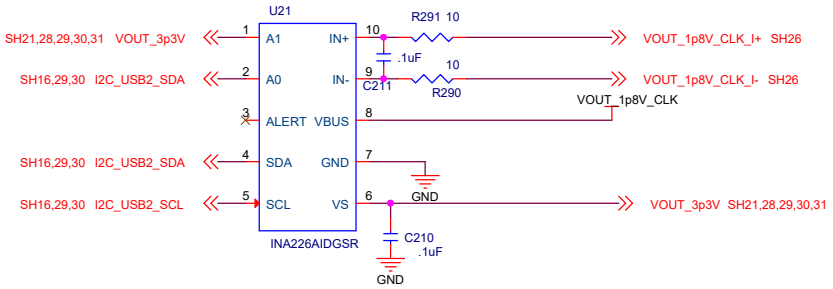

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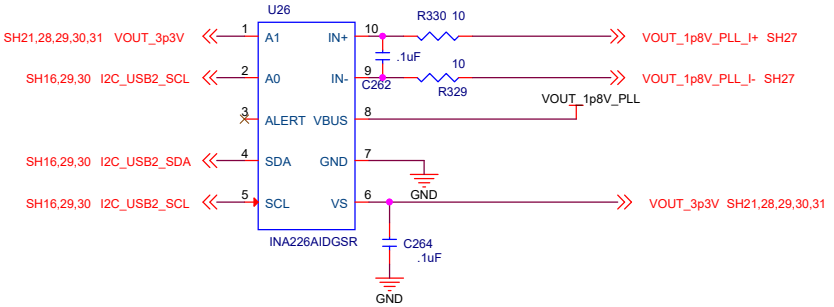

All VBUS to be connected to sense lines of LDO

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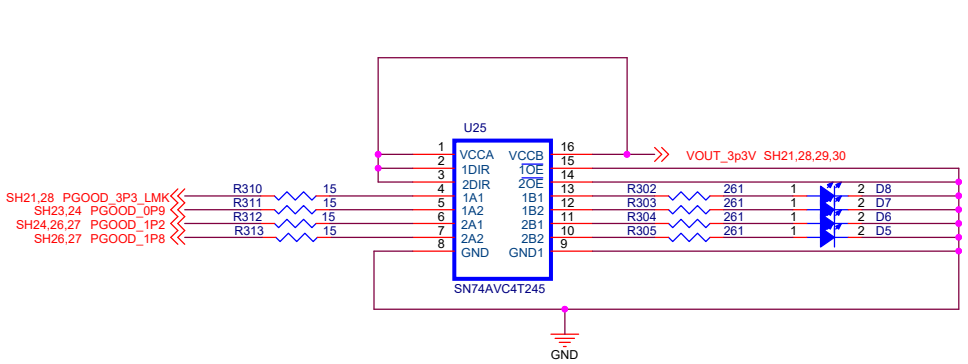

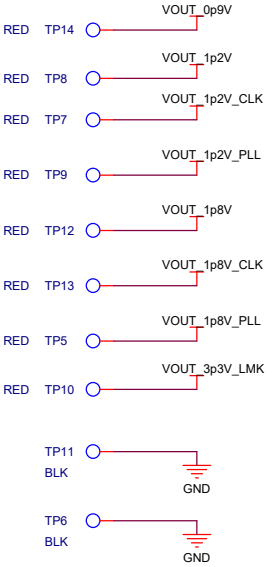

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MP3_HS1

HEAT SINK 17MM X 17MM X 19.5MM
ATS-54170R-C1-R0

MP4

17mm FAN FOR HEATSINK
GM0517PDV2-8.GN

Screws, M2-0.4 x 12mm DIN 7985 PHIL Pan Head

Screws, M2-0.4 x 12mm DIN 7985 PHIL Pan Head

MT1 1
STANDOFF, 4-40, 3/16 Rd x 1 3/16 Length, ALUM

MT2 1
STANDOFF, 4-40, 3/16 Rd x 1 3/16 Length, ALUM

MT3 1
STANDOFF, 4-40, 3/16 Rd x 1 3/16 Length, ALUM

MT4 1
STANDOFF, 4-40, 3/16 Rd x 1 3/16 Length, ALUM

MT5 1
STANDOFF, 4-40, 3/16 Rd x 1 3/16 Length, ALUM

MT6 1
STANDOFF, 4-40, 3/16 Rd x 1 3/16 Length, ALUM

MP6_P1

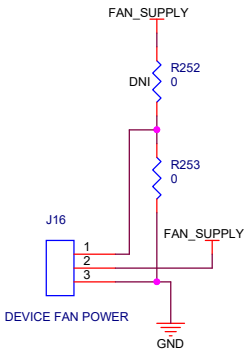
MECH

Mating Connector for J16
22-01-3037
For fan wires assembly; use crimp terminal 0008550102

0008550102

0008550102

Printed Circuit Board, AFE7950



SCREW, PHIL, 4-40x3/8", SS

SCREW, PHIL, 4-40x3/8", SS

SCREW, PHIL, 4-40x3/8", SS

SCREW, PHIL, 4-40x3/8", SS

SCREW, PHIL, 4-40x3/8", SS

SCREW, PHIL, 4-40x3/8", SS

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