AFE79xx: TX DSA Gain/Phase Calibration

Texas Instruments

High Speed Data Converters

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TX DSA – Gain/Phase Calibration

- The TX DSA Gain/Phase Calibration has two modes of operation.
  1. Gain/Phase Calibration Mode
  2. Calibration Packet Load Mode

- Gain/Phase Calibration Mode: The calibration mode operation is performed once for each device, as part of factory calibration.
  - During the calibration mode, a test tone is transmitted and looped-back to enable the device to estimate the gain and phase error as a function of the TX DSA gain steps.
  - The gain/phase parameters are computed for the TX DSA in each of the 4 transmitters.
  - The estimated gain/phase parameters are to be read by the host and stored in a non-volatile memory.

- Calibration Packet Load Mode: The calibration packet load mode operation is performed once during every power up.
  - During the calibration packet load mode, the gain/phase parameters stored by the host in a non-volatile memory are configured in to the device.
  - The configured parameters are used, internally in the device, to compensate for gain/phase errors as the RX DSA gain steps are changed during normal operation.

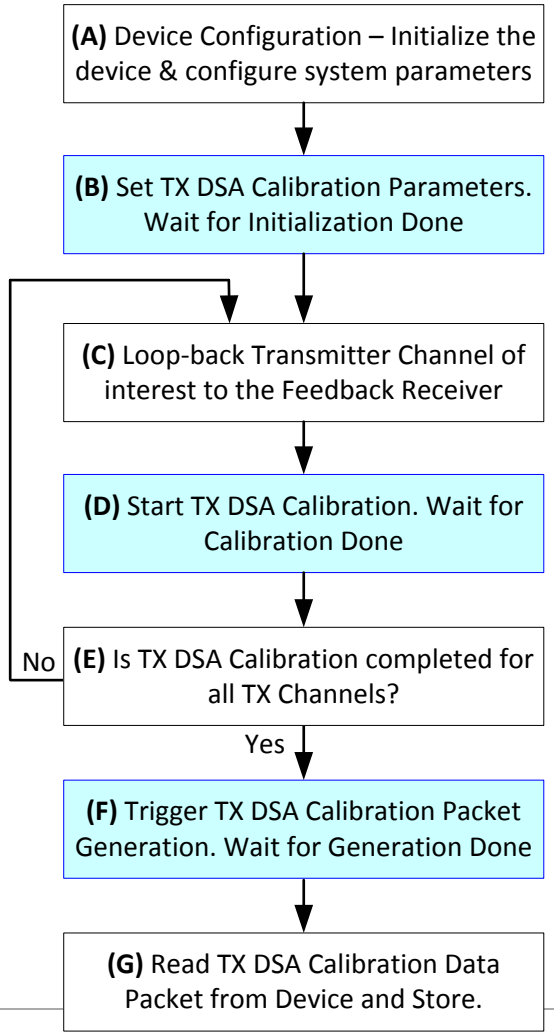
TX DSA – Calibration Mode

- Requirement on TX Loop-back Configuration to FB Receiver:
  - The test signal would be generated internally within the device from each of the transmitters.
  - The host needs to connect the transmit channel for which DSA gain/phase calibration needs to be performed to the feedback channel. This information needs to be provided to the device.
  - The TX DSA gain/phase calibration would be performed sequentially for each of the transmitters.

- Calibration Mode Configuration
  - The specific frequency band of interest for the TX DSA and the interpolation factor (e.g., correct interface rate) need to be used during the calibration mode.
  - After calibration, the gain/phase error parameters are expected to hold only for the frequency band of interest.

TX DSA – Calibration Flowchart (1)

- The TX DSA calibration mode flowchart is illustrated.
  - Additional details on the states of the flowchart are provided in the following slides.



TX DSA – Calibration Flowchart (2)

- State A: The device is brought out of reset by setting the appropriate SPI registers. The device needs to be configured in to the appropriate state with the desired system parameters (Band center frequency, interface rate, etc.)

- State B: The initialization parameters for TX DSA calibration needs to be programmed.
  - An SPI register bit indicating initialization done event needs to be monitored. If the 'Initialization_Done bit' is 1, then proceed to State C.

- State C: The transmitter channel of interest needs to be looped back to the appropriate feed-back channel.

- State D: The appropriate set of SPI registers corresponding to the TX DSA calibration macro needs to be programmed to start the TX DSA calibration procedure.
  - An SPI register bit indicating calibration done event needs to be monitored. If the 'Calibration_Done bit' is 1, then record the 'Error_Status'.
  - Take appropriate action based on the 'Error_Status' (e.g., Signal power too low, Signal power too high, etc.) and then repeat the step to start TX DSA calibration (State D).
  - Otherwise, proceed to State E.

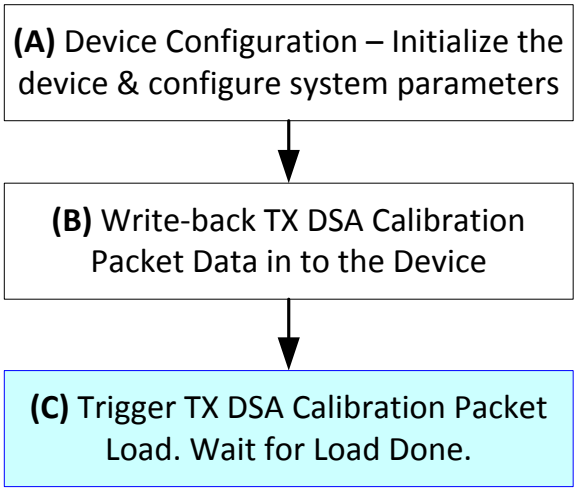
TX DSA – Calibration Flowchart (3)

- State E: Check if TX DSA gain/phase calibration has been completed for all TX channels. If yes, the proceed to State F. Otherwise, proceed to State C.

- State F: Program appropriate SPI registers to trigger the generation of the TX DSA gain/phase calibration packet.
  - An SPI register bit indicating packet generation done event needs to be monitored. If the Generation_Done bit is 1, then record the 'Error_Status'.
  - In case the 'Error_Status' indicates an error, then exit to an "Error State" and record error status indicators. If no error, then proceed to State G.

- State G: Read the TX DSA calibration data packet from the device and store it in non-volatile memory.
  - The size of the calibration data packet (in bytes) can be read from an SPI status register, 'Calibration Packet Size'.

TX DSA – Calibration Packet Load Mode



- State A: The device is brought out of reset by setting the appropriate SPI digital registers. The device needs to be configured in to the appropriate state with the desired system parameters (Band center frequency, interface rate, etc.)
- State B: Write-back the TX DSA calibration data, stored in a non-volatile memory, in to the device.
- State C: Trigger (by SPI writes) load of TX DSA gain/phase calibration packet.
  - An SPI register bit indicating packet load done event needs to be monitored. If the Load_Done bit is 1, then record the 'Error_Status'.
  - In case the 'Error_Status' indicates a packet error, then exit to an "Error State" and record error status indicators. If no error, then calibration packet load mode is complete.

TX DSA – Calibration Data Packet Size

- TX DSA Calibration Packet: The size of the data packet that needs to be stored for the TX DSA calibration, is ~1900 bytes for 4 TX channels, with each programmed to be in dual band mode.
  - The data packet size is ~1200 bytes for single band mode of operation.