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# DTN

# SBC Worst Case Analysis

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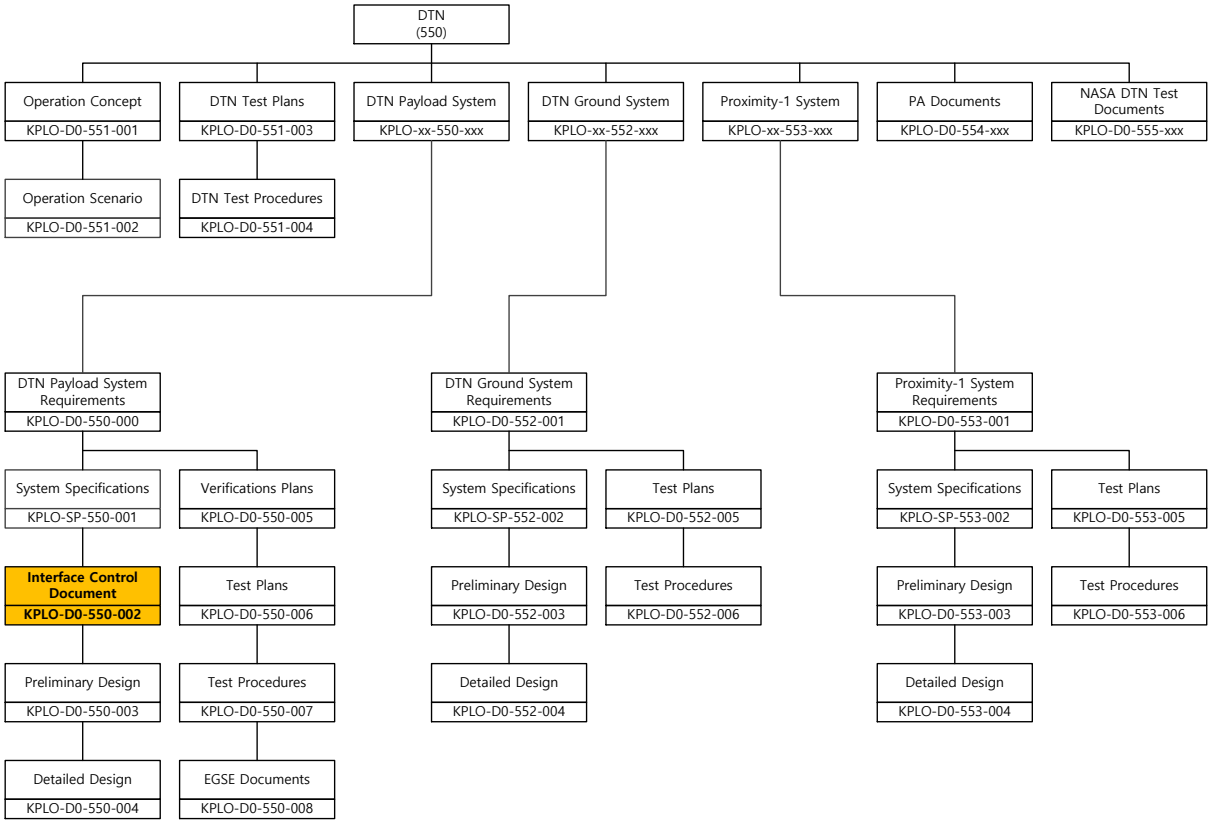
# Documents Tree



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# 1 INTRODUCTION

## 1.1 SCOPE

This document summarizes Part Stress Analysis for the Single Board Computer (SBC) to be developed for the DTN. Part Stress analysis procedures and documentation shall be performed in accordance with PAR

## 1.2 DTN Overview

The mission of DTN is to validate DTN communication protocols by space-link testing through KPLO. So DTN operations are focused on testing the DTN protocols using KPLO space-links.

# 2 DOCUMENTS

## 2.1 APPLICABLE DOCUMENTS

| | Document No. | Title |
|---|---|---|
| AD-1 | KPLO-D0-210-003 | User Requirements Document (KARI) |
| AD-2 | KPLO-D0-524-008 | User Requirements Document (ETRI) |

## 2.2 REFERENCE DOCUMENTS

| | Document No. | Title |
|---|---|---|
| RD-1 | MIL-STD-461E | Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment |
| RD-2 | MIL-STD-462D | Measurements of Electromagnetic Interference Characteristics |
| RD-3 | ECSS-E-ST-10-06C | Space engineering Technical Requirements specification |
| RD-4 | ECSS-Q-60-11A | Derating and End of Life parameter drifts-EEE Components |
| RD-5 | MIL-HDBK-217 | Reliability Prediction for Electronic Equipment |
| RD-6 | ESA PSS-01-301 | Derating Requirement and Application Rules for Electronic Components |

# 3 ACRONYMS AND ABBREVIATIONS

| | |
|---|---|
| AMS | Asynchronous Message Service |
| AOS | Advanced Orbiting System |
| BP | Bundle Protocol |
| BSS | Bundle Streaming Service |
| CCSDS | Consultative Committee for Space Data Systems |
| CFDP | CCSDS File Delivery Protocol |
| DCC | DTN Control Center |
| DTN | Delay(Disruption) Tolerant Network |
| DTNPL | DTN Payload |
| IP | Internet Protocol |
| KPLO | Korea Pathfinder Lunar Orbiter |
| LCM | Lander Communication Model |
| LTP | Liklider Transmission Protocol |
| M&C | Monitor & Control |
| RCM | Rover Communication Model |
| SLE | Space Link Extension |
| TBC | To Be Confirmed |
| TBD | To Be Defined |
| TCP | Transmission Control Protocol |
| UDP | User Datagram Protocol |

# 4 Method

## 4.1 Approach

The Worst Case Analysis (WCA) evaluates the range of functional performance that will be experienced as a result of variations in component and operational tolerances. The analysis assumes that all components are in good working order and that they have assembled correctly.

The WCA is structured in 3 levels :

(i) The evaluation of the components total parametric variation (DP)
(resulting from initial tolerance, temperature, aging and radiation drifts)

(ii) The analysis of circuit functional blocks, based on the DP of the used components

(iii) The analysis of the interface inputs and loads Derating requirements are provided in the clause 6 for each component family.

## 4.2 Parametric variations and tolerances

The total parametric variation of an electronic component depends on variations resulting from a number of causes. Therefore the WCA requires knowledge of the total part variations over the life and environmental extremes of the particular project.

The following effect will be taken into account

(i) Component Initial Tolerance

The tolerance to which the manufacturer has screened the component nominal value.

(ii) Component aging drift (End-of-Life Tolerance)

The aging of electronic parts is a continuing process of chemical change. This parameter is either mentioned as a drift in ppm/year or as an End-Of-Life (EOL) absolute tolerance. The absolute parametric drift is calculated for a lifetime of 10 years.

(iii) Temperature drift

The upper temperature extreme to which parts are to be analyzed shall be based on a thermal analysis for an 85°C design. The lower analysis temperature extreme shall be at -20°C. The WCA is calculated for a nominal temperature of 25°C and a range from -35°C to +85°C.

Temp = -20°C < 25°C < 85°C

The temperature difference are therefore +60°C and -+45°C.

(iv) Radiation drift

Passive components are not subject to degradation at typical space exposures of total dose radiation levels. Semiconductors, however, are susceptible to degradation due to radiation. WCA is calculated for a TID of 13 krad.

## 4.3 Parametric variation calculation

This WCA uses the JPL [1] method EVA (Extreme Value Analysis). EVA is used for both the derivation of part variations and the combinations of circuit parts values. The EVA method yields very conservative results which represent the absolute boundary conditions for the components and the circuit.

The EVA worst case variation (DP = total parametric variation) for a component is the product of the individual parametric variations, as follows:

DP = -1 + (1+dx) * (l+dt) * (l+da) * (l+dr) // total parametric tolerance

where: DP is the total parametric variation

dx is the part initial tolerance

dt is the variation due to temperature (worst case direction)

da is the variation due to aging and drift

dr is the variation due to radiation degradation

All of the above deltas are normalized as variations from their nominal, which is a ±1% initial tolerance yields a dx of 0.01.

## 5. Circuit description

The Configuration of DTN SBC is shown as below (Figure 5-1)

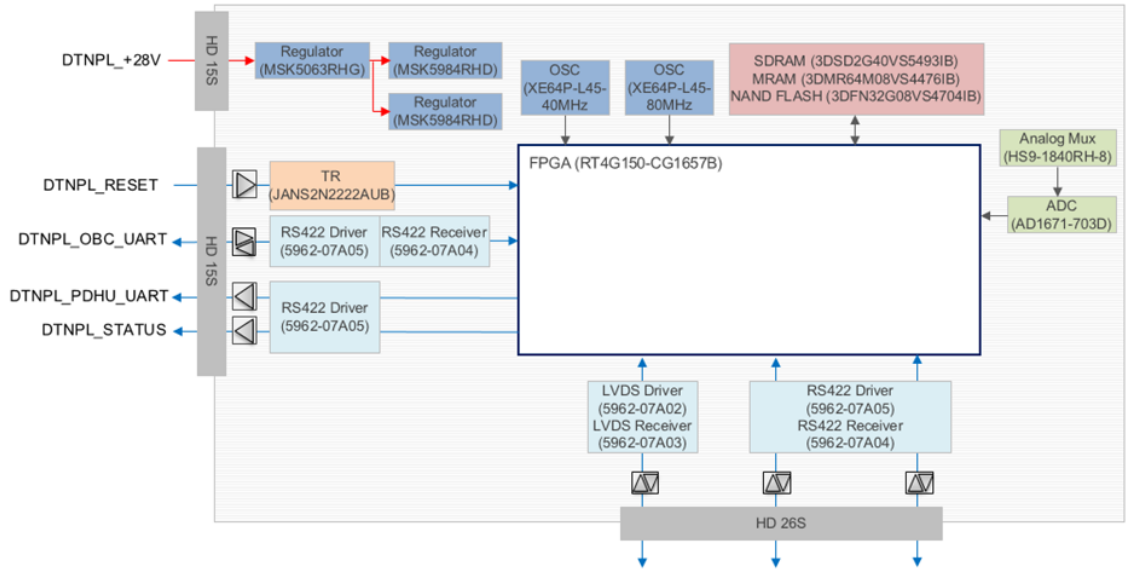


**Figure 5-1 SBC Configuration**

Functional blocks

(i) Power interface

28V의 입력 전원을 내부의 전원으로 변환한다.

(ii) UART I/F

UART 통신을 위해 구성되었다.

(iii) SpW I/F

SpW 통신을 위새 구성되었다.

(iv) Memory I/F

Memory 는 SDRAM, MRAM, NAND FLASH으로 구성되어 있다.

(v) Reset Circuit

Bi-Level CMD로 reset이 발생하면 reset 된다

## 2. 6. Evaluation of components total parametric variation and tolerances

In the following the total parametric variation and drift tolerances for the components are calculated. The calculation is based on the EVA approach as described above. Data is taken from the datasheets of the components. For the different components, the following tolerances and drift parameters are taken into the calculation:

**Table 2-1 Components Parameters and Tolerances**

| Component type | Source of variation | Parameter effected |
|---|---|---|
| Zener Diodes/<br>References | ■ Initial tolerance<br>■ Temperature<br>■ Aging | ■ Reference voltage |
| Resistors | ■ Initial tolerance<br>■ Temperature<br>■ Aging drift / EOL Tolerance | ■ Resistance |
| Capacitors | … | … |
| Linear ICs (OPs) | … | … |
| Digital ICs | … | … |

## 5.1 Oscillator

FPGA 에서 사용되는 클럭 소스원이다.

**Table 2-2 FPGA DataSheet Reference**

| Component | Specification | Nominal Value | Initial Tolerance | Temp. Tolerance | Aging / End of Life (EOL) Tolerance | Radiation Tolerance |
|---|---|---|---|---|---|---|
| XE64S-L63-40.000MHz | MIL-PRF-55310 | 40 MHz | 10 ppm | 50 ppm (max.) | 3 ppm/year | 0 |

DP calculation:

| | Tolerance/Drift | Factor | Total |
|---|---|---|---|
| **Initial Tolerance** | 0.000010 | 1 | 0.000010 |
| **Temperature drift** | 0.000050 | 1 | 0.000050 |
| **Aging drift** | 0.000003 | 10 | 0.000030 |
| **Radiation drift** | 0 | 0 | 0 |
| | | **DP(osc)=** | **0.000090** |

## 5.2 Regulator(Power Circuit)

DCDC Conv.에서 제공을 하지 않는 낮은 전압을 생성하는 파트이다.

**Table 2-3 Regulator DataSheet Reference**

| Component | Output Voltage Tolerance | Line Regulation | Load Regulation | Dropout Voltage |
|---|---|---|---|---|
| MSK5920-1.5KRHS | 0.1 % | 0.1 % | 0.06 % | 0.22 V |
| MSK5920-1.8KRHS | 0.1 % | 0.1 % | 0.06 % | 0.22 V |

DP calculation:

| | **Tolerance/Drift** |
|---|---|
| **Initial Tolerance** | 0.1 |
| Line Regulation | 0.1 |
| Load Regulation | 0.06 |
| **DP(reg)=** | **0.26** |

## 5.3 LVDS

**Table 2-4 LVDS DataSheet Reference**

| Component | Maximum Differential Skew & Jitter |
|---|---|
| 3DLVDS3302VS1609 (Driver) | 0.6 ns |
| 3DLVDS3302VS1609 (Receiver) | 0.2 ns |
| UT54LVDS031LV | 0.4ns |
| UT54LVDS032LV | 0.35ns |

## 5.4 Switching Transistor

Bi-Level CMD 에서 Switch 역할을 하는 TR 이다.

**Table 2-5 Switching Transistor DataSheet Reference**

| Component | Emitter-Base Voltage | Emitter-Base Saturation Voltage |
|---|---|---|
| JANS2N2222UA | 6.0 Vdc | Min 0.6Vdc<br>Max 2.0 Vdc |

## 5.5 Resistor

일반목적으로 사용된 저항이다.

**Table 2-6 Resistor DataSheet Reference**

| Component | Tolerance | **Temp. Tolerance** | **Aging / End of Life (EOL) Tolerance** |
|---|---|---|---|
| M55342K12B---DR | 1 % | 100ppm | 0.5% |

DP calculation:

| | **Tolerance/Drift** | **Factor** | **Total** |
|---|---|---|---|
| **Initial Tolerance** | 0.01 | 1 | 0.01 |
| **Temperature drift** | 0.0001 | 1 | 0.0001 |
| **Aging drift** | 0.005 | 1 | 0.005 |
| | | **DP(res)=** | **0.0151** |

## 5.6 Rectifier diode

역전압 방지용 다이오드이다.

**Table 2-7 Rectifier Diode DataSheet Reference**

| Component | Working Peak Reverse Voltage | Maximum Forward Voltage (@If = 1.0 A) | Maximum Forward Voltage (@If = 2.5 A) |
|---|---|---|---|
| JANS1N5806US | 150 V | 0.875 V | 0.975 V |

# 6. Analysis of functional blocks

## 6.1 Oscillator

### 6.1.1 Drift Variation of 80MHz Oscillator

Calculation of worst case Min/Max :

$\Delta F(t) = F(t)_{NOM} * DP(osc) = \pm 7{,}200$ Hz

$F(t)_{NOM} = 80{,}000{,}000$ Hz

DP(osc) = 0.00009

$F(t) = 80{,}000{,}000 \pm 7{,}200$ Hz

$F(t)_{Min} = 79{,}992{,}800$ Hz

$F(t)_{Max} = 80{,}007{,}200$ Hz

### 6.1.2 Drift Variation of 40MHz Oscillator

Calculation of worst case Min/Max :

$\Delta F(t) = F(t)_{NOM} * DP(osc) = \pm 3{,}600$ Hz

$F(t)_{NOM} = 40{,}000{,}000$ Hz

DP(osc) = 0.00009

$F(t) = 40{,}000{,}000 \pm 3{,}600$ Hz

$F(t)_{Min} = 39{,}996{,}400$ Hz

$F(t)_{Max} = 30{,}003{,}600$ Hz

## 6.2 Regulator(Power Circuit)

### 6.2.1 Output Variation of 1.5V Regulator

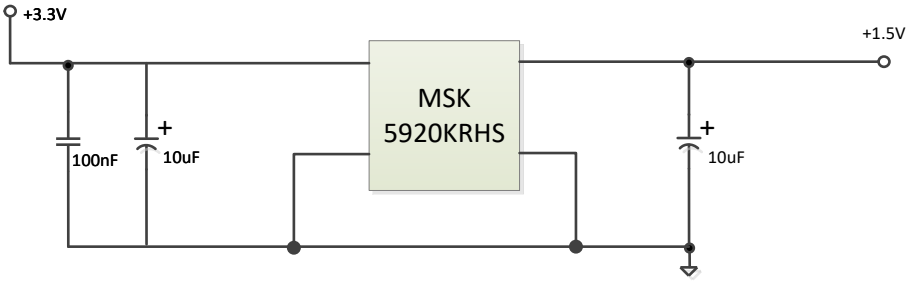


**Figure 6-1 Circuit diagram of the +1.5V Power**

$V(reg1V5)_{NOM}$ = Nominal output Voltage value = 1.5 V

Calculation of worst case Min/Max:

$\Delta V(reg1V5) = V(reg1V5)_{NOM} * DP(reg) = \pm 0.0039$ V

$V(reg1V5)_{NOM} = 1.5$V

DP(reg) = 0.26 %

V(reg1V5) = 1.5 ± 0.0039 V

$F(t)_{Min}$ = 1.4961 V

$F(t)_{Max}$ = 1.5039 V

**Table 6-1 +1.5V Power Circuit Result**

| Input Voltage | Nominal Current | Used for | Linear Regulator | Max in regulator | Dropout | Minimum Input Rating |
|---|---|---|---|---|---|---|
| +3.3V | 0.5 A | Support FPGA | MSK5920-1.5KRHS | +6.5V | 0.22 | +1.72V |

### 6.2.2 Output Variation of 1.8V Regulator

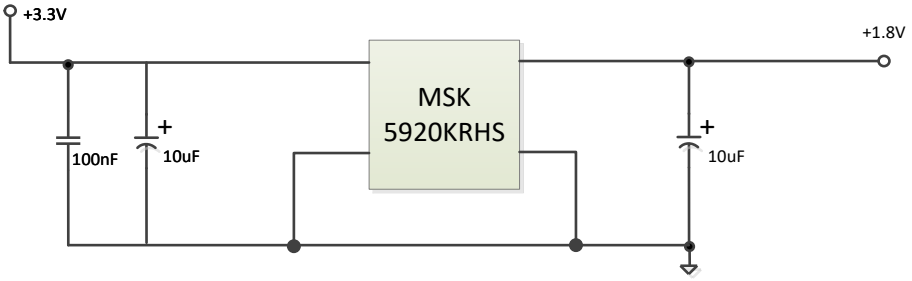


**Figure 6-2 Circuit diagram of the +1.8V Power**

V(reg1V8)$_{NOM}$ = Nominal output voltage value = 1.8 V

Calculation of worst case Min/Max:

ΔV(reg1V8) = V(reg1V8)$_{NOM}$ * DP(reg) = ± 0.00468 V

V(reg1V8)$_{NOM}$ = 1.8V

DP(reg) = 0.26 %

V(reg1V8) = 1.8 ± 0.00468 V

V(t)$_{Min}$ = 1.79532 V

V(t)$_{Max}$ = 1.80468 V

**Table 6-2 +1.8V Power Circuit Result**

| Input Voltage | Nominal Current | Used for | Linear Regulator | Max in regulator | Dropout | Minimum Input Rating |
|---|---|---|---|---|---|---|
| +3.3 V | 0.5 A | FPGA | MSK5920-1.8KRHS | +6.5V | 0.22 | +2.02V |

## 6.3 Memory I/F

### 6.3.1 NAND FLASH Timing

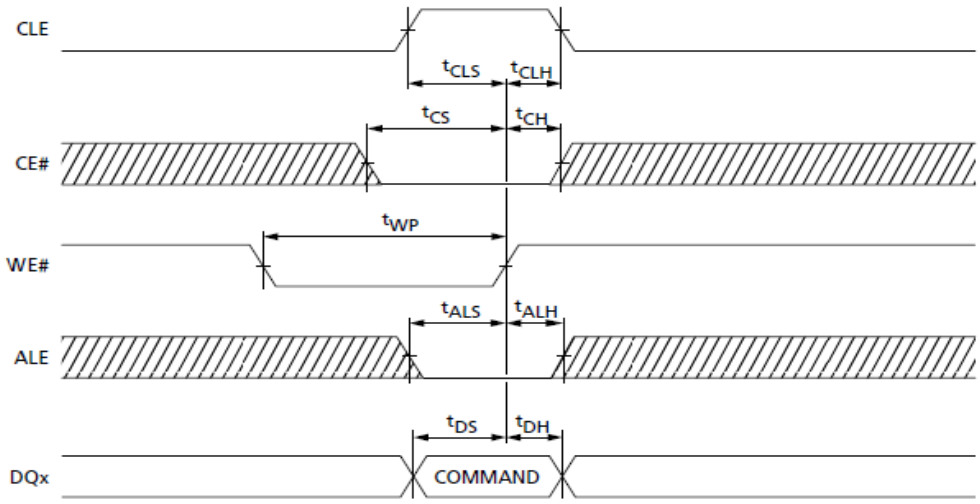


**Figure 6-3 NAND FLASH Timing**

**Table 6-3 NAND FLASH Description**

| Symbol | Description | Min | Max |
|---|---|---|---|
| $t_{CLS}$ | CLE setup time | 10 ns | - |
| $t_{CLH}$ | CLE hold time | 5 ns | - |
| $t_{CS}$ | CE# setup time | 20 ns | - |
| $t_{CH}$ | CE# hold time | 5 ns | - |
| $t_{WP}$ | WE# pulse width | 12 ns | - |
| $t_{ALS}$ | ALE setup time | 10 ns | - |
| $t_{ALH}$ | ALE hold time | 5 ns | - |
| $t_{DS}$ | Data setup time | 10 ns | - |
| $t_{DH}$ | Data hold time | 5 ns | - |

40MHz 의 clock 을 사용하므로 각 ALE, CE#, WE#, Data, CLE minimum pulse width 는 25ns 이다.

### 6.3.2 SDRAM Access Delay

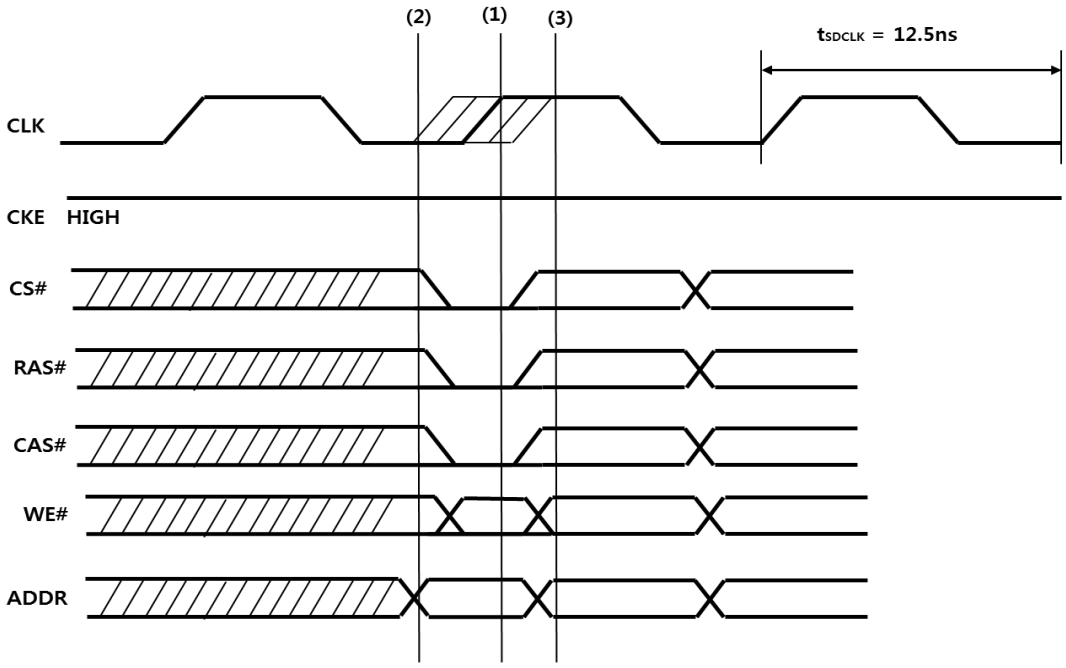


**Figure 6-4 SDRAM CLOCK Jitter**

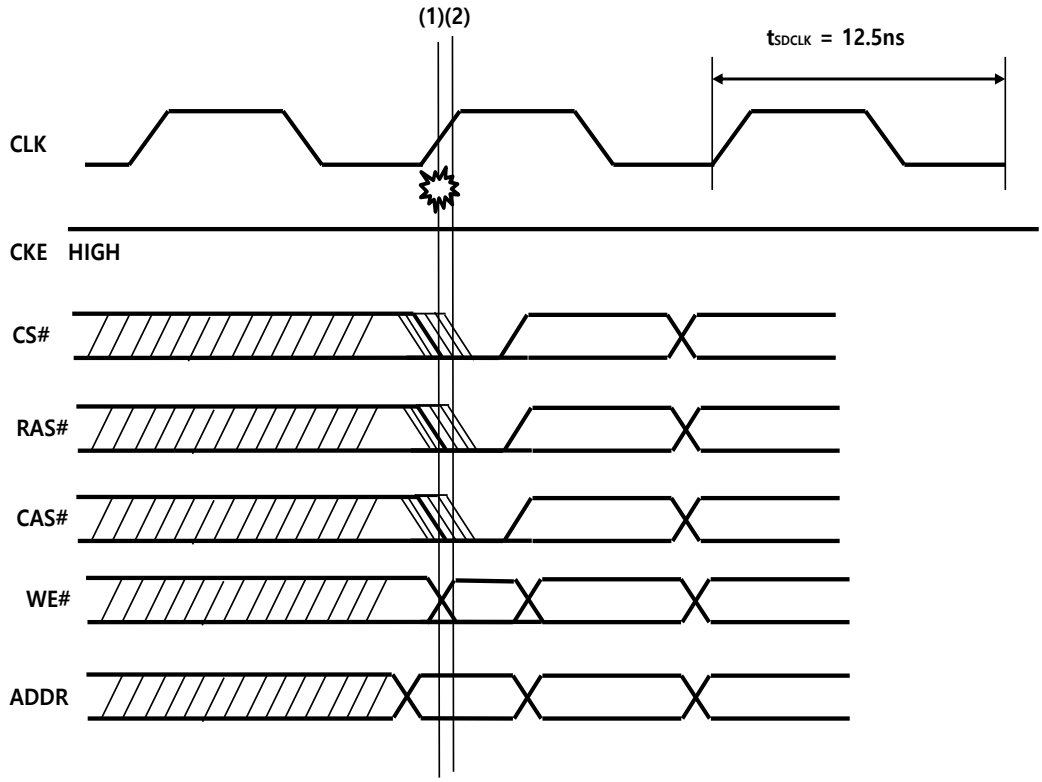


**Figure 6-5 SDRAM Control Signals Jitter**

80MHz 로 SDRAM 동작에서 jitter 는 one cycle = 12.5ns 이다

## 6.4 SpaceWire

### 6.4.1 Synchronization (FPGA)

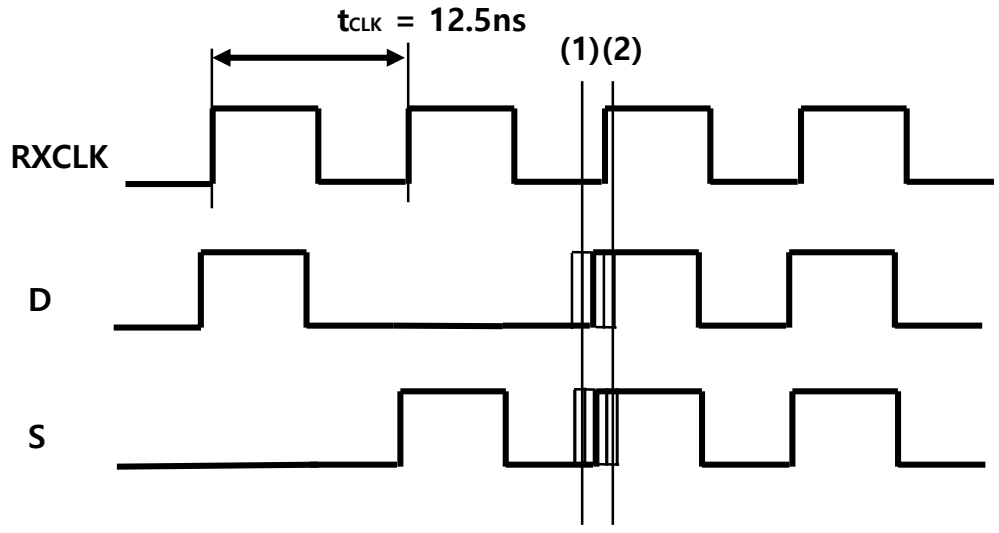


**Figure 6-6 FPGA Synchronization**

FPGA Receive Clock : 80MHz

Link Speed : 80Mbps

**Table 6-4 3DLV3302VS1619 Synchronization**

| | Data Jitter ($t_{Jitter}$) | Strobe Jitter ($t_{Jitter}$) | Skew ($t_{Skew}$) | Minimum Edge Separation ($t_{DS}$) |
|---|---|---|---|---|
| Driver (3DLV3302VS1619) | 0.6 ns | 0.6 ns | 1.0 ns | |
| Cable | 0.5 ns | 0.5 ns | 1.0 ns | |
| Receiver (3DLV3302VS1619) | 0.2 ns | 0.2 ns | 0.5 ns | |
| FPGA | | | | 1 ns |
| Total | 1.3 ns | 1.3 ns | 2.5 ns | 1 ns |

$T_{Jitter\_Max} = t_{Skew} + 2*t_{Jitter} + t_{DS}$

$= 2.5\ ns + 2 * 1.3\ ns + 1\ ns = 6.1\ ns$

**Table 6-5 UT54LVDS031LV Synchronization**

| | Data Jitter ($t_{Jitter}$) | Strobe Jitter ($t_{Jitter}$) | Skew ($t_{Skew}$) | Minimum Edge Separation ($t_{DS}$) |
|---|---|---|---|---|
| Driver (UT54LVDS031LV) | 0.4 ns | 0.4 ns | 0.5 ns | |
| Cable | 0.5 ns | 0.5 ns | 1.0 ns | |
| Receiver (UT54LVDS032LV) | 0.35 ns | 0.35 ns | 0.5 ns | |
| FPGA | | | | 1 ns |
| Total | 1.25 ns | 1.25 ns | 2.0 ns | 1 ns |

$T_{Jitter\_Max} = t_{Skew} + 2*t_{Jitter} + t_{DS}$

$= 2.5\ ns + 2 * 1.25\ ns + 1\ ns = 6.0\ n$

# 7. Summary of component variation

## 7.1 Oscillator

Table 7-1 Oscillator Variation

| Component | Ref. | Nominal Value | IT = Initial Tolerance | DT = Drift Tolerance | DP = Total parametric variance |
|---|---|---|---|---|---|
| XE64S-L63-80.000MHz | OSC | 80,000,000 Hz | IT(osc)= 0.000010 | DT(osc)= 0.000080 | DP(osc)= 0.000090 |
| XE64S-L63-40.000MHz | OSC | 40,000,000 Hz | IT(osc)= 0.000010 | DT(osc)= 0.000080 | DP(osc)= 0.000090 |

## 7.2 Regulator

Table 7-2 Regulator Variation

| Component | Ref. | Nominal Value | IT = Initial Tolerance | DT = Drift Tolerance | DP = Total parametric variance |
|---|---|---|---|---|---|
| MSK5920-1.5KRHS | Reg | 1.5 V | IT(Reg)= 0.1 | DT(Reg)= 0.16 | DP(Reg)= 0.26 |
| MSK5920-1.8KRHS | Reg | 1.8V | IT(Reg)= 0.1 | DT(Reg)= 0.16 | DP(Reg)= 0.26 |

## 7.3 Resistor

Table 7-3 Resistor Variation

| Component | Ref. | Nominal Value | IT = Initial Tolerance | DT = Drift Tolerance | DP = Total parametric variance |
|---|---|---|---|---|---|
| Resistor | res | - | IT(res)=0.01 | DT(res)=0.051 | DP(res)=0.0151 |

## 8. Analysis Results

The circuit is analysed to determine the Min/Max range of functional responses to initial settings, component tolerances, aging and temperature. Circuit Min/Max responses are compared to required responses and the results are categorized in the summary as follows:

OK: The analysed Min/Max response for this functional block is fully within the specification limits.

Caution: The Min or Max response exceeds the specification limits within ±10 %.

Alert: The Min or Max response exceeds the specification limits more than ±10 %.

Analysis results are summarized bellow. Calculation details are provided in the following worksheets.

**Table 8-1 Oscillator and Regulator Analysis**

| Line Item | Functional Block | Component | Parameter Unit | Nominal Value Limit Tolerance | Limit Min / Max | Analyzed Min/ Max | Status |
|---|---|---|---|---|---|---|---|
| 1 | Oscillator | XE64S-L63-80.000MHz | F<br>Hz | 80,000,000<br>(± 0.01 %) | 79,992,000<br>80,008,000 | 79,993,299<br>80,006,800 | Ok |
| 2 | Oscillator | XE64S-L63-40.000MHz | F<br>Hz | 40,000,000<br>(± 0.01 %) | 39,996,000<br>40,004,000 | 79,996,400<br>40,003,600 | Ok |
| 3 | Regulator | MSK5920-1.5KRHS | V | 1.5 | 1.45<br>/ 1.55 | 1.4961<br>/ 1.5039 | OK |
| 4 | Regulator | MSK5920-1.5KRHS | V | 1.5 | 1.75<br>/ 1.85 | 1.795<br>/ 1.804 | OK |

**Table 8-2 Interface Analysis**

| Line Item | Interface | Limit Delay Min/Max | Analyzed Delay Min/Max | Description | Status |
|---|---|---|---|---|---|
| 1 | NAND FLASH | 25ns<br>- | -<br>25ns | | Ok |
| 2 | SDRAM | 10ns<br>- | -<br>12.5ns | | Ok |
| 3 | FPGA SpaceWire Synchronization | -<br>12.5 ns | -<br>6.0 ns | | Ok |

**Table 8-3 Bi-Level TR Analysis**

| Line Item | Functional Block | Component(s) | Parameter Unit | Nominal Value Limit Tolerance | Limit Min / Max | Analyzed Min/ Max | Status |
|---|---|---|---|---|---|---|---|
| 1 | Bi-Level TR | JANS2N2222A UB | Emitter-Base Voltage | - | 0<br>/6 | 2.948<br>/3.038 | OK |