3D PLUS S.A.S.
408, rue Hélène Boucher - Z.I.
78532 BUC Cedex - France

DETAIL SPECIFICATION
32Gbit NAND FLASH – 4G x 8 – 3.3V
SOP 50-05 – Package D4a
Part Number: 3DFN32G08VS4704

3DPA-6780-2

Written by	Responsibility	Date	Signature
S. BERSIN	Product Specification Manager	03/28/2017	

Verified by	Responsibility	Date	Signature
N. FIANT	Design Center Manager	05/11/17	
P.X. WANG	High Rel. Products Manager	04/05/2017	
M.C. VASSAL	Project Group Manager	05/15/2017	
D. BLAIN	Product Assurance Manager	05/16/2017	

Approved by	Responsibility	Date	Signature
P. MAURICE	President	05/16/2017	
P.E. BERTHET	Sales & Marketing Director	05/16/17	

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CHANGE RECORD

Ed./Rev.	Date	Verified and Approved by	Description	Writers
1	07/05/16	NF / PXW / MCV / DB / PM / PEB	Initial document in accordance with Master 3DPA-6810-1	SB
2	03/28/17	NF / PXW / MCV / DB / PM / PEB	Document updated as per Master 3DPA-6810-2 • §1.1 Table 1 and §4.5.4: Web link for assembly recommendations updated • §1.5 Table 4 and §4.1.5.1 Table 13: I_{SB} stand-by current limit increased from 50 to 70 µA	SB

TABLE OF CONTENT

TABLES AND FIGURES

1. GENERAL

1.1. PURPOSE AND SCOPE

The following document details all the activities to be performed to produce and test a 3D PLUS memory module for space application. In particular, it details the ratings, physical and electrical characteristics, tests and inspection data for the 3D PLUS Module 32Gbit NAND FLASH 4G x 8, P/N: 3DFN32G08VS4704 and shall be read in conjunction with the applicable documents, the requirements of which are supplemented herein.

1.2. TYPE VARIANTS

Variants of the module specified herein, which are also covered by this specification, are given in Table 1.

Variant – Part Number	Operating Temperature Range	Grade	Case	Leads Material and Finish
3DFN32G08VS4704 IB	-40 °C to +85 °C	Industrial	SOP 50 pins – Package D4a (see Figure 1)	Kovar Ni+Au plating
3DFN32G08VS4704 IS	-40 °C to +85 °C	Space	SOP 50 pins – Package D4a (see Figure 1)	Kovar Ni+Au plating
3DFN32G08VS4704 MS	-55 °C to +125 °C	Space	SOP 50 pins – Package D4a (see Figure 1)	Kovar Ni+Au plating

Table 1: Component type variants

Note:
These variants are suitable for automatic reflow assembly process qualified by ESA (PID 3300-0546).
Module assembly on board must follow reflow guidelines as defined in:
http://www.3d-plus.com/technical-documentation.php
It shall be noted that recommendations are different for Manual assembly and Automatic reflow.

1.3. MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the module specified herein, are as scheduled in Table 2.

N°	Characteristic	Symbol	Maximum Ratings	Unit	Remark
1	Supply voltage relative to V_{SS}	V_{CC}	-0.6 to +4.6	V	
2	Voltage on any pin relative to V_{SS}	V_{IN}	-0.6 to +4.6	V	
3	Storage Temperature Range	Tstg	-65 to +150	°C	
4	Power Dissipation	P_{DMAX}	2	W	
5	Junction Temperature	T_J	+150	°C	
6	Maximum Body Temperature (short exposure only)	Tmax	+215	°C	Measured at module side level (exposure < 60 s)

Table 2: Absolute maximum ratings (Note 1)

Note:
Permanent module damage, including package and Die, may occur if Absolute maximum ratings are exceeded. Operating Temperature Range may be increased to +125 °C during dynamic Burn-In and Life test. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

1.4. RECOMMENDED OPERATING CONDITIONS

N°	Characteristic	Symbol	Min	Typ	Max	Unit
1	Supply Voltage	V_{CC}	2.7	3.3	3.6	V
2	Ground Voltage	V_{SS}	0	0	0	V
3	Input High Voltage	V_{IH}	0.8 x V_{CC}	-	V_{CC} + 0.3	V
4	Input Low Voltage	V_{IL}	-0.3	-	0.2 x V_{CC}	V
5	Thermal Resistance Junction to Case	$R_{TH(J-C)}$ (Note 1)	-	-	10	°C/W
6	Thermal Resistance Junction to Ambient	$R_{TH(J-A)}$ (Note 2)	-	-	60	°C/W

Table 3: Recommended operating conditions table

Note 1:
In $R_{TH(J-C)}$ (Thermal resistance Junction to Case), Case is defined as the temperature at the module lateral sides, Junction is defined as the Junction Temperature of the top die in the stack.
Note 2:
In $R_{TH(J-A)}$ (Thermal resistance Junction to Ambient), Ambient is defined as the temperature at the bottom of the leads in contact with the board.

1.5. ELECTRICAL CHARACTERISTICS

The table below describes module electrical characteristics based on embedded components manufacturer's test conditions (see **AD3**).

Parameter	Symbol	Conditions	MODULE		Unit
			Min	Max	
Array read current	I_{CC1}	-	-	51	mA
Array program current	I_{CC2}	-	-	51	mA
Erase current	I_{CC3}	-	-	51	mA
I/O burst read current	I_{CC4R}	$t_{RC} = t_{RC\ (min)}$ I_{OUT}= 0 mA	-	11	mA
I/O burst write current	I_{CC4W}	$t_{WC} = t_{WC\ (min)}$	-	11	mA
Bus idle current	I_{CC5}	-	-	6	mA
Current during first RESET command after power-on	I_{CC6}	-	-	11	mA
Standby Current	I_{SB}	V_{CCMAX} #WP = 0 V / V_{CC} #CE = V_{CC} – 0.2	-	280	µA
Input Leakage Current Low	I_{LIL}	V_{CCMAX} V_{IN} = 0 V	-10	+10	µA
Input Leakage Current High	I_{LIH}	V_{CCMAX} V_{IN} = V_{CCMAX}	-10	+10	µA
Output Leakage Current Low	I_{LOL}	V_{CCMAX} V_{OUT} = 0 V	-10	+10	µA
Output Leakage Current High	I_{LOH}	V_{CCMAX} V_{OUT} = V_{CCMAX}	-10	+10	µA

Table 4: Electrical characteristics

1.6. PHYSICAL DIMENSIONS

The physical dimensions of the used package are shown in Figure 1.

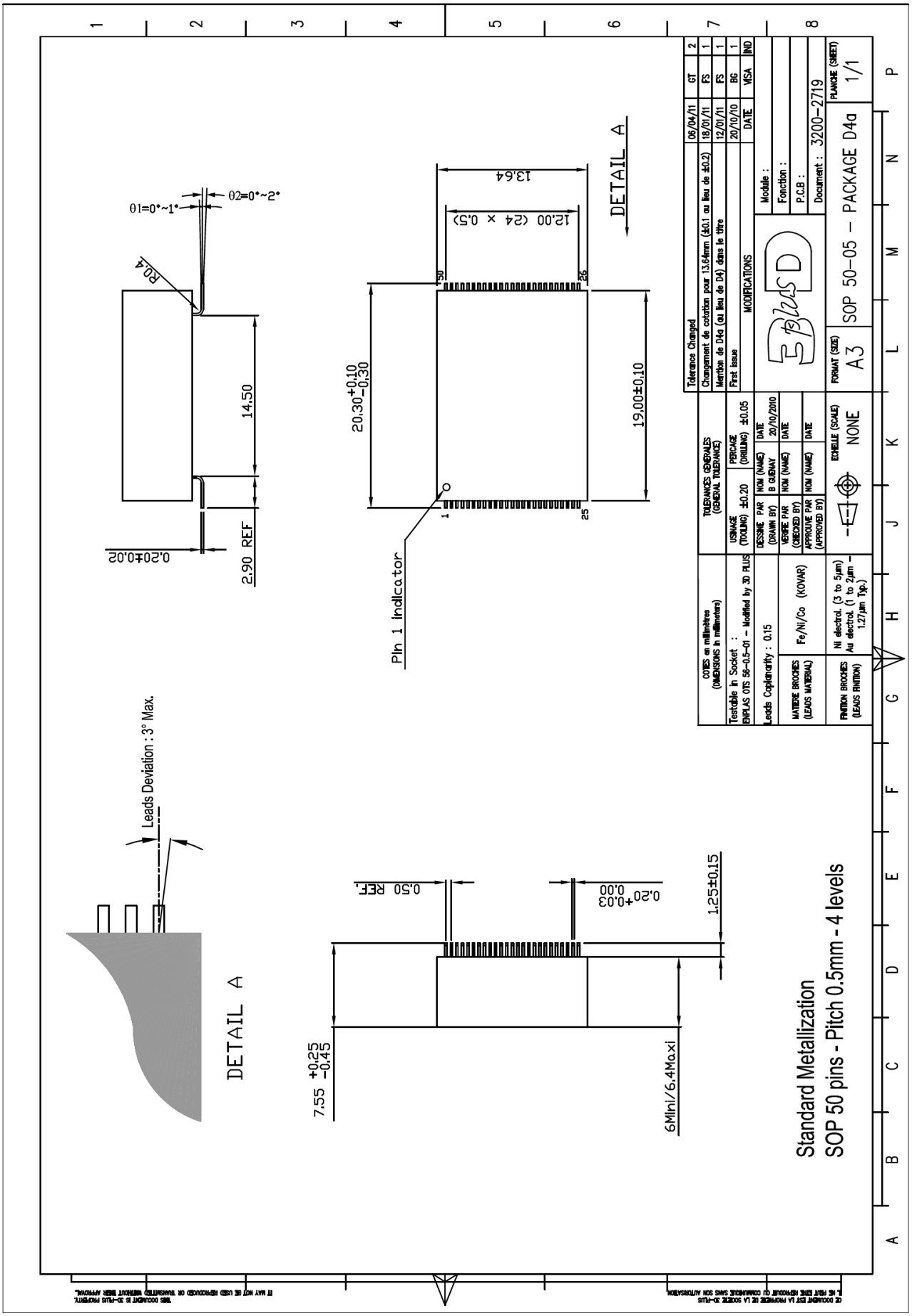

Figure 1: Physical dimensions

1.7. PIN ASSIGNMENT

Pin Nbr	Signal Name	Pin Nbr	Signal Name	Pin Nbr	Signal Name	Pin Nbr	Signal Name	Pin Nbr	Signal Name
1	NC	11	#CE1	21	#WE1	31	I/O1	41	#RE2
2	NC	12	#CE2	22	#WE2	32	I/O2	42	I/O4
3	NC	13	VCC	23	#WE3	33	I/O3	43	I/O5
4	NC	14	VSS	24	NC	34	NC	44	I/O6
5	#RB3	15	#CE3	25	NC	35	VSS	45	I/O7
6	#RB2	16	NC	26	NC	36	VSS	46	#RE3
7	#RB1	17	CLE	27	NC	37	VSS	47	NC
8	#RB0	18	ALE	28	NC	38	VCC	48	NC
9	#RE0	19	#WE0	29	NC	39	VCC	49	NC
10	#CE0	20	#WP	30	I/O0	40	#RE1	50	NC

Table 5: Pins assignment

Case is tied at V_{SS}.

1.8. ELECTRICAL SCHEMATIC

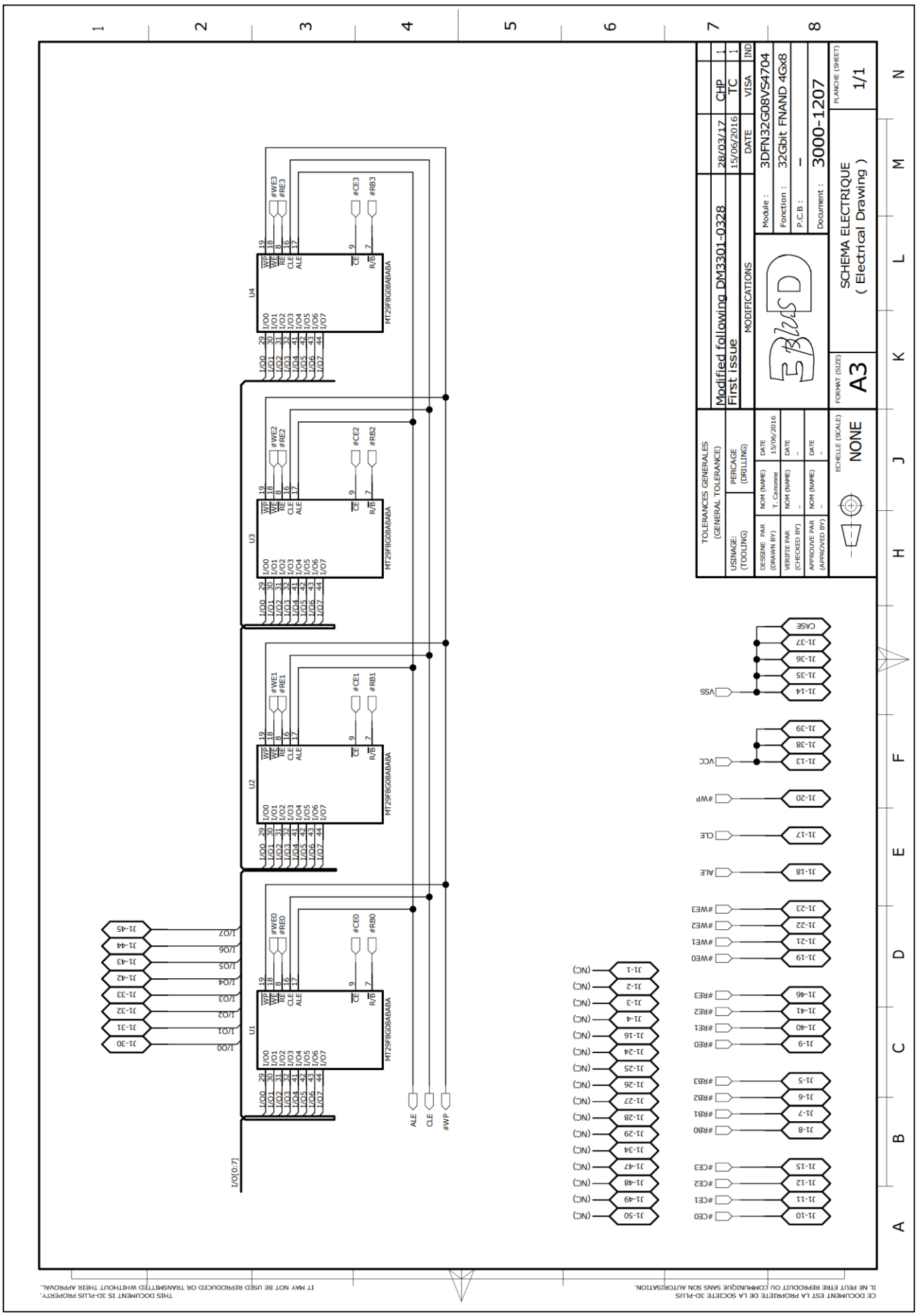

Figure 2: Electrical schematic

1.9. MODULE CAPACITANCE TABLE

For the 32Gbit NAND FLASH module 3DFN32G08VS4704 the capacitance values are (Ta=25 °C, f = 1.0 MHz, V_{IN} = 0 V):

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (#CE[0:3], #WE[0:3], #RE[0:3] and #RB[0:3])	C_{IN}	-	-	10	pF
Input Capacitance (all other inputs)	C_{IN1}	-	-	40	pF
Input/Output Capacitance	$C_{I/O}$	-	-	20	pF

Table 6: Module capacitance values

Note:
Capacitance values are calculated from values specified in **AD3** document.

1.10. MODULE TIMING DIAGRAMS AND MODE SELECTION

Timing waveforms are detailed in the Memory Datasheet **AD3.**

Command	Command Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Valid While Selected LUN is Busy[1]	Valid While Other LUNs are Busy[2]	Notes
Reset Operations							
RESET	FFh	0	–	–	Yes	Yes	
SYNCHRONOUS RESET	FCh	0	–	–	Yes	Yes	
Identification Operations							
READ ID	90h	1	–	–			3
READ PARAMETER PAGE	ECh	1	–	–			
READ UNIQUE ID	EDh	1	–	–			
Configuration Operations							
GET FEATURES	EEh	1	–	–			3
SET FEATURES	EFh	1	4	–			4
Status Operations							
READ STATUS	70h	0	–	–	Yes		
READ STATUS ENHANCED	78h	3	–	–	Yes	Yes	
Column Address Operations							
CHANGE READ COLUMN	05h	2	–	E0h		Yes	
CHANGE READ COLUMN ENHANCED	06h	5	–	E0h		Yes	
CHANGE WRITE COLUMN	85h	2	Optional	–		Yes	
CHANGE ROW ADDRESS	85h	5	Optional	–		Yes	5
Read Operations							
READ MODE	00h	0	–	–		Yes	
READ PAGE	00h	5	–	30h		Yes	6
READ PAGE MULTIPLANE	00h	5	–	32h		Yes	
READ PAGE CACHE SEQUENTIAL	31h	0	–	–		Yes	7
READ PAGE CACHE RANDOM	00h	5	–	31h		Yes	6,7
READ PAGE CACHE LAST	3Fh	0	–	–		Yes	7
Program Operations							
PROGRAM PAGE	80h	5	Yes	10h		Yes	
PROGRAM PAGE MULTI-PLANE	80h	5	Yes	11h		Yes	
PROGRAM PAGE CACHE	80h	5	Yes	15h		Yes	8
Erase Operations							
ERASE BLOCK	60h	3	–	D0h		Yes	
ERASE BLOCK MULTI-PLANE	60h	3	–	D1h		Yes	
Copyback Operations							
COPYBACK READ	00h	5	–	35h		Yes	6
COPYBACK PROGRAM	85h	5	Optional	10h		Yes	
COPYBACK PROGRAM MULTI-PLANE	85h	5	Optional	11h		Yes	

Table 7: TSOP Command set

Note 1:
Busy means RDY = 0.
Note 2:
These commands can be used for interleaved die (multi-LUN) operations (see Interleaved Die (Multi-LUN) Operations.
Note 3:
The READ ID (90h) and GET FEATURES (EEh) output identical data on rising and falling DQS edges.
Note 4:
The SET FEATURES (EFh) command requires data transition prior to the rising edge of CLK, with identical data for the rising and falling edges.
Note 5:
Command cycle #2 of 11h is conditional. See CHANGE ROW ADDRESS (85h) (page 63) for more details.
Note 6:
This command can be preceded by up to one READ PAGE MULTI-PLANE (00h-32h) command to accommodate a maximum simultaneous two-plane array operation.
Note 7:
Issuing a READ PAGE CACHE-series (31h, 00h-31h, 00h-32h, 3Fh) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a READ PAGE (00h-30h) or READ PAGE CACHE-series command; otherwise, it is prohibited.
Note 8:
Issuing a PROGRAM PAGE CACHE (80h-15h) command when the array is busy (RDY = 1,ARDY = 0) is supported if the previous command was a PROGRAM PAGE CACHE (80h-15h) command; otherwise, it is prohibited.

Mode	CE#	CLE	ALE	WE#	RE#	DQx	WP#
Standby	H	X	X	X	X	X	0V/V_{CC} [2]
Bus idle	L	X	X	H	H	X	X
Command input	L	H	L	↑	H	input	H
Address input	L	L	H	↑	H	input	H
Data input	L	L	L	↑	H	input	H
Data output	L	L	L	H	↓	output	X
Write protect	X	X	X	X	X	X	L

Table 8: TSOP Selection mode

Note 1:
#WP should be biased to CMOS LOW or HIGH for standby.
Note 2:
Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

2. DOCUMENTATION

2.1. APPLICABLE DOCUMENTS

The following documents, at the relevant issue in effect on the date of the purchase order placement, form a part of this specification to the extent specified herein, and shall be read in conjunction with it:

- PID 3D PLUS – **ref**. **3300-0546** – **AD1**
- Exigences générales d'approvisionnement et de contrôle d'entrée des composants EEE – **ref**. **3DPA-0350** – **AD2**
- Datasheet Micron MT29F8G08ABABA 1Gbit x 8 NAND Flash Memory, Revision F dated 04/14 EN – **AD3**
- Design file – 32Gbit NAND FLASH – 4G x 8 – 3.3V SOP 50-05 – Package D4a – **ref. 3301-0328** – **AD4**
- EIDP Format Procedure – **ref**. **3DPQ-0050** – **AD5**
- Exigences générales d'approvisionnement et de contrôle d'entrée des Circuits Imprimés – **ref**. **3DPA-0460** – **AD6**
- Procédure de DPA module – **ref. 3DPF-2290** – **AD7**
- Test Plan Nand Flash – **ref. 3DPT-0180** – **AD8**
- Glossaire d'inspection visuelle d'un module 3D PLUS métallisé – **ref. 3300-0776** – **AD9**

2.2. DOCUMENTS IN REFERENCE

The following documents, at the relevant issue in effect on the date of the purchase order placement, form a part of this specification to the extent specified herein, and shall be read in conjunction with it:

- **MIL-STD-883**: "Tests Methods and Procedures for Microelectronics" – **RD1**
- **MIL-PRF-38534**: "Hybrid Microcircuits, General Specifications for" – **RD2**
- **ECSS-Q-ST-60-05**: "Space Product Assurance – Generic procurement Requirements for Hybrid Microcircuits" – **RD3**

2.3. LIST OF ACRONYMS / ABBREVIATIONS

BB: Bad Block
An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC.

DNU: Do Not Use

DPA: Destructive Physical Analysis

EIDP: End Item Data Package

ESD: ElectroStatic Discharge

LAT: Lot Acceptance Test

NC: No Connection

SEL: Single Event Latchup

SEU: Single Event Upset

TID: Total Ionizing Dose

3. PACKAGING REQUIREMENTS

3.1. MECHANICAL REQUIREMENTS

3.1.1. DIMENSION CHECK

The dimensions of the module shall be checked on a sample of 3 pieces per lot in step 12 of the screening (see § 4.1.5). They shall conform to those shown in Figure 1.

3.1.2. WEIGHT

The weight of the module specified herein shall be 4.0 g max.

3.2. CASE, MATERIAL AND FINISHES

3.2.1. CASE

The case corresponds to 3D PLUS Package: SOP 50 leads – Package D4a – See Figure 1.

3.2.2. LEAD MATERIAL AND FINISHES

Lead material: FeNiCo (Kovar)
Finishes: Gold Plating (1 to 2 µm) over Nickel (3 to 5 µm)

3.3. MARKING

3.3.1. GENERAL

Each component shall be marked during laser grooving manufacturing step with:

a) 3D PLUS Logo
b) Pin 1 indicator
c) Part Number
d) Module Serial Number (only for space grade models)
e) Date Code

3.3.2. PIN 1 INDICATOR

An index shall be located at the top of the package in the position defined in Figure 1 to identify pin N°1. The pin numbering shall be read in a counter clockwise order starting with pin N°1.

3.3.3. MODULE PART NUMBER

Each module will be marked with the Module P/N as defined in the left column of Table 1.

3.3.4. MODULE SERIAL NUMBER (ONLY FOR SPACE GRADE MODELS)

Each component will be serialized. Such number will not be re-affected to another part corresponding to the same device.

3.3.5. DATE CODE (YYWW)

Each module will be marked with a date code corresponding to the Year (YY) and the Week (WW) of the laser marking operation date of the first parts of the Module Lot.

The Module Lot is defined by following common elements:

- Homogeneous lots of components.
- Manufacturing & Screening steps of the Module Lot are performed at the same time or within an uninterrupted period of time.

For each module the full traceability (linked to the SN of the module) is given in the EIDP.

4. MEMORY MODULE

4.1. GENERAL

4.1.1. PROCUREMENT OF EEE COMPONENTS

The module is made of 4 memories 8Gbit (1G x 8) NAND FLASH from Micron P/N: MT29F8G08ABABA – Package TSOP type I, Die revision B, procured in accordance with **AD2**.

Micron 8Gbit NAND FLASH are from the same lot if they have the same Date Code and Lot Number.

4.1.2. PROCUREMENT OF PRINTED CIRCUITS BOARD (PCB)

A PCB is used for the leads assembly. It is procured in accordance with **AD6** for type 4.1 PCB.

4.1.3. 8Gbit NAND FLASH TSOP LOT ACCEPTANCE TEST

For each 8Gbit NAND FLASH TSOP lot used for Flight (Space grade), 22 pcs/lot are following the below flow.

Step	Test Description	Test Condition	Quantity (Reject allowed)
1	Component Serialization		22(0)
2	Electrical Measurements (22 Parts) Read & Record at 25°C	According to § 4.1.5.1	22(1)
3	Dynamic Burn-In – 240 h at +125 °C (20 Parts) (Note 1) (Note 2)	MIL-STD-883 Meth.1015 cond.D and according to § 4.1.5.2	
4	Electrical Measurements (22 Parts) Read & Record at 25°C	According to § 4.1.5.1	
5	Electrical Measurements (22 Parts) Read & Record at –55 °C and +125 °C (Note 3)	According to § 4.1.5.4	
6	Parameter Drift Calculation at +25°C	According to § 4.1.5.5	
7	Life Test – 1000 h at +125 °C (20 parts (Note 1) (Note 2)	MIL-STD-883 Meth.1015 cond.D and according to § 4.1.5.2	22(0) or 21(0) if 1 Failure during steps 2, 4, 5 or 6.
8	Electrical Measurements (22 Parts) Read & Record at 25 °C	According to § 4.1.5.1	
9	Electrical Measurements (22 Parts) Read & Record at –55 °C and +125 °C	According to § 4.1.5.4	
10	Parameter Drift Calculation at +25°C	According to § 4.1.5.5	

Table 9: TSOP Lot Acceptance Test flow

Note 1:
If Junction Temperature during life test or Burn-In is above Max. ratings, then Burn-In or Life Test Temperature of the oven is given by:

T_{LT} (°C) = 125 – P_D * $R_{TH(J-C)}$

P_D = V_{CCMAX} * I_{COMP} = Power dissipated during Burn-In or Life Test

$R_{TH(J-C)}$ = Thermal Resistance junction/case of the component.

Note 2:
Only 20 pieces follow the steps 3 & 7. The remaining 2 pieces are used as reference.

4.1.4. MODULE MANUFACTURING

According to 3D PLUS PID (**AD1**) for stacked TSOP (Flow1).

4.1.5. MODULE SCREENING

Each Flight Module will follow the following screening flow:

Step	Test Description	Test Condition
1	Stabilization bake – 72 h at +125 °C	MIL-STD-883 Meth.1008 cond.B
2	Temperature Cycling – 10 Cycles –55 °C / +125 °C	MIL-STD-883 Meth.1010 cond.B
3	Electrical Test at +25 °C with R&R	According to § 4.1.5.1
4	Bad block checking	According to § 4.1.7
5	Dynamic Burn-In – 240 h at +125 °C (Notes 2 and 3)	MIL-STD-883 Meth.1015 cond.D and according to § 4.1.5.2
6	Electrical Test at +25 °C, Tmin and Tmax with R&R	According to § 4.1.5.4
7	Bad block checking	According to § 4.1.7
8	Functional test Full Memory	According to § 4.1.5.3
9	Parameter Drift Calculation	According to § 4.1.5.5
10	PDA Calculation	According to § 4.3
11	External Visual Inspection	3D PLUS Procedure ref. 3300-0776
12	Dimension check	According to § 3.3.1

Table 10: Module screening flow

Note 1:
For industrial grade Models, Screening is limited to steps 1, 2, 6, 7, 11 & 12.
Note 2:
If Junction Temperature during Burn-In is above Max. ratings, then Burn-In Temperature of the oven is given by:
T_{LT} (°C) = 125 – P_D * $R_{TH(J-C)}$
P_D = V_{CCMAX} * I_{COMP} = Power dissipated during Burn-In
$R_{TH(J-C)}$ = Thermal Resistance junction/case of the component.
Note 3:
Burn-In test sequence, according to **AD8**, includes the full memory functional test as per § 4.1.5.3

4.1.5.1. Electrical Measurements at +25 °C

Functional test sequence (Table 11) and electrical measurements (Table 12 and Table 13) are performed per each #CE.

Pattern	Test conditions	Memory	Test Result
ID CHECK	V_{CCMIN} then V_{CCMAX} trc = 100 ns V_{OL} = 1.4 V V_{OH} = 1.4 V	Block0 + 1st block valid from plane 1	PASS/ FAIL (Note1)
ERASE			
VIRGINITY			
WRITE CHECKERBOARD			
READ CHECKERBOARD			
ERASE			
VIRGINITY			
BANK DECODER (Note 2)			

Table 11: Functional patterns

Note 1:
The PASS or FAIL status is recorded in the datalog file
Note 2:
This pattern is not applicable at TSOP level or for module with one single Bank.

The Timing measurements for AC parameters are performed according to **AD8**:

Parameter	Symbol	Test conditions	TSOP		MODULE		Unit
			Min	Max	Min	Max	
#RE access Time (Serial Data Access)	t_{REA}	V_{CCMIN} V_{OL} = 1.4 V V_{OH} = 1.4 V	-	16	-	25	ns
Block Erase time (Note 2)	t_{BERS}		-	3	-	-	ms

Table 12: Timing measurement AC parameters

Note 1:
All these parameters are recorded in the datalog file
Note 2:
Block Erase Time should only be measured at all blocks in the Electrical measurements of FLASH TSOP Lot Acceptance Test at 25 °C according to § 4.1.3. Before the measurement, all blocks should be written in 00h.

Parameter	Symbol	Test conditions	TSOP		MODULE		Unit
			Min	Max	Min	Max	
Array read current	I_{CC1}	V_{CCMAX} t_{RC} = 100 ns	-	50	-	51	mA
Array program current	I_{CC2}	V_{CCMAX} t_{RC} = 100 ns	-	50	-	51	mA
Erase current	I_{CC3}	V_{CCMAX} t_{RC} = 100 ns	-	50	-	51	mA
I/O burst read current	I_{CC4R}	V_{CCMAX} t_{RC} = $t_{RC\ (min)}$ (25 ns); I_{OUT}= 0 mA	-	10	-	11	mA
I/O burst write current	I_{CC4W}	V_{CCMAX} t_{WC} = $t_{WC\ (min)}$ (25 ns)	-	10	-	11	mA
Bus idle current	I_{CC5}	V_{CCMAX} t_{RC} = 100 ns	-	5	-	6	mA
Current during first RESET command after power-on	I_{CC6}	V_{CCMAX} t_{RC} = 100 ns	-	10	-	11	mA
Standby current	I_{SB}	V_{CCMAX} #WP=V_{CC} #CE = V_{CC} - 0.2 V	-	70	-	280	µA
Input Leakage Current Low	I_{LIL}	V_{CCMAX} V_{IN} = 0 V	-10	+10	-10	+10	µA
Input Leakage Current High	I_{LIH}	V_{CCMAX} V_{IN} = V_{CCMAX}	-10	+10	-10	+10	µA
Output Leakage Current Low	I_{LOL}	V_{CCMAX} V_{OUT} = 0 V	-10	+10	-10	+10	µA
Output Leakage Current High	I_{LOH}	V_{CCMAX} V_{OUT} = V_{CCMAX}	-10	+10	-10	+10	µA
Output low voltage	V_{OL}	V_{CCMIN} I_{OL} = 2.1 mA	-	0.4	-	0.4	V
Output high voltage	V_{OH}	V_{CCMIN} I_{OH} = -0.4 mA	2.4	-	2.4	-	V

Table 13: Electrical measurements DC parameters

Note:
All these parameters are recorded in the datalog file.

4.1.5.2. Dynamic Burn-In

The test shall be performed according to the MIL-STD-883, Method 1015 Condition D for Dynamic Burn-In.

Burn-In and life test circuit for TSOP is given in Figure 3.
Burn-In and life test circuit for module is given in Figure 4.

During Burn-In & life test continuous reading are performed and #WP pin is connected at GND through a resistor (R between 1 kΩ to 10 kΩ) (all inadvertent Write/Erase will therefore be avoided).

No.	Characteristic	Symbol	Condition	Unit
1	Clock Frequency	f	125	kHz
2	Power Supply	V_{CC}	V_{CCMAX}	V
3	Oven Temperature	T_{LT} (Note 1)	125	°C
4	Duration time Burn-In	-	240	h
5	Duration time life test	-	1000	h

Table 14: Conditions for dynamic Burn-In and Life Test

Note 1:
If Junction Temperature during life test or burn-In is above Max. ratings, then Burn-In or Life Test Temperature of the oven is given by:

T_{LT} (°C) = 125 – P_D * $R_{TH(J-C)}$
P_D = V_{CCMAX} * I_{COMP} = Power dissipated during Burn-In or Life Test
$R_{TH(J-C)}$ = Thermal Resistance junction/case of the component.

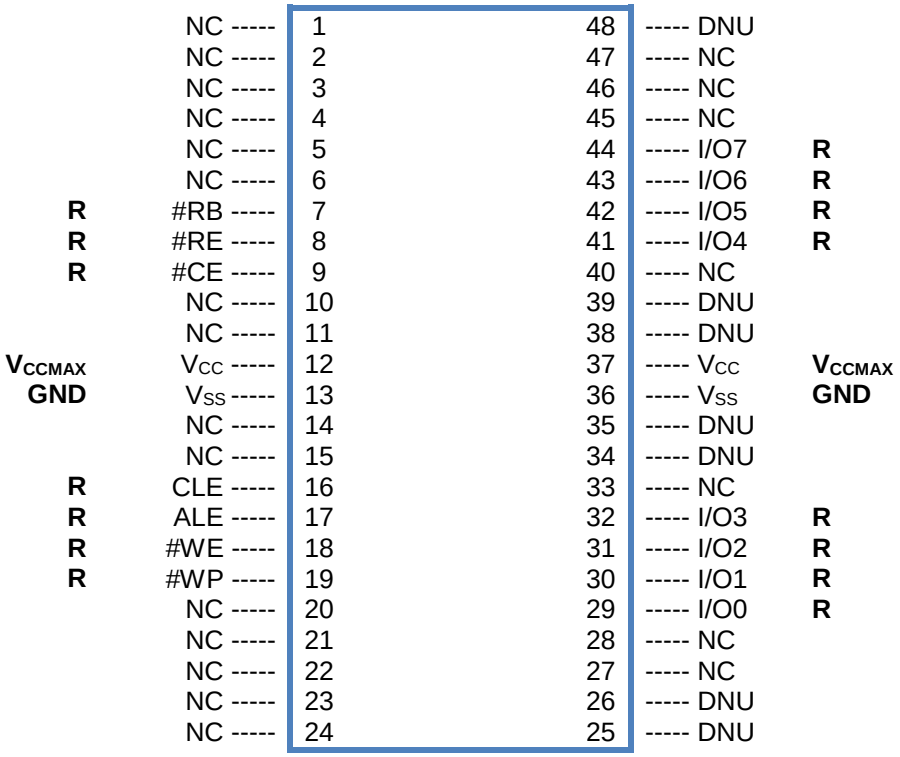

Figure 3: Dynamic Burn-In and Life Test circuit for 8Gbit NAND FLASH TSOP

- Each signal (input or output) is connected to a resistor (R between 1 kΩ to 10 kΩ) to ensure electrical insulation between the different positions.
- Addresses, Data and command signals are connected to the driver board for Burn-In software operation.

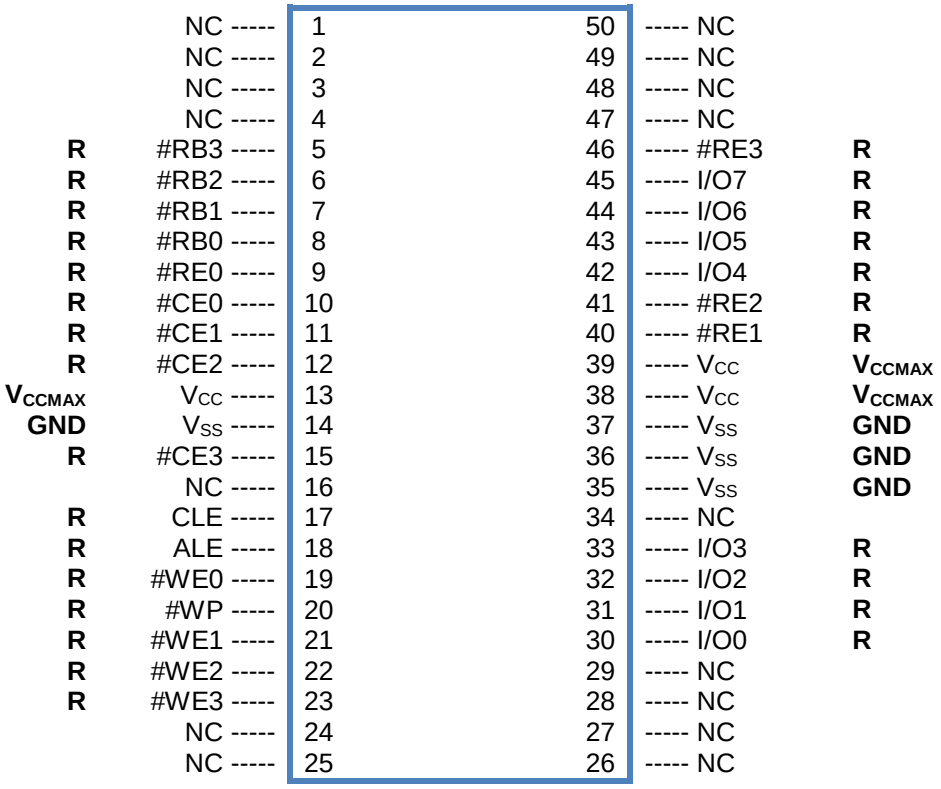

Figure 4: Dynamic Burn-In and Life Test circuit for 32Gbit NAND FLASH memory module

- Each signal (input or output) is connected to a resistor (R between 1 kΩ to 10 kΩ) to ensure electrical insulation between the different positions.
- Addresses, Data and command signals are connected to the driver board for Burn-In software operation.

4.1.5.3. Full Memory Functional Test, +25 °C

All valid blocks should be Functionally tested with the sequences Erase/Program/Read back at +25 °C (according to **AD8**).

4.1.5.4. Electrical Test at Tmin, +25 °C and Tmax

At Tmin and Tmax, the test conditions and limits are identical to those performed at +25 °C.

Grade	Tmin	Tmax
IB and IS	-40 °C	+85 °C
MS	-55 °C	+125 °C

Table 15: Test conditions

The electrical measurements shall be performed with read and record according to § 4.1.5.1 of this document.

4.1.5.5. Parameter Drift Calculation

Parameter drift values between pre and post dynamic Burn-In test measurements at 25 °C shall be calculated and recorded in absolute values for all parameters measured, as per Table 16 of this document.

Parameter	Symbol	Drift Limit TSOP			Drift Limit MODULE		
		Min	Max	Unit	Min	Max	Unit
#RE access Time (Serial Data Access)	t_{REA}	-10	+10	%	-10	+10	%
Array Read Current	I_{CC1}	-10	+10	%	-10	+10	%
Array program current	I_{CC2}	-10	+10	%	-10	+10	%
Erase current	I_{CC3}	-10	+10	%	-10	+10	%
I/O burst read current	I_{CC4R}	-1	+1	mA	-1	+1	mA
I/O burst write current	I_{CC4W}	-2	+2	mA	-4	+4	mA
Bus idle current	I_{CC5}	-1	+1	mA	-2	+2	mA
Current during first RESET command after power-on	I_{CC6}	-1	+1	mA	-2	+2	mA
Standby current	I_{SB}	-5	+5	µA	-20	+20	µA
Input leakage current	$I_{LI(H-L)}$	-5	+5	µA	-5	+5	µA
Output leakage current	$I_{LO(H-L)}$	-5	+5	µA	-5	+5	µA
Output Voltage low level	V_{OL}	-100	+100	mV	-100	+100	mV
Output Voltage high level	V_{OH}	-0.1	+0.1	V	-0.1	+0.1	V

Table 16: Parameter drift calculation

4.1.6. MODULE LOT ACCEPTANCE TEST (NOT APPLICABLE FOR INDUSTRIAL GRADE MODEL)

Some modules that passed module screening will be used for module LAT. Modules with minor visual defects may be accepted for LAT. The table below gives the quantity of modules.
DPA is performed on 1 module that went through life testing.

Module lot size	Sample 1st lot	Sample next lots
1 to 25	2	1
26 to 50	3	2
51 to 90	4	3
>90	5	4

Table 17: LAT module size according to module lot size

The following test flow shall be applied to LAT Modules:

Step	Test Description	Test Condition
1	Dynamic Life Test	Test conditions for Life test detailed in Table 14 Test circuit as per Figure 4
2	Electrical test at Tmin/ +25 °C/ Tmax	As per § 4.1.5.4 of this document
3	Parameter Drift Calculation	As per § 4.1.5.5 of this document
4	Specific Block data retention	160 h at 125 °C unbiased According to **AD8**
5	External Visual Inspection	According to **AD9**
6	DPA (1 module / LAT Lot)	According to **AD7**

Table 18: Module Lot Acceptance Test flow

4.1.7. Bad Block Checking

According to **AD3** specification, the number of valid blocks for each level of TSOP will be superior or equal to 2008.
For industrial grade models, the bad block checking is to verify the total number of bad blocks (less or equal than 160).
For space grade models, bad blocks shall be listed and recorded for each level in a datalog file.

4.2. Failure Criteria

A component shall be considered as having failed if it exhibits one or more of the failure modes described in this subclause.

4.2.1. Parameter Drift Failure

A parameter drift failure is when the changes between the 0 hour and after Burn-In or life test reading, based on the 0 hour reading, are larger than the specified delta limit. The acceptable delta limit is specified in Table 16.

4.2.2. Parameter Limit Failure

A component shall be counted as a limit failure if one or more parameters exceed the limits shown in Table 12 and Table 13 of this specification. Any component which exhibits a limit failure prior to the Burn-In sequence shall be rejected, but not counted when determining lot rejection.

4.2.3. Other Failure

A component shall be counted as a failure in any of the following cases:
- catastrophic failure;
- mechanical failure;
- handling failure;
- lost component.

4.3. Lot Rejection

On the basis of the failure criteria described above (excluding handling failures and lost components) the following criteria will be applied:
- If the number of modules that do not pass the drift calculation at +25 °C, is above +5 %, the lot is rejected.
- If the cumulative number of modules that do not pass the drift calculation at +25 °C and the electrical tests at Tmin, +25 °C, Tmax after Burn-In is above 10 %; the lot is rejected.

4.4. DATA DOCUMENTATION

The Flight modules (Space Grade) are delivered with an End Item Data Package (EIDP), whose format is defined in **AD5.** This document includes a Certificate of Conformance to this specification, and lists all the information regarding:

- Traceability
- Electrical test results
- Screening test results
- Non Conformances

For industrial grade Models, modules are delivered with Certificate of Conformance only.

4.5. PACKING, HANDLING, STORAGE AND MOUNTING REQUIREMENTS

4.5.1. PACKING

Modules are packed in trays.
Each tray is sealed with antistatic bag under vacuum with desiccant sachet.
Each packing is marked with:

- 3D PLUS Logo
- Module description: 32Gbit NAND Flash
- Module P/N: See Table 1
- Quantity

4.5.2. HANDLING

3D PLUS modules must be handled with antistatic gloves and ESD wrist strap.

4.5.3. STORAGE

In order to avoid degradation due to humidity, components must be handled according to the following procedure:

- Storage in sealed bags: the calculated shelf life for dry sealed packed components is 12 months from the pack seal date, when stored in a non-condensing atmospheric environment of < 40 °C and < 90 % RH. Beyond this period, the reconditioning is mandatory; modules shall be baked at 125 °C during 48 hours.
- If the provided sealed bags are opened, please refer to relevant assembly recommendations**.**

4.5.4. BOARD ASSEMBLY

After sealed bag opening, 3D PLUS modules have to be baked 24 hours at 125 °C.
Caution: Device containers cannot be subjected to higher temperatures than their temperature limit indicated on the bag's label.
The use of any scotch tape (e.g. Kapton) on the side of the module during assembly is prohibited.

Module assembly on board must follow reflow guidelines as defined in:
http://www.3d-plus.com/technical-documentation.php
It shall be noted that recommendations are different for manual assembly and automatic reflow.
Module reinforcement, coating and leads tinning operation are also described in these documents.

Module cleaning after assembly must be done with isopropylic alcohol preferentially, or with de-ionized water otherwise. For other cleaning products, please consult 3D PLUS for further information.

4.5.5. ELECTROSTATIC DISCHARGE SENSITIVITY

In order to avoid ESD damage and to guarantee reliable assembling of the 32Gbit NAND FLASH module, 3D PLUS methods and instructions for ESD protections or equivalent have to be applied.
Human Body Model Classification (JS-001-2014) is 2000 V.

4.6. RADIATIONS

4.6.1. GENERIC RADIATION DATA

The following generic radiation tolerance data are available at 3D PLUS:

Parameter	Description
Total Dose Radiation (TID)	> 60 krad (Si)
Single Event Latchup (SEL)	> 62.5 MeV.cm²/mg
Single Event Upset (SEU)	Threshold = 1.3 MeV.cm²/mg Saturated Xsection: 2 x 10^{-10} cm²/bit
Single Event Functional Interruption (SEFI)	Threshold = 3.3 MeV.cm²/mg Saturated Xsection: 1 x 10^{-4} cm²/device

Table 19: Generic radiation data

4.6.2. DEDICATED TID TEST SPECIFICATION

Specific radiation verification test can be performed if purchased.
Conditions described below are only applicable from the date of this specification.

Dose Irradiation Parameter	Condition
Number of parts	11 parts (10 + 1 ref)
Bias	V_{CCMAX} according to Figure 5
Constant Dose Rate	36 – 360 rad(Si)/h
Temperature	24 °C +/- 6 °C
Functional Test	According to § 4.6.2.2
Electrical measurement	According to § 4.6.2.1

Table 20: Dose irradiation conditions

Burn-In	0	1	2	3	4
240 h +125 °C	0 / Initial	30 ±10% krad(Si)	60 0/+10% krad(Si)	A1 (Note 1)	A2 / Final (Note 1)

Table 21: Irradiation steps table

Note 1:
A1 = Annealing step n°1 = 24 hours at 25 °C / part is biased
A2 = Annealing step n°2 = 168 hours at 100 °C / part is biased

4.6.2.1. Electrical Test Conditions

The tests are performed in accordance with TSOP limits indicated in Table 12 & Table 13.
Test conditions are performed in accordance to **AD8**.

4.6.2.2. Functional Test Conditions

Functional patterns used are indicated § 4.1.5.1 Table 11.
Test conditions are performed in accordance to **AD8**.

4.6.2.3. Memory Bias Schematic during TID Exposure

		NC -----	1	48	----- DNU		
		NC -----	2	47	----- NC		
		NC -----	3	46	----- NC		
		NC -----	4	45	----- NC		
		NC -----	5	44	----- I/O7	**R**	**V_{CCMAX}**
		NC -----	6	43	----- I/O6	**R**	**V_{CCMAX}**
		#RB -----	7	42	----- I/O5	**R**	**V_{CCMAX}**
V_{CCMAX}	**R**	#RE -----	8	41	----- I/O4	**R**	**V_{CCMAX}**
V_{CCMAX}	**R**	#CE -----	9	40	----- NC		
		NC -----	10	39	----- DNU		
		NC -----	11	38	----- DNU		
	V_{CCMAX}	V_{CC} -----	12	37	----- V_{CC}	**V_{CCMAX}**	
	GND	V_{SS} -----	13	36	----- V_{SS}	**GND**	
		NC -----	14	35	----- DNU		
		NC -----	15	34	----- DNU		
GND	**R**	CLE -----	16	33	----- NC		
GND	**R**	ALE -----	17	32	----- I/O3	**R**	**V_{CCMAX}**
V_{CCMAX}	**R**	#WE -----	18	31	----- I/O2	**R**	**V_{CCMAX}**
GND	**R**	#WP -----	19	30	----- I/O1	**R**	**V_{CCMAX}**
		NC -----	20	29	----- I/O0	**R**	**V_{CCMAX}**
		NC -----	21	28	----- NC		
		NC -----	22	27	----- NC		
		NC -----	23	26	----- DNU		
		NC -----	24	25	----- DNU		

Figure 5: Memory Bias schematic during TID

- Each signal (input or output) is connected to a resistor (R between 1 kΩ to 10 kΩ) to ensure electrical insulation between the different positions.